

ZXMN3F318DN8

30V SO8 Asymmetrical dual N-channel enhancement mode MOSFET

Summary

Device	$V_{(BR)DSS}$	Q_G (nC)	$R_{DS(on)}$ (Ω)	I_D (A)
Q1	30	12.9	0.024 @ $V_{GS}=10V$	7.3
			0.039 @ $V_{GS}=4.5V$	5.7
Q2	30	9	0.035 @ $V_{GS}=10V$	6
			0.055 @ $V_{GS}=4.5V$	4.8



Description

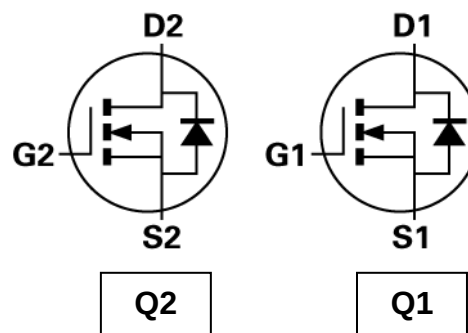
This new generation dual Trench MOSFET from Zetex features low on-resistance achievable with low (4.5V) gate drive.

Features

- Low on-resistance
- 4.5V gate drive capability
- Low profile SOIC package

Applications

- DC-DC Converters
- SMPS
- Load switching
- Motor control
- Backlighting



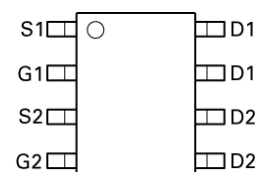
Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMN3F318DN8TA	7	12	500

Device marking

ZXMN

3F318



Pinout – top view

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	LIMIT Q1	LIMIT Q2	UNIT
Drain-Source Voltage	V_{DSS}	30	30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current $V_{GS}=10V$; $T_A=25^\circ C$ (b) $V_{GS}=10V$; $T_A=70^\circ C$ (b) $V_{GS}=10V$; $T_A=25^\circ C$ (a)	I_D	7.3 5.9 5.7	6 4.8 4.6	A
Pulsed Drain Current (c)	I_{DM}	33	25	A
Continuous Source Current (Body Diode) (b)	I_S	3.5	3.3	A
Pulsed Source Current (Body Diode) (c)	I_{SM}	33	25	A
Power Dissipation at $T_A=25^\circ C$ (a) (d) Linear Derating Factor	P_D	1.25 10		W mW/ $^\circ C$
Power Dissipation at $T_A=25^\circ C$ (a) (e) Linear Derating Factor	P_D	1.8 14		W mW/ $^\circ C$
Power Dissipation at $T_A=25^\circ C$ (b) (d) Linear Derating Factor	P_D	2.1 17		W mW/ $^\circ C$
Operating and Storage Temperature Range	T_j, T_{stg}	-55 to +150		$^\circ C$

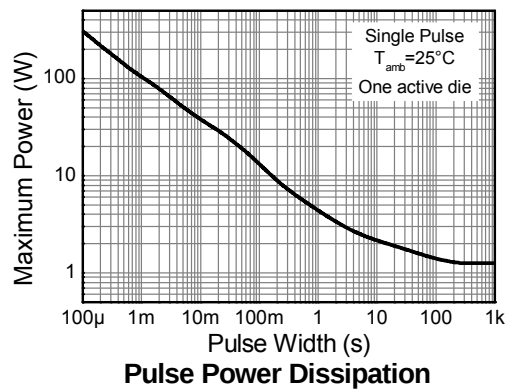
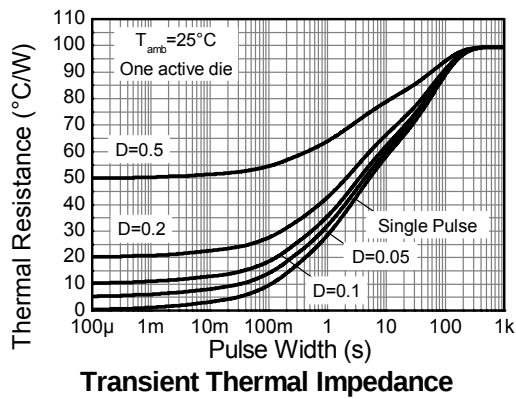
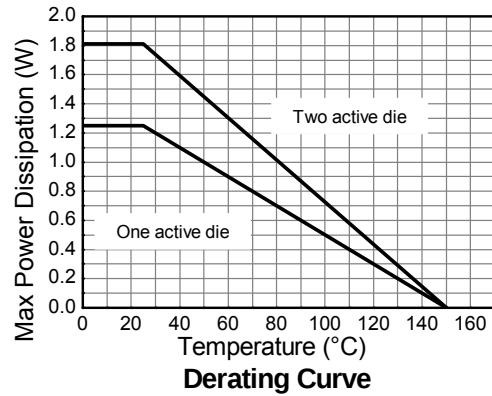
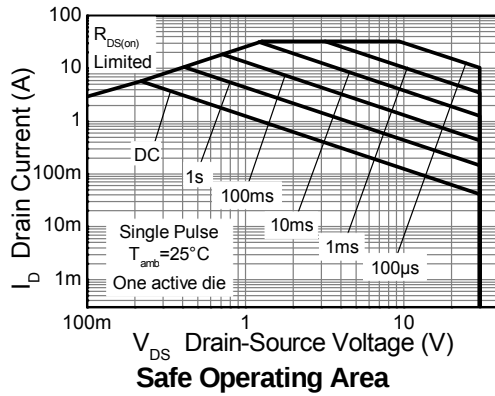
THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient (a) (d)	$R_{\theta JA}$	100	$^\circ C/W$
Junction to Ambient (a) (e)	$R_{\theta JA}$	70	$^\circ C/W$
Junction to Ambient (b) (d)	$R_{\theta JA}$	60	$^\circ C/W$
Junction to Lead (f)	$R_{\theta JL}$	53	$^\circ C/W$

NOTES

- (a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.
- (b) For a device surface mounted on FR4 PCB measured at $t \leq 10$ sec.
- (c) Repetitive rating - 25mm x 25mm FR4 PCB, $D=0.02$, pulse width 300us – pulse width limited by maximum junction temperature.
- (d) For a dual device with one active die.
- (e) For a device with two active die running at equal power.
- (f) Thermal resistance from junction to solder-point (at the end of the drain lead).

Q1 Thermal Characteristics



ZXMN3F318DN8

Q1 ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated).

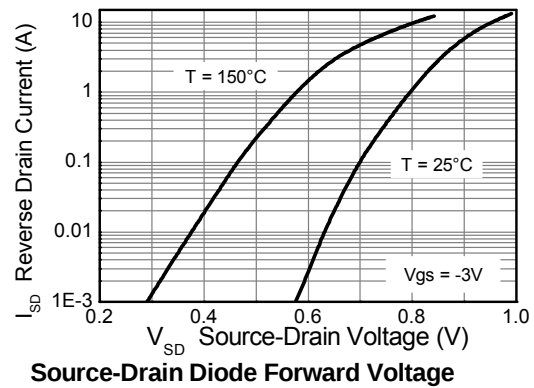
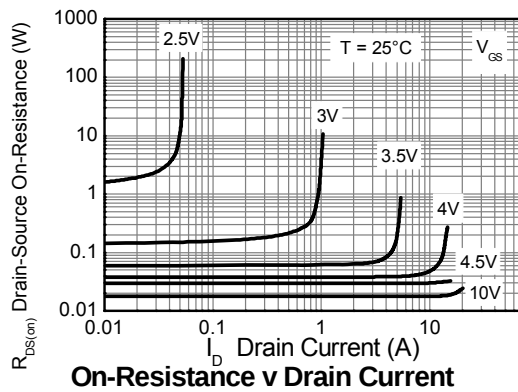
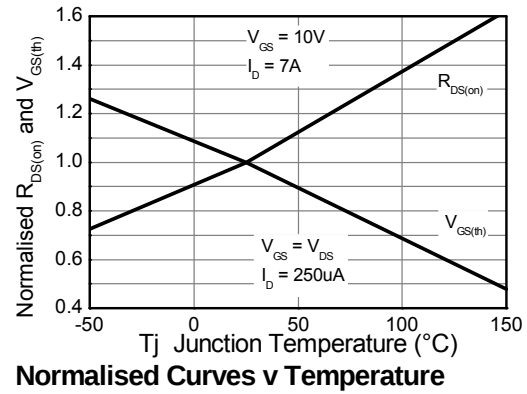
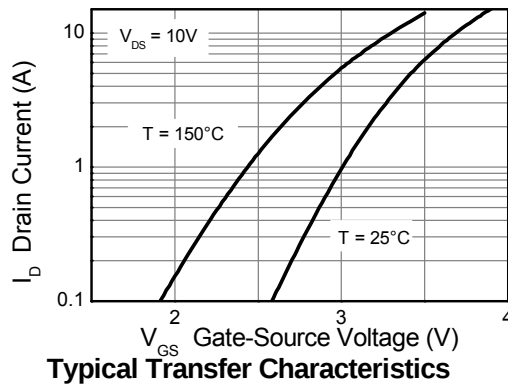
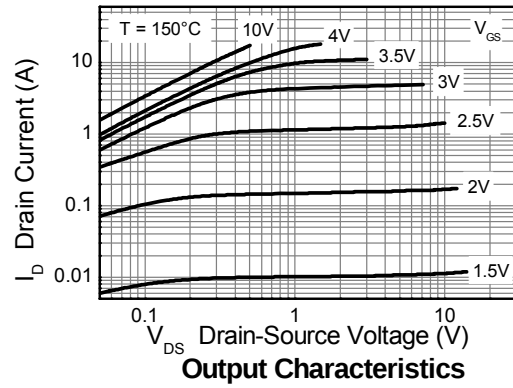
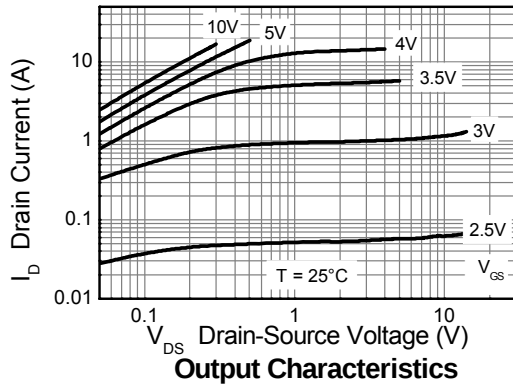
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	30			V	I _D = 250μA, V _{GS} =0V
Zero Gate Voltage Drain Current	I _{DSS}			0.5	μA	V _{DS} = 30V, V _{GS} =0V
Gate-Body Leakage	I _{GSS}			100	nA	V _{GS} =±20V, V _{DS} =0V
Gate-Source Threshold Voltage	V _{GS(th)}	1.0		3.0	V	I _D = 250μA, V _{DS} =V _{GS}
Static Drain-Source On-State Resistance (1)	R _{DS(on)}			0.024	Ω	V _{GS} = 10V, I _D = 7.0A
				0.039	Ω	V _{GS} = 4.5V, I _D = 6.0A
Forward Transconductance (1) (3)	g _{fs}		16.5		S	V _{DS} = 15V, I _D = 7A
DYNAMIC (3)						
Input Capacitance	C _{iss}		608		pF	V _{DS} = 15V, V _{GS} =0V f=1MHz
Output Capacitance	C _{oss}		132		pF	
Reverse Transfer Capacitance	C _{rss}		71		pF	
SWITCHING (2) (3)						
Turn-On-Delay Time	t _{d(on)}		2.9		ns	V _{DD} = 15V, I _D = 1A R _G ≅6.0Ω, V _{GS} = 10V
Rise Time	t _r		3.3		ns	
Turn-Off Delay Time	t _{d(off)}		16		ns	
Fall Time	t _f		8		ns	
Total Gate Charge	Q _g		12.9		nC	V _{DS} = 15V, V _{GS} = 10V I _D = 7A
Gate-Source Charge	Q _{gs}		2.5		nC	
Gate Drain Charge	Q _{gd}		2.52		nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage (1)	V _{SD}		0.82	1.2	V	T _j =25°C, I _S = 1.7A, V _{GS} =0V
Reverse Recovery Time (3)	t _{rr}		12		ns	T _j =25°C, I _S = 2.2A, di/dt=100A/μs
Reverse Recovery Charge (3)	Q _{rr}		4.8		nC	

(1) Measured under pulsed conditions. Pulse width = $300\mu\text{s}$. Duty cycle $\leq 2\%$.

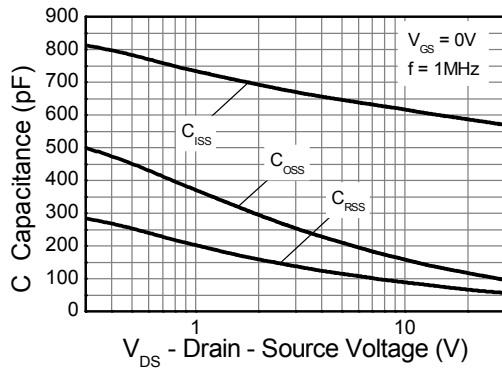
(2) Switching characteristics are independent of operating junction temperature.

(3) For design aid only, not subject to production testing.

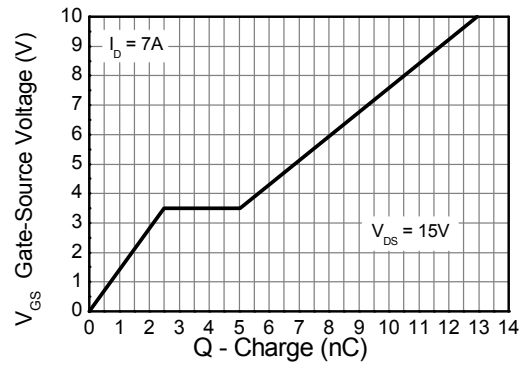
Q1 Typical Characteristics



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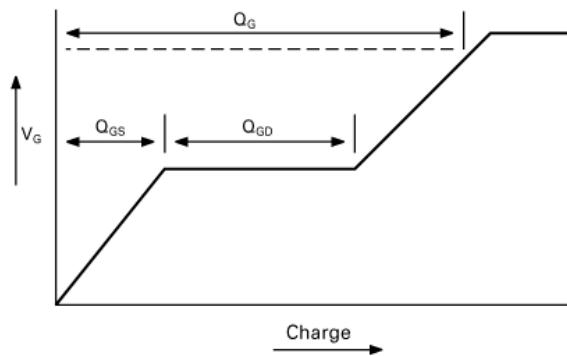


Capacitance v Drain-Source Voltage

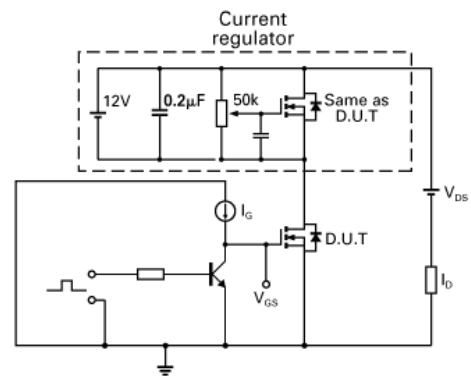


Gate-Source Voltage v Gate Charge

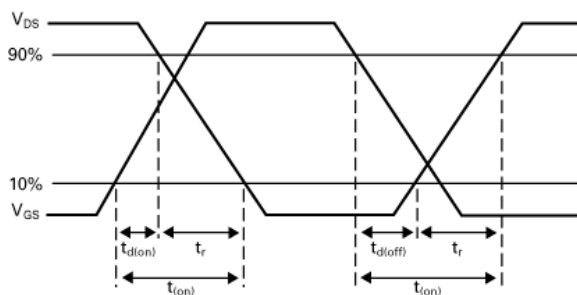
Test Circuits



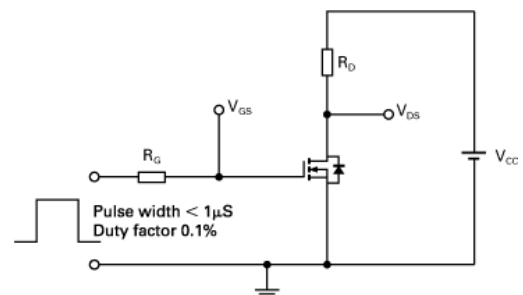
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



Switching time test circuit

ZXMN3F318DN8

Q2 ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated).

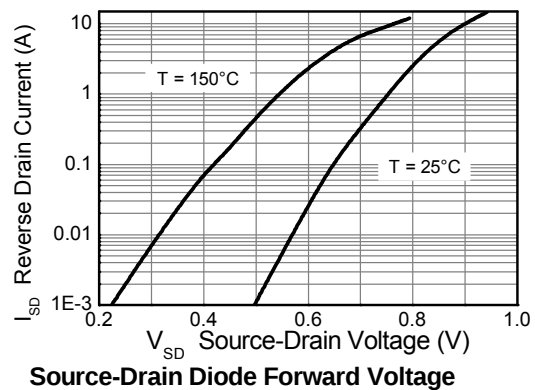
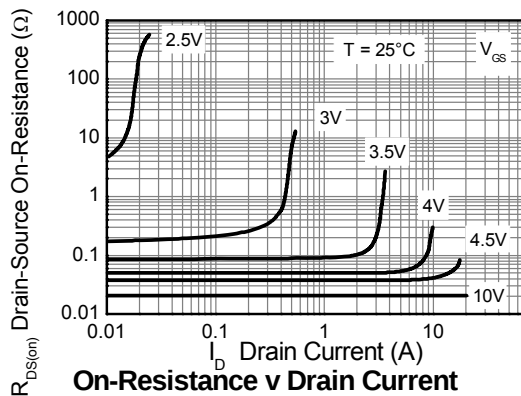
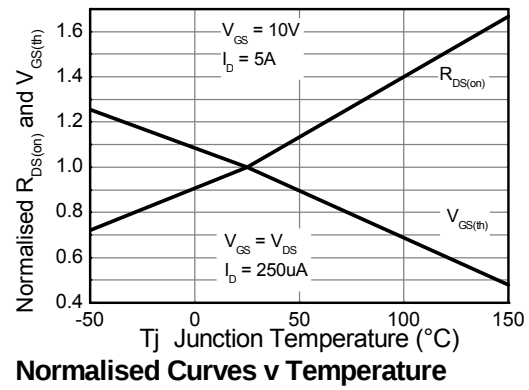
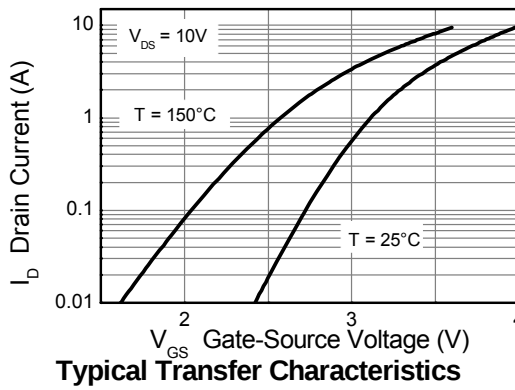
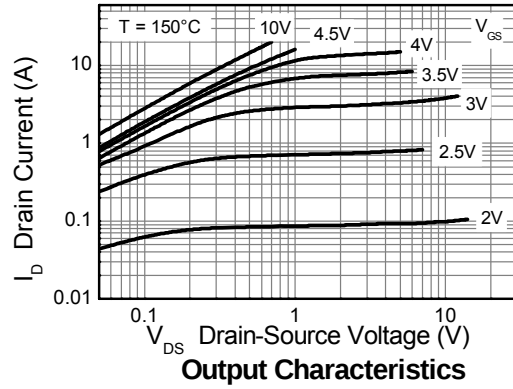
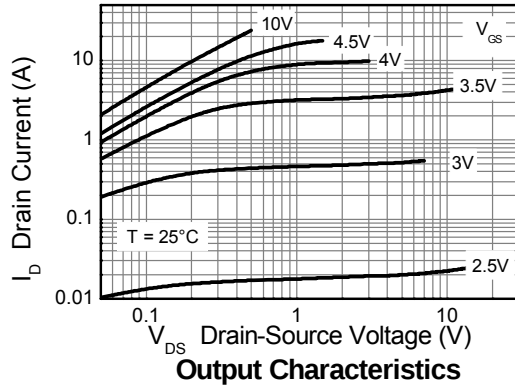
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	30			V	I _D = 250μA, V _{GS} =0V
Zero Gate Voltage Drain Current	I _{DSS}			0.5	μA	V _{DS} = 30V, V _{GS} =0V
Gate-Body Leakage	I _{GSS}			100	nA	V _{GS} =±20V, V _{DS} =0V
Gate-Source Threshold Voltage	V _{GS(th)}	1.0		3.0	V	I _D = 250μA, V _{DS} =V _{GS}
Static Drain-Source On-State Resistance (1)	R _{DS(on)}			0.035	Ω	V _{GS} = 10V, I _D = 5.0A
				0.055	Ω	V _{GS} = 4.5V, I _D = 4A
Forward Transconductance (1) (3)	g _{fs}		11.8		S	V _{DS} = 15V, I _D = 5A
DYNAMIC (3)						
Input Capacitance	C _{iss}		430		pF	V _{DS} = 15V, V _{GS} =0V f=1MHz
Output Capacitance	C _{oss}		101		pF	
Reverse Transfer Capacitance	C _{rss}		56		pF	
SWITCHING (2) (3)						
Turn-On-Delay Time	t _{d(on)}		2.5		ns	V _{DD} = 15V, I _D = 1A R _G ≐6.0Ω, V _{GS} = 10V
Rise Time	t _r		3.3		ns	
Turn-Off Delay Time	t _{d(off)}		11.5		ns	
Fall Time	t _f		6.3		ns	
Total Gate Charge	Q _g		9		nC	V _{DS} = 15V, V _{GS} = 10V I _D = 5A
Gate-Source Charge	Q _{gs}		1.7		nC	
Gate Drain Charge	Q _{gd}		2		nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage (1)	V _{SD}		0.82	1.2	V	T _j =25°C, I _S = 1.7A, V _{GS} =0V
Reverse Recovery Time (3)	t _{rr}		12		ns	T _j =25°C, I _S = 2.1A, di/dt=100A/μs
Reverse Recovery Charge (3)	Q _{rr}		4.9		nC	

1 Measured under pulsed conditions. Pulse width = $300\mu\text{s}$. Duty cycle $\leq 2\%$.

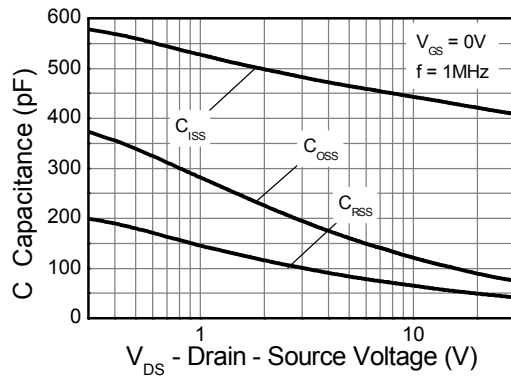
2 Switching characteristics are independent of operating junction temperature.

3 For design aid only, not subject to production testing.

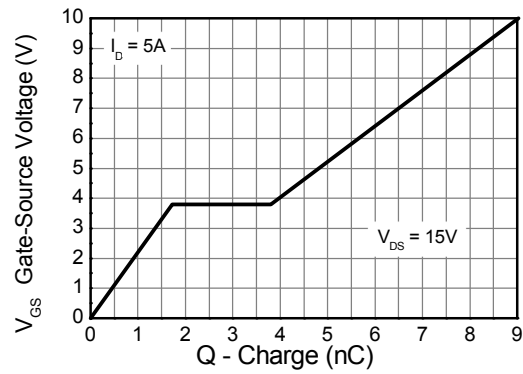
Q2 Typical Characteristics



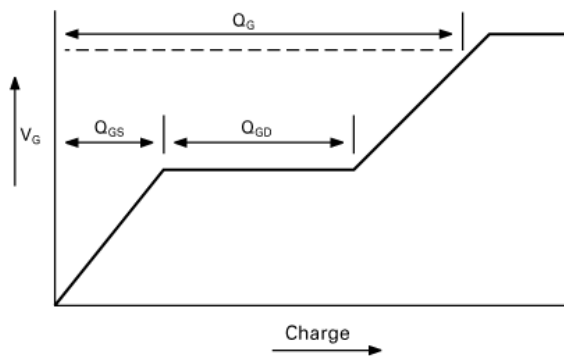
Q2 Typical Characteristics



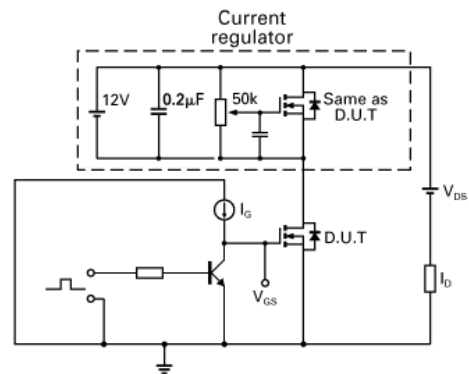
Capacitance v Drain-Source Voltage



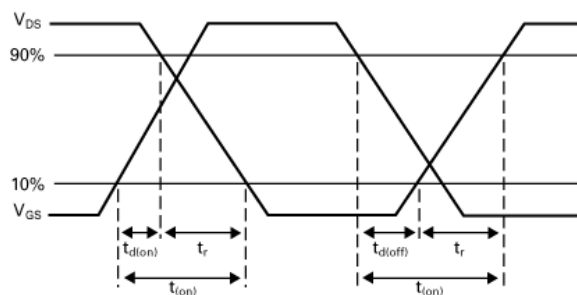
Gate-Source Voltage v Gate Charge



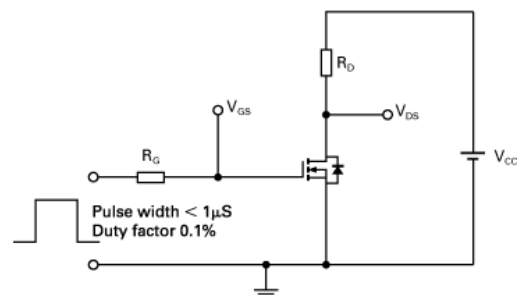
Basic gate charge waveform



Gate charge test circuit



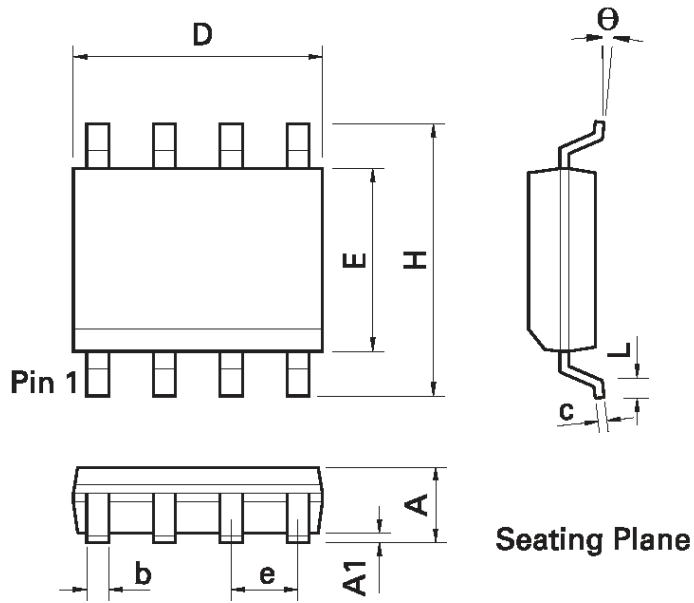
Switching time waveforms



Switching time test circuit

Packaging details – SO8

Package outline



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	Θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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"Active"	Product status recommended for new designs
"Last time buy (LTB)"	Device will be discontinued and last time buy period and delivery is in effect
"Not recommended for new designs"	Device is still in production to support existing designs and production
"Obsolete"	Production has been discontinued

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"Provisional version"	This term denotes a pre-release datasheet. It provides a clear indication of anticipated performance. However, changes to the test conditions and specifications may occur, at any time and without notice.
"Issue"	This term denotes an issued datasheet containing finalized specifications. However, changes to specifications may occur, at any time and without notice.

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