

# NBXDPA018

## 2.5 V / 3.3 V, 155.52 MHz / 311.04 MHz LVDS Clock Oscillator

The NBXDPA018 dual frequency crystal oscillator (XO) is designed to meet today's requirements for 2.5 V and 3.3 V LVDS clock generation applications. The device uses a high Q fundamental crystal and Phase Lock Loop (PLL) multiplier to provide selectable 155.52 MHz or 311.04 MHz, ultra low jitter and phase noise LVDS differential output.

This device is a member of ON Semiconductor's PureEdge™ clock family that provides accurate and precision clock solutions.

Available in 5 mm x 7 mm SMD (CLCC) package on 16 mm tape and reel in quantities of 1000.

### Features

- LVDS Differential Output
- Uses High Q Fundamental Mode Crystal and PLL Multiplier
- Ultra Low Jitter and Phase Noise – 0.5 ps (12 kHz – 20 MHz)
- Selectable Output Frequency – 155.52 MHz (default) / 311.04 MHz
- Hermetically Sealed Ceramic SMD Package
- RoHS Compliant
- Operating Range: 2.5 V  $\pm 5\%$   
3.3 V  $\pm 10\%$
- Total Frequency Stability –  $\pm 50$  ppm
- This is a Pb-Free Device

### Applications

- SONET Line Card
- Networking
- Optical Systems

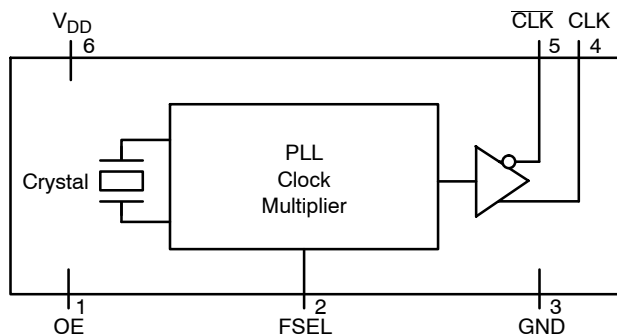
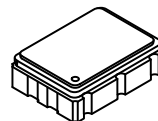


Figure 1. Simplified Logic Diagram



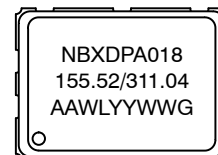
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<http://onsemi.com>



**6 PIN CLCC  
LN SUFFIX  
CASE 848AB**

### MARKING DIAGRAM



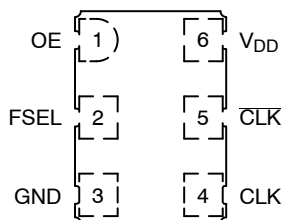
NBXDPA018 = NBXDPA018 ( $\pm 50$  PPM)  
155.52/311.04 = Output Frequency (MHz)  
AA = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G or ■ = Pb-Free Package

### ORDERING INFORMATION

| Device          | Package             | Shipping†            |
|-----------------|---------------------|----------------------|
| NBXDPA018LN1TAG | CLCC-6<br>(Pb-Free) | 1000/<br>Tape & Reel |
| NBXDPA018LNHTAG | CLCC-6<br>(Pb-Free) | 100/<br>Tape & Reel  |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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**Figure 2. Pin Connections** (Top View)

**Table 1. PIN DESCRIPTION**

| Pin No. | Symbol                  | I/O                        | Description                                                                                                                      |
|---------|-------------------------|----------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| 1       | OE                      | LVTTL/LVCMOS Control Input | Output Enable Pin. When left floating pin defaults to logic HIGH and output is active. See OE pin description Table 2.           |
| 2       | FSEL                    | LVTTL/LVCMOS Control Input | Output Frequency Select Pin. Pin will default to logic HIGH when left open. See Output Frequency Select pin description Table 3. |
| 3       | GND                     | Power Supply               | Ground 0 V                                                                                                                       |
| 4       | CLK                     | LVDS Output                | Non-Inverted Clock Output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.            |
| 5       | $\overline{\text{CLK}}$ | LVDS Output                | Inverted Clock Output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.                |
| 6       | V <sub>DD</sub>         | Power Supply               | Positive power supply voltage. Voltage should not exceed 2.5 V $\pm 5\%$ or 3.3 V $\pm 10\%$ .                                   |

**Table 2. OUTPUT ENABLE TRI-STATE FUNCTION**

| OE Pin     | Output Pins |
|------------|-------------|
| Open       | Active      |
| HIGH Level | Active      |
| LOW Level  | High Z      |

**Table 3. OUTPUT FREQUENCY SELECT**

| FSEL Pin                      | Output Frequency (MHz) |
|-------------------------------|------------------------|
| Open<br>(pin will float high) | 155.52                 |
| HIGH Level                    | 155.52                 |
| LOW Level                     | 311.04                 |

**Table 4. ATTRIBUTES**

| Characteristic                                             | Value          |
|------------------------------------------------------------|----------------|
| Input Default State Resistor                               | 170 k $\Omega$ |
| ESD Protection Human Body Model<br>Machine Model           | 2 kV<br>200 V  |
| Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test |                |

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

**Table 5. MAXIMUM RATINGS**

| Symbol           | Parameter                   | Condition 1         | Condition 2 | Rating      | Units |
|------------------|-----------------------------|---------------------|-------------|-------------|-------|
| V <sub>DD</sub>  | Positive Power Supply       | GND = 0 V           |             | 4.6         | V     |
| I <sub>out</sub> | LVDS Output Current         | Continuous<br>Surge |             | 25<br>50    | mA    |
| T <sub>A</sub>   | Operating Temperature Range |                     |             | -40 to +85  | °C    |
| T <sub>stg</sub> | Storage Temperature Range   |                     |             | -55 to +120 | °C    |
| T <sub>sol</sub> | Wave Solder                 | See Figure 6        |             | 260         | °C    |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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**Table 6. DC CHARACTERISTICS** ( $V_{DD} = 2.5\text{ V} \pm 5\%$  or  $V_{DD} = 3.3\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) (Note 2)

| Symbol          | Characteristic                                                           | Conditions                                         | Min.         | Typ. | Max.         | Units         |
|-----------------|--------------------------------------------------------------------------|----------------------------------------------------|--------------|------|--------------|---------------|
| $I_{DD}$        | Power Supply Current                                                     |                                                    |              | 85   | 105          | mA            |
| $V_{IH}$        | OE and FSEL Input HIGH Voltage                                           |                                                    | 2000         |      | $V_{DD}$     | mV            |
| $V_{IL}$        | OE and FSEL Input LOW Voltage                                            |                                                    | GND – 300    |      | 800          | mV            |
| $I_{IH}$        | Input HIGH Current                                                       | OE<br>FSEL                                         | –100<br>–100 |      | +100<br>+100 | $\mu\text{A}$ |
| $I_{IL}$        | Input LOW Current                                                        | OE<br>FSEL                                         | –100<br>–100 |      | +100<br>+100 | $\mu\text{A}$ |
| $\Delta V_{OD}$ | Change in Magnitude of $V_{OD}$ for Complementary Output States (Note 3) |                                                    | 0            | 1    | 25           | mV            |
| $V_{OS}$        | Offset Voltage                                                           |                                                    | 1125         |      | 1375         | mV            |
| $\Delta V_{OS}$ | Change in Magnitude of $V_{OS}$ for Complementary Output States (Note 3) |                                                    | 0            | 1    | 25           | mV            |
| $V_{OH}$        | Output HIGH Voltage                                                      | $V_{DD} = 2.5\text{ V}$<br>$V_{DD} = 3.3\text{ V}$ |              | 1425 | 1600         | mV            |
| $V_{OL}$        | Output LOW Voltage                                                       | $V_{DD} = 2.5\text{ V}$<br>$V_{DD} = 3.3\text{ V}$ | 900          | 1075 |              | mV            |
| $V_{OD}$        | Differential Output Voltage                                              |                                                    | 250          |      | 450          | mV            |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Measurement taken with outputs terminated with 100 ohm across differential pair. See Figure 5.
- Parameter guaranteed by design verification not tested in production.

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**Table 7. AC CHARACTERISTICS** ( $V_{DD} = 2.5\text{ V} \pm 5\%$  or  $V_{DD} = 3.3\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) (Note 4)

| Symbol            | Characteristic                                                                                         | Conditions                       | Min. | Typ.      | Max.     | Units  |
|-------------------|--------------------------------------------------------------------------------------------------------|----------------------------------|------|-----------|----------|--------|
| $f_{CLKOUT}$      | Output Clock Frequency                                                                                 | FSEL = HIGH                      |      | 155.52    |          | MHz    |
|                   |                                                                                                        | FSEL = LOW                       |      | 311.04    |          |        |
| $\Delta f$        | Frequency Stability – NBXDPA018                                                                        | (Note 5)                         |      |           | $\pm 50$ | ppm    |
| $\Phi_{NOISE}$    | Phase-Noise Performance<br>$f_{CLKout} = 155.52\text{ MHz}/311.04\text{ MHz}$<br>(See Figures 3 and 4) | 100 Hz of Carrier                |      | -103/-107 |          | dBc/Hz |
|                   |                                                                                                        | 1 kHz of Carrier                 |      | -120/-114 |          | dBc/Hz |
|                   |                                                                                                        | 10 kHz of Carrier                |      | -127/-122 |          | dBc/Hz |
|                   |                                                                                                        | 100 kHz of Carrier               |      | -128/-122 |          | dBc/Hz |
|                   |                                                                                                        | 1 MHz of Carrier                 |      | -135/-129 |          | dBc/Hz |
|                   |                                                                                                        | 10 MHz of Carrier                |      | -158/-154 |          | dBc/Hz |
| $t_{jit}(\Phi)$   | RMS Phase Jitter                                                                                       | 12 kHz to 20 MHz                 |      | 0.5       | 0.75     | ps     |
| $t_{jitter}$      | Cycle to Cycle, RMS                                                                                    | 1000 Cycles                      |      | 4         | 8        | ps     |
|                   | Cycle to Cycle, Peak-to-Peak                                                                           | 1000 Cycles                      |      | 16        | 35       | ps     |
|                   | Period, RMS                                                                                            | 10,000 Cycles                    |      | 2         | 4        | ps     |
|                   | Period, Peak-to-Peak                                                                                   | 10,000 Cycles                    |      | 11        | 20       | ps     |
| $t_{OE/OD}$       | Output Enable/Disable Time                                                                             |                                  |      |           | 200      | ns     |
| $t_{DUTY\_CYCLE}$ | Output Clock Duty Cycle<br>(Measured at Cross Point)                                                   |                                  | 48   | 50        | 52       | %      |
| $t_R$             | Output Rise Time (20% and 80%)                                                                         |                                  |      | 115       | 400      | ps     |
| $t_F$             | Output Fall Time (80% and 20%)                                                                         |                                  |      | 115       | 400      | ps     |
| $t_{start}$       | Start-up Time                                                                                          |                                  |      | 1         | 5        | ms     |
|                   | Aging                                                                                                  | 1 <sup>st</sup> Year             |      |           | 3        | ppm    |
|                   |                                                                                                        | Every Year After 1 <sup>st</sup> |      |           | 1        | ppm    |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Measurement taken with outputs terminated with 100 ohm across differential pair. See Figure 5.
- Parameter guarantees 10 years of aging. Includes initial stability at 25°C, shock, vibration and first year aging.

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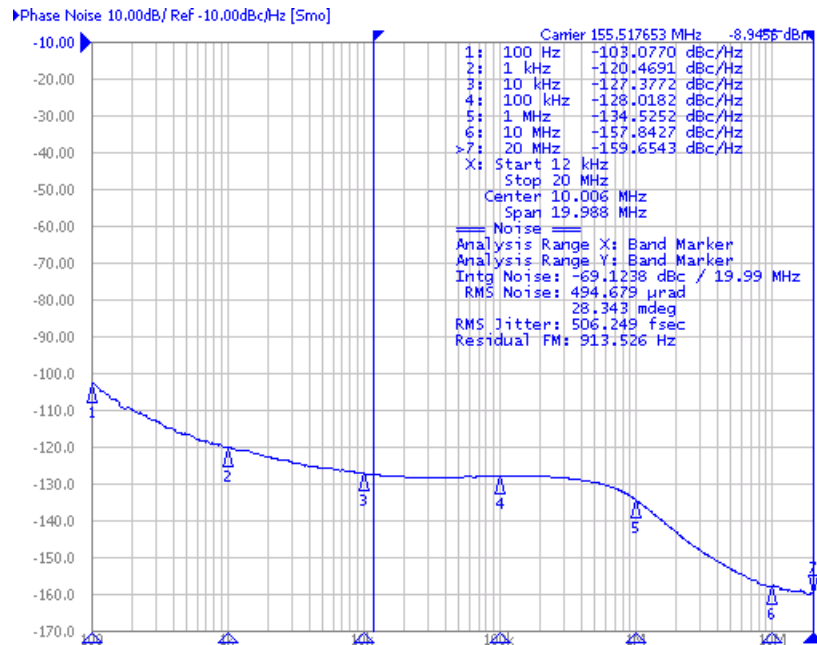


Figure 3. Typical Phase Noise Plot at 155.52 MHz

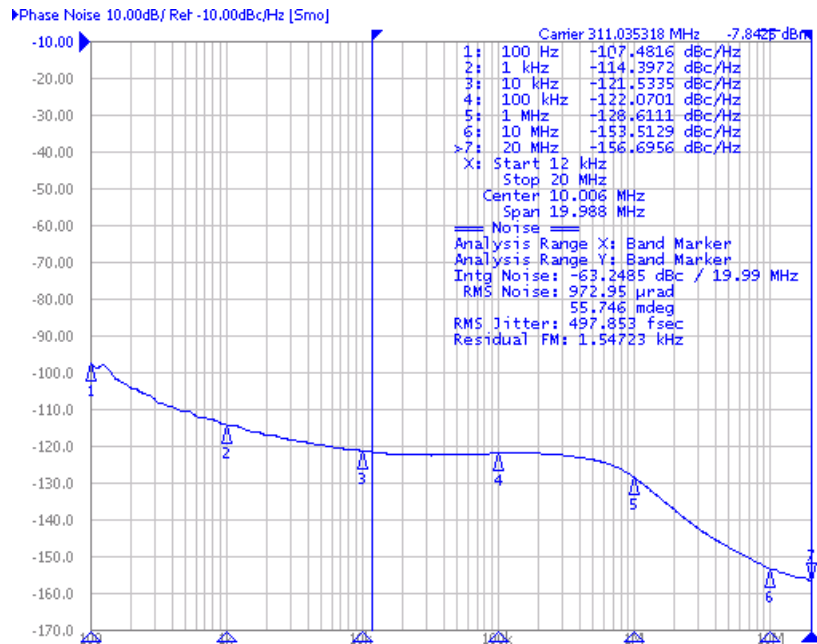


Figure 4. Typical Phase Noise Plot at 311.04 MHz

Table 8. RELIABILITY COMPLIANCE

| Parameter                    | Standard    | Method                                    |
|------------------------------|-------------|-------------------------------------------|
| Shock                        | Mechanical  | MIL-STD-833, Method 2002, Condition B     |
| Solderability                | Mechanical  | MIL-STD-833, Method 2003                  |
| Vibration                    | Mechanical  | MIL-STD-833, Method 2007, Condition A     |
| Solvent Resistance           | Mechanical  | MIL-STD-202, Method 215                   |
| Resistance to Soldering Heat | Mechanical  | MIL-STD-203, Method 210, Condition I or J |
| Thermal Shock                | Environment | MIL-STD-833, Method 1001, Condition A     |
| Moisture Resistance          | Environment | MIL-STD-833, Method 1004                  |

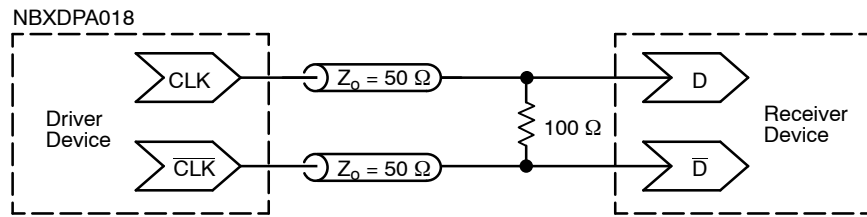


Figure 5. Typical Termination for Output Driver and Device Evaluation

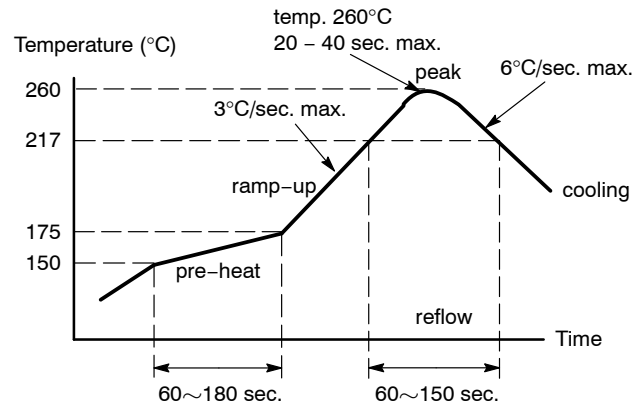
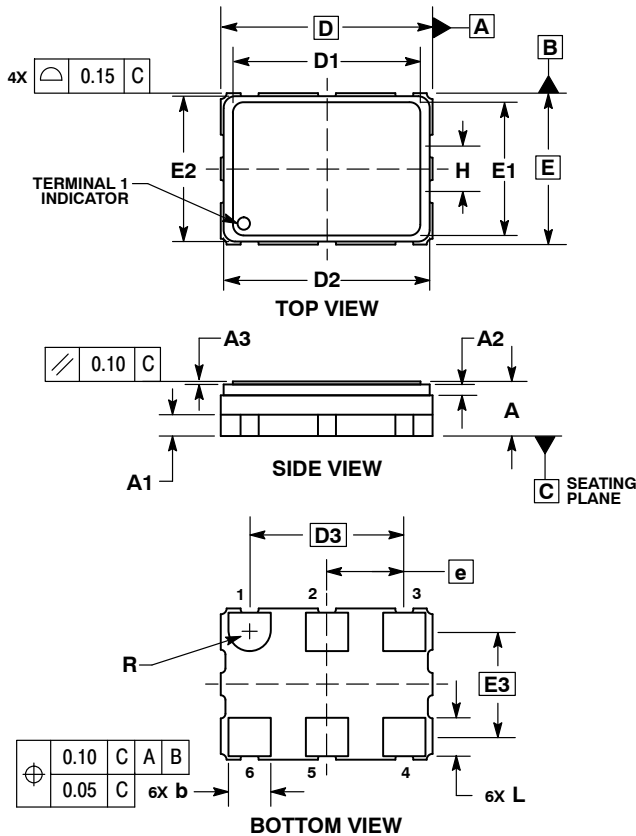


Figure 6. Recommended Reflow Soldering Profile

# NBXDPA018

## PACKAGE DIMENSIONS

6 PIN CLCC, 7x5, 2.54P  
CASE 848AB-01  
ISSUE C

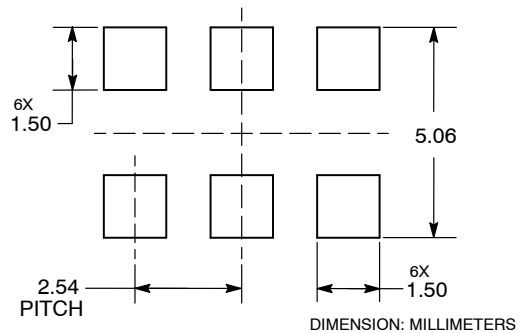


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

| DIM | MILLIMETERS |          |      |
|-----|-------------|----------|------|
|     | MIN         | NOM      | MAX  |
| A   | 1.70        | 1.80     | 1.90 |
| A1  |             | 0.70 REF |      |
| A2  |             | 0.36 REF |      |
| A3  | 0.08        | 0.10     | 0.12 |
| b   | 1.30        | 1.40     | 1.50 |
| D   |             | 7.00 BSC |      |
| D1  | 6.17        | 6.20     | 6.23 |
| D2  | 6.66        | 6.81     | 6.96 |
| D3  |             | 5.08 BSC |      |
| E   |             | 5.00 BSC |      |
| E1  | 4.37        | 4.40     | 4.43 |
| E2  | 4.65        | 4.80     | 4.95 |
| E3  |             | 3.49 BSC |      |
| e   |             | 2.54 BSC |      |
| H   |             | 1.80 REF |      |
| L   | 1.17        | 1.27     | 1.37 |
| R   |             | 0.70 REF |      |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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