

NUP4114UCLW1

Transient Voltage Suppressors

ESD Protection Diodes with Low Clamping Voltage

The NUP4114UCLW1 transient voltage suppressor is designed to protect high speed data lines from ESD. Ultra-low capacitance and high level of ESD protection makes this device well suited for use in USB 2.0 high speed applications.

Features

- Low Capacitance < 0.6 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
0.082" x 0.078" (2.10 mm x 1.25 mm)
- Low Body Height: 0.043" (1.10 mm)
- Response Time is Typically < 1.0 ns
- IEC61000-4-2 Level 4 ESD Protection
- This is a Pb-Free Device

Typical Applications

- LVDS
- USB 2.0
- HDMI
- Display Port

Mechanical Characteristics:

CASE: Void-free, transfer-molded, thermosetting plastic
Epoxy Meets UL 94 V-0

LEAD FINISH: 100% Matte Sn (Tin)

MOUNTING POSITION: Any

QUALIFIED MAX REFLOW TEMPERATURE: 260°C

Device Meets MSL 1 Requirements

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T _J	-40 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T _L	260	°C
IEC 61000-4-2 (ESD)	Contact Air	±8 ±15	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

See Application Note AND8308/D for further description of survivability specs.



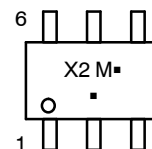
ON Semiconductor®

<http://onsemi.com>



SC-88
W1 SUFFIX
CASE 419B

MARKING DIAGRAM



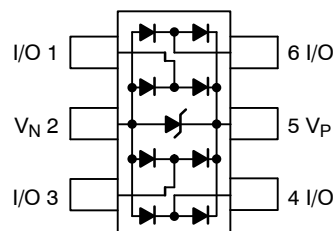
X2 = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

Device	Package	Shipping
NUP4114UCLW1T2G	SC-88 (Pb-Free)	3000 / Tape & Reel

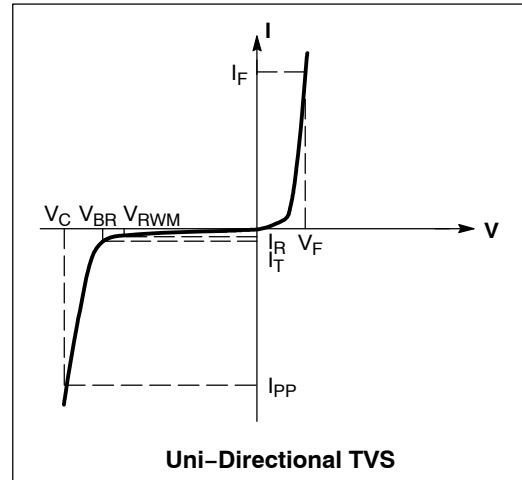
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ $V_R = 0$ and $f = 1.0$ MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	(Note 1)			5.5	V
Breakdown Voltage	V_{BR}	$I_T = 1$ mA, (Note 2)	6.0			V
Reverse Leakage Current	I_R	$V_{RWM} = 5.5$ V			1.0	μA
Clamping Voltage	V_C	$I_{PP} = 1$ A (Note 3)		8.3	10	V
ESD Clamping Voltage	V_C	Per IEC61000-4-2 (Note 4)	See Figures 1 & 2			
Junction Capacitance	C_J	$V_R = 0$ V, $f = 1$ MHz between I/O Pins and GND			0.6	pF
Junction Capacitance	C_J	$V_R = 0$ V, $f = 1$ MHz between I/O Pins			0.3	pF

1. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
2. V_{BR} is measured at pulse test current I_T .
3. Nonrepetitive current pulse (I/O to GND).
4. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

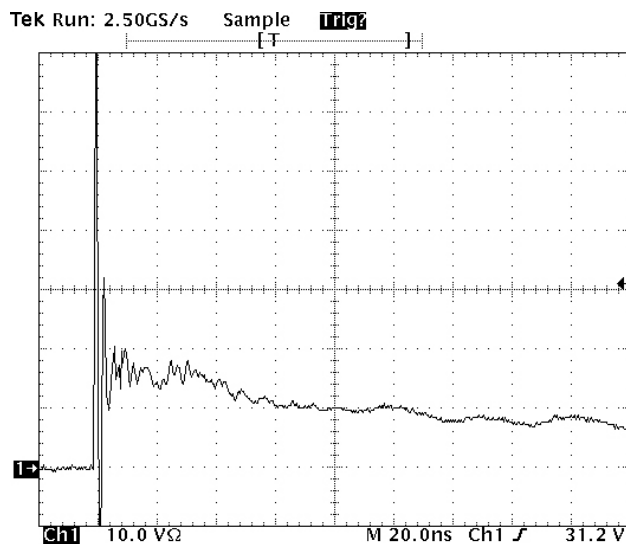


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

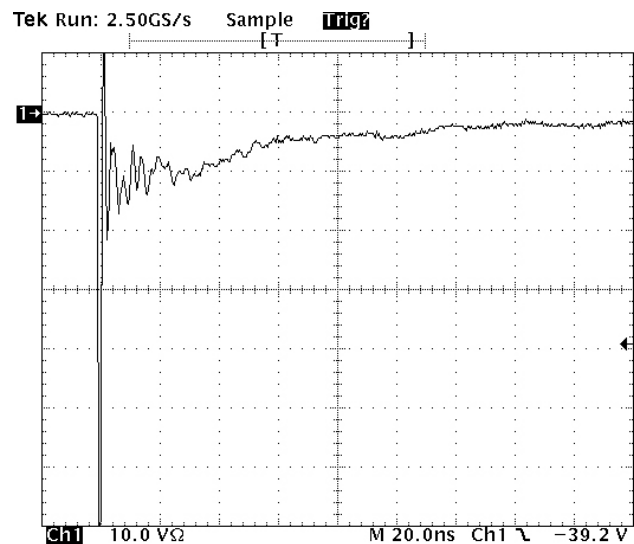


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

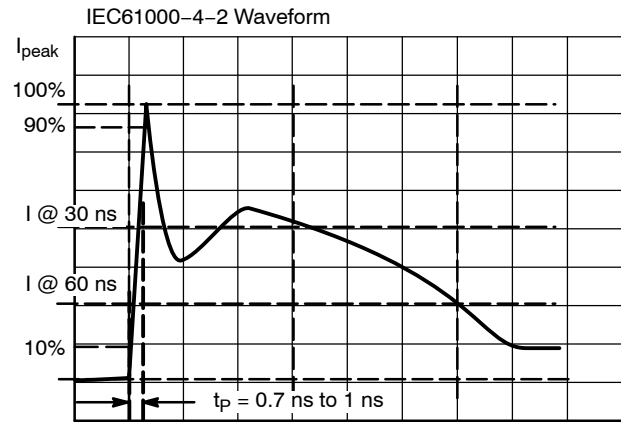


Figure 3. IEC61000-4-2 Spec

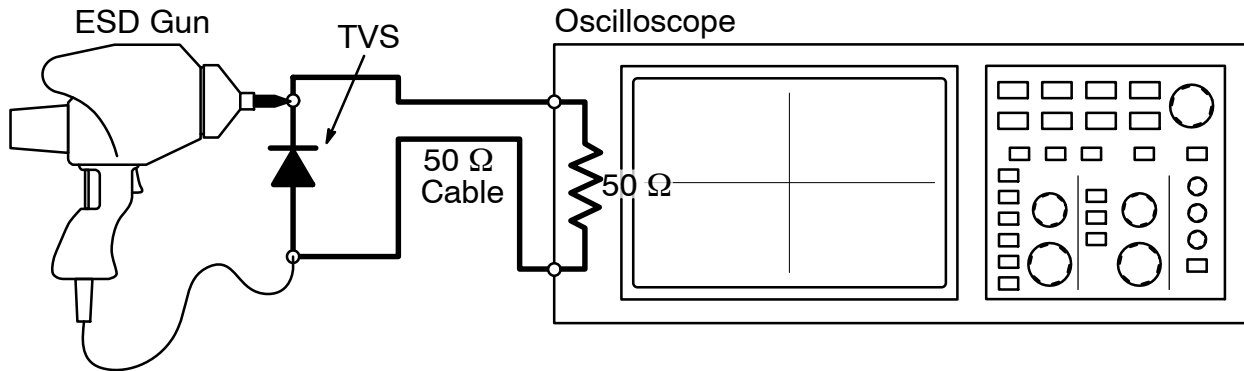


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

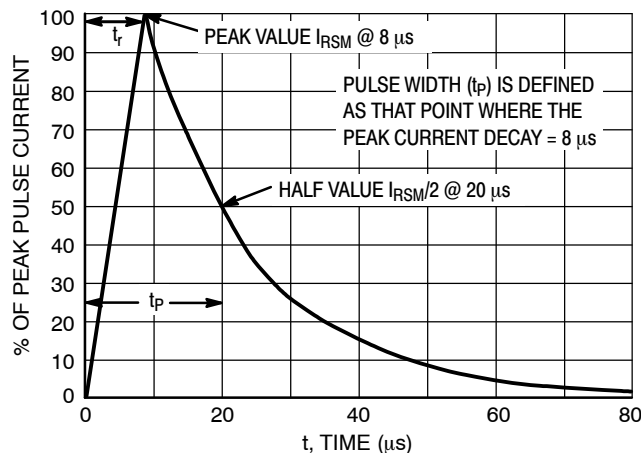
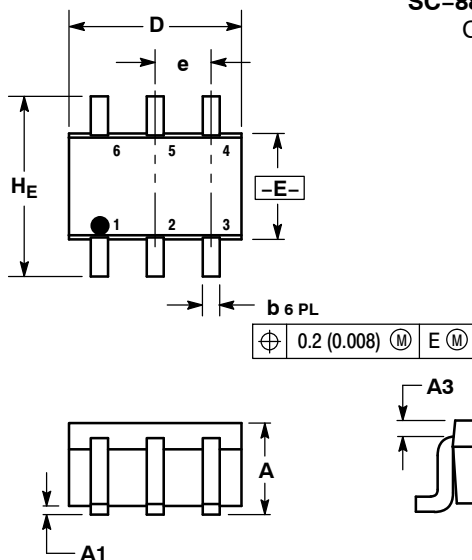


Figure 5. 8 X 20 μ s Pulse Waveform

NUP4114UCLW1

PACKAGE DIMENSIONS

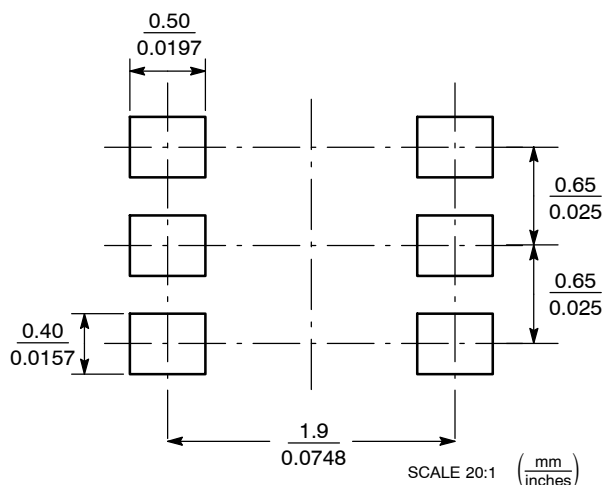
SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE W



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 419B-01 OBSOLETE, NEW STANDARD 419B-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.20 REF			0.008 REF		
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
He	2.00	2.10	2.20	0.078	0.082	0.086

SOLDERING FOOTPRINT*



SC-88/SC70-6/SOT-363

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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