

Silicon NPN Power Transistors

2SC1161

DESCRIPTION

- With TO-66 package
- Low collector saturation voltage

APPLICATIONS

- For low frequency high voltage power amplifier TV vertical deflection output applications.

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

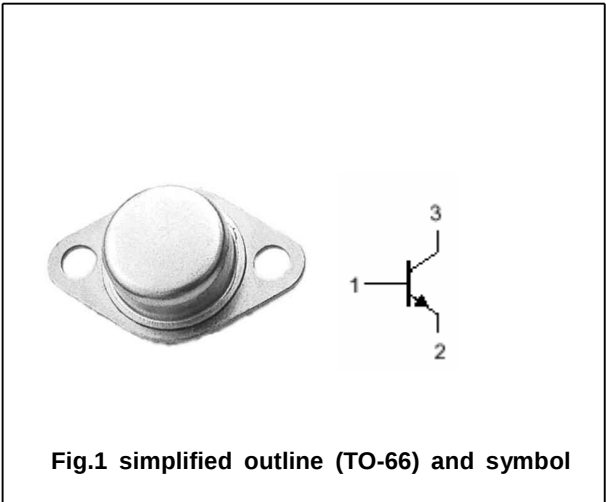


Fig.1 simplified outline (TO-66) and symbol

Absolute maximum ratings(Ta=?)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	200	V
V_{CEO}	Collector-emitter voltage	Open base	120	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		1	A
P_D	Total power dissipation	$T_C=25^{\circ}$	15	W
T_j	Junction temperature		150	?
T_{stg}	Storage temperature		-55~150	?

Silicon NPN Power Transistors**2SC1161****CHARACTERISTICS**T_j=25° unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =50mA ; I _B =0	120			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA ; I _C =0	6			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =500mA; I _B =50mA			1.5	V
V _{BE sat}	Base-emitter saturation voltage	I _C =500mA; I _B =50mA			2.0	V
I _{CBO}	Collector cut-off current	V _{CB} =120V; I _E =0			1.0	μA
I _{EBO}	Emitter cut-off current	V _{EB} =6V; I _C =0			1.0	μA
h _{FE}	DC current gain	I _C =200mA ; V _{CE} =5V	30		200	
f _T	Transition frequency	I _C =200mA ; V _{CE} =10V	5			MHz

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PACKAGE OUTLINE

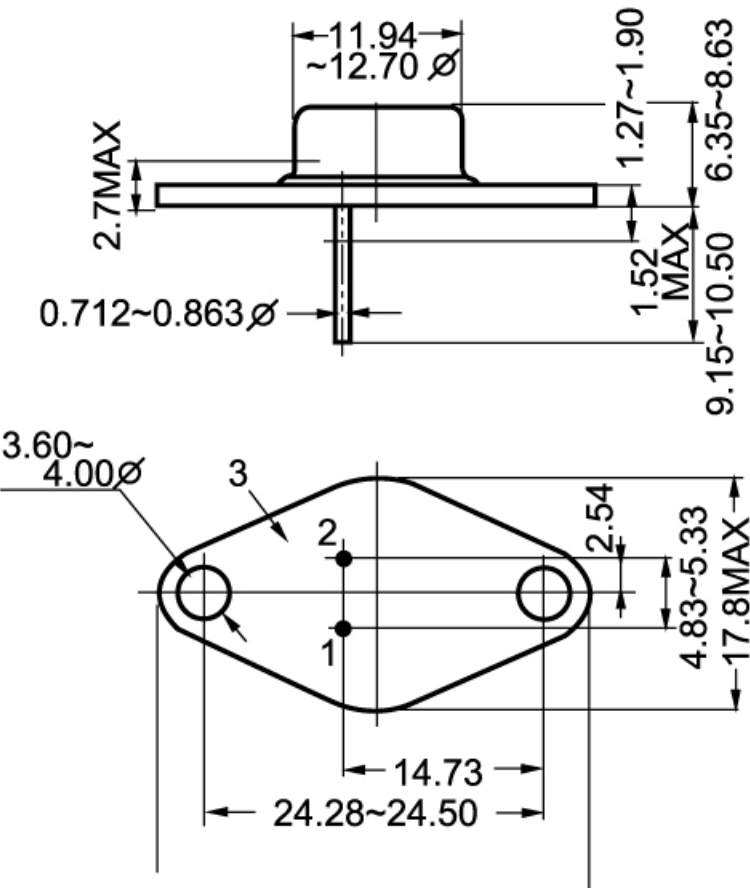


Fig.2 outline dimensions