ON Semiconductor®

VGA Port Companion Circuit

PACVGA200

Features

- Single chip solution for the VGA port interface
- Includes ESD protection, level shifting, and RGB termination
- Seven channels of ESD protection for all VGA port connector pins meeting IEC-61000-4-2 Level-4 ESD requirements (±8kV contact discharge)
- Very low loading capacitance from ESD protection diodes on VIDEO lines, 4pF typical
- 75Ω termination resistors for VIDEO lines (matched to 1% typ.)
- TTL to CMOS level-translating buffers with power down mode for HSYNC and VSYNC lines
- Bi-directional level shifting N-channel FETs provided for DDC_CLK & DDC_DATA channels
- Compact 24-pin QSOP package
- Lead-free version available

Applications

- Notebook computers with VGA port
- Desktop PCs with VGA port

Product Description

The PACVGA200 incorporates seven channels of ESD protection for all signal lines commonly found in a VGA port. ESD protection is implemented with current steering diodes designed to safely handle the high surge currents encountered with IEC-61000-4-2 Level-4 ESD Protection (±8kV contact discharge). When a channel is subjected to an electrostatic discharge, the ESD current pulse is diverted via the protection diodes into either the positive supply rail or ground where it may be safely dissipated. Separate positive supply rails are provided for the VIDEO, DDC and SYNC channels to facilitate interfacing with low voltage Video Controller ICs and provide design flexibility in multi-supply-voltage environments.

Two non-inverting drivers provide buffering for the HSYNC and VSYNC signals from the Video Controller IC (SYNC_IN1, SYNC_IN2). These buffers accept TTL input levels and convert them to CMOS output levels that swing between Ground and $V_{cc}4$.

These drivers have nominal 60 Ω output impedance (R_s) to match the characteristic impedance of the HSYNC & VSYNC lines of the video cables typically used in PC applications. Two N-channel FETs provide the level shifting function required when the DDC controller is operated at a lower supply voltage than the monitor. Three 75 Ω termination resistors suitable for terminating the video signals from the video DAC are also provided. These resistors have separate input pins to allow insertion of additional EMI filtering, if required, between the termination point and the ESD protection diodes. These resistors are matched to better than 2% for excellent signal level matching for the R/G/B signals.

When the PWR_UP input is driven LOW, the SYNC inputs can be floated without causing the SYNC buffers to draw any current from the $V_{cc}4$ supply. When the PWR_UP input is LOW, the SYNC outputs are driven LOW.

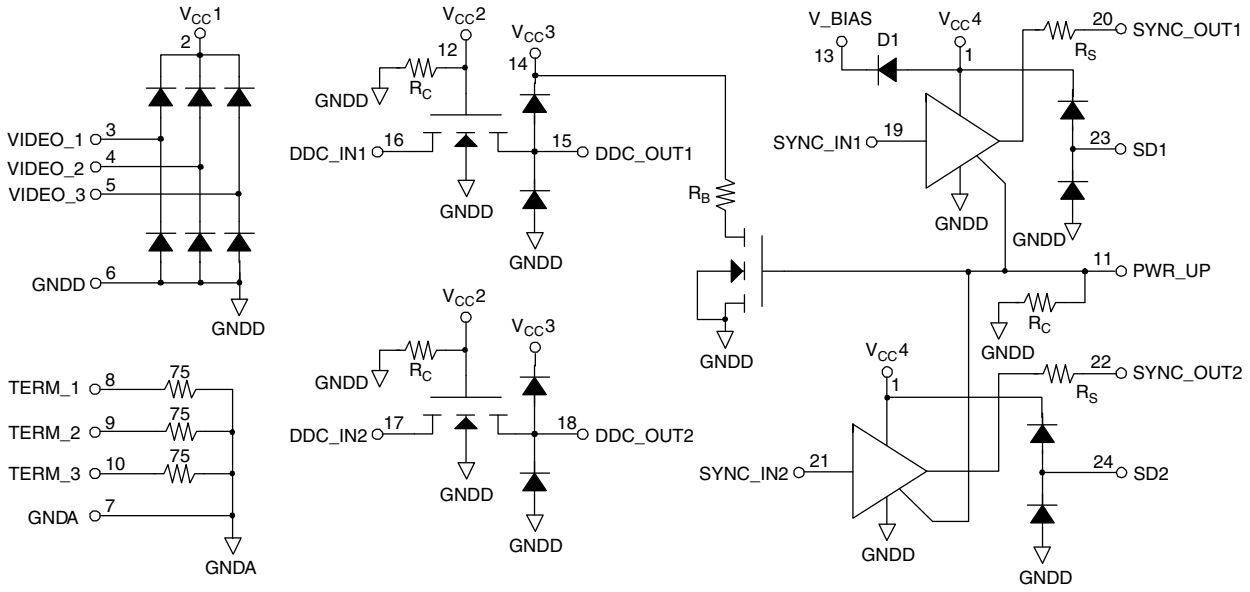
An internal diode (D1 in schematic on previous page) is also provided so that $V_{cc}3$ can be derived from $V_{cc}4$, if desired, by connecting $V_{cc}3$ to V_BIAS. In applications where $V_{cc}4$ may be powered down, diode D1 blocks any DC current paths from the DDC_OUT pins back to the powered down $V_{cc}4$ rail via the top ESD protection diodes.

The PACVGA200 device is housed in a 24-pin QSOP package and is available with optional lead-free finishing.

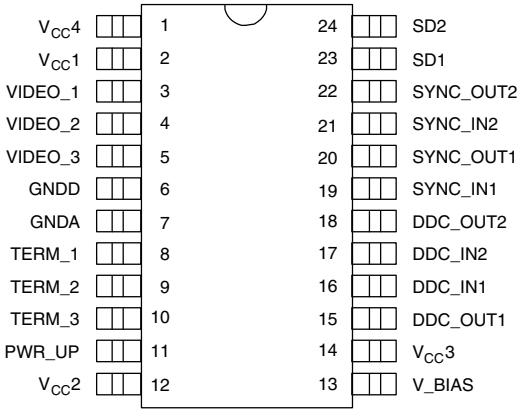
May 2010 Rev. 2

Publication Order Number:
PACVGA200/D

Simplified Electrical Schematic



Top View



24-pin QSOP

Note: This drawing is not to scale.

Ordering Information

PART NUMBERING INFORMATION			
Pins	Package	Lead-free Finish	
		Ordering Part Number[1]	Part Marking
24	QSOP-24	PACVGA200QR	PACVGA200QR

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

PIN DESCRIPTIONS		
LEAD(s)	NAME	DESCRIPTION
1	$V_{CC}4$	Positive voltage supply pin. This is an isolated V_{CC} pin for the SYNC_1, SYNC_2, SD1 and SD2 circuits.
2	$V_{CC}1$	Positive voltage supply pin. This is an isolated V_{CC} pin for the VIDEO_1, VIDEO_2 and VIDEO_3 ESD circuits.
3-5	VIDEO_1, VIDEO_2, VIDEO_3	RGB Video Protection Channels. These pins tie to the RGB video lines (for example, the Blue signal) between the VGA controller device and the video connector.
6	GNDD	Digital Ground reference supply pin.
7	GNDA	Ground reference supply pin for TERM_1, TERM_2 and TERM_3 pins.
8-10	TERM_1, TERM_2, TERM_3	RGB Video Termination Channels. These pins tie to the RGB video lines (for example, the Blue signal) providing a 75Ω termination to GNDA for the given video channel.
11	PWR_UP	Sync Signal Output 1. Ties to the video connector side of one of the sync lines (for example the Horizontal Sync signal).
12	$V_{CC}2$	Positive voltage supply pin. This is an isolated V_{CC} pin for the DDC_IN1 and DDC_IN2 input circuits. Defines the logic one level for the DDC_OUTn outputs.
13	V_BIAS	Used to derive V_{CC3} from V_{CC4} input.
14	$V_{CC}3$	Positive voltage supply pin. This is an isolated V_{CC} pin for the DDC_OUT1 and DDC_OUT2 ESD protection circuits.
15	DDC_OUT1	DDC Signal Output 1. Connects to the connector side of one of the DDC signals (for example, the bidirectional DDC_Data serial line).
16	DDC_IN1	DDC Signal Input 1. Connects to the VGA Controller side of one of the DDC signals (for example, the bidirectional DDC_Data serial line).
17	DDC_IN2	DDC Signal Input 2. Connects to the VGA Controller side of one of the DDC signals (for example, the bidirectional DDC_Clk).

LEAD(s)	NAME	DESCRIPTION
18	DDC_OUT2	DDC Signal Output 2. Connects to the connector side of one of the DDC signals (for example, the bidirectional DDC_Clk).
19	SYNC_IN1	Sync Signal Buffer Input 1. Connects to the VGA Controller side of one of the sync lines (for example, the Horizontal Sync signal).
20	SYNC_OUT1	Sync Signal Buffer Output 1. Connects to the video connector side of one of the sync lines (for example the Horizontal Sync signal).
21	SYNC_IN2	Sync Signal Buffer Input 2. Connects to the VGA Controller side of one of the sync lines (for example, the Vertical Sync signal).
22	SYNC_OUT2	Sync Signal Buffer Output 2. Connects to the video connector side of one of the sync lines (for example the Vertical Sync signal).
23	SD1	Sync Signal Filter 1. Connects to the video connector side of one of the sync lines (for example the Vertical Sync signal).
24	SD2	Sync Signal Filter 2. Connects to the video connector side of one of the sync lines (for example the Horizontal Sync signal).

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
$V_{cc}1$,$V_{cc}2$,$V_{cc}3$, and $V_{cc}4$ Supply Voltage	[GND - 0.5] to +6.0	V
Diode D1 Forward DC Current	100	μA
Storage Temperature Range	-65 to +150	°C
DC Voltage at Inputs VIDEO_1, VIDEO_2, VIDEO_3 TERM_1, TERM_2, TERM_3 DDC_IN1, DDC_IN2 DDC_OUT1, DDC_OUT2 SYNC_IN1, SYNC_IN2	 (GND - 0.5) to ($V_{cc}1$ + 0.5) -6.0, +6.0 (GND - 0.5) to ($V_{cc}2$ + 0.5) (GND - 0.5) to ($V_{cc}3$ + 0.5) (GND - 0.5) to ($V_{cc}4$ + 0.5)	 V V V V V
Package Power Rating	1000	mW

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Operating Temperature Range	0 to +70	°C

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC1}	$V_{CC}1$ Supply Current	$V_{CC}1$ = 5.0V, VIDEO inputs at $V_{CC}1$ or GND level			10	μA
I_{CC2}, I_{CC3}	$V_{CC}2$ & $V_{CC}3$ Supply Current	$V_{CC}2 = V_{CC}3$ = 5.0V			10	μA
I_{CC4}	$V_{CC}4$ Supply Current	$V_{CC}4$ = 5.0V; SYNC inputs at GND or $V_{CC}4$ level; PWR-UP pin at $V_{CC}4$; SYNC outputs unloaded		10		μA
		$V_{CC}4$ = 5.0V; SYNC inputs at 3.0V; PWR-UP pin at $V_{CC}4$; SYNC outputs unloaded		200		μA
		$V_{CC}4$ = 5.0V; PWR-UP input at GND; SYNC outputs unloaded			10	μA
V_{BIAS}	V_{BIAS} Open Circuit Voltage	No external current drawn from V_{BIAS} pin		$V_{CC}4$-0.8		V
R_T	Video Termination Resistance		71.25	75	78.75	Ω
	R_T Resistance Matching			1	2	%
V_{IH}	Logic High Input Voltage	$V_{CC}4$ = 5.0V; See Note 2	2.0			V
V_{IL}	Logic Low Input Voltage	$V_{CC}4$ = 5.0V; See Note 2			0.8	V
V_{OH}	Logic High Output Voltage	I_{OH} = -4mA, $V_{CC}4$ = 5.0V; See Note 2	4.5		4.8	V
V_{OL}	Logic Low Output Voltage	I_{OL} = 4mA, $V_{CC}4$ = 5.0V; See Note 2	0.18		0.32	V
R_{OH}	Output Resistance	See Note 2	50		125	Ω
R_{OL}			45		80	Ω
R_B,R_P	Resistor Value	PWR_UP = $V_{CC}3$ = 5.0V	0.5	1.0	2.0	MΩ
R_C	$V_{CC}2$ Pull-down Resistor Value	$V_{CC}2$ = 3.0V	0.5	1.5	3.0	MΩ
I_N	Input Current VIDEO inputs HSYNC, VSYNC inputs	 $V_{CC}1$= 5.0V; V_{IN}= $V_{CC}1$ or GND $V_{CC}4$ = 5.0V; V_{IN} = $V_{CC}4$ or GND			 ±1 ±1	 μA μA
I_{OFF}	Off-state Leakage Current, Level-shifting NFET	$(V_{CC}2 - V_{DDC\_IN}) \leq 0.4V$; $V_{DDC\_OUT} = V_{CC}2$ $(V_{CC}2 - V_{DDC\_OUT}) \leq 0.4V$; $V_{DDC\_IN} = V_{CC}2$			10 10	μA μA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ON}	Voltage drop across level shifting NFET when turned ON	$V_{CC}2$= 2.5V; V_S = GND; I_{DS} = 3mA			0.15	V
C_{IN}	Input Capacitance VIDEO_1,VIDEO_2 & VIDEO_3 inputs	$V_{CC}1$ = 5.0V; V_{IN} = 2.5V; measured at 1MHz $V_{CC}1$ = 2.5V; V_{IN} = 1.25V; measured at 1MHz	3.0 3.0	4.0 4.5	5.0 5.6	pF pF
t_{PLH}	SYNC Drivers L => H Propagation Delay	C_L = 50pF; V_{CC}=5.0V,Input t_R and $t_F \leq$ 5ns		8.0	12.0	ns
t_{PHL}	SYNC Drivers H => L Propagation Delay	C_L = 50pF; V_{CC}=5.0V; Input t_R and $t_F \leq$ 5ns		8.0	12.0	ns
t_R, t_F	SYNC Drivers Output Rise & Fall Times	C_L = 50pF; V_{CC}=5.0V; Input t_R and $t_F \leq$ 5ns (measured 10% - 90%)	5.0	7.0	10.0	ns
V_{ESD}	ESD Withstand Voltage	$V_{CC}1 = V_{CC}3 = V_{CC}4$ = 5V; Note 3	±8			kV

Note 1: All parameters specified over standard operating conditions unless otherwise noted.

Note 2: This parameter applies only to the HSYNC and VSYNC channels. HSYNC and VSYNC have 8mA drivers with R_S added in series to terminate transmission line.

Note 3: Per the IEC-61000-4-2 International ESD Standard, Level 4 contact discharge method. $V_{CC}1$, $V_{CC}3$ and $V_{CC}4$ must be bypassed to GND via a low impedance ground plane with a 0.2uF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the applicable pins and GND. ESD pulse can be positive or negative with respect to GND. Applicable pins are: VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SD1, SYNC_OUT2, SD2, DDC_OUT1 and DDC_OUT2. All other pins are ESD protected to the industry standard 2kV per the Human Body Model (MIL-STD-883, Method 3015).

Test Circuit Information

Average Current through $V_{cc}4$ ($I_{cc}4$)

The circuit in Figure 1 was used to characterize $I_{cc}4$ current as SYNC_IN signal frequency varies. A square wave signal was connected to the input of one of the SYNC buffers (i.e. pin 19 or pin 21). The frequency of this signal was varied between 0 and 100 kHz. The risetime and falltime was kept constant at 10ns. Three different values of C1 were used: 0pF, 50pF and 100pF. The results are plotted in Figure 2.

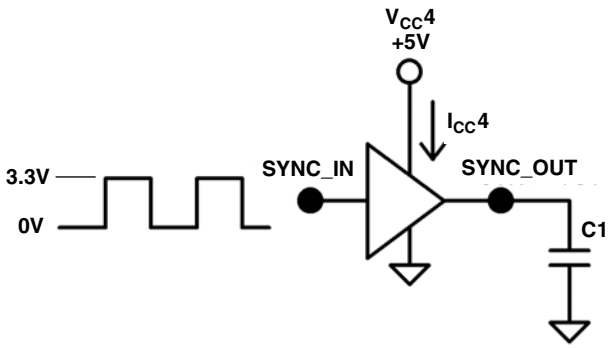


Figure 1. Sync Buffer $I_{cc}4$ Test Circuit

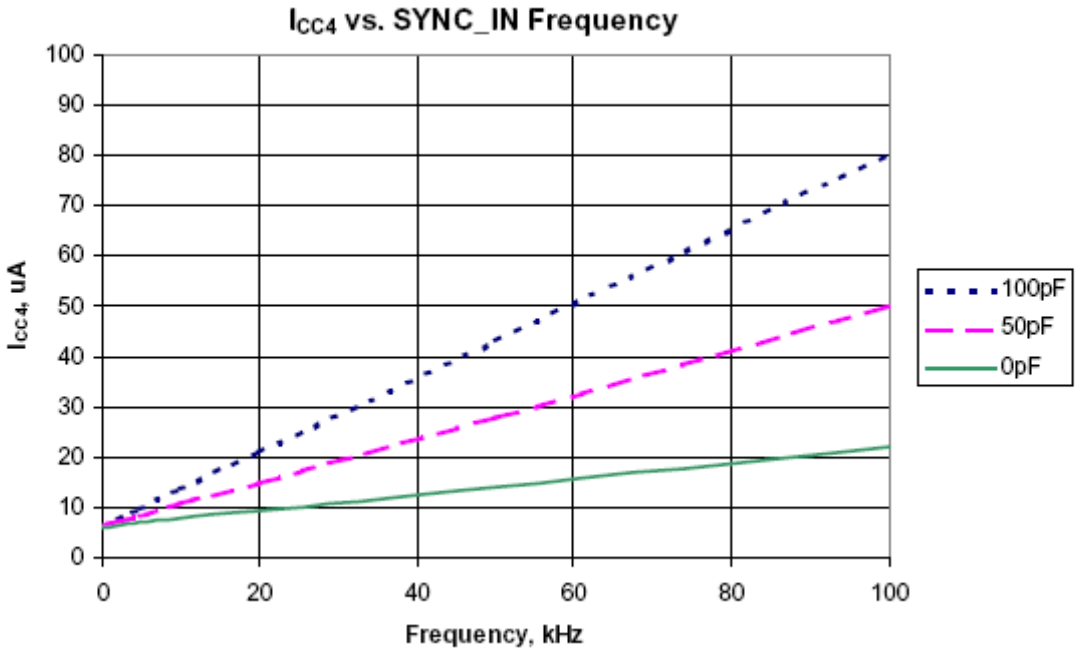


Figure 2. $I_{cc}4$ vs. SYNC_IN Frequency Performance Data

Application Information

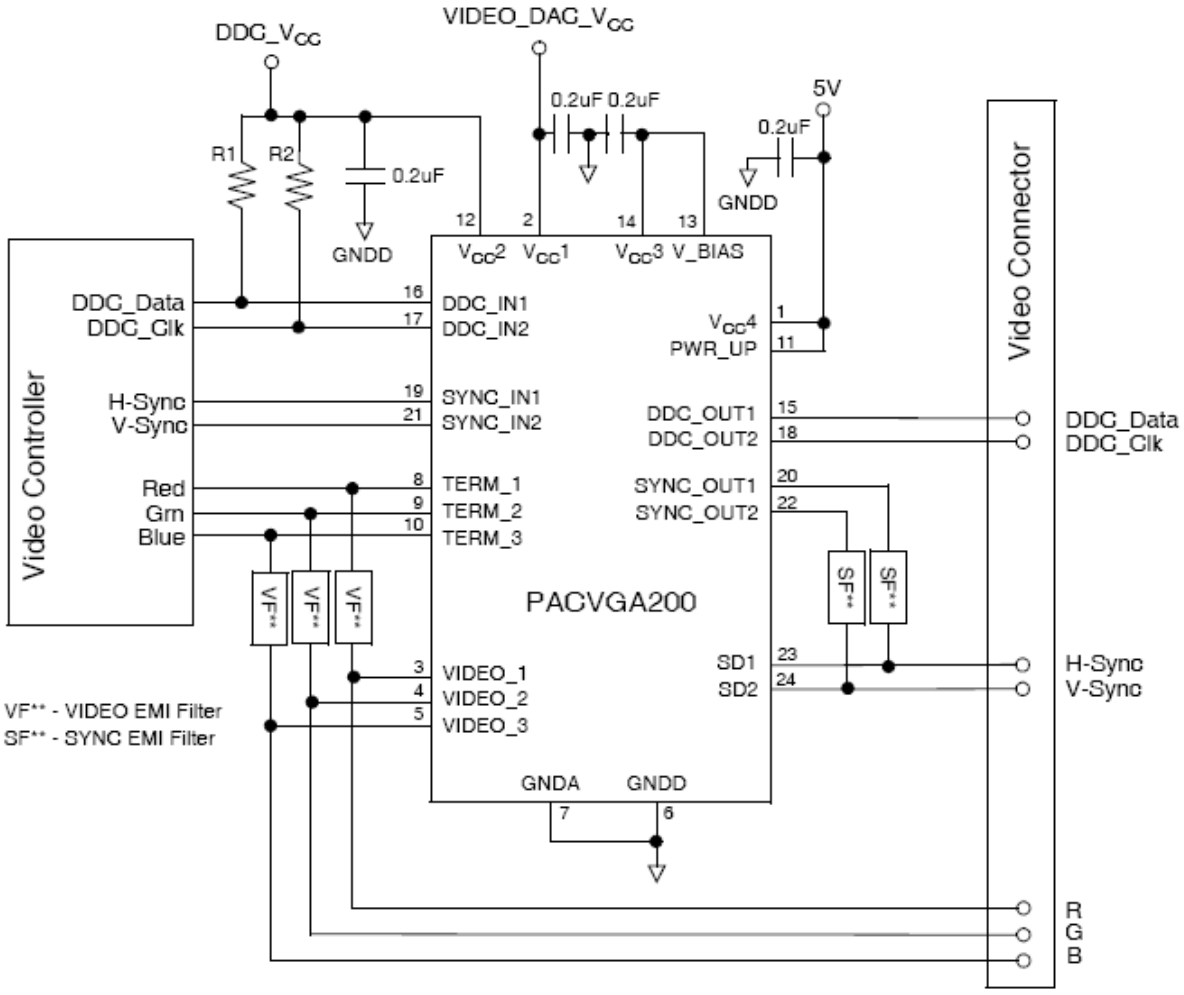


Figure 3. Typical Connection Diagram

A resistor may be necessary between the $V_{CC}3$ pin and ground if protection against a stream of ESD pulses is required while the PACVGA200 is in the power-down state. The value of this resistor should be chosen such that the extra charge deposited into the $V_{CC}3$ bypass capacitor by each ESD pulse will be discharged before the next ESD pulse occurs. The maximum ESD repetition rate specified by the IEC-61000-4-2 standard is one pulse per second. When the PACVGA200 is in the power-up state, an internal discharge resistor is connected to ground via an FET switch for this purpose.

For the same reason, $V_{CC}1$ and $V_{CC}4$ may also require bypass capacitor discharging resistors to ground if there are no other components in the system to provide a discharge path to ground.

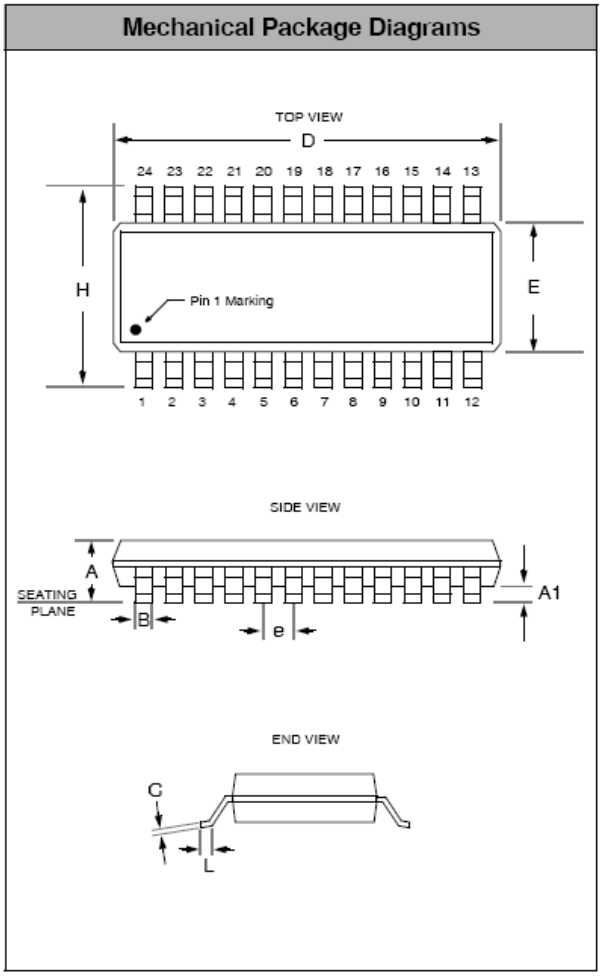
GNDA, the reference voltage for the 75Ω resistors is not connected internally to GNDD and should ideally be connected to the ground of the video DAC IC.

Mechanical Details

QSOP Mechanical Specifications:

PACVGA200 devices are packaged in 24-pin QSOP packages. Dimensions are presented below. For complete information on the QSOP-24 package, see the California Micro Devices QSOP Package Information document.

PACKAGE DIMENSIONS				
Package	QSOP (JEDEC name is SSOP)			
Pins	24			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.20	0.30	0.008	0.012
C	0.18	0.25	0.007	0.010
D	8.56	8.73	0.337	0.344
E	3.81	3.98	0.150	0.157
e	0.64 BSC		0.025 BSC	
H	5.79	6.19	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	55 pcs*			
# per tape and reel	2500 pcs			
Controlling dimension: inches				



Package Dimensions for QSOP-24

* This is an approximate number which may vary.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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