Low-Power, 8-Channel, 24-Bit Analog Front-End for Biopotential Measurements

Check for Samples: ADS1294, ADS1296, ADS1298

FEATURES

- **Eight Low-Noise PGAs and Eight High-Resolution ADCs (ADS1298)**
- **Low Power: 0.75mW/channel**
- **Input-Referred Noise: 4μV_{PP} (150Hz BW, G = 6)**
- **Input Bias Current: 200pA**
- **Data Rate: 250SPS to 32kSPS**
- **CMRR: –115dB**
- **Programmable Gain: 1, 2, 3, 4, 6, 8, or 12**
- **Supplies: Unipolar or Bipolar**
  - **Analog: 2.7V to 5.25V**
  - **Digital: 1.65V to 3.6V**
- **Built-In Right Leg Drive Amplifier, Lead-Off Detection, WCT, Test Signals**
- **Pace Detection**
- **Digital Pace Detection Capability**
- **Built-In Oscillator and Reference**
- **Flexible Power-Down, Standby Mode**
- **SPI™-Compatible Serial Interface**
- **Operating Temperature Range: 0°C to +70°C (–40°C to +85°C grade available soon)**

APPLICATIONS

- **Medical Instrumentation (ECG and EEG) including:**
  - **Patient monitoring; Holter, event, stress, and vital signs ECG, AED, telemedicine, fetal ECG**
  - **Bispectral index (BIS), Evoked audio potential (EAP), Sleep study monitor**
- **High-Precision, Simultaneous, Multichannel Signal Acquisition**

DESCRIPTION

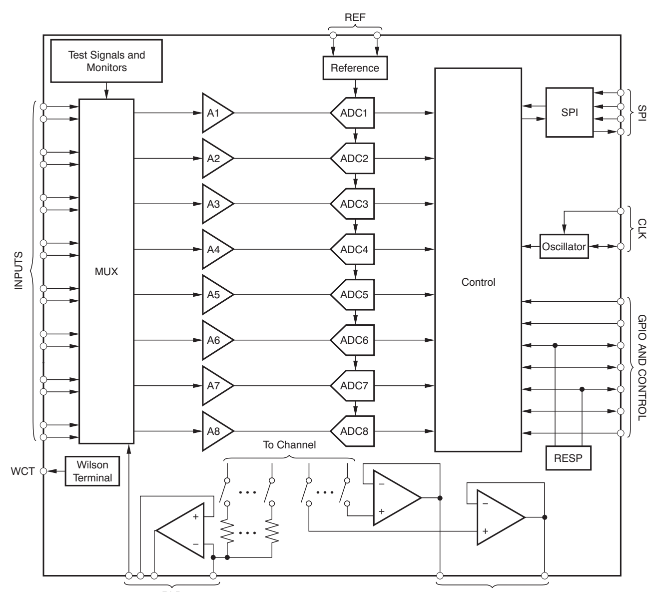
The ADS1294/6/8 are a family of multichannel, simultaneous sampling, 24-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with a built-in programmable gain amplifier (PGA), internal reference, and an onboard oscillator. The ADS1294/6/8 incorporate all of the features that are commonly required in medical electrocardiogram (ECG) and electroencephalogram (EEG) applications.

With its high levels of integration and exceptional performance, the ADS1294/6/8 family enables the creation of scalable medical instrumentation systems at significantly reduced size, power, and overall cost.

The ADS1294/6/8 have a flexible input multiplexer per channel that can be independently connected to the internally-generated signals for test, temperature, and lead-off detection. Additionally, any configuration of input channels can be selected for derivation of the right leg drive (RLD) output signal. The ADS1294/6/8 operate at data rates as high as 32kSPS, thereby allowing the implementation of software pace detection. Lead-off detection can be implemented internal to the device, either with a pull-up/pull-down resistor or an excitation current sink/source. Three integrated amplifiers generate the Wilson Central Terminal (WCT) and the Goldberger Central Terminals (GCT) required for a standard 12-lead ECG.

Multiple ADS1294/6/8 devices can be cascaded in high channel count systems in a daisy-chain configuration.

Package options include a tiny 8mm × 8mm, 64-ball BGA and a TQFP-64. Both packages are specified from 0°C to +70°C (–40°C to +85°C for TQFP industrial grade version available soon).



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FAMILY AND ORDERING INFORMATION(1)

PRODUCT	PACKAGE OPTION	NUMBER OF CHANNELS	ADC RESOLUTION	MAXIMUM SAMPLE RATE (kSPS)	OPERATING TEMPERATURE RANGE	RESPIRATION CIRCUITRY
ADS1194	BGA	4	16	8	0°C to +70°C	No
	TQFP	4	16	8	0°C to +70°C	No
ADS1196	BGA	6	16	8	0°C to +70°C	No
	TQFP	6	16	8	0°C to +70°C	No
ADS1198	BGA	8	16	8	0°C to +70°C	No
	TQFP	8	16	8	0°C to +70°C	No
ADS1294	BGA	4	24	32	0°C to +70°C	External
ADS1296	BGA	6	24	32	0°C to +70°C	External
ADS1298	BGA	8	24	32	0°C to +70°C	External
ADS1298I	TQFP	8	24	32	–40°C to +85°C	External

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	ADS1294, ADS1296, ADS1298	UNIT
AVDD to AVSS	–0.3 to +5.5	V
DVDD to DGND	–0.3 to +3.9	V
AVSS to DGND	–3 to +0.2	V
V_{REF} input to AVSS	AVSS – 0.3 to AVDD + 0.3	V
Analog input to AVSS	AVSS – 0.3 to AVDD + 0.3	V
Digital input voltage to DGND	–0.3 to DVDD + 0.3	V
Digital output voltage to DGND	–0.3 to DVDD + 0.3	V
Digital input voltage to DGND	–0.3 to DVDD + 0.3	V
Digital output voltage to DGND	–0.3 to DVDD + 0.3	V
Operating temperature range	0 to +70	°C
Operating temperature range (industrial grade only)	–40 to +85	°C
Storage temperature range	–60 to +150	°C
Maximum junction temperature (T_J)	+150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

Minimum/maximum specifications apply from 0°C to +70°C. Typical specifications are at +25°C. All specifications at DVDD = 1.8V, AVDD – AVSS = 3V(1), V_{REF} = 2.4V, external f_{CLK} = 2.048MHz, data rate = 500SPS, high resolution mode, and gain = 6, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1294, ADS1296, ADS1298			UNIT
		MIN	TYP	MAX	
ANALOG INPUTS					
Full-scale differential input voltage (AINP – AINN)			$\pm V_{REF}$/GAIN		V
Input common-mode range			See the *Input Common-Mode Range* subsection of the *PGA Settings and Input Range* section		
Input capacitance			20		pF
Input bias current	T_A = +25°C, input = 1.5V			±200	pA
	T_A = 0°C to +70°C, input = 1.5V		±1		nA
DC input impedance	No lead-off	1000			MΩ
	Current source lead-off detection		500		MΩ
	Pull-up resistor lead-off detection		10		MΩ
PGA PERFORMANCE					
Gain settings			1, 2, 3, 4, 6, 8, 12		
Bandwidth			See Table 6		
ADC PERFORMANCE					
Resolution	DR[2:0] = 011 to 110, no missing codes	24			Bits
	DR[2:0] = 001	19			Bits
	DR[2:0] = 000	17			Bits
Data rate	f_{CLK} = 2.048MHz	500		32000	SPS
	f_{CLK} = 2.048MHz, Low-Power mode	125		16000	SPS
CHANNEL PERFORMANCE					
DC Performance					
Input-referred noise	Gain = 6(2), 10 seconds of data		5		μV_{PP}
	Gain = 6, 256 points, 0.5 seconds of data		4	7	μV_{PP}
	Gain settings other than 6, data rate other than 500SPS		See *Noise Measurements* section		
Integral nonlinearity	Full-scale with gain = 6, best fit		8		ppm
Offset error			±500		µV
Offset error drift			2		µV/°C
Gain error	Excluding voltage reference error		±0.2	±0.5	% of FS
Gain drift	Excluding voltage reference drift		5		ppm/°C
Gain match between channels			0.3		% of FS
AC Performance					
Common-mode rejection	f_{CM} = 50Hz, 60Hz(3)	105	115		dB
Power-supply rejection	f_{PS} = 50Hz, 60Hz		90		dB
Crosstalk	f_{IN} = 50Hz, 60Hz		–126		dB
Signal-to-noise ratio (SNR)	f_{IN} = 10Hz input, gain = 6		112		dB
Total harmonic distortion (THD)	10Hz, –0.5dBFs		–98		dB
	100Hz, –0.5dBFs		–100		dB

(1) Performance is applicable for 5V operation as well. Production testing for limits is performed at 3V.
(2) Noise data measured in a 10-second interval. Test not performed in production. Input-referred noise is calculated with input shorted (without electrode resistance) over a 10-second interval.
(3) CMRR is measured with a common-mode signal of AVSS + 0.3V to AVDD – 0.3V. The values indicated are the minimum of the eight channels.

ELECTRICAL CHARACTERISTICS (continued)

Minimum/maximum specifications apply from 0°C to +70°C. Typical specifications are at +25°C. All specifications at DVDD = 1.8V, AVDD – AVSS = 3V (1), V_{REF} = 2.4V, external f_{CLK} = 2.048MHz, data rate = 500SPS, high resolution mode, and gain = 6, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1294, ADS1296, ADS1298			UNIT
		MIN	TYP	MAX	
RIGHT LEG DRIVE (RLD) AMPLIFIER AND PACE AMPLIFIERS					
Integrated noise	BW = 150Hz		7		μV_{RMS}
Gain bandwidth product	50kΩ || 10pF load, gain = 1		100		kHz
Slew rate	50kΩ || 10pF load, gain = 1		0.25		V/µs
Total harmonic distortion	f_{IN} = 100Hz, gain = 1		–70		dB
Common-mode input range		AVSS + 0.7		AVDD – 0.3	V
Common-mode resistor matching	Internal 200kΩ resistor matching		0.1		%
Short-circuit current			±0.25		mA
Quiescent power consumption	Either RLD or pace amplifier		20		µA
WILSON CENTRAL TERMINAL (WCT) AMPLIFIER					
Integrated noise	BW = 150Hz		See Table 5		nV/√Hz
Gain bandwidth product			See Table 5		kHz
Slew rate			See Table 5		V/s
Total harmonic distortion	f_{IN} = 100Hz		90		dB
Common-mode input range		AVSS + 0.3		AVDD – 0.3	V
Short-circuit current			±0.25		mA
Quiescent power consumption			See Table 5		µA
LEAD-OFF DETECT					
Frequency	See the *Register Map* section for settings		0, f_{DR}/4		kHz
Current	See the *Register Map* section for settings		6, 12, 18, 24		nA
Current accuracy			±10		%
Comparator threshold accuracy			±30		mV
EXTERNAL REFERENCE					
Reference input voltage	3V supply V_{REF} = (VREFP – VREFN)		2.5		V
	5V supply V_{REF} = (VREFP – VREFN)		4.0		V
Negative input (VREFN)			AVSS		V
Positive input (VREFP)			AVSS + 2.5		V
Input impedance			10		kΩ
INTERNAL REFERENCE					
Output voltage	CONFIG3.VREF_4V = 0		2.4		V
	CONFIG3.VREF_4V = 1		4.0		V
V_{REF} accuracy			±0.2		%
Drift			25		ppm/°C
Start-up time			150		ms
SYSTEM MONITORS					
Analog supply reading error			2		%
Digital supply reading error			2		%
Device wake up	From power-up to $\overline{DRDY}$ low		150		ms
	STANDBY mode		9		ms
Temperature sensor reading, voltage	T_A = +25°C		145		mV
Temperature sensor reading, coefficient			490		µV/°C
Test Signal					
Signal frequency	See *Register Map* section for settings		$f_{CLK}/2^{21}$, $f_{CLK}/2^{20}$		Hz
Signal voltage	See *Register Map* section for settings		±1, ±2		mV
Accuracy			±2		%

ELECTRICAL CHARACTERISTICS (continued)

Minimum/maximum specifications apply from 0°C to +70°C. Typical specifications are at +25°C. All specifications at DVDD = 1.8V, AVDD – AVSS = 3V [(1)], V_{REF} = 2.4V, external f_{CLK} = 2.048MHz, data rate = 500SPS, high resolution mode, and gain = 6, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1294, ADS1296, ADS1298 MIN	TYP	MAX	UNIT
CLOCK						
Internal oscillator clock frequency		Nominal Frequency		2.048		MHz
Internal clock accuracy		T_A = +25°C			±0.5	%
		0°C ≤ T_A ≤ +70°C			±2	%
		–40°C ≤ T_A ≤ +85°C (industrial grade versions only)			±5	%
Internal oscillator start-up time					20	μs
Internal oscillator power consumption				120		μW
External clock input frequency		CLKSEL pin = 0	0.5	2.048	2.25	MHz
DIGITAL INPUT/OUTPUT (DVDD = 1.65V to 3.6V)						
Logic level	V_{IH}		0.8DVDD		DVDD + 0.1	V
	V_{IL}		–0.1		0.2DVDD	V
	V_{OH}	I_{OH} = –500μA	DVDD – 0.4			V
	V_{OL}	I_{OL} = +500μA			0.4	V
	Input current (I_{IN})	0V < $V_{DigitalInput}$ < DVDD	–10		+10	μA
POWER-SUPPLY REQUIREMENTS						
Analog supply (AVDD – AVSS)			2.7	3.0	5.25	V
Digital supply (DVDD)			1.65	1.8	3.6	V
AVDD – DVDD			–2.1		3.6	V
SUPPLY CURRENT (RLD, WCT, and Pace Amplifiers Turned Off)						
High-Resolution mode	I_{AVDD}	AVDD – AVSS = 3V		2.75		mA
		AVDD – AVSS = 5V		3.1		mA
	I_{DVDD}	DVDD = 3.0V		0.5		mA
		DVDD = 1.8V		0.3		mA
Low-Power mode	I_{AVDD}	AVDD – AVSS = 3V		1.8		mA
		AVDD – AVSS = 5V		2.1		mA
	I_{DVDD}	DVDD = 3.0V		0.5		mA
		DVDD = 1.8V		0.3		mA

ELECTRICAL CHARACTERISTICS (continued)

Minimum/maximum specifications apply from 0°C to +70°C. Typical specifications are at +25°C. All specifications at DVDD = 1.8V, AVDD – AVSS = 3V [(1)], V_{REF} = 2.4V, external f_{CLK} = 2.048MHz, data rate = 500SPS, high resolution mode, and gain = 6, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1294, ADS1296, ADS1298 MIN	TYP	MAX	UNIT
POWER DISSIPATION (Analog Supply = 3V, RLD, WCT, and Pace Amplifiers Turned Off)						
Quiescent power dissipation (ADS1298)		High-Resolution mode		8.8	9.5	mW
		Low-Power mode (250SPS)		6.0	7.0	mW
		Power-down		10		µW
		Standby mode		2		mW
Quiescent power dissipation, per channel	ADS1298	High-Resolution mode		1.10		mW
		Low-Power mode		0.75		mW
	ADS1296	High-Resolution mode		1.2		mW
		Low-Power mode		0.85		mW
	ADS1294	High-Resolution mode		1.30		mW
		Low-Power mode		0.90		mW
POWER DISSIPATION (Analog Supply = 5V, RLD, WCT, and Pace Amplifiers Turned Off)						
Quiescent power dissipation (ADS1298)		High-Resolution mode		17.5		mW
		Low-Power mode		12.5		mW
		Power-down		20		µW
		Standby mode, internal reference		4		mW
Quiescent power dissipation, per channel	ADS1298	High-Resolution mode		2		mW
		Low-Power mode		1.5		mW
	ADS1296	High-Resolution mode		2.3		mW
		Low-Power mode		1.6		mW
	ADS1294	High-Resolution mode		2.6		mW
		Low-Power mode		2		mW
TEMPERATURE						
Specified temperature range			0		+70	°C
Operating temperature range			0		+70	°C
Specified temperature range (industrial grade only)			–40		+85	°C
Operating temperature range (industrial grade only)			–40		+85	°C
Storage temperature range			–60		+150	°C

NOISE MEASUREMENTS

The ADS1294/6/8 noise performance can be optimized by adjusting the data rate and PGA setting. As the averaging is increased by reducing the data rate, the noise drops correspondingly. Increasing the PGA value reduces the input-referred noise, which is particularly useful when measuring low-level biopotential signals. Table 1 and Table 2 summarize the noise performance of the ADS1294/6/8 in the High-Resolution (HR) mode and Low-Power (LP) mode, respectively, with a 3V analog power supply. Table 3 and Table 4 summarize the noise performance of the ADS1294/6/8 in the HR mode and LP mode, respectively, with a 5V analog power supply. The data are representative of typical noise performance at T_A = +25°C. The data shown are the result of averaging the readings from multiple devices and are measured with the inputs shorted together. A minimum of 1000 consecutive readings are used to calculate the RMS and peak-to-peak noise for each reading. For the two highest data rates, the noise is limited by quantization noise of the ADC and does not have a gaussian distribution. Thus, the ratio between rms noise and peak-to-peak noise is approximately 10. For the lower data rates, the ratio is approximately 6.6.

Table 1 to Table 4 show measurements taken with an internal reference. The data are also representative of the ADS1294/6/8 noise performance when using a low-noise external reference such as the REF5025.

Table 1. Input-Referred Noise ($\mu V_{RMS}/\mu V_{PP}$) in High-Resolution Mode 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12
000	32000	8398	335/3553	168/1701	112/1100	85/823	58/529	42.5/378	28.6/248
001	16000	4193	56/613	28/295	18.8/188	14.3/143	9.7/94	7.4/69	5.2/44.3
010	8000	2096	12.4/111	6.5/54	4.5/37.9	3.5/29.7	2.6/21.7	2.2/17.8	1.8/13.8
011	4000	1048	6.1/44.8	3.2/23.3	2.4/17.1	1.9/14.0	1.5/11.1	1.3/9.7	1.2/8.5
100	2000	524	4.1/27.8	2.2/15.4	1.6/11.0	1.3/9.1	1.1/7.3	1.0/6.5	0.9/6.0
101	1000	262	2.9/19.0	1.6/10.1	1.2/7.5	1.0/6.2	0.8/5.0	0.7/4.6	0.6/4.1
110	500	131	2.1/12.5	1.1/6.8	0.9/5.1	0.7/4.3	0.6/3.5	0.5/3.1	0.5/2.9

(1) At least 1000 consecutive readings were used to calculate the RMS and peak-to-peak noise values in this table.

Table 2. Input-Referred Noise ($\mu V_{RMS}/\mu V_{PP}$) in Low-Power Mode 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12
000	16000	4193	333/3481	166/1836	111/1168	84/834	56/576	42/450	28/284
001	8000	2096	56/554	28/272	19/177	14.3/133	9.7/85	7.4/64	5.0/42.4
010	4000	1048	12.5/99	6.5/51	4.5/35.0	3.4/25.9	2.4/18.8	2.0/14.5	1.5/11.3
011	2000	524	6.1/41.8	3.2/22.2	2.3/15.9	1.8/12.1	1.4/9.3	1.2/7.8	1.0/6.7
100	1000	262	4.1/26.3	2.2/14.6	1.6/9.9	1.3/8.1	1.0/6.2	0.8/5.4	0.7/4.7
101	500	131	3.0/17.9	1.6/9.8	1.1/6.8	0.9/5.7	0.7/4.2	0.6/3.6	0.5/3.4
110	250	65	2.1/11.9	1.1/6.3	0.8/4.6	0.7/4.0	0.5/3.0	0.5/2.6	0.4/2.4

(1) At least 1000 consecutive readings were used to calculate the RMS and peak-to-peak noise values in this table.

Table 3. Input-Referred Noise ($\mu V_{RMS}/\mu V_{PP}$) in High-Resolution Mode 5V Analog Supply and 4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12
000	32000	8398	521/5388	260/2900	173/1946	130/1403	87/917	65/692	44/483
001	16000	4193	86/1252	43/633	29/402	22/298	15/206	11/141	7/91
010	8000	2096	17/207	9/112	6/71	4/57	3/36	3/29	2/18
011	4000	1048	6.4/48.2	3.4/25.9	2.417.7	1.9/15.4	1.5/11.2	1.3/9.6	1.1/8.2
100	2000	524	4.2/29.9	2.3/15.9	1.6/11.1	1.3/9.3	1.0/7.5	0.9/6.6	0.8/5.8
101	1000	262	2.9/18.8	1.6/10.4	1.1/7.8	0.9/6.1	0.7/4.9	0.6/4.7	0.6/3.9
110	500	131	2.0/12.8	1.1/7.2	0.8/5.2	0.7/4.0	0.5/3.3	0.5/3.3	0.4/2.7

(1) At least 1000 consecutive readings were used to calculate the RMS and peak-to-peak noise values in this table.

Table 4. Input-Referred Noise ($\mu V_{RMS}/\mu V_{PP}$) in Low-Power Mode 5V Analog Supply and 4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1	PGA GAIN = 2	PGA GAIN = 3	PGA GAIN = 4	PGA GAIN = 6	PGA GAIN = 8	PGA GAIN = 12
000	16000	4193	526/5985	263/2953	175/1918	132/1410	88/896	66/681	44/458
001	8000	2096	88/1201	44/619	29/411	22/280	15/191	11/139	7/83
010	4000	1048	17/208	9/103	6/62	4/52	3/37	2/25	2/16
011	2000	524	6.0/41.1	3.3/23.3	2.2/15.5	1.8/12.3	1.3/9.8	1.1/7.8	0.9/6.5
100	1000	262	4.1/27.1	2.3/14.8	1.5/10.1	1.2/8.1	0.9/6.0	0.8/5.4	0.7/4.4
101	500	131	2.9/17.4	1.6/9.6	1.1/6.6	0.9/5.9	0.7/4.3	0.6/3.4	0.5/3.2
110	250	65	2.1/11.9	1.1/6.6	0.8/4.6	0.6/3.7	0.5/3.0	0.4/2.5	0.4/2.2

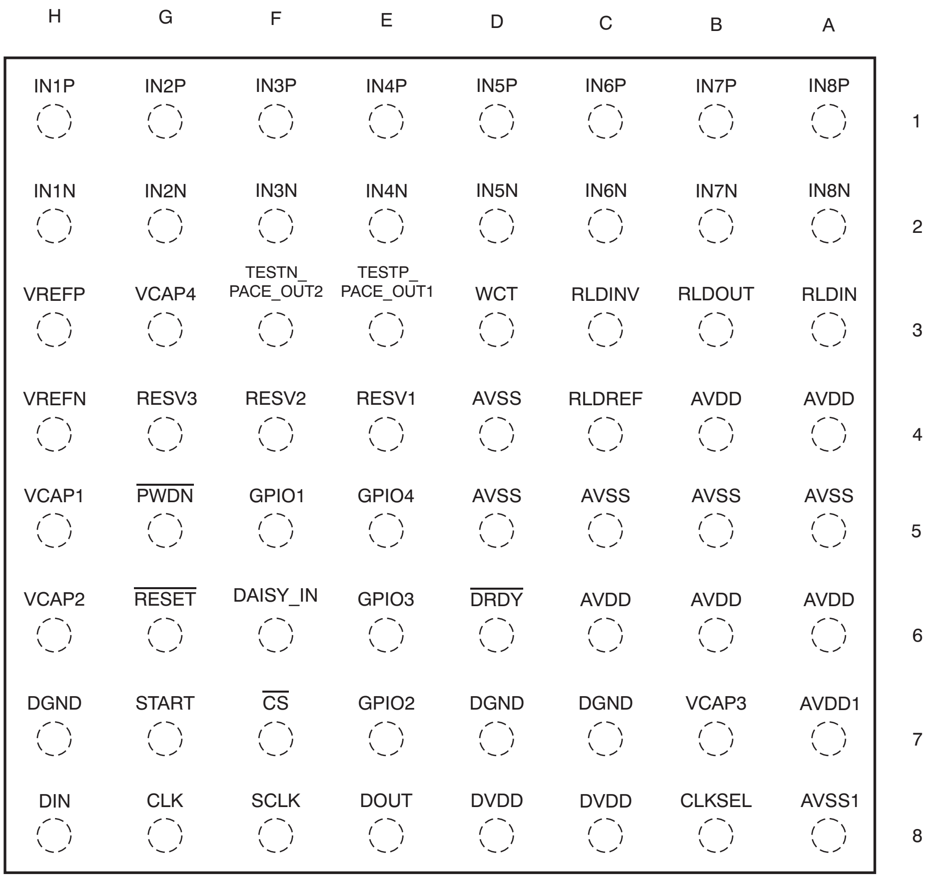
(1) At least 1000 consecutive readings were used to calculate the RMS and peak-to-peak noise values in this table.

Table 5. Typical WCT Performance

PARAMETER	ANY ONE (A, B, or C)	ANY TWO (A+B, A+C, or B+C)	ALL THREE (A+B+C)	UNIT
Integrated noise	540	382	312	nV_{RMS}
Power	53	59	65	μA
–3dB BW	30	59	89	kHz
Slew rate	BW limited	BW limited	BW limited	—

PIN CONFIGURATIONS

ZXG PACKAGE
BGA-64
(TOP VIEW, SOLDER BUMPS ON BOTTOM SIDE)



BGA PIN ASSIGNMENTS

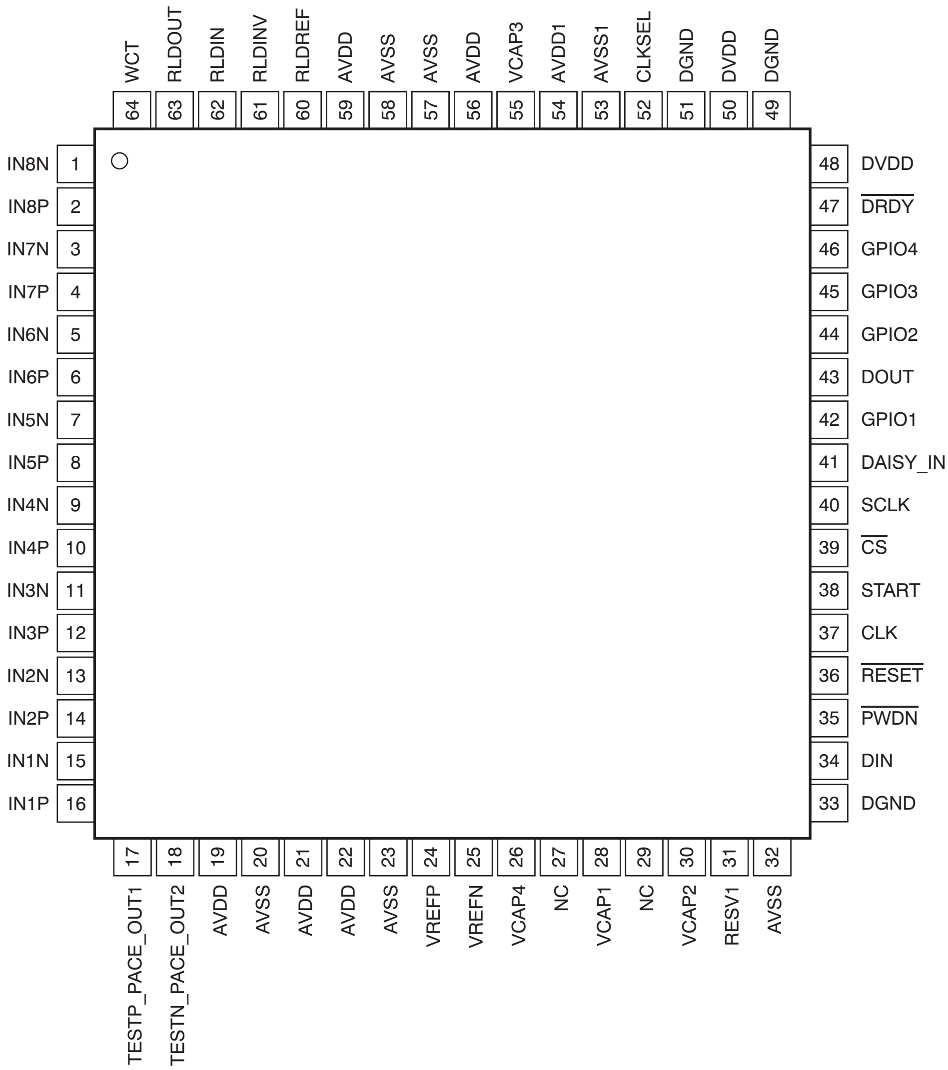
NAME	TERMINAL	FUNCTION	DESCRIPTION
IN8P(1)	1A	Analog input	Differential analog positive input 8 (ADS1298 only)
IN7P(1)	1B	Analog input	Differential analog positive input 7 (ADS1298 only)
IN6P(1)	1C	Analog input	Differential analog positive input 6 (ADS1296/8 only)
IN5P(1)	1D	Analog input	Differential analog positive input 5 (ADS1296/8 only)
IN4P(1)	1E	Analog input	Differential analog positive input 4
IN3P(1)	1F	Analog input	Differential analog positive input 3
IN2P(1)	1G	Analog input	Differential analog positive input 2
IN1P(1)	1H	Analog input	Differential analog positive input 1
IN8N(1)	2A	Analog input	Differential analog negative input 8 (ADS1298 only)
IN7N(1)	2B	Analog input	Differential analog negative input 7 (ADS1298 only)
IN6N(1)	2C	Analog input	Differential analog negative input 6 (ADS1296/8 only)
IN5N(1)	2D	Analog input	Differential analog negative input 5 (ADS1296/8 only)
IN4N(1)	2E	Analog input	Differential analog negative input 4
IN3N(1)	2F	Analog input	Differential analog negative input 3
IN2N(1)	2G	Analog input	Differential analog negative input 2
IN1N(1)	2H	Analog input	Differential analog negative input 1

(1) Connect unused analog inputs IN1x to IN8x to AVDD.

BGA PIN ASSIGNMENTS (continued)

NAME	TERMINAL	FUNCTION	DESCRIPTION
RLDIN	3A	Analog input	Right leg drive input to MUX
RLDOUT	3B	Analog output	Right leg drive output
RLDINV	3C	Analog input/output	Right leg drive inverting input
WCT	3D	Analog output	Wilson Central Terminal output
TESTP_PACE_OUT1	3E	Analog input/buffer output	Internal test signal/single-ended buffer output based on register settings
TESTN_PACE_OUT2	3F	Analog input/output	Internal test signal/single-ended buffer output based on register settings
VCAP4	3G	Analog output	Analog bypass capacitor
VREFP	3H	Analog input/output	Positive reference voltage
AVDD	4A	Supply	Analog supply
AVDD	4B	Supply	Analog supply
RLDREF	4C	Analog input	Right leg drive noninverting input
AVSS	4D	Supply	Analog ground
RESV1	4E	Digital input	Reserved for future use. Must tie to logic low (DGND)
RESV2	4F	Analog output	Reserved for future use
RESV3	4G	Analog output	Reserved for future use
VREFN	4H	Analog input	Negative reference voltage
AVSS	5A	Supply	Analog ground
AVSS	5B	Supply	Analog ground
AVSS	5C	Supply	Analog ground
AVSS	5D	Supply	Analog ground
GPIO4	5E	Digital input/output	GPIO4 in normal mode, RESP_PH in respiration mode
GPIO1	5F	Digital input/output	General purpose input/output pin
$\overline{\text{PWDN}}$	5G	Digital input	Power-down; active low
VCAP1	5H	Analog input/output	Analog bypass capacitor
AVDD	6A	Supply	Analog supply
AVDD	6B	Supply	Analog supply
AVDD	6C	Supply	Analog supply
$\overline{\text{DRDY}}$	6D	Digital output	Data ready; active low
GPIO3	6E	Digital input/output	GPIO3 in normal mode, RESP in respiration mode
DAISY_IN	6F	Digital input	Daisy-chain input
$\overline{\text{RESET}}$	6G	Digital input	System reset; active low
VCAP2	6H	—	Analog bypass capacitor
AVDD1	7A	Supply	Analog supply for charge pump
VCAP3	7B	—	Analog bypass capacitor
DGND	7C	Supply	Digital ground
DGND	7D	Supply	Digital ground
GPIO2	7E	Digital input/output	General-purpose input/output pin
$\overline{\text{CS}}$	7F	Digital input	SPI chip select; active low
START	7G	Digital input	Start conversion
DGND	7H	Supply	Digital ground
AVSS1	8A	Supply	Analog ground for charge pump
CLKSEL	8B	Digital input	Master clock select
DVDD	8C	Supply	Digital power supply
DVDD	8D	Supply	Digital power supply
DOUT	8E	Digital output	SPI data out
SCLK	8F	Digital input	SPI clock
CLK	8G	Digital input	Master clock input
DIN	8H	Digital input	SPI data in

PAG PACKAGE
TQFP-64
(TOP VIEW)



PAG PIN ASSIGNMENTS

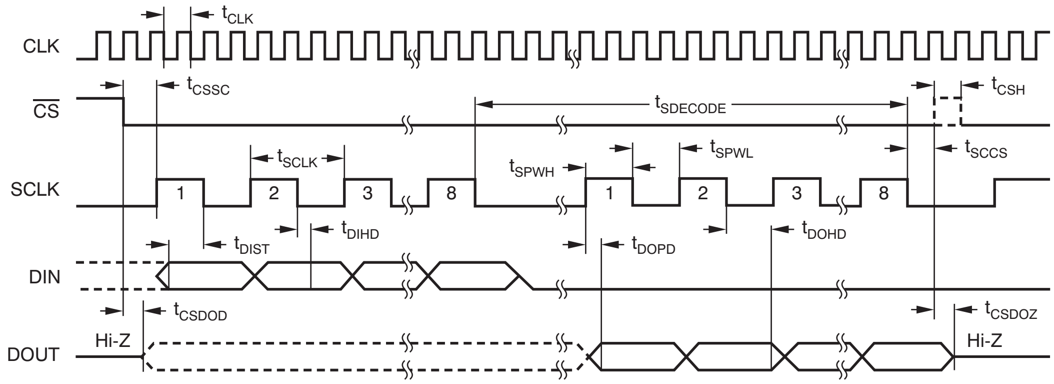
NAME	TERMINAL	FUNCTION	DESCRIPTION
IN8N(1)	1	Analog input	Differential analog negative input 8 (ADS1298 only)
IN8P(1)	2	Analog input	Differential analog positive input 8 (ADS1298 only)
IN7N(1)	3	Analog input	Differential analog negative input 7 (ADS1298 only)
IN7P(1)	4	Analog input	Differential analog positive input 7 (ADS1298 only)
IN6N(1)	5	Analog input	Differential analog negative input 6 (ADS1296/8 only)
IN6P(1)	6	Analog input	Differential analog positive input 6 (ADS1296/8 only)
IN5N(1)	7	Analog input	Differential analog negative input 5 (ADS1296/8 only)
IN5P(1)	8	Analog input	Differential analog positive input 5 (ADS1296/8 only)
IN4N(1)	9	Analog input	Differential analog negative input 4
IN4P(1)	10	Analog input	Differential analog positive input 4
IN3N(1)	11	Analog input	Differential analog negative input 3
IN3P(1)	12	Analog input	Differential analog positive input 3
IN2N(1)	13	Analog input	Differential analog negative input 2
IN2P(1)	14	Analog input	Differential analog positive input 2

(1) Connect unused analog inputs IN1x to IN8x to AVDD.

PAG PIN ASSIGNMENTS (continued)

NAME	TERMINAL	FUNCTION	DESCRIPTION
IN1N[(1)]	15	Analog input	Differential analog negative input 1
IN1P[(1)]	16	Analog input	Differential analog positive input 1
TESTP_PACE_OUT1	17	Analog input/buffer output	Internal test signal/single-ended buffer output based on register settings
TESTN_PACE_OUT2	18	Analog input/output	Internal test signal/single-ended buffer output based on register settings
AVDD	19	Supply	Analog supply
AVSS	20	Supply	Analog ground
AVDD	21	Supply	Analog supply
AVDD	22	Supply	Analog supply
AVSS	23	Supply	Analog ground
VREFP	24	Analog input/output	Positive reference voltage
VREFN	25	Analog input	Negative reference voltage
VCAP4	26	Analog output	Analog bypass capacitor
NC	27	—	No connection
VCAP1	28	—	Analog bypass capacitor
NC	29	—	No connection
VCAP2	30	—	Analog bypass capacitor
RESV1	31	Digital input	Reserved for future use. Must tie to logic low (DGND)
AVSS	32	Supply	Analog ground
DGND	33	Supply	Digital ground
DIN	34	Digital input	SPI data in
$\overline{\text{PWDN}}$	35	Digital input	Power-down; active low
$\overline{\text{RESET}}$	36	Digital input	System reset; active low
CLK	37	Digital input	Master clock input
START	38	Digital input	Start conversion
$\overline{\text{CS}}$	39	Digital input	SPI chip select; active low
SCLK	40	Digital input	SPI clock
DAISY_IN	41	Digital input	Daisy-chain input
GPIO1	42	Digital input/output	General purpose input/output pin
DOUT	43	Digital output	SPI data out
GPIO2	44	Digital input/output	General-purpose input/output pin
GPIO3	45	Digital input/output	GPIO3 in normal mode, RESP in respiration mode
GPIO4	46	Digital input/output	GPIO4 in normal mode, RESP_PH in respiration mode
$\overline{\text{DRDY}}$	47	Digital output	Data ready; active low
DVDD	48	Supply	Digital power supply
DGND	49	Supply	Digital ground
DVDD	50	Supply	Digital power supply
DGND	51	Supply	Digital ground
CLKSEL	52	Digital input	Master clock select
AVSS1	53	Supply	Analog ground
AVDD1	54	Supply	Analog supply
VCAP3	55	Analog	Analog bypass capacitor
AVDD	56	Supply	Analog supply
AVSS	57	Supply	Analog ground
AVSS	58	Supply	Analog ground for charge pump
AVDD	59	Supply	Analog supply for charge pump
RLDREF	60	Analog input	Right leg drive noninverting input
RLDINV	61	Analog input/output	Right leg drive inverting input
RLDIN	62	Analog input	Right leg drive input to MUX
RLDOUT	63	Analog output	Right leg drive output
WCT	64	Analog output	Wilson Central Terminal output

TIMING CHARACTERISTICS



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 1. Serial Interface Timing

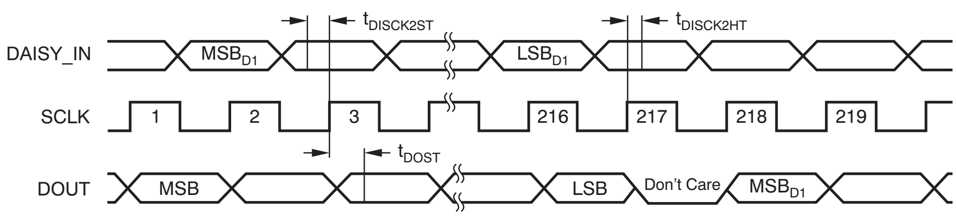


Figure 2. Daisy-Chain Interface Timing

Timing Requirements For Figure 1 and Figure 2

Specifications apply from 0°C to +70°C. Load on D_{OUT} = 20pF || 100kΩ.

PARAMETER	DESCRIPTION	2.7V ≤ DVDD ≤ 3.6V MIN	TYP	MAX	1.65V ≤ DVDD ≤ 2V MIN	TYP	MAX	UNIT
t_{CLK}	Master clock period	414		514	414		514	ns
t_{CSSC}	$\overline{CS}$ low to first SCLK, setup time	6			17			ns
t_{SCLK}	SCLK period	50			66.6			ns
$t_{SPWH, L}$	SCLK pulse width, high and low	15			25			ns
t_{DIST}	DIN valid to SCLK falling edge: setup time	10			10			ns
t_{DIHD}	Valid DIN after SCLK falling edge: hold time	10			11			ns
t_{DOHD}	SCLK falling edge to invalid DOUT: hold time	10			10			ns
t_{DOPD}	SCLK rising edge to DOUT valid: setup time			17			32	ns
t_{CSH}	$\overline{CS}$ high pulse	2			2			t_{CLK}s
t_{CSDOD}	$\overline{CS}$ low to DOUT driven	10			20			ns
t_{SCCS}	Eighth SCLK falling edge to $\overline{CS}$ high	4			4			t_{CLK}s
$t_{SDECODE}$	Command decode time	4			4			t_{CLK}s
t_{CSDOZ}	$\overline{CS}$ high to DOUT Hi-Z			10			20	ns
$t_{DISCK2ST}$	DAISY_IN valid to SCLK rising edge: setup time	10			10			ns
$t_{DISCK2HT}$	DAISY_IN valid after SCLK rising edge: hold time	10			10			ns

TYPICAL CHARACTERISTICS

All plots at T_A = +25°C, AVDD = 3V, AVSS = 0V, DVDD = 1.8V, internal VREFP = 2.4V, VREFN = AVSS, external clock = 2.048MHz, data rate = 500SPS, High-Resolution mode, and gain = 6, unless otherwise noted.

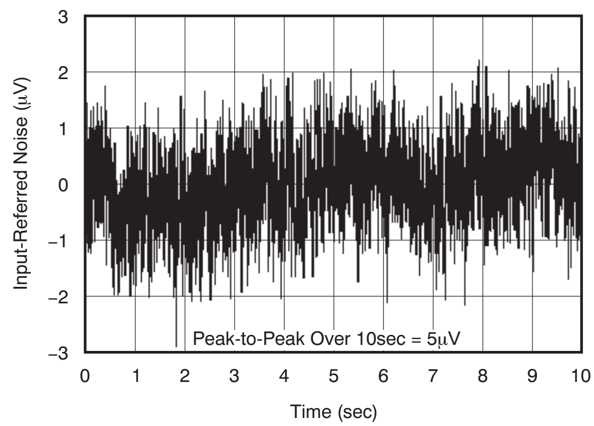


Figure 3.

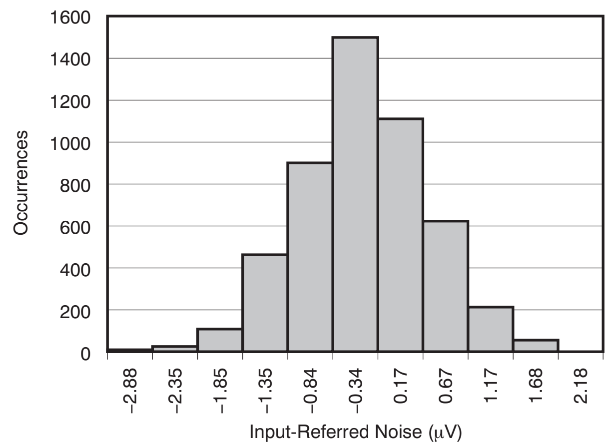


Figure 4.

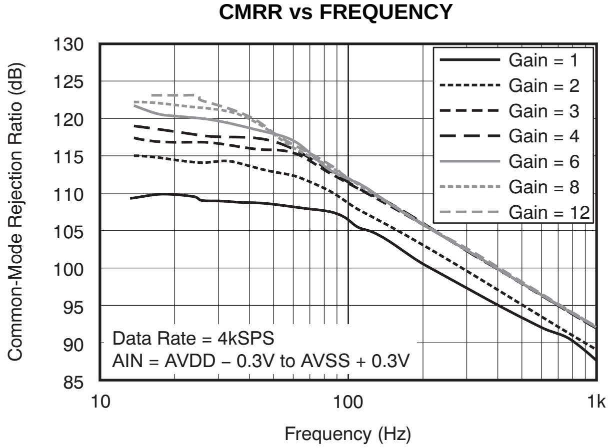


Figure 5.

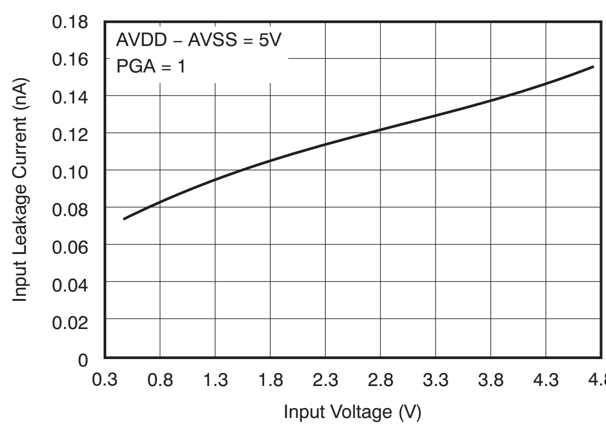


Figure 6.

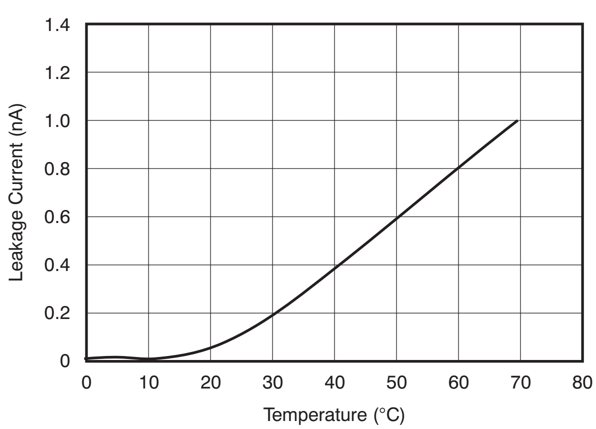


Figure 7.

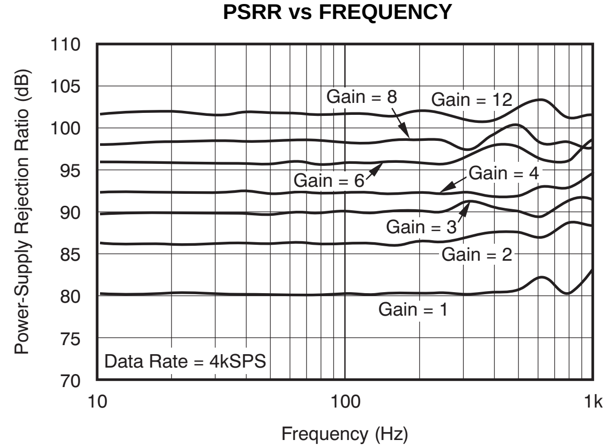


Figure 8.

TYPICAL CHARACTERISTICS (continued)

All plots at T_A = +25°C, AVDD = 3V, AVSS = 0V, DVDD = 1.8V, internal VREFP = 2.4V, VREFN = AVSS, external clock = 2.048MHz, data rate = 500SPS, High-Resolution mode, and gain = 6, unless otherwise noted.

THD vs FREQUENCY

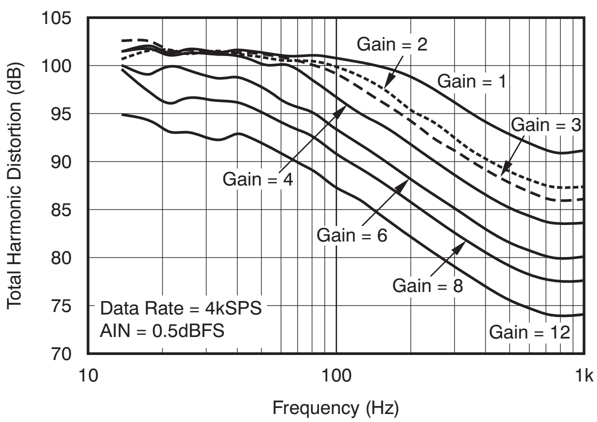


Figure 9.

INL vs PGA GAIN

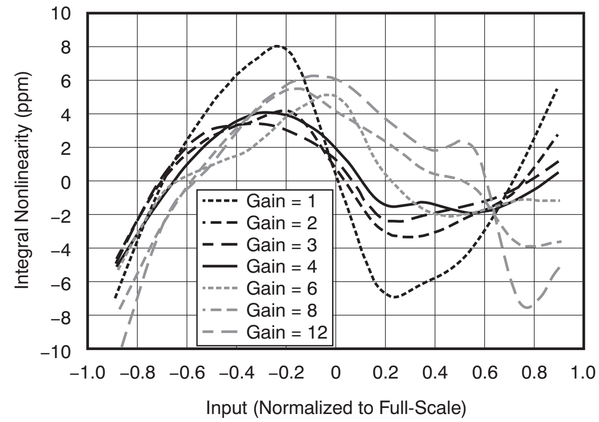


Figure 10.

INL vs TEMPERATURE

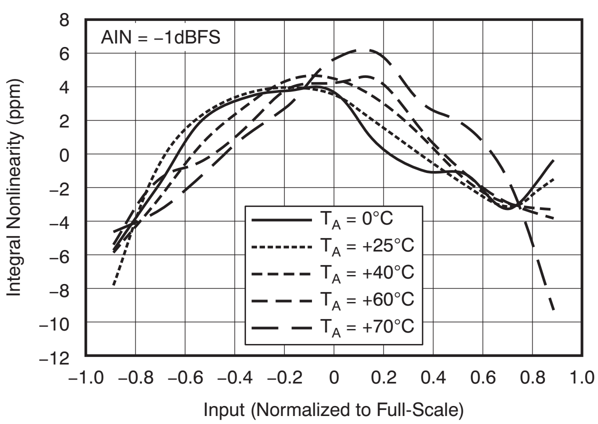


Figure 11.

THD FFT PLOT
(60Hz Signal)

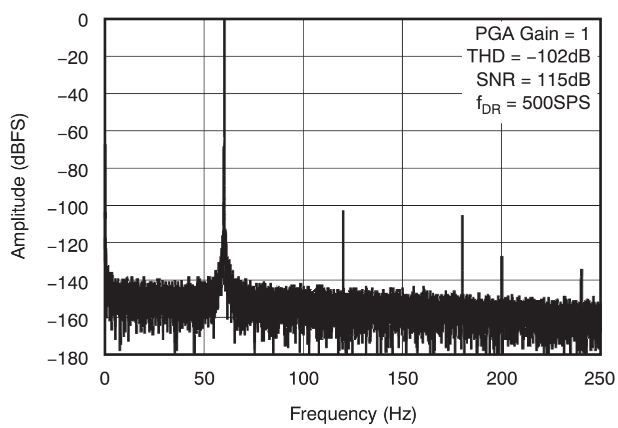


Figure 12.

TYPICAL CHARACTERISTICS (continued)

All plots at T_A = +25°C, AVDD = 3V, AVSS = 0V, DVDD = 1.8V, internal VREFP = 2.4V, VREFN = AVSS, external clock = 2.048MHz, data rate = 500SPS, High-Resolution mode, and gain = 6, unless otherwise noted.

FFT PLOT
(60Hz Signal)

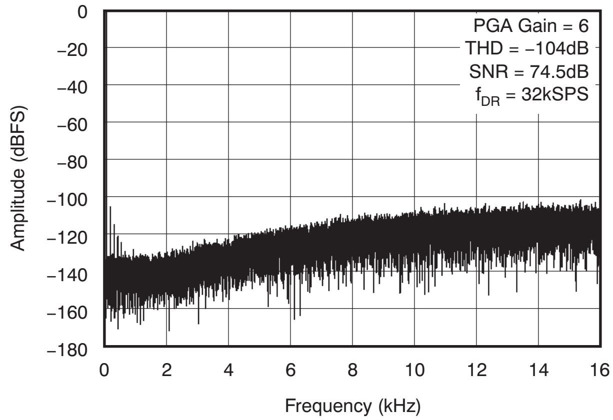


Figure 13.

OFFSET vs PGA GAIN
(ABSOLUTE VALUE)

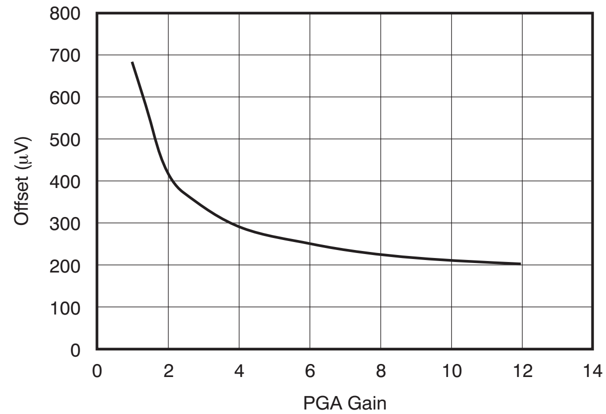


Figure 14.

TEST SIGNAL AMPLITUDE ACCURACY

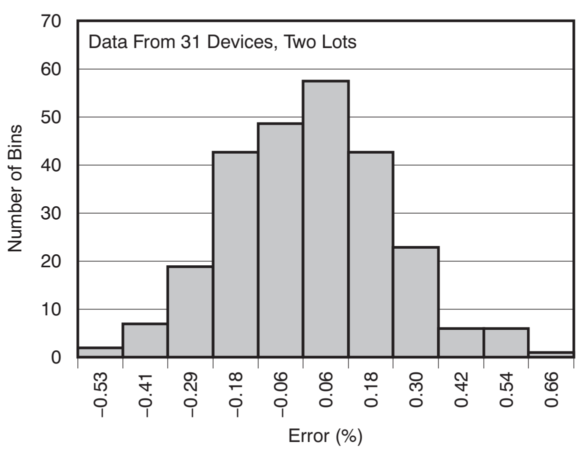


Figure 15.

LEAD-OFF COMPARATOR THRESHOLD ACCURACY

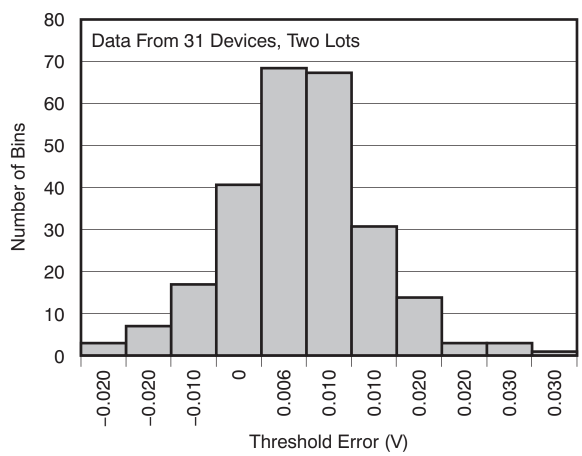


Figure 16.

LEAD-OFF CURRENT SOURCE ACCURACY DISTRIBUTION

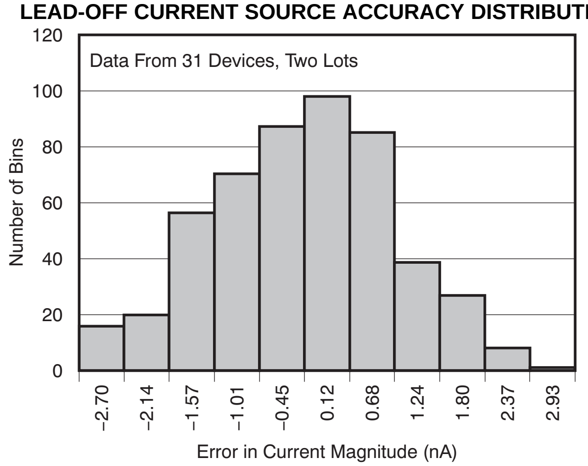


Figure 17.

OVERVIEW

The ADS1294/6/8 are low-power, multichannel, simultaneously-sampling, 24-bit delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with integrated programmable gain amplifiers (PGAs). These devices integrate various ECG-specific functions that make them well-suited for scalable electrocardiogram (ECG), electroencephalography (EEG), and electromyography (EMG) applications. The devices can also be used in high-performance, multichannel data acquisition systems by powering down the ECG-specific circuitry.

The ADS1294/6/8 have a highly programmable multiplexer that allows for temperature, supply, input short, and RLD measurements. Additionally, the multiplexer allows any of the input electrodes to be programmed as the patient reference drive. The PGA gain can be chosen from one of seven settings (1, 2, 3, 4, 6, 8, and 12). The ADCs in the device offer data rates from 250SPS to 32kSPS. Communication to the device is accomplished using an SPI-compatible interface. The device provides four GPIO pins for general use. Multiple devices can be synchronized using the START pin.

The internal reference can be programmed to either 2.4V or 4V. The internal oscillator generates a 2.048MHz clock. The versatile right leg drive (RLD) block allows the user to choose the average of any combination of electrodes to generate the patient drive signal. Lead-off detection can be accomplished either by using a pull-up/pull-down resistor or a current source/sink. An internal ac lead-off detection feature is also available. The device supports both hardware pace detection and software pace detection. The Wilson Central Terminal (WCT) block can be used to generate the WCT point of the standard 12-lead ECG.

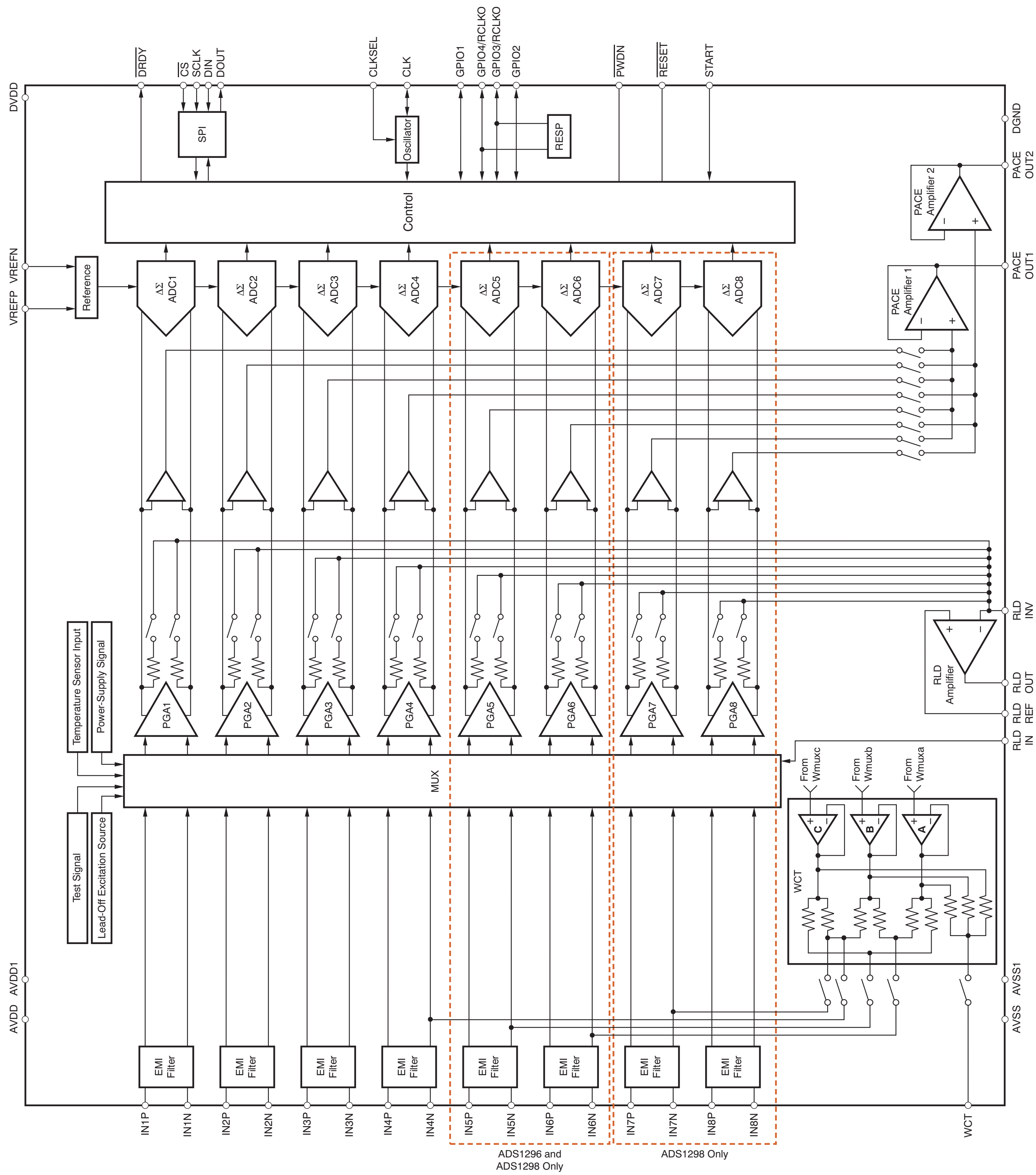


Figure 18. Functional Block Diagram

THEORY OF OPERATION

This section contains details of the ADS1294/6/8 internal functional elements. The analog blocks are discussed first followed by the digital interface. Blocks implementing ECG-specific functions are covered in the end.

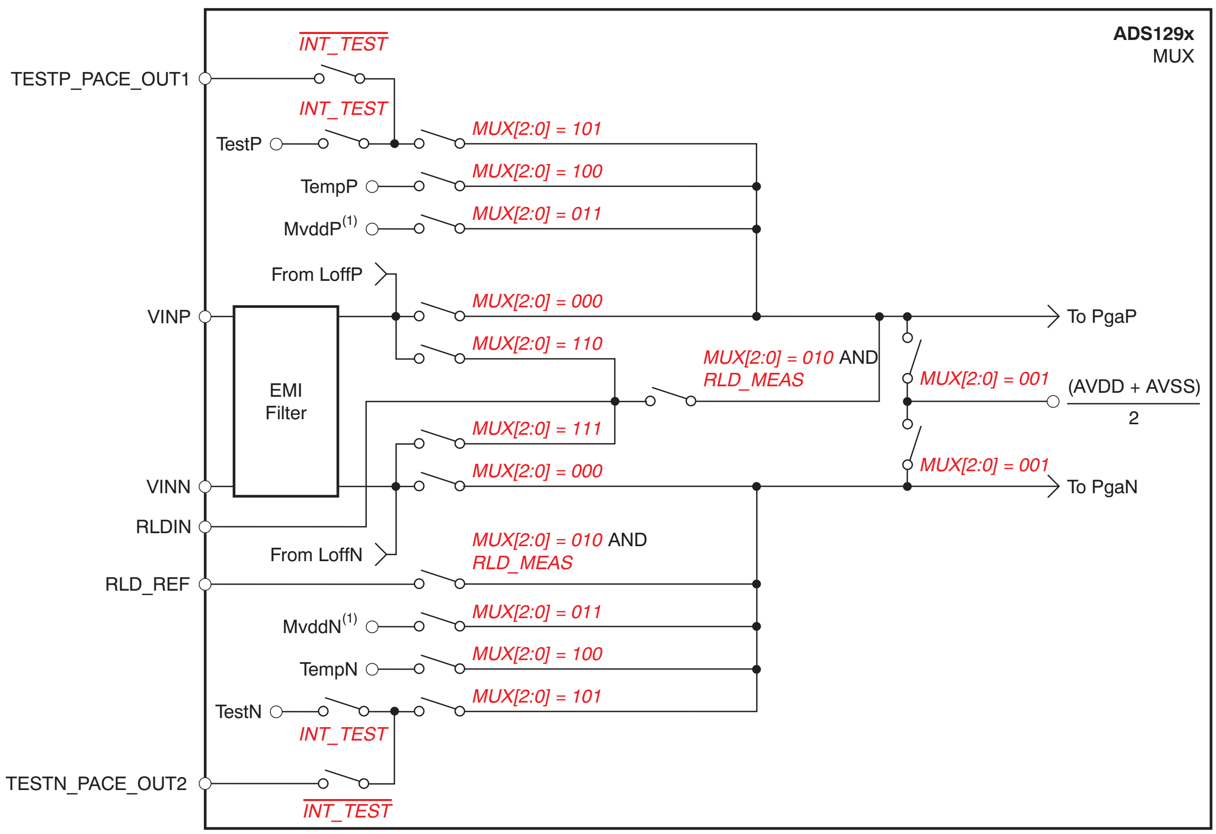
Throughout this document, f_{CLK} denotes the frequency of the signal at the CLK pin, t_{CLK} denotes the period of the signal at the CLK pin, f_{DR} denotes the output data rate, t_{DR} denotes the time period of the output data, and f_{MOD} denotes the frequency at which the modulator samples the input.

EMI FILTER

An RC filter at the input acts as an EMI filter on all of the channels. The –3dB filter bandwidth is approximately 3MHz.

INPUT MULTIPLEXER

The ADS1294/6/8 input multiplexers are very flexible and provide many configurable signal switching options. Figure 19 shows the multiplexer on a single channel of the device. Note that the device has eight such blocks, one for each channel. TEST_PACE_OUT1, TEST_PACE_OUT2, and RLD_IN are common to all eight blocks. VINP and VINN are separate for each of the eight blocks. This flexibility allows for significant device and sub-system diagnostics, calibration and configuration. Selection of switch settings for each channel is made by writing the appropriate values to the CHnSET[2:0] register (see the *CHnSET: Individual Channel Settings* section for details) and by writing the RLD_MEAS bit in the CONFIG3 register (see the *CONFIG3: Configuration Register 3* subsection of the *Register Map* section for details). More details of the ECG-specific features of the multiplexer are discussed in the *Input Multiplexer* subsection of the *ECG-Specifc Functions* section.



(1) MVDD monitor voltage supply depends on channel number; see the *Supply Measurements (MVDDP, MVDDN)* section.

Figure 19. Input Multiplexer Block for One Channel

Device Noise Measurements

Setting CHnSET[2:0] = 001 sets the common-mode voltage of (AVDD + AVSS)/2 to both inputs of the channel. This setting can be used to test the inherent noise of the device in the user system.

Test Signals (TestP and TestN)

Setting CHnSET[2:0] = 101 provides internally-generated test signals for use in sub-system verification at power-up. This functionality allows the entire signal chain to be tested out. Although the test signals are similar to the CAL signals described in the IEC60601-2-51 specification, this feature is not intended for use in compliance testing.

Control of the test signals is accomplished through register settings (see the *CONFIG2: Configuration Register 2* subsection in the *Register Map* section for details). TEST_AMP controls the signal amplitude and TEST_FREQ controls switching at the required frequency.

The test signals are multiplexed and transmitted out of the device at the TESTP_PACE_OUT1 and TESTN_PACE_OUT2 pins. A bit register (CONFIG2.INT_TEST = 0) deactivates the internal test signals so that the test signal can be driven externally. This feature allows the calibration of multiple devices with the same signal. The test signal feature cannot be used in conjunction with the external hardware pace feature (see the *External Hardware Approach* subsection of the *ECG-Specific Functions* section for details).

Auxiliary Differential Input (TESTP_PACE_OUT1, TESTN_PACE_OUT2)

When hardware pace detect is not used, the TESTP_PACE_OUT1 and TESPN_PACE_OUT2 signals can be used as a multiplexed differential input channel. These inputs can be multiplexed to any of the eight channels. The performance of the differential input signal fed through these pins is identical to the normal channel performance.

Temperature Sensor (TempP, TempN)

The ADS1294/6/8 contain an on-chip temperature sensor. This sensor uses two internal diodes with one diode having a current density 16x that of the other, as shown in Figure 20. The difference in current densities of the diodes yields a difference in voltage that is proportional to absolute temperature.

As a result of the low thermal resistance of the package to the printed circuit board (PCB), the internal device temperature tracks the PCB temperature closely. Note that self-heating of the ADS1294/6/8 causes a higher reading than the temperature of the surrounding PCB.

The scale factor of Equation 1 converts the temperature reading to °C. Before using this equation, the temperature reading code must first be scaled to μV.

$$\text{Temperature }(^\circ\text{C}) = \left(\frac{\text{Temperature Reading }(\mu\text{V}) - 145{,}300\mu\text{V}}{490\mu\text{V}/^\circ\text{C}}\right) + 25^\circ\text{C} \quad (1)$$

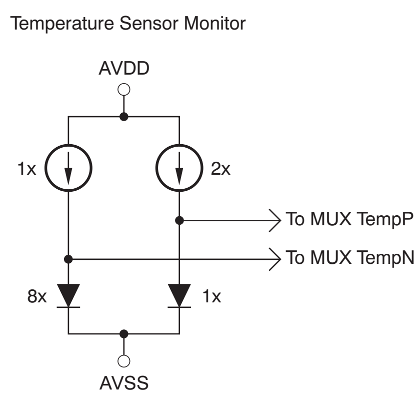


Figure 20. Measurement of the Temperature Sensor in the Input

Supply Measurements (MVDDP, MVDDN)

Setting CHnSET[2:0] = 011 sets the channel inputs to different supply voltages of the device. For channels 1, 2, 5, 6, 7, and 8, (MVDDP – MVDDN) is [0.5 × (AVDD + AVSS)]; for channel 3 and for channel 4, (MVDDP – MVDDN) is DVDD/4. Note that to avoid saturating the PGA while measuring power supplies, the gain must be set to '1'.

Lead-Off Excitation Signals (LoffP, LoffN)

The lead-off excitation signals are fed into the multiplexer before the switches. The comparators that detect the lead-off condition are also connected to the multiplexer block before the switches. For a detailed description of the lead-off block, refer to the *Lead-Off Detection* subsection in the *ECG-Specific Functions* section.

Auxiliary Single-Ended Input

The RLD_IN pin is primarily used for routing the right leg drive signal to any of the electrodes in case the right leg drive electrode falls off. However, the RLD_IN pin can be used as a multiple single-ended input channel. The signal at the RLD_IN pin can be measured with respect to the voltage at the RLD_REF pin using any of the eight channels. This measurement is done by setting the channel multiplexer setting to '010' and the RLD_MEAS bit of the CONFIG3 register to '1'.

ANALOG INPUT

The analog input to the ADS1298 is fully differential. Assuming PGA = 1, the input (INP – INN) can span between $-V_{REF}$ to $+V_{REF}$. Refer to Table 8 for an explanation of the correlation between the analog input and the digital codes. There are two general methods of driving the analog input of the ADS1298: single-ended or differential, as shown in Figure 21 and Figure 22. Note that INP and INN are 180°C out-of-phase in the differential input method. When the input is single-ended, the INN input is held at the common-mode voltage, preferably at mid-supply. The INP input swings around the same common voltage and the peak-to-peak amplitude is the (common-mode + $1/2V_{REF}$) and the (common-mode – $1/2V_{REF}$). When the input is differential, the common-mode is given by (INP + INN)/2. Both the INP and INN inputs swing from (common-mode + $1/2V_{REF}$ to common-mode – $1/2V_{REF}$). For optimal performance, it is recommended that the ADS1298 be used in a differential configuration.

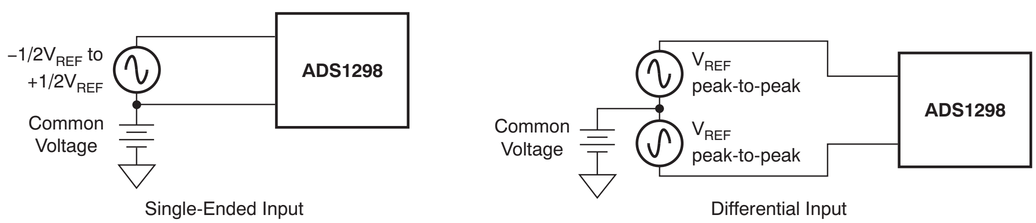
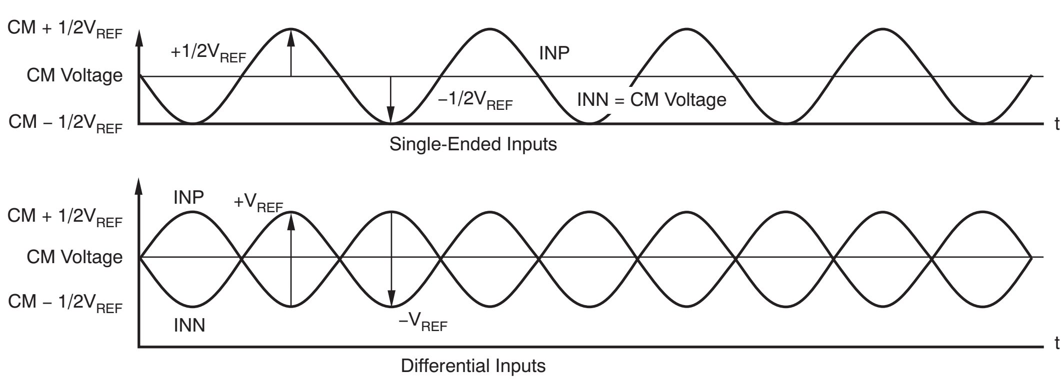


Figure 21. Methods of Driving the ADS1298: Single-Ended or Differential



$$\text{Common-Mode Voltage (Differential Mode)} = \frac{(INP) + (INN)}{2}, \text{ Common-Mode Voltage (Single-Ended Mode)} = INN.$$

$$\text{Input Range (Differential Mode)} = (AINP - AINN) = V_{REF} - (-V_{REF}) = 2V_{REF}.$$

Figure 22. Using the ADS1298 in the Single-Ended and Differential Input Modes

PGA SETTINGS AND INPUT RANGE

The PGA is a differential input/differential output amplifier, as shown in Figure 23. It has seven gain settings (1, 2, 3, 4, 6, 8, and 12) that can be set by writing to the CHnSET register (see the *CHnSET: Individual Channel Settings* subsection of the *Register Map* section for details). The ADS1294/6/8 have CMOS inputs and hence have negligible current noise. Table 6 shows the typical values of bandwidths for various gain settings. Note that Table 6 shows the small-signal bandwidth. For large signals, the performance is limited by the slew rate of the PGA.

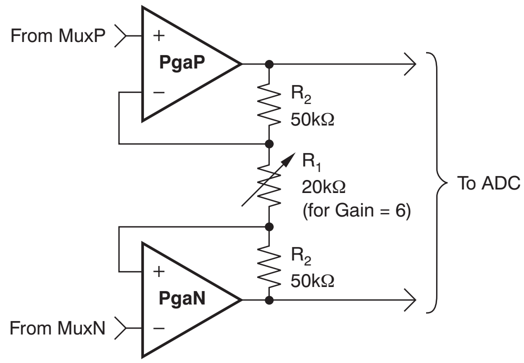


Figure 23. PGA Implementation

Table 6. PGA Gain versus Bandwidth

GAIN	NOMINAL BANDWIDTH AT ROOM TEMPERATURE (kHz)
1	237
2	146
3	127
4	96
6	64
8	48
12	32

The resistor string of the PGA that implements the gain has 120kΩ of resistance for a gain of 6. This resistance provides a current path across the outputs of the PGA in the presence of a differential input signal. This current is in addition to the quiescent current specified for the device in the presence of differential signal at input.

Input Common-Mode Range

The usable input common-mode range of the front end depends on various parameters, including the maximum differential input signal, supply voltage, PGA gain, etc. This range is described in Equation 2:

$$AVDD - 0.2 - \left(\frac{Gain\ V_{MAX\_DIFF}}{2}\right) > CM > AVSS + 0.2 + \left(\frac{Gain\ V_{MAX\_DIFF}}{2}\right)$$

where:

V_{MAX_DIFF} = maximum differential signal at the input of the PGA

CM = common-mode range (2)

For example:

If V_{DD} = 3V, gain = 6, and V_{MAX_DIFF} = 350mV
Then 1.25V < CM < 1.75V

Input Differential Dynamic Range

The differential (INP – INN) signal range depends on the analog supply and reference used in the system. This range is shown in Equation 3.

$$\text{Max (INP – INN)} < \frac{V_{REF}}{Gain}; \quad \text{Full-Scale Range} = \frac{\pm V_{REF}}{Gain} = \frac{2V_{REF}}{Gain} \tag{3}$$

The 3V supply, with a reference of 2.4V and a gain of 6 for ECGs, is optimized for power with a differential input signal of approximately 300mV. For higher dynamic range, a 5V supply with a reference of 4V (set by the VREF_4V bit of the CONFIG3 register) can be used to increase the differential dynamic range.

ADC ΔΣ Modulator

Each channel of the ADS1294/6/8 has a 24-bit ΔΣ ADC. This converter uses a second-order modulator optimized for low-power applications. The modulator samples the input signal at the rate of $f_{MOD} = f_{CLK}/4$ for high-resolution mode and $f_{MOD} = f_{CLK}/8$ for the low-power mode. As in the case of any ΔΣ modulator, the noise of the ADS1294/6/8 is shaped until $f_{MOD}/2$, as shown in Figure 24. The on-chip digital decimation filters explained in the next section can be used to filter out the noise at higher frequencies. These on-chip decimation filters also provide antialias filtering. This feature of the ΔΣ converters drastically reduces the complexity of the analog antialiasing filters that are typically needed with nyquist ADCs.

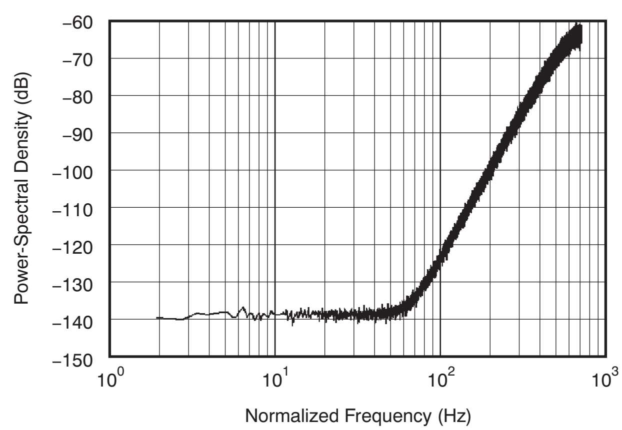


Figure 24. Modulator Noise Spectrum Up To 0.5 × f_{MOD}

DIGITAL DECIMATION FILTER

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rates. Higher data rates are typically used in ECG applications for implement software pace detection and ac lead-off detection.

The digital filter on each channel consists of a third-order sinc filter. The decimation ratio on the sinc filters can be adjusted by the DR bits in the CONFIG2 register (see the *Register Map* section for details). This setting is a global setting that affects all channels and, therefore, in a device all channels operate at the same data rate.

Sinc Filter Stage (sinx/x)

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD}. The sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream into parallel data. The decimation rate affects the overall data rate of the converter.

Equation 4 shows the scaled Z-domain transfer function of the sinc filter.

$$|H(z)| = \left| \frac{1 - Z^{-N}}{1 - Z^{-1}} \right|^3 \quad (4)$$

The frequency domain transfer function of the sinc filter is shown in Equation 5.

$$|H(f)| = \left| \frac{\sin\left(\frac{N4\pi \times f}{f_{CLK}}\right)}{N\left(\frac{4\pi \times f}{f_{CLK}}\right)} \right|^3$$

where:

N = decimation ratio (5)

The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. Figure 25 shows the frequency response of the sinc filter and Figure 26 shows the roll-off of the sinc filter. With a step change at input, the filter takes 3 × t_{DR} to settle. After a rising edge of the START signal, the filter takes t_{SETTLE} time to give the first data output. The settling time of the filters at various data rates are discussed in the *START* subsection of the *SPI Interface* section. Figure 27 and Figure 28 show the filter transfer function until $f_{MOD}/2$ and $f_{MOD}/16$, respectively, at different data rates. Figure 29 shows the transfer function extended until 4 × f_{MOD}. It can be seen that the passband of the ADS1294/6/8 repeats itself at every f_{MOD}. The input R-C anti-aliasing filters in the system should be chosen such that any interference in frequencies around multiples of f_{MOD} are attenuated sufficiently.

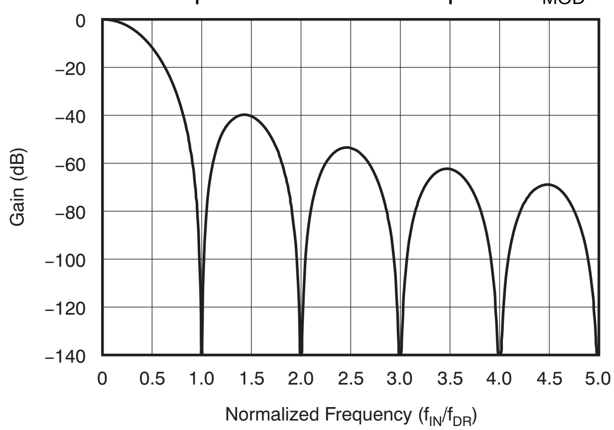


Figure 25. Sinc Filter Frequency Response

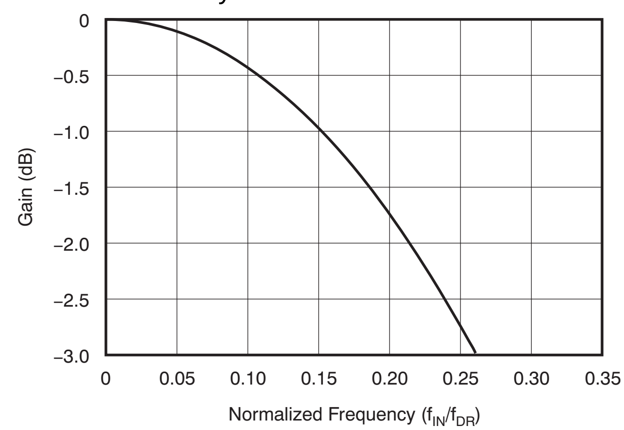


Figure 26. Sinc Filter Roll-Off

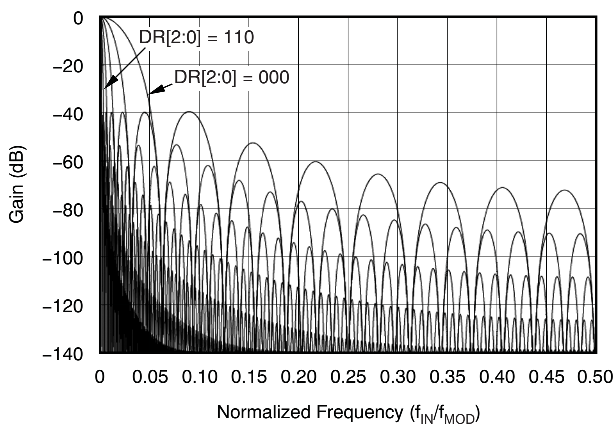


Figure 27. Transfer Function of On-Chip Decimation Filters Until $f_{MOD}/2$

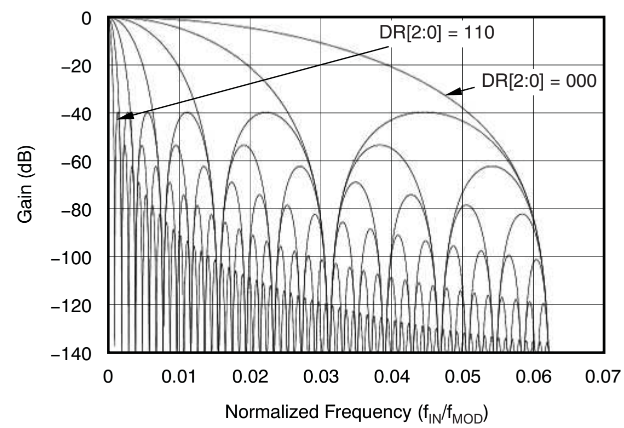


Figure 28. Transfer Function of On-Chip Decimation Filters Until $f_{MOD}/16$

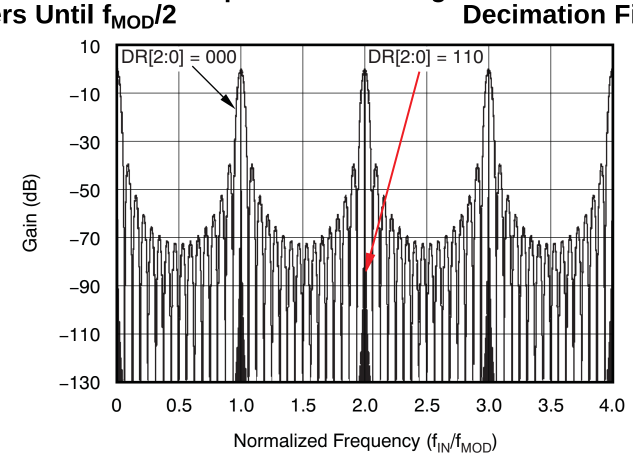
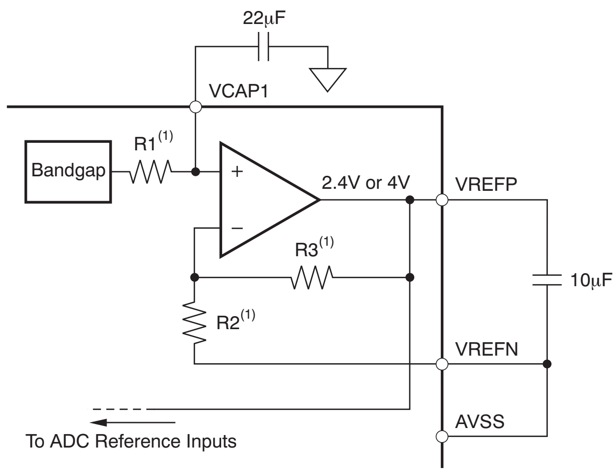


Figure 29. Transfer Function of On-Chip Decimation Filters Until $4f_{MOD}$ for DR[2:0] = 000 and DR[2:0] = 110

REFERENCE

Figure 30 shows a simplified block diagram of the internal reference of the ADS1294/6/8. The reference voltage is generated with respect to AVSS. When using the internal voltage reference, connect VREFN to AVSS.



(1) For V_{REF} = 2.4V: R1 = 12.5kΩ, R2 = 25kΩ, and R3 = 25kΩ. For V_{REF} = 4V: R1 = 12.5kΩ, R2 = 15kΩ, and R3 = 35kΩ.

Figure 30. Internal Reference

The external band-limiting capacitors determine the amount of reference noise contribution. For high-end ECG systems, the capacitor values should be chosen such that the bandwidth is limited to less than 10Hz, so that the reference noise does not dominate the system noise. When using a 3V analog supply, the internal reference must be set to 2.4V. In case of a 5V analog supply, the internal reference can be set to 4V by setting the VREF_4V bit in the CONFIG2 register.

Alternatively, the internal reference buffer can be powered down and VREFP can be applied externally. Figure 31 shows a typical external reference drive circuitry. Power-down is controlled by the PD_REFBUF bit in the CONFIG3 register. This power-down is also used to share internal references when two devices are cascaded. By default the device wakes up in external reference mode.

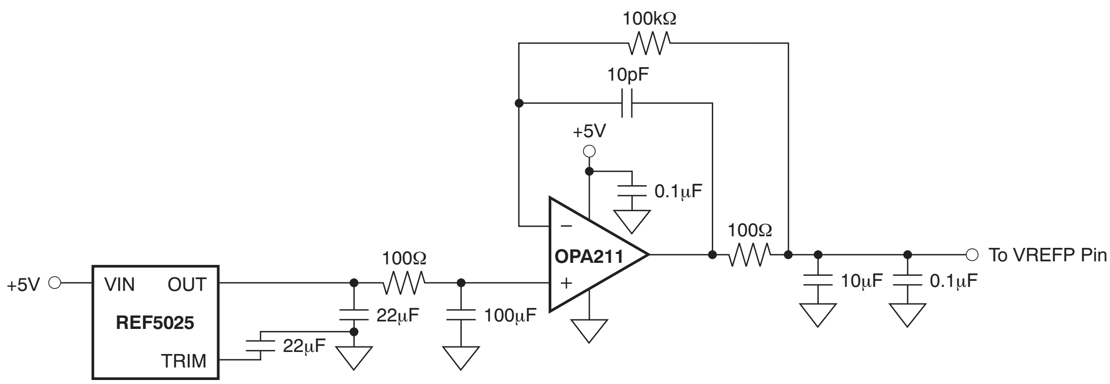


Figure 31. External Reference Driver

CLOCK

The ADS1294/6/8 provide two different methods for device clocking: internal and external. Internal clocking is ideally suited for low-power, battery-powered systems. The internal oscillator is trimmed for accuracy at room temperature. Over the specified temperature range the accuracy varies; see the Electrical Characteristics. Clock selection is controlled by the CLKSEL pin and the CLK_EN register bit.

The CLKSEL pin selects either the internal or external clock. The CLK_EN bit in the CONFIG1 register enables and disables the oscillator clock to be output in the CLK pin. A truth table for these two pins is shown in Table 7. The CLK_EN bit is useful when multiple devices are used in a daisy-chain configuration. It is recommended that during power-down the external clock is shut down to save power.

Table 7. CLKSEL Pin and CLK_EN Bit

CLKSEL PIN	CONFIG1.CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal clock oscillator	3-state
1	1	Internal clock oscillator	Output: internal clock oscillator

DATA FORMAT

The ADS1294/6/8 outputs 24 bits of data per channel in binary twos complement format, MSB first. The LSB has a weight of $V_{REF}/(2^{23} – 1)$. A positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 8 summarizes the ideal output codes for different input signals. Note that for DR[2:0] = 000 and 001, the device has only 17 and 19 bits of resolution, respectively.

Table 8. Ideal Input Code versus Input Signal

INPUT SIGNAL, V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(1)
$\geq V_{REF}$	7FFFFFh
$+V_{REF}/(2^{23} – 1)$	000001h
0	000000h
$–V_{REF}/(2^{23} – 1)$	FFFFFFh
$\leq –V_{REF}\ (2^{23}/2^{23} – 1)$	800000h

(1) Excludes effects of noise, linearity, offset, and gain error.

SPI INTERFACE

The SPI-compatible serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. The interface reads conversion data, reads and writes registers, and controls the ADS1294/6/8 operation. The $\overline{DRDY}$ output is used as a status signal to indicate when data are ready. $\overline{DRDY}$ goes low when new data are available.

Chip Select ($\overline{CS}$)

Chip select ($\overline{CS}$) selects the ADS1294/6/8 for SPI communication. $\overline{CS}$ must remain low for the entire duration of the serial communication. After the serial communication is finished, always wait four or more t_{CLK} cycles before taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK and DIN are ignored, and DOUT enters a high-impedance state. $\overline{DRDY}$ asserts when data conversion is complete, regardless of whether $\overline{CS}$ is high or low.

Serial Clock (SCLK)

SCLK is the serial peripheral interface (SPI) serial clock. It is used to shift in commands and shift out data from the device. The serial clock (SCLK) features a Schmitt-triggered input and clocks data on the DIN and DOUT pins into and out of the ADS1294/6/8. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally forcing a clock event. The absolute maximum limit for SCLK is specified in the *Serial Interface Timing* table. When shifting in commands with SCLK, make sure that the entire set of SCLKs is issued to the device. Failure to do so could result in the device serial interface being placed into an unknown state, requiring $\overline{CS}$ to be taken high to recover.

For a single device, the minimum speed needed for the SCLK depends on the number of channels, number of bits of resolution, and output data rate. (For multiple cascaded devices, see the *Cascade Mode* subsection of the *Multiple Device Configuration* section.)

$$t_{SCLK} < (t_{DR} - 4t_{CLK})/(N_{BITS} \times N_{CHANNELS} + 24) \quad (6)$$

For example, if the ADS1298 is used in a 500SPS mode (8 channels, 24-bit resolution), the minimum SCLK speed is 110kHz.

Data retrieval can be done either by putting the device in RDATAC mode or by issuing a RDATA command for data on demand. The above SCLK rate limitation applies to RDATAC. For the RDATA command, the limitation applies if data must be read in between two consecutive $\overline{DRDY}$ signals. The above calculation assumes that there are no other commands issued in between data captures.

Data Input (DIN)

The data input pin (DIN) is used along with SCLK to communicate with the ADS1294/6/8 (opcode commands and register data). The device latches data on DIN on the falling edge of SCLK.

Data Output (DOUT)

The data output pin (DOUT) is used with SCLK to read conversion and register data from the ADS1294/6/8. Data on DOUT are shifted out on the rising edge of SCLK. DOUT goes to a high-impedance state when CS is high. In read data continuous mode (see the *SPI Command Definitions* section for more details), the DOUT output line also indicates when new data are available. This feature can be used to minimize the number of connections between the device and the system controller.

Figure 32 shows the data output protocol for ADS1298.

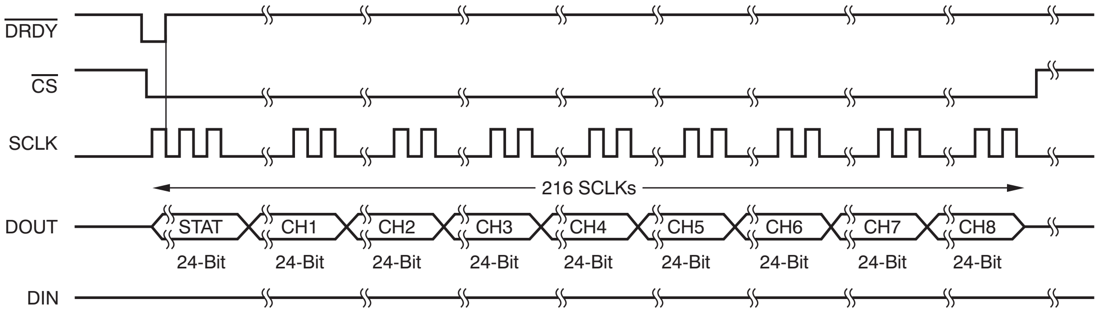


Figure 32. SPI Bus Data Output for the ADS1298 (8-Channels)

Data Retrieval

Data retrieval can be accomplished in one of two methods. The read data continuous command (see the *RDATAC: Read Data Continuous* section) can be used to set the device in a mode to read the data continuously without sending opcodes. The read data command (see the *RDATA: Read Data* section) can be used to read just one data output from the device (see the *SPI Command Definitions* section for more details). The conversion data are read by shifting the data out on DOUT. The MSB of the data on DOUT is clocked out on the first SCLK rising edge. DRDY returns to high on the first SCLK falling edge. DIN should remain low for the entire read operation.

The number of bits in the data output depends on the number of channels and the number of bits per channel. For the ADS1298, the number of data outputs is (24 status bits + 24 bits × 8 channels) = 216 bits. The format of the 24 status bits is: (1100 + LOFF_STATP + LOFF_STATN + bits[4:7] of the GPIO register). The data format for each channel data are twos complement and MSB first. When channels are powered down using the user register setting, the corresponding channel output is set to '0'. However, the sequence of channel outputs remains the same. For the ADS1294 and the ADS1296, the last four and two channel outputs are set to '0', respectively.

The ADS1294/6/8 also provide a multiple readback feature. The data can be read out multiple times by simply giving more SCLKs, in which case the MSB data byte repeats after reading the last byte. The DAISY_EN bit in CONFIG1 register must be set to '1' for multiple readbacks.

Data Ready (DRDY)

DRDY is an output. When it transitions low new conversion data are ready. The CS signal has no effect on the data ready signal. The behavior of DRDY is determined by whether the device is in RDATAC mode or the RDATA command is being used to read data on demand. (See the *RDATAC: Read Data Continuous* and *RDATA: Read Data* subsections of the *SPI Command Definitions* section for further details).

When reading data with the RDATA command, the read operation can overlap the occurrence of the next DRDY without data corruption.

The START pin or the START command is used to place the device either in normal data capture mode or pulse data capture mode.

Figure 33 shows the relationship between DRDY, DOUT, and SCLK during data retrieval (in case of an ADS1298 with a selected data rate that gives 24-bit resolution). DOUT is latched out at the rising edge of SCLK. DRDY is pulled high at the falling edge of SCLK. Note that DRDY goes high on the first falling edge SCLK regardless of whether data are being retrieved from the device or a command is being sent through the DIN pin.

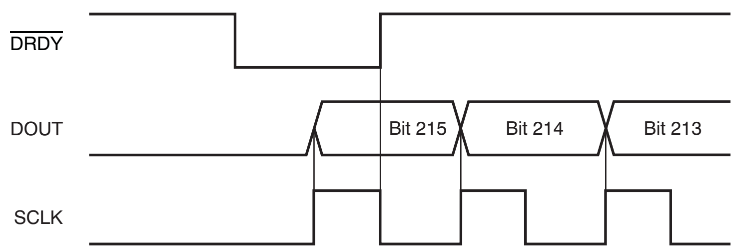


Figure 33. DRDY with Data Retrieval (CS = 0)

GPIO

The ADS1294/6/8 have a total of four general-purpose digital I/O (GPIO) pins available in the normal mode of operation. The digital I/O pins are individually configurable as either inputs or as outputs through the GPIOC bits register. The GPIOD bits in the GPIO register control the level of the pins. When reading the GPIOD bits, the data returned are the logic level of the pins, whether they are programmed as inputs or outputs. When the GPIO pin is configured as an input, a write to the corresponding GPIOD bit has no effect. When configured as an output, a write to the GPIOD bit sets the output value.

If configured as inputs, these pins must be driven (do not float). The GPIO pins are set as inputs after power-on or after a reset. Figure 34 shows the GPIO port structure. The pins should be shorted to DGND if not used.

GPIO1 can be used as the PACEIN signal; GPIO2 is multiplexed with RESP_BLK signal; GPIO3 is multiplexed with the RESP signal; and GPIO4 is multiplexed with the RESP_PH signal.

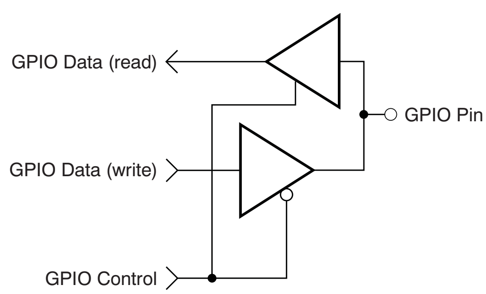


Figure 34. GPIO Port Pin

Power-Down (PWDN)

When PWDN is pulled low, all on-chip circuitry is powered down. To exit power-down mode, take the PWDN pin high. Upon exiting from power-down mode, the internal oscillator and the reference require time to wake up. It is recommended that during power-down the external clock is shut down to save power.

Reset (RESET)

There are two methods to reset the ADS1294/6/8: pull the RESET pin low, or send the RESET opcode command. When using the RESET pin, take it low to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the RESET pin back high. The RESET command takes effect on the eighth SCLK falling edge of the opcode command. On reset it takes 18 t_{CLK} cycles to complete initialization of the configuration registers to the default states and start the conversion cycle. Note that an internal RESET is automatically issued to the digital filter whenever registers CONFIG1 and RESP are set to a new value with a WREG command.

START

The START pin or the START command can be used to control conversions. START must be high or the START command must be sent to be able to read conversion data from the device. When START is low and the START command is not sent, the device does not issue a DRDY signal.

When using the START opcode to control conversion, hold the START pin low. The ADS1294/6/8 features two modes to control conversion: continuous mode and single-shot mode. The mode is selected by SINGLE_SHOT (bit 3 of the CONFIG4 register). In multiple device configurations the START pin is used to synchronize devices (see the *Multiple Device Configuration* subsection of the *SPI Interface* section for more details).

Settling Time

The settling time (t_{SETTLE}) is the time it takes for the converter to output fully settled data when START signal is pulled high. Once START is pulled high, DRDY is also pulled high. The next falling edge of DRDY indicates that data are ready. Figure 35 shows the timing diagram and Table 9 shows the settling time for different data rates. The settling time depends on f_{CLK} and the decimation ratio (controlled by the DR[2:0] bits in the CONFIG1 register). Table 8 shows the settling time as a function of t_{CLK}. Note that when START is held high and there is a step change in the input signal, it takes 3 × t_{DR} for the filter to settle to the new value. This time must be considered when trying to measure narrow pace pulses for pacer detection.

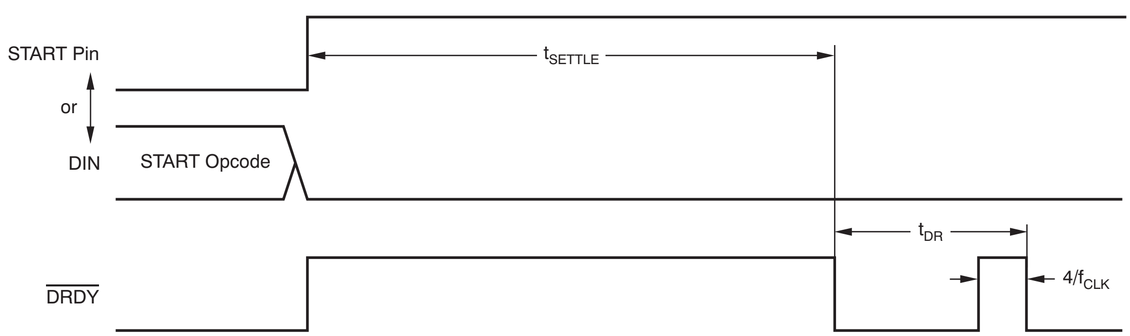


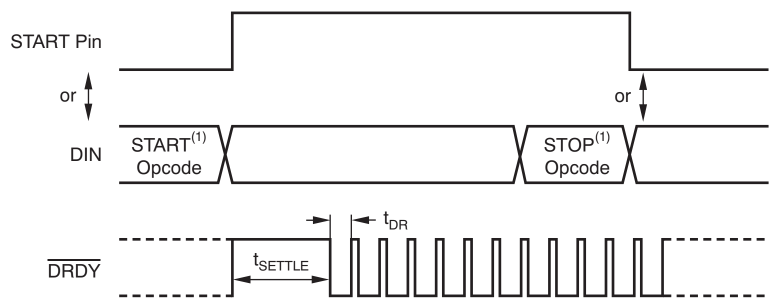
Figure 35. Settling Time

Table 9. Settling Time for Different Data Rates

DR[2:0]	HIGH-RESOLUTION MODE	LOW-POWER MODE	UNIT
000	296	584	t_{CLK}
001	584	1160	t_{CLK}
010	1160	2312	t_{CLK}
011	2312	4616	t_{CLK}
100	4616	9224	t_{CLK}
101	9224	18440	t_{CLK}
110	18440	36872	t_{CLK}

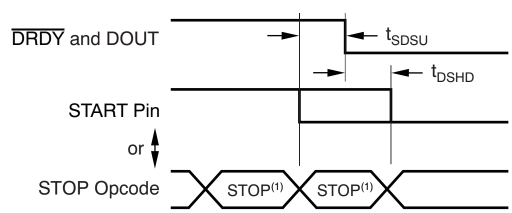
Continuous Mode

Conversions begin when the START pin is taken high or when the START opcode command is sent. As seen in Figure 36, the DRDY output goes high when conversions are started and goes low when data are ready. Conversions continue indefinitely until the START pin is taken low or the STOP opcode command is transmitted. When the START pin is pulled low or the stop command is issued, the conversion in progress is allowed to complete. Figure 37 and Table 10 show the required timing of DRDY to the START pin and the START/STOP opcode commands when controlling conversions in this mode. To keep the converter running continuously, the START pin can be permanently tied high. Note that when switching from pulse mode to continuous mode, the START signal is pulsed or a STOP command must be issued followed by a START command.



(1) START and STOP opcode commands take effect on the seventh SCLK falling edge.

Figure 36. Continuous Conversion Mode



(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Figure 37. START to DRDY Timing

Table 10. Timing Characteristics for Figure 37 (1)

SYMBOL	DESCRIPTION	MIN	UNIT
t_{SDSU}	START pin low or STOP opcode to DRDY setup time to halt further conversions	16	$1/f_{CLK}$
t_{DSHD}	START pin low or STOP opcode to complete current conversion	16	$1/f_{CLK}$

(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Single-Shot Mode

The single-shot mode is set by setting SINGLE_SHOT bit in CONFIG4 register to '1'. In single-shot mode, the ADS1294/6/8 perform a single conversion when the START pin is taken high or when the START opcode command is sent. As seen in Figure 37, when a conversion is complete, $\overline{DRDY}$ goes low and further conversions are stopped. Regardless of whether the conversion data are read or not, $\overline{DRDY}$ remains low. To begin a new conversion, take the START pin low and then back high, or transmit the START opcode again. Note that when switching from continuous mode to pulse mode, make sure the START signal is pulsed or issue a STOP command followed by a START command.

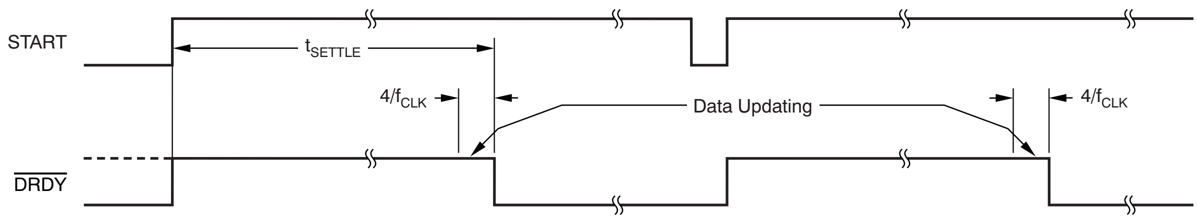


Figure 38. $\overline{DRDY}$ with No Data Retrieval in Single-Shot Mode

MULTIPLE DEVICE CONFIGURATION

The ADS1294/6/8 are designed to provide configuration flexibility when multiple devices are used in a system. The SPI interface typically needs four signals DIN, DOUT, SCLK, and $\overline{CS}$. With one additional chip select signal per device, multiple devices can be connected together. The number of signals needed to interface *n* devices is 3 + *n*.

The right-leg drive amplifiers can be daisy-chained as explained in the *RLD Configuration with Multiple Devices* subsection of the *ECG-Specific Functions* section. To use the internal oscillator in a daisy-chain configuration, one of the devices must be set as the master for the clock source with the internal oscillator enabled (CLKSEL pin = 1) and the internal oscillator clock brought out of the device by setting the CLK_EN register bit to '1'. This master device clock is used as the external clock source for the other devices.

When using multiple devices, the devices can be synchronized with the START signal. The delay from START to the $\overline{DRDY}$ signal is fixed for a fixed data rate (see the *START* subsection of the *SPI Interface* section for more details on the settling times). Figure 39 shows the behavior of two devices when synchronized with the START signal.

There are two ways to connect multiple devices with a optimal number of interface pins: cascade mode and daisy-chain mode.

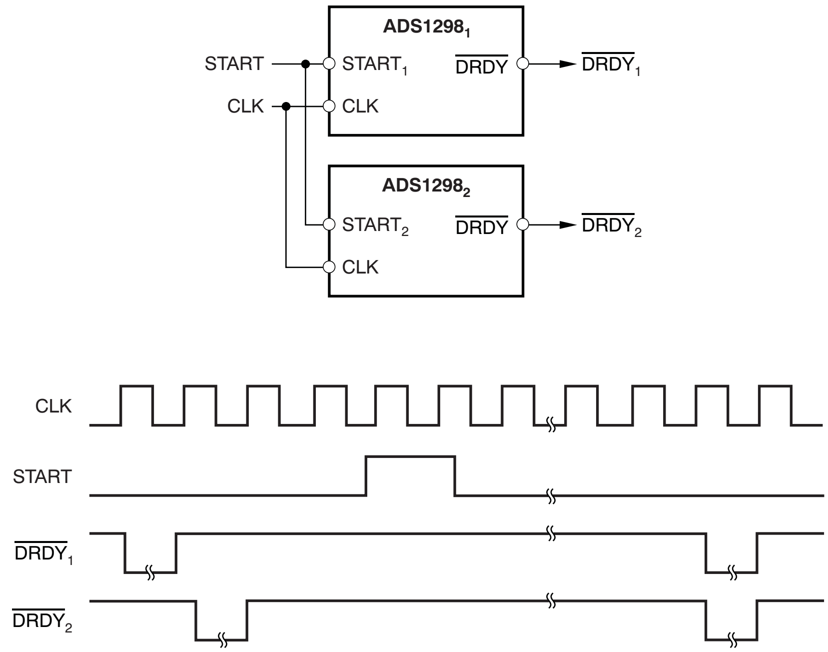


Figure 39. Synchronizing Multiple Converters

Standard Mode

Figure 40a shows a configuration with two devices cascaded together. One of the devices is an ADS1298 (eight-channel) and the other is an ADS1294 (four-channel). Together, they create a system with 12 channels. DOUT, SCLK, and DIN are shared. Each device has its own chip select. When a device is not selected by the corresponding CS being driven to logic 1, the DOUT of this device is high-impedance. This structure allows the other device to take control of the DOUT bus.

Daisy-Chain Mode

Daisy-chain mode is enabled by setting the DAISY_EN bit in the CONFIG1 register. Figure 40b shows the daisy-chain configuration. In this mode SCLK and CS are shared across multiple devices. Each device has its own DIN signal. This configuration allows each device to be programmed independently. The DOUT of one device is hooked up to the DAISY_IN of the other device, thereby creating a chain. One extra SCLK must be issued in between each data set. Also, when using daisy chain mode the multiple readback feature is not available.

In a case where all devices in the chain are operated in the same register setting, DIN can be shared as well and thereby reduces the SPI communication signals to four, regardless of the number of devices. However, because the individual devices cannot be programmed, the RLD driver cannot be shared among the multiple devices. Furthermore, an external clock must be used.

Note that the SCLK rising edge shifts data out on DOUT. The SCLK rising edge also latches data to the DAISY_IN pin. It is necessary to ensure that daisy-chain mode setup and hold times are met. This can be achieved with PCB layout techniques or by placing an external buffer between the DOUT and DAISY_IN pins.

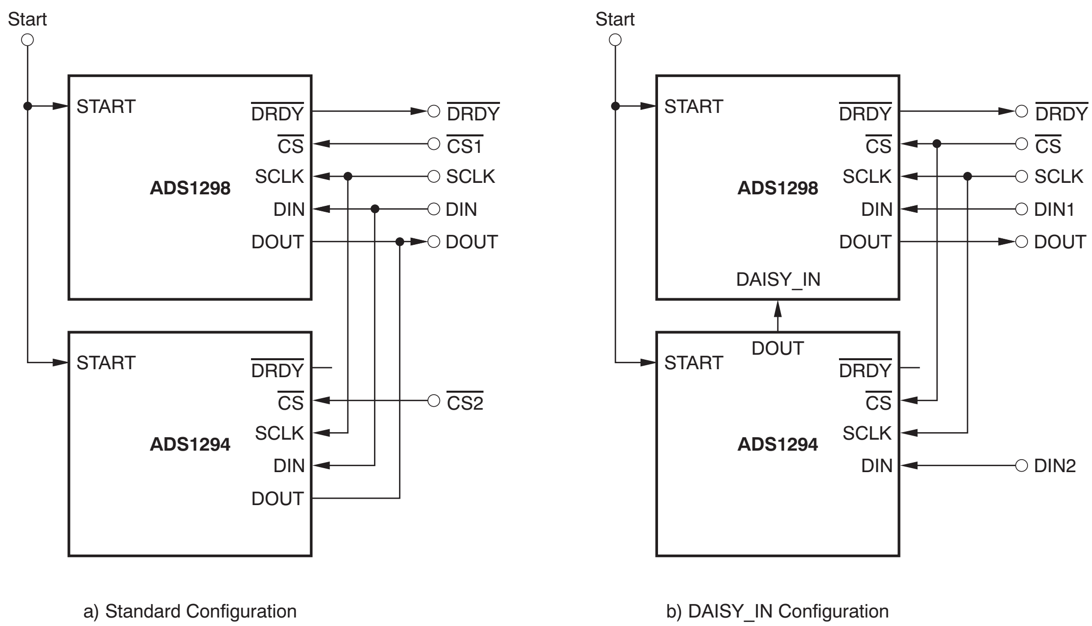


Figure 40. Multiple Device Configurations

The maximum number of devices that can be daisy-chained depends on the data rate at which the device is being operated. The maximum number of devices can be approximately calculated with Equation 7.

$$N_{DEVICES} = \frac{f_{SCLK}}{f_{DR}\,(N_{BITS})(N_{CHANNELS}) + 24}$$

where:

N_{BITS} = device resolution (depends on data rate), and

$N_{CHANNELS}$ = number of channels in the device (4, 6, or 8). (7)

For example, when the ADS1298 (eight-channel, 24-bit version) is operated at a 2kSPS data rate with a 4MHz f_{SCLK}, 10 devices can be daisy-chained.

SPI COMMAND DEFINITIONS

The ADS1294/6/8 provide flexible configuration control. The opcode commands, summarized in Table 11, control and configure the operation of the ADS1294/6/8. The opcode commands are stand-alone, except for the register read and register write operations that require a second command byte plus data. CS can be taken high or held low between opcode commands but must stay low for the entire command operation (especially for multi-byte commands). System opcode commands and the RDATA command are decoded by the ADS1294/6/8 on the seventh falling edge of SCLK. The register read/write opcodes are decoded on the eighth SCLK falling edge. Be sure to follow SPI timing requirements when pulling CS high after issuing a command.

Table 11. Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
System Commands			
WAKEUP	Wake-up from standby mode	0000 0010 (02h)	
STANDBY	Enter standby mode	0000 0100 (04h)	
RESET	Reset the device	0000 0110 (06h)	
START	Start/restart (synchronize) conversions	0000 1000 (08h)	
STOP	Stop conversion	0000 1010 (0Ah)	
Data Read Commands			
RDATAC	Enable Read Data Continuous mode. This mode is the default mode at power-up.(1)	0001 0000 (10h)	
SDATAC	Stop Read Data Continuously mode	0001 0001 (11h)	
RDATA	Read data by command; supports multiple read back.	0001 0010 (12h)	
Register Read Commands			
RREG	Read *n nnnn* registers starting at address *r rrrr*	001*r rrrr* (2xh)(2)	000*n nnnn*(2)
WREG	Write *n nnnn* registers starting at address *r rrrr*	010*r rrrr* (4xh)(2)	000*n nnnn*(2)

(1) When in RDATAC mode, the RREG command is ignored.
(2) *n nnnn* = number of registers to be read/written – 1. For example, to read/write three registers, set *n nnnn* = 0 (0010). *r rrrr* = starting register address for read/write opcodes.

WAKEUP: Exit STANDBY Mode

This opcode exits the low-power standby mode; see the *STANDBY: Enter STANDBY Mode* subsection of the *SPI Command Definitions* section. Time is required when exiting standby mode (see the Electrical Characteristics for details). **There are no restrictions on the SCLK rate for this command and it can be issued any time.** Any following command must be sent after 4 t_{CLK} cycles.

STANDBY: Enter STANDBY Mode

This opcode command enters the low-power standby mode. All parts of the circuit are shut down except for the reference section. The standby mode power consumption is specified in the Electrical Characteristics. **There are no restrictions on the SCLK rate for this command and it can be issued any time.** Do not send any other command other than the wakeup command after the device enters the standby mode.

RESET: Reset Registers to Default Values

This command resets the digital filter cycle and returns all register settings to the default values. See the *Reset (RESET)* subsection of the *SPI Interface* section for more details. **There are no restrictions on the SCLK rate for this command and it can be issued any time.** It takes 18 t_{CLK} cycles to execute the RESET command. Avoid sending any commands during this time.

START: Start Conversions

This opcode starts data conversions. Tie the START pin low to control conversions by command. If conversions are in progress this command has no effect. The STOP opcode command is used to stop conversions. If the START command is immediately followed by a STOP command then have a gap of 4 t_{CLK} cycles between them. When the START opcode is sent to the device, keep the START pin low until the STOP command is issued. (See the *START* subsection of the *SPI Interface* section for more details.) **There are no restrictions on the SCLK rate for this command and it can be issued any time.**

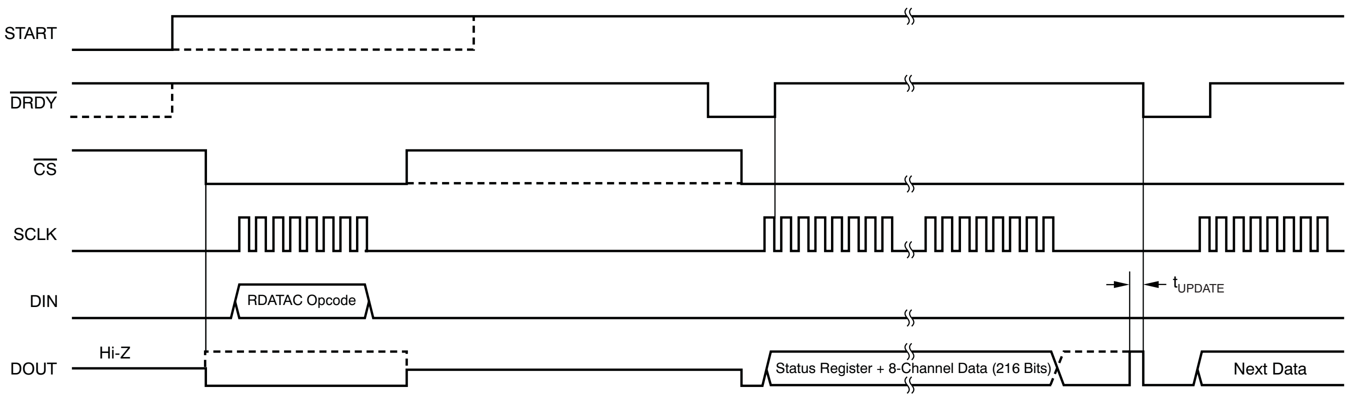
STOP: Stop Conversions

This opcode stops conversions. Tie the START pin low to control conversions by command. When the STOP command is sent, the conversion in progress completes and further conversions are stopped. If conversions are already stopped, this command has no effect. There are no restrictions on the SCLK rate for this command and it can be issued any time.

RDATAC: Read Data Continuous

This opcode enables the output of conversion data on each $\overline{DRDY}$ without the need to issue subsequent read data opcodes. This mode places the conversion data in the output register and may be shifted out directly. The read data continuous mode is the default mode of the device and the device defaults in this mode on power-up.

RDATAC mode is cancelled by the Stop Read Data Continuous command. If the device is in RDATAC mode, a SDATAC command must be issued before any other commands can be sent to the device. There is no restriction on the SCLK rate for this command. However, the following data retrieval SCLKs or the SDATAC opcode command should wait at least 4 t_{CLK} cycles. The timing for RDATAC is shown in Figure 41. As Figure 41 shows, there is a *keep out* zone of 4 t_{CLK} cycles around the $\overline{DRDY}$ pulse where this command cannot be issued in. If no data are retrieved from the device, DOUT and $\overline{DRDY}$ behave similarly in this mode. To retrieve data from the device after RDATAC command is issued, make sure either the START pin is high or the START command is issued. Figure 41 shows the recommended way to use the RDATAC command.



(1) $t_{UPDATE} = 4/f_{CLK}$. Do not read data during this time.

Figure 41. RDATAC Usage

SDATAC: Stop Read Data Continuous

This opcode cancels the Read Data Continuous mode. There is no restriction on the SCLK rate for this command, but the following command must wait for 4 t_{CLK} cycles.

RDATA: Read Data

Issue this command after $\overline{DRDY}$ goes low to read the conversion result (in Stop Read Data Continuous mode). There is no restriction on the SCLK rate for this command, and there is no wait time needed for the subsequent commands or data retrieval SCLKs. To retrieve data from the device after RDATA command is issued, make sure either the START pin is high or the START command is issued. When reading data with the RDATA command, the read operation can overlap the occurrence of the next $\overline{DRDY}$ without data corruption. Figure 42 shows the recommended way to use the RDATA command.

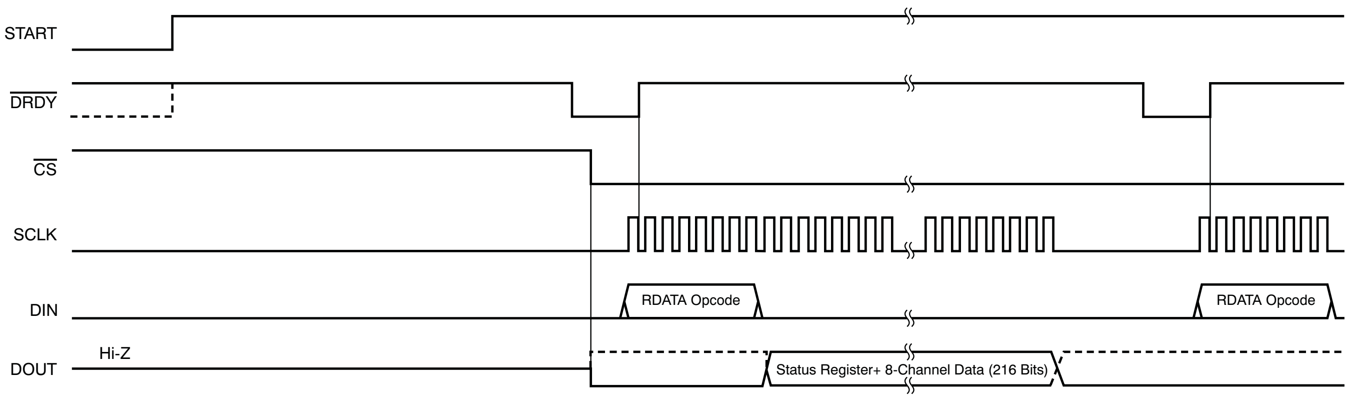


Figure 42. RDATA Usage

Sending Multi-Byte Commands

The ADS1294/6/8 serial interface decodes commands in bytes and requires 4 t_{CLK} cycles to decode and execute. Therefore, when sending multi-byte commands, a 4 t_{CLK} period must separate the end of one byte (or opcode) and the next.

Assume CLK is 2.048MHz, then $t_{SDECODE}$ (4 t_{CLK}) is 1.96µs. When SCLK is 16MHz, one byte can be transferred in 500ns. This byte transfer time does not meet the $t_{SDECODE}$ specification; therefore, a delay must be inserted so the end of the second byte arrives 1.46µs later. If SCLK is 4MHz, one byte is transferred in 2µs. Because this transfer time exceeds the $t_{SDECODE}$ specification, the processor can send subsequent bytes without delay. In this later scenario, the serial port can be programmed to cease single-byte transfer per cycle to multiple bytes.

RREG: Read From Register

This opcode reads register data. The Register Read command is a two-byte opcode followed by the output of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to read – 1.

First opcode byte: 001*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte: 000*n nnnn*, where *n nnnn* is the number of registers to read – 1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in Figure 43. When the device is in read data continuous mode it is necessary to issue a SDATAC command before RREG command can be issued. RREG command can be issued any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the *Serial Clock (SCLK)* subsection of the *SPI Interface* section for more details. Note that CS must be low for the entire command.

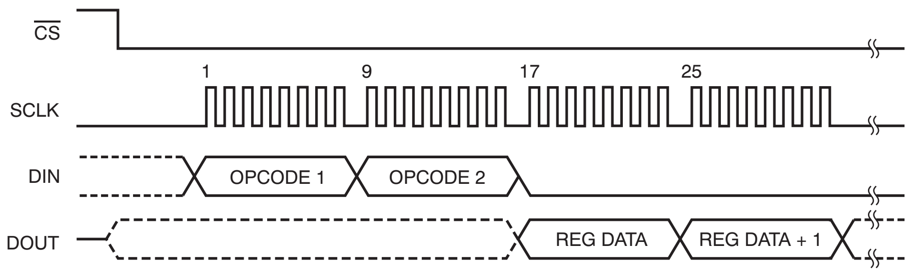


Figure 43. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

WREG: Write to Register

This opcode writes register data. The Register Write command is a two-byte opcode followed by the input of the register data. The first byte contains the command opcode and the register address.

The second byte of the opcode specifies the number of registers to write – 1.

First opcode byte: 010*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte: 000*n nnnn*, where *n nnnn* is the number of registers to write – 1.

After the opcode bytes, the register data follows (in MSB-first format), as shown in Figure 44. WREG command can be issued any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the *Serial Clock (SCLK)* subsection of the *SPI Interface* section for more details. Note that CS must be low for the entire command.

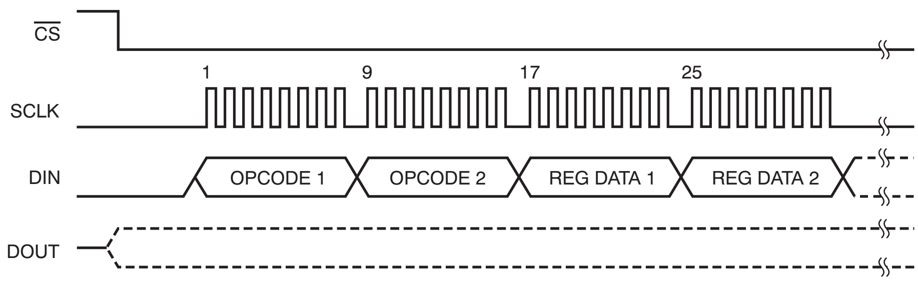


Figure 44. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (OPCODE 1 = 0100 0000, OPCODE 2 = 0000 0001)

REGISTER MAP

Table 12 describes the various ADS1294/6/8 registers.

Table 12. Register Assignments

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device Settings (Read-Only Registers)										
00h	ID	xx	REV_ID3	REV_ID2	REV_ID1	N/A	DEV_ID2	DEV_ID1	NU_CH2	NU_CH1
Global Settings Across Channels										
01h	CONFIG1	06	HR	DAISY_EN	CLK_EN	0	0	DR2	DR1	DR0
02h	CONFIG2	40	0	1	0	INT_TEST	0	TEST_AMP	TEST_FREQ1	TEST_FREQ0
03h	CONFIG3	40	PD_REFBUF	1	VREF_4V	RLD_MEAS	RLDREF_INT	PD_RLD	RLD_LOFF_SENS	RLD_STAT
04h	LOFF	00	COMP_TH2	COMP_TH1	COMP_TH0	VLEAD_OFF_EN	ILEAD_OFF1	ILEAD_OFF0	FLEAD_OFF1	FLEAD_OFF0
Channel-Specific Settings										
05h	CH1SET	00	PD1	GAIN12	GAIN11	GAIN10	0	MUXn2	MUXn1	MUXn0
06h	CH2SET	00	PD2	GAIN22	GAIN21	GAIN20	0	MUX22	MUX21	MUX20
07h	CH3SET	00	PD3	GAIN32	GAIN31	GAIN30	0	MUX32	MUX31	MUX30
08h	CH4SET	00	PD4	GAIN42	GAIN41	GAIN40	0	MUX42	MUX41	MUX40
09h	CH5SET(1)	00	PD5	GAIN52	GAIN51	GAIN50	0	MUX52	MUX51	MUX50
0Ah	CH6SET(1)	00	PD6	GAIN62	GAIN61	GAIN60	0	MUX62	MUX61	MUX60
0Bh	CH7SET(1)	00	PD7	GAIN72	GAIN71	GAIN70	0	MUX72	MUX71	MUX70
0Ch	CH8SET(1)	00	PD8	GAIN82	GAIN81	GAIN80	0	MUX82	MUX81	MUX80
0Dh	RLD_SENSP (2)	00	RLD8P(1)	RLD7P(1)	RLD6P(1)	RLD5P(1)	RLD4P	RLD3P	RLD2P	RLD1P
0Eh	RLD_SENSN (2)	00	RLD8N(1)	RLD7N(1)	RLD6N(1)	RLD5N(1)	RLD4N	RLD3N	RLD2N	RLD1N
0Fh	LOFF_SENSP (2)	00	LOFF8P	LOFF7P	LOFF6P	LOFF5P	LOFF4P	LOFF3P	LOFF2P	LOFF1P
10h	LOFF_SENSN (2)	00	LOFF8N	LOFF7N	LOFF6N	LOFF5N	LOFF4N	LOFF3N	LOFF2N	LOFF1N
11h	LOFF_FLIP	00	LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1
Lead-Off Status Registers (Read-Only Registers)										
12h	LOFF_STATP	00	IN8P_OFF	IN7P_OFF	IN6P_OFF	IN5P_OFF	IN4P_OFF	IN3P_OFF	IN2P_OFF	IN1P_OFF
13h	LOFF_STATN	00	IN8N_OFF	IN7N_OFF	IN6N_OFF	IN5N_OFF	IN4N_OFF	IN3N_OFF	IN2N_OFF	IN1N_OFF
GPIO and OTHER Registers										
14h	GPIO	0F	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1
15h	PACE	00	0	0	0	PACEE1	PACEE0	PACEO1	PACEO0	PD_PACE
16h	RESP	00	0	0	0	RESP_PH2	RESP_PH1	RESP_PH0	RESP_CTRL1	RESP_CTRL0
17h	CONFIG4	00	RESP_FREQ2	RESP_FREQ1	RESP_FREQ0	0	SINGLE_SHOT	WCT_TO_RLD	PD_LOFF_COMP	0
18h	WCT1	00	aVF_CH6	aVL_CH5	aVR_CH7	avR_CH4	PD_WCTA	WCTA2	WCTA1	WCTA0
19h	WCT2	00	PD_WCTC	PD_WCTB	WCTB2	WCTB1	WCTB0	WCTC2	WCTC1	WCTC0

(1) CH5SET and CH6SET are not available for the ADS1294. CH7SET and CH8SET registers are not available for the ADS1294 and ADS1296.
(2) The RLD_SENSP, PACE_SENSP, LOFF_SENSP, LOFF_SENSN, and LOFF_FLIP registers bits[5:4] are not available for the ADS1294. Bits[7:6] are not available for the ADS1294/6.

User Register Description

ID: ID Control Register (Factory-Programmed, Read-Only)

Address = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REV_ID3	REV_ID2	REV_ID1	N/A	DEV_ID2	DEV_ID1	NU_CH2	NU_CH1

The ID Control Register is programmed during device manufacture to indicate device characteristics.

Bits[7:3] **N/A**

Bits[2:0] **Factory-programmed device identification bits (read-only)**

These bits indicate the device version.
000 = ADS1294; 24-bit resolution, 4 channels
001 = ADS1296; 24-bit resolution, 6 channels
010 = ADS1298; 24-bit resolution, 8 channels
011 = Reserved for future use
100 = Reserved for future use
101 = Reserved for future use
110 = Reserved for future use
111 = Reserved for future use

CONFIG1: Configuration Register 1

Address = 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HR	$\overline{\text{DAISY\_EN}}$	CLK_EN	0	0	DR2	DR1	DR0

Bit 7 **HR: High-Resolution/Low-Power mode**

This bit determines whether the device runs in Low-Power or High-Resolution mode.
0 = Low-Power mode (default)
1 = High-Resolution mode

Bit 6 **$\overline{\text{DAISY\_EN}}$: Daisy-chain/multiple readback mode**

This bit determines which mode is enabled.
0 = Daisy-chain mode (default)
1 = Multiple readback mode

Bit 5 **CLK_EN: CLK connection(1)**

This bit determines if the internal oscillator signal is connected to the CLK pin when the CLKSEL pin = 1.
0 = Oscillator clock output disabled (default)
1 = Oscillator clock output enabled

Bits[4:3] **Must always be set to '0'**

Bits[2:0] **DR[2:0]: Output data rate.**

For high resolution mode, $f_{MOD} = f_{CLK}/4$. For low power mode, $f_{MOD} = f_{CLK}/8$.
These bits determine the output data rate of the device.

(1) Additional power will be consumed when driving external devices.

BIT	DATA RATE	HIGH-RESOLUTION MODE(1)	LOW-POWER MODE(2)
000	$f_{MOD}/16$	32kSPS	16kSPS
001	$f_{MOD}/32$	16kSPS	8kSPS
010	$f_{MOD}/64$	8kSPS	4kSPS
011	$f_{MOD}/128$	4kSPS	2kSPS
100	$f_{MOD}/256$	2kSPS	1kSPS
101	$f_{MOD}/512$	1kSPS	500SPS
110 (default)	$f_{MOD}/1024$	500SPS	250SPS
111	DO NOT USE	N/A	N/A

(1) Additional power will be consumed when driving external devices.
(2) f_{CLK} = 2.048MHz.

CONFIG2: Configuration Register 2

Address = 02h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	INT_TEST	0	TEST_AMP	TEST_FREQ1	TEST_FREQ0

Configuration Register 2 configures the test signal generation. See the *Input Multiplexer* section for more details.

Bits[7:6] **Must always be set to '0'**

Bit 5 **Must always be set to '1'**

Default at power-up is '0'.

Bit 4 **INT_TEST: TEST source**

This bit determines the source for the Test signal.
0 = Test signals are driven externally (default)
1 = Test signals are generated internally

Bit 3 **Must always be set to '0'**

Bit 2 **TEST_AMP: Test signal amplitude**

These bits determine the Calibration signal amplitude.
0 = 1 × (VREFP – VREFN)/2.4mV (default)
1 = 2 × (VREFP – VREFN)/2.4mV

Bits[1:0] **TEST_FREQ[1:0]: Test signal frequency**

These bits determine the calibration signal frequency.
00 = Pulsed at $f_{CLK}/2^{21}$ (default)
01 = Pulsed at $f_{CLK}/2^{20}$
10 = Not used
11 = At dc

CONFIG3: Configuration Register 3

Address = 03h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{\text{PD\_REFBUF}}$	1	VREF_4V	RLD_MEAS	RLDREF_INT	$\overline{\text{PD\_RLD}}$	RLD_LOFF_SENS	RLD_STAT

Configuration Register 3 configures multi-reference and RLD operation.

Bit 7 **$\overline{\text{PD\_REFBUF}}$: Power-down reference buffer**

This bit determines the power-down reference buffer state.
0 = Power-down internal reference buffer (default)
1 = Enable internal reference buffer

Bit 6 **Must always be set to '1'. Default is '1' at power-up.**

Bit 5 **VREF_4V: Reference voltage**

This bit determines the reference voltage, VREFP.
0 = VREFP is set to 2.4V (default)
1 = VREFP is set to 4V (use only with a 5V analog supply)

Bit 4 **RLD_MEAS: RLD measurement**

This bit enables RLD measurement. The RLD signal may be measured with any channel.
0 = Open (default)
1 = RLD_IN signal is routed to the channel that has the MUX_Setting *010* (V_{REF})

Bit 3 **RLDREF_INT: RLDREF signal**

This bit determines the RLDREF signal source.
0 = RLDREF signal fed externally (default)
1 = RLDREF signal (AVDD – AVSS)/2 generated internally

Bit 2 **$\overline{\text{PD\_RLD}}$: RLD buffer power**

This bit determines the RLD buffer power state.
0 = RLD buffer is powered down (default)
1 = RLD buffer is enabled

Bit 1 **RLD_LOFF_SENS: RLD sense function**

This bit enables the RLD sense function.
0 = RLD sense is disabled (default)
1 = RLD sense is enabled

Bit 0 **RLD_STAT: RLD lead off status**

This bit determines the RLD status.
0 = RLD is connected (default)
1 = RLD is not connected

LOFF: Lead-Off Control Register

Address = 04h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMP_TH2	COMP_TH1	COMP_TH0	VLEAD_OFF_EN	ILEAD_OFF1	ILEAD_OFF0	FLEAD_OFF1	FLEAD_OFF0

The Lead-Off Control Register configures the Lead-Off detection operation.

Bits[7:5] **COMP_TH[2:0]: Lead-off comparator threshold**

These bits determine the lead-off comparator threshold level setting. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for a detailed description.

Comparator positive side

000 = 95% (default)
001 = 92.5%
010 = 90%
011 = 87.5%
100 = 85%
101 = 80%
110 = 75%
111 = 70%

Comparator negative side

000 = 5% (default)
001 = 7.5%
010 = 10%
011 = 12.5%
100 = 15%
101 = 20%
110 = 25%
111 = 30%

Bit 4 **VLEAD_OFF_EN: Lead-off detection mode**

This bit determines the lead-off detection mode.
0 = Current source mode lead-off (default)
1 = Pull-up/pull-down resistor mode lead-off

Bits[3:2] **ILEAD_OFF[1:0]: Lead-off current magnitude**

These bits determine the magnitude of current for the current lead-off mode.
00 = 6nA (default)
01 = 12nA
10 = 18nA
11 = 24nA

Bits[1:0] **FLEAD_OFF[1:0]: Lead-off frequency**

These bits determine the frequency of lead-off detect for each channel.
00 = When any bits of the LOFF_SENSP or LOFF_SENSN registers are turned on, make sure that FLEAD[1:0] are either set to 01 or 11 (default)
01 = AC lead-off detection at $f_{DR}/4$
10 = Not used
11 = DC lead-off detection turned on

CHnSET: Individual Channel Settings (n = 1 : 8)

Address = 05h to 0Ch

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PD	GAIN2	GAIN1	GAIN0	0	MUXn2	MUXn1	MUXn0

The CH[1:8]SET Control Register configures the power mode, PGA gain, and multiplexer settings channels. See the *Input Multiplexer* section for details. CH[2:8]SET are similar to CH1SET, corresponding to the respective channels.

Bit 7 **PD: Power-down**

This bit determines the channel power mode for the corresponding channel.
0 = Normal operation (default)
1 = Channel power-down

Bits[6:4] **GAIN[2:0]: PGA gain**

These bits determine the PGA gain setting.

000 = 6 (default)
001 = 1
010 = 2
011 = 3
100 = 4
101 = 8
110 = 12

Bit 3 **Always write '0'**

Bits[2:0] **MUXn[2:0]: Channel input**

These bits determine the channel input selection.

000 = Normal electrode input (default)
001 = Input shorted (for offset or noise measurements)
010 = Used in conjunction with RLD_MEAS bit for RLD measurements. See the *Right Leg Drive (RLD DC Bias Circuit)* subsection of the *ECG-Specific Functions* section for more details.
011 = MVDD for supply measurement
100 = Temperature sensor
101 = Test signal
110 = RLD_DRP (positive electrode is the driver)
111 = RLD_DRN (negative electrode is the driver)

RLD_SENSP

Address = 0Dh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RLD8P	RLD7P	RLD6P	RLD5P	RLD4P	RLD3P	RLD2P	RLD1P

This register controls the selection of the positive signals from each channel for right leg drive derivation. See the *Right Leg Drive (RLD DC Bias Circuit)* subsection of the *ECG-Specific Functions* section for details.

Note that registers bits[5:4] are not available for the ADS1294. Bits[7:6] are not available for the ADS1294/6.

RLD_SENSN

Address = 0Eh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RLD8N	RLD7N	RLD6N	RLD5N	RLD4N	RLD3N	RLD2N	RLD1N

This register controls the selection of the negative signals from each channel for right leg drive derivation. See the *Right Leg Drive (RLD DC Bias Circuit)* subsection of the *ECG-Specific Functions* section for details.

Note that registers bits[5:4] are not available for the ADS1294. Bits[7:6] are not available for the ADS1294/6.

LOFF_SENSP

Address = 0Fh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOFF8P	LOFF7P	LOFF6P	LOFF5P	LOFF4P	LOFF3P	LOFF2P	LOFF1P

This register selects the positive side from each channel for lead-off detection. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for details. Note that the LOFF_STATP register bits are only valid if the corresponding LOFF_SENSP bits are set to '1'.

Note that registers bits[5:4] are not available for the ADS1294. Bits[7:6] are not available for the ADS1294/6.

LOFF_SENSN

Address = 10h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOFF8N	LOFF7N	LOFF6N	LOFF5N	LOFF4N	LOFF3N	LOFF2N	LOFF1N

This register selects the negative side from each channel for lead-off detection. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for details. Note that the LOFF_STATN register bits are only valid if the corresponding LOFF_SENSN bits are set to '1'.

Note that registers bits[5:4] are not available for the ADS1294. Bits[7:6] are not available for the ADS1294/6.

LOFF_FLIP

Address = 11h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1

This register controls the direction of the current used for lead-off derivation. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for details.

LOFF_STATP (Read-Only Register)

Address = 12h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IN8P_OFF	IN7P_OFF	IN6P_OFF	IN5P_OFF	IN4P_OFF	IN3P_OFF	IN2P_OFF	IN1P_OFF

This register stores the status of whether the positive electrode on each channel is on or off. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for details. Ignore the LOFF_STATP values if the corresponding LOFF_SENSP bits are not set to '1'.

'0' is lead-on (default) and '1' is lead-off.

LOFF_STATN (Read-Only Register)

Address = 13h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IN8N_OFF	IN7N_OFF	IN6N_OFF	IN5N_OFF	IN4N_OFF	IN3N_OFF	IN2N_OFF	IN1N_OFF

This register stores the status of whether the negative electrode on each channel is on or off. See the *Lead-Off Detection* subsection of the *ECG-Specific Functions* section for details. Ignore the LOFF_STATN values if the corresponding LOFF_SENSN bits are not set to '1'.

'0' is lead-on (default) and '1' is lead-off.

GPIO: General-Purpose I/O Register

Address = 14h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1

The General-Purpose I/O Register controls the action of the three GPIO pins. Note that when RESP_CTRL[1:0] is in mode 01 and 11, the GPIO2, GPIO3, and GPIO4 pins are not available for use.

Bits[7:4] **GPIOD[4:1]: GPIO data**

These bits are used to read and write data to the GPIO ports.
When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or as outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect. GPIO is not available in certain respiration modes.

Bits[3:0] **GPIOC[4:1]: GPIO control (corresponding GPIOD)**

These bits determine if the corresponding GPIOD pin is an input or output.
0 = Output
1 = Input (default)

PACE: PACE Detect Register

Address = 15h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	PACEE1	PACEE0	PACEO1	PACEO0	$\overline{\text{PD\_PACE}}$

This register provides the PACE controls that configure the channel signal used to feed the external PACE detect circuitry. See the *Pace Detect* subsection of the *ECG-Specific Functions* section for details.

Bits[7:5] **Must always be set to '0'**

Bits[4:3] **PACEE[1:0]: PACE_OUT2 even**

These bits control the selection of the even number channels available on TEST_PACE_OUT2. Note that only one channel may be selected at any time.
00 = Channel 2 (default)
01 = Channel 4
10 = Channel 6, ADS1296/8/8R only
11 = Channel 8, ADS1298 only

Bits[2:1] **PACEO[1:0]: PACE_OUT1 odd**

These bits control the selection of the odd number channels available on TEST_PACE_OUT1. Note that only one channel may be selected at any time.
00 = Channel 1 (default)
01 = Channel 3
10 = Channel 5, ADS1296/8/8R only (default)
11 = Channel 7, ADS1298/8R only

Bit 0 **$\overline{\text{PD\_PACE}}$: PACE detect buffer**

This bit is used to enable/disable the PACE detect buffer.
0 = PACE detect buffer turned off (default)
1 = PACE detect buffer turned on

RESP: Respiration Control Register

Address = 16h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	RESP_PH2	RESP_PH1	RESP_PH0	RESP_CTRL1	RESP_CTRL0

This register provides the controls for the respiration circuitry; see the *Respiration* section for details.

Bits[7:5] **Must always be set to '0'**

Bits[4:2] **RESP_PH[2:0]: Respiration phase**[(1)]

These bits control the phase of the respiration demodulation control signal. (GPIO4 is out-of-phase with GPIO3 by the phase determined by the RESP_PH bits)

000 = 22.5°
001 = 45°
010 = 67.5°
011 = 90°
100 = 112.5°
101 = 135° (default)
110 = 157.5°
111 = 180°

Bits[1:0] **RESP_CTRL[1:0]: Respiration control**

These bits set the mode of the respiration circuitry.
00 = No respiration
01= External respiration (default)
10 = N/A
11 = N/A

(1) RESP_PH[2:0] do not function at sample rates less than 32kSPS.

CONFIG4: Configuration Register 4

Address = 17h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RESP_FREQ2	RESP_FREQ1	RESP_FREQ0	0	SINGLE_SHOT	WCT_TO_RLD	$\overline{\text{PD\_LOFF\_COMP}}$	0

Bits[7:5] **RESP_FREQ[2:0]: Respiration control frequency**

These bits control the respiration control frequency when RESP_CTRL[1:0] = 10[(1)].

000 = 64kHz (GPIO4 is out-of-phase with GPIO3 by the frequency determined by the RESP_PH bits)
001 = 32kHz (GPIO4 is out-of-phase with GPIO3 by the frequency determined by the RESP_PH bits)
010 = 16kHz (GPIO4 is 180° out-of-phase with GPIO3)
011 = 8kHz (GPIO4 is 180° out-of-phase with GPIO3)
100 = 4kHz (GPIO4 is 180° out-of-phase with GPIO3)
101 = 2kHz (GPIO4 is 180° out-of-phase with GPIO3)
110 = 1kHz (GPIO4 is 180° out-of-phase with GPIO3)
111 = 500Hz (GPIO4 is 180° out-of-phase with GPIO3)

(1) These frequencies assume f_{CLK} = 2.048MHz.

Bit 4 **Must always be set to '0'**

Bit 3 **SINGLE_SHOT: Single-shot conversion**

This bit sets the conversion mode.
0 = Continuous conversion mode (default)
1 = Single-shot mode

Bit 2 **WCT_TO_RLD: Connects the WCT to the RLD**

This bit connects WCT to RLD.
0 = WCT to RLD connection off (default)
1 = WCT to RLD connection on

Bit 1 **$\overline{\text{PD\_LOFF\_COMP}}$: Lead-off comparator power-down**

This bit powers down the lead-off comparators.
0 = Lead-off comparators disabled (default)
1 = Lead-off comparators enabled

Bit 0 **Must always be set to '0'**

WCT1: Wilson Central Terminal and Augmented Lead Control Register

Address = 18h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
aVF_CH6	aVL_CH5	aVR_CH7	aVR_CH4	$\overline{\text{PD\_WCTA}}$	WCTA2	WCTA1	WCTA0

The WCT1 control register configures the device WCT circuit channel selection and the augmented leads.

Bit 7 **aVF_CH6: Enable (WCTA + WCTB)/2 to the negative input of channel 6 (ADS1296/8/8R only)**

0 = Disabled (default)
1 = Enabled

Bit 6 **aVL_CH5: Enable (WCTA + WCTC)/2 to the negative input of channel 5 (ADS1296/8/8R only)**

0 = Disabled (default)
1 = Enabled

Bit 5 **aVR_CH7: Enable (WCTB + WCTC)/2 to the negative input of channel 7 (ADS1298/8R only)**

0 = Disabled (default)
1 = Enabled

Bit 4 **aVR_CH4: Enable (WCTB + WCTC)/2 to the negative input of channel 4 (ADS1296/8/8R only)**

0 = Disabled (default)
1 = Enabled

Bit 3 **$\overline{\text{PD\_WCTA}}$: Power-down WCTA**

0 = Powered down (default)
1 = Powered on

Bits[2:0] **WCTA[2:0]: WCT amplifier *A* channel selection; typically connected to RA electrode.**

These bits select one of the eight electrode inputs of channels 1 to 4.

000 = Channel 1 positive input connected to WCTA amplifier (default)
001 = Channel 1 negative input connected to WCTA amplifier
010 = Channel 2 positive input connected to WCTA amplifier
011 = Channel 2 negative input connected to WCTA amplifier
100 = Channel 3 Positive input connected to WCTA amplifier
101 = Channel 3 negative input connected to WCTA amplifier
110 = Channel 4 positive input connected to WCTA amplifier
111 = Channel 4 negative input connected to WCTA amplifier

WCT2: Wilson Central Terminal Control Register

Address = 19h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{\text{PD\_WCTC}}$	$\overline{\text{PD\_WCTBC}}$	WCTB2	WCTB1	WCTB0	WCTC2	WCTC1	WCTC0

The WCT2 configuration register configures the device WCT circuit channel selection.

Bit 7 **$\overline{\text{PD\_WCTC}}$: Power-down WCTC**

0 = Powered down (default)
1 = Powered on

Bit 6 **$\overline{\text{PD\_WCTB}}$: Power-down WCTB**

0 = Powered down (default)
1 = Powered on

Bits[5:3] **WCTB[2:0]: WCT amplifier *B* channel selection; typically connected to LA electrode.**

These bits select one of the eight electrode inputs of channels 1 to 4.

000 = Channel 1 positive input connected to WCTB amplifier
001 = Channel 1 negative input connected to WCTB amplifier
010 = Channel 2 positive input connected to WCTB amplifier (default)
011 = Channel 2 negative input connected to WCTB amplifier
100 = Channel 3 positive input connected to WCTB amplifier
101 = Channel 3 negative input connected to WCTB amplifier
110 = Channel 4 positive input connected to WCTB amplifier
111 = Channel 4 negative input connected to WCTB amplifier

Bits[2:0] **WCTC[2:0]: WCT amplifier *C* channel selection; typically connected to LL electrode.**

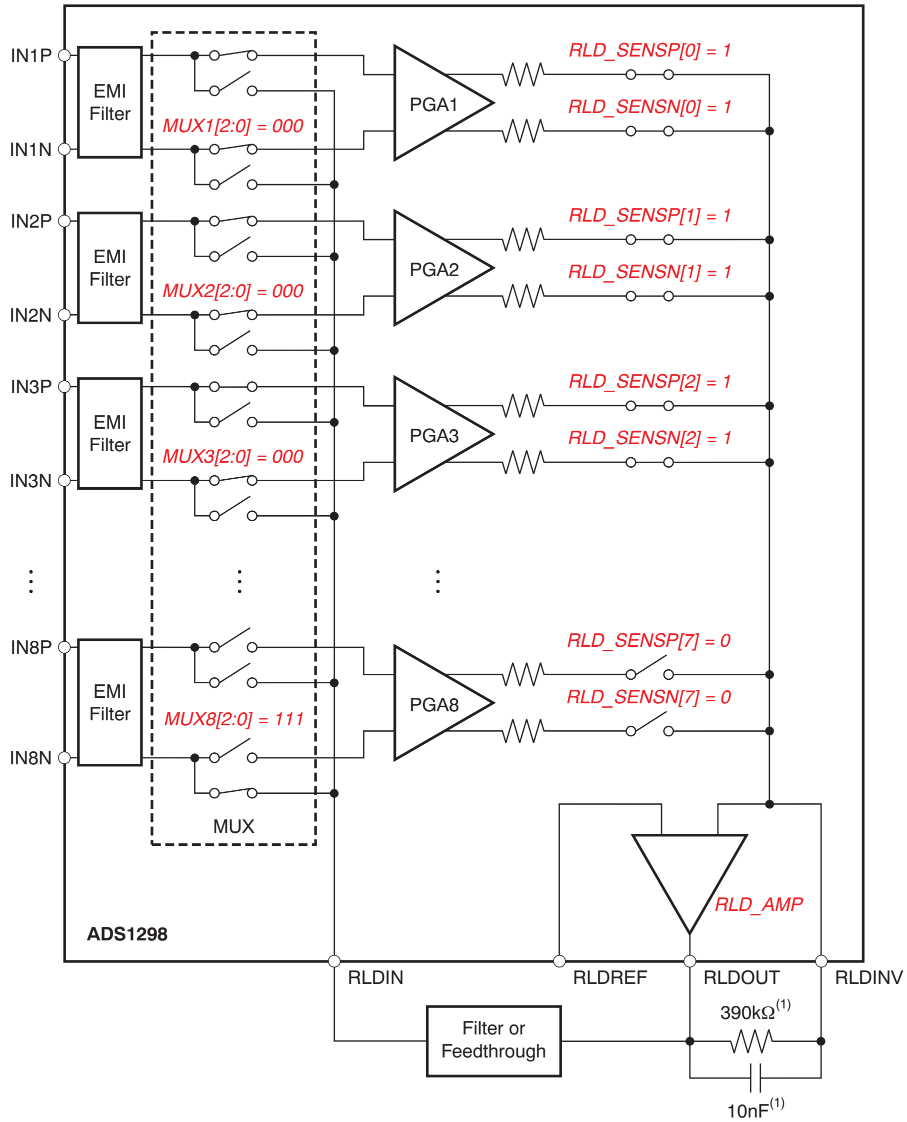
These bits select one of the eight electrode inputs of channels 1 to 4.

000 = Channel 1 positive input connected to WCTC amplifier
001 = Channel 1 negative input connected to WCTC amplifier
010 = Channel 2 positive input connected to WCTC amplifier
011 = Channel 2 negative input connected to WCTC amplifier
100 = Channel 3 positive input connected to WCTC amplifier (default)
101 = Channel 3 negative input connected to WCTC amplifier
110 = Channel 4 positive input connected to WCTC amplifier
111 = Channel 4 negative input connected to WCTC amplifier

ECG-SPECIFIC FUNCTIONS

Input Multiplexer (Rerouting the Right Leg Drive Signal)

The input multiplexer has ECG-specific functions for the right-leg drive signal. The RLD signal is available at the RLDOUT pin once the appropriate channels are selected for the RLD derivation, feedback elements are installed external to the chip, and the loop is closed. This signal can be fed after filtering or fed directly into the RLDIN pin as shown in Figure 45. This RLDIN signal can be multiplexed into any one of the input electrodes by setting the MUX bits of the appropriate channel set registers to 110 for P-side or 111 for N-side. Figure 45 shows the RLD signal generated from channels 1, 2, and 3 and routed to the N-side of channel 8. This feature can be used to dynamically change the electrode that is used as the reference signal to drive the patient body. Note that the corresponding channel cannot be used and can be powered down.

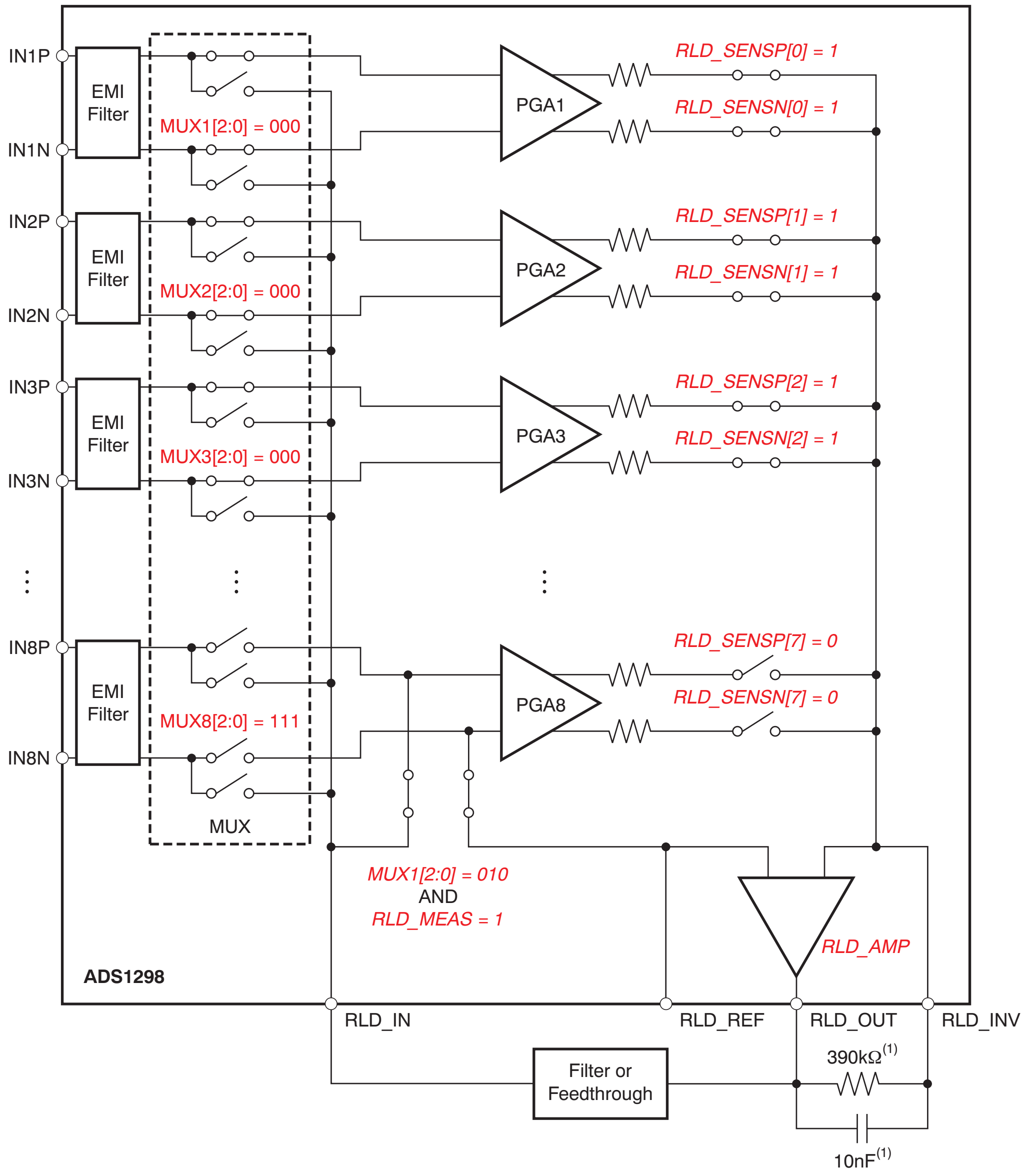


(1) Typical values for example only.

Figure 45. Example of RLDOUT Signal Configured to be Routed to IN8N

Input Multiplexer (Measuring the Right Leg Drive Signal)

Also, the RLDOUT signal can be routed to a channel (that is not used for the calculation of RLD) for measurement. Figure 46 shows the register settings to route the RLDIN signal to channel 8. The measurement is done with respect to the voltage on the RLDREF pin. If RLDREF is chosen to be internal, it would be at (AVDD + AVSS)/2. This feature is useful for debugging purposes during product development.



(1) Typical values for example only.

Figure 46. RLDOUT Signal Configured to be Read Back by Channel 8

Wilson Central Terminal (WCT) and Chest Leads

In the standard 12-lead ECG, WCT voltage is defined as the average of Right Arm (RA), Left Arm (LA), and Left Leg (LL) electrodes. This voltage is used as the reference voltage for the measurement of the chest leads. The ADS1294/6/8 has three integrated low-noise amplifiers that generate the WCT voltage. Figure 47 shows the block diagram of the implementation.

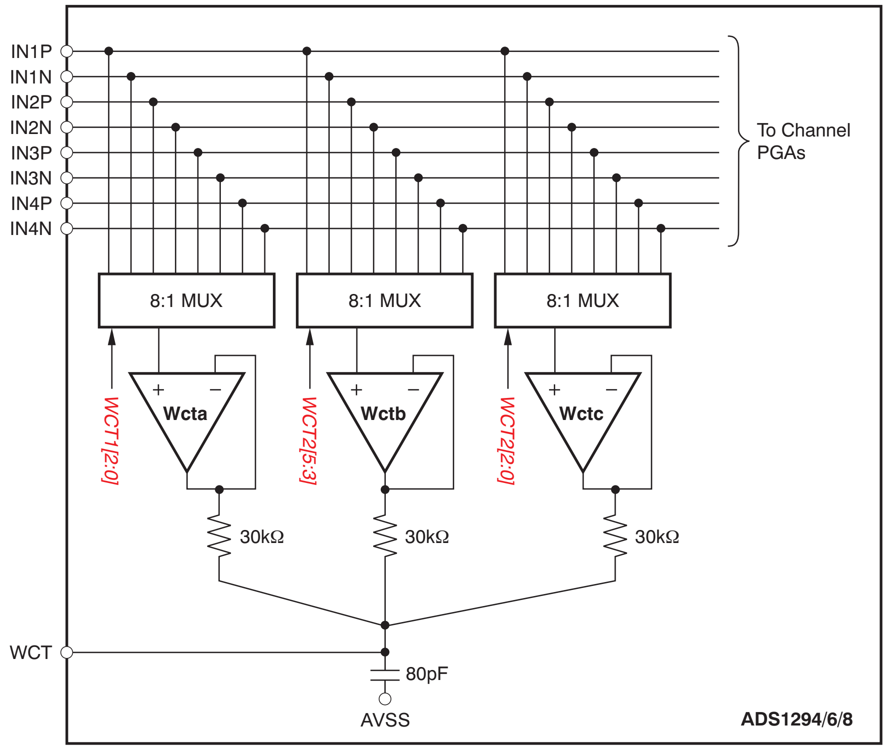


Figure 47. WCT Voltage

The devices provide flexibility to choose any one of the eight signals (IN1P to IN4N) to be routed to each of the amplifiers to generate the average. Having this flexibility allows the RA, LA, and LL electrodes to be connected to any input of the first four channels depending on the lead configuration.

Each of the three amplifiers in the WCT circuitry can be powered down individually with register settings. By powering up two amplifiers, the average of any two electrodes can be generated at the WCT pin. Powering up one amplifier provides the buffered electrode voltage at the WCT pin. Note that the WCT amplifiers have limited drive strength and thus should be buffered if used to drive a low-impedance load.

See Table 5 for performance when using any 1, 2, or 3 of the WCT buffers.

As can be seen in Table 5, the overall noise reduces when more than one WCT amplifier is powered up. This noise reduction is due to the fact that noise is averaged by the passive summing network at the output of the amplifiers. Powering down individual buffers gives negligible power savings because a significant portion of the circuitry is shared between the three amplifiers. The bandwidth of the WCT node is limited by the RC network. The internal summing network consists of three 30kΩ resistors and a 80pF capacitor. It is recommended that an external 100pF capacitor be added for optimal performance. The effective bandwidth depends on the number of amplifiers that are powered up, as shown in Table 5.

The WCT node should be only be used to drive very high input impedances (typically greater than 500MΩ). Typical application would be to connect this WCT signal to the negative inputs of a ADS1294/6/8 to be used as a reference signal for the chest leads.

As mentioned previously in this section, all three WCT amplifiers can be connected to one of eight analog input pins. The inputs of the amplifiers are chopped and the chopping frequency varies with the data rates of the ADS1294/6/8. The chop frequency for the three highest data rates scale 1:1. For example, at 32kSPS, the chop frequency is 32kHz. The chopping frequency of the four lower data rates (that is, 4kSPS, 2kSPS, 1kSPS, and 500SPS) have the chop frequency fixed to 4kHz. The chop frequency shows itself at the output of the WCT amplifiers as a small square wave riding on dc. The amplitude of the square wave is the offset of the amplifier and is typically $5mV_{PP}$. This artifact as a result of chopping is out-of-band and thus does not interfere with ECG-related measurements. As a result of the chopping function, the input current leakage on the pins with WCT amplifiers connected sees increased leakage currents at higher data rates and as the input common voltage swings closer to 0V (AVSS), as shown in Figure 48.

Note that if the output of a channel connected to the WCT amplifier (for example, the *V* lead channels) is connected to one of the pace amplifiers for external pace detection, the artifact of chopping appears at the pace amplifier output.

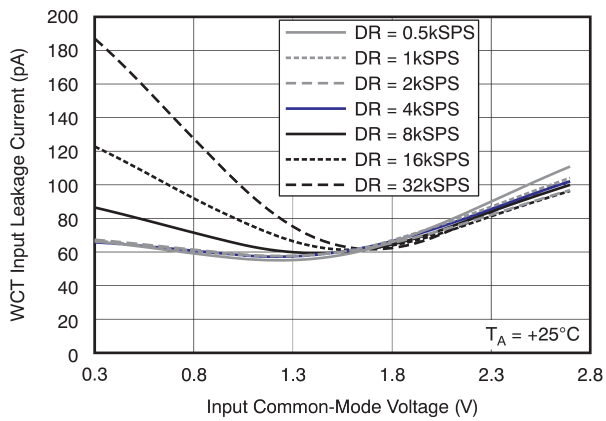


Figure 48. WCT Input Leakage Current versus Input Voltage

Augmented Leads

In the typical implementation of the 12-lead ECG with eight channels, the augmented leads are calculated digitally. In certain applications, it may be required that all leads be derived in analog rather than digital. The ADS1298 provides the option to generate the augmented leads by routing appropriate averages to channels 5 to 7. The same three amplifiers that are used to generate the WCT signal are used to generate the Goldberger Central Terminal signals as well. Figure 49 shows an example of generating the augmented leads in analog domain. Note that in this implementation it takes more than eight channels to generate the standard 12 leads. Also, this feature is not available in the ADS1296 and ADS1294.

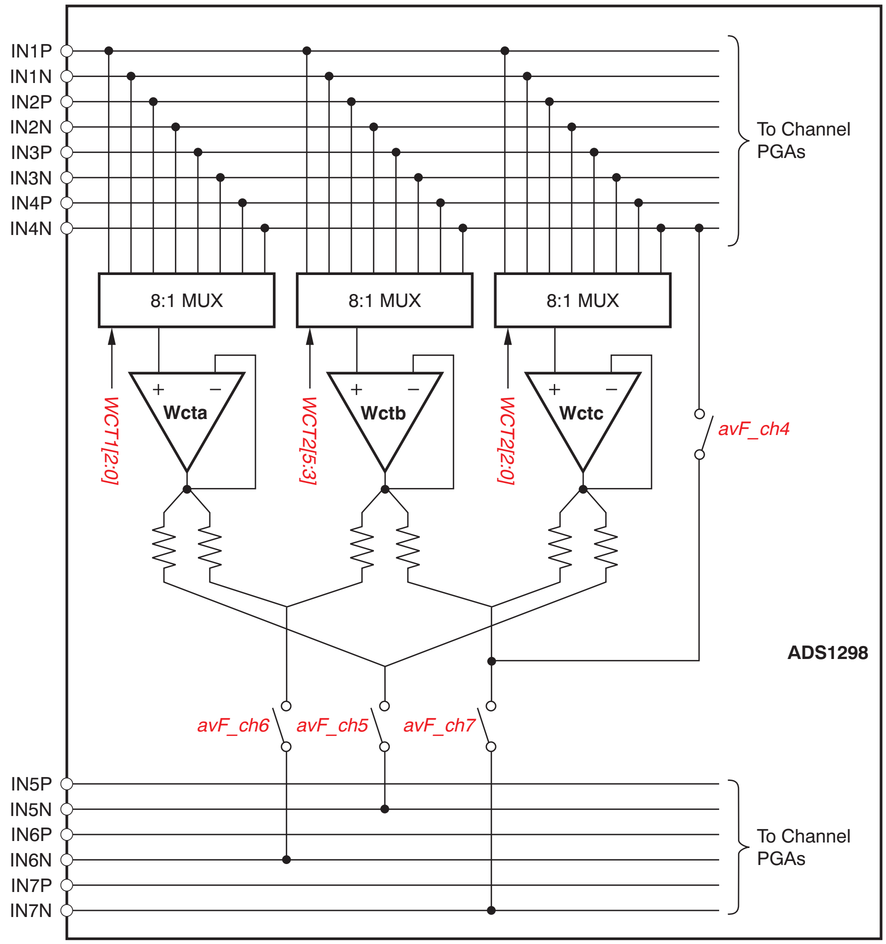


Figure 49. Analog Domain Augmented Leads

Right Leg Drive with the WCT Point

In certain applications, the out-of-phase version of the WCT is used as the right leg drive reference. The ADS1298 provides the option to have a buffered version of the WCT terminal at the RLD_OUT pin. This signal can be inverted in phase using an external amplifier and used as the right leg drive. Refer to the *Right Leg Drive (RLD DC Bias Circuit)* section for more details.

Lead-Off Detection

Patient electrode impedances are known to decay over time. It is necessary to continuously monitor these electrode connections to verify a suitable connection is present. The ADS1294/6/8 lead-off detection functional block provides significant flexibility to the user to choose from various lead-off detection strategies. Though called lead-off detection, this is in fact an *electrode-off* detection.

The basic principle is to inject an excitation signal and measure the response to find out if the electrode is off. As shown in the lead-off detection functional block diagram in Figure 52, this circuit provides two different methods of determining the state of the patient electrode. The methods differ in the frequency content of the excitation signal. Lead-off can be selectively done on a per channel basis using the LOFF_SENSP and LOFF_SENSN registers. Also, the internal excitation circuitry can be disabled and just the sensing circuitry can be enabled.

DC Lead-Off

In this method, the lead-off excitation is with a dc signal. The dc excitation signal can be chosen from either a pull-up/pull-down resistor or a current source/sink, shown in Figure 50. The selection is done by setting the VLEAD_OFF_EN bit in the LOFF register. One side of the channel is pulled to supply and the other side is pulled to ground. The pull-up resistor and pull-down resistor can be swapped (as shown in Figure 51) by setting the bits in the LOFF_FLIP register. In case of current source/sink, the magnitude of the current can be set by using the ILEAD_OFF[1:0] bits in the LOFF register. The current source/sink gives larger input impedance compared to the 10MΩ pull-up/pull-down resistor.

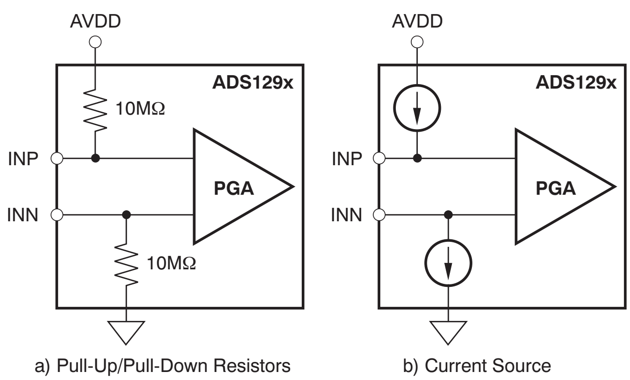


Figure 50. DC Lead-Off Excitation Options

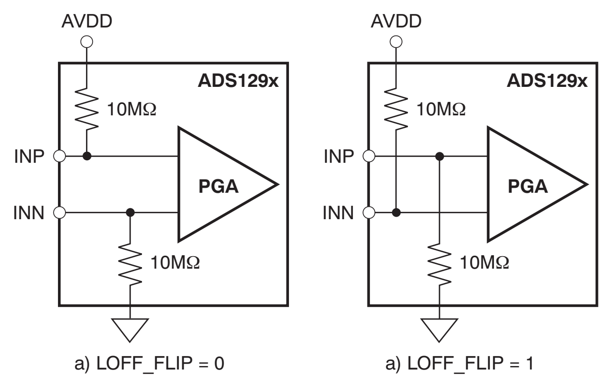


Figure 51. LOFF_FLIP Usage

Sensing of the response can be done either by looking at the digital output code from the device or by monitoring the input voltages with an on-chip comparator. If either of the electrodes is off, the pull-up resistors and/or the pull-down resistors saturate the channel. By looking at the output code it can be determined that either the P-side or the N-side is off. To pinpoint which one is off, the comparators must be used. The input voltage is also monitored using a comparator and a 4-bit DAC whose levels are set by the COMP_TH[2:0] bits in the LOFF register. The output of the comparators are stored in the LOFF_STATUSP and LOFF_STATUSN registers. These two registers are available as a part of the output data stream. (See the *Data Output Protocol (DOUT)* subsection of the *SPI Interface* section.) If dc lead-off is not used, the lead-off comparators can be powered down by setting the PD_LOFF_COMP bit in the CONFIG4 register.

An example procedure to turn on dc lead-off is given in the *Lead-Off* subsection of the *Guide to Get Up and Running* section.

AC Lead-Off

In this method, an out-of-band ac signal is used for excitation. The ac signal is generated by alternatively providing pull-up resistors and pull-down resistors at the input with a fixed frequency. The ac signal is passed through an anti-aliasing filter to avoid aliasing. The frequency can be chosen by the FLEAD_OFF[1:0] bits in the LOFF register. The excitation frequency is a function of the output data rate and is $f_{DR}/4$. This out-of-band excitation signal is passed through the channel and measured at the output.

Sensing of the ac signal is done by passing the signal through the channel to digitize it and measure at the output. The ac excitation signals are introduced at a frequency that is above the band of interest, generating an out-of-band differential signal that can be filtered out separately and processed. By measuring the magnitude of the excitation signal at the output spectrum, the lead-off status can be calculated. Therefore, the ac lead-off detection can be accomplished simultaneously with the ECG signal acquisition.

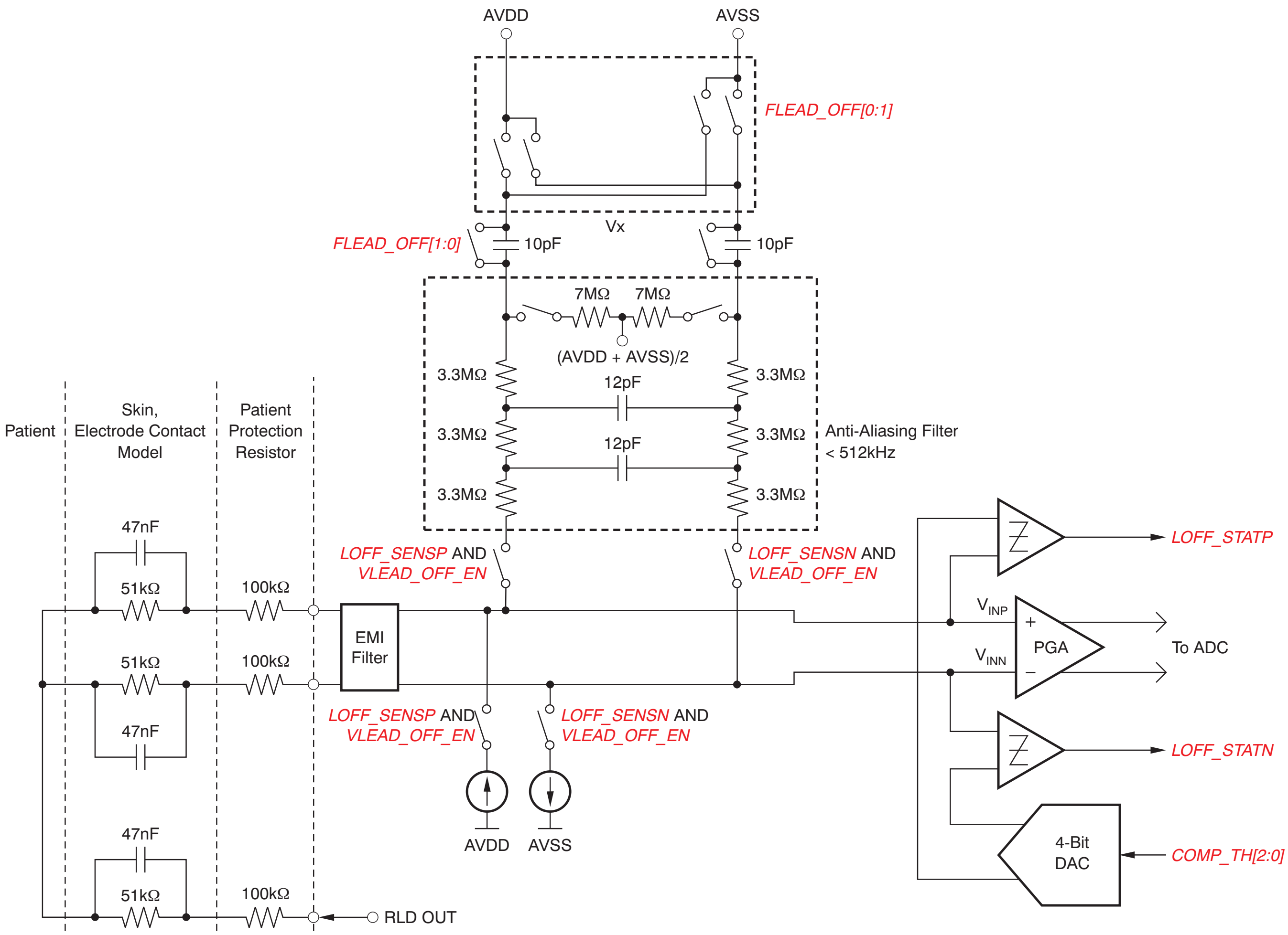


Figure 52. Lead-Off Detection

RLD Lead-Off

The ADS1294/6/8 provide two modes for determining whether the RLD is correctly connected:

- RLD lead-off detection during normal operation
- RLD lead-off detection during power-up

The following sections provide details of the two modes of operation.

RLD Lead-Off Detection During Normal Operation

During normal operation, the ADS1294/6/8 RLD lead-off at power-up function cannot be used because it is necessary to power off the RLD amplifier.

RLD Lead Off Detection At Power-Up

This feature is included in the ADS1294/6/8 for use in determining whether the right leg electrode is suitably connected. At power-up, the ADS1294/6/8 provide two measurement procedures to determine the RLD electrode connection status using either a current or a voltage pull-down resistor, as shown in Figure 53. The reference level of the comparator is set to determine the acceptable RLD impedance threshold.

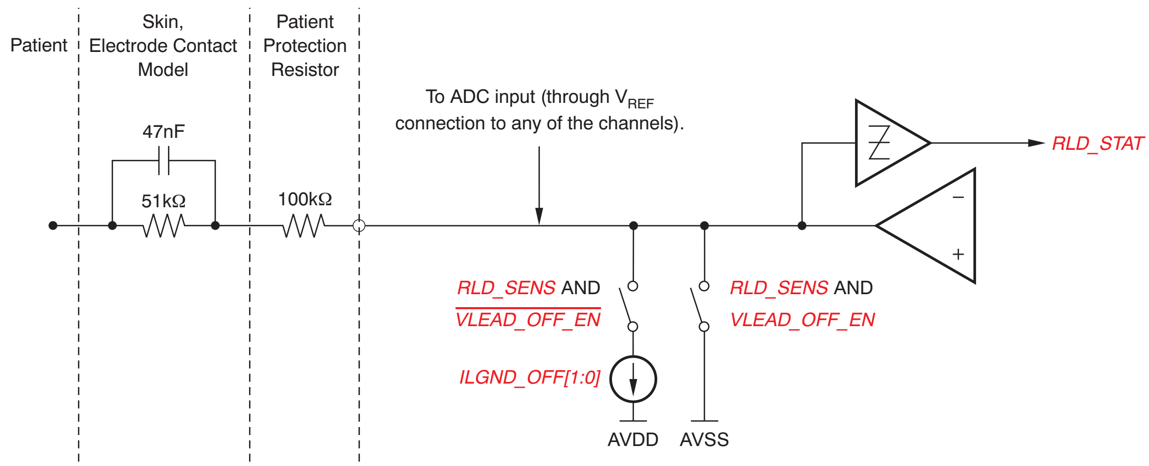


Figure 53. RLD Lead-Off Detection at Power-Up

When the RLD amplifier is powered on, the current source has no function. Only the comparator can be used to sense the voltage at the output of the RLD amplifier. The comparator thresholds are set by the same LOFF[7:5] bits used to set the thresholds for other negative inputs.

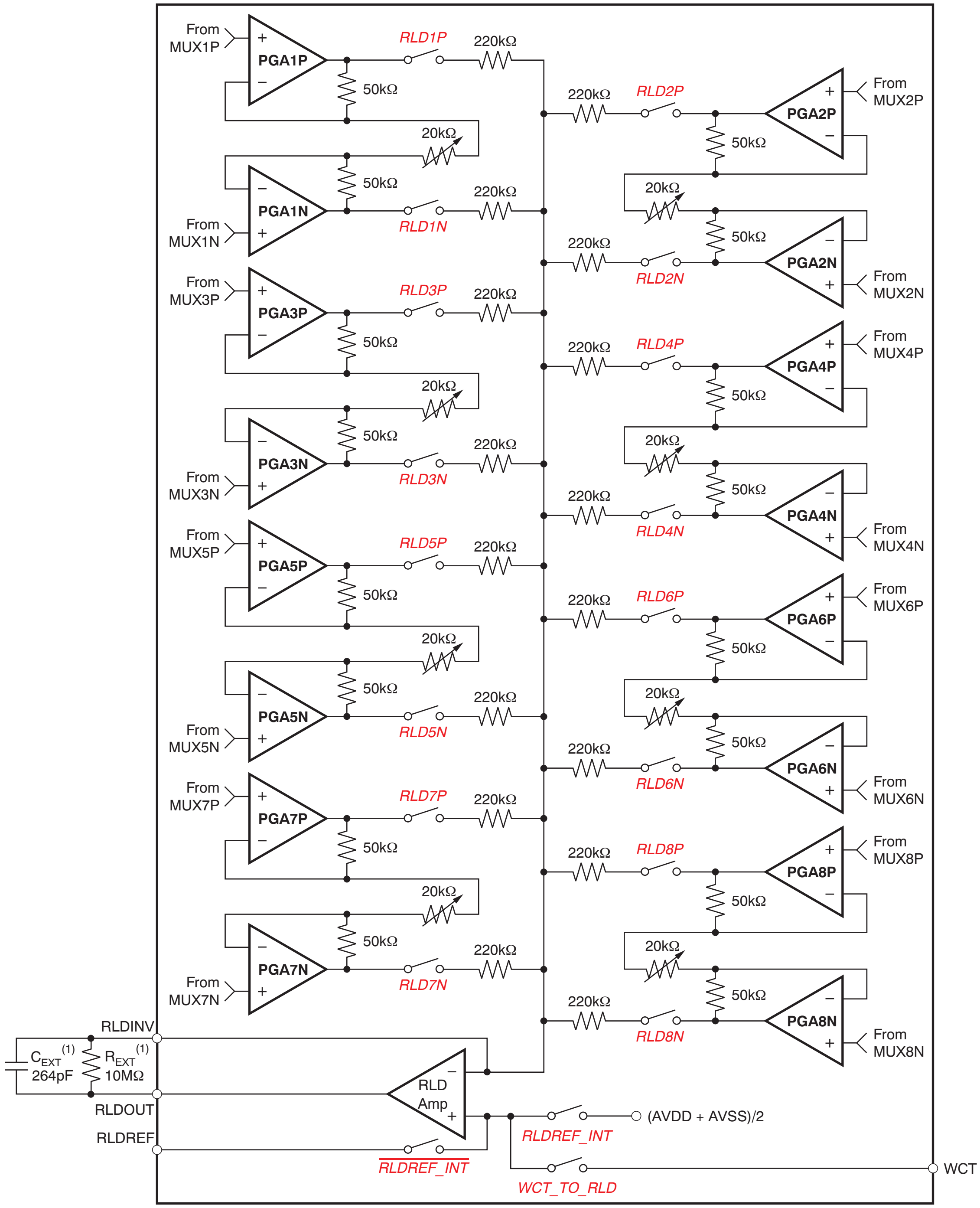
Right Leg Drive (RLD DC Bias Circuit)

The right leg drive (RLD) circuitry is used as a means to counter the common-mode interference in a ECG system as a result of power lines and other sources, including fluorescent lights. The RLD circuit senses the common-mode of a selected set of electrodes and creates a negative feedback loop by driving the body with an inverted common-mode signal. The negative feedback loop restricts the common-mode movement to a narrow range, depending on the loop gain. Stabilizing the entire loop is specific to the individual user system based on the various poles in the loop. The ADS1294/6/8 integrates the muxes to select the channel and an operational amplifier. All the amplifier terminals are available at the pins, allowing the user to choose the components for the feedback loop. The circuit shown in Figure 54 shows the overall functional connectivity for the RLD bias circuit.

The reference voltage for the right leg drive can be chosen to be internally generated (AVDD + AVSS)/2 or it can be provided externally with a resistive divider. The selection of an internal versus external reference voltage for the RLD loop is defined by writing the appropriate value to the RLDREF_INT bit in the COFIG3 register.

If the RLD function is not used, the amplifier can be powered down using the PD_RLD bit (see the *CONFIG3: Configuration Register 3* subsection of the *Register Map* section for details). This bit is also used in daisy-chain mode to power-down all but one of the RLD amplifiers.

The functionality of the RLDIN pin is explained in the *Input Multiplexer* section. An example procedure to use the RLD amplifier is shown in the *Right Leg Drive* subsection of the *Guide to Get Up and Running* section.



(1) Typical values.

Figure 54. RLD Channel Selection

WCT as RLD

In certain applications, the right leg drive is derived as the average of RA, LA, and LL. This level is the same as the WCT voltage. The WCT amplifier has limited drive strength and thus should be used only to drive very high impedances directly. The ADS1294/6/8 provide an option to internally buffer the WCT signal by setting the WCT_TO_RLD bit in the CONFIG4 register. The RLD_OUT and RLD_INV pins should be shorted external to the device. Note that before the RLD_OUT signal is connected to the RLD electrode, an external amplifier should be used to invert the phase of the signal for negative feedback.

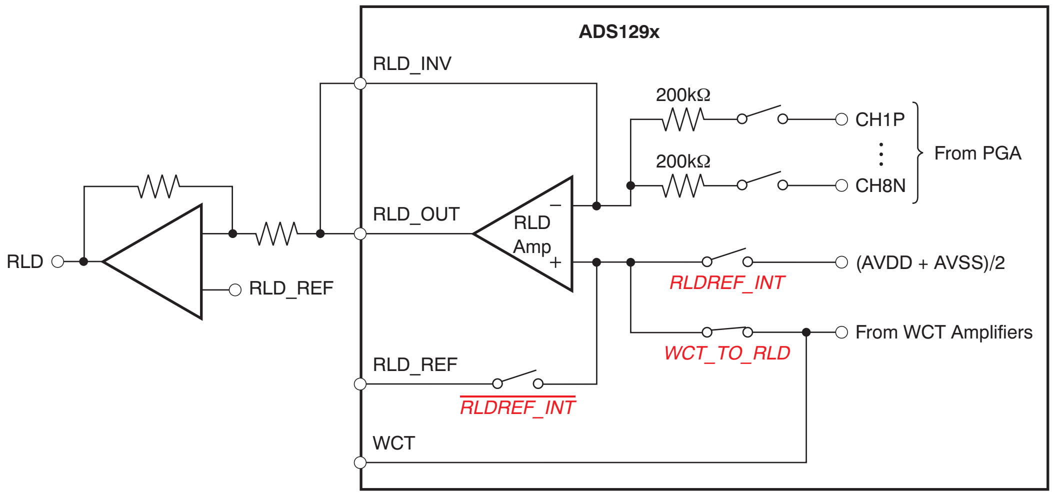


Figure 55. Using the WCT as the Right Leg Drive

RLD Configuration with Multiple Devices

Figure 56 shows multiple devices connected to an RLD.

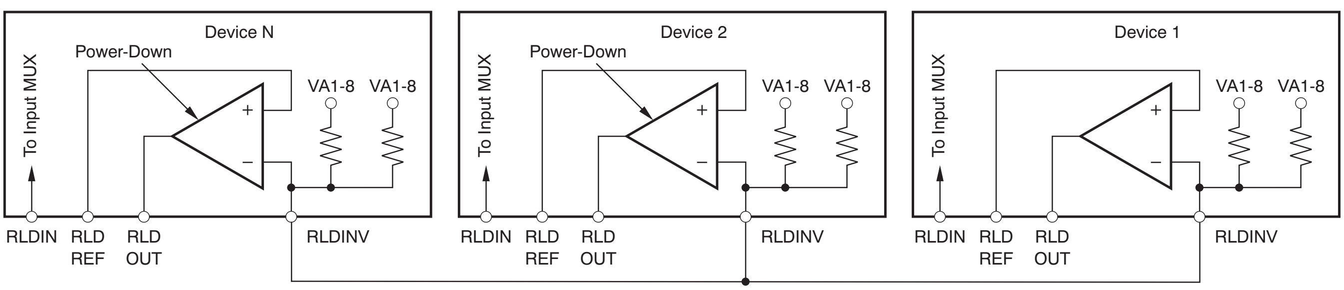


Figure 56. RLD Connection for Multiple Devices

Pace Detect

The ADS1294/6/8 provide flexibility for PACE detection either in software or by external hardware. The software approach is made possible by providing sampling rates up to 32kSPS. The external hardware approach is made possible by bringing out the output of the PGA at two pins: TESTP_PACE_OUT1 and TESTN_PACE_OUT2. Note that if the WCT amplifier is connected to the signal path, the user sees switching noise as a result of chopping; see the *Wilson Central Terminal (WCT)* section for details.

Software Approach

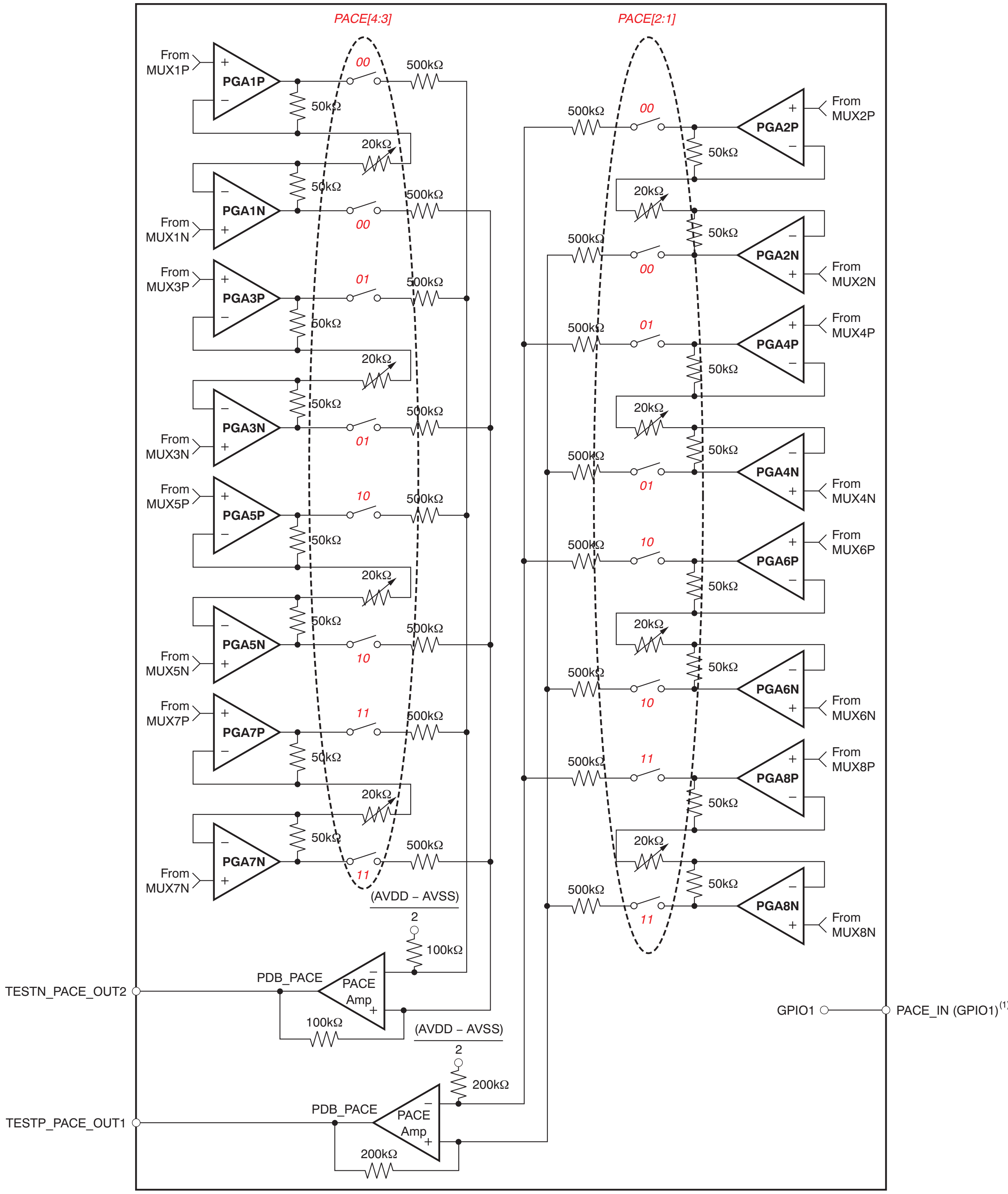
To use the software approach, the device must be operated at 8kSPS or more to be able to capture the fastest pulse. Afterwards, digital signal processing can be used to identify the presence of the pacemaker pulse. The software approach gives the utmost flexibility to the user to be able to program the pace detect threshold on the fly using software. This becomes increasingly important as pacemakers evolve over time. Two parameters must be considered while measuring fast pace pulses:

1. The PGA bandwidth shown in Table 6.
2. For a step change in input, the digital decimation filter takes 3 × t_{DR} to settle. The PGA bandwidth determines the gain setting that can be used and the settling time determines the data rate that the device must be operated at.

External Hardware Approach

One of the drawbacks of using the software approach is that all channels on a single device need to operate at higher data rates. For systems where it is of concern, The ADS1294/6/8 provide the option of bringing out the output of the PGA. External hardware circuitry can be used to detect the presence of the pulse. The output of the pace detection logic can then be fed into the device through one of the GPIO pins. The GPIO data are transmitted through the SPI port. Two of the eight channels can be selected using register bits in the PACE register, one from the odd-numbered channels and the other from the even-numbered channels. During the differential to single-ended conversion, there is an attenuation of 0.4. Therefore, the total gain in the pace path is equal to (0.4 × PGA_GAIN). The pace out signals are multiplexed with the TESTP and TESTN signals through the TESTP_PACE_OUT1 and TESTN_PACE_OUT2 pins respectively. The channel selection is done by setting bits[4:1] of the PACE register. If the pace circuitry is not used, the pace amplifiers can be turned off using the PD_PACE bit in the PACE register.

Note that if the output of a channel connected to the WCT amplifier (for example, the *V* lead channels) is connected to one of the pace amplifiers for external pace detection, the artifact of chopping appears at the pace amplifier output. Refer to the *Wilson Central Terminal (WCT)* section for more details.



(1) GPIO1 can be used as the PACE_IN signal.

Figure 57. Hardware Pace Detection Option

Respiration

The ADS1294/6/8 provide clock signals for driving external respiration circuitry, as shown in Table 13.

Table 13. Respiration Control

RESP_CTRL[1]	RESP_CTRL[0]	DESCRIPTION
0	0	No respiration
0	1	External respiration circuitry required. The ADS1294/6/8 send clocks that can be used with the external respiration circuitry through the GPIO2, GPIO3, and GPIO4 pins.

External Respiration Circuitry Option

This mode is set by RESP_CTRL = 01. In this mode, GPIO2, GPIO3, and GPIO4 are automatically configured as outputs. The phase relationship between the signals is shown in Figure 58. GPIO2 is the exor of GPIO3 and GPIO4; GPIO3 is the in-phase signal; and GPIO4 is the out-of-phase signal. Note that GPIO2, GPIO3, and GPIO4 are available for other use in this mode. The frequency is set by the RESP_FREQ[2:0] bits in the CONFIG4 register. The phase is set by the RESP_PH[2:0] bits in the RESP register.

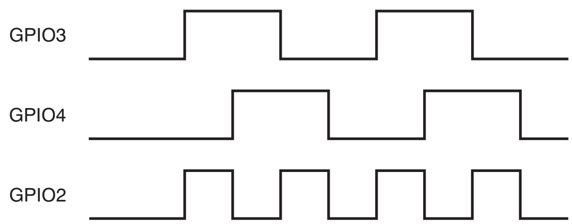


Figure 58. GPIOx Timing Diagram

GUIDE TO GET UP AND RUNNING

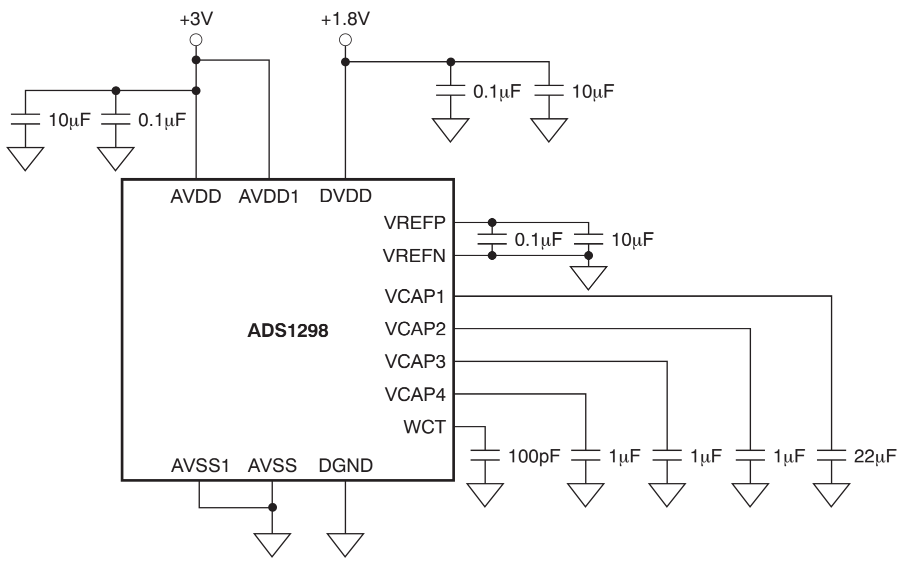
PCB LAYOUT

Power Supplies and Grounding

The ADS1294/6/8 has three supplies: AVDD, AVDD1, and DVDD. Both AVDD and AVDD1 should be as quiet as possible. AVDD1 provides supply to the charge pump block and has transients at f_{CLK}. So it is recommended that AVDD1 and AVSS1 be star connected to AVDD and AVSS. It is important to eliminate noise from AVDD and AVDD1 that is non-synchronous with the ADS1294/6/8 operation; see the EVM layout for star ground connection example (application report SBAA175, *SPI Timing Considerations for the ADS119x/129x Devices*). Each supply of the ADS1294/6/8 should be bypassed with 10μF and a 0.1μF solid ceramic capacitors. It is recommended that placement of the digital circuits (DSP, microcontrollers, FPGAs, etc) in the system is done such that the return currents on those devices do not cross the analog return path of the ADS1294/6/8. The ADS1294/6/8 can be powered from unipolar or bipolar supplies.

Connecting the Device to Unipolar (+3V/+1.8V) Supplies

Figure 59 illustrates the ADS1294/6/8 connected to a unipolar supply. In this example, analog supply (AVDD) is referenced to analog ground (AVSS) and digital supplies (DVDD) are referenced to digital ground (DGND).

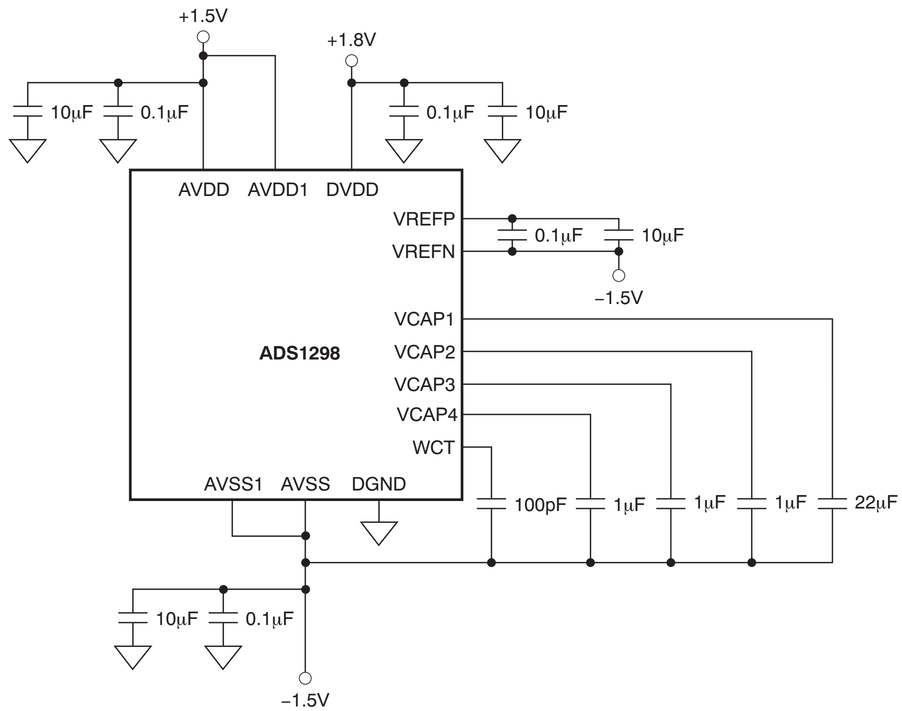


NOTE: Place the capacitors for supply, reference, WCT, and VCAP1 to VCAP4 as close to the package as possible.

Figure 59. Single-Supply Operation

Connecting the Device to Bipolar (±1.5V/1.8V) Supplies

Figure 60 illustrates the ADS1294/6/8 connected to a bipolar supply. In this example, the analog supplies connect to the device analog supply (AVDD). This is referenced to the device analog return (AVSS) and digital supplies (DVDD and DVDD) are referenced to the device digital ground return (DVDD).



NOTE: Place the capacitors for supply, reference, WCT, and VCAP1 to VCAP4 as close to the package as possible.

Figure 60. Bipolar Supply Operation

Shielding Analog Signal Paths

As with any precision circuit, careful printed circuit board (PCB) layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins and AVSS. These analog input pins are high-impedance and extremely sensitive to extraneous noise. The AVSS pin should be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the input bias current of the ADS1294/6/8 if shielding is not implemented. Digital signals should be kept as far as possible from the analog input signals on the PCB.

POWER-UP SEQUENCING

Before device power-up, all digital and analog inputs must be low. At the time of power-up, all of these signals should remain low until the power supplies have stabilized, as shown in Figure 61. At this time, begin supplying the master clock signal to the CLK pin. Wait for time t_{POR}, then transmit a RESET pulse. After releasing RESET, the configuration register must be programmed, see the *CONFIG1: Configuration Register 1* subsection of the *Register Map* section for details. The power-up sequence timing is shown in Table 14.

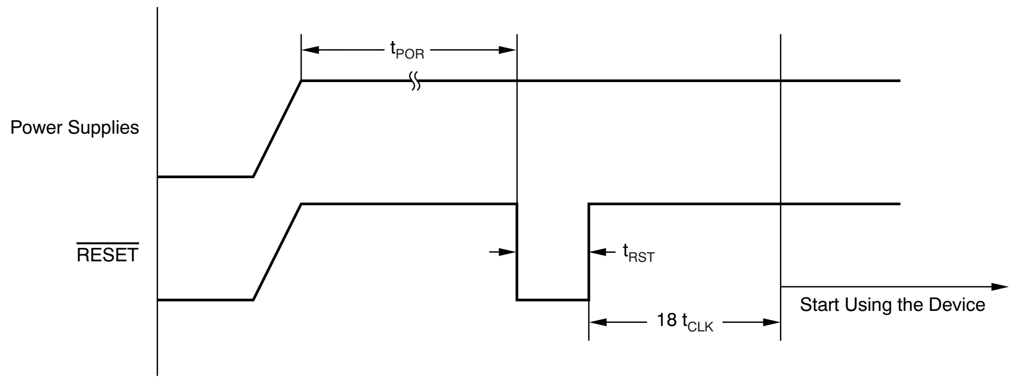


Figure 61. Power-Up Timing Diagram

Table 14. Power-Up Sequence Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{POR}	Wait after power-up until reset	2^{16}			t_{CLK}
t_{RST}	Reset low width	2			t_{CLK}

SETTING THE DEVICE FOR BASIC DATA CAPTURE

The following section outlines the procedure to configure the device in a basic state and capture data. This procedure is intended to put the device in a data sheet condition to check if the device is working properly in the user's system. It is recommended that this procedure be followed initially to get familiar with the device settings. Once this procedure has been verified, the device can be configured as needed. For details on the timings for commands refer to the appropriate sections in the data sheet. Also, some sample programming codes are added for the ECG-specific functions.

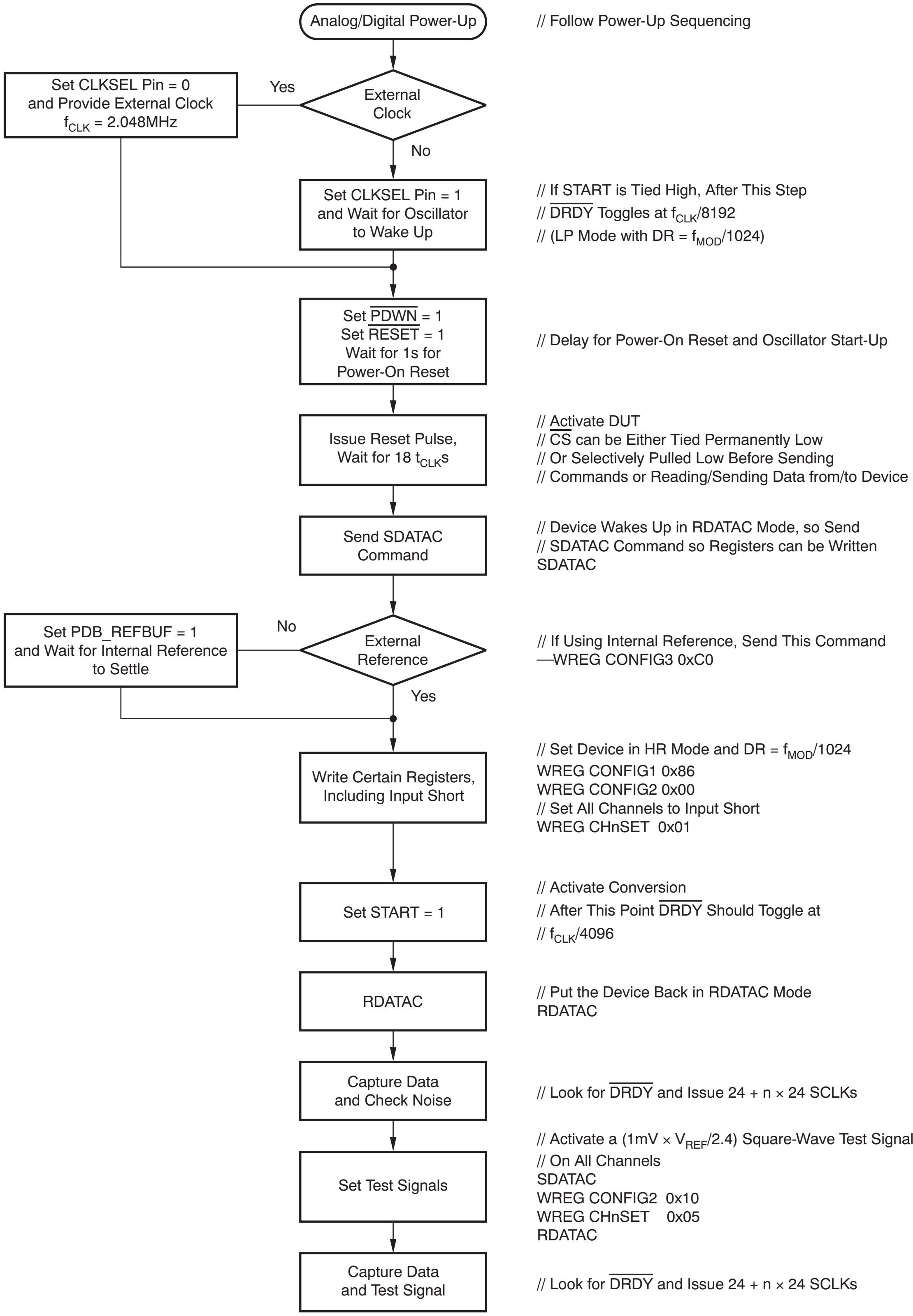


Figure 62. Initial Flow at Power-Up

Lead-Off

Sample code to set dc lead-off with pull-up/pull-down resistors on all channels

WREG LOFF 0x13 // Comparator threshold at 95% and 5%, pull-up/pull-down resistor // DC lead-off

WREG CONFIG4 0x02 // Turn-on dc lead-off comparators

WREG LOFF_SENSP 0xFF // Turn on the P-side of all channels for lead-off sensing

WREG LOFF_SENSN 0xFF // Turn on the N-side of all channels for lead-off sensing

Observe the status bits of the output data stream to monitor lead-off status.

Right Leg Drive

Sample code to choose RLD as an average of the first three channels.

WREG RLD_SENSP 0x07 // Select channel 1—3 P-side for RLD sensing

WREG RLD_SENSN 0x07 // Select channel 1—3 N-side for RLD sensing

WREG CONFIG3 b’x1xx 1100 // Turn on RLD amplifier, set internal RLDREF voltage

Sample code to route the RLD_OUT signal through channel 4 N-side and measure RLD with channel 5. Make sure the external side to the chip RLDOUT is connected to RLDIN.

WREG CONFIG3 b’xxx1 1100 // Turn on RLD amplifier, set internal RLDREF voltage, set RLD measurement bit

WREG CH4SET b’1xxx 0111 // Route RLDIN to channel 4 N-side

WREG CH5SET b’1xxx 0010 // Route RLDIN to be measured at channel 5 w.r.t RLDREF

Pace Detection

Sample code to select channel 5 and 6 outputs for PACE

WREG PACE b’0001 0101 // Power-up pace amplifier and select channel 5 and 6 for pace out

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS1294CZXGR	PREVIEW	NFBGA	ZXG	64		TBD	Call TI	Call TI	Samples Not Available
ADS1294CZXGT	PREVIEW	NFBGA	ZXG	64		TBD	Call TI	Call TI	Samples Not Available
ADS1294IPAG	PREVIEW	TQFP	PAG	64		TBD	Call TI	Call TI	Samples Not Available
ADS1294IPAGR	PREVIEW	TQFP	PAG	64		TBD	Call TI	Call TI	Samples Not Available
ADS1296CZXGR	PREVIEW	NFBGA	ZXG	64		TBD	Call TI	Call TI	Samples Not Available
ADS1296CZXGT	PREVIEW	NFBGA	ZXG	64		TBD	Call TI	Call TI	Samples Not Available
ADS1296IPAG	PREVIEW	TQFP	PAG	64		TBD	Call TI	Call TI	Samples Not Available
ADS1296IPAGR	PREVIEW	TQFP	PAG	64		TBD	Call TI	Call TI	Samples Not Available
ADS1298CZXGR	ACTIVE	NFBGA	ZXG	64	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	Purchase Samples
ADS1298CZXGT	ACTIVE	NFBGA	ZXG	64	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	Request Free Samples
ADS1298IPAG	PREVIEW	TQFP	PAG	64	160	TBD	Call TI	Call TI	Samples Not Available
ADS1298IPAGR	PREVIEW	TQFP	PAG	64	1500	TBD	Call TI	Call TI	Samples Not Available
PADS1294IPAG	PREVIEW	TQFP	PAG	64		TBD	Call TI	Call TI	Samples Not Available
PADS1296IPAG	PREVIEW	TQFP	PAG	64		TBD	Call TI	Call TI	Samples Not Available
PADS1298IPAG	PREVIEW	TQFP	PAG	64		TBD	Call TI	Call TI	Samples Not Available

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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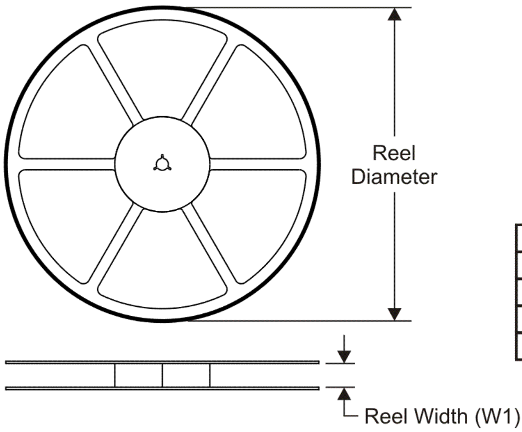
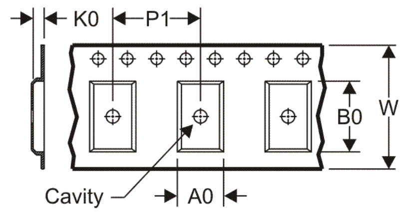
TAPE AND REEL INFORMATION

REEL DIMENSIONS

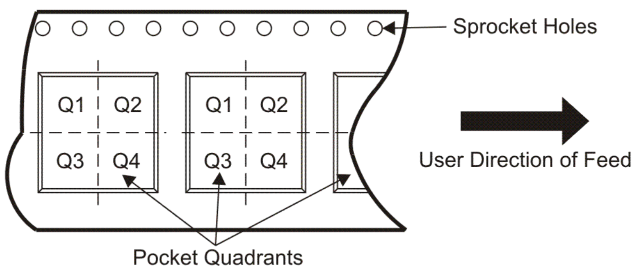


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

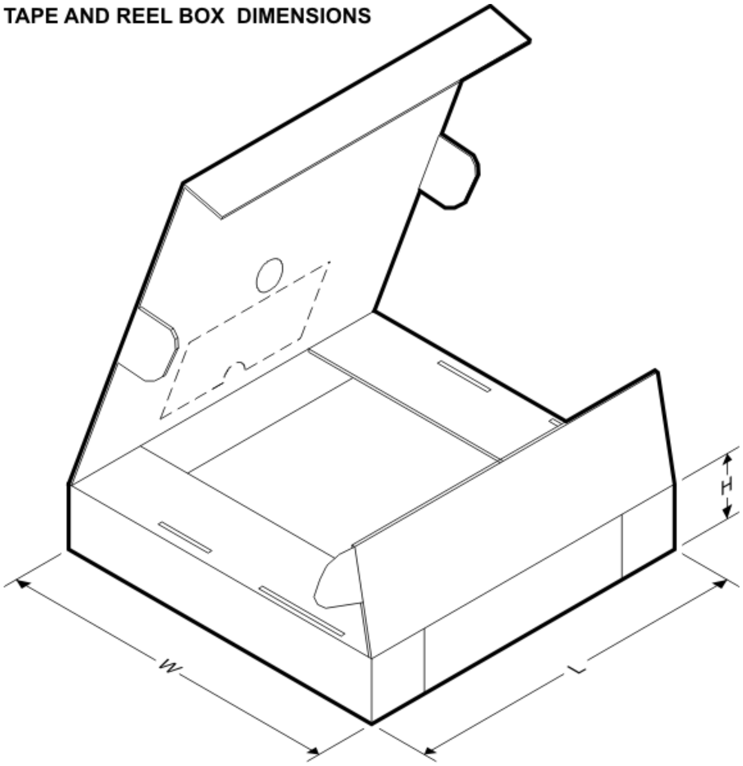
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1298CZXGR	NFBGA	ZXG	64	1000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q1
ADS1298CZXGT	NFBGA	ZXG	64	250	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q1

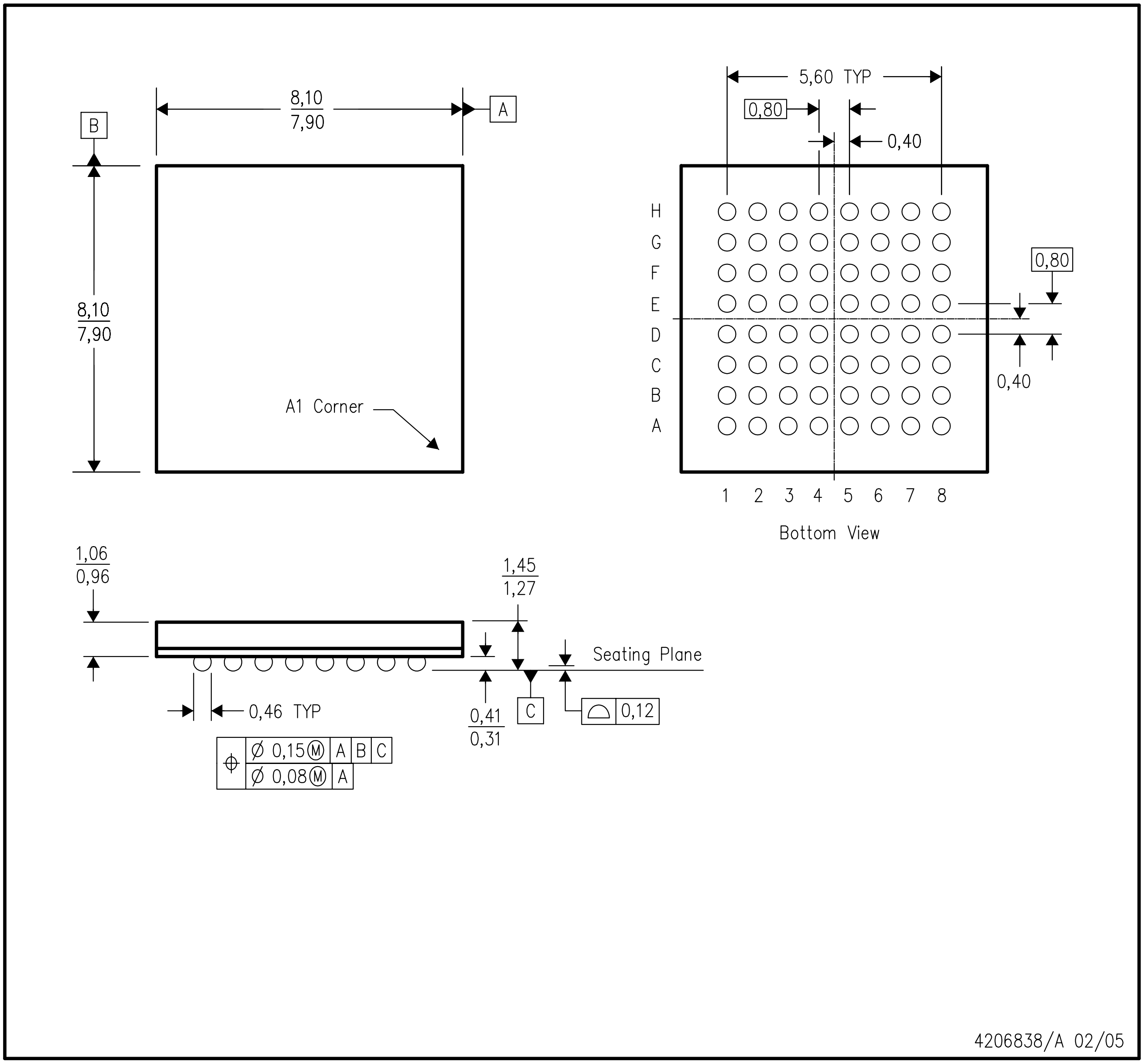
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

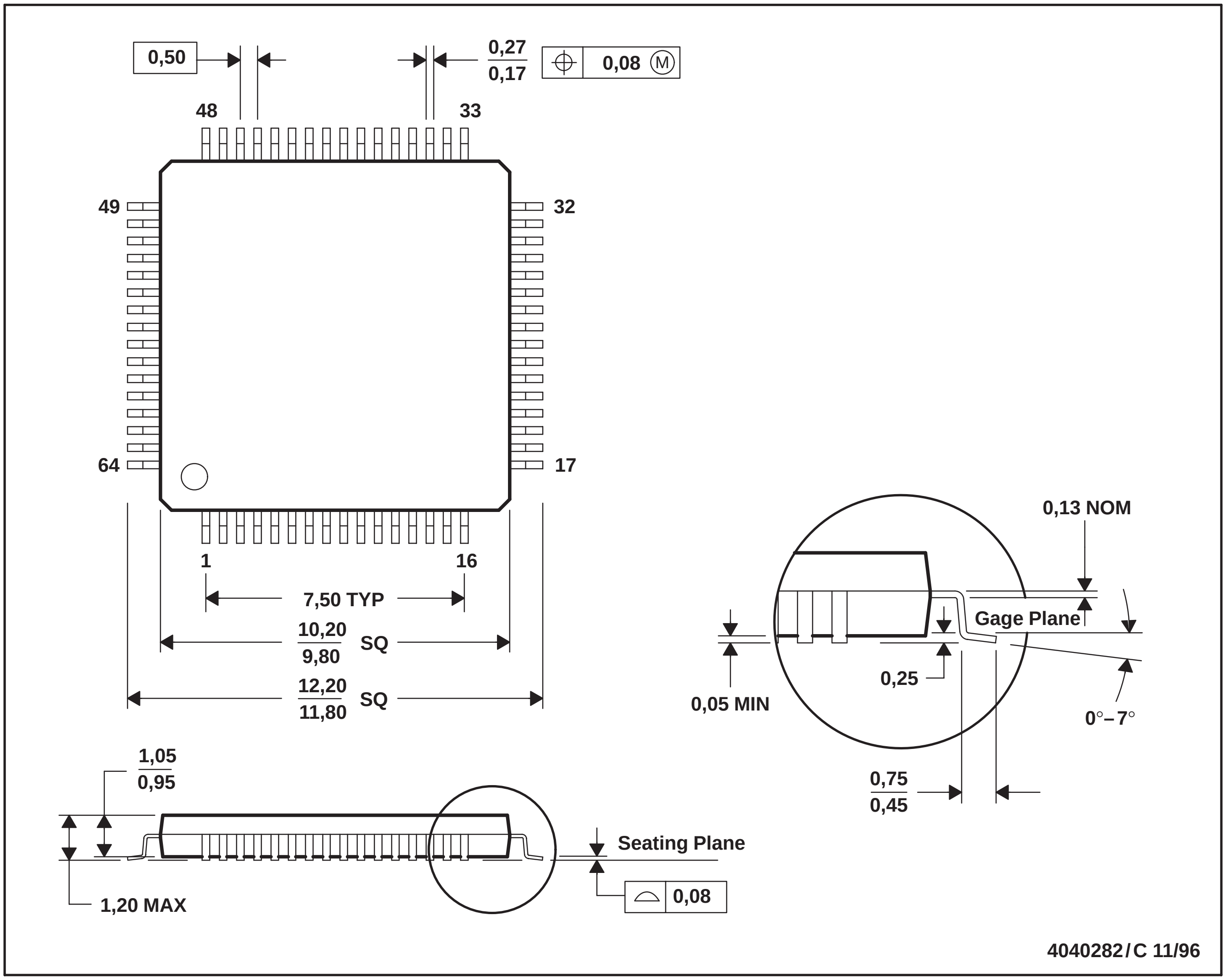
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1298CZXGR	NFBGA	ZXG	64	1000	333.2	345.9	28.6
ADS1298CZXGT	NFBGA	ZXG	64	250	333.2	345.9	28.6

ZXG (S–PBGA–N64) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. This package is lead–free.

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026