GENLINX™ *II* GS9028 Cable Driver with Two Adjustable Outputs

DATA SHEET

FEATURES

- **SMPTE 259M compliant**
- **two complementary outputs, adjustable from 50 to 1000mVp-p into 75Ω loads**
- **operational from DC to 622Mb/s**
- **nominal 470ps rise and fall times**
- **< ±7% output amplitude control**
- **45% system power reduction over the GS9008**
- **no external pulldown resistors required**
- **input hysteresis**
- **operational down to 80mV input amplitude**
- **operates from a single +5 or -5 volt supply**
- **8 pin SOIC**
- **Pb-free and Green**

APPLICATIONS

4*f*sc, 4:2:2, and 4:4:4:4 serial digital video interfaces from 143Mb/s to 540Mb/s; general purpose high speed cable driver applications.

DESCRIPTION

The GS9028 is a second generation bipolar integrated circuit designed to drive two 75Ω co-axial cables.

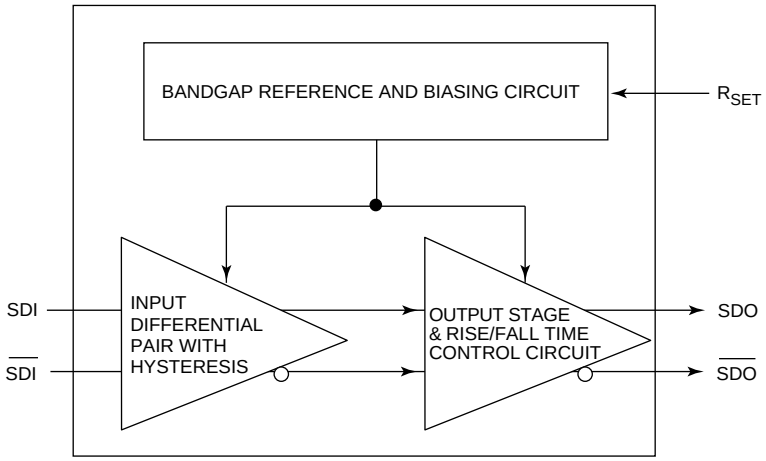
The GS9028 features two complementary outputs whose amplitude is controlled within ± 7%. The output signal levels are also adjustable from as low as 50mV to as high as 1000mV with little change in other performance parameters. The output amplitude of the output stage is varied by adjusting the R_{SET} resistor value.

The GS9028 consumes 45% less system power than the GS9008 and does not require external pulldown resistors resulting in a smaller PCB footprint. Operational with input amplitudes as low as 80mV, the GS9028 is a robust serial interface device.

The GS9028 is packaged in an 8 pin SOIC and operates from a single +5 or -5 volt supply.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	Pb-FREE AND GREEN
GS9028-CKA	8 pin SOIC	0°C to 70°C	No
GS9028-CTA	8 pin SOIC Tape	0°C to 70°C	No
GS9028-CKAE3	8 pin SOIC	0°C to 70°C	Yes
GS9028-CTAE3	8 pin SOIC Tape	0°C to 70°C	Yes



BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified

PARAMETER	VALUE
Supply Voltage	5.5V
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0 to 70°C
Storage Temperature	-65 to 150°C
Lead Temperature (soldering, 10 sec)	260°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 0°C to 70°C unless otherwise shown. Specifications assume 800mV output amplitude levels into end terminated 75Ω transmission lines.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Supply Voltage	V_{CC}		4.75	5.00	5.25	V		1
System Power Consumption	P_D	Driving two 75Ω cables	-	165	195	mW		3
Supply Current	I_S		-	33	39	mA		3
Common Mode Input Voltage Range	$V_{CM,IN}$		2.4+(V_{DIFF}/2)	-	V_{CC}-(V_{DIFF}/2)	V		2
Differential Input	V_{DIFF}		80	-	1000	mV		2
Common Mode Output Voltage Range	$V_{CM,OUT}$		-	V_{CC}-V_{OUT}	-	V		2
Differential Output	V_{OUT}	R_{SET} = 59Ω	750	800	850	mV		1
Input Hysteresis			10	-	-	mV		2

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 0°C to 70°C unless otherwise shown. Specifications assume 800mV output amplitude levels into end terminated 75Ω transmission lines.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Serial Data Rate			0	-	622	Mb/s		1
Additive Jitter		270Mb/s	-	25	-	ps p-p	1	2
		540Mb/s	-	25	-			
		622Mb/s	-	50	-			
Output Rise/Fall Time	t_R, t_F	20% - 80%	400	470	700	ps		3
Mismatch in Output Rise/Fall Times			-	50	100	ps		1
Overshoot			-	5	8	%		1
Duty Cycle Distortion			-	50	100	ps		2
Output Return Loss		540MHz	-	17	-	dB	2	

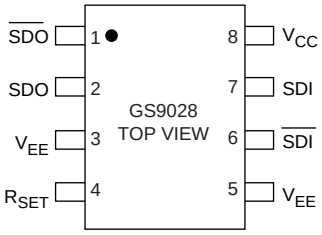
TEST LEVELS

1. 100% tested at 25°C.
2. Guaranteed by design.
3. Correlated value.

NOTES

1. RMS additive jitter measured using Pseudo Random bit sequence (2^{23} - 1).
2. Measured with Gennum Evaluation Board (EB-RD35).

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1	$\overline{SDO}$	O	Serial data output (inverse).
2	SDO	O	Serial data output.
4	R_{SET}	I	Output amplitude control resistor.
6	$\overline{SDI}$	I	Serial data input (inverse).
7	SDI	I	Serial data input.

INPUT/OUTPUT CIRCUITS

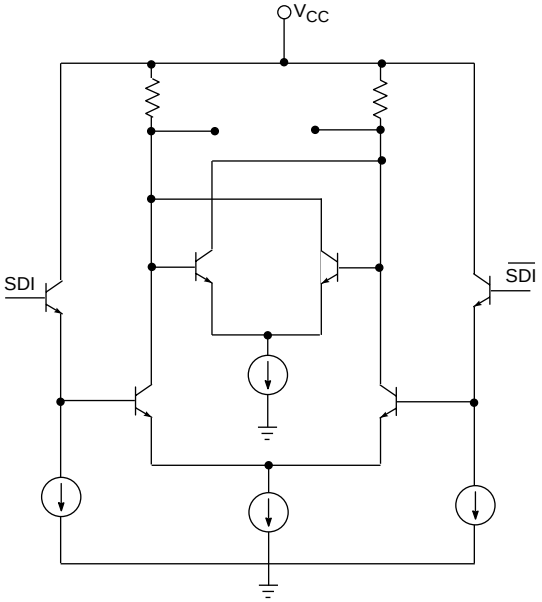


Fig. 1 Input Circuit (pins 6 and 7)

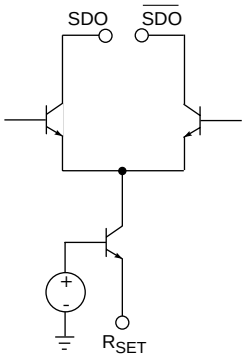


Fig. 2 Output Circuit (pins 1 and 2)

TYPICAL PERFORMACE CURVES (measured using the Typical Application Circuit)

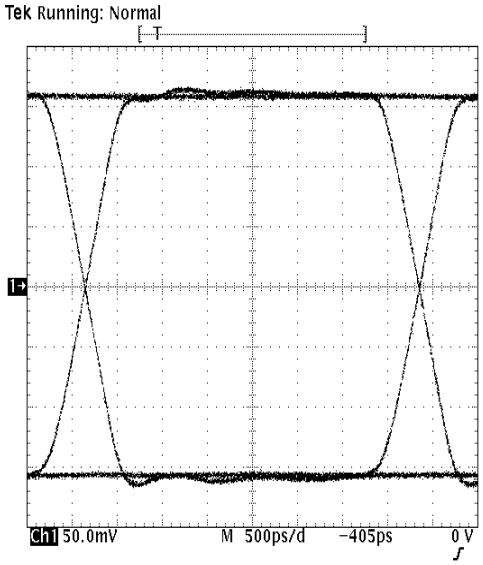


Fig. 3 Output Eye Diagram 270Mb/s

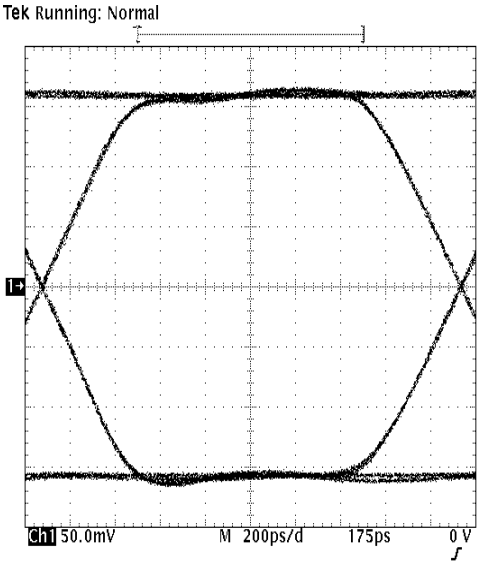


Fig. 4 Output Eye diagram 540Mb/s

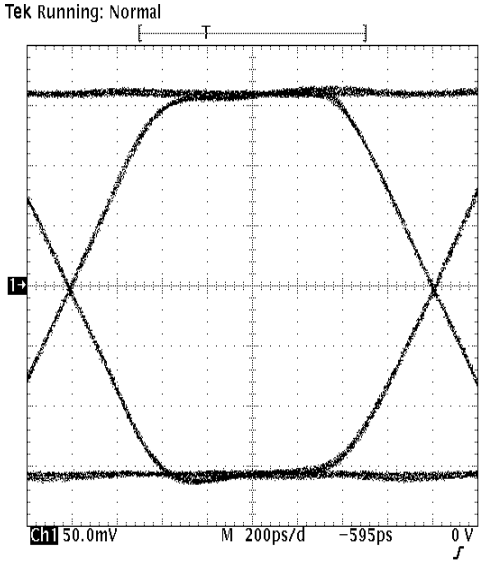


Fig. 5 Output Eye Diagram 622Mb/s

DETAILED DESCRIPTION

INPUT INTERFACING

SDI/$\overline{\text{SDI}}$ are high impedance differential inputs. Two conditions must be observed when interfacing to these inputs:

1. The input signal amplitude must be between 80mV and 1000mV.
2. The common mode voltage range must be as specified in the DC Characteristics Table (page 2). For 800mV input amplitude signals, this corresponds to a common mode voltage range between 2.8 and 4.6 volts.

Figures 6 and 7 illustrate two methods of interfacing the GS9028 to the Gennum GS9024 (Cable Equalizer), GS9035 (Reclocker) or the GS9025 (Receiver).

Figure 6 illustrates the simplest interface and is recommended when the trace lengths between the driver and the GS9028 are less than 0.5in. The pull up resistors should be placed near the GS9028 to serve as end terminations.

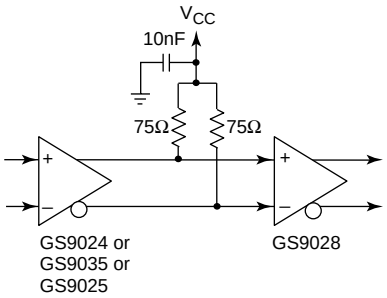


Fig. 6

When trace lengths become longer than 0.5in and data rates greater than 360Mb/s, electromagnetic reflections begin to affect signal integrity. To minimize reflections, controlled impedance traces and source and end terminations should be used as shown in Figure 7. Although terminations on both sides reduce the signal swing by a factor of two, the GS9028 is designed to meet this need with ultra low input amplitude requirements (as low as 80mV). This low input amplitude requirement also allows the use of 50Ω transmission lines (which are more robust and easier to control in multilayer boards) to interconnect the GS9024/25/35 and the GS9028.

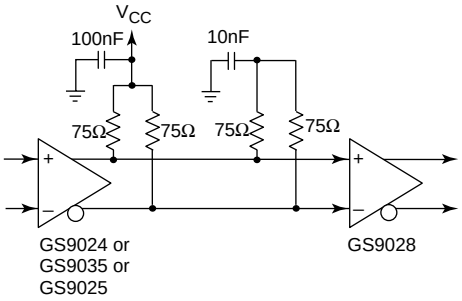


Fig. 7

The GS9028 can also be configured to accept ac coupled input signals. In this case, the inputs must be dc biased as illustrated in Figure 8.

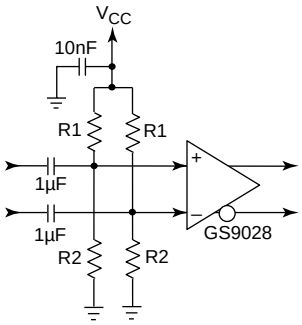


Fig. 8

The recommended values for R1 and R2 are:

$R1 = 1.35Z_O$

$R2 = 3.85Z_O$

where Z_O is the transmission line characteristic impedance.

For 75Ω cable, R1 = 100Ω and R2 = 287Ω.

OUTPUT INTERFACING

Figure 9 illustrates the recommended interface for ac coupled outputs.

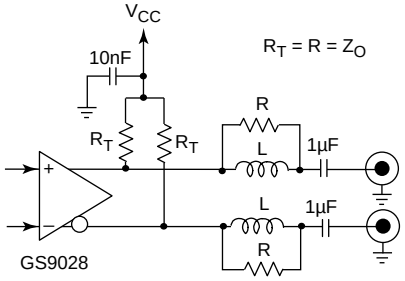


Fig. 9

The termination resistor (R_T) value should be equal to the characteristic impedance of the cable. Controlled impedance traces should be used for the outputs and the termination resistors should be placed near the GS9028. The inductor (L) and resistor (R) are used to optimize the output return loss and are PCB dependent. Typically, R equals the transmission line characteristic impedance and L is approximately 8.2nH.

OUTPUT AMPLITUDE ADJUSTMENT

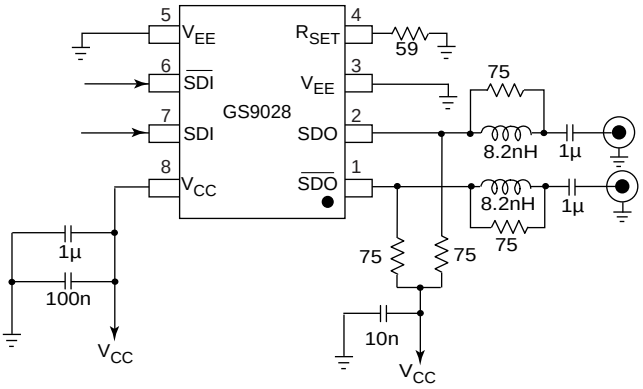
The GS9028 outputs are adjustable from as low as 50mV to as high as 1000mV. The output amplitude is set by the R_{SET} resistor connected to pin 4. The relationship between the output amplitude (V_{OUT}) and R_{SET} is approximately given by the equation below:

$R_{SET} = (1.3696 \times Z_O)/(2 \times V_{OUT}) - 5.5$

where Z_O is in ohms and V_{OUT} is in volts.

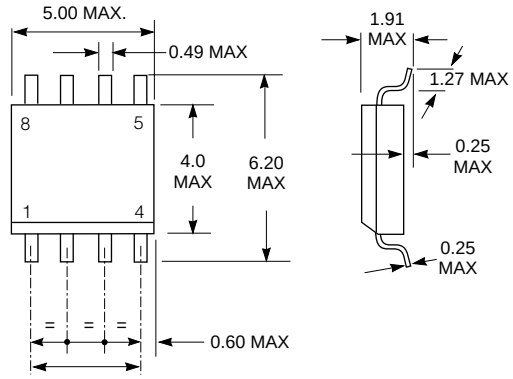
The minimum value of R_{SET} is 46Ω. For 75Ω cable and 800mV output amplitudes, the value of R_{SET} is 59Ω. Also, note that the above formula assumes that the transmission line is properly end terminated.

TYPICAL APPLICATION CIRCUIT



All resistors in ohms, all capacitors in farads, unless otherwise shown.

PACKAGE DIMENSIONS



8 pin SOIC

CAUTION

ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION

DATA SHEET

The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:

Added lead-free and green information.

GENNUM CORPORATION

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