SIEMENS

ICs for Communications

Two Channel Codec Filter with IOM®-2 Interface (IOM®-2 – SICOFI®-2)

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1 Overview

The two Channel Codec Filter PEB 2265 IOM-2 – SICOFI-2 is the logic continuation of a well-established family of Siemens Codec-Filter-ICs.

The IOM-2 – SICOFI-2 is a fully integrated PCM codec and filter fabricated in low power 1 µm CMOS technology for applications in digital communication systems. Based on an advanced digital filter concept, the PEB 2265 provides excellent transmission performance and high flexibility. The new filter concept (second generation) lends to a maximum of independence between the different filter blocks. Each filter block can be seen like an one to one representative of the corresponding network element.

Only very few external components are needed, to complete the functionality of the IOM-2 – SICOFI-2. The internal level accuracy is based on a very accurate bandgap reference. The frequency behavior is mainly determined by digital filters, which do not have any fluctuations. As a result of the new ADC and DAC concepts linearity is only limited by second order parasitic effects. Although the device works with only one single 5-V supply there is a very good dynamic range available.

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Two Channel Codec Filter with IOM®-2 Interface PEB 2265
IOM®-2 – SICOFI®-2

1.1 Features

P-MQFP-64-1-2

- Single chip CODEC and FILTER to handle two CO- or PABX-channels
- Specification according to relevant CCITT, EIA and LSSGR recommendations
- Digital signal processing technique
- Programmable interface optimized to current feed SLICs and transformer solutions
- Four pin serial IOM-2 Interface
- Single power supply 5 V
- Advanced low power 1µm analog CMOS technology
- Standard 64-pin P-MQFP-64 package
- High performance Analog to Digital Conversion
- High performance Digital to Analog Conversion
- Programmable digital filters to adapt the transmission behavior especially for
  - AC impedance matching
  - transhybrid balancing
  - frequency response
  - gain
- Advanced test capabilities
  - all digital pins can be tested within a boundary scan scheme (IEEE 1149.1)
  - five digital loops
  - four analog loops
  - two programmable tone generators per channel
- Comprehensive development platform available
  - software for automatic filter coefficient calculation – QSICOS
  - Hardware development board – STUT 2465

Type	Ordering Code	Package
PEB 2265 H V1.1	on request	P-MQFP-64-1-2

1.2 Pin Configuration (top view)

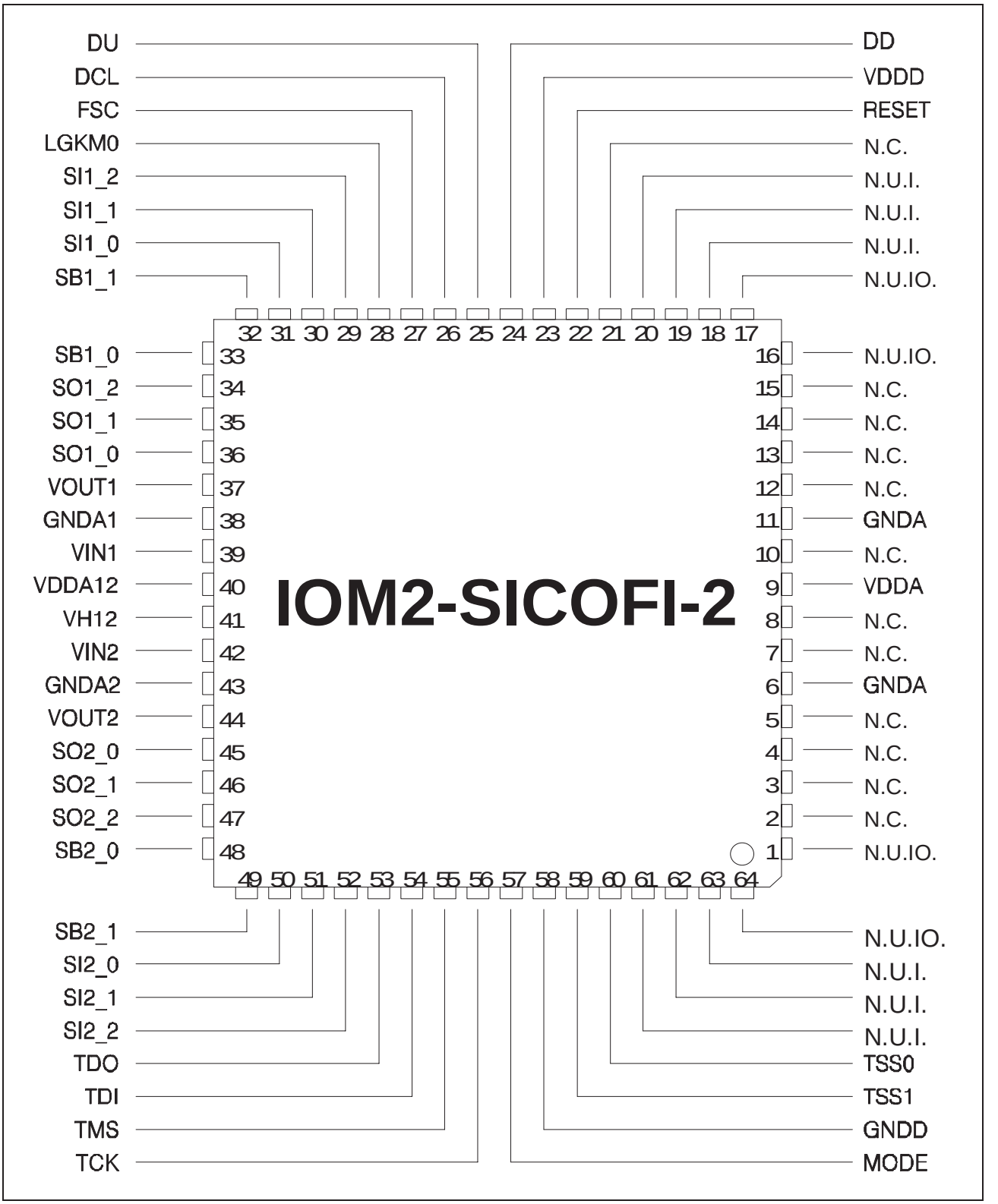


Figure 1

1.3 Pin Definition and Functions

1.3.1 Common Pins for all Channels

Table 1

Pin No.	Symbol	Input (I) Output (O)	Function
23	VDDD	I	+ 5 V supply for the digital circuitry[1)]
58	GNDD	I	Ground Digital, not internally connected to GNDA 1, 2 or GNDA (pin 6 and pin 11). All digital signals are referred to this pin
40	VDDA12	I	+ 5 V Analog supply voltage for channel 1 and 2[1)]
9	VDDA	I	+ 5 V Analog supply voltage[1)]
6,11	GNDA	I	Ground Analog, not internally connected to GNDD or GNDA1,2
27	FSC	I	IOM-2: Frame synchronization clock, 8 kHz
26	DCL	I	IOM-2: Data clock, 2048 kHz or 4096 kHz depending on MODE
25	DU	O	IOM-2: Data upstream, open drain output
24	DD	I	IOM-2: Data downstream, input
22	RESET	I	Reset input - forces the device to the default mode, active high
57	MODE	I	IOM-2: Mode Selection
60	TSS0	I	IOM-2: Time slot selection pin 0
59	TSS1	I	IOM-2: Time slot selection pin 1
56	TCK	I	Boundary scan: Test Clock
55	TMS	I	Boundary scan: Test Mode Select
54	TDI	I	Boundary scan: Test Data Input
53	TDO	O	Boundary scan: Test Data Output
28	LGKM0	O	Loop/Ground Key Multiplexing output 0 for channel 1, 2
41	VH12	I/O	Reference voltage for channel 1 and 2, has to be connected via a 220 nF cap. to ground
18,19,20 61,62,63	N.U.I.	I	None Usable Input, tie directly to Digital Ground

Table 1 (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
1,16 17,64	N.U.IO.	I/O	None Usable Input/Output, tie via a Pull-Down-Resistor to Digital Ground
2,3,4,5,7 8,10,12 13,14,15 21	N.C.		not connected

[1] A 100 nF cap. should be used for blocking these pin.

1.3.2 Specific Pins for Channel 1

Table 2

Pin No.	Symbol	Input (I) Output (O)	Function
38	GNDA1	I	Ground Analog for channel 1, not internally connected to GNDD or GNDA2 or GNDA (pin 6 and pin 11)
39	VIN1	I	Analog voice (voltage) input for channel 1
37	VOUT1	O	Analog voice (voltage) output for channel 1
31	SI1_0	I	Signaling indication input pin 0 for channel 1
30	SI1_1	I	Signaling indication input pin 1 for channel 1
29	SI1_2	I	Signaling indication input pin 2 for channel 1
36	SO1_0	O	Signaling command output pin 0 for channel 1
35	SO1_1	O	Signaling command output pin 1 for channel 1
34	SO1_2	O	Signaling command output pin 2 for channel 1
33	SB1_0	I/O	Bi-directional signal. Command indication pin 0 for channel 1
32	SB1_1	I/O	Bi-directional signal. Command indication pin 1 for channel 1

1.3.3 Specific Pins for Channel 2

Table 3

Pin No.	Symbol	Input (I) Output (O)	Function
43	GNDA2	I	Ground Analog for channel 2, not internally connected to GNDD or GNDA1 or GNDA (pin 6 and pin 11)
42	VIN2	I	Analog voice (voltage) input for channel 2
44	VOUT2	O	Analog voice (voltage) output for channel 2
50	SI2_0	I	Signaling indication input pin 0 for channel 2
51	SI2_1	I	Signaling indication input pin 1 for channel 2
52	SI2_2	I	Signaling indication input pin 2 for channel 2
45	SO2_0	O	Signaling command output pin 0 for channel 2
46	SO2_1	O	Signaling command output pin 1 for channel 2
47	SO2_2	O	Signaling command output pin 2 for channel 2
48	SB2_0	I/O	Bi-directional signal. command indication pin 0 for channel 2
49	SB2_1	I/O	Bi-directional signal. command indication pin 1 for channel 2

2 IOM®-2 – SICOFI®-2 Principles

The change from 2 µm to 1 µm CMOS process requires new concepts in the realization of the analog functions. High performance (in the terms of gain, speed, stability …) 1 µm CMOS devices can not withstand more than 5.5 V of supply voltage. On that account the negative supply voltage V_{SS} of the previous SICOFIs will be omitted. This is a benefit for the user but it makes a very high demand on the analog circuitry.

ADC and DAC are changed to Sigma-Delta-concepts to fulfill the stringent requirements on the dynamic parameters.

Using 1 µm CMOS does not only lend to problems – it is the only acceptable solution in terms of area and power consumption for the integration of more then two SICOFI channels on a single chip.

It is rather pointless to implement 2 codec-filter-channels on one chip with pure analog circuitry. The use of a DSP-concept (the SICOFI and the SICOFI-2-approach) for this function seems to be a must for an adequate two channel architecture.

2.1 IOM®-2 – SICOFI®-2 Signal Flow Graph (for either channel)

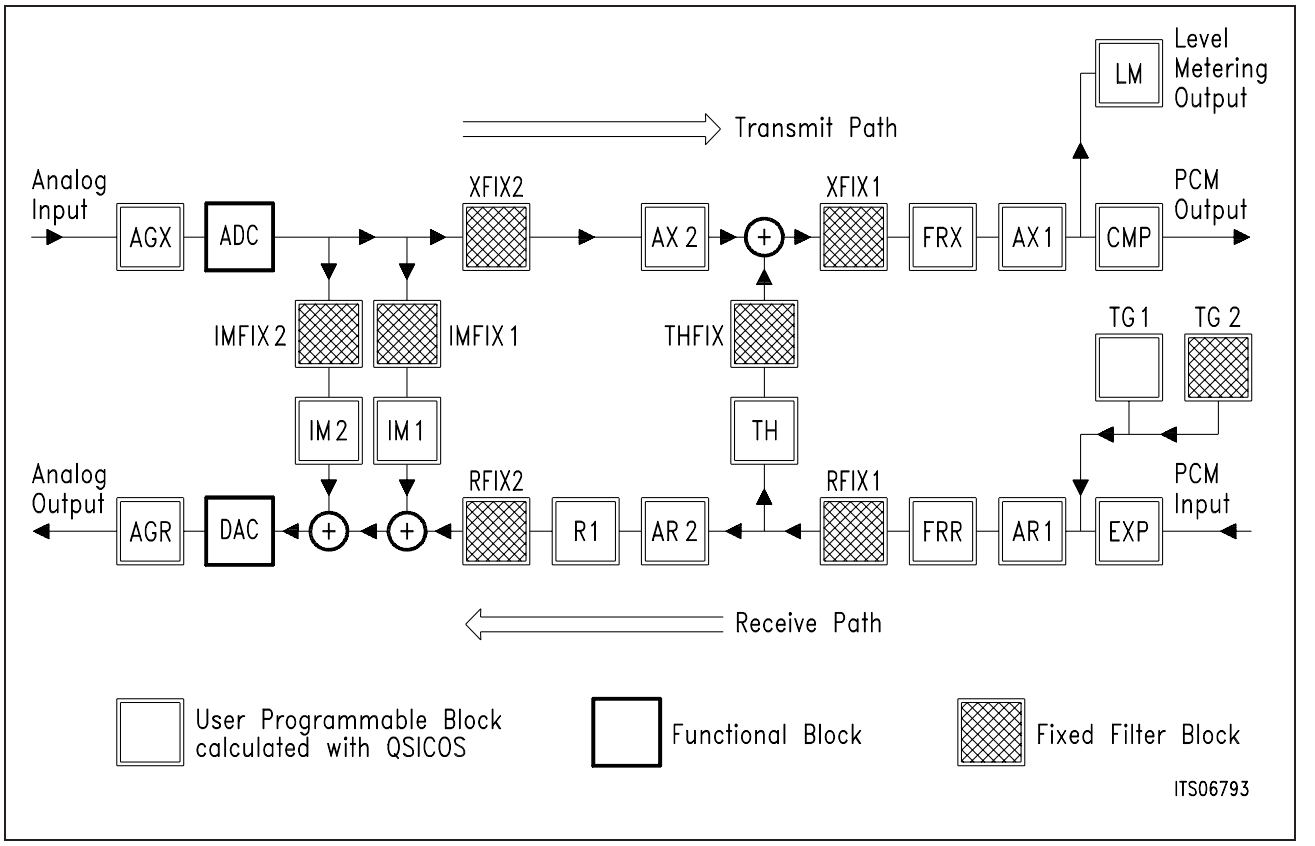


Figure 2

2.1.1 Transmit Path

The analog input signal has to be DC-free connected by an external capacitor because there is an internal virtual reference ground potential. After passing a simple antialiasing prefilter (PREFI) the voice signal is converted to a 1-bit digital data stream in the Sigma-Delta-converter. The first downsampling steps are done in fast running digital hardware filters. The following steps are implemented in the micro-code which has to be executed by the central Digital Signal Processor. This DSP-machine is able to handle the workload for all two channels. At the end the fully processed signal (flexibly programmed in many parameters) is transferred to the IOM-2 interface in a PCM-compressed signal representation.

2.1.2 Receive Path

The digital input signal is received via the IOM-2 interface. Expansion, PCM-law-pass-filtering, gain correction and frequency response correction are the next steps which are done by the DSP-machine. The upsampling interpolation steps are again processed by fast hardware structures to reduce the DSP-workload. The upsampled 1-bit data stream is then converted to an analog equivalent which is smoothed by a POST-Filter (POFI). As the signal VOUT is also referenced to an internal virtual ground potential, an external capacitor is required for DC-decoupling.

2.1.3 Loops

There are two loops implemented. The first is to generate the AC-input impedance (IM) and the second is to perform a proper hybrid balancing (TH). A simple extra path IM2 (from the transmit to the receive path) supports the impedance matching function.

2.1.4 Test Features

There are four analog and five digital test loops implemented in the IOM-2 – SICOFI-2. For special tests it is possible to “Cut Off” the receive and the transmit path at two different points.

2.2 IOM®-2 – SICOFI®-2 Block Diagram

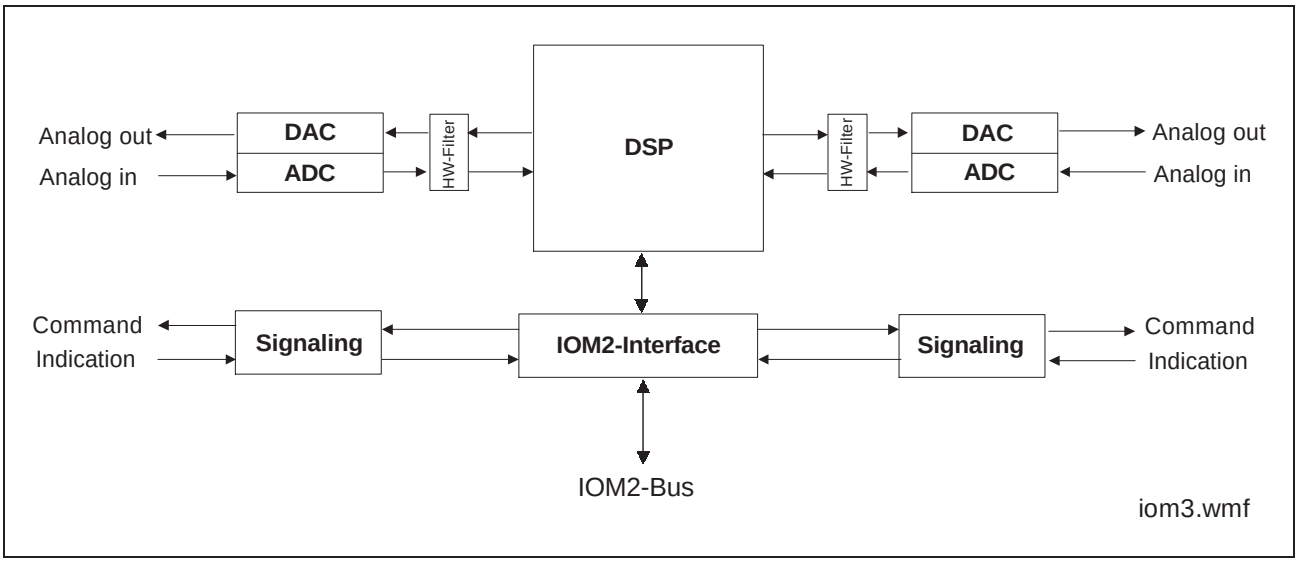


Figure 3

The IOM-2 – SICOFI-2 bridges the gap between analog and digital voice signal transmission in modern telecommunication systems. High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) provide the required conversion accuracy. Analog antialiasing prefilters (PREFI) and smoothing postfilters (POFI) are included. The connection between the ADC and the DAC (with high sampling rate) and the DSP, is done by specific Hardware Filters, for filtering like interpolation and decimation. The dedicated Digital Signal Processor (DSP) handles all the algorithms necessary e.g. for PCM bandpass filtering, sample rate conversion and PCM companding. The IOM-2 Interface handles digital voice transmission, IOM-2 – SICOFI-2 feature control and transparent access to the IOM-2 – SICOFI-2 command and indication pins. To program the filters, precalculated sets of coefficients are downloaded from the system to the on chip coefficient ram (CRAM).

2.3 IOM®-2 Interface

The IOM-2 Interface consists of two data lines and two clock lines. DU (data upstream) carries data from the IOM-2 – SICOFI-2 to a master device. This master device performs the interface between the PCM-backplane, the µController and up to 24 IOM-2 – SICOFI-2's. DD (data downstream) carries data from the master device to the IOM-2-SICOF-2. A frame synchronization clock signal (8 kHz, FSC) as well as a data clock signal (2048 kHz or 4096 kHz DCL) has to be supplied to the IOM-2 – SICOFI-2. The IOM-2 – SICOFI-2 handles data as described in the IOM-2 specification for analog devices.

2.3.1 IOM®-2 Interface Timing for 16 voice channels (per 8 kHz frame)

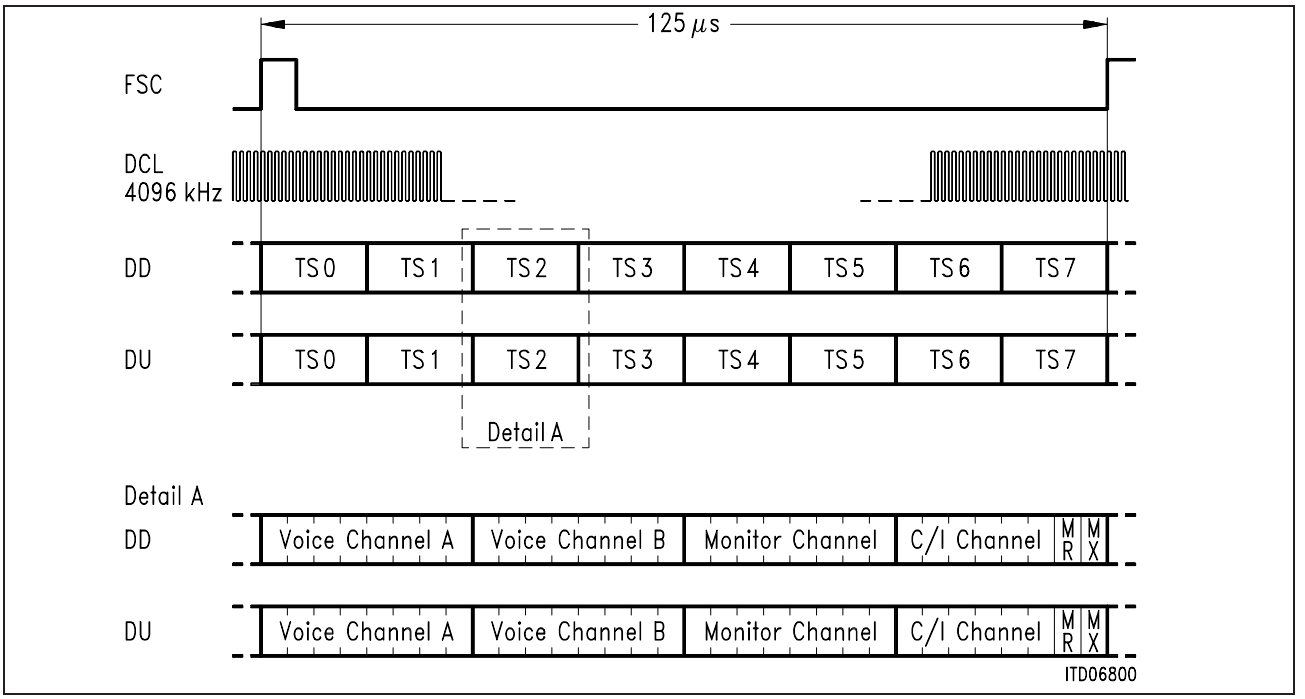


Figure 4

2.3.2 IOM®-2 Interface Timing (DCL = 4096 kHz, MODE = 1, per 8 kHz frame)

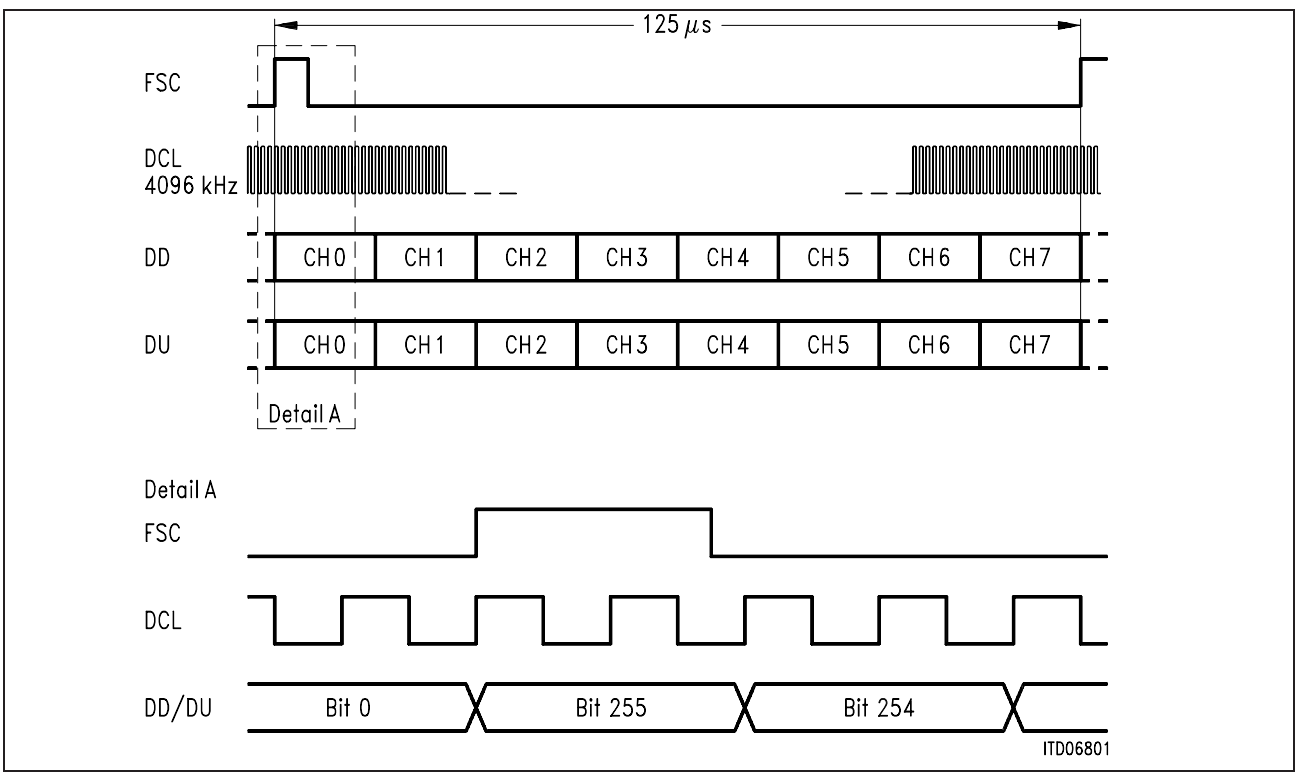


Figure 5

2.3.3 IOM®-2 Interface Timing (DCL = 2048 kHz, MODE = 0)

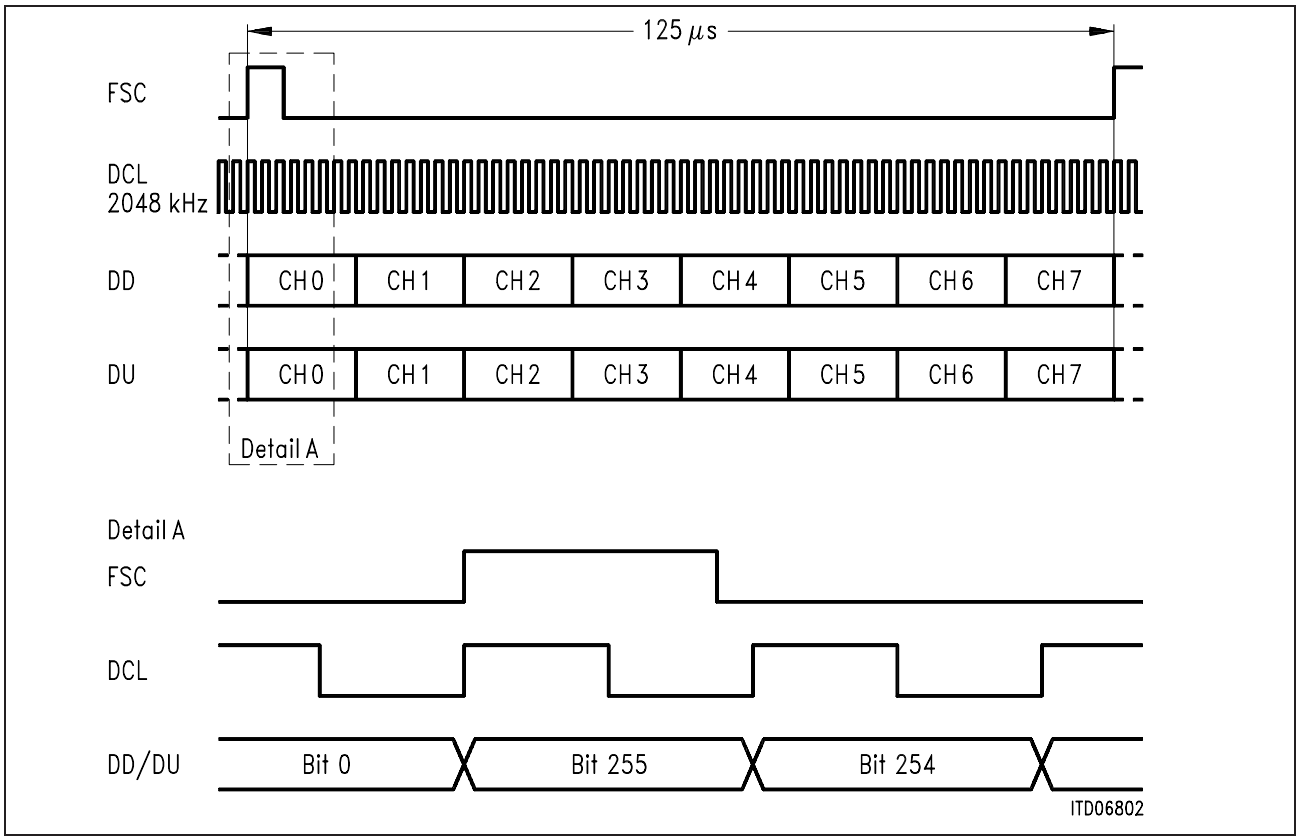


Figure 6

2.3.4 IOM®-2 Time Slot Selection

The two channels (1 and 2) of the IOM-2 – SICOFI-2 can be assigned to 4 time slots by pin-strapping the pins TSS0 and TSS1 (TS0, TS2, TS4, TS6). The IOM-2 operating mode is selected by the MODE pin.

Table 4

TSS1	TSS0	MODE	IOM®-2 Operating Mode
0	0	1	Time slot 0; DCL= 4096 kHz
0	1	1	Time slot 2; DCL= 4096 kHz
1	0	1	Time slot 4; DCL= 4096 kHz
1	1	1	Time slot 6; DCL= 4096 kHz
0	0	0	Time slot 0; DCL= 2048 kHz
0	1	0	Time slot 2; DCL= 2048 kHz
1	0	0	Time slot 4; DCL= 2048 kHz
1	1	0	Time slot 6; DCL= 2048 kHz

Each IOM time slot contains 2 voice channels (A and B). Those two voice channels share a common IOM-Monitor-byte as well as a common C/I-byte. The AD-bit in the Monitor command defines which of the two voice channels should be affected (programmed). (For more information on IOM-2 specific Monitor Channel Data Structure see appendix, **page 64**).

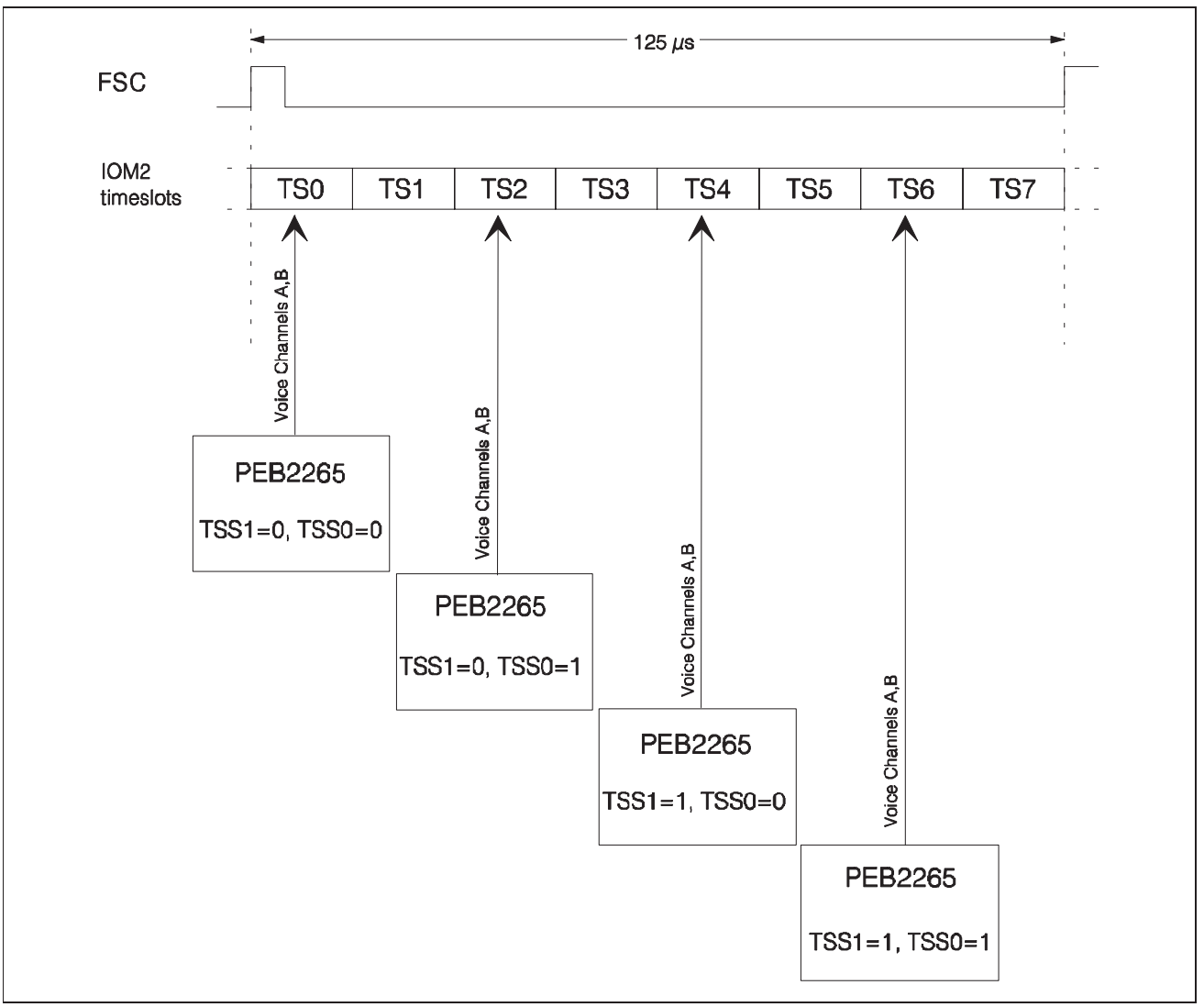


Figure 7

Table 5

	TSS1 = 0, TSS0 = 0		TSS1 = 0, TSS0 = 1		TSS1 = 1, TSS0 = 0		TSS1 = 1, TSS0 = 1	
IOM®-2 – SICOFI®-2 Channels	**TS**	**Voice Channel**	**TS**	**Voice Channel**	**TS**	**Voice Channel**	**TS**	**Voice Channel**
1	TS0	A	TS2	A	TS4	A	TS6	A
2	TS0	B	TS2	B	TS4	B	TS6	B

3 Programming the IOM®-2 – SICOFI®-2

With the appropriate commands, the IOM-2 – SICOFI-2 can be programmed and verified very flexibly via the IOM-2 Interface monitor channel.

Data transfer to the IOM-2 – SICOFI-2 starts with a SICOFI-specific address byte (81_H). With the second byte one of 3 different types of commands (SOP, XOP and COP) is selected. Each of those can be used as a write or read command. Due to the extended IOM-2 – SICOFI-2 feature control facilities, SOP, COP and XOP commands contain additional information (e.g. number of subsequent bytes) for programming (write) and verifying (read) the IOM-2 – SICOFI-2 status.

A write command is followed by up to 8 bytes of data. The IOM-2 – SICOFI-2 responds to a read command with its IOM-2 specific address and the requested information, that is up to 8 bytes of data (see programming Procedure, **page 18**).

Attention: Each byte on the monitor channel, has to be sent twice at least, according to the IOM-2 Monitor handshake procedure (For more information on IOM-2 specific Monitor Channel Data Structure see appendix, **page 64**).

3.1 Types of Monitor Bytes

The 8-bit Monitor Bytes have to be interpreted as either commands or status information stored in Configuration Registers or the Coefficient RAM. There are three different types of IOM-2 – SICOFI-2 commands which are selected by bit 3 and 4 as shown below.

SOP **STATUS OPERATION:** IOM-2 – SICOFI-2 status setting/monitoring

Bit	7	6	5	4	3	2	1	0
				1	0			

XOP **EXTENDED OPERATIO:** C/I channel configuration/evaluation

Bit	7	6	5	4	3	2	1	0
	X			1	1			

COP **COEFFICIENT OPERATION:** filter coefficient setting/monitoring

Bit	7	6	5	4	3	2	1	0
				0				

Storage of Programming Information:

4 configuration registers per channel:	CR1, CR2, CR3, CR4 accessed by SOP commands
4 common configuration registers:	XR1, XR2, XR3 and XR4 accessed by XOP commands (the contents are valid for two voice channels i.e. 1 IOM-2 time slot)
1 coefficient RAM per channel:	CRAM accessed by COP commands

3.2 IOM®-2 – SICOFI®-2 Commands

3.2.1 SOP - Write Commands

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
SOP-Write 1 Byte		0		1	0	0	0	1	
CR1	Data								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
Idle								

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
SOP-Write 2 Bytes		0		1	0	0	1	0	
CR2	Data								
CR1	Data								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
Idle								
Idle								0

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
SOP-Write 3 Bytes		0		1	0	0	1	1	
CR3	Data								
CR2	Data								
CR1	Data								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
Idle								
Idle								
Idle								

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
SOP-Write 4 Bytes		0		1	0	1	0	0	
CR4	Data								
CR3	Data								
CR2	Data								
CR1	Data								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
Idle								
Idle								
Idle								
Idle								

3.2.2 XOP - Write Commands

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
XOP-Write 2 Bytes		0		1	1	0	1	0	
XR2	Data								
XR1	Data								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
Idle								
Idle								

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
XOP-Write 3 Bytes		0		1	1	0	1	0	
XR3	Data								
XR2	Data								
XR1	Data								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
Idle								
Idle								
Idle								

3.2.3 COP - Write Commands

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
COP-Write 4 Bytes		0		0	1					Idle								
Coeff. 4	Data									Idle								
Coeff. 3	Data									Idle								
Coeff. 2	Data									Idle								
Coeff. 1	Data									Idle								

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
COP-Write 8 Bytes		0		0	0					Idle								
Coeff. 8	Data									Idle								
Coeff. 7	Data									Idle								
Coeff. 6	Data									Idle								
Coeff. 5	Data									Idle								
Coeff. 4	Data									Idle								
Coeff. 3	Data									Idle								
Coeff. 2	Data									Idle								
Coeff. 1	Data									Idle								

3.2.4 SOP - Read Commands

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
SOP-Read 1 Byte		1		1	0	0	0	1	
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
1	0	0	0	0	0	0	1	Address
Data								CR1

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
SOP-Read 2 Bytes		1		1	0	0	1	0	
	Idle								
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
1	0	0	0	0	0	0	1	Address
Data								CR2
Data								CR1

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
SOP-Read 3 Bytes		1		1	0	0	1	1	
	Idle								
	Idle								
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
1	0	0	0	0	0	0	1	Address
Data								CR3
Data								CR2
Data								CR1

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
SOP-Read 4 Bytes		1		1	0	1	0	0	
	Idle								
	Idle								
	Idle								
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
1	0	0	0	0	0	0	1	Address
Data								CR4
Data								CR3
Data								CR2
Data								CR1

3.2.5 XOP - Read Commands

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
XOP-Read 1 Byte		1		1	1	0	0	1	
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
1	0	0	0	0	0	0	1	Address
Data								XR1

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
XOP-Read 2 Bytes		1		1	1	0	1	0	
	Idle								
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
1	0	0	0	0	0	0	1	Address
Data								XR2
Data								XR1

DD	7	6	5	4	3	2	1	0	Bit
Address	1	0	0	0	0	0	0	1	
XOP-Read 3 Bytes		1		1	1	0	1	1	
	Idle								
	Idle								
	Idle								
	Idle								

7	6	5	4	3	2	1	0	DU
Idle								
Idle								
1	0	0	0	0	0	0	1	Address
Data								XR3
Data								XR2
Data								XR1

3.2.6 COP - Read Commands

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
COP-Read 4 bytes		1		0	1					Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle									Data								Coeff.4
	Idle									Data								Coeff.3
	Idle									Data								Coeff.2
	Idle									Data								Coeff.1

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
COP-Read 8 Bytes		1		0	0					Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle									Data								Coeff.8
	Idle									Data								Coeff.7
	Idle									Data								Coeff.6
	Idle									Data								Coeff.5
	Idle									Data								Coeff.4
	Idle									Data								Coeff.3
	Idle									Data								Coeff.2
	Idle									Data								Coeff.1

3.2.7 Example for a Mixed Command

DD	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DU
Address	1	0	0	0	0	0	0	1		Idle								
SOP-Write 4 Bytes		0		1	0	1	0	0		Idle								
CR4	Data									Idle								
CR3	Data									Idle								
CR2	Data									Idle								
CR1	Data									Idle								
XOP-Write 2 Bytes		0		1	1	0	1	0		Idle								
XR2	Data									Idle								
XR1	Data									Idle								
COP-Write 4 Bytes		0		0	1					Idle								
Coeff. 4	Data									Idle								
Coeff. 3	Data									Idle								
Coeff. 2	Data									Idle								
Coeff. 1	Data									Idle								
SOP-Read 3 Bytes		1		1	0	0	1	1		Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle									Data								CR3
	Idle									Data								CR2
	Idle									Data								CR1
Address	1	0	0	0	0	0	0	1		Idle								
COP-Read 4 Bytes		1		0	1					Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle									Data								Coeff.4
	Idle									Data								Coeff.3
	Idle									Data								Coeff.2
	Idle									Data								Coeff.1
Address	1	0	0	0	0	0	0	1		Idle								
XOP-Read 1 Byte		1		1	1	0	0	1		Idle								
	Idle									1	0	0	0	0	0	0	1	Address
	Idle									Data								XR1

3.3 SOP Command

To modify or evaluate the IOM-2 – SICOFI-2IOM-2 – SICOFI-2 status, the contents of up to four configuration registers CR1, CR2, CR3 and CR4 may be transferred to or from the IOM-2 – SICOFI-2. This is started by a SOP-Command (status operation command).

Bit	7	6	5	4	3	2	1	0
	AD	RW	PWRUP	1	0	LSEL2	LSEL1	LSEL0

AD Address Information
- AD = 0 IOM-2 – SICOFI-2 channel 1 is addressed with this cmd.
- AD = 1 IOM-2 – SICOFI-2 channel 2 is addressed with this cmd.

RW Read/Write Information: Enables reading from the IOM-2 – SICOFI-2 or writing information to the IOM-2 – SICOFI-2
- RW = 0 Write to IOM-2 – SICOFI-2
- RW = 1 Read from IOM-2 – SICOFI-2

PWRUP Power Up / Power Down
- PWRUP = 1 sets the assigned channel (see bit AD) of IOM-2 – SICOFI-2 to power-up (operating mode)
- PWRUP = 0 resets the assigned channel of IOM-2 – SICOFI-2 to power-down (standby mode)

LSEL Length select information (see also programming procedure)
This field identifies the number of subsequent data bytes
- LSEL = 000 0 bytes of data are following
- LSEL = 001 1 byte of data is following (CR1)
- LSEL = 010 2 bytes of data are following (CR2, CR1)
- LSEL = 011 3 bytes of data are following (CR3, CR2, CR1)
- LSEL = 100 4 bytes of data are following (CR4, CR3, CR2, CR1)

All other codes are reserved for future use!

It is possible to program each configuration register separately, just by putting only one byte into the FIFO of the upstream master device (e.g. EPIC), and aborting after transmission of one (or n) byte.

3.3.1 CR1 Configuration Register 1

Configuration register CR1 defines the basic IOM-2 – SICOFI-2 settings, which are: enabling/disabling the programmable digital filters and tone generators.

Bit	7	6	5	4	3	2	1	0
	TH	IM/R1	FRX	FRR	AX	AR	ETG2	ETG1

TH Enable TH- (Trans Hybrid Balancing) Filter
- TH = 0: TH-filter disabled
- TH = 1: TH-filter enabled

IM/R1 Enable IM-(Impedance Matching) Filter and R1-Filter
- IM/R1 = 0: IM-filter and R1-filter disabled
- IM/R1 = 1: IM-filter and R1-filter enabled

FRX Enable FRX (Frequency Response Transmit)-Filter
- FRX = 0: FRX-filter disabled
- FRX = 1: FRX-filter enabled

FRR Enable FRR (Frequency Response Receive)-Filter
- FRR = 0: FRR-filter disabled
- FRR = 1: FRR-filter enabled

AX Enable AX-(Amplification/Attenuation Transmit) Filter
- AX = 0: AX-filter disabled
- AX = 1: AX-filter enabled

AR Enable AR-(Amplification/Attenuation Receive) Filter
- AR = 0: AR-filter disabled
- AR = 1: AR-filter enabled

ETG2 Enable programmable tone generator 2[1)]
- ETG2 = 0: programmable tone generator 2 is disabled
- ETG2 = 1: programmable tone generator 2 is enabled

ETG1 Enable programmable tone generator 1
- ETG1 = 0: programmable tone generator 1 is disabled
- ETG1 = 1: programmable tone generator 1 is enabled

1) Tone generator 2 is not available if Level Metering Function is enabled!

3.3.2 CR2 Configuration Register 2

Bit	7	6	5	4	3	2	1	0
	TH-Sel		LM	LMR	LAW	LIN	PTG2	PTG1

TH-Sel 2 bit field to select one of two programmed TH-filter coefficient sets
TH-Sel = 0 0: TH-filter coefficient set 1 is selected
TH-Sel = 0 1: TH-filter coefficient set 2 is selected

LM Level Metering function[1)]
LM = 0: level metering function is disabled
LM = 1: level metering function is enabled

LMR Result of Level Metering function (this bit can not be written)
LMR = 0: level detected was lower than the reference
LMR = 1: level detected was higher than the reference

LAW PCM - law selection
LAW = 0: A-Law is selected
LAW = 1: µ-Law (µ255 PCM) is selected

LIN Linear mode selection
LIN = 0: PCM-mode is selected
LIN = 1: linear mode is selected[2)]

PTG2 User programmed frequency or fixed frequency is selected
PTG2 = 0: fixed frequency for tone generator 2 is selected (1 kHz)
PTG2 = 1: programmed frequency for tone generator 2 is selected

PTG1 User programmed frequency or fixed frequency is selected
PTG1 = 0: fixed frequency for tone generator 1 is selected (1 kHz)
PTG1 = 1: programmed frequency for tone generator 1 is selected

1) Explanation of the level metering function:
A signal fed to A/µ-Law compression via AX- and HPX-filters (from a digital loop, or externally via VIN), is rectified, and the power is measured. If the power exceeds a certain value, loaded to XR4, bit LMR is set to '1'. The power of the incoming signal can be adjusted by AX-filters.

2) During Linear operation only one 16 bit voice channel, is available per time slot. Depending on the address bit (AD) the voice-data of channel 1 or 2 is transmitted. The other voice channel is not available during this time.

3.3.3 CR3 Configuration Register 3

Bit	7	6	5	4	3	2	1	0
	COT/R			0	IDR	Version		

COT/R Selection of Cut Off Transmit/Receive Paths

0 0 0:	Normal Operation	
0 0 1:	COT_16K	Cut Off Transmit Path at 16 kHz (input of TH-Filter)
0 1 0:	COT_PCM	Cut Off Transmit Path at 8 kHz (input of compression) (output is zero for µ-law and linear mode, 1 LSB for A-law)
1 0 1:	COR_PFI	Cut Off Receive Path at 4 MHz (POFI-output)
1 1 0:	COR_64K	Cut Off Receive Path at 64 kHz (IM-filter input)

IDR Initialize Data RAM

IDR = 0:	Normal operation is selected
IDR = 1:	Contents of Data RAM is set to 0
	(used for production test purposes)

Version The Version number shows the actual design version of IOM-2-SICOFI-2 (100 for PEB 2265 V1.1)

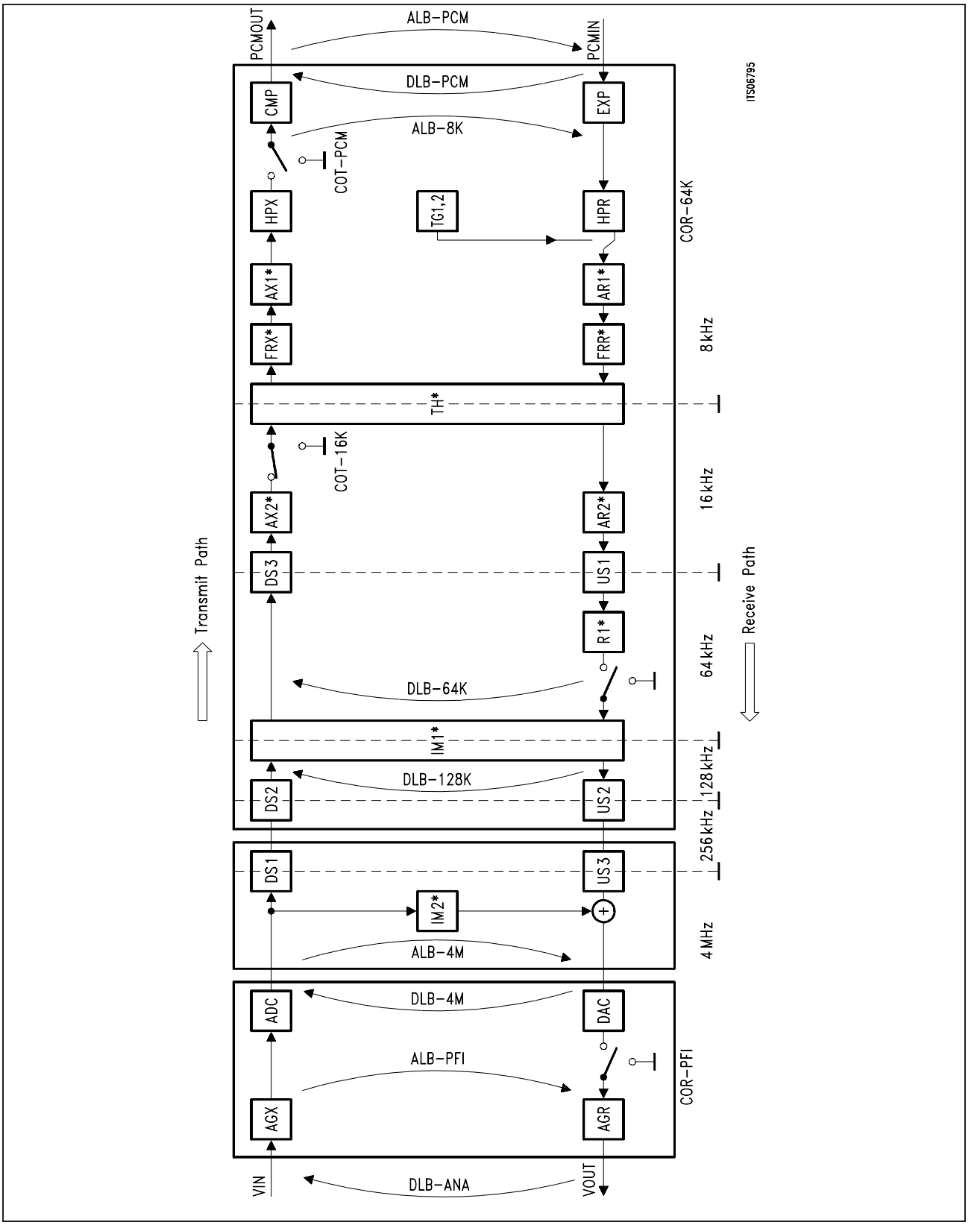


Figure 8
CUT OFF‘s’ and Loops

3.3.4 CR4 Configuration Register 4

Bit	7	6	5	4	3	2	1	0
	Test-Loops				AGX	AGR	D-HPX	D-HPR

Test-Loops 4 bit field for selection of Analog and Digital Loop Backs

0 0 0 0:		no loop back is selected (normal operation)
0 0 0 1:	ALB-PFI	analog loop back via PREFI-POFI is selected
0 0 1 1:	ALB-4M	analog loop back via 4 MHz is selected
0 1 0 0:	ALB-PCM	analog loop back via 8 kHz (PCM) is selected
0 1 0 1:	ALB-8K	analog loop back via 8 kHz (linear) is selected
1 0 0 0:	DLB-ANA	digital loop back via analog port is selected
1 0 0 1:	DLB-4M	digital loop back via 4 MHz is selected
1 1 0 0:	DLB-128K	digital loop back via 128 kHz is selected
1 1 0 1:	DLB-64K	digital loop back via 64 kHz is selected
1 1 1 1:	DLB-PCM	digital loop back via PCM-registers is selected

AGX Analog gain in transmit direction

AGX = 0: analog gain is disabled

AGX = 1: analog gain is enabled (6,02dB amplification)

AGR Analog gain in receive direction

AGR = 0: analog gain is disabled

AGR = 1: analog gain is enabled (6,02dB attenuation)

D-HPX Disable highpass in transmit direction

D-HPX = 0: transmit high pass is enabled

D-HPX = 1: transmit high pass is disabled [1)]

D-HPR Disable highpass in receive direction

D-HPR = 0: receive high pass is enabled

D-HPR = 1: receive high pass is disabled [2)]

1) In this case the transmit-path signal is attenuated 0.06 dB
2) In this case the receive-path signal is attenuated 0.12 dB

3.4 COP Command

With a COP Command coefficients for the programmable filters can be written to the IOM-2 – SICOFI-2 Coefficient RAM or read from the Coefficient RAM via the IOM-2 interface for verification

Bit	7	6	5	4	3	2	1	0
	AD	RW	RST	0	CODE3	CODE2	CODE1	CODE0

AD Address
AD = 0 IOM-2 – SICOFI-2 channel 1 is addressed
AD = 1 IOM-2 – SICOFI-2 channel 2 is addressed

RW Read/Write
RW = 0 Subsequent data is written to the IOM-2 – SICOFI-2
RW = 1 Read data from IOM-2 – SICOFI-2

RST Reset
RST = 1 Reset IOM-2 – SICOFI-2
(same as RESET-Pin, valid for all two channels)

CODE includes number of following bytes and filter-address

0	0	0	0	TH-Filter coefficients (part 1)	(followed by 8 bytes of data)
0	0	0	1	TH-Filter coefficients (part 2)	(followed by 8 bytes of data)
0	0	1	0	TH-Filter coefficients (part3)	(followed by 8 bytes of data)
0	1	0	0	IM-Filter coefficients (part1)	(followed by 8 bytes of data)
0	1	0	1	IM-Filter coefficients (part2)	(followed by 8 bytes of data)
0	1	1	0	FRX-Filter coefficients	(followed by 8 bytes of data)
0	1	1	1	FRR-Filter coefficients	(followed by 8 bytes of data)
1	0	0	0	AX-Filter coefficients	(followed by 4 bytes of data)
1	0	0	1	AR-Filter coefficients	(followed by 4 bytes of data)
1	1	0	0	TG1-Filter coefficients	(followed by 4 bytes of data)
1	1	0	1	TG2-Filter coefficients	(followed by 4 bytes of data)

How to Program the Filter Coefficients

TH-Filter: Two sets of TH-filter coefficients can be loaded to the IOM-2 – SICOFI-2.Each of the two sets can be selected for any of the two IOM-2 – SICOFI-2 channels, by setting the value of TH-SEL in configuration register CR2. Coefficient set 1 is loaded to the IOM-2-SICOFI-2 via channel 1, set 2 is loaded via channel 2.

AX, AR, IM, FRX, FRR-Filter: An individual coefficient set is available for each of the two channels

Tone-Generators: An individual coefficient set is available for each of the two channels

An **independent set** of coefficients is available for all the two channels, for all the filters and Tone-Generators.

Two sets of TH-filter coefficients can be loaded to the IOM-2 – SICOFI-2. Each of the two sets can be selected for any of the two IOM-2 – SICOFI-2 channels, by setting the value of TH-SEL in configuration register CR2. Coefficients set #1 is loaded to the IOM-2-SICOFI-2 via channel 1, set #2 is loaded via channel 2 and so on.

Note: After RESET coefficient set #1 is used for all of the two channels, as all bits in configuration register CR2 are set to '0'.

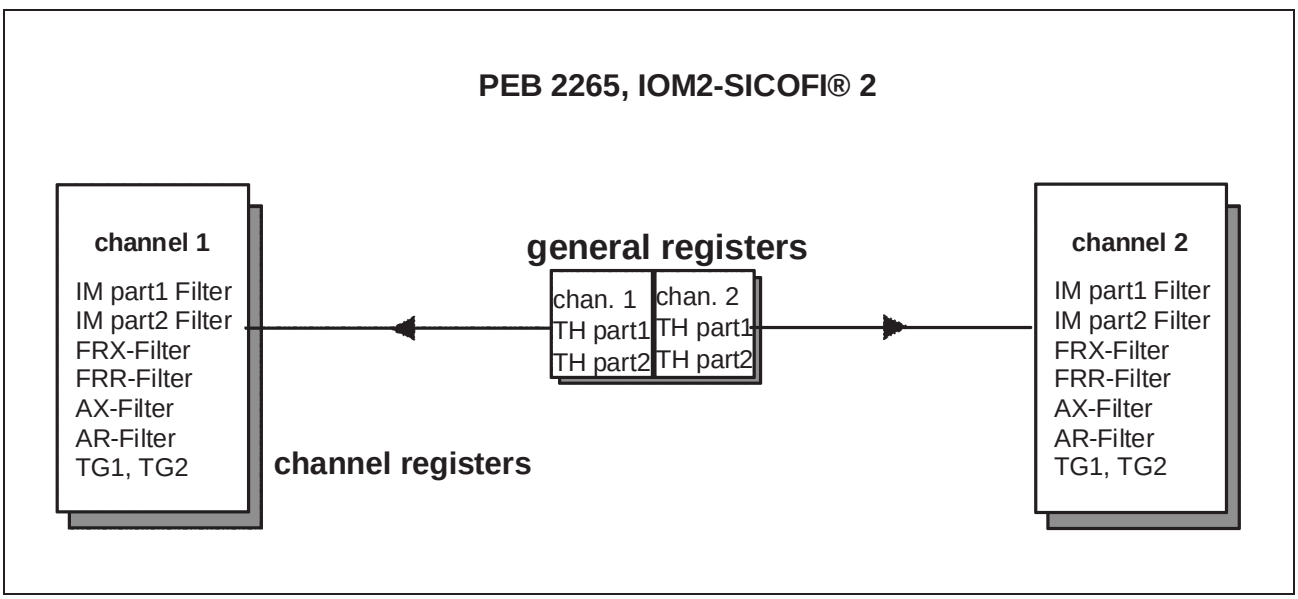


Figure 9

3.5 XOP Command

With the XOP command, the IOM-2 – SICOFI-2 C/I channel in the selected time slot[1] is configured and evaluated.

Bit	7	6	5	4	3	2	1	0
	0	RW	0	1	1	LSEL2	LSEL1	LSEL0

RW Read / Write Information: Enables reading from the IOM-2 – SICOFI-2 or writing information to the IOM-2 – SICOFI-2
RW = 0 Write to IOM-2 – SICOFI-2
RW = 1 Read from IOM-2 – SICOFI-2

LSEL Length select information, for setting the number of subsequent data bytes
LSEL = 000 0 bytes of data are following
LSEL = 001 1 byte of data is following (XR1)
LSEL = 010 2 bytes of data are following (XR2, XR1)
LSEL = 011 3 bytes of data are following (XR3, XR2, XR1)
LSEL = 100 4 bytes of data are following (XR4, XR3, XR2, XR1)

3.5.1 XR1 Extended Register[2]

Bit	7	6	5	4	3	2	1	0
	SB2_1	SB2_0	SI2_0[1]	SI2_0[1]	SB1_1	SB1_0	SI1_0[1]	SI1_0[1]

[1] Bits SI1_0 and SI2_0 have special meaning depending on contents of XR2 (see **page 35**).

SB2_1 status of pin SB2_1 is transferred to the upstream master device
SB2_0 status of pin SB2_0 is transferred to the upstream master device
SI2_0 status of pin SI2_0 is transferred to the upstream master device
SB1_1 status of pin SB1_1 is transferred to the upstream master device
SB1_0 status of pin SB1_0 is transferred to the upstream master device
SI1_0 status of pin SI1 _0 is transferred to the upstream master device

[1] IOM-2 time slot TS0, TS2, TS4 or TS6, by pin-strapping the pins TSS0 and TSS1
[2] Register XR1 can only be read.

3.5.2 XR2 Extended Register 2

Register XR2 configures the data-upstream command/indication channel.

Bit	7	6	5	4	3	2	1	0
	N				T			

Upstream Update Interval N

To restrict the rate of upstream C/I-bit changes, deglitching (persistence checking) of the status information from the SLIC may be applied. New status information will be transmitted upstream, after it has been stable for N milliseconds. N is programmable in the range of 1 to 15 ms in steps of 1 ms, with N = 0 the deglitching is disabled.

Field N				Update Interval Time
0	0	0	0	Deglitching is disabled
0	0	0	1	Upstream transmission after 1 ms
0	0	1	0	Upstream transmission after 2 ms
.	.	.	.	.
.	.	.	.	.
1	1	1	0	Upstream transmission after 14 ms
1	1	1	1	Upstream transmission after 15 ms

Detector Select Sampling Interval T

SLICs with multiplexed loop- and ground-key-status, which have a single status output pin for carrying the loop- and ground-keystatus information, need a special detector select input.

Field T				Time Interval T between Detector selected High States
0	0	0	0	Detector select output LGKM0 is program. To 0 permanently
0	0	0	1	Time interval T is 1 ms
0	0	1	0	Time interval T is 2 ms
.	.	.	.	.
.	.	.	.	.
1	1	1	0	Time interval T is 14 ms
1	1	1	1	Detector select output LGKM0 is program. to 1 permanently

LGKM0 is detector select output for channel 1 and 2.

SLICs with Multiplexed Loop / Ground Key Detect

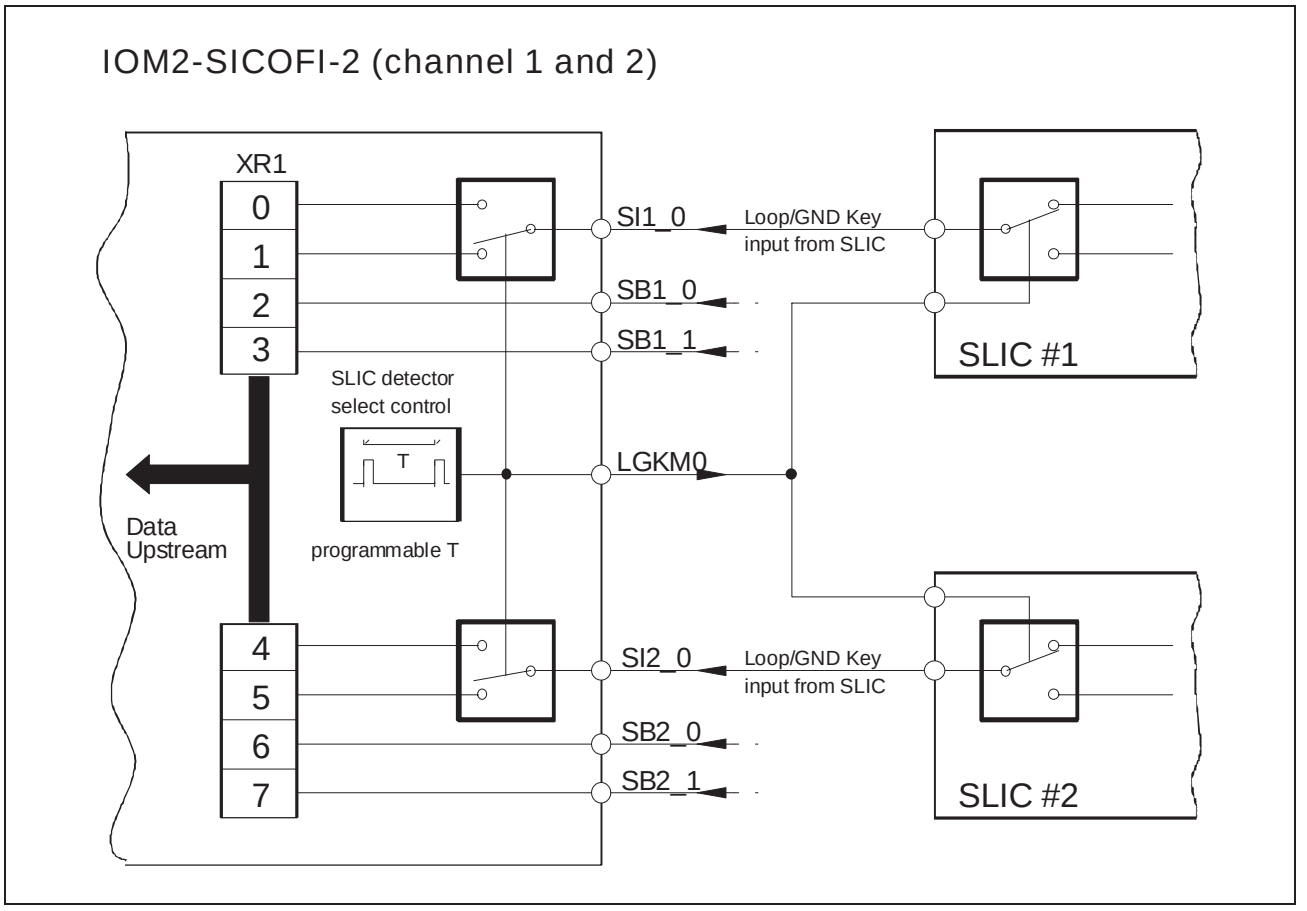


Figure 10

IOM-2 – SICOFI-2 pin LGKM0 is a detector select output. This command output pin are normally set to logical ‘0’, such that the SLIC outputs loop status, which is passed to XR1-bits 0 and 4 via indication pins SI1_0 and SI2_0.

Every T milliseconds, the detector select output change to logical ‘1’ for a time of 125 µs (period FSC). During this time the ground key status is read from the SLIC and transferred upstream using XR1 - bits 1 and 5 via indication pins SIx_0 and SIy_0.

The time interval T is programmable from 1 ms to 14 ms in 1ms steps. It is possible to program the output to be permanently logical ‘0’ or ‘1’.

3.5.3 XR3 Extended Register 3

This register controls the direction of the programmable C/I pins.

Bit	7	6	5	4	3	2	1	0
	PSB2_1	PSB2_0	0	0	PSB1_1	PSB1_0	0	0

PSB2_1 Programmable bi-directional C/I pin SB2_1 is programmed
PSB2_1 = 0: pin SB2_1 is indication input
PSB2_1 = 1: pin SB2_1 is command output

PSB2_0 Programmable bi-directional C/I pin SB2_0 is programmed
PSB2_0 = 0: pin SB2_0 is indication input
PSB2_0 = 1: pin SB2_0 is command output

PSB1_1 Programmable bi-directional C/I pin SB1_1 is programmed
PSB1_1 = 0: pin SB1_1 is indication input
PSB1_1 = 1: pin SB1_1 is command output

PSB1_0 Programmable bi-directional C/I pin SB1_0 is programmed
PSB1_0 = 0: pin SB1_0 is indication input
PSB1_0 = 1: pin SB1_0 is command output

3.5.4 XR4 Extended Register 4

This register holds the offset value for the level metering function. It is only available via the first used time slot.

Bit	7	6	5	4	3	2	1	0
	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

3.6 SLIC Interface

The signaling connection between IOM-2 – SICOFI-2 and a SLIC is performed by the IOM-2 – SICOFI-2 command/indication pins. Data received from the downstream C/I byte are inverted and transferred to command output pins (SB, SO). Data on input pins (SI, SB) are inverted and transferred to the upstream C/I-byte.

3.7 IOM®-2 Interface Command/Indication Byte

The IOM-2 – SICOFI-2 offers a 8 pin parallel command/indication SLIC interface per channel.

Indication Input Pins	SIx_0, SIx_1 SIx_2
Command Output Pins	SOx_0, SOx_1, SOx_2
Program. Command/Indication Pins	SBx_0, SBx_1 (with x: 1 … 4)

Data present at SIx_0, SIx_1, SIx_2 and SBx_0, SBx_1 (if programmed as input) are sampled, inverted and transferred upstream. Data received downstream from IOM-2-interface are latched, inverted and fed to SOx_0, SOx_1, SOx_2 and SBx_0, SBx_1 (if output).

Data-Downstream C/I Channel Byte Format (receive)

The IOM-2 channel contains 6 bits (for two voice channels) in both directions for analog devices like the IOM-2 – SICOFI-2. As the IOM-2 – SICOFI-2 has up to five command output pins per channel (depending on XR3) it is not possible to send commands to all pins at a time. So C/I-channel bit 5 is used as an address bit to select the channel for the command data on C/I-channel bits 4 … 0.

General Case:

Bit	5	4	3	2	1	0
	AD	SBx_1	SBx_0	SOx_2	SOx_1	SOx_0

Example for IOM-2 – SICOFI-2 channels 1 and 2 (IOM-2 time slot 0):

Bit	5	4	3	2	1	0
	1	SB1_1[1)]	SB1_0[1)]	SO1_2	SO1_1	SO1_0

1) If SBx_y is programmed as command output.

Bit	5	4	3	2	1	0
	0	SB2_1[1)]	SB2_0[1)]	SO2_2	SO2_1	SO2_0

Data Upstream C/I Channel Byte Format (transmit)

As the C/I-channel holds only 6 bits for two voice channels and the IOM-2 – SICOFI-2 has up to five indication pins per voice channel, only pins SI1_1 and SI1_2 for voice channel 1, and pins SI2_1 and SI2_2 for voice channel 2 are fed directly to the C/I-channel. Any change at one of the other indication pins (SIx_0, SBx_0 and SBx_1) will generate an interrupt per channel, which is transmitted upstream immediately (C/I-channel bits 2 and 5). Data on those pins is fed to register XR1 and can be evaluated with a XOP-read command.

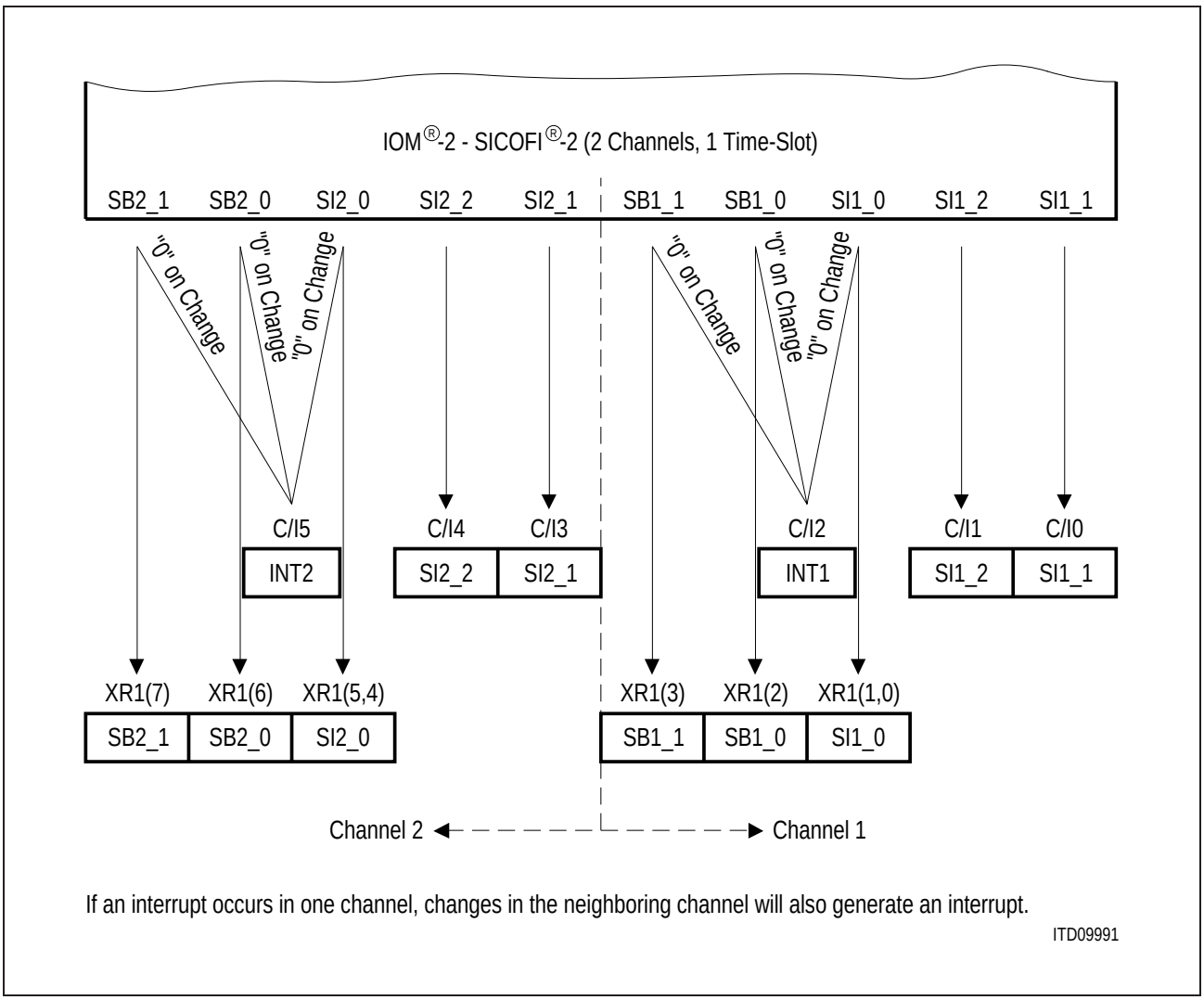


Figure 11

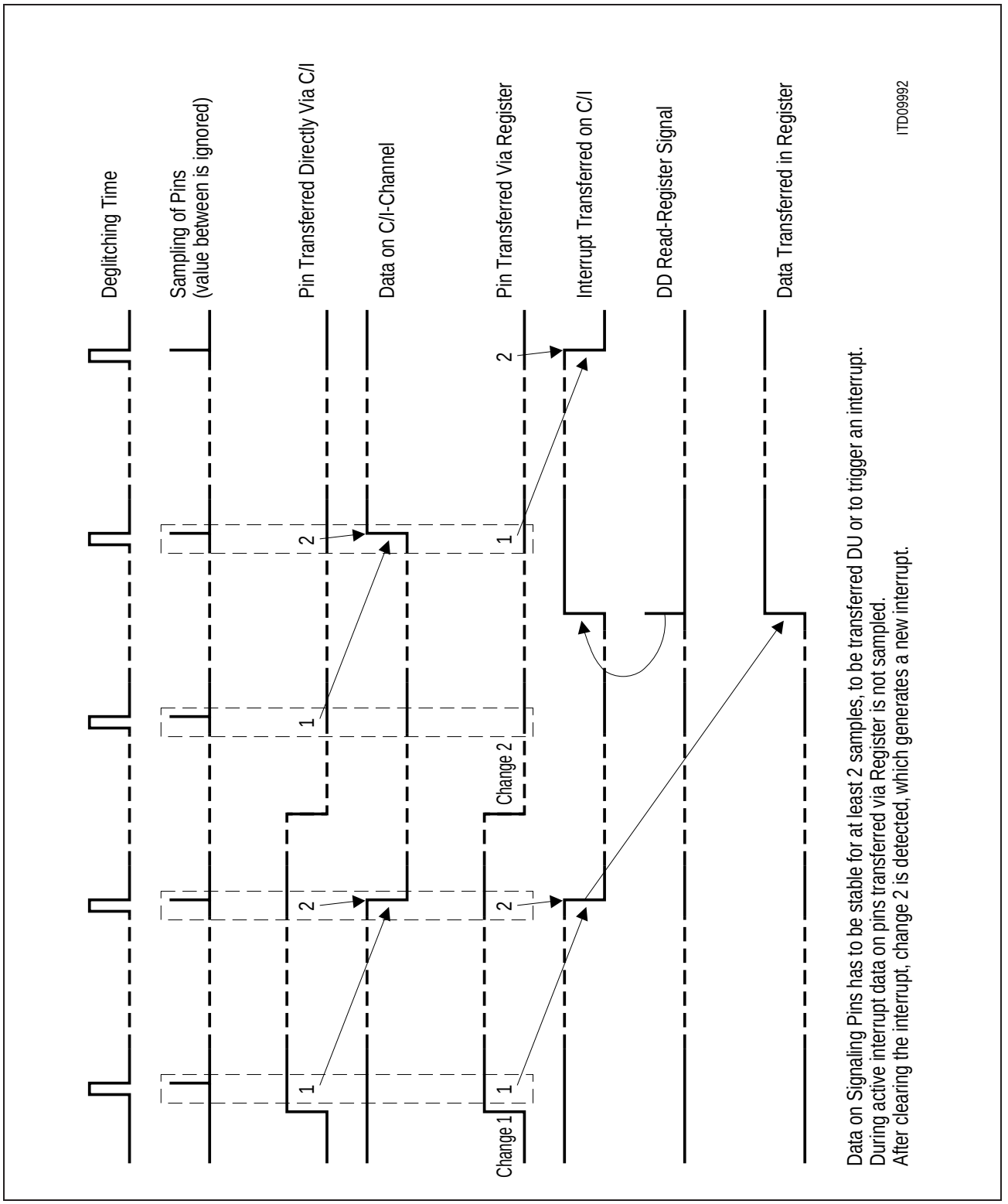


Figure 12
Data Flow

3.8 Operating Modes

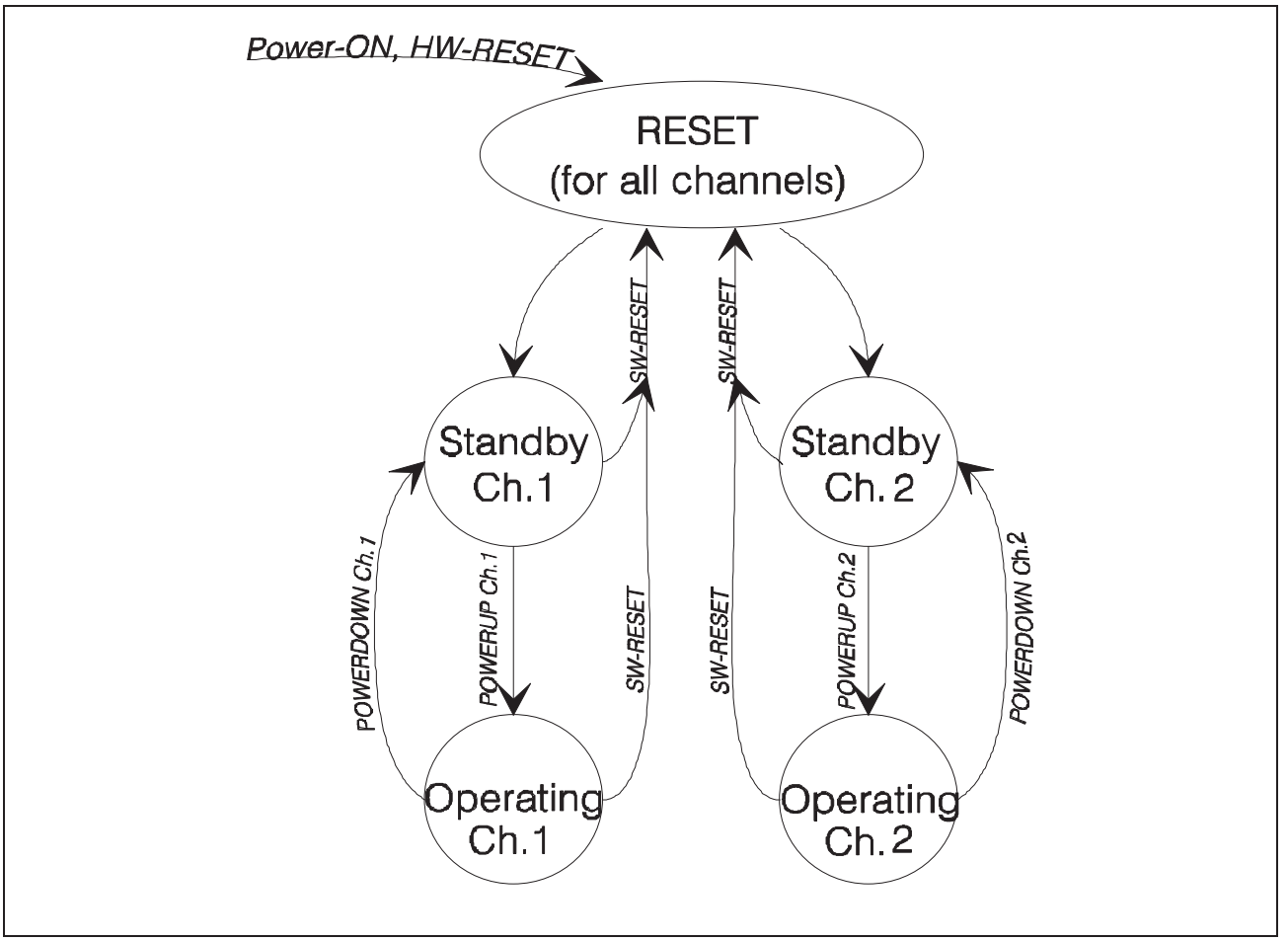


Figure 13

3.8.1 RESET (Basic setting mode)

Upon initial application of V_{DD} or resetting pin RESET to '1' during operation, or by software-reset (see COP command), the IOM-2 – SICOFI-2 enters a basic setting mode. Basic setting means, that the IOM-2 – SICOFI-2 configuration registers CR1q … CR4 and XR1 … XR3 are initialized to '0' for all channels.

All programmable filters are disabled, A-law is chosen, all programmable command/indication pins are inputs. The two tone generators as well as any testmodes are disabled. There is no persistence checking. Receive signaling registers are cleared. DU-pin is in high impedance state, the analog outputs and the signaling outputs are forced to ground.

Table 6

CR1 … CR4	00_H
XR1 … XR4	00_H
Coefficient RAM	Not defined
Command Stack	Cleared
DD-input	Ignored
DU-output	High impedance
VOUT1,2	GNDA1,2
SBx_y	Input
SOx_y	GNDD

If any voltage is applied to any input-pin before initial application of V_{DD}, the IOM-2 – SICOFI-2 may not enter the basic setting mode. In this case it is necessary to reset the IOM-2 – SICOFI-2 or to initialize the IOM-2 – SICOFI-2 configuration registers to ‘0’. The IOM-2 – SICOFI-2 leaves this mode automatically with the beginning of the next 8-kHz frame (RESET-pin is released).

3.8.2 Standby Mode

After releasing the RESET-pin, (RESET-state), beginning with the next 8 kHz frame, the IOM-2 – SICOFI-2 will enter the Standby mode. The IOM-2 – SICOFI-2 is forced to standby mode with the PWRUP bit set to ‘0’ in the SOP command (POWERDOWN). The two channels must be programmed separately. During standby mode the serial IOM-2 – SICOFI-2 IOM-2 interface is ready to receive and transmit commands and data. Received voice data on DD-pin will be ignored. IOM-2 – SICOFI-2 configuration registers and coefficient RAM can be loaded and read back in this mode. Data downstream C/I-channel data is fed to appropriate command pins. Data on indication pins is transmitted data upstream.

Table 7

IOM-2 Voice Channels	‘11111111’ (idle)
VOUT1, 2	GNDA1, 2

3.8.3 Operating Mode

The operating mode for any of the two channels is entered upon recognition of a PWRUP bit set to ‘1’ in a SOP command for the specific channel.

3.9 Programmable Filters

Based on an advanced digital filter concept, the PEB 2265 provides excellent transmission performance and high flexibility. The new filter concept leads to a maximum independence between the different filter blocks.

3.9.1 Impedance Matching Filter

- Realization by 3 different loops
  - 4 MHz: Multiplication by a constant (12 bit)
  - 128 kHz: Wave Digital Filter (IIR) (60 bit)
    improves low frequency response)
  - 64 kHz: FIR-Filter (48 bit)
    (for fine-tuning)
- Improved stability behavior of feedback loops
- Real part of termination impedance positive under all conditions
- Improved overflow performance for transients
- Return loss better 30 dB

3.9.2 Transhybrid Balancing (TH) Filter

- New concept: 2 loops at 16 kHz
- Flexible realization allows optimization of wide impedance range
- Consists of a fixed and a programmable part
  - 2nd order Wave Digital Filter (IIR) (106 bit)
    (improves low frequency response)
  - 7-TAP FIR-Filter (84 bit)
    (for fine-tuning)
- Trans-Hybrid-Loss better 30 dB (typically better 40 dB, device only)
- Adaptation to different lines by:
  - Easy selection between two different downloaded coefficient sets

3.9.3 Filters for Frequency Response Correction

- For line equalization and compensation of attenuation distortion
- Improvement of Group-Delay-Distortion by using minimum phase filters (instead of linear phase filters)
- FRR filter for correction of receive path distortion
  - 5 TAP programmable FIR filter operating at 8 kHz (60 bit)
- FRX filter for correction of transmit path distortion
  - 5 TAP programmable FIR filter operating at 8 kHz (60 bit)
- Frequency response better 0.1 dB

3.9.4 Amplification/Attenuation -Filters AX1, AX2, AR1, AR2

- Improved level adjustment for transmit and receive
- Two separate filters at each direction for
  - Improved trans-hybrid balancing
  - Optimal adjustment of digital dynamic range
  - Gain adjustments independent of TH-filter

3.9.5 Amplification/Attenuation Receive (AR1, AR2)-Filter

Step size for AR-Filter range 3 ... – 14 dB: step size 0.02 ... 0.05 dB
range – 14 ... – 24 dB:step size 0.5 dB

3.9.6 Amplification/Attenuation Transmit (AX1, AX2)-Filter

Step size for AX-Filter range – 3 ... 14 dB: step size 0.02 … 0.05 dB
range 14 ... 24 dB: step size 0.5 dB

4 QSICOS Software

The QSICOS-software has been developed to help to obtain an optimized set of coefficients both quickly and easily. The QSICOS program runs on any PC with at least 575 Kbytes of memory. This also requires MS-DOS Version 5.0 or higher, as well as extended memory.

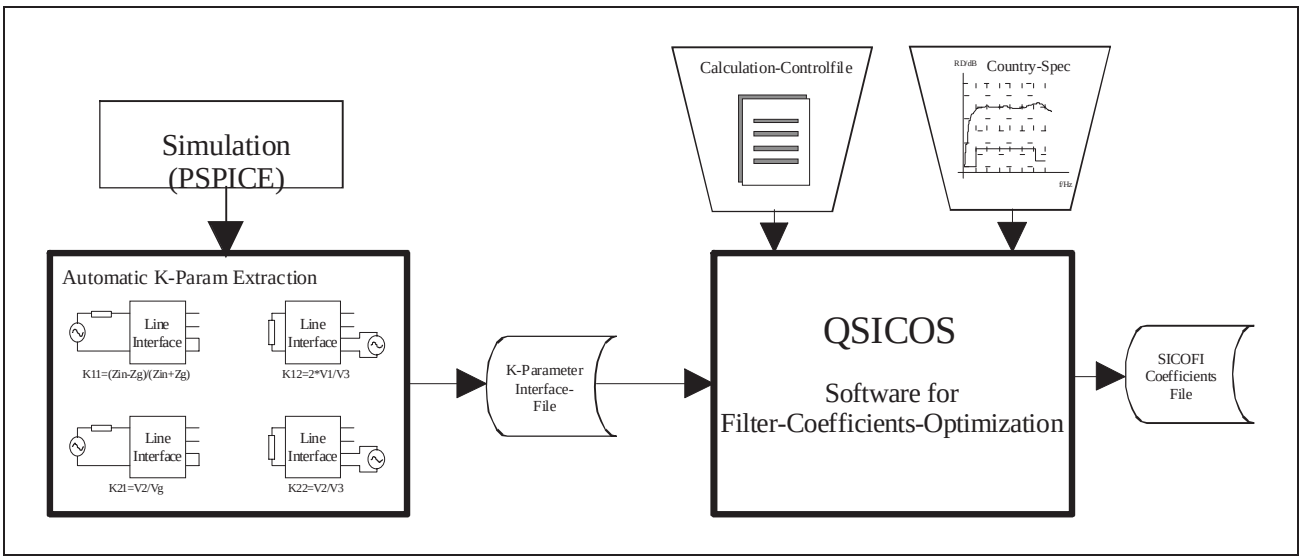


Figure 14

4.1 QSICOS Supports

- **Calculation of coefficients for the**
  - Impedance Filter (IM) for return loss calculation
  - FRR and FRX-Filters for frequency response in receive and transmit path
  - AR1, AR2 and AX1, AX2-Filter for level adjustment in receive and transmit path
  - Trans-Hybrid Balancing Filter (TH) and
  - two programmable tone generators (TG 1 and TG 2)
- **Simulation of the PEB 2265 and SLIC system** with fixed filter coefficients allows simulations of tolerances which may be caused e.g. by discrete external components.
- **Graphical output of transfer functions to the screen** for
  - Return Loss
  - Frequency responses in receive and transmit path
  - Transhybrid Loss
- **Calculation of the PEB 2265 and SLIC system stability**. The IM-Filter of the PEB 2265 adjust the total system impedance by making a feedback loop. Because the line is also a part of the total system, a very robust method has to used to avoid oscillations and to ensure system stability. The input impedance of the PEB 2265 and SLIC combination is calculated. If the real part of the system input impedance is positive, the total system stability can be guaranteed.

5 Transmission Characteristics

The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) needs a complete knowledge of the IOM-2 – SICOFI-2's analog environment, and it is suggested to use the QSICOS-program for calculating the propriate coefficients. Unless otherwise stated, the transmission characteristics are guaranteed within the test conditions.

Test Conditions

T_A = 0 °C to 70 °C; V_{DD} = 5 V ± 5 %; GNDA1 … 4 = GNDD = 0 V
R_L[1]) > 20 kΩ; C_L < 20 pF; H(IM) = H(TH) = 0; H(R1) = H(FRX) = H(FRR) = 1;

HPR and HPX enabled;

AR[2]) = AR1 + AR2 = 0 to – 13 dB for sine-wave-, and
0 to – 11 dB for CCITT-noise-measurements

AX[3]) = AX1 + AX2 = 0 to 13 dB for sine-wave-, and
0 to 11 dB for CCITT-noise-measurements

f = 1014 Hz; 0 dBm0; A-Law or μ-Law;

AGX = 0 dB, 6.02 dB, AGR = 0 dB, – 6.02 dB;

In Transmit direction for μ-law an additional gain of 1.94 dB is implemented automatically, in the companding block (CMP). This additional gain has to be considered at all gain calculations, and reduces possible AX-gain.

A 0dBm04[4]) signal is equivalent to 1.095 [1.0906] Vrms. A +3.14 [3.17] dBm0 signal is equivalent to 1.57 Vrms which corresponds to the overload point of 2.223 V (A-law,[μ-law]).

When the gain in the receive path is set at 0 dB, an 1014 Hz PCM sinewave input with a level 0dBm0 will correspond to a voltage of 1.095 Vrms at A-Law (1,0906 V μ-Law) at the analog output.

When the gain in the transmit path is set at 0 dB, an 1014Hz sine wave signal with a voltage of 1.095 Vrms A-Law (1.0906 V μ-Law) will correspond to a level of 0 dBm0 at the PCM output.

---

1) R_L,C_l forms the load on VOUT
2) Consider, in a complete System,
AR = AR1 + AR2 + FRR + R1 = 0 to – 13 dB (– 11 dB for CCITT-noise-measurement)
3) Consider, in a complete System,
AX = AX1 + AX2 + FRX = 0 to 13 dB (11 dB for CCITT-noise-measurement) for A-Law,
0 to 11 dB (9 dB for CCITT-noise-measurement) for μ-Law
4) The absolute power level in decibels referred to the PCM interface levels.

Table 8

Parameter	Symbol	Limit Values			Unit
		min	typ.	max.	
Gain absolute (AGX = AGR = 0) T_A = 25 °C; V_{DD} = 5 V T_A = 0 – 70 °C; V_{DD} = 5 V ± 5 %	G	 – 0.15 – 0.25	 ± 0.10	 + 0.15 + 0.25	 dB dB
Gain absolute (AGX = 6.02 dB, AGR = – 6.02 dB) T_A = 25 °C; V_{DD} = 5 V T_A = 0 – 70 °C; V_{DD} = 5 V ± 5 %		 – 0.15 – 0.25	 ± 0.10	 + 0.15 + 0.25	 dB dB
Harmonic distortion, 0 dBm0; f = 1000 Hz; 2nd, 3rd order	HD		– 50	– 44	dB
Intermodulation[1)] R_2 R_3	IMD IMD		– 46 – 56		dB dB
Crosstalk 0 dBm0; f = 200 Hz to 3400 Hz any combination of direction and channel	CT		– 85	– 80	dB
Idle channel noise, Transmit, A-law, psophometric V_{IN} = 0 V Transmit, µ-law, C-message V_{IN} = 0 V Receive, A-law, psophometric idle code + 0 Receive, µ-law, C-message idle code + 0	 N_{TP} N_{TC} N_{RP} N_{RC}		 – 85 5	 – 67.4 17.5 – 78.0 12.0	 dBm0p dBmc dBm0p dBmc

1) Using equal-level, 4-tone method (EIA) at a composite level of – 13 dBm0 with frequencies in the range between 300 Hz and 3400 Hz.

5.1 Frequency Response

5.1.1 **Receive:** reference frequency 1 kHz, input signal level 0 dBm0

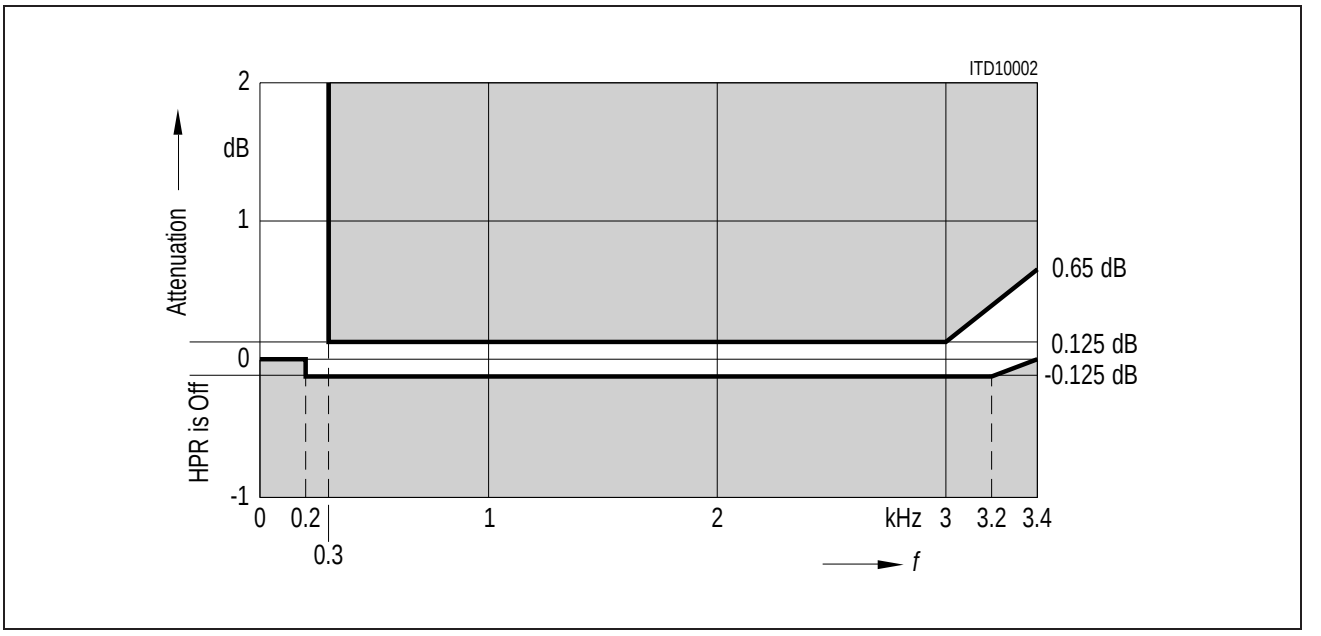


Figure 15

5.1.2 **Transmit:** reference frequency 1 kHz, input signal level 0 dBm0

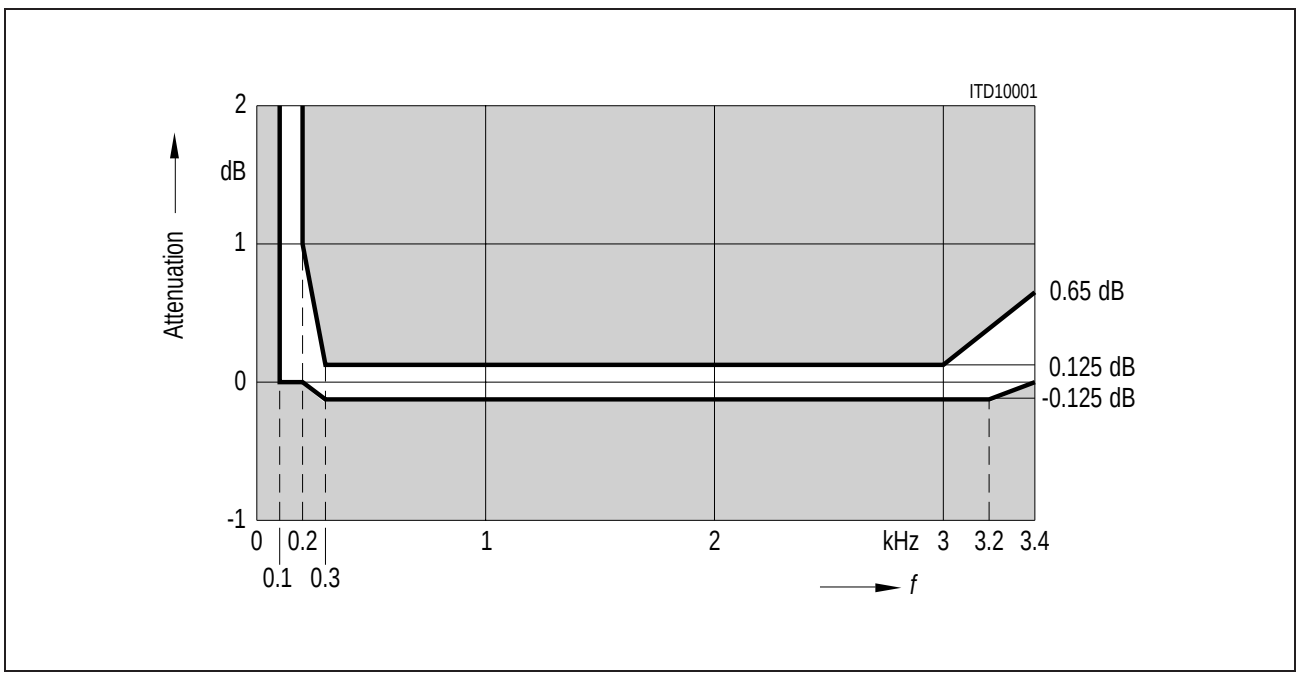


Figure 16

5.2 Group Delay

Maximum delays when the IOM-2 – SICOFI-2 is operating with H(TH) = H(IM) = 0 and H(FRR) = H(FRX) = 1 including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group Delay deviations stay within the limits in the figures below.

5.2.1 Group Delay absolute values: Input signal level 0 dBm0

Table 9

Parameter	Symbol	Limit Values			Unit	Reference
		min.	typ.	max.		
Transmit delay	D_{XA}			300	µs	
Receive delay	D_{RA}			250	µs	

5.2.2 Group Delay Distortion transmit: Input signal level 0 dBm0

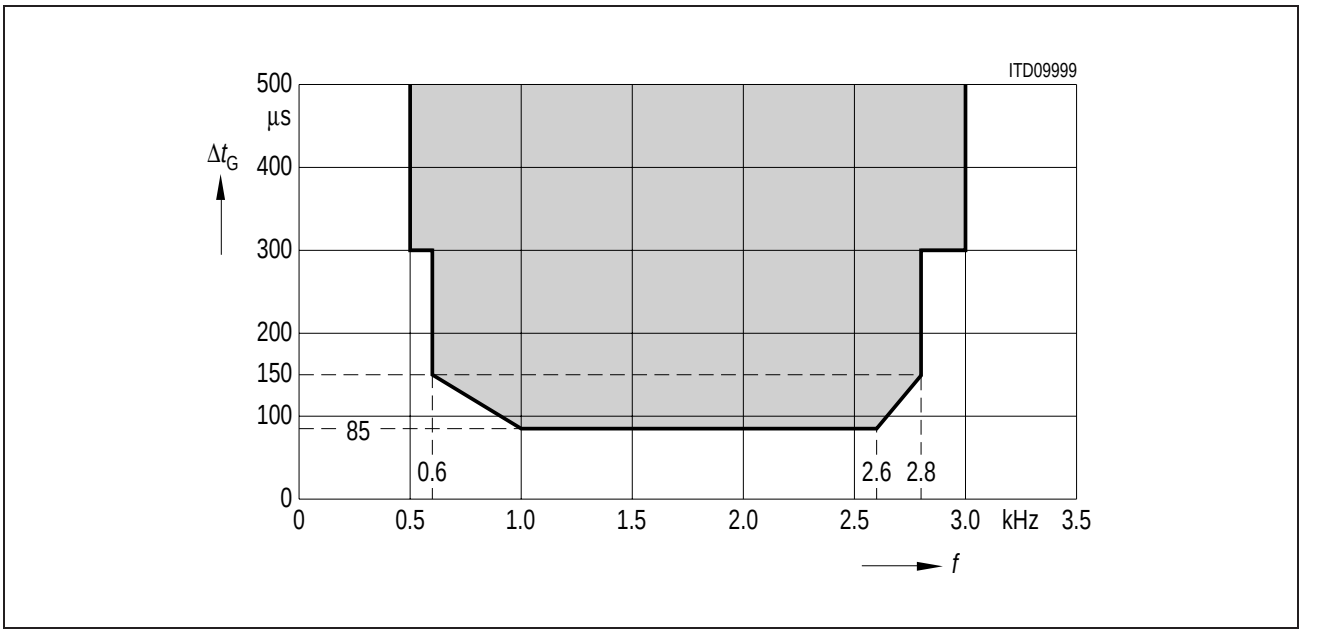


Figure 17

5.2.3 Group Delay Distortion receive: Input signal level 0dBm0[1)]

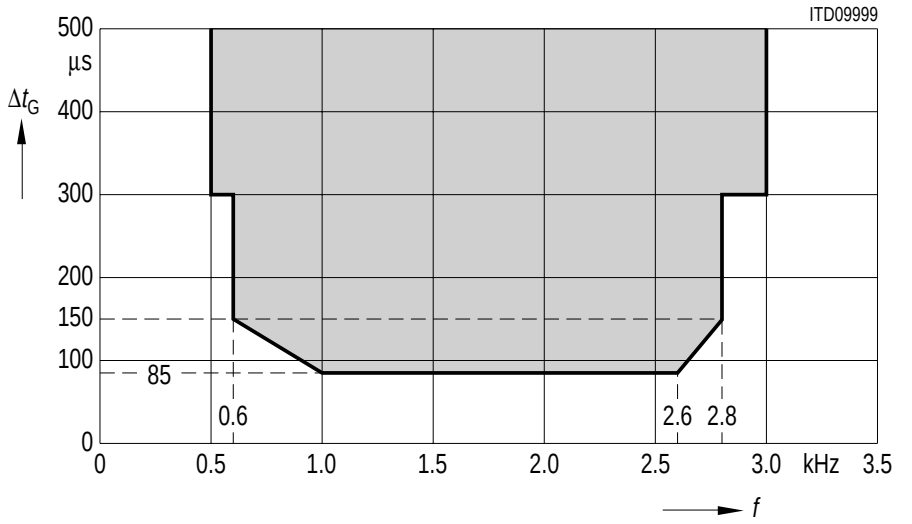


Figure 18

5.3 Out-of-Band Signals at Analog Input

With an 0 dBm0 out-of-band sine wave signal with frequency f (<<100 Hz or 3,4 kHz to 100 kHz) applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog input.[2)]

1) HPR is switched on: reference point is at t_{Gmin}
HPR is switched off: reference point is at 1.5 kHz

2) Poles at 12 kHz ± 150 Hz and 16 kHz ± 150 Hz are be provided

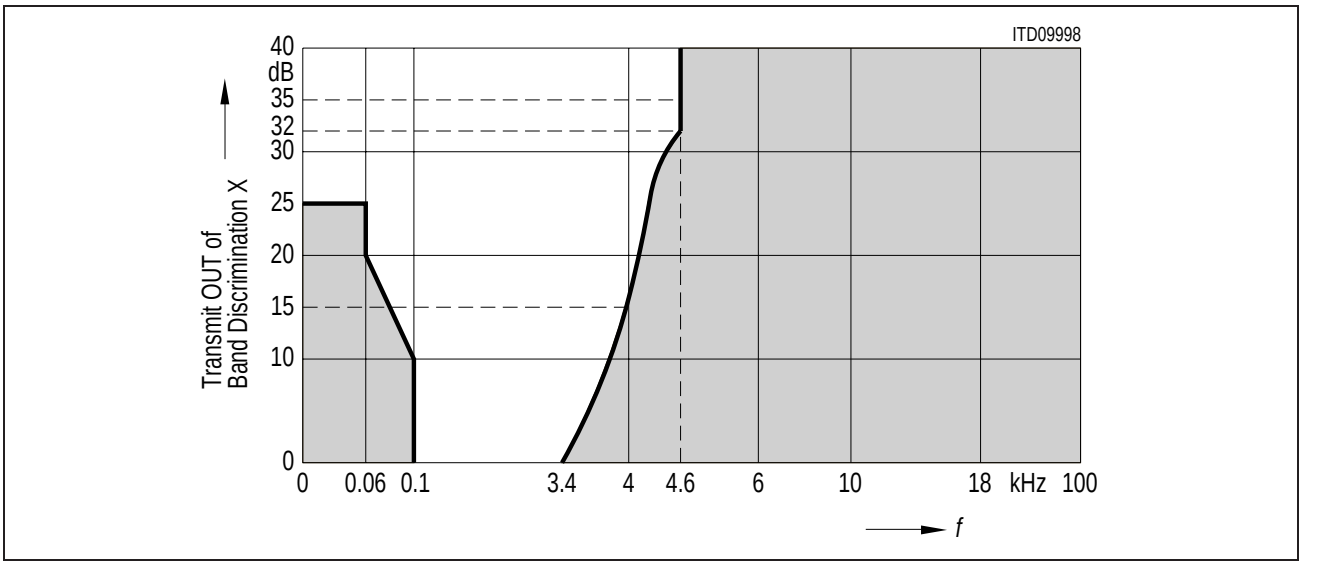


Figure 19

3.4 … 4.0 kHz: $X = -14\left(\sin\left(\pi \times \frac{4000 - F}{1200}\right) - 1\right)$

4.0 … 4.6 kHz: $X = -18\left(\sin\left(\pi \times \frac{4000 - F}{1200}\right) - \frac{7}{9}\right)$

5.4 Out-of-Band Signals at Analog Output

With a 0 dBm0 sine wave with frequency f (300 Hz to 3.99 kHz) applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.

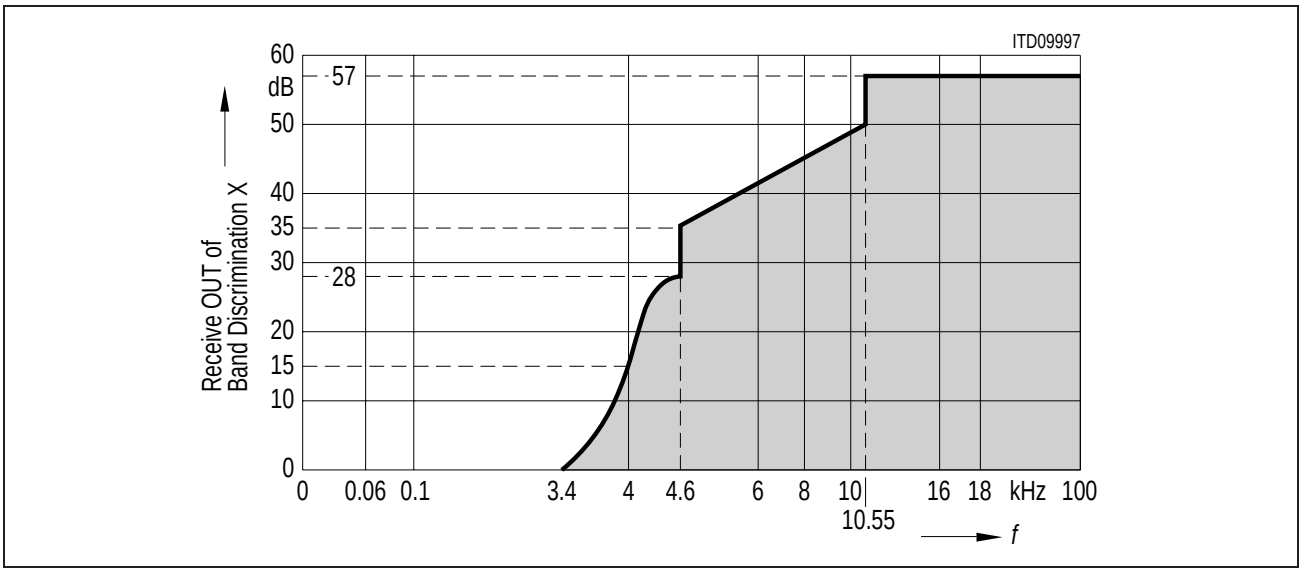


Figure 20

3.4 … 4.6 kHz: $X = -14\left(\sin\left(\pi \times \frac{4000 - F}{1200}\right) - 1\right)$

5.5 Out of Band Idle Channel Noise at Analog Output

With an idle code applied to the digital input, the level of any resulting out-of-band power spectral density (measured with 3 kHz bandwidth) at the analog output, will be not greater than the limit curve shown in the figure below.

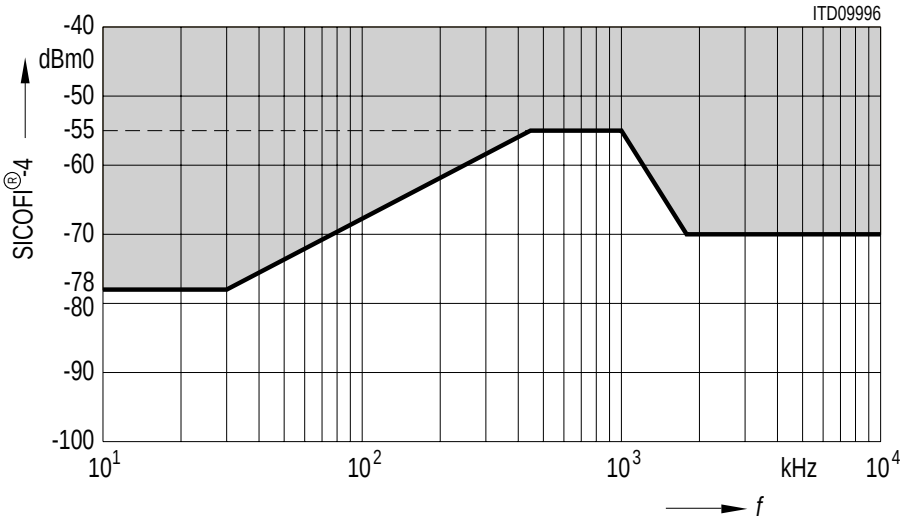


Figure 21

5.6 Overload Compression

μ-law, transmit: measured with sine wave f = 1014 Hz.

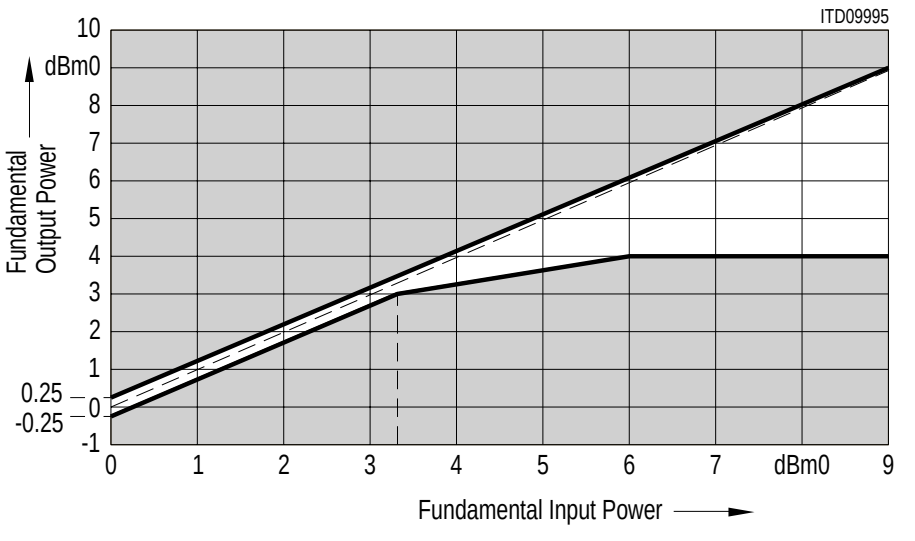


Figure 22

5.7 Gain Tracking (receive or transmit)

The gain deviations stay within the limits in the figures below

Gain Tracking: (measured with sine wave f = 1014 Hz, reference level is 0 dBm0)

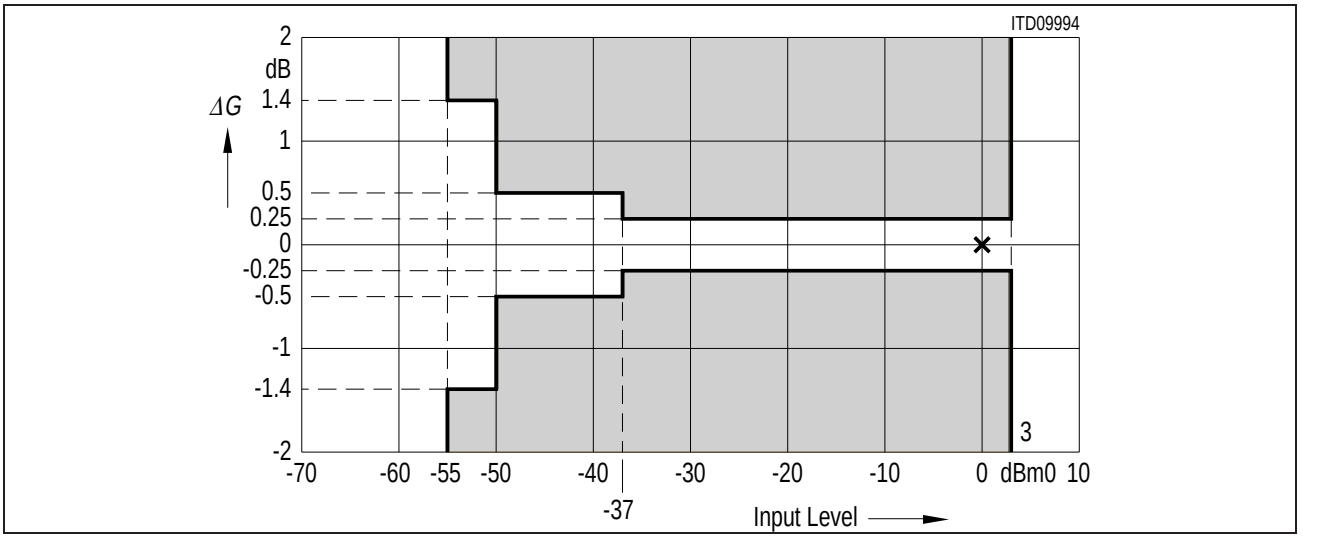


Figure 23

5.8 Total Distortion

The signal to distortion ratio exceeds the limits in the following figure.

5.8.1 Total Distortion Measured with Sine Wave

Receive or Transmit: measured with sine wave f = 1014 Hz. (C-message weighted for µ-law, psophometricaly weighted for A-law)

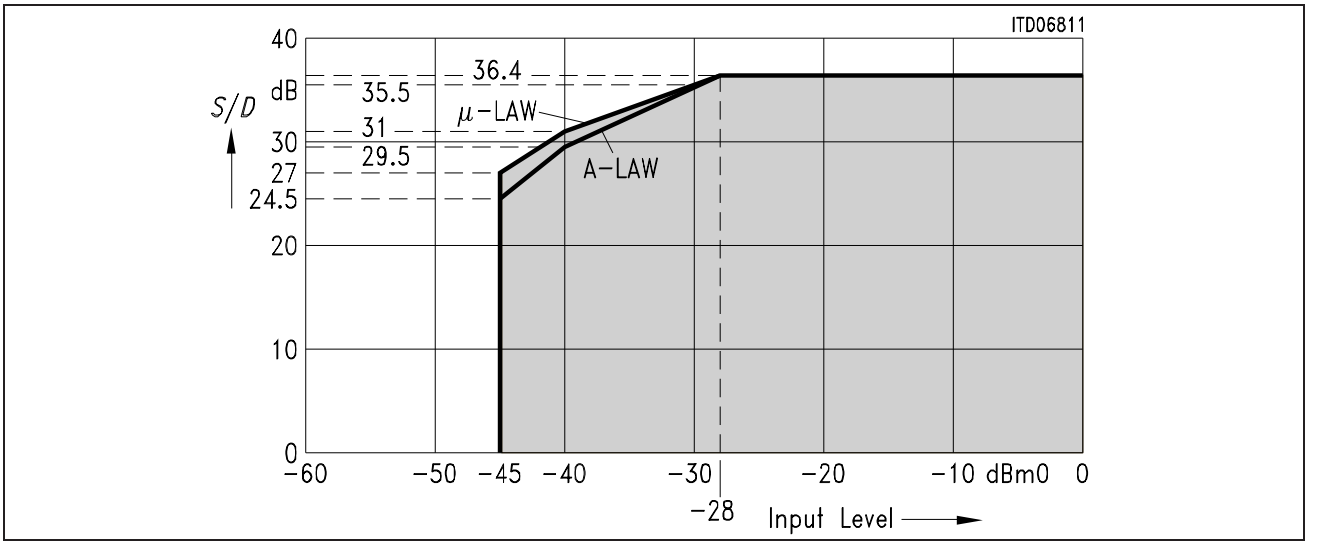


Figure 24

5.8.2 Total Distortion Measured with Noise According to CCITT

Receive

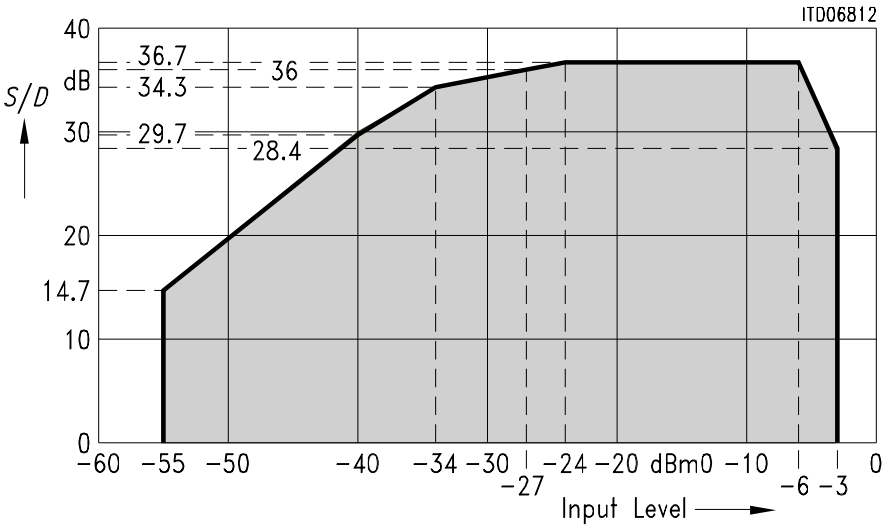


Figure 25

Transmit

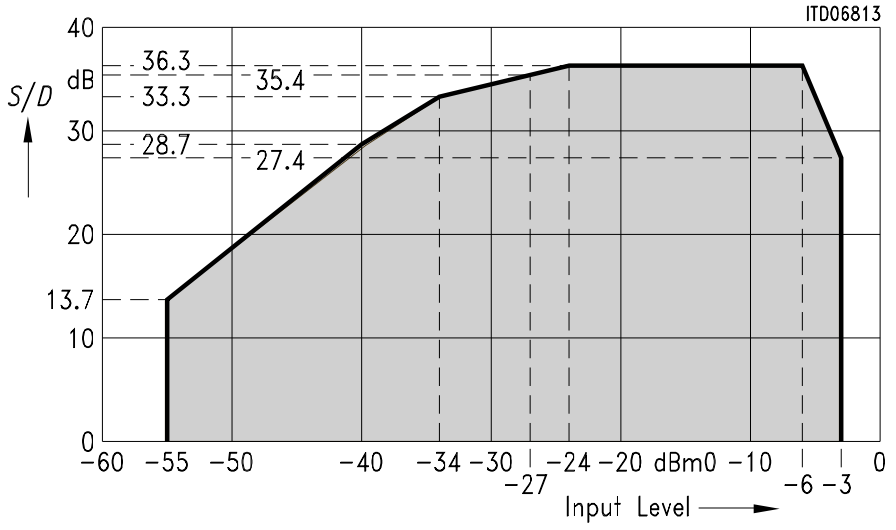


Figure 26

5.9 Single Frequency Distortion

An input signal with its frequency swept between 0.3 to 3 kHz for the receive path, or 0 to 12 kHz for the transmit path, any generated output signal with other frequency than the input frequency will stay 28 dB below the maximum input level of 0 dBm0.

Table 10

Receive		Transmit	
Frequency	**Max. Input Level**	**Frequency**	**Max. Input Level**
300 Hz to 3.4 kHz	0 dBm0	0 to 12 kHz	0 dBm0

5.10 Transhybrid Loss

The quality of Transhybrid-Balancing is very sensitive to deviations in gain and group delay - deviations inherent to the IOM-2 – SICOFI-2 A/D- and D/A-converters as well as to all external components used on a line card (SLIC, OP' s etc.)

Measurement of IOM-2 – SICOFI-2 transhybrid-loss: A 0 dBm0 sine wave signal and a frequency in the range between 300 - 3400 Hz is applied to the digital input. The resulting analog output signal at pin V_{OUT} is directly connected to V_{IN}, e.g. with the IOM-2 – SICOFI-2 testmode "Digital Loop Back via Analog Port". The programmable filters FRR, AR, FRX, AX and IM are disabled, the balancing filter TH is enabled with coefficients optimized for this configuration (V_{OUT} = V_{IN}).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below (Filter coefficients will be provided).

Table 11

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	typ.		
Trans Hybrid Loss at 300 Hz	THL_{300}	27	40	dB	T_A = 25 °C; V_{DD} = 5 V
Trans Hybrid Loss at 500 Hz	THL_{500}	33	45	dB	T_A = 25 °C; V_{DD} = 5 V
Trans Hybrid Loss at 2500 Hz	THL_{2500}	29	40	dB	T_A = 25 °C; V_{DD} = 5 V
Trans Hybrid Loss at 3000 Hz	THL_{3000}	27	35	dB	T_A = 25 °C; V_{DD} = 5 V
Trans Hybrid Loss at 3400 Hz	THL_{3400}	27	35	dB	T_A = 25 °C; V_{DD} = 5 V

The listed values for THL correspond to a typical variation of the signal amplitude and -delay in the analog blocks.

Δ amplitude = typ. $\pm$ 0.15 dB
Δ delay = typ. $\pm$ 0.5 µs

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 12

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
V_{DD} referred to GNDD		– 0.3	7.0	V	
GNDA to GNDD		– 0.6	0.6	V	
Analog input and output voltage referred to V_{DD} = 5 V; referred to GNDA = 0 V		 – 5.3 – 0.3	 0.3 5.3	 V V	

All digital input voltages
referred to GNDD = 0 V;
(V_{DD} = 5 V)
referred to V_{DD} = 5 V;
(GNDD = 0 V)
		
		– 0.3
		
		– 5.3
			
			5.3
			
			0.3
				
				V
				
				V	

DC input and output current at any input or output pin (free from latch -up)			10	mA	
Storage temperature	T_{STG}	– 60	125	°C	
Ambient temperature under bias	T_A	– 10	80	°C	
Power dissipation (package)	P_D		1	W	

6.2 Operating Range

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; GNDD = 0 V; GNDA = 0 V

Table 13

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current standby operating (2 channels)	I_{DD}		 1.2 27	 2 40	 mA mA	
Power supply rejection of either supply/direction receive V_{DD} guaranteed receive V_{DD} target value	$PSRR$	 30 14 30			 dB dB dB	Ripple: 0 to 150 kHz, 70 mVrms Measured: 300 Hz to 3.4 kHz Measured: at f: 3.4 to 150 kHz
Power dissipation standby	PD_S		15	20	mW	
Power dissipation operating	PD_{o1}		75	110	mW	1 channel operating
Power dissipation operating	PD_{o2}		100	140	mW	2 channels operating

6.3 Digital Interface

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; GNDD = 0 V; GNDA = 0 V

All input-pins, with exception of the RESET-pin, have a TTL-input characteristic.

Table 14

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Low-input voltage	V_{IL}	– 0.3	0.8	V	
High-input voltage	V_{IH}	2.0		V	
Low-output voltage	V_{OL}		0.45	V	I_O = – 5 mA
Low-output voltage DU pin	V_{OL}		0.45	V	I_O = – 7 mA, R_L = 1 kΩ
High-output voltage	V_{OH}	4.4		V	I_0 = 5 mA
Input leakage current	I_{IL}		± 1	µA	$-0.3 \le V_{IN} \le V_{DD}$

6.4 Analog Interface

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %; GNDD = 0 V; GNDA = 0 V

Table 15

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Analog input resistance	R_I	160	270	480	kΩ	
Analog output resistance	R_O			10	W	
Analog output load	R_L C_L	20		 20	kΩ pF	
Input leakage current	I_{IL}		± 0.1	± 1.0	µA	$0 \le V_{IN} \le V_{DD}$
Input voltage range (AC)	V_{IR}			±± 2.223.	V	

6.5 RESET Timing

To reset the IOM-2 – SICOFI-2 to basic setting mode, positive pulses applied to pin RS have to be higher than 2.4 V (CMOS-Schmitt-Trigger Input) and longer than 3 µs. Signals shorter than 1 µs will be ignored.

6.6 IOM®-2 Interface Timing

6.6.1 4-MHz Operation Mode (Mode = 1)

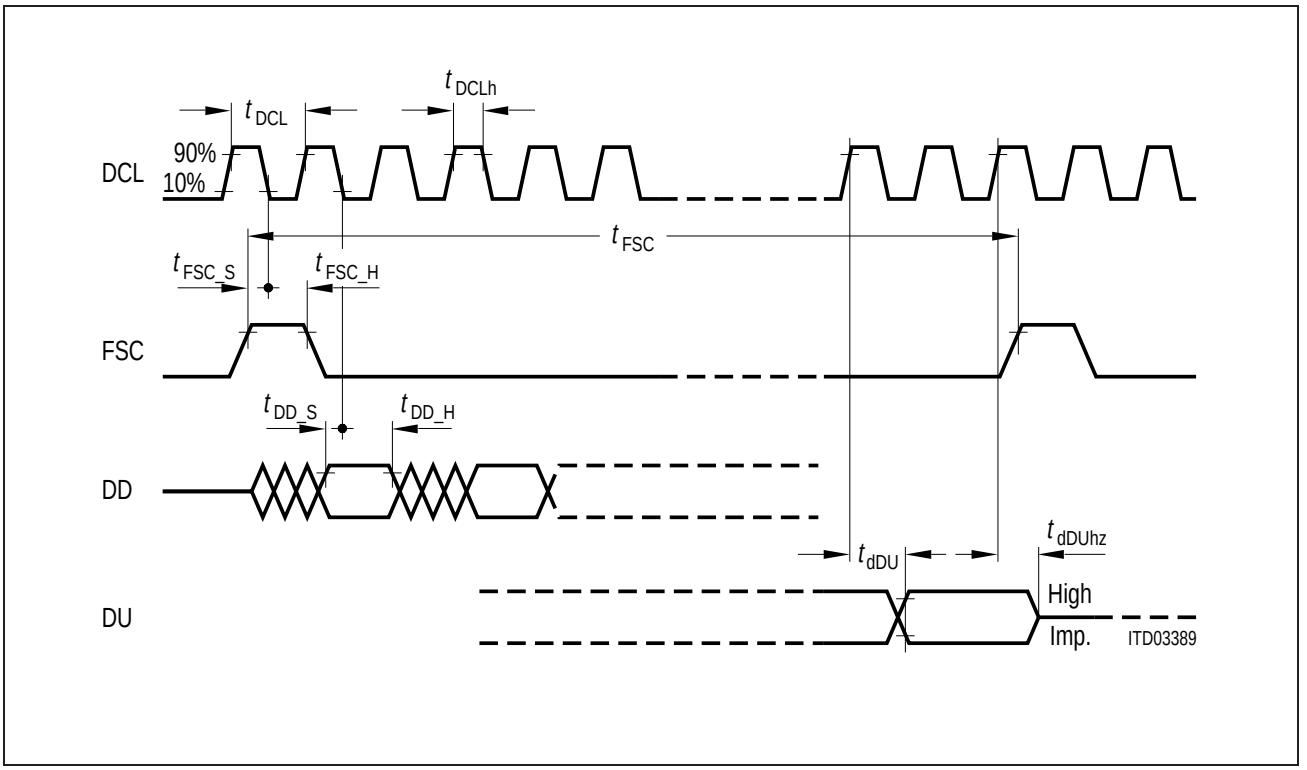


Figure 27

Switching Characteristics

Table 16

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL ‘fast’ mode [1]	t_{DCL}		1/4096		kHz
DCL duty cycle		40		60	%
Period FSC [1]	t_{FSC}		125		µs
FSC setup time	t_{FSC_S}	70	t_{DCLh}		ns
FSC hold time	t_{FSC_H}	40			ns
DD data in setup time	t_{DD_S}	20			ns
DD data in hold time	t_{DD_H}	50			ns
DU data out delay [2]	t_{dDU}		150	320	ns

[1] DCL = 4096 kHz: $t_{FSC} = 512 \times t_{DCL}$
[2] Depending on Pull-up resistor used in application (typical 1 kΩ), DU is a “open drain” - line

6.6.2 2-MHz Operation Mode (Mode = 0)

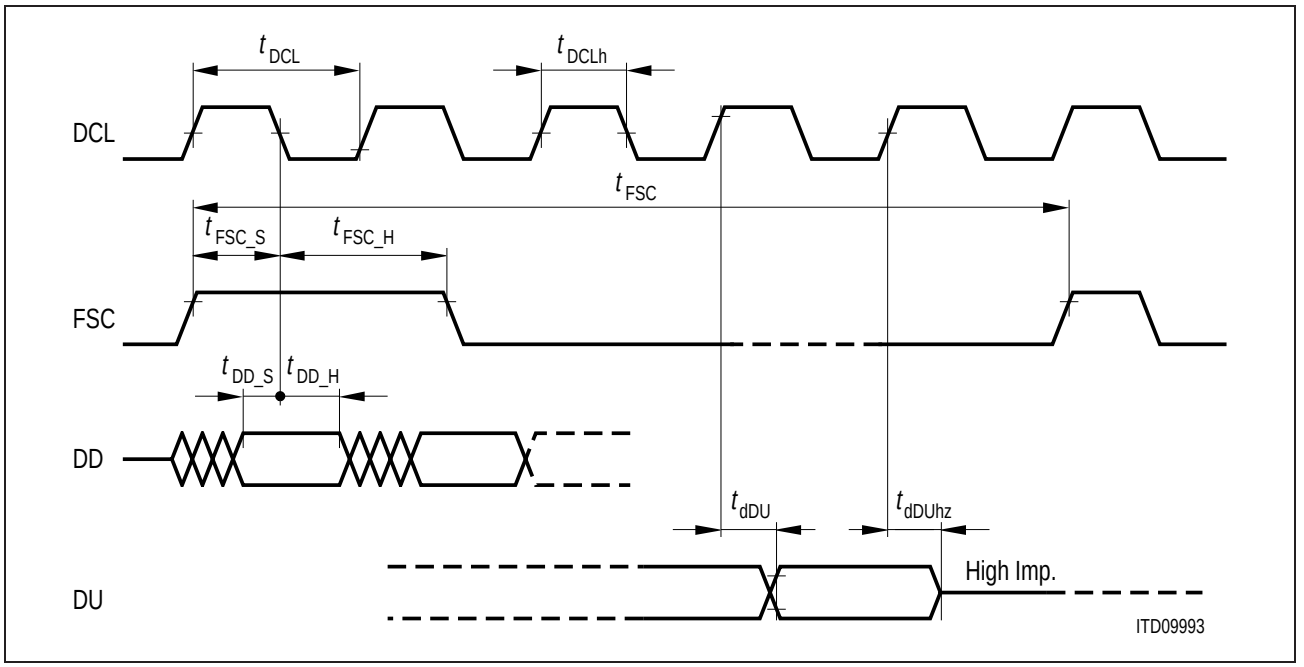


Figure 28

Switching Characteristics

Table 17

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL “slow” mode[1)]	t_{DCL}		1/2048		kHz
DCL duty cycle		40		60	%
Period FSC[1)]	t_{FSC}		125		µs
FSC setup time	t_{FSC_S}	70	t_{DCLh}		ns
FSC hold time	t_{FSC_H}	40			ns
DD data in setup time	t_{DD_S}	20			ns
DD data in hold time	t_{DD_H}	50			ns
DU data out delay[2)]	t_{dDU}		150	175	ns

1) DCL = 2048 kHz: $t_{FSC} = 256 \times t_{DCL}$
2) Depending on pull up resistor used in application (typical 1 kΩ), DU is a “open drain” - line.

6.7 IOM®-2 Command/Indication Interface Timing

6.7.1 4-MHz Operation Mode (Mode = 1)

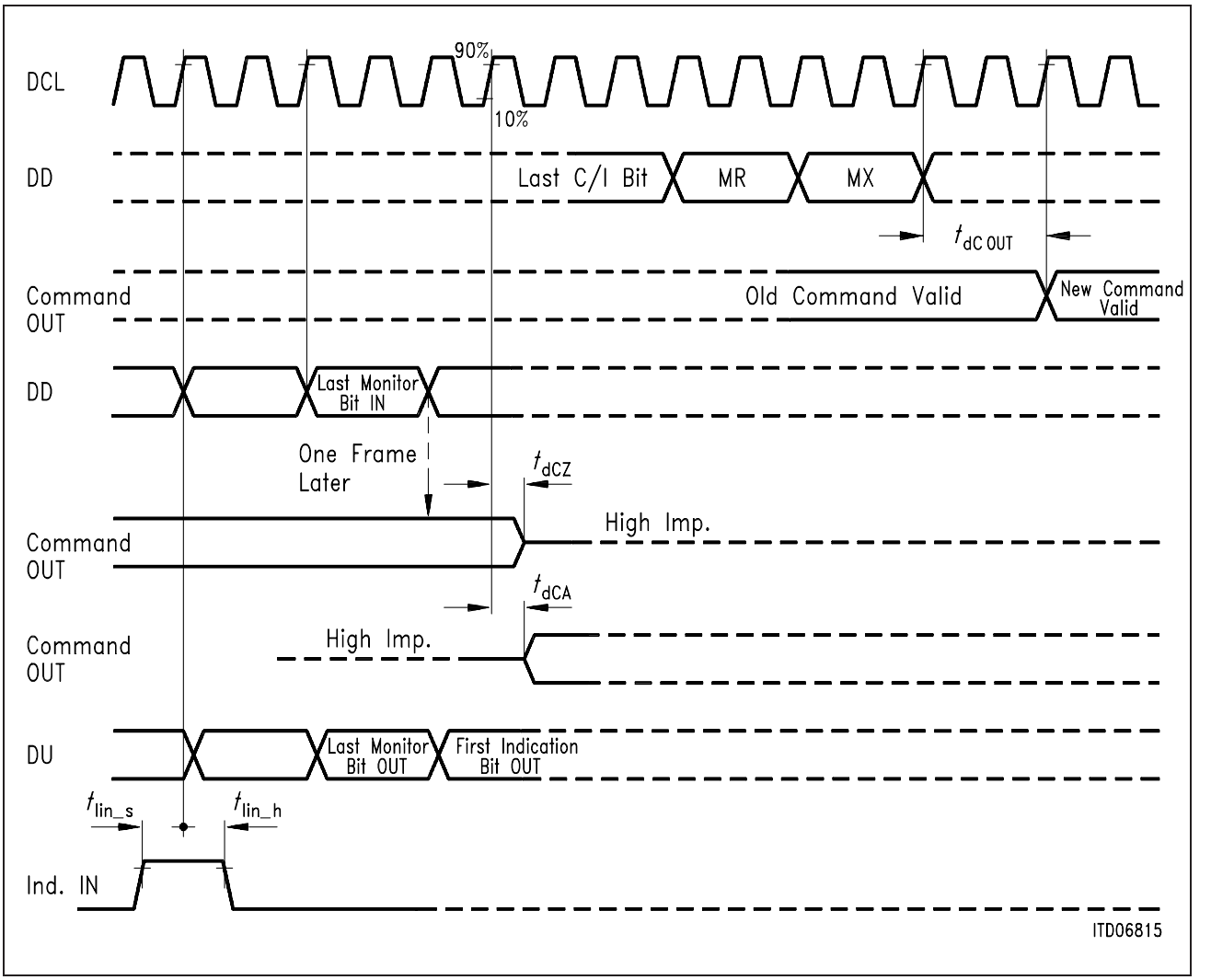


Figure 29

6.7.2 2-MHz Operation Mode (Mode = 0)

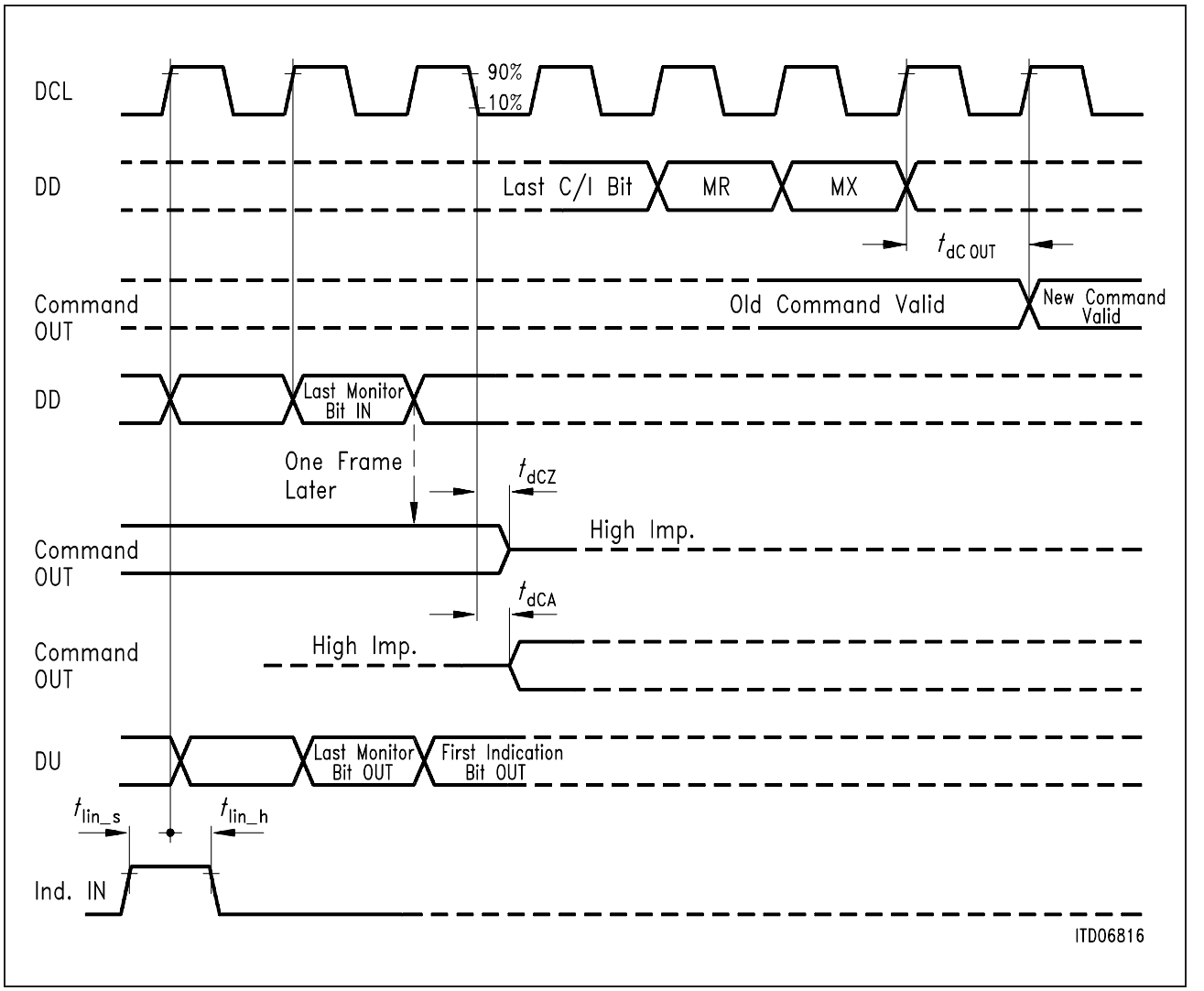


Figure 30

Switching Characteristics

Table 18

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Command out delay	t_{dCout}		150	250	ns
Command out high impedance	t_{dCZ}		150	250	ns
Command out active	t_{dCA}		150	250	ns
Indication in setup time	t_{lin_s}	50			ns
Indication in hold time	t_{lin_h}	100			ns

6.8 Detector Select Timing

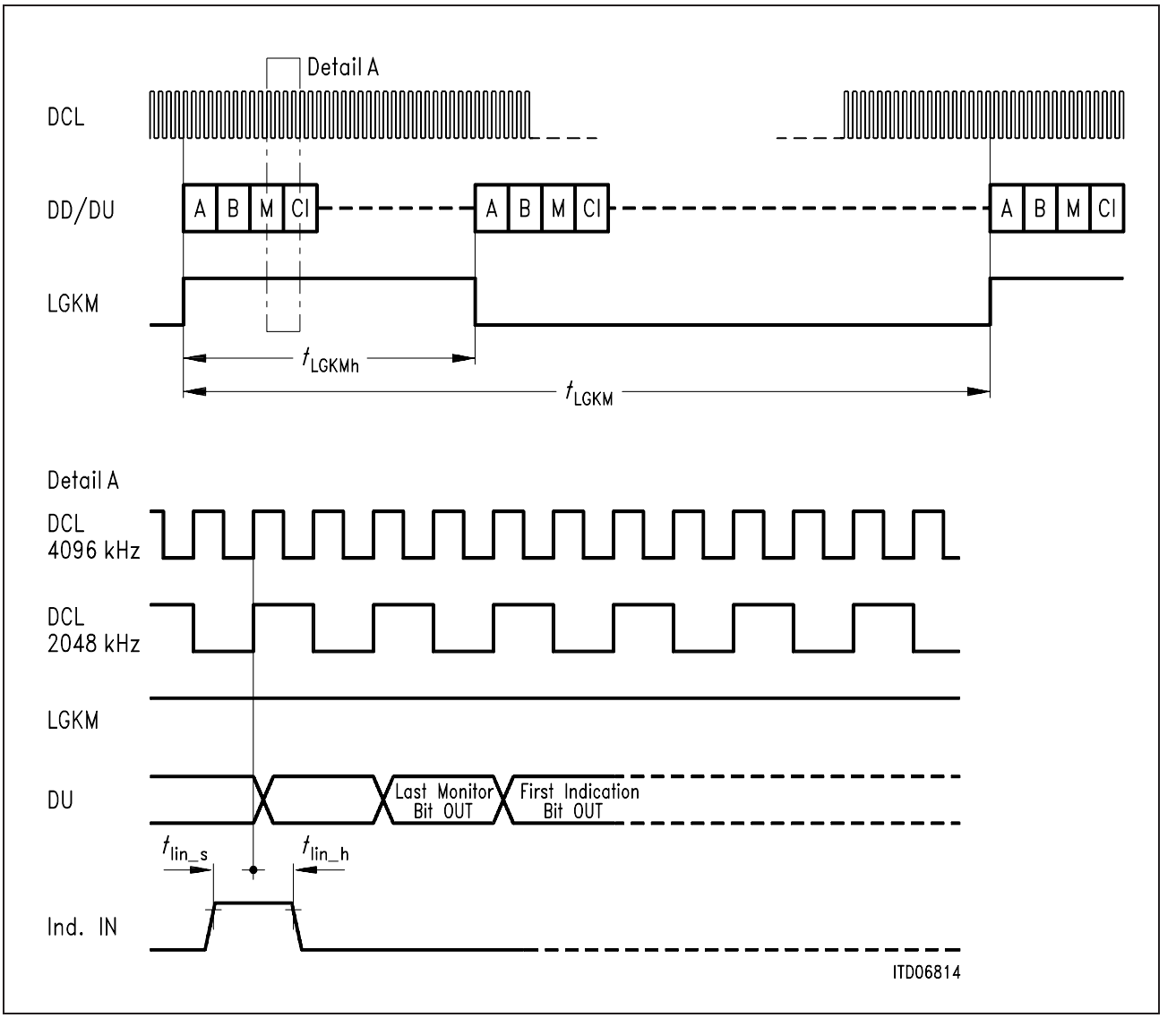


Figure 31

6.8.1 Switching Characteristics

Table 19

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Detector select high time	t_{LGKMh}		125		µs
Detector select repeat	t_{LGKM}		1 ... 14		ms
Indication in setup time	t_{lin_s}	50			ns
Indication in hold time	t_{lin_h}	100			ns

7 Appendix

7.1 IOM®-2 Interface Monitor Transfer Protocol

7.1.1 Monitor Channel Operation

The Monitor Channel is used for the transfer of maintenance information between two functional blocks. Using two monitor control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure. The MR and MX bits in the fourth octet (C/I channel) of the IOM-2 frame are used for the handshake procedure of the monitor channel.

The monitor channel transmission operates on a pseudo-asynchronous basis:

– Data transfer (bits) on the bus is synchronized to Frame Sync FSC
– Data flow (bytes) are asynchronously controlled by the handshake procedure.

For example: Data is placed onto the DD-monitor-channel by the monitor-transmitter of the master device (DD-MX-Bit is activated i.e. set to ‘0’). This data transfer will be repeated within each frame (125 µs rate) until it is acknowledged by the IOM-2 – SICOFI-2 monitor-receiver by setting the DU-MR-bit to ‘0’, which is checked by the monitor-transmitter of the master device. Thus, the data rate is not 8 kbyte/s.

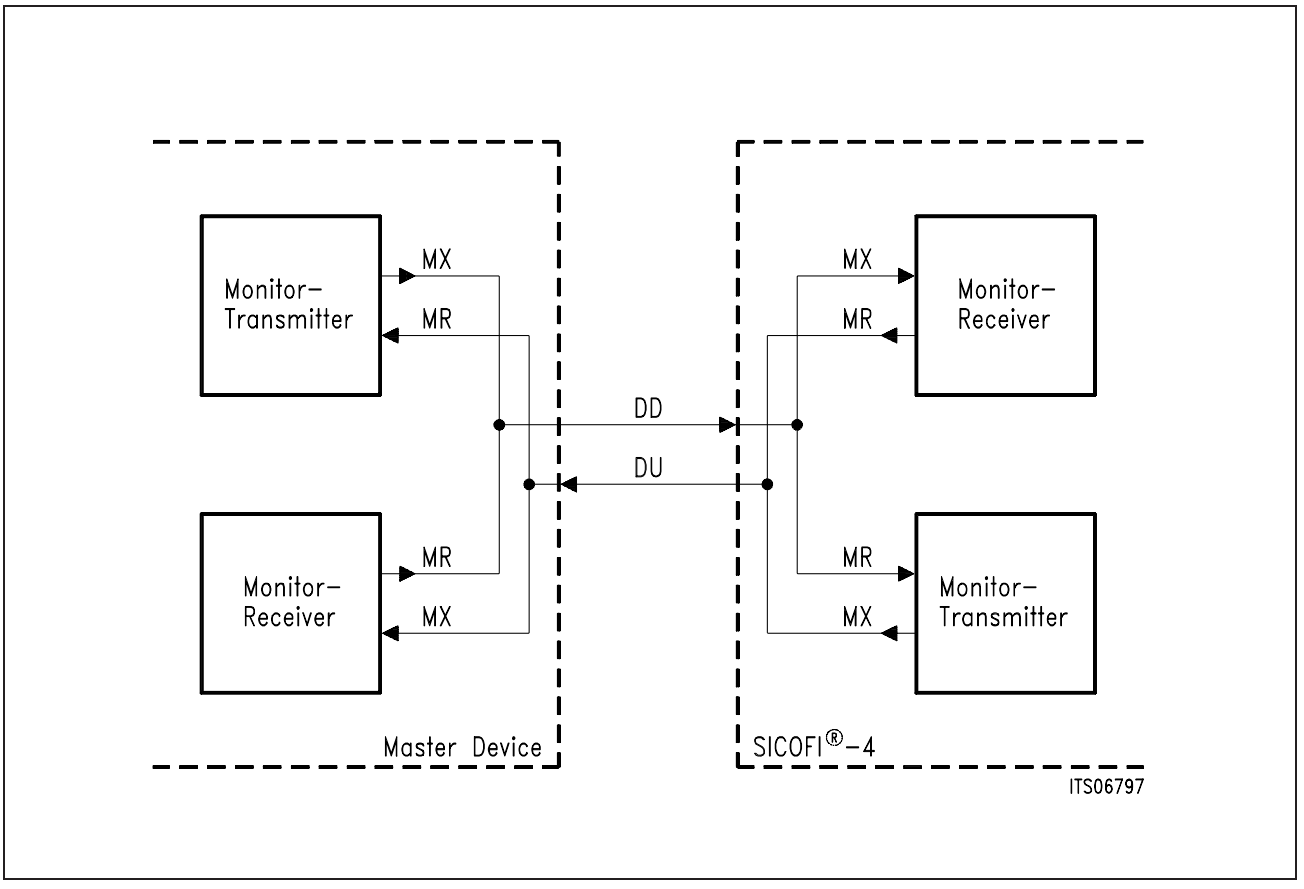


Figure 32

7.1.2 Monitor Handshake Procedure

The monitor channel works in 3 states

– idle state: A pair of inactive (set to ‘1’) MR- and MX-bits during two or more consecutive frames: End of Message (EOM)
– sending state: MX-bit is activated (set to ‘0’) by the monitor-transmitter, together with data-bytes (can be changed) on the monitor-channel
– acknowledging: MR-bit is set to active (set to ‘0’) by the monitor-receiver, together with a data-byte remaining in the monitor-channel.

A start of transmission is initiated by a monitor-transmitter in sending out an active MX-bit together with the first byte of data (the address of the receiver) to be transmitted in the monitor-channel.

This state remains until the addressed monitor-receiver acknowledges the received data by sending out an active MR-bit, which means that the data-transmission is repeated each 125 µs frame (minimum is one repetition). During this time the monitor-transmitter evaluates the MR-bit.

Flow control, means in the form of transmission delay, can only take place when the transmitters MX and the receivers MR bit are in active state.

Since the receiver is able to receive the monitor data at least twice (in two consecutive frames), it is able to check for data errors. If two different bytes are received the receiver will wait for the receipt of two identical successive bytes (last look function).

A collision resolution mechanism (check if another device is trying to send data during the same time) is implemented in the transmitter. This is done by looking for the inactive (‘1’) phase of the MX-bit and making a per bit collision check on the transmitted monitor data (check if transmitted ‘1’s are on DU/DD-line; DU/DD-line are open-drain lines).

Any abort leads to a reset of the IOM-2 – SICOFI-2 command stack, the device is ready to receive new commands.

To obtain a maximum speed data transfer, the transmitter anticipates the falling edge of the receivers acknowledgment.

Due to the inherent programming structure, duplex operation is not possible. It is **not allowed** to send any data to the IOM-2 – SICOFI-2, while transmission is active.

7.1.3 State Diagram of the IOM®-2 – SICOFI®-2 Monitor Transmitter

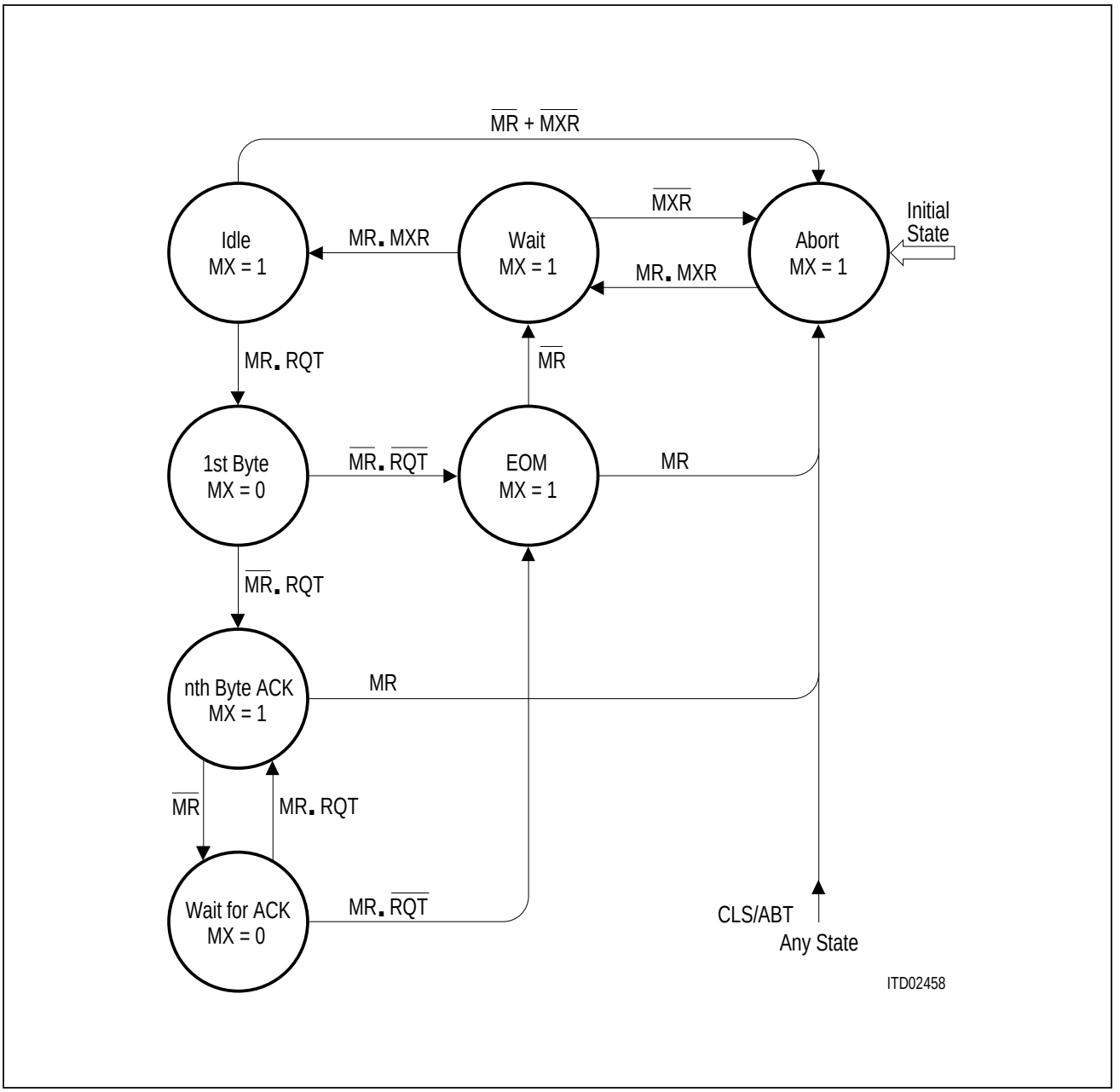


Figure 33

MR …	MR - bit received on DD - line
MX …	MX - bit calculated and expected on DU - line
MXR …	MX - bit sampled on DU - line
CLS …	Collision within the monitor data byte on DU - line
RQT …	Request for transmission form internal source
ABT …	Abort request/indication
. …	logical AND
+ …	logical OR

7.1.4 State Diagram of the IOM®-2 – SICOFI®-2 Monitor Receiver

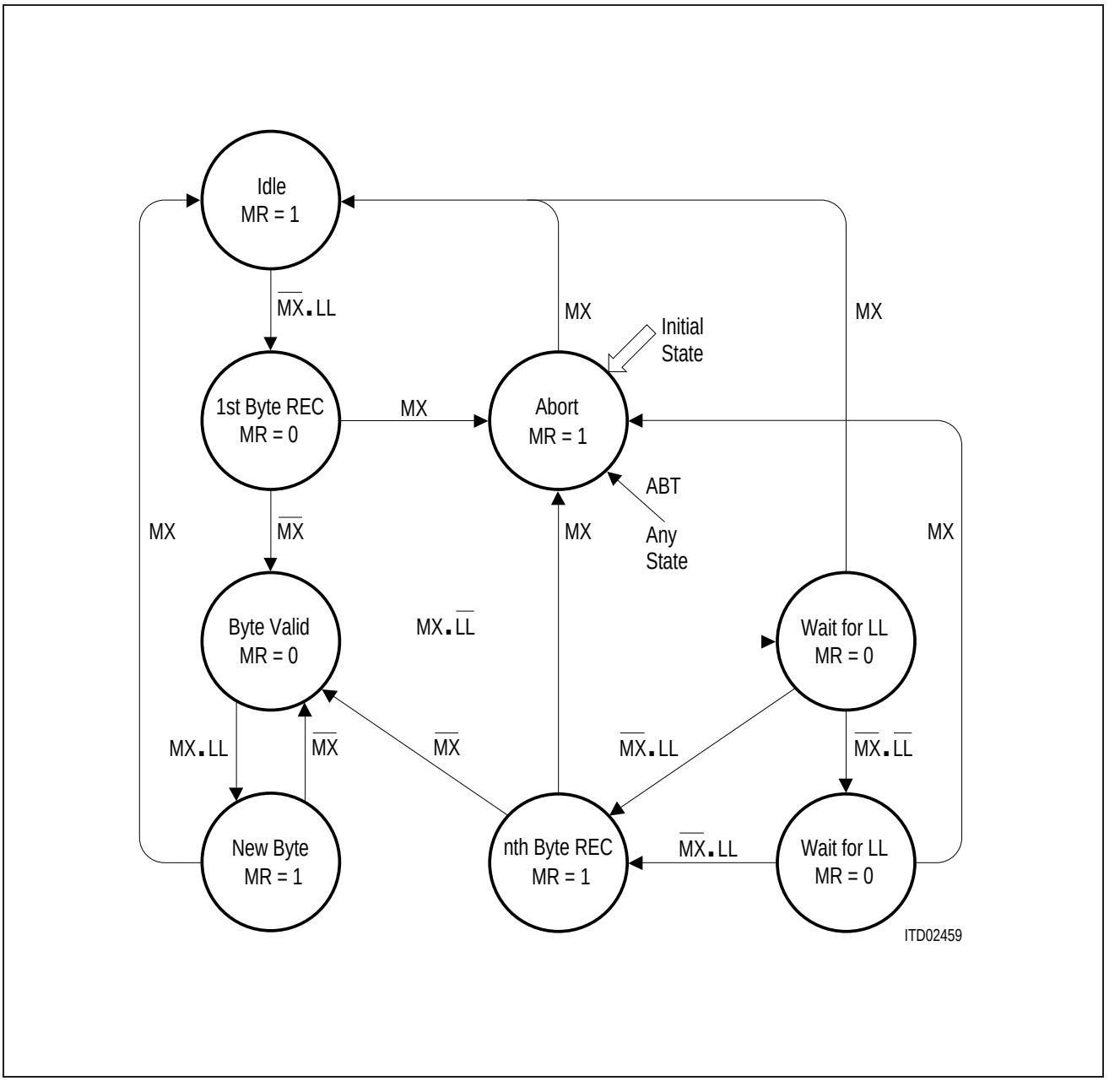


Figure 34

MR … MR - bit calculated and transmitted on DU - line
MX … MX - bit received data downstream (DD - line)
LL … Last lock of monitor byte received on DD - line
ABT … Abort indication to internal source
. … logical AND
+ … logical OR

7.2 Monitor Channel Data Structure

The monitor channel is used for the transfer of maintenance information between two functional blocks. By use of two monitor control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure.

7.2.1 Address Byte

Messages to and from the IOM-2 – SICOFI-2 are started with the following Monitor byte:

Bit	7	6	5	4	3	2	1	0
	1	0	0	0	0	0	0	1

Thus providing information for two voice channels, the IOM-2 – SICOFI-2 is one device on one IOM-2 time slot. Monitor data for a specific voice channel is selected by the IOM-2 – SICOFI-2 specific command (SOP or COP).

7.2.2 Identification Command

In order to be able to unambiguously identify different devices by software, a two byte identification command is defined for analog lines IOM-2 devices.

1	0	0	0	0	0	0	0

0	0	0	0	0	0	0	0

Each device will then respond with its specific identification code. For the IOM-2 – SICOFI-2 this two byte identification code is:

1	0	0	0	0	0	0	0

1	0	0	0	0	0	1	0

Each byte is transferred at least twice (in two consecutive frames).

7.3 IOM®-2 Interface Programming Procedure

Example for a typical IOM-2 interface programming procedure, consisting of identification request and answer, a SOP Write command with three byte following, and SOP Read to verify the programming.

Table 20

Frame	Data Down		Data Up	
	Monitor	**MR/MX**	**Monitor**	**MR/MX**
1	11111111	11	11111111	11
2	IDRQT. 1st byte	10	11111111	11
3	IDRQT. 1st byte	10	11111111	01
4	IDRQT. 2nd byte	11	11111111	01
5	IDRQT. 2nd byte	10	11111111	11
6	11111111	11	11111111	01
7	11111111	11	IDANS. 1st byte	10
8	11111111	01	IDANS. 1st byte	10
9	11111111	01	IDANS. 2nd byte	11
10	11111111	11	IDANS. 2nd byte	10
11	11111111	01	11111111	11
12	Address	10	11111111	11
13	Address	10	11111111	01
14	SOP Write	11	11111111	01
15	SOP Write	10	11111111	11
16	CR3	11	11111111	01
17	CR3	10	11111111	11
18	CR2	11	11111111	01
19	CR2	10	11111111	11
20	CR1	11	11111111	01
21	CR1	10	11111111	11
22	SOP Read	11	11111111	01
23	SOP Read	10	11111111	11
24	11111111	11	11111111	01
25	11111111	11	Address	10

Table 20 (cont'd)

Frame	Data Down		Data Up	
	Monitor	**MR/MX**	**Monitor**	**MR/MX**
26	11111111	01	Address	10
27	11111111	01	CR3	11
28	11111111	11	CR3	10
29	11111111	01	CR2	11
30	11111111	11	CR2	10
31	11111111	01	CR1	11
32	11111111	11	CR1	10
33	11111111	01	11111111	11

IDRQT … identification request (80_H, 00_H)

IDANS … answer to identification request (80_H, 82_H)

Address … IOM-2 – SICOFI-2 specific address byte (81_H)

CRx … Data for/from configuration register x.

8 Test Features

8.1 Boundary Scan

8.1.1 General

The IOM-2 – SICOFI-2 provides fully IEEE Std. 1149.1 compatible boundary scan support consisting of:

– a complete boundary scan (digital pins)
– a test access port controller (TAP)
– four dedicated pins (TCK, TMS, TDI, TDO)
– a 32 bit ICODE register

All IOM-2 – SICOFI-2 digital pins expect power supply $V_{DD\,D}$ and ground GNDD are included in the boundary scan. Depending on the pin functionality one, two or three boundary cells are provided.

Table 21

Pin Type	Number of Boundary Scan Cells	Usage
Input	1	Input
Output	2	Output, enable
I/O	3	Input, output, enable

When the TAP controller is in the appropriate mode, data is shifted into/out of the boundary scan via the pins TDI/TDO controlled by the clock applied to pin TCK.

The IOM-2 – SICOFI-2 pins are included in the following sequence in the boundary scan:

Table 22

Pin Number	Pin Name	Type
57	MODE	I
59	TSS1	I
60	TSS0	I
61	N.U.I.	I
62	N.U.I.	I
63	N.U.I.	I
64	N.U.IO.	I/O
1	N.U.IO.	I/O

Table 22 (cont'd)

Pin Number	Pin Name	Type
2	N.C.	O
3	N.C.	O
4	N.C.	O
13	N.C.	O
14	N.C.	O
15	N.C.	O
16	N.U.IO.	I/O
17	N.U.IO.	I/O
18	N.U.I.	I
19	N.U.I.	I
20	N.U.I.	I
21	N.C.	O
22	RESET	I
24	DD	I
25	DU	O (open drain)
26	DCL	I
27	FSC	I
28	LGKM0	O
29	SI1_2	I
30	SI1_1	I
31	SI1_0	I
32	SB1_1	I/O
33	SB1_0	I/O
34	SO1_2	O
35	SO1_1	O
36	SO1_0	O
45	SO2_0	O
46	SO2_1	O
47	SO2_2	O
48	SB2_0	I/O

Table 22 (cont'd)

Pin Number	Pin Name	Type
49	SB2_1	I/O
50	SI2_0	I
51	SI2_1	I
52	SI2_0	I

8.1.2 The TAP-Controller

The Test Access Port (TAP) controller implements the state machine defined in the JTAG standard IEEE Std. 1149.1. Transitions on pin TMS (Test Mode Select) cause the TAP controller to perform a state change. According to the standard definition five instructions are executable:

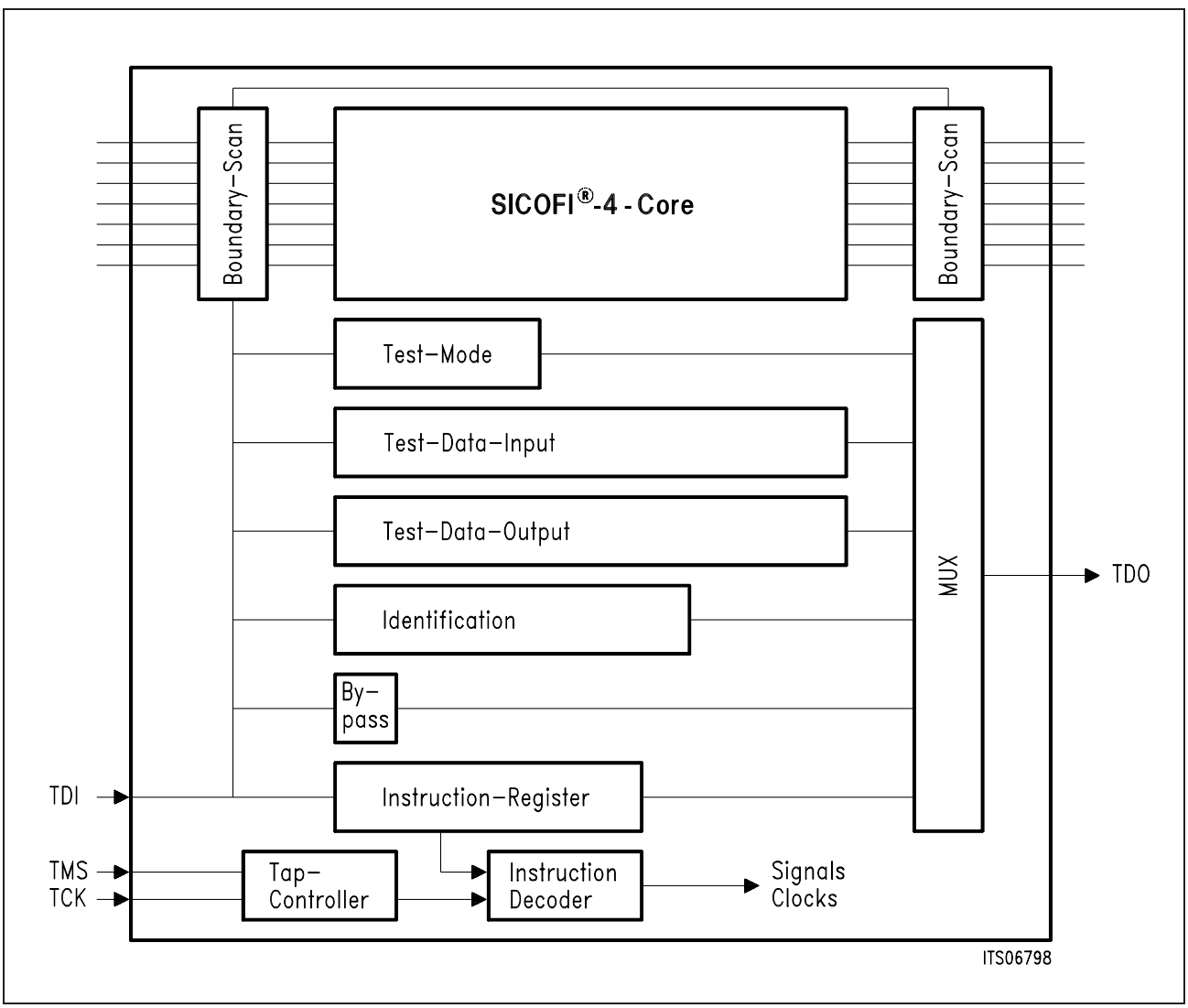


Figure 35

Table 23

Code	Instruction	Function
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing
0011	ICODE	Reading ID code
0100	Tap_Test 1	Configuration for Level Metering
0101	Tap_Test 2	Wait for result
1000	Tap_Test 5	Serial testdata output (Level Metering Results)
0111	Tap_Test 4	Switch off Test
11xx	BYPASS	Bypass operation

EXTEST Is used to examine the board interconnections.

INTEST Supports internal chip testing (is the default value of the instruction register)

SAMPLE/PRELOAD Provides a snap-shot of the pin level during normal operation, or is used to preload the boundary scan with a test vector

ICODE The 32 bit identification register is serially read out via TDO. It contains a version number (4 bit), a device code (16 bit) and the manufacture code (11 bit). The LSB is fixed to '1'.
For the IOM-2 – SICOFI-2 V1.1 the Code is: '0011 0000 0000 0001 0101 0000 1000 001 1'

TAP_TEST1 39 bit field for selecting operation
(Level Metering Offset, Loops, Tone Generator …)

TAP_TEST2 Wait for Level Metering result ready (should be > t.b.d. mS)

TAP_TEST5 Level Metering Data output (1 bit result of Level Metering per channel)

TAP_TEST4 Level Metering Operation is switched off

BYPASS a bit entering TDI is shifted to TDO after one TCK clock cycle

8.2 Level Metering Function

The Level Metering Function is a functional selftest (available per channel), which allows selftest of the chip (digital, or digital and analogue), and also selftest of the board (including the SLIC).

An external or internally generated sine-wave signal is fed to the receive path. After switching a loop (internal or external via the SLIC) to the transmit-path the return level is measured and compared to a programmable offset value. The result of this operation (greater or smaller than offset) can be read out via the IOM-2 interface (bit LMR in configuration register CR2).

There is a single-8-bit Offset-Register available for both two channels. This offset register can be accessed as XR4 with a XOP-Command (Field LSEL = 100)

This register contains the 2's complement offset value for the level metering function

Bit	7	6	5	4	3	2	1	0
	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

Block Diagram

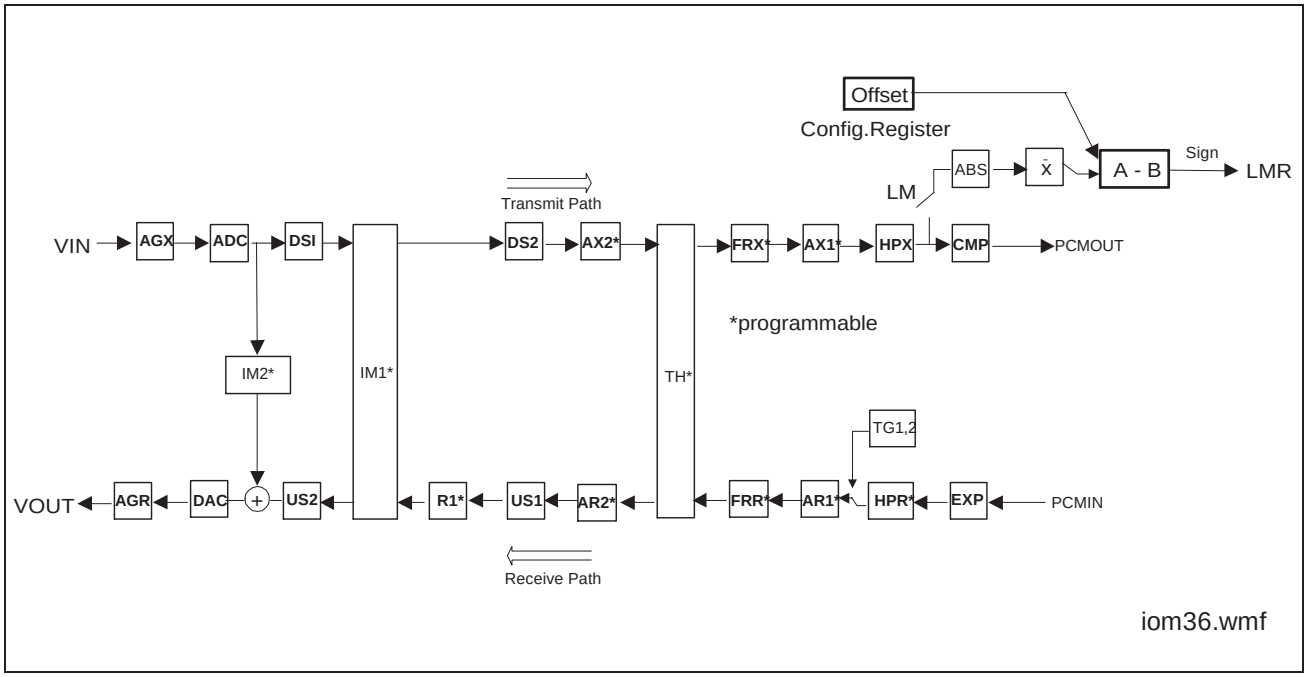


Figure 36

(For further information, an Application Note describing the calculation of the offset value and the sensitivity, is available).

8.3 Programming the IOM®-2 – SICOFI®-2 Tone Generators

Two independent Tone Generators are available per channel. When one or both tone-generators are switched on, the voice signal is switched off automatically for the selected voice channel. To make the generated signal sufficient for DTMF, a programmable bandpass-filter is included. The default frequency for both tone generators is 1000 Hz.

The QSICOS-program contains a program for generating coefficients for variable frequencies.

Byte sequences for programming both the tone generators and the bandpass-filters:

Table 24

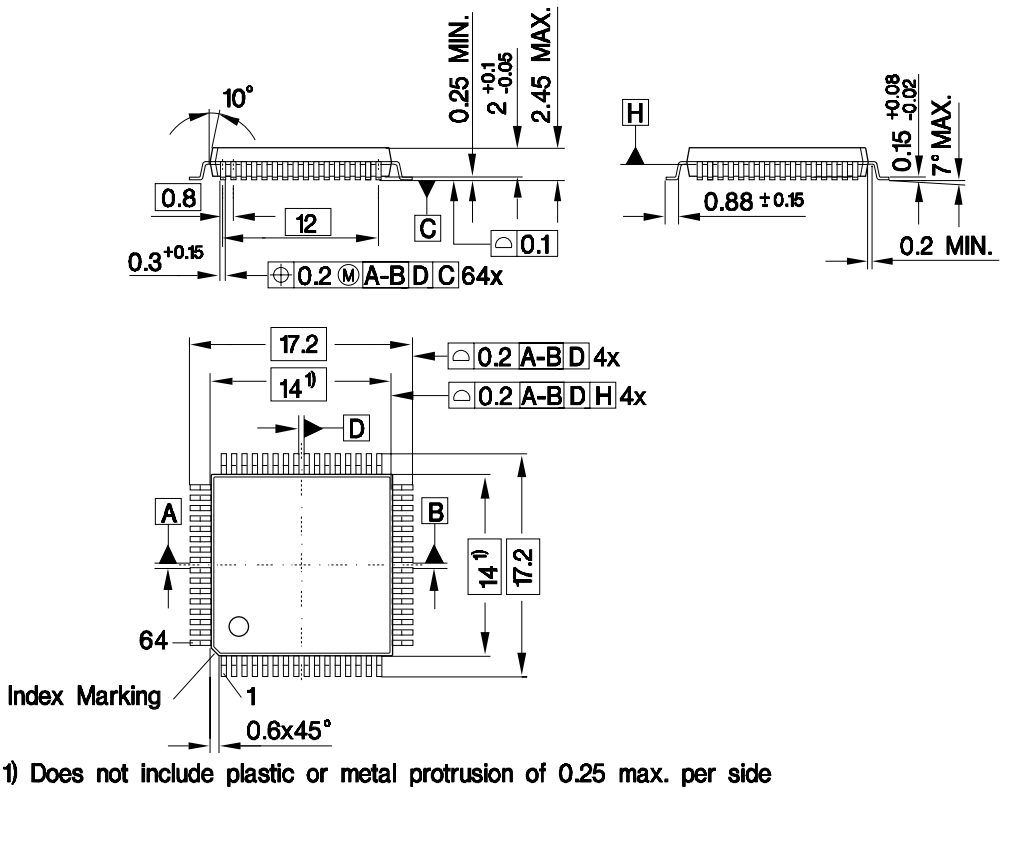
Frequency	Command	Byte 1	Byte 2	Byte 3	Byte 4
697 Hz	0C/0D[1)]	0A	33	5A	2C
770 Hz	0C/0D[1)]	12	33	5A	C3
852 Hz	0C/0D[1)]	13	3C	5B	32
941 Hz	0C/0D[1)]	1D	1B	5C	CC
1209 Hz	0C/0D[1)]	32	32	52	B3
1336 Hz	0C/0D[1)]	EC	1D	52	22
1477 Hz	0C/0D[1)]	AA	AC	51	D2
800 Hz	0C/0D[1)]	12	D6	5A	C0
950 Hz	0C/0D[1)]	1C	F0	5C	C0
1008 Hz	0C/0D[1)]	1A	AE	57	70
2000 Hz	0C/0D[1)]	00	80	50	09

[1)] 0C is used for programming Tone Generator 1, in channel 1.
0D is used for programming Tone Generator 2, in channel 1.

The resulting signal amplitude can be set by transmitting the AR1 and AR2 filters. By switching a “digital loop” the generated sine-wave signal can be fed to the transmit path.

9 Package Outlines

P-MQFP-64-1-2 (SMD)
(Plastic Metric Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm