

PHX20N06T

N-channel TrenchMOS™ standard level FET

Rev. 01 — 16 February 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a fully isolated plastic package using TrenchMOS™ technology.

1.2 Features

- Standard level compatible
- Isolated package.

1.3 Applications

- DC motor control
- DC-to-DC converters
- Synchronous rectification
- General purpose power switching.

1.4 Quick reference data

- $V_{DS} \leq 55 \text{ V}$
- $I_D \leq 12.9 \text{ A}$
- $P_{tot} \leq 23 \text{ W}$
- $R_{DS(on)} \leq 75 \text{ m}\Omega$.

2. Pinning information

Table 1: Pinning - SOT186A (TO-220F), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	source (s)		
3	drain (d)		
mb	mounting base; isolated		

SOT186A (TO-220F)



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3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PHX20N06T	TO-220F	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 'full pack'	SOT186A

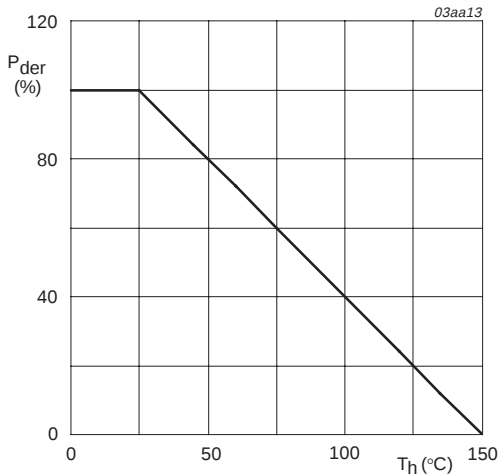
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

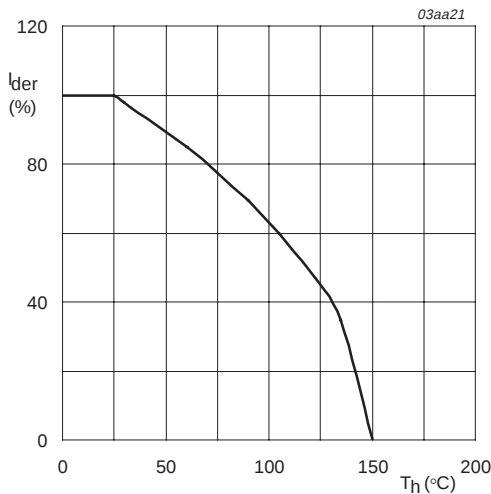
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	55	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_h = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	[1] -	12.9	A
		$T_h = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	[1] -	8.1	A
I_{DM}	peak drain current	$T_h = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	[1]	51.6	A
P_{tot}	total power dissipation	$T_h = 25\text{ °C}$; Figure 1	[1] -	23	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_h = 25\text{ °C}$	[1] -	12.9	A
I_{SM}	peak source (diode forward) current	$T_h = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	[1] -	51.6	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 11\text{ A}$; $t_p = 0.06\text{ ms}$; $V_{DD} \leq 15\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting $T_j = 25\text{ °C}$	-	30.3	mJ

[1] External heatsink connected to mounting base.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

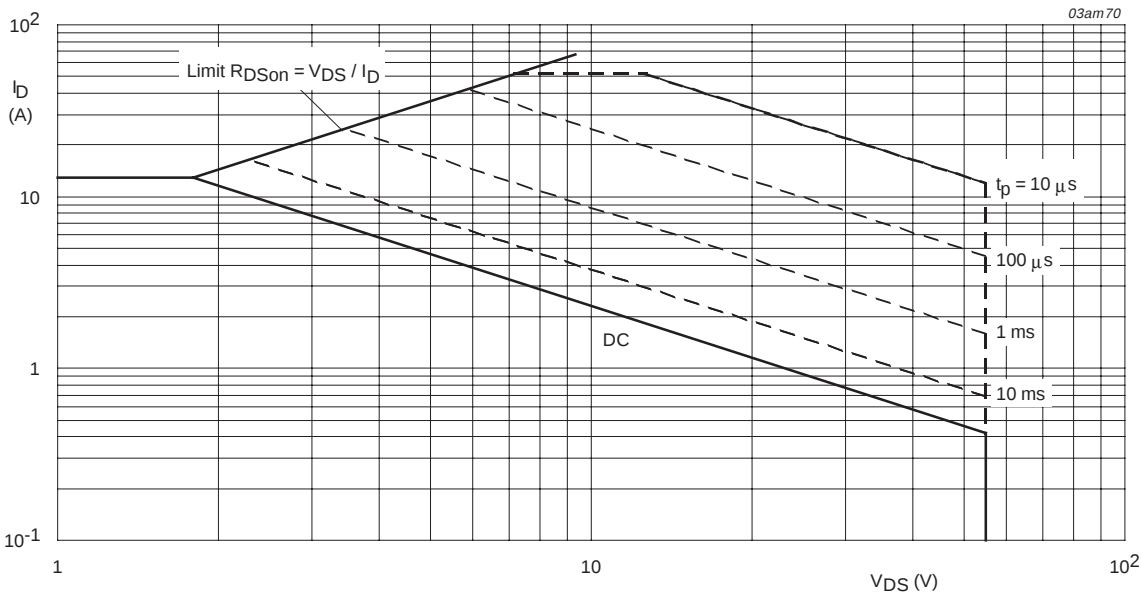
Fig 1. Normalized total power dissipation as a function of heatsink temperature.



$V_{GS} \geq 10\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of heatsink temperature.



$T_h = 25\text{ }^{\circ}\text{C}$; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

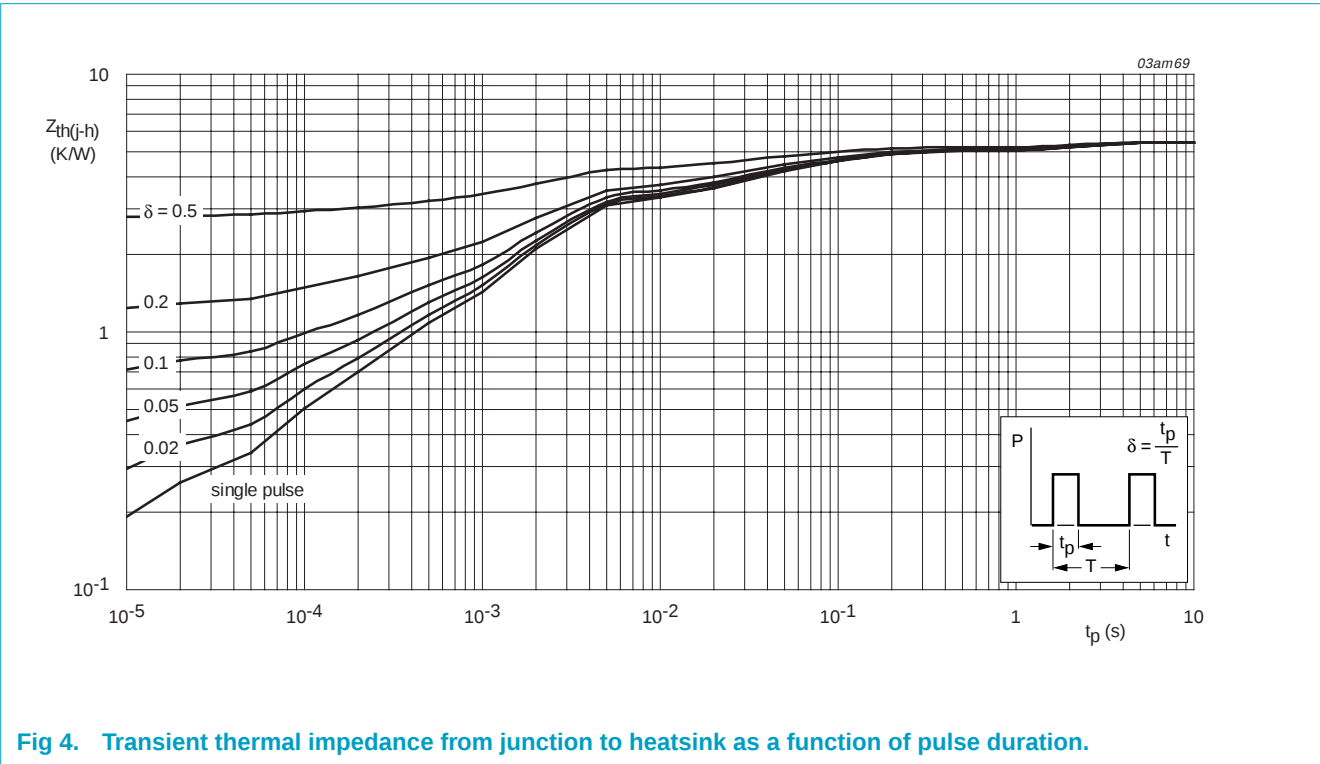
5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink.	Figure 4	[1]	-	-	5.4 K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient.	vertical in still air	-	55	-	K/W

[1] External heatsink connected to mounting base.

5.1 Transient thermal impedance

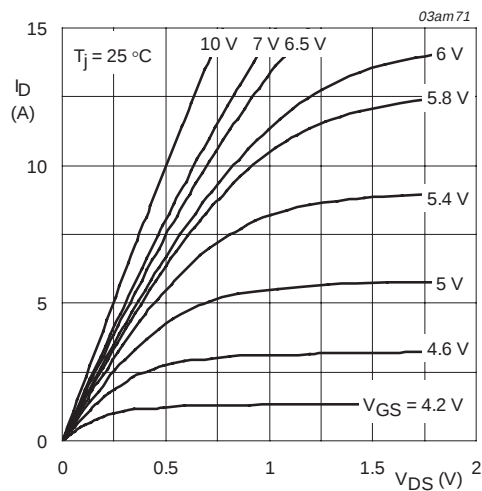


6. Characteristics

Table 5: Characteristics

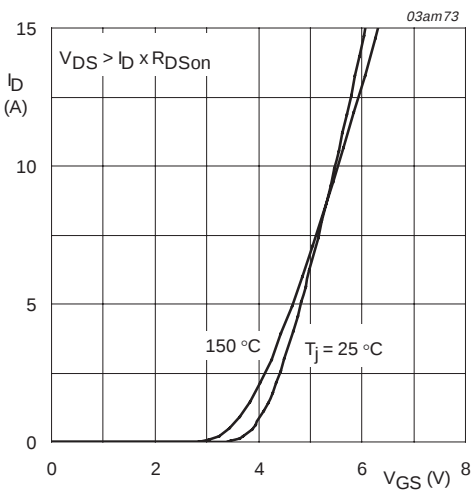
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	55	-	-	V
		$T_j = -55\text{ °C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 150\text{ °C}$	1.2	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 55\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.05	10	μA
		$T_j = 150\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	50	75	m Ω
		$T_j = 150\text{ °C}$	-	75	138	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 10\text{ A}$; $V_{DD} = 44\text{ V}$; $V_{GS} = 10\text{ V}$; Figure 13	-	9.8	-	nC
Q_{gs}	gate-source charge		-	2.2	-	nC
Q_{gd}	gate-drain (Miller) charge		-	4.7	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; Figure 11	-	320	-	pF
C_{oss}	output capacitance		-	90	-	pF
C_{rss}	reverse transfer capacitance		-	60	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\text{ V}$; $R_L = 1.2\text{ }\Omega$;	-	10	-	ns
t_r	rise time	$V_{GS} = 10\text{ V}$; $R_G = 10\text{ }\Omega$;	-	50	-	ns
$t_{d(off)}$	turn-off delay time		-	70	-	ns
t_f	fall time		-	40	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 15\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	-	1.02	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$;	-	32	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$	-	120	-	nC



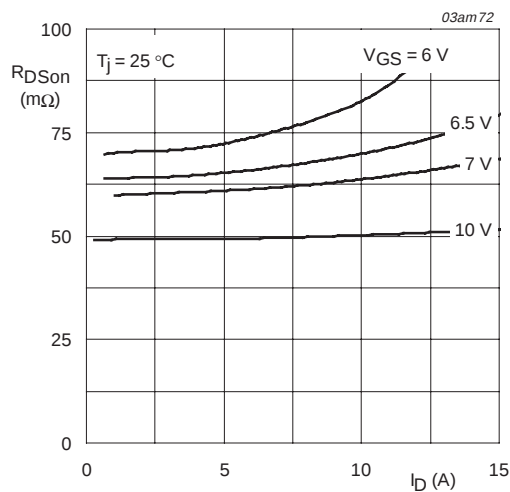
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



$T_j = 25\text{ °C}$ and 150 °C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$T_j = 25\text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.

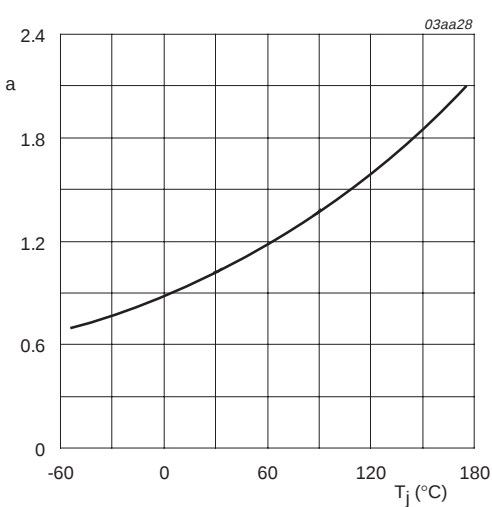
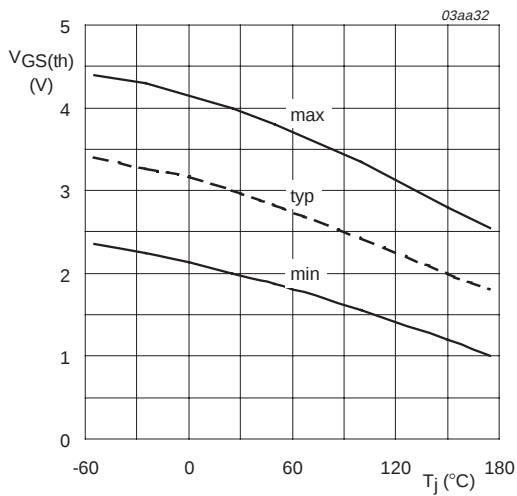
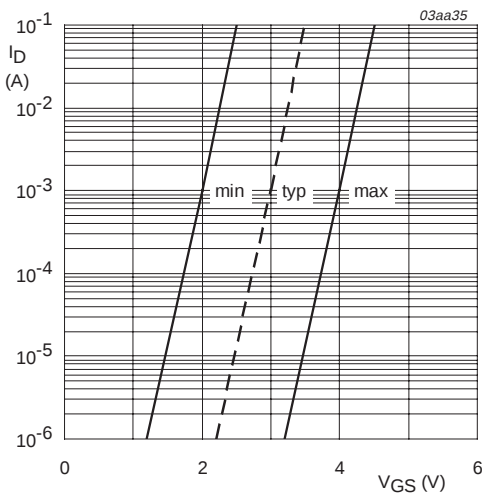


Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



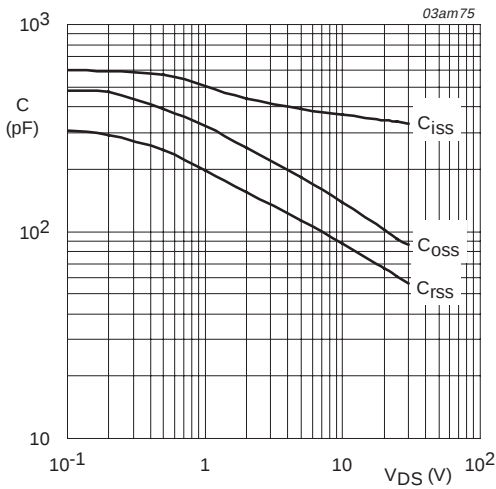
$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



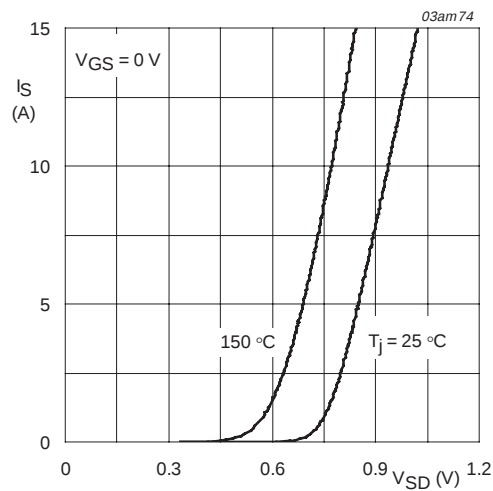
$T_j = 25\text{ °C}$; $V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



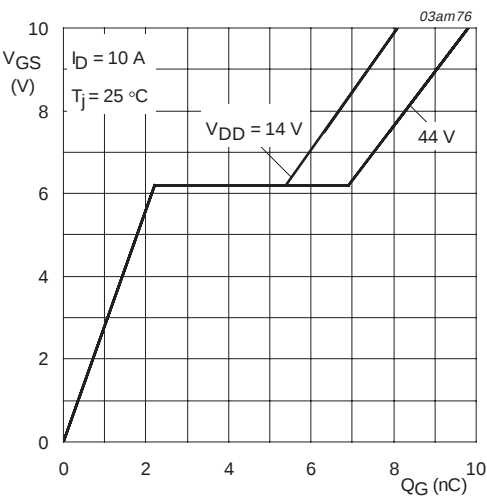
$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$V_{GS} = 0$ V

Fig 12. Reverse diode current as a function of reverse diode voltage; typical values.



$I_D = 10$ A; $V_{DD} = 14$ V and 44 V

Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values.

7. Isolation characteristics

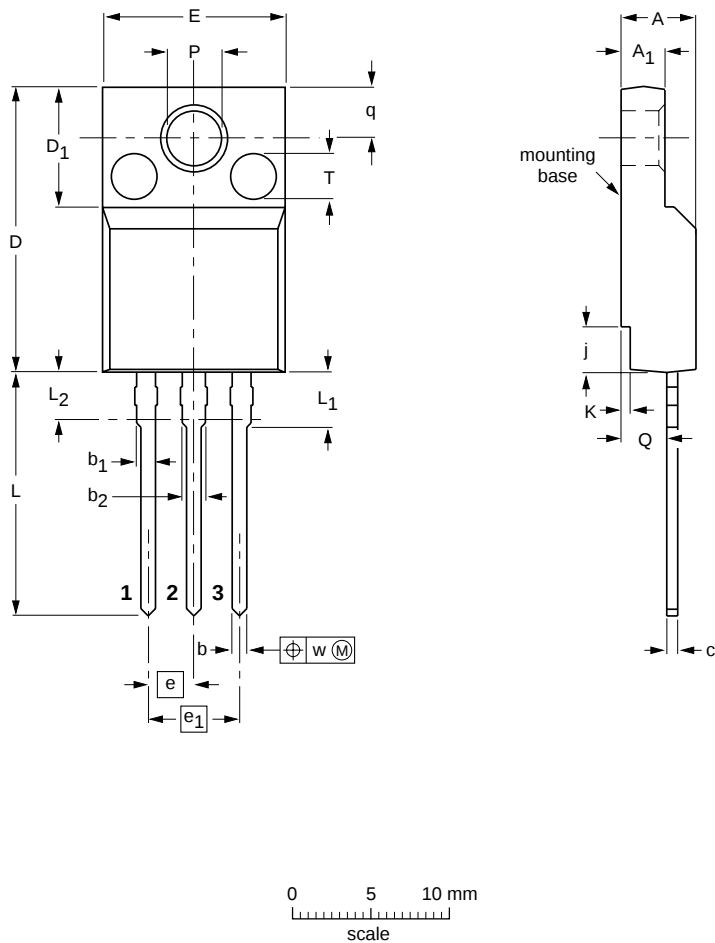
Table 6: Isolation characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{(isol)RMS}$	RMS isolation voltage from all three terminals to external heatsink	$f = 50\text{-}60$ Hz; sinusoidal waveform; $RH \leq 65$ %; clean and dust-free.	-	-	2500	V
$C_{(d-h)}$	Capacitance from drain to external heatsink		-	10	-	pF

8. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3 lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	b ₂	c	D	D ₁	E	e	e ₁	j	K	L	L ₁	L ₂ ⁽¹⁾ max.	P	Q	q	T ⁽²⁾	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

- 1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
- 2. Both recesses are $\varnothing 2.5 \times 0.8$ max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				02-03-12 02-04-09

Fig 14. SOT186A (TO-220F).

9. Revision history

Table 7: Revision history

Rev	Date	CPCN	Description
01	20040216	-	Product data (9397 750 12834).

10. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

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