

NTZD3156C

Small Signal MOSFET

20 V, 540 mA / -20 V, -430 mA

Complementary N- and P-Channel
MOSFETs with Integrated Pull Up/Down
Resistor and ESD Protection

Features

- Leading Trench Technology for Low $R_{DS(on)}$ Performance
- High Efficiency System Performance
- Low Threshold Voltage
- Integrated G-S Resistor on Both Devices
- ESD Protected Gate
- Small Footprint 1.6 x 1.6 mm
- These are Pb-Free Devices

Applications

- Load/Power Switching with Level Shift
- Portable Electronic Products such as GPS, Cell Phones, DSC, PMP, Bluetooth Accessories

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	20	V
Gate-to-Source Voltage			V_{GS}	± 6	V
N-Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	540	mA
		$T_A = 85^{\circ}\text{C}$		390	
	$t \leq 5\text{ s}$	$T_A = 25^{\circ}\text{C}$		570	
P-Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$		-430	
		$T_A = 85^{\circ}\text{C}$		-310	
	$t \leq 5\text{ s}$	$T_A = 25^{\circ}\text{C}$		-455	
Power Dissipation (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	P_D	250	mW
				$t \leq 5\text{ s}$	
Pulsed Drain Current	N-Channel	$t_p = 10\text{ }\mu\text{s}$	I_{DM}	1500	mA
	P-Channel			-750	
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	350	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq [1 oz] including traces).

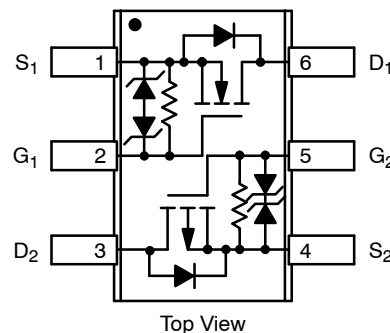


ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max (Note 1)
N-Channel 20 V	0.55 Ω @ 4.5 V	540 mA
	0.7 Ω @ 2.5 V	
	0.9 Ω @ 1.8 V	
P-Channel -20 V	0.9 Ω @ -4.5 V	-430 mA
	1.2 Ω @ -2.5 V	
	2.0 Ω @ -1.8 V	

PINOUT: SOT-563



SOT-563-6
CASE 463A
STYLE 9

MARKING DIAGRAM



ZC = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTZD3156CT1G	SOT-563	4000 / Tape & Reel
NTZD3156CT2G	SOT-563	4000 / Tape & Reel
NTZD3156CT5G	SOT-563	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTZD3156C

Thermal Resistance Ratings

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	116	°C/W
Junction-to-Ambient – $t = 5$ s (Note 2)		304	

2. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	N/P	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	N	$V_{GS} = 0\text{ V}$	$I_D = 250\text{ }\mu\text{A}$	20		V
		P		$I_D = -250\text{ }\mu\text{A}$	-20		
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				20		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	N	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
		P	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$			-1.0	
		N	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}$	$T_J = 125^\circ\text{C}$		2.0	μA
		P	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$			-5.0	
Gate-to-Source Leakage Current	I_{GSS}	N	$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			± 50	μA
		P				± 50	

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	N	$V_{GS} = V_{DS}$	$I_D = 250\text{ }\mu\text{A}$	0.45	1.0	V
		P		$I_D = -250\text{ }\mu\text{A}$	-0.45	-1.0	
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				2.0		-mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	N	$V_{GS} = 4.5\text{ V}, I_D = 540\text{ mA}$		0.19	0.55	Ω
		P	$V_{GS} = -4.5\text{ V}, I_D = -430\text{ mA}$		0.39	0.9	
		N	$V_{GS} = 2.5\text{ V}, I_D = 500\text{ mA}$		0.26	0.7	
		P	$V_{GS} = -2.5\text{ V}, I_D = -300\text{ mA}$		0.53	1.2	
		N	$V_{GS} = 1.8\text{ V}, I_D = 350\text{ mA}$		0.36	0.9	
		P	$V_{GS} = -1.8\text{ V}, I_D = -150\text{ mA}$		0.72	2.0	
Forward Transconductance	g_{FS}	N	$V_{DS} = 10\text{ V}, I_D = 540\text{ mA}$		1.46		S
		P	$V_{DS} = -10\text{ V}, I_D = -430\text{ mA}$		1.18		

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	N	$f = 1\text{ MHz}, V_{GS} = 0\text{ V}$ $V_{DS} = 16\text{ V}$		72		pF
Output Capacitance	C_{OSS}				13		
Reverse Transfer Capacitance	C_{RSS}				10		
Input Capacitance	C_{ISS}	P	$f = 1\text{ MHz}, V_{GS} = 0\text{ V}$ $V_{DS} = -16\text{ V}$		93		
Output Capacitance	C_{OSS}				15		
Reverse Transfer Capacitance	C_{RSS}				11		

3. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

NTZD3156C

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	N/P	Test Condition	Min	Typ	Max	Unit
-----------	--------	-----	----------------	-----	-----	-----	------

CHARGES, CAPACITANCES AND GATE RESISTANCE

Total Gate Charge	$Q_{G(TOT)}$	N	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}; I_D = 540\text{ mA}$		1.39	2.5	nC
Threshold Gate Charge	$Q_{G(TH)}$				0.1		
Gate-to-Source Charge	Q_{GS}				0.26		
Gate-to-Drain Charge	Q_{GD}				0.39		
Total Gate Charge	$Q_{G(TOT)}$	P	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}; I_D = -430\text{ mA}$		1.49	2.5	
Threshold Gate Charge	$Q_{G(TH)}$				0.1		
Gate-to-Source Charge	Q_{GS}				0.3		
Gate-to-Drain Charge	Q_{GD}				0.37		

SWITCHING CHARACTERISTICS ($V_{GS} = V$) (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	N	$V_{GS} = 4.5\text{ V}, V_{DD} = 10\text{ V}, I_D = 540\text{ mA}, R_G = 10\ \Omega$		7.7		ns
Rise Time	t_r				5.3		
Turn-Off Delay Time	$t_{d(OFF)}$				21		
Fall Time	t_f				10		
Turn-On Delay Time	$t_{d(ON)}$	P	$V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V}, I_D = -430\text{ mA}, R_G = 10\ \Omega$		9.2		
Rise Time	t_r				6.5		
Turn-Off Delay Time	$t_{d(OFF)}$				29		
Fall Time	t_f				19.5		

Drain-Source Diode Characteristics

Forward Diode Voltage	V_{SD}	N	$V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	$I_S = 350\text{ mA}$		0.77	1.2	V
		P		$I_S = -350\text{ mA}$		-0.77	-1.2	
		N	$V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$	$I_S = 350\text{ mA}$		0.65		
		P		$I_S = -350\text{ mA}$		0.63		
Reverse Recovery Time	t_{RR}	N	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}$	$I_S = 350\text{ mA}$		9.4		ns
		P		$I_S = -350\text{ mA}$		14.6		

4. Switching characteristics are independent of operating junction temperatures

N-CHANNEL TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

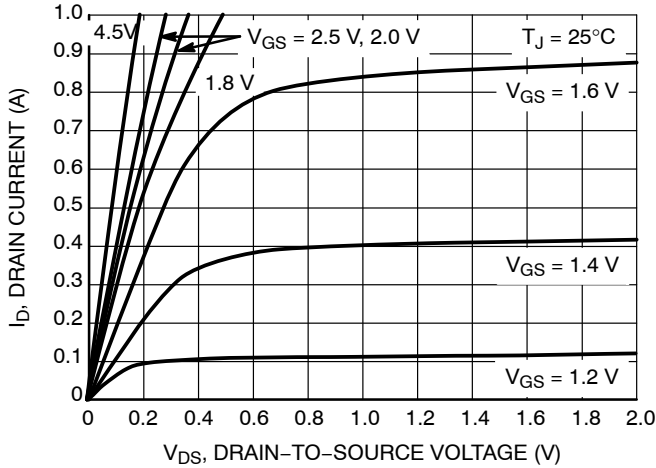


Figure 1. On-Region Characteristics

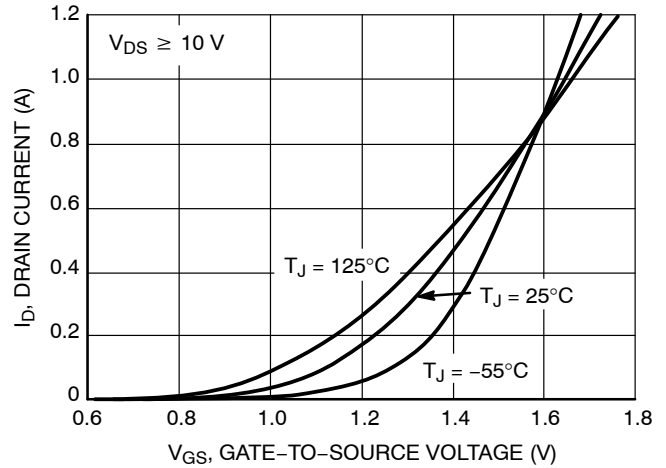


Figure 2. Transfer Characteristics

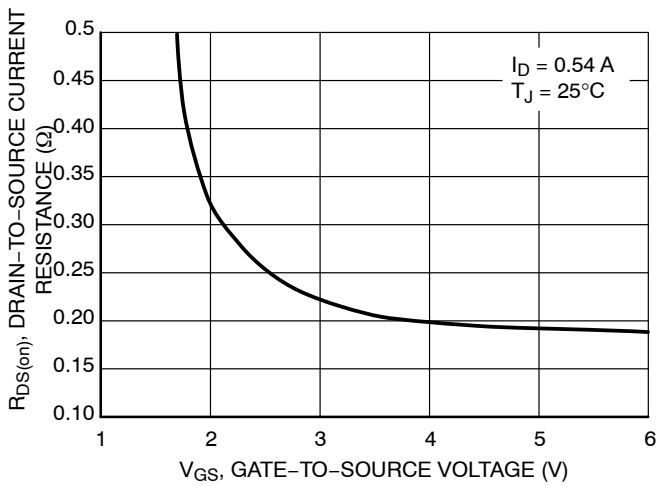


Figure 3. On-Resistance versus Gate-to-Source Voltage

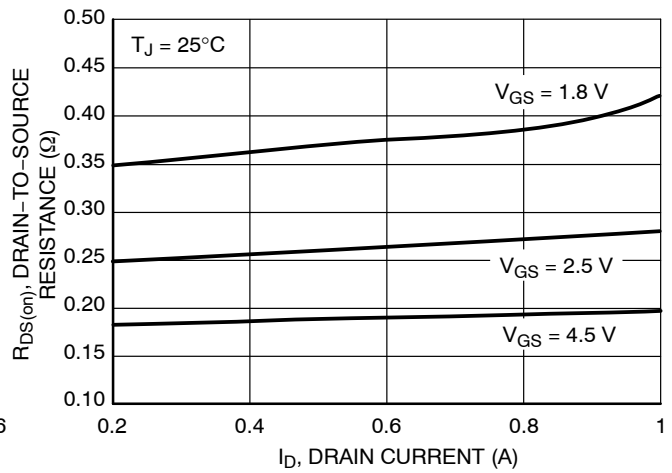


Figure 4. On-Resistance versus Drain Current and Gate Voltage

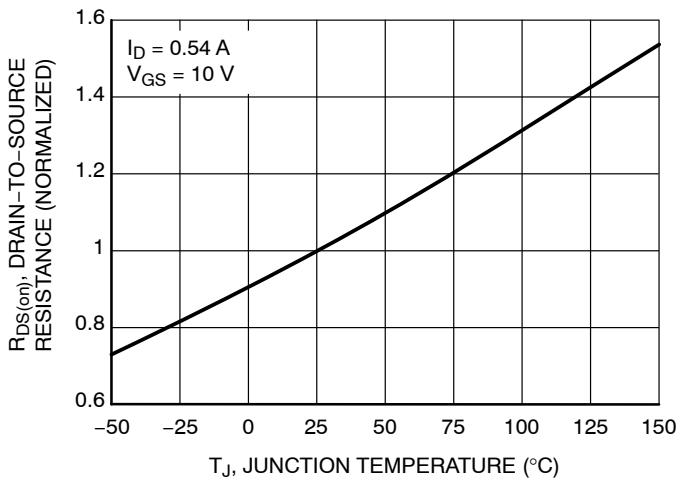


Figure 5. On-Resistance Variation with Temperature

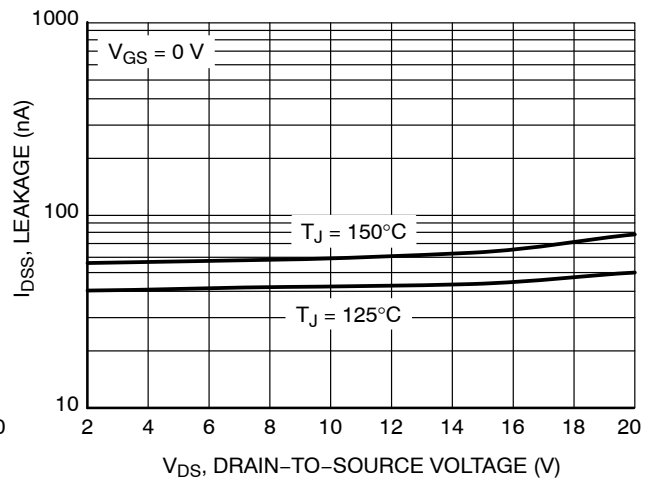


Figure 6. Drain-to-Source Leakage Current versus Voltage

N-CHANNEL TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

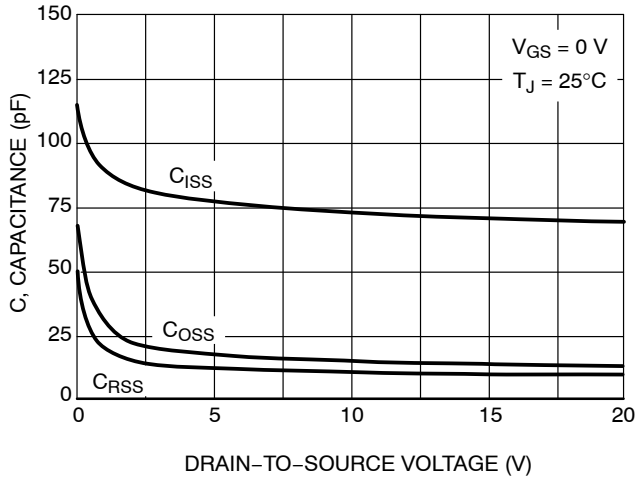


Figure 7. Capacitance Variation

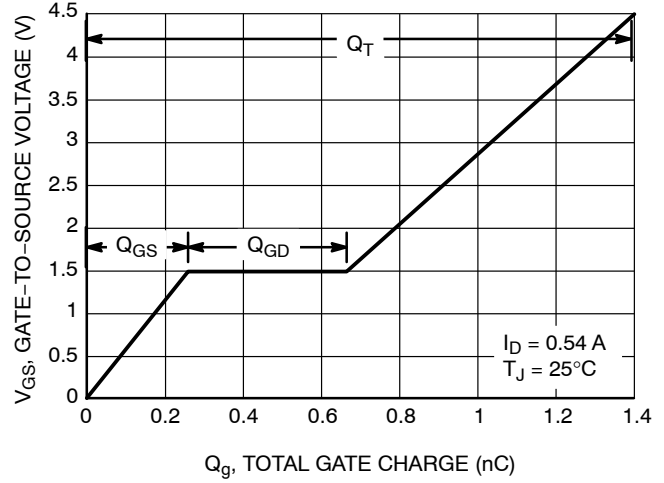


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

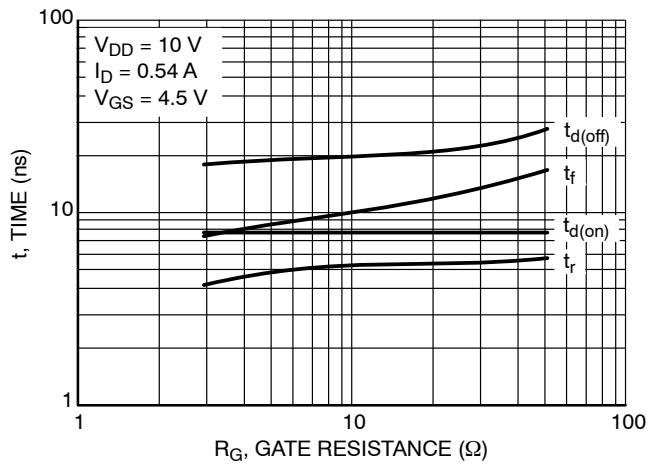


Figure 9. Resistive Switching Time Variation versus Gate Resistance

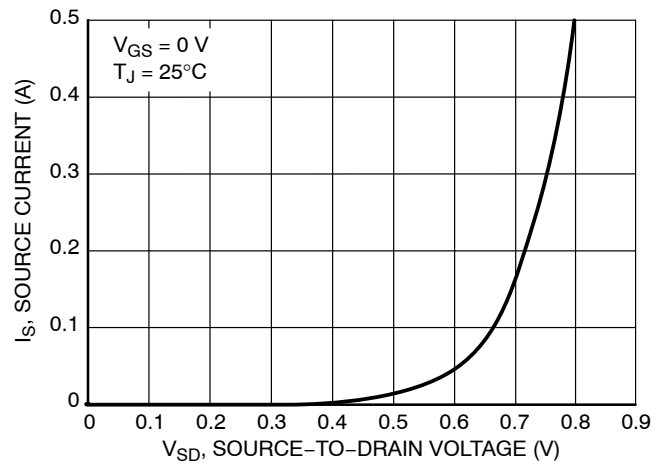


Figure 10. Diode Forward Voltage versus Current

P-CHANNEL TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

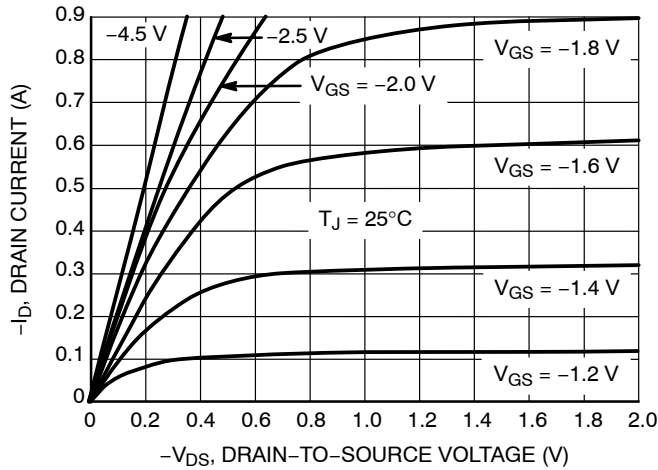


Figure 11. On-Region Characteristics

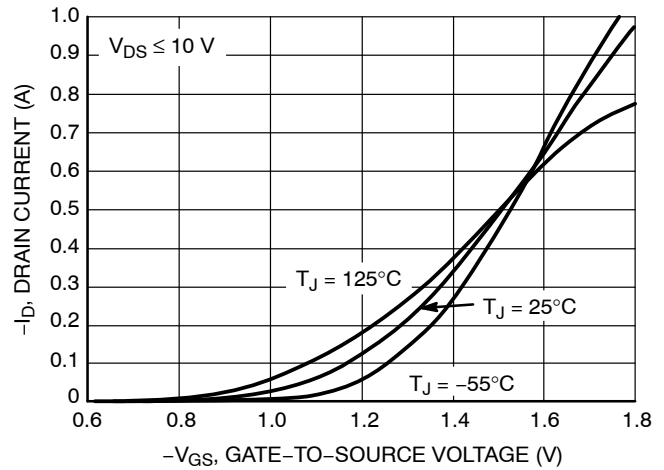


Figure 12. Transfer Characteristics

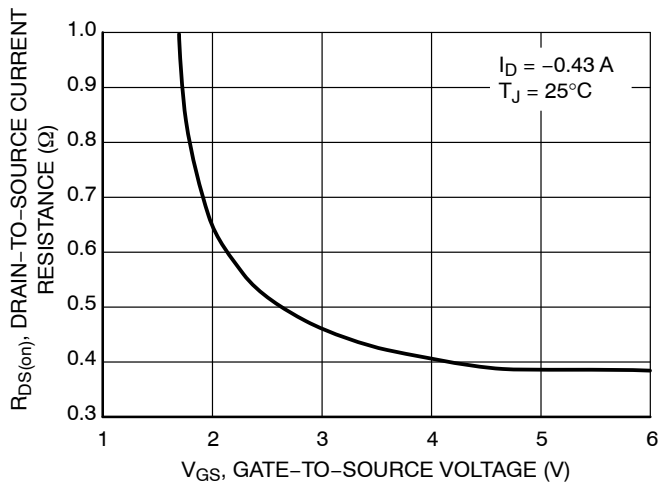


Figure 13. On-Resistance versus Gate-to-Source Voltage

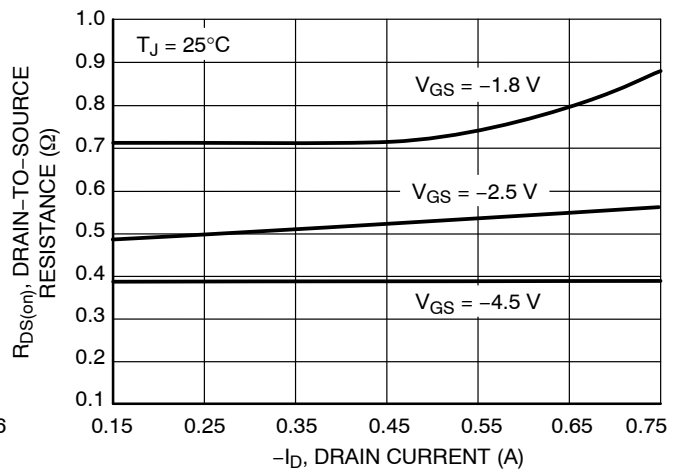


Figure 14. On-Resistance versus Drain Current and Gate Voltage

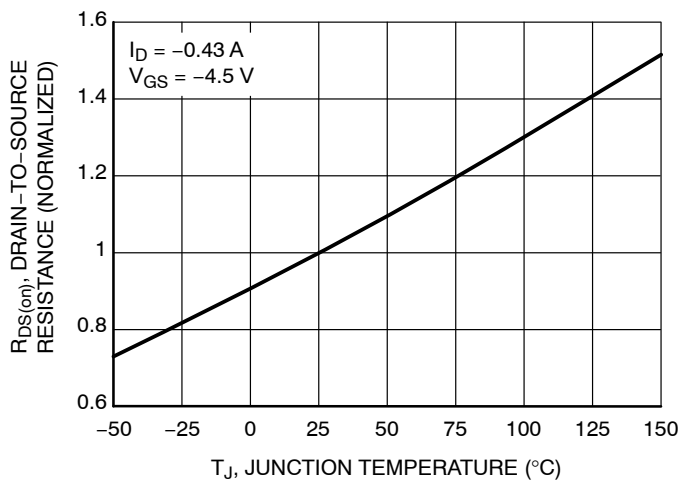


Figure 15. On-Resistance Variation with Temperature

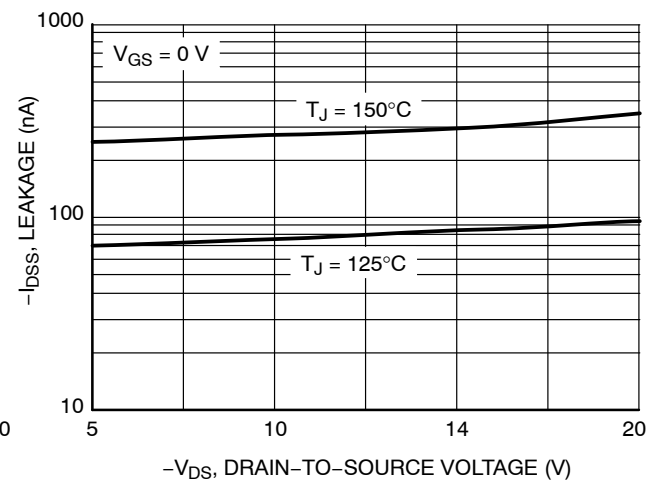


Figure 16. Drain-to-Source Leakage Current versus Voltage

P-CHANNEL TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

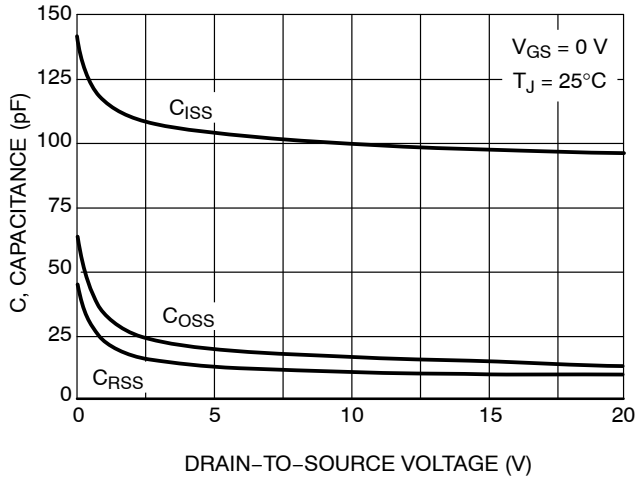


Figure 17. Capacitance Variation

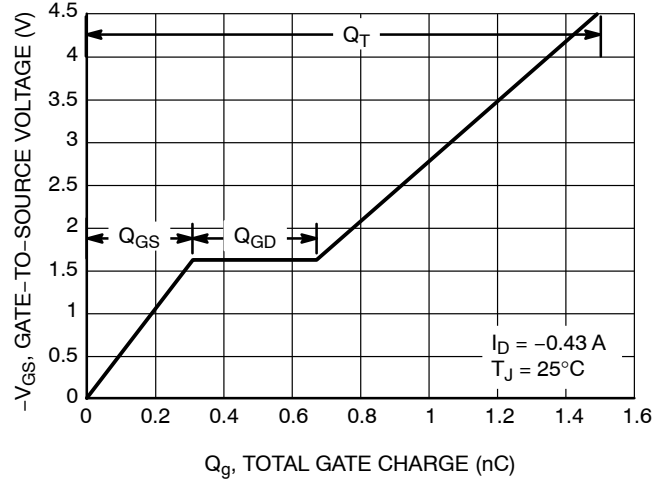


Figure 18. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

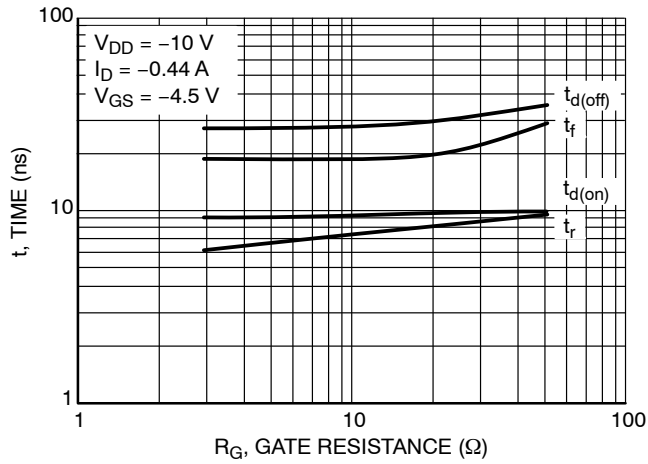


Figure 19. Resistive Switching Time Variation versus Gate Resistance

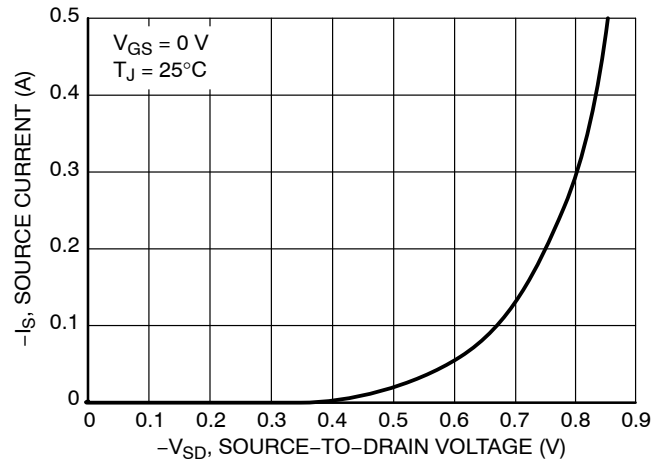
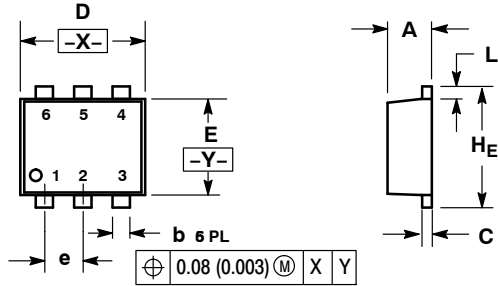


Figure 20. Diode Forward Voltage versus Current

NTZD3156C

PACKAGE DIMENSIONS

SOT-563, 6 LEAD CASE 463A-01 ISSUE F



NOTES:

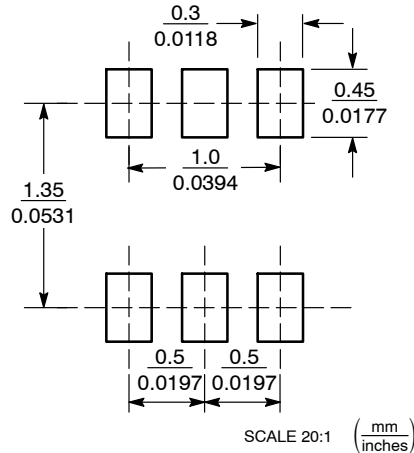
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H _E	1.50	1.60	1.70	0.059	0.062	0.066

STYLE 9:

- PIN 1. SOURCE 1
- GATE 1
- DRAIN 2
- SOURCE 2
- GATE 2
- DRAIN 1

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative