

NUP3115UPMU

Transient Voltage Suppressors

Low Capacitance ESD Protection for High Speed Data

The three-line voltage transient suppressor array is designed to protect voltage-sensitive components that require ultra-low capacitance from ESD and transient voltage events. This device features a common anode design which protects three independent high speed data lines and a V_{CC} power line in a single six-lead UDFN low profile package.

Excellent clamping capability, low capacitance, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as a USB 2.0 high speed.

Features

- Low Capacitance 0.8 pF
- UDFN Package, 1.6 x 1.6 mm
- Low Profile of 0.50 mm for Ultra Slim Design
- Stand Off Voltage: 5.5 V
- Low Leakage
- Protects up to Three Data Lines Plus a V_{CC} Pin
- V_{CC} Pin = 15 V Protection
- D_1 , D_2 , and D_3 Pins = 6.4 V Minimum Protection
- IEC61000-4-2: Level 4 ESD Protection
- This is a Pb-Free Device

Typical Applications

- USB 2.0 High-Speed Interface
- Cell Phones
- MP3 Players
- SIM Card Protection

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Rating	Value	Unit
I_{PK}	Peak Pulse Current V_{CC} Diode 8x20 μsec double exponential waveform	5.0	A
T_J	Operating Junction Temperature Range	-40 to 125	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Solder Temperature – Maximum (10 seconds)	260	$^\circ\text{C}$
ESD	IEC 61000-4-2 Contact	8000	V

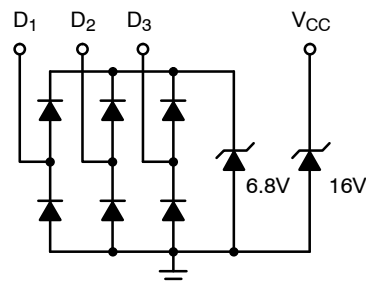
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

See Application Note AND8308/D for further description of survivability specs.



ON Semiconductor®

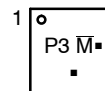
<http://onsemi.com>



MARKING DIAGRAM



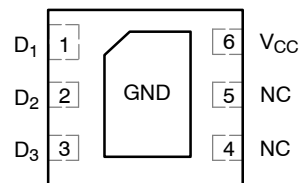
UDFN6 1.6x1.6
MU SUFFIX
CASE 517AP



P3 = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NUP3115UPMUTAG	UDFN6 (Pb-Free)	3000/Tape & Reel

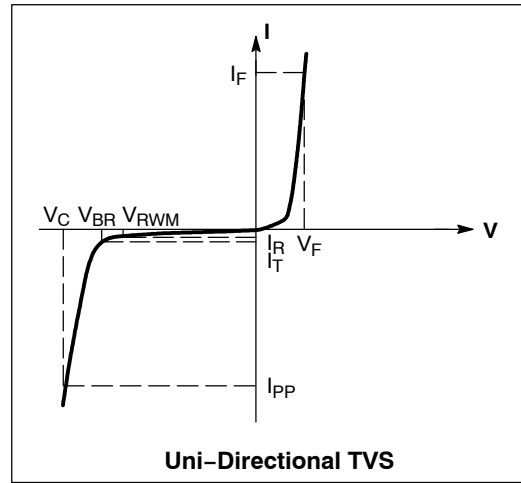
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I _{PP}	Maximum Reverse Peak Pulse Current
V _C	Clamping Voltage @ I _{PP}
V _{RWM}	Working Peak Reverse Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V _{BR}	Breakdown Voltage @ I _T
I _T	Test Current
I _F	Forward Current
V _F	Forward Voltage @ I _F
P _{pk}	Peak Power Dissipation
C	Max. Capacitance @ V _R = 0 and f = 1.0 MHz

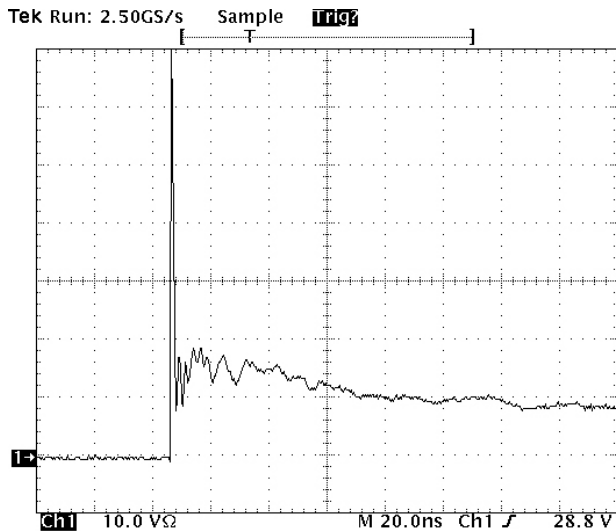
*See Application Note AND8308/D for detailed explanations of datasheet parameters.



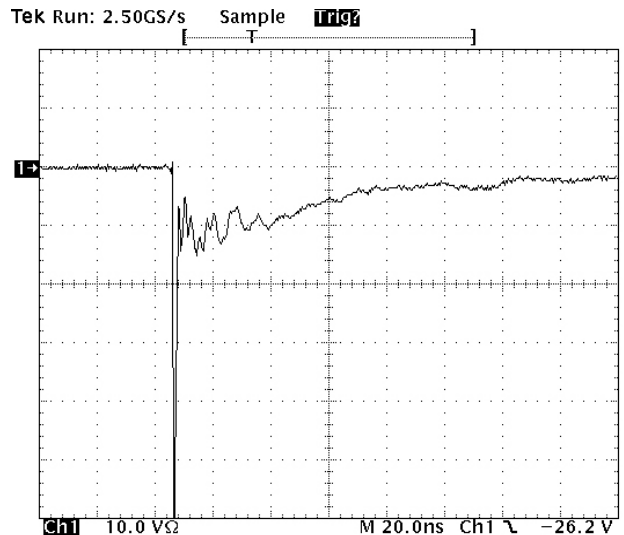
ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Reverse Working Voltage (D ₁ , D ₂ , and D ₃)	(Note 1)	V _{RWM1}	–	–	5.5	V
Reverse Working Voltage (V _{CC})	(Note 1)	V _{RWM2}	–	–	12	V
Breakdown Voltage (D ₁ , D ₂ , and D ₃)	I _T = 1 mA, (Note 2)	V _{BR}	6.4	6.8	8.0	V
Breakdown Voltage (V _{CC})	I _T = 1 mA, (Note 2)	V _{BR2}	15	16	16.8	V
Reverse Leakage Current (D ₁ , D ₂ , and D ₃)	@ V _{RWM1}	I _R	–	–	1.0	μA
Reverse Leakage Current (D ₁ , D ₂ , and D ₃)	@ 3.3 V	I _R	–	–	85	nA
Reverse Leakage Current (V _{CC})	@ V _{RWM2}	I _R	–	–	1.0	μA
Clamping Voltage (D ₁ , D ₂ , and D ₃)	I _{PP} = 1 A	V _C	–	9.4	–	V
Clamping Voltage (V _{CC})	I _{PP} = 1 A	V _C	–	18.5	–	V
Clamping Voltage (V _{CC})	I _{PP} = 3 A	V _C	–	22	–	V
Junction Capacitance (D ₁ , D ₂ , and D ₃)	V _R = 0 V, f = 1 MHz (Line to GND)	C _J	–	0.8	1.0	pF
Clamping Voltage	Per IEC 61000–4–2 (Note 4)	V _C	Figure 1 and 2			V

1. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
2. V_{BR} is measured at pulse test current I_T.
3. Surge current waveform per Figure 5.
4. Typical waveform. For test procedure see Figures 3 and 4 and Application Note AND8307/D.



**Figure 1. ESD Clamping Voltage Screenshot
Positive 8 kV Contact per IEC61000–4–2**



**Figure 2. ESD Clamping Voltage Screenshot
Negative 8 kV Contact per IEC61000–4–2**

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

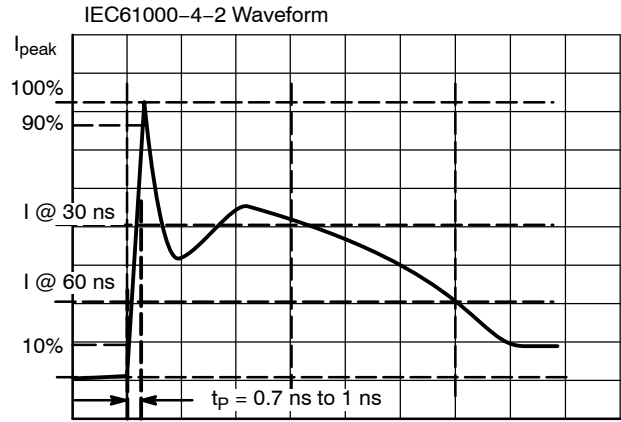


Figure 3. IEC61000-4-2 Spec

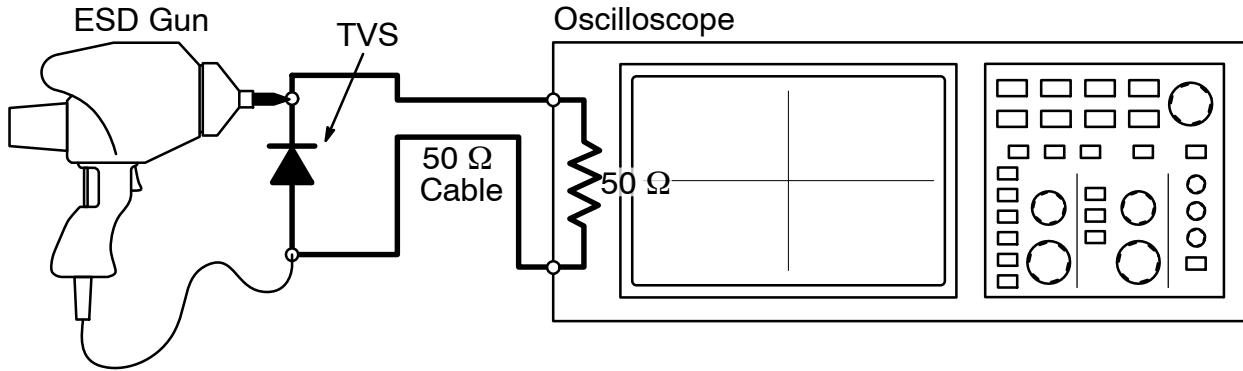


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

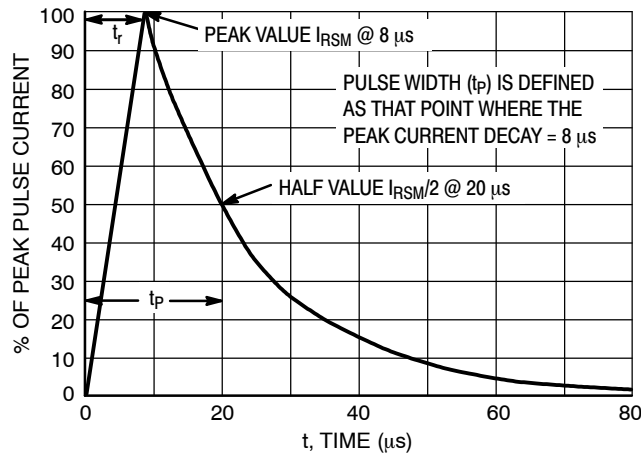
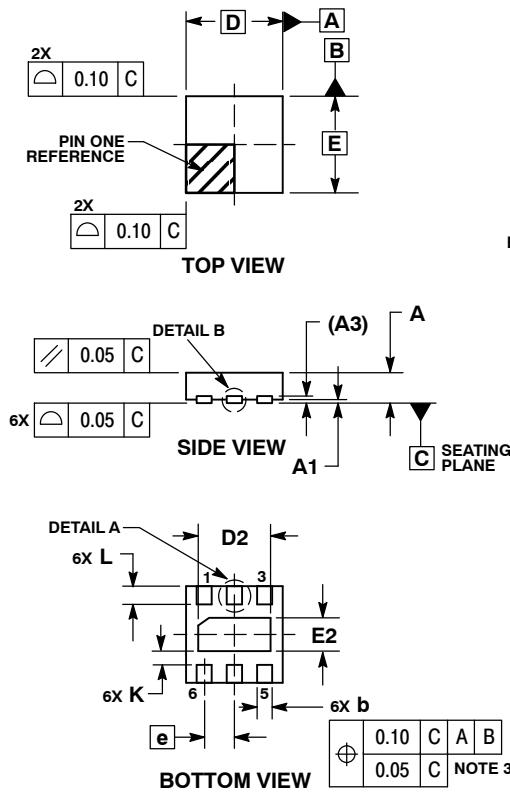


Figure 5. 8 X 20 μ s Pulse Waveform

NUP3115UPMU

PACKAGE DIMENSIONS

UDFN6, 1.6x1.6, 0.5P
CASE 517AP-01
ISSUE O

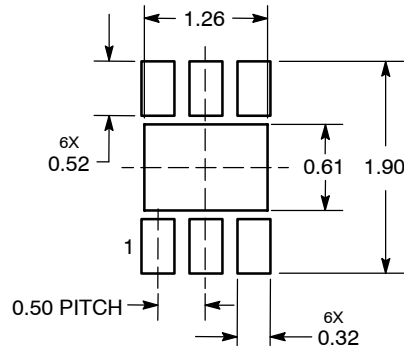


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.20	0.30
D	1.60	BSC
E	1.60	BSC
e	0.50	BSC
D2	1.10	1.30
E2	0.45	0.65
K	0.20	---
L	0.20	0.40
L1	0.00	0.15

SOLDERMASK DEFINED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative