VIV0005TFJ

VTM™ DC to DC Voltage Transformer

FEATURES

- 40 Vdc to 1 Vdc 130 A Voltage Transformer
  - Operating from standard 48 V or 24 V PRM™ regulators
- 150 A rated with reduced case temperature at 30°C
- High efficiency (>91%) reduces system power consumption
- High density (117 A/in²)
- "Full Chip" V•I Chip package enables surface mount, low impedance interconnect to system board
- Contains built-in protection features:
  - Overvoltage Lockout
  - Overcurrent
  - Short Circuit
  - Over Temperature
- Provides enable / disable control, internal temperature monitoring, current monitoring
- ZVS / ZCS resonant Sine Amplitude Converter topology
- Less than 50°C temperature rise at full load in typical applications

TYPICAL APPLICATION

- High End Computing Systems
- Automated Test Equipment
- High Density Power Supplies

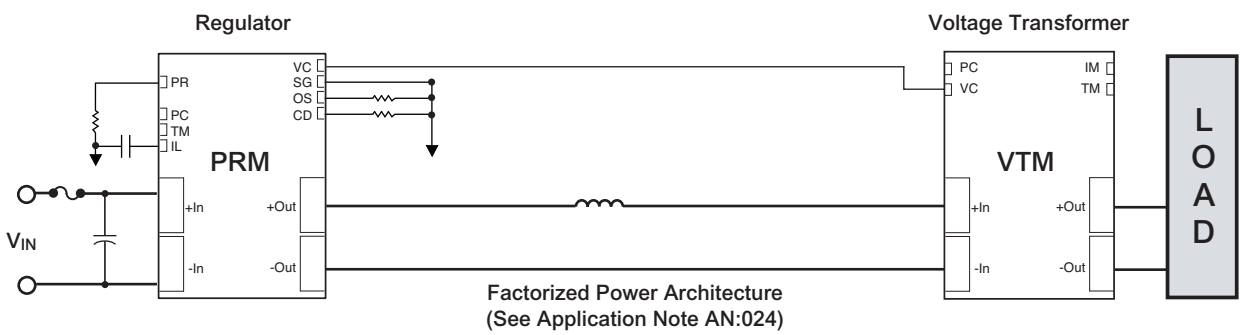
DESCRIPTION

The V•I Chip Voltage Transformer is a high efficiency (>91%) Sine Amplitude Converter (SAC)™ operating from a 26 to 55 Vdc primary bus to deliver an isolated output. The Sine Amplitude Converter offers a low AC impedance beyond the bandwidth of most downstream regulators, which means that capacitance normally at the load can be located at the input to the Sine Amplitude Converter. Since the K factor of the VIV0005TFJ is 1/40, that capacitance value can be reduced by a factor of 1600, resulting in savings of board area, materials and total system cost.

The VIV0005TFJ is provided in a V•I Chip package compatible with standard pick-and-place and surface mount assembly processes. The co-molded V•I Chip package provides enhanced thermal management due to large thermal interface area and superior thermal conductivity. With high conversion efficiency the VIV0005TFJ increases overall system efficiency and lowers operating costs compared to conventional approaches.
The VIV0005TFJ enables the utilization of Factorized Power Architecture™ providing efficiency and size benefits by lowering conversion and distribution losses and promoting high density point of load conversion.

V_{IN} = 26 to 55 V	I_{OUT} = 130 A (NOM)
V_{OUT} = 0.65 to 1.37 V (NO LOAD)	K = 1/40

PART NUMBER	DESCRIPTION
VIV0005TFJ	-40°C to 125°C T_J



1.0 ABSOLUTE MAXIMUM VOLTAGE RATINGS

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

	MIN	MAX	UNIT
+ IN to - IN	-1	60	V_{DC}
PC to - IN	-0.3	20	V_{DC}
TM to -IN	-0.3	7	V_{DC}
VC to - IN	-0.3	20	V_{DC}

	MIN	MAX	UNIT
IM to - IN	0	3.15	V_{DC}
+ IN / - IN to + OUT / - OUT (hipot)		100	V_{DC}
+ IN / - IN to + OUT / - OUT (working)		60	V_{DC}
+ OUT to - OUT	-1	5.5	V_{DC}

2.0 ELECTRICAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T_J < 125°C (T-Grade)**; All other specifications are at **T_J = 25°C** unless otherwise noted.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	No external VC applied	**26**		**55**	V_{DC}
		VC applied	**0**		**55**	
V_{IN} Slew Rate	dV_{IN}/dt				**1**	V/µs
V_{IN} UV Turn Off	V_{IN_UV}	Module latched shutdown, No external VC applied, I_{OUT} = 130A		18	**26**	V
No Load Power Dissipation	P_{NL}	V_{IN} = 40 V	**2**		**6.3**	W
		V_{IN} = 26 V to 55 V			**7.5**	
		V_{IN} = 40 V, T_C = 25°C		3.2	4.5	
		V_{IN} = 26 V to 55 V, T_C = 25°C			6	
DC Input Current	I_{IN_DC}				**4**	A
Transfer Ratio	K	K = V_{OUT}/V_{IN}, I_{OUT} = 0 A		**1/40**		V/V
Output Voltage	V_{OUT}	$V_{OUT} = V_{IN} \cdot K - I_{OUT} \cdot R_{OUT}$, Section 11				V
Output Current (Average)	I_{OUT_AVG}	30°C < T_C < 100°C, I_{OUT_MAX} = - (2/7) * T_C + 159			**130**	A
		T_C = 30°C			150	
Output Current (Peak)	I_{OUT_PK}	T_{PEAK} <10 ms, $I_{OUT\_AVG} \leq$ 130 A			**195**	A
Output Power (Average)	P_{OUT_AVG}	$I_{OUT\_AVG} \leq$ 130 A			**178**	W
Efficiency (Ambient)	η_{AMB}	V_{IN} = 40 V, I_{OUT} = 130 A	87.5	89.2		%
		V_{IN} = 26 V to 55 V, I_{OUT} = 130 A	81.7			
		V_{IN} = 40 V, I_{OUT} = 65 A	89.1	91		
		V_{IN} = 40 V, I_{OUT} = 150 A	86.2	88.2		
Efficiency (Hot)	η_{HOT}	V_{IN} = 40 V, T_c = 100°C, I_{OUT} = 130 A	85.1	87.5		%
Efficiency (Over Load Range)	$\eta_{20\%}$	26 A < I_{OUT} < 130 A	**78**			%
Output Resistance (Cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 130 A	0.45	0.575	0.75	mΩ
Output Resistance (Ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 130 A	0.55	0.668	0.87	mΩ
Output Resistance (Hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 130 A	0.7	0.82	1.02	mΩ
Switching Frequency	F_{SW}		**1.53**	1.61	**1.67**	MHz
Output Ripple Frequency	F_{SW_RP}		**3.06**	3.22	**3.34**	MHz
Output Voltage Ripple	V_{OUT_PP}	C_{OUT} = 0 F, I_{OUT} = 130 A, V_{IN} = 40 V, 20 MHz BW, Section 12		125	**150**	mV
Output Inductance (Parasitic)	L_{OUT_PAR}	Frequency up to 30 MHz, Simulated J-lead model		150		pH
Output Capacitance (Internal)	C_{OUT_INT}			360		µF
PROTECTION						
OVLO	V_{IN_OVLO+}	Module latched shutdown	55.01	57.5	59.99	V
Overvoltage Lockout Response Time	T_{OVLO}	Effective internal RC filter		0.24		µs
Output Overcurrent Trip	I_{OCP}		165	200	275	A
Short Circuit Protection Trip Current	I_{SCP}		275			A
Output Overcurrent Response Time Constant	T_{OCP}	Effective internal RC filter (Integrative).		7.13		ms
Short Circuit Protection Response Time	T_{SCP}	From detection to cessation of switching (Instantaneous)		2		µs
Thermal Shutdown Setpoint	T_{J_OTP}		125	130	135	°C

3.0 SIGNAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T_J < 125°C (T-Grade)**; All other specifications are at **T_J = 25°C** unless otherwise noted.

VTM CONTROL : VC

- Used to wake up powertrain circuit.
- A minimum of 11.5 V must be applied indefinitely for V_{IN} < 26 V to ensure normal operation.
- VC slew rate must be within range for a succesful start.
- PRM VC can be used as valid wake-up signal source.
- VC voltage may be continuously applied; there will be no VC current drawn when V_{IN} > 26 V.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Steady	External VC Voltage	V_{VC_EXT}	Required for startup, and operation below 26 V. See Section 7.	**11.5**		**16.5**	V
		VC Current Draw	I_{VC}	VC = 11.5 V, V_{IN} = 0 V		100	**150**	mA
				VC = 11.5 V, V_{IN} > 26 V	**0**	**0**	**0**	
				Fault mode. VC > 11.5 V		**60**		
	Start Up	VC Slew Rate	dVC/dt	Required for proper startup; 0 °C < T_C < 100 °C	**0.001**		**0.25**	V/µs
				Required for proper startup; -40 °C < T_C < 100 °C	**0.0025**		**0.25**	
		VC Inrush Current	I_{INR_VC}	VC = 16.5 V, dVC/dt = 0.25 V/µs			**250**	mA
	Transitional	VC to PC Delay	T_{VC_PC}	VC = 11.5 V to PC high, V_{IN} = 0 V, dVC/dt = 0.25 V/µs		75	**125**	µs
		Internal VC Capacitance	C_{VC_INT}	VC = 0 V		1		µF

PRIMARY CONTROL : PC

- The PC pin enables and disables the VTM. When held below 2.0 V, the VTM will be disabled.
- PC pin outputs 5 V during normal operation. PC pin is equal to 2.5 V during fault mode given V_{IN} > 26 V and VC > 11.5 V.
- After successful start-up and under no fault condition, PC can be used as a 5 V regulated voltage source with a 2 mA maximum current.
- Module will shutdown when pulled low with an impedance less than 850 Ω.
- In an array of VTMs, connect PC pin to synchronize startup.
- PC pin can't sink current and will not disable other module during fault mode.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	PC Voltage	V_{PC}		**4.7**	**5**	**5.3**	V
		PC Source Current	I_{PC_OP}				**2**	mA
		PC Resistance (Internal)	R_{PC_INT}	Internal pull down resistor	**50**	150	**400**	kΩ
	Start Up	PC Source Current	I_{PC_EN}		**50**	100	**300**	µA
		PC Capacitance (Internal)	C_{PC_INT}	Section 7			**1000**	pF
		PC Resistance (External)	R_{PC_EXT}		**60**			kΩ
DIGITAL INPUT / OUPUT	Enable	PC Voltage	V_{PC_EN}		**2**	2.5	**3**	V
	Disable	PC Voltage (Disable)	V_{PC_DIS}				**2**	V
		PC Pull Down Current	I_{PC_PD}		**5.1**			mA
	Transitional	PC Disable Time	$T_{PC\_DIS\_T}$			5		µs
		PC Fault Response Time	T_{FR_PC}	From fault to PC = 2.0 V		100		µs

TEMPERATURE MONITOR : TM

- The TM pin monitors the internal temperature of the VTM controller IC within an accuracy of ±5°C.
- Can be used as a "Power Good" flag to verify that the VTM is operating.
- The TM pin has a room temperature setpoint of 3 V and approximate gain of 10 mV/°C.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	TM Voltage	V_{TM_AMB}	T_J controller = 27°C	2.95	3	3.05	V
		TM Source Current	I_{TM}				**100**	µA
		TM Gain	A_{TM}			10		mV/°C
		TM Voltage Ripple	V_{TM_PP}	C_{TM} = 0 F, V_{IN} = 40 V, I_{OUT} = 40 A		120	**200**	mV
DIGITAL OUTPUT (FAULT FLAG)	Disable	TM Voltage	V_{TM_DIS}			0		V
	Transitional	TM Resistance (Internal)	R_{TM_INT}	Internal pull down resistor	**25**	40	**50**	kΩ
		TM Capacitance (External)	C_{TM_EXT}				**50**	pF
		TM Fault Response Time	T_{FR_TM}	From fault to TM = 1.5 V		10		µs

3.0 SIGNAL CHARACTERISTICS (CONT.)

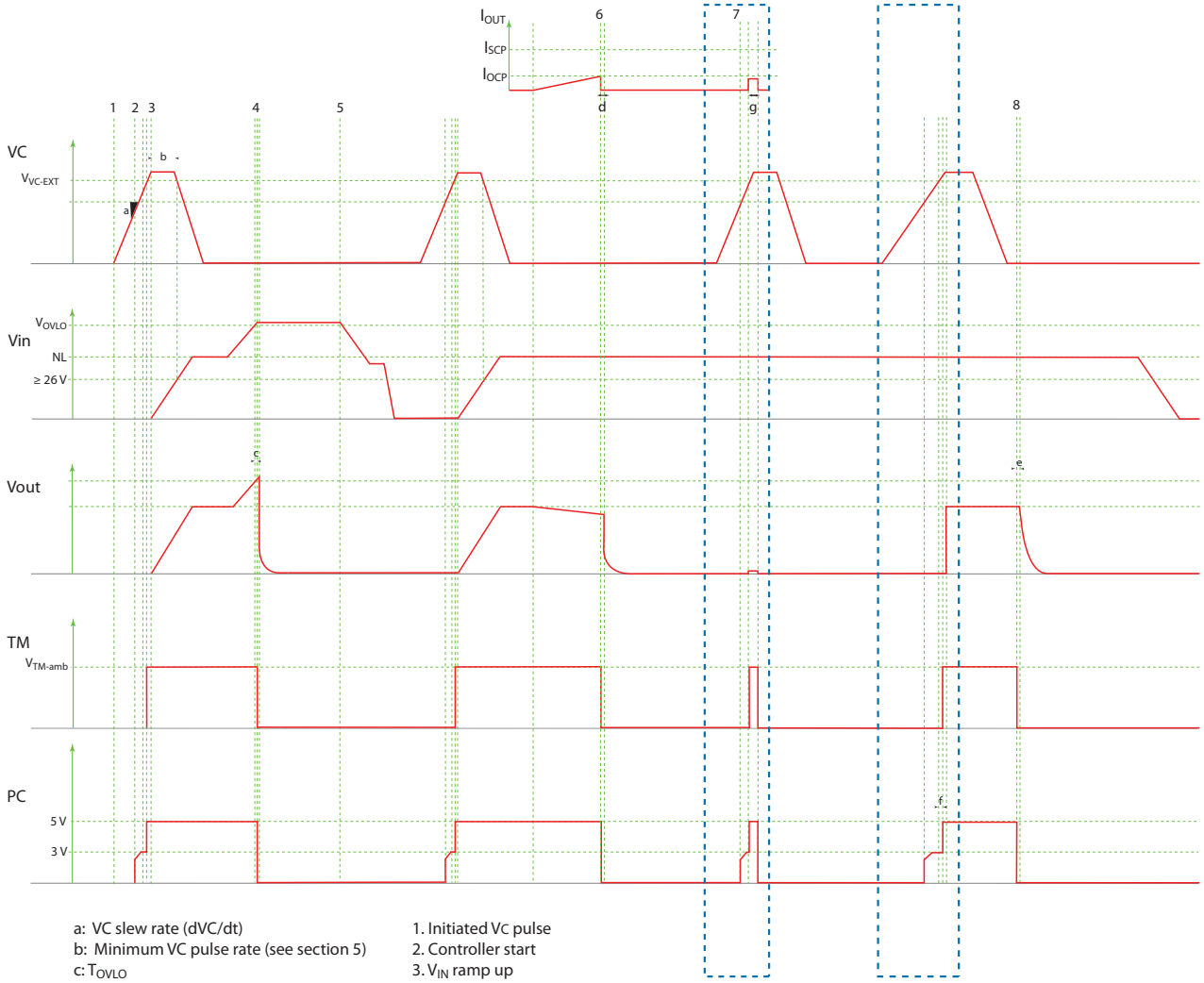
Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T_J < 125°C (T-Grade)**; All other specifications are at **T_J = 25°C** unless otherwise noted.

CURRENT MONITOR : IM

- The IM pin voltage varies between 0.1 V and 1.825 V representing the output current within ±25% under all operating line temperature conditions between 50% and 100%.
- The IM pin provides a DC analog voltage proportional to the output current of the VTM.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	IM Voltage (No Load)	V_{IM_NL}	T_J = 25°C, V_{IN} = 40 V, I_{OUT} = 0 A	0.1	0.206	0.4	V
		IM Voltage (50%)	$V_{IM\_50\%}$	T_J = 25°C, V_{IN} = 40 V, I_{OUT} = 65 A		0.857		V
		IM Voltage (Full Load)	V_{IM_FL}	T_J = 25°C, V_{IN} = 40 V, I_{OUT} = 130 A		1.825		V
		IM Gain	A_{IM}	T_J = 25°C, V_{IN} = 40 V, I_{OUT} > 65 A		14.9		mV/A
		IM Resistance (External)	R_{IM_EXT}		**3**			MΩ

4.0 TIMING DIAGRAM



a: VC slew rate (dVC/dt)
b: Minimum VC pulse rate (see section 5)
c: T_{OVLO}
d: T_{OCP}
e: PC disable time (T_{PC-dis})
f: VC to PC delay
g: T_{SCP}

1. Initiated VC pulse
2. Controller start
3. V_{IN} ramp up
4. V_{IN} = V_{OVLO}
5. V_{IN} ramp down no VC pulse
6. Overcurrent
7. Start up on short circuit
8. PC driven low

Caution:
The module is not designed to start in this sequence.

Notes:
– Timing and voltage is not to scale
– Error pulse width is load dependent

5.0 APPLICATION CHARACTERISTICS

The following values, typical of an application environment, are collected at **T_J = 25°C** unless otherwise noted. See associated figures for general trend data.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	TYP	UNIT
No Load Power Dissipation	P_{NL}	V_{IN} = 42 V, PC enabled	3.2	W
Efficiency (Ambient)	η_{AMB}	V_{IN} = 42 V, I_{OUT} = 130 A	89.5	%
Efficiency (Hot)	η_{HOT}	V_{IN} = 42 V, I_{OUT} = 130 A	88	%
Output Resistance (Ambient)	R_{OUT_AMB}	V_{IN} = 42 V	0.69	mΩ
Output Resistance (Hot)	R_{OUT_HOT}	V_{IN} = 42 V	0.85	mΩ
Output Resistance (Cold)	R_{OUT_COLD}	V_{IN} = 42 V	0.6	mΩ
Output Voltage Ripple	V_{OUT_PP}	C_{OUT} = 0 F, I_{OUT} = 130 A, V_{IN} = 40 V, 20 MHz BW, Section 12	116	mV
V_{OUT} Transient (Positive)	V_{OUT_TRAN+}	I_{OUT_STEP} = 0 A TO 150A, V_{IN} = 40 V, I_{SLEW} >10 A/us	90	mV
V_{OUT} Transient (Negative)	V_{OUT_TRAN-}	I_{OUT_STEP} = 150 A to 0 A, V_{IN} = 40 V I_{SLEW} > 10 A/us	100	mV

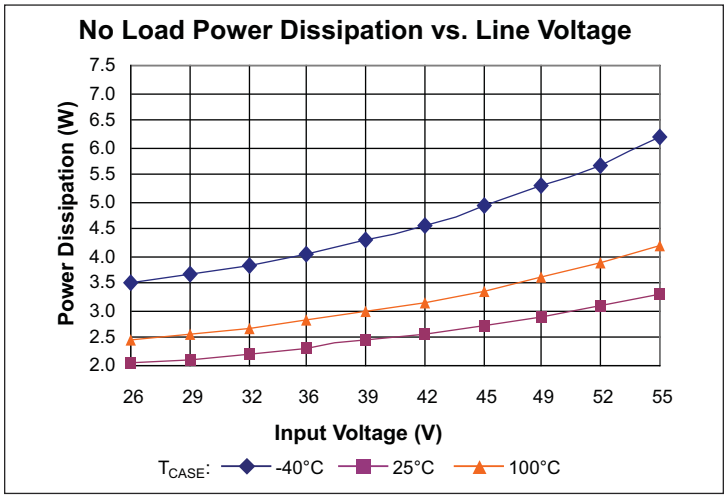


Figure 1 – *No load power dissipation vs. V_{IN}*

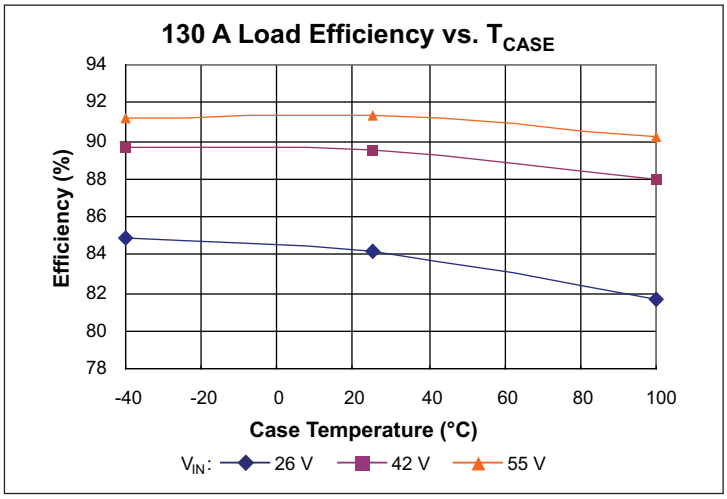


Figure 2 – *Full load efficiency vs. temperature*

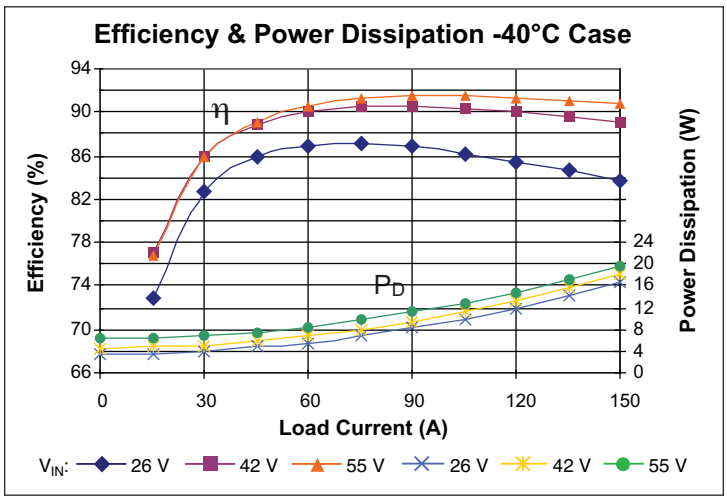


Figure 3 – *Efficiency and power dissipation at –40°C*

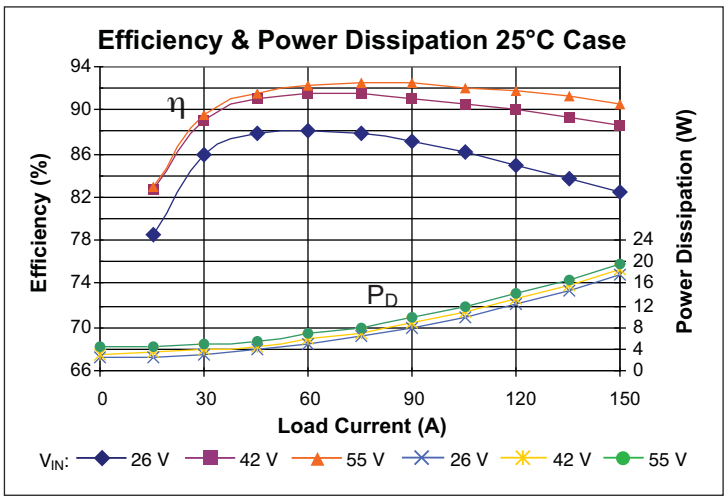


Figure 4 – *Efficiency and power dissipation at 25°C*

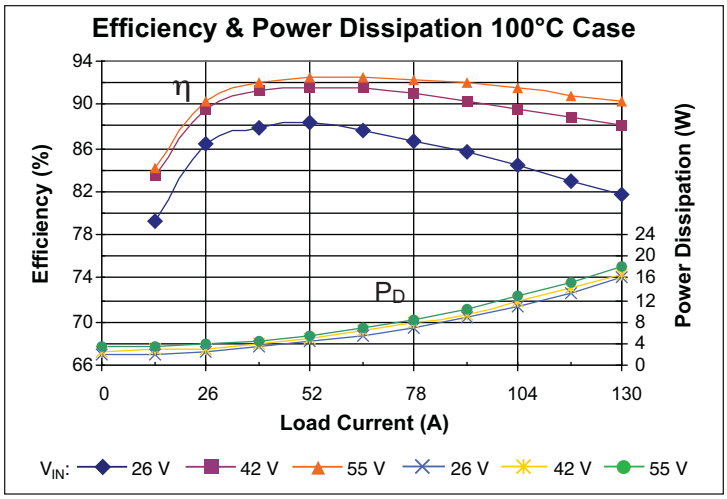


Figure 5 – *Efficiency and power dissipation at 100°C*

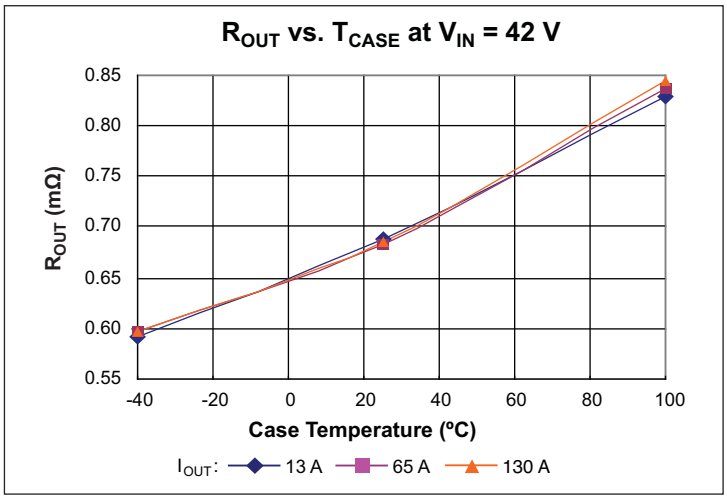


Figure 6 – *R_{OUT} vs. temperature*

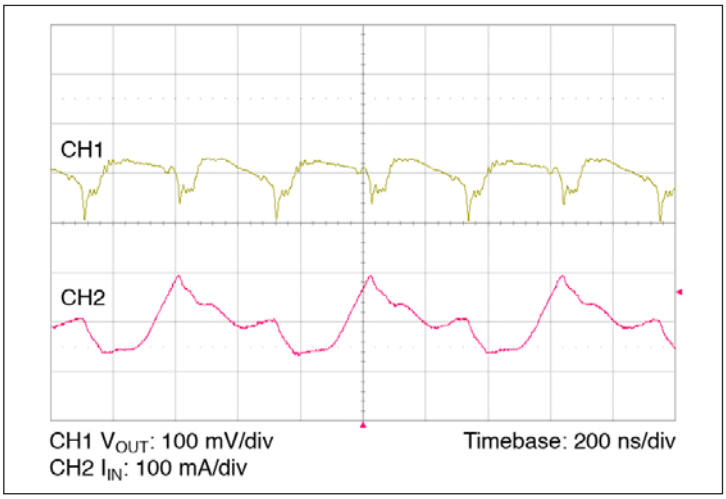


Figure 7 – *Full load ripple, 100 µF C_{IN}; No external C_{OUT}. Board mounted module, scope setting : 20 MHz analog BW, digital filter 1.5 bits -3 dB @ 12 MHz*

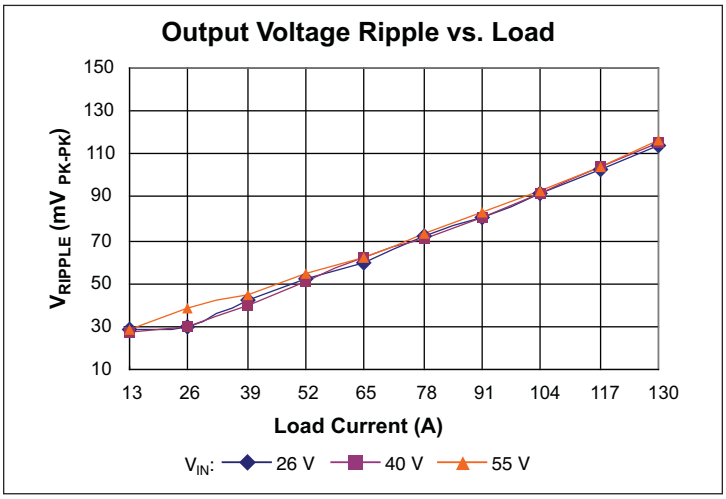


Figure 8 – *V_{RIPPLE} vs. I_{OUT} ; V_{IN}, No external C_{OUT}. Board mounted module, scope setting : 20 MHz analog BW, digital filter 1.5 bits -3 dB @ 12 MHz*

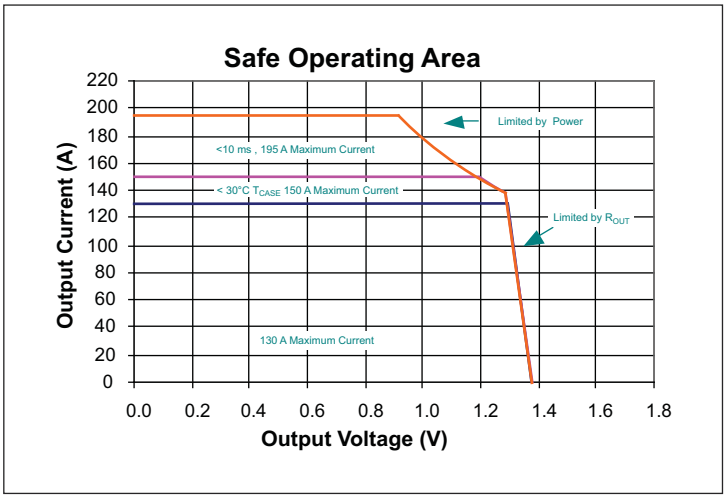


Figure 9 – *Safe operating area*

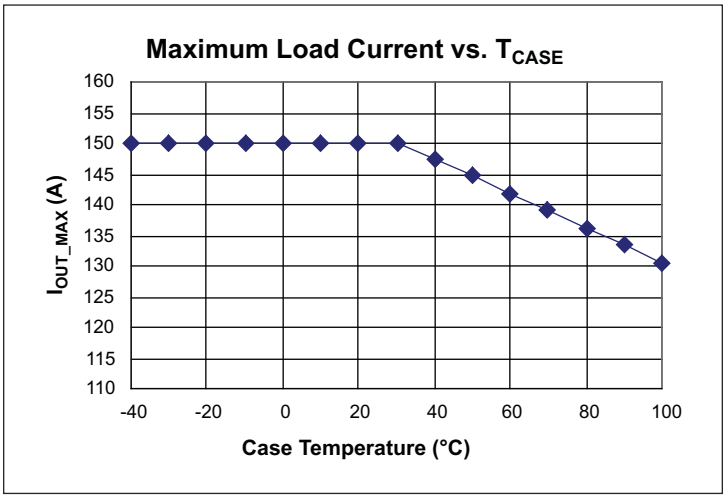


Figure 10 – *Maximum load current using I_{out_max} = - (2/7) * T_C + 159. Junction temperature less than 125°C*

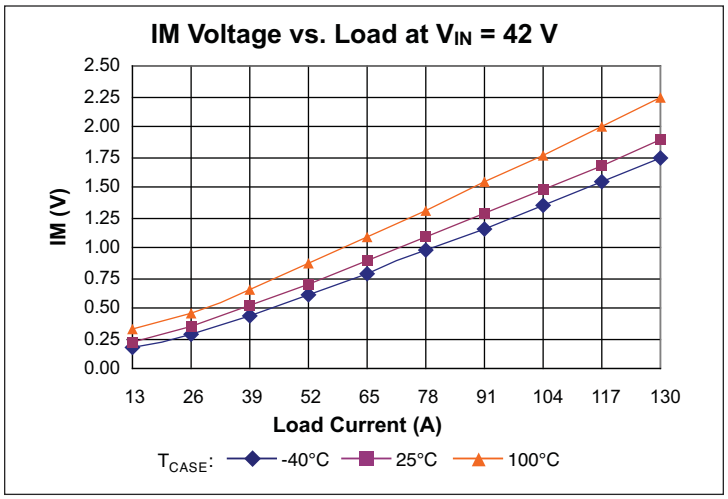


Figure 11 – *IM voltage vs. load*

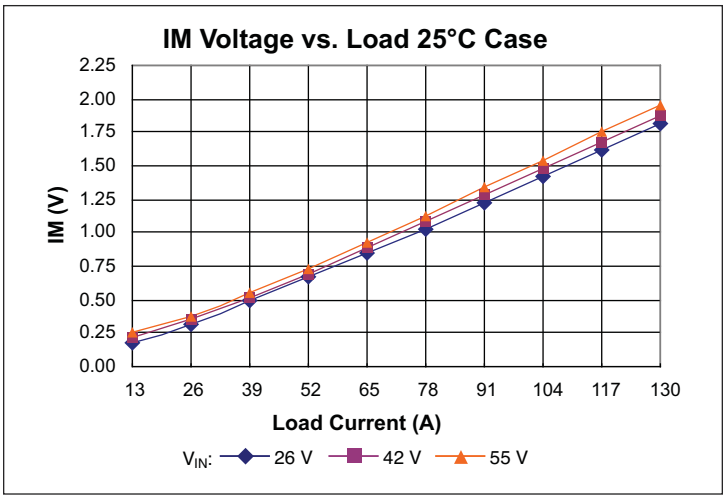


Figure 12 – *IM voltage vs. load*

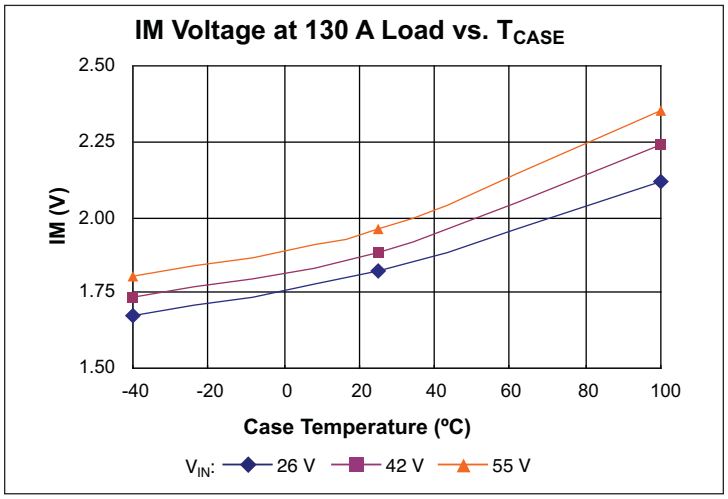


Figure 13 – *Full load IM voltage vs. T_{CASE}*

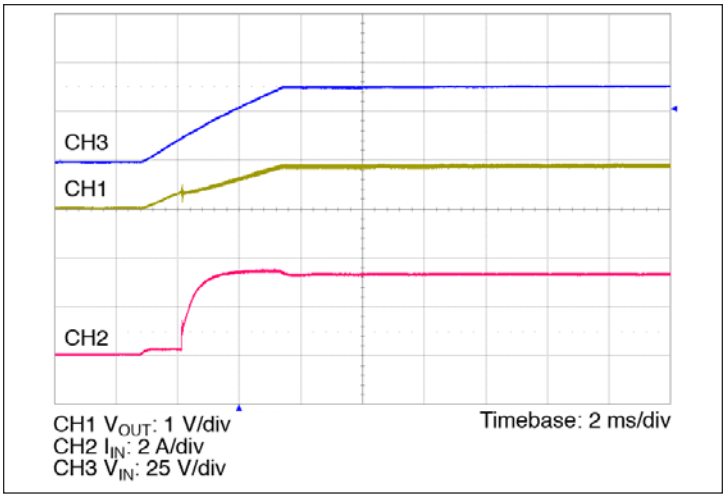


Figure 14 – *Start up from application of V_{IN}: VC pre-applied*

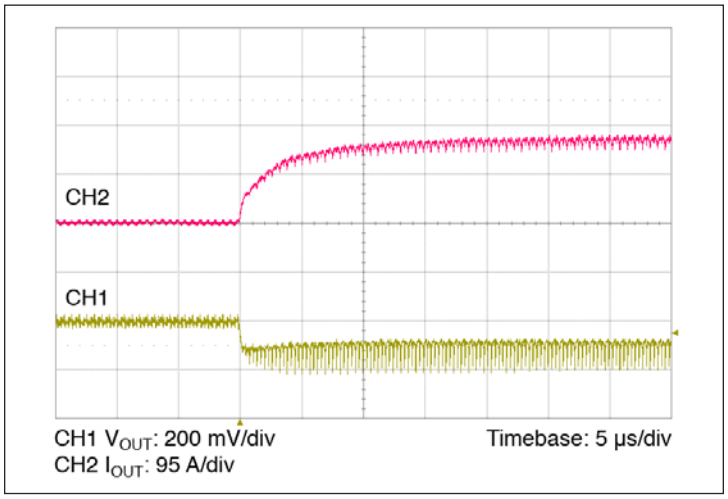


Figure 15 – *0 A– 150 A transient response: C_{IN} = 100 µF, no external C_{OUT}*

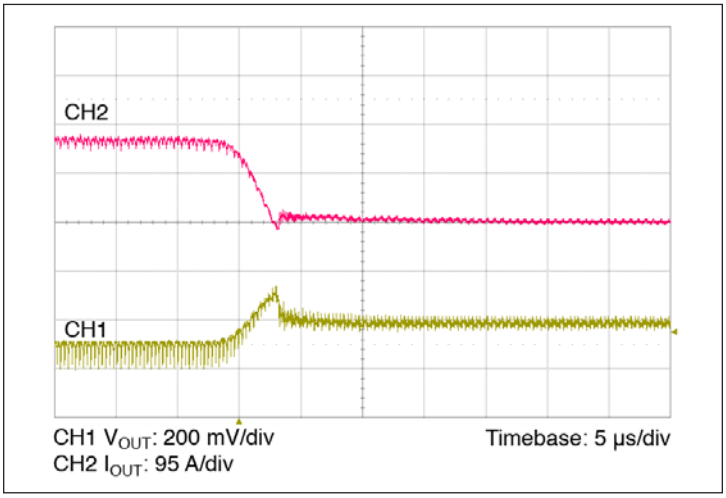


Figure 16 – *150 A – 0 A transient response: C_{IN} = 100 µF, no external C_{OUT}*

6.0 GENERAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T_J < 125°C (T-Grade)**; All Other specifications are at **T_J = 25°C** unless otherwise noted.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
MECHANICAL						
Length	L		32.25 / 1.27	32.5 / 1.28	32.75 / 1.29	mm/in
Width	W		21.75 / 0.86	22.0 / 0.87	22.25 / 0.88	mm/in
Height	H		6.48 / 0.255	6.73 / 0.265	6.98 / 0.275	mm/in
Volume	Vol	No heat sink		4.82 / 0.29		cm^3/in^3
Weight	W			0.512 / 14.5		oz/g
Lead Finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
THERMAL						
Operating Temperature	T_J		-40		125	°C
Thermal Capacity				9		Ws/°C
ASSEMBLY						
Peak Compressive Force Applied to Case (Z-axis)		Supported by J-lead only		5	6	lbs
Storage Temperature	T_{ST}		-40		125	°C
Moisture Sensitivity Level	MSL	225°C Reflow	5			
ESD Withstand	ESD_{HBM}	Human Body Model, "JEDEC JESD 22-A114C.01"	1000			V_{DC}
	ESD_{CDM}	Charged Device Model, "JEDEC JESD 22-C101D"	400			
SOLDERING						
Peak Temperature During Reflow					225	°C
Peak Time Above 183°C					150	s
Peak Heating Rate During Reflow				1.5	2	°C/s
Peak Cooling Rate Post Reflow				2.5	3	°C/s
SAFETY						
Working Voltage (IN – OUT)	V_{IN_OUT}				**60**	VDC
Isolation Voltage (hipot)	V_{HIPOT}		**100**			VDC
Isolation Capacitance	C_{IN_OUT}	Unpowered Unit	**0.018**	**0.02**	**0.022**	µF
Isolation Resistance	R_{IN_OUT}		**10**			MΩ
MTBF		MIL HDBK 217 Plus, 25°C, Ground Benign		3.9		MHrs
		Telcordia Issue 2, Method I		6.73		
Agency Approvals / Standards		cTUVus				
		cULus				
		CE Mark				
		RoHS 6 of 6				

7.0 USING THE CONTROL SIGNALS VC, PC, TM, IM

VTM Control (VC) pin is an input pin which powers the internal VCC circuitry within the specified voltage range of 26 V to 55 V. This voltage is required in order for the VTM to start, and must be applied as long as the input is below 26 V. In order to ensure a proper start, the slew rate of the applied voltage must be within the specified range. VC must be applied first to activate the controller prior to the input. When the input voltage is applied, the VTM output voltage will track the input allowing for a soft-start. If the VC voltage is removed prior to the input reaching 26 V, the VTM may shut down.

Some additional notes on using the VC pin:

- In most applications, the VTM will be powered by an upstream PRM, in which case the PRM will provide a typical 10 ms VC pulse during startup. In these applications the VC pins of the PRM and VTM should be tied together.
- The fault response of the VTM is latching. A positive edge on VC, or toggling PC if VC is continuously applied, is required in order to restart the unit.
- The VTM is designed for continuous operation with VC applied.

Primary Control (PC) pin can be used to accomplish the following functions:

- Delayed start: Upon the application of VC, the PC pin will source a constant 100 µA current to the internal RC network. Adding an external capacitor will allow further delay in reaching the 2.5 V threshold for module start.
- Auxiliary voltage source: Once enabled in regular operational conditions (no fault), each VTM PC provides a regulated 5 V, 2 mA voltage source.
- Output disable: PC pin can be actively pulled down in order to disable the module. Pull down impedance shall be lower than 850 Ω.
- Fault detection flag: The PC 5 V voltage source is internally turned off as soon as a fault is detected. It is important to notice that PC doesn't have current sink capability. Therefore, in an array, PC line will not be capable of disabling neighboring modules if a fault is detected.
- Fault reset: PC may be toggled to restart the unit if VC is continuously applied.

Temperature Monitor (TM) pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- Monitor the control IC temperature: The temperature in Kelvin is equal to the voltage on the TM pin scaled by 100. (i.e. 3.0 V = 300 K = 27°C). If a heat sink is applied, TM can be used to thermally protect the system.
- Fault detection flag: The TM voltage source is internally turned off as soon as a fault is detected. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of TM signal.

Current Monitor (IM) pin provides a voltage proportional to the output current of the VTM. The voltage will vary between 0.206 V and 1.825 V over the output current range of the VTM (See Figures 11–13). The accuracy of the IM pin will be within 25% under all line and temperature conditions between 50% and 100% load. The accuracy of the pin can be improved using a predictive algorithm based on the input voltage and internal temperature.

8.0 THERMAL CONSIDERATIONS

V•I Chip products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input / output conditions, thermal management and environmental conditions. Maintaining the top of the VIV0005TFJ case to less than 100°C will keep all junctions within the V•I Chip below 125°C for most applications.

The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB board surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.

It is not recommended to use a V•I Chip for an extended period of time at full load without proper heatsinking.

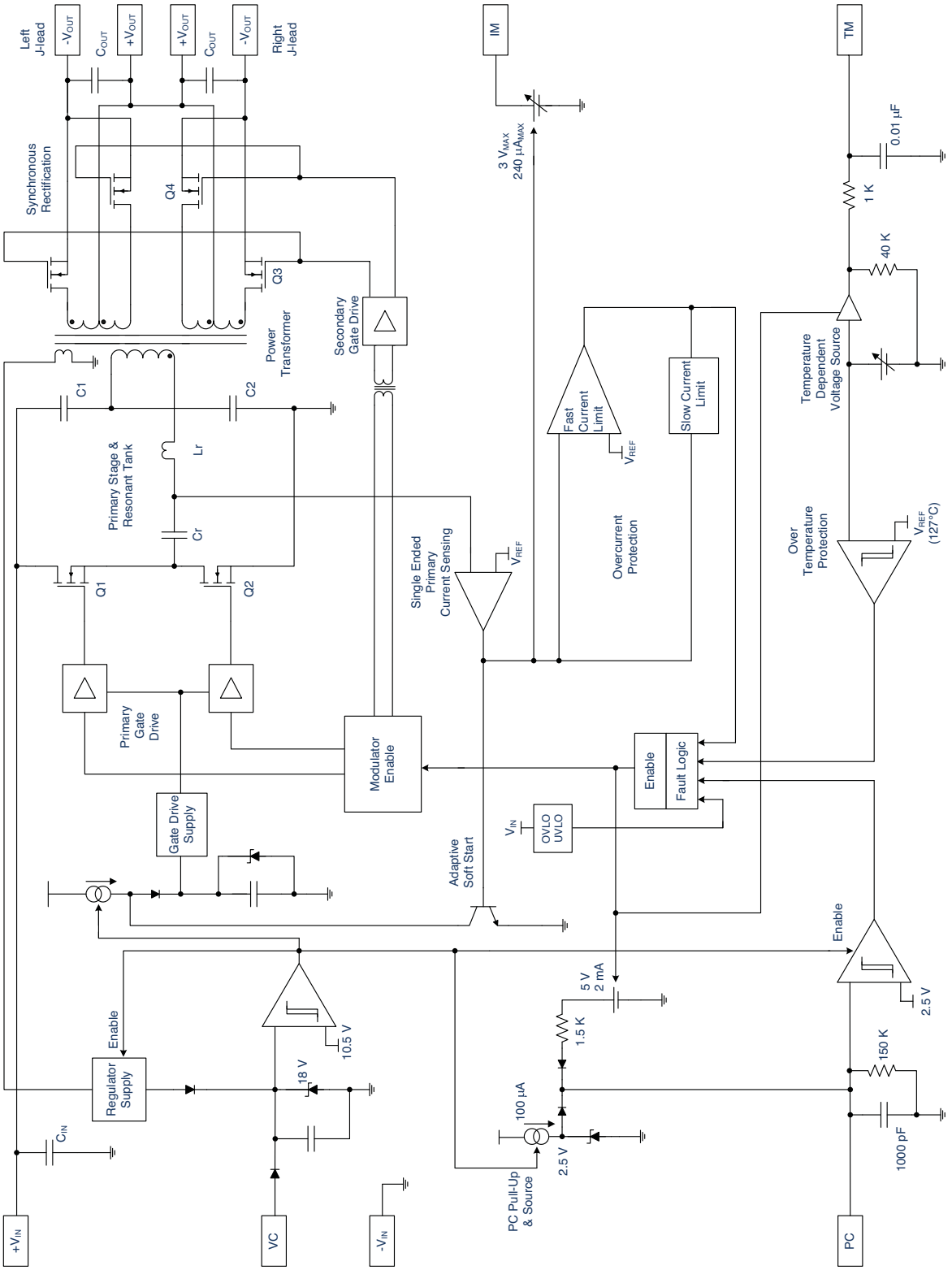
9.0 FUSE SELECTION

In order to provide flexibility in configuring power systems V•I Chip products are not internally fused. Input line fusing of V•I Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than maximum VTM current)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t

10.0 VTM BLOCK DIAGRAM



11.0 SINE AMPLITUDE CONVERTER POINT OF LOAD CONVERSION

The Sine Amplitude Converter (SAC) uses a high frequency resonant tank to move energy from input to output. The resonant tank formed by Cr and leakage inductance Lr in the power transformer windings as shown in the VTM Block Diagram (See Section 10). The resonant LC tank, operated at high frequency, is amplitude modulated as function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving power density.

The VIV0005TFJ SAC can be simplified into the following model:

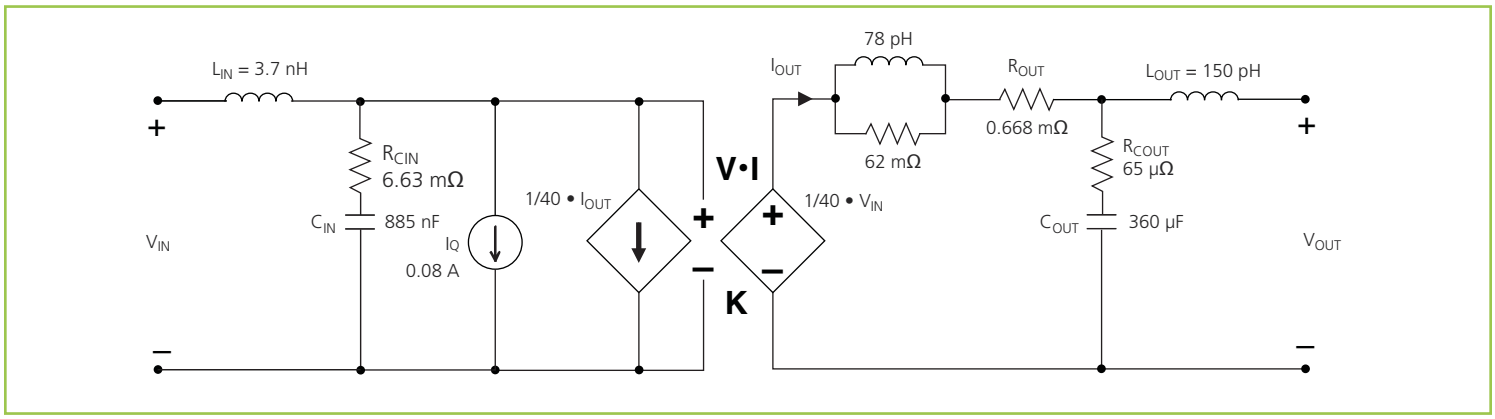


Figure 17 – *V•I Chip AC model*

At no load:

$$V_{OUT} = V_{IN} \bullet K \quad (1)$$

K represents the "turns ratio" of the SAC. Rearranging Eq (1):

$$K = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

In the presence of load, V_{OUT} is represented by:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{OUT} \quad (3)$$

and I_{OUT} is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \quad (4)$$

R_{OUT} represents the impedance of the SAC, and is a function of the R_{DSON} of the input MOSFETs and the winding resistance of the Power transformer. I_Q represents the quiescent current of the SAC control and gate drive circuitry.

The use of DC voltage transformation provides additional interesting attributes. Assuming for the moment that R_{OUT} and I_Q = 0 A, Eq. (3) now becomes Eq. (2) and is essentially load independent. A resistor R is now placed in series with V_{IN} as shown in Figure 18.

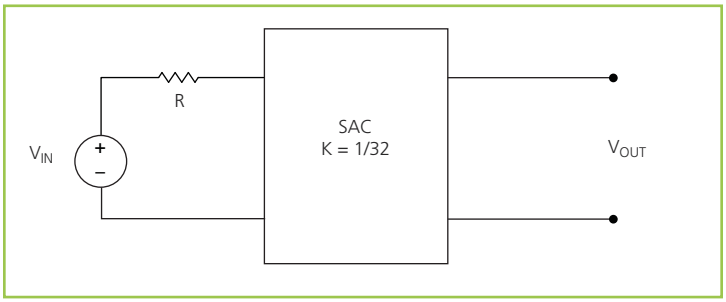


Figure 18 – *K = 1/32 Sine Amplitude Converter with series input resistor*

The relationship between V_{IN} and V_{OUT} becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \bullet R) \bullet K \quad (5)$$

Substituting the simplified version of Eq. (4) (I_Q is assumed = 0 A) into Eq. (5) yields:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R \bullet K^2 \quad (6)$$

This is similar in form to Eq. (3), where R_{OUT} is used to represent the characteristic impedance of the SAC. However, in this case a real R on the input side of the SAC is effectively scaled by K^2 with respect to the output.

Assuming that R = 1 Ω, the effective R as seen from the secondary side is 0.98 mΩ, with K = 1/32 as shown in Figure 18.

A similar exercise should be performed with the additon of a capacitor, or shunt impedance, at the input to the SAC. A switch in series with V_{IN} is added to the circuit. This is depicted in Figure 19.

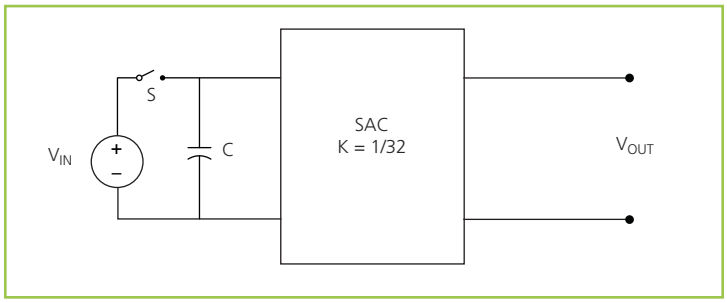


Figure 19 – *Sine Amplitude Converter with input capacitor*

A change in V_{IN} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{IN}}{dt} \quad (7)$$

Assume that with the capacitor charged to V_{IN}, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{OUT} \bullet K \quad (8)$$

Substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{OUT} = \frac{C}{K^2} \bullet \frac{dV_{OUT}}{dt} \quad (9)$$

Writing the equation in terms of the output has yielded a K^2 scaling factor for C, this time in the denominator of the equation. For a K factor less than unity, this results in an effectively larger capacitance on the output when expressed in terms of the input. With a K = 1/32 as shown in Figure 19, C = 1 µF would effectively appear as C = 1024 µF when viewed from the output.

Low impedance is a key requirement for powering a high current, low voltage load efficiently. A switching regulation stage should have minimal impedance, while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit, scaling down series impedance leading back to the source and scaling up shunt capacitance (or energy storage) as a function of its K factor squared. However, these benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables magnetic components to be small since magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies reduces core losses as well.

The two main terms of power loss in the VTM module are:

- No load power dissipation (P_{NL}): defined as the power used to power up the module with an enabled power train at no load.
- Resistive loss (R_{OUT}): refers to the power loss across the VTM modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{R_{OUT}} \quad (10)$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{R_{OUT}} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{R_{OUT}}}{P_{IN}} \quad (12)$$

$$= \frac{V_{IN} \bullet I_{IN} - P_{NL} - (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}$$

$$= 1 - \left(\frac{P_{NL} + (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}\right)$$

12.0 INPUT AND OUTPUT FILTER DESIGN

A major advantage of a SAC system versus a conventional PWM converter is that the former does not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving high power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

1. Guarantee low source impedance.

   To take full advantage of the VTM dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The connection of the V•I Chip to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

2. Further reduce input and/or output voltage ripple without sacrificing dynamic response.

   Given the wide bandwidth of the VTM, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the VTM multiplied by its K factor.

3. Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures.

   The V•I Chip input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it. A criterion for protection is the maximum amount of energy that the input or output switches can tolerate if avalanched.

13.0 CAPACITIVE FILTERING CONSIDERATIONS FOR A SINE AMPLITUDE CONVERTER

It is important to consider the impact of adding input and output capacitance to a Sine Amplitude Converter on the system as a whole. Both the capacitance value, and the effective impedance of the capacitor must be considered.

A Sine Amplitude Converter has a DC R_{OUT} value which has already been discussed in section 11. The AC R_{OUT} of the SAC contains several terms:

- Resonant tank impedance
- Input lead inductance and internal capacitance
- Output lead inductance and internal capacitance

The values of these terms are shown in the behavioral model in section 11. It is important to note on which side of the transformer these impedances appear and how they reflect across the transformer given the K factor.

The overall AC impedance varies from model to model but for most models it is dominated by DC R_{OUT} value from DC to beyond 500 KHz. The behavioral model in section 11 should be used to approximate the AC impedance of the specific model.

Any capacitors placed at the output of the VTM reflect back to the input of the VTM by the square of the K factor (Eq. 9) with the impedance of the VTM appearing in series. It is very important to keep this in mind when using a PRM to power the VTM. Most PRMs have a limit on the maximum amount of capacitance that can be applied to the output. This capacitance includes both the PRM output capacitance and the VTM output capacitance reflected back to the input. In PRM remote sense applications, it is important to consider the reflected value of VTM output capacitance when designing and compensating the PRM control loop.

Capacitance placed at the input of the VTM appear to the load reflected by the K factor, with the impedance of the VTM in series. In step-down VTM ratios, the effective capacitance is increased by the K factor. The effective ESR of the capacitor is decreased by the square of the K factor, but the impedance of the VTM appears in series. Still, in most step-down VTMs an electrolytic capacitor placed at the input of the VTM will have a lower effective impedance compared to an electrolytic capacitor placed at the output. This is important to consider when placing capacitors at the output of the VTM. Even though the capacitor may be placed at the output, the majority of the AC current will be sourced from the lower impedance, which in most cases will be the VTM. This should be studied carefully in any system design using a VTM. In most cases, it should be clear that electrolytic output capacitors are not necessary to design a stable, well-bypassed system.

14.0 CURRENT SHARING

The SAC topology bases its performance on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with some resistive drop and positive temperature coefficient.

This type of characteristic is close to the impedance characteristic of a DC power distribution system, both in behavior (AC dynamic) and absolute value (DC dynamic).

When connected in an array with the same K factor, the VTM module will inherently share the load current with parallel units, according to the equivalent impedance divider that the system implements from the power source to the point of load.

It is important to notice that, when successfully started, VTMs are capable of bi-directional operation. Reverse power transfer is enabled if the VTM input falls within its operating range and the VTM is otherwise enabled. In parallel arrays, because of R_{OUT}, circulating currents are never experienced due to energy conservation law.

Some general recommendations to achieve matched array impedances:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide the PCB layout as symmetric as possible.
- Apply same input / output filters (if present) to each unit.

For further details see AN:016 Using BCM™ Bus Converters in High Power Arrays.

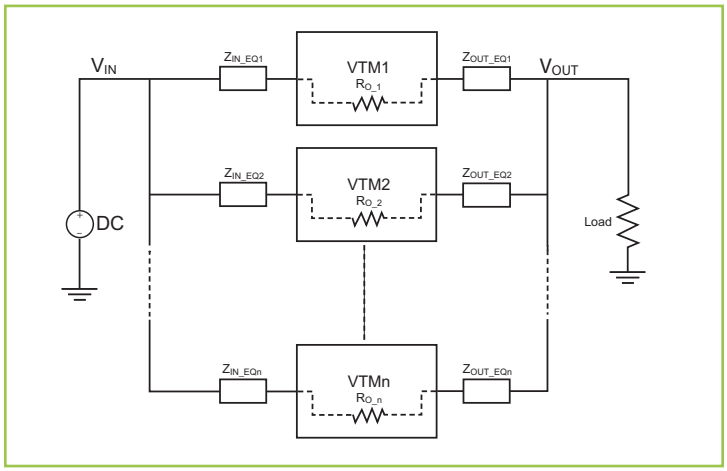
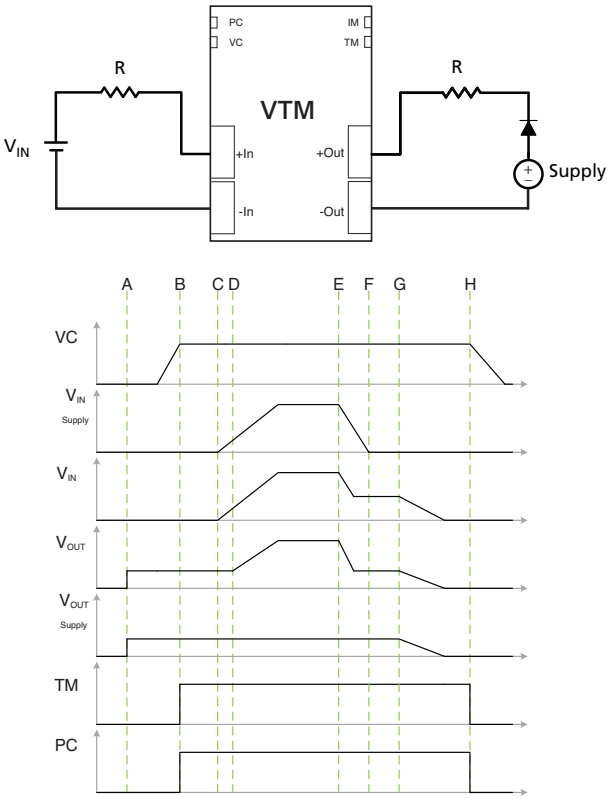


Figure 20 – *VTM array*

15.0 REVERSE INRUSH CURRENT PROTECTION

The VIV0005TFJ provides reverse inrush protection which prevents reverse current flow until the input voltage is high enough to first establish current flow in the forward direction. In the event that there is a DC voltage present on the output before the VTM is powered up, this feature protects sensitive loads from excessive dV/dT during power up as shown in Figure 21.

If a voltage is present at the output of the VTM which satisfies the condition $V_{OUT} > V_{IN} \bullet K$ after a successful power up the energy will be transferred from secondary to primary. The input to output ratio of the VTM will be maintained. The VTM will continue to operate in reverse as long as the input and output voltages are within the specified range. The VIV0005TFJ has not been qualified for continuous reverse operation.



A: V_{OUT} supply > 0 V
B: VC to -IN > 11.5 V controller wakes-up, PC & TM pulled high, reverse inrush protection blocks V_{OUT} supplying V_{IN}
C: V_{IN} supply ramps up
D: $V_{IN} > V_{OUT}/K$, powertrain starts in normal mode
E: V_{IN} supply ramps down
F: $V_{IN} > V_{OUT}/K$, powertrain transfers reverse energy
G: V_{OUT} ramps down, V_{IN} follows
H: VC turns off

Figure 21 – *Reverse inrush protection*

16.0 LAYOUT CONSIDERATIONS

The VIV0005TFJ requires equal current density along the output J-leads to achieve rated efficiency and output power level. The negative output J-leads are not connected internally and must be connected on the board as close to the VTM as possible. The layout must also prevent the high output current of the VIV0005TFJ from interfering with the input-referenced signals.

To achieve these requirements, the following layout guidelines are recommended:

- The total current path length from any point on the V_{+OUT} J-leads to the corresponding point on the V_{-OUT} J-leads should be equal (see Figure 22) .
- Use vias along the negative output J-leads to connect the negative output to a common power plane.
- Use sufficient copper weight and number of layers to carry the output current to the load or to the output connectors.
- Be sure to include enough vias along both the positive and negative J leads to distribute the current among the layers of the PCB.
- Do not run input-referenced signal traces (VC, PC, TM and IM) between the layers of the secondary outputs.
- Run the input-referenced signal traces (VC, PC, TM and IM) such that V_{-IN} shields the signals. See AN:005 FPA Printed Circuit Board Layout Guidelines for more details.

Equalizing the current paths is most easily accomplished by centering the VTM output J-leads between the output connections of the PCB and by designing the board such that the layout is symmetric from both sides of the output and from the front and back ends of the output as shown in Figures 23 and 24.

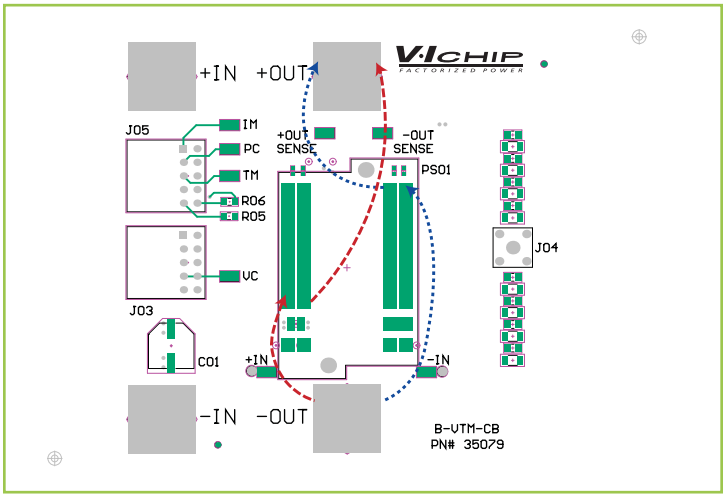


Figure 22 – *Equal current path*

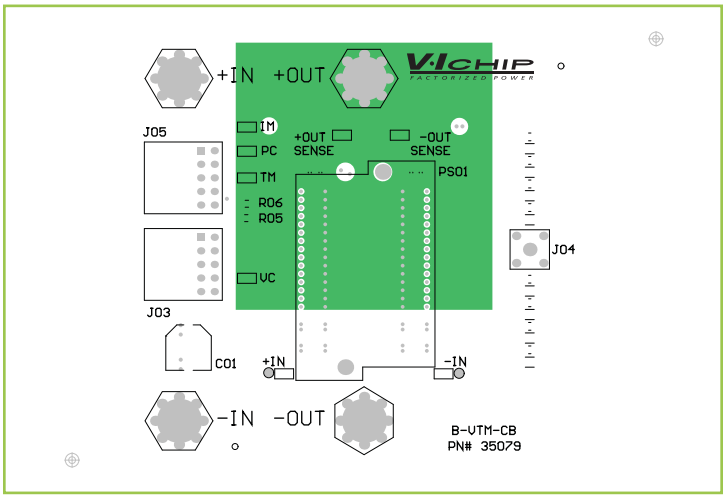


Figure 23 – *Symmetric layout*

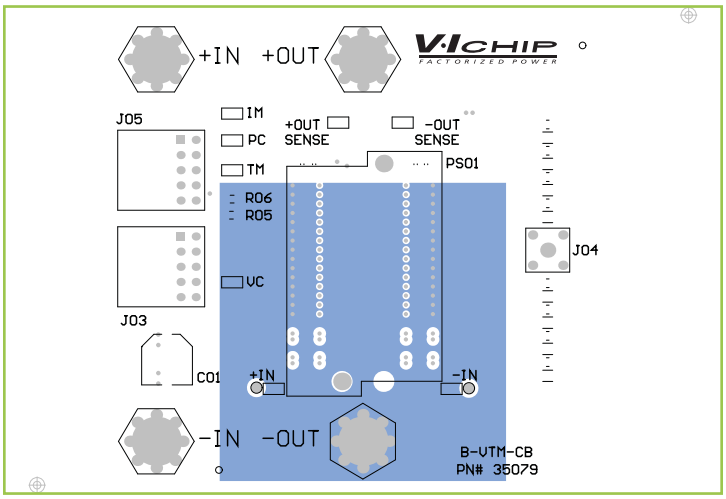
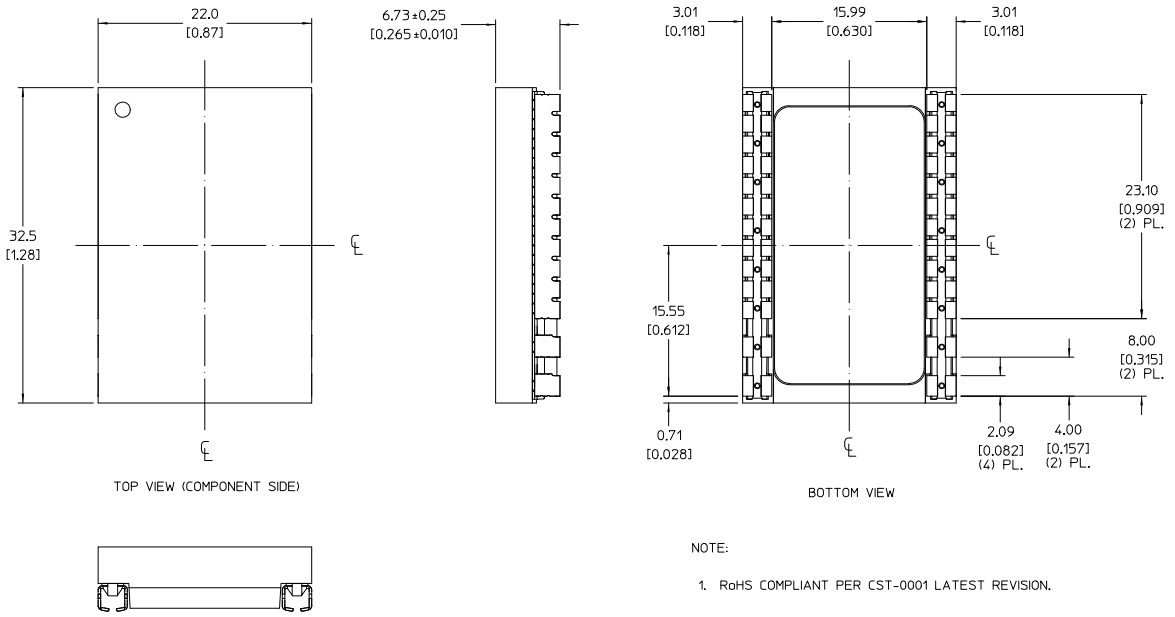


Figure 24 – *Symmetric layout*

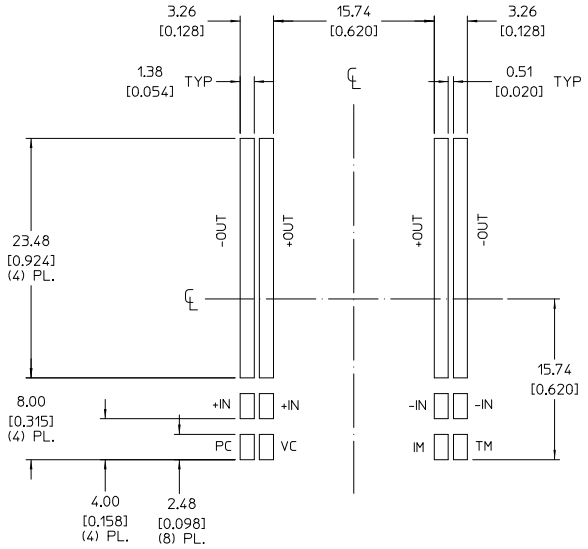
17.0 MECHANICAL DRAWING

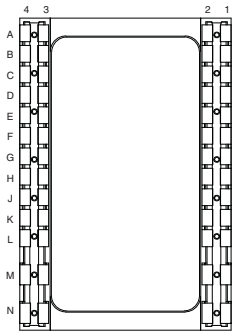


NOTE:

1. RoHS COMPLIANT PER CST-0001 LATEST REVISION.

17.1 RECOMMENDED LAND PATTERN





Bottom View

Signal Name	Designation
+In	M2, M1
–In	M4, M3
IM	N3
TM	N4
VC	N2
PC	N1
+Out	A3-L3, A2-L2
–Out	A4-L4, A1-L1

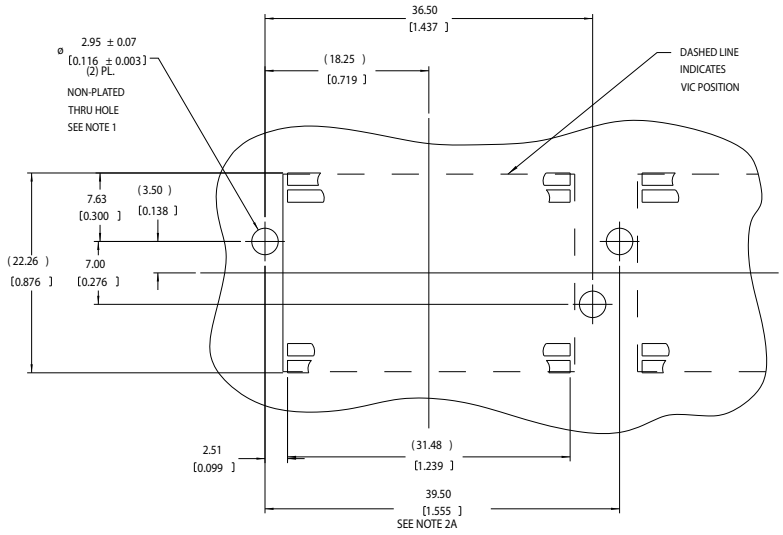
NOTES: mm / inch
1. DIMENSIONS ARE
2. UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
   X.XX = ≠±0.25 [0.01]
   X.XXX = ≠±0.127 [0.005]
3. RoHS COMPLIANT PER CST-0001 LATEST REVISION.

DXF and PDF files are available on vicorpower.com

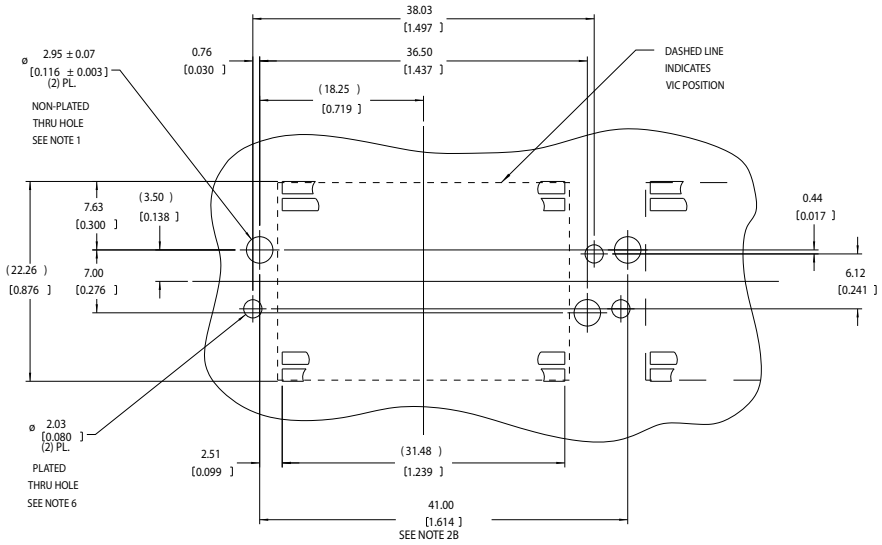
Click here to view original mechanical drawing on the Vicor website.

17.2 RECOMMENDED LAND PATTERN FOR PUSH PIN HEAT SINK

RECOMMENDED LAND PATTERN
(NO GROUNDING CLIPS)
TOP SIDE SHOWN



RECOMMENDED LAND PATTERN
(With GROUNDING CLIPS)
TOP SIDE SHOWN



NOTES:

1. MAINTAIN 3.50 [0.138] DIA. KEEP-OUT ZONE FREE OF COPPER, ALL PCB LAYERS.
2. (A) MINIMUM RECOMMENDED PITCH IS 39.50 [1.555], THIS PROVIDES 7.00 [0.275] COMPONENT EDGE-TO-EDGE SPACING, AND 0.50 [0.020] CLEARANCE BETWEEN VICOR HEAT SINKS.

   (B) MINIMUM RECOMMENDED PITCH IS 41.00 [1.614], THIS PROVIDES 8.50 [0.334] COMPONENT EDGE-TO-EDGE SPACING, AND 2.00 [0.079] CLEARANCE BETWEEN VICOR HEAT SINKS.
3. V•I CHIP LAND PATTERN SHOWN FOR REFERENCE ONLY; ACTUAL LAND PATTERN MAY DIFFER. DIMENSIONS FROM EDGES OF LAND PATTERN TO PUSH-PIN HOLES WILL BE THE SAME FOR ALL FULL SIZE V•ICHIP PRODUCTS.
4. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
5. UNLESS OTHERWISE SPECIFIED:
   DIMENSIONS ARE MM [INCH].
   TOLERANCES ARE:
   X.X [X.XX] = ±0.3 [0.01]
   X.XX [X.XXX] = ±0.13 [0.005]
6. PLATED THROUGH HOLES FOR GROUNDING CLIPS (33855) SHOWN FOR REFERENCE. HEATSINK ORIENTATION AND DEVICE PITCH WILL DICTATE FINAL GROUNDING SOLUTION.

Click here to view original mechanical drawing on the Vicor website.

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5,945,130; 6,403,009; 6,710,257; 6,911,848; 6,930,893; 6,934,166; 6,940,013; 6,969,909; 7,038,917; 7,145,186; 7,166,898; 7,187,263; 7,202,646; 7,361,844; D496,906; D505,114; D506,438; D509,472; and for use under 6,975,098 and 6,984,965.

Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715

email
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com