XE61C Series

Standard Voltage Detectors (V_{DF}=1.6V～6.0V)

■GENERAL DESCRIPTION

The XE61C series is a highly precise, low power consumption voltage detector, manufactured using CMOS process and laser trimming technologies.

Detect voltage is extremely accurate with minimal temperature drift.

Both CMOS and N-channel open drain output configurations are available.

The XE61C assures all temperature range (Ta= - 40°C ~ + 85°C).

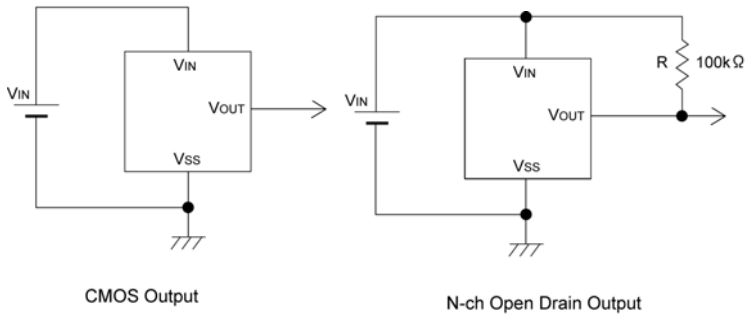
■APPLICATIONS

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors

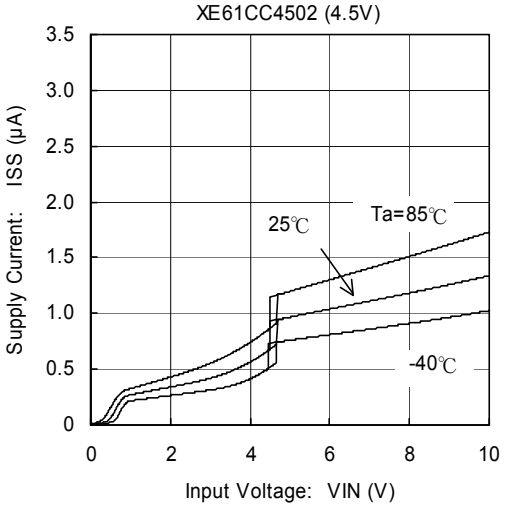
■FEATURES

Detect Voltage Accuracy	: ± 2% (Ta=25°C) ± 4% (Ta=-40°C～+85℃)
Detect Voltage	: 1.6V～6.0V (0.1V increments)
Temperature Characteristics	: ±400ppm/℃ (Ta=- 40°C~+85°C)
Operating Voltage Range	: 0.7V～10.0V
Low Power Consumption	: 0.7μA TYP. (V_{IN}=1.5V)
Output Configuration	: N-channel open drain or CMOS
Packages	: SOT-23 SOT-89
Environmentally Friendly	: EU RoHS Compliant, Pb Free

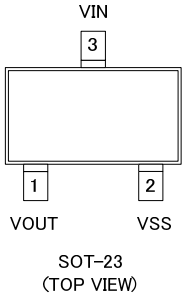
■TYPICAL APPLICATION CIRCUITS



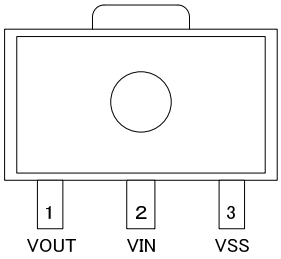
■TYPICAL PERFORMANCE CHARACTERISTICS



■PIN CONFIGURATION



SOT-23
(TOP VIEW)



SOT-89
(TOP VIEW)

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-23	SOT-89		
3	2	V_{IN}	Supply Voltage
2	3	V_{SS}	Ground
1	1	V_{OUT}	Output
-		NC	No Connection

■PRODUCT CLASSIFICATION

●Ordering Information

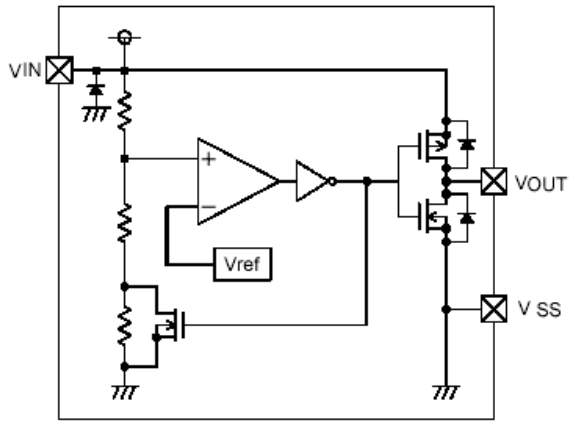
XE61C①②③④⑤⑥⑦-⑧(*1)

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	N-ch open drain output
② ③	Detect Voltage (V_{DF})	16 ~ 60	e.g.1.6V → ②1, ③6
④	Output Delay	0	No delay
⑤	Detect Accuracy	2	Within ±2%
⑥⑦-⑧	Packages Taping Type (*2)	MR	SOT-23
		MR-G	SOT-23 (Halogen & Antimony free)
		PR	SOT-89

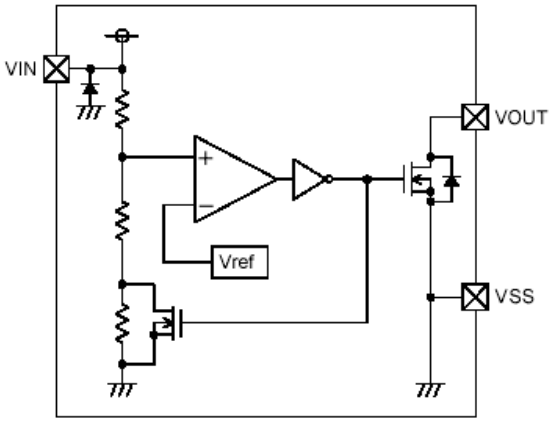
(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully RoHS compliant.
(*2) The device orientation is fixed in its embossed tape pocket. For reverse orientation, please contact your local Torex sales office or representative. (Standard orientation: ⑥R-⑧, Reverse orientation: ⑥L-⑧)

■BLOCK DIAGRAMS

(1) CMOS Output



(2) N-ch Open Drain Output



■ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		VIN	12.0	V
Output Current		IOUT	50	mA
Output Voltage	CMOS	VOUT	VSS -0.3 ~ VIN +0.3	V
	N-ch Open Drain Output		VSS -0.3 ~ 12.0	
Power Dissipation	SOT-23	Pd	250	mW
	SOT-89		500	
Operating Temperature Range		Topr	- 40～+85	°C
Storage Temperature Range		Tstg	-55～+125	°C

■ELECTRICAL CHARACTERISTICS

XE61C Series

$V_{DF(T)}$=1.6~6.0V, Ta= - 40℃ ~ 85℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS	CIRCUITS
Detect Voltage	V_{DF}			$V_{DF(T)}$ x 0.96	$V_{DF(T)}$	$V_{DF(T)}$ x 1.04	V	1
Hysteresis Width	V_{HYS}			V_{DF} x 0.02	V_{DF} x 0.05	V_{DF} x 0.08	V	1
Supply Current	I_{SS}		V_{IN} = 1.5V	-	0.7	2.8	μA	2
			V_{IN} = 2.0V	-	0.8	3.3		
			V_{IN} = 3.0V	-	0.9	3.5		
			V_{IN} = 4.0V	-	1.0	3.7		
			V_{IN} = 5.0V	-	1.1	3.9		
Operating Voltage	V_{IN}	$V_{DF(T)}$ = 1.6V to 6.0V		0.7	-	10.0	V	1
Output Current	I_{OUT}	N-ch V_{DS} = 0.5V	V_{IN} = 1.0V	0.4	2.2	-	mA	3
			V_{IN} = 2.0V	3.0	7.7	-		
			V_{IN} = 3.0V	5.0	10.1	-		
			V_{IN} = 4.0V	6.0	11.5	-		
			V_{IN} = 5.0V	7.0	13.0	-		
		CMOS, P-ch V_{DS} = 2.1V,	V_{IN} = 8.0V	-	-10.0	-2.0		4
Leakage Current (CMOS Output)	I_{leak}	V_{IN}=10.0V V_{OUT}=10.0V		-	10	-	nA	3
Leakage Current (N-ch Open Drain Output)	I_{leak}			-	10	400		
Temperature Characteristics	$\frac{\Delta V_{DF}}{\Delta Topr \cdot V_{DF}}$	-40℃ ≦ Topr ≦ 85℃		-	±100	±400	ppm/℃	-
Delay Time (V_{DR}→V_{OUT} inversion)	T_{DLY}	Inverts from V_{DR} to V_{OUT}		-	0.03	0.20	ms	5

NOTE:
$V_{DF\ (T)}$: Nominal detect voltage
Release Voltage: $V_{DR} = V_{DF} + V_{HYS}$

■OPERATIONAL EXPLANATION

(Especially explained for the CMOS output products)

① When input voltage (V_{IN}) rises above detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to V_{IN}.
(A condition of high impedance exists with N-ch open drain output configurations.)

② When input voltage (V_{IN}) falls below detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to the ground voltage (V_{SS}) level.

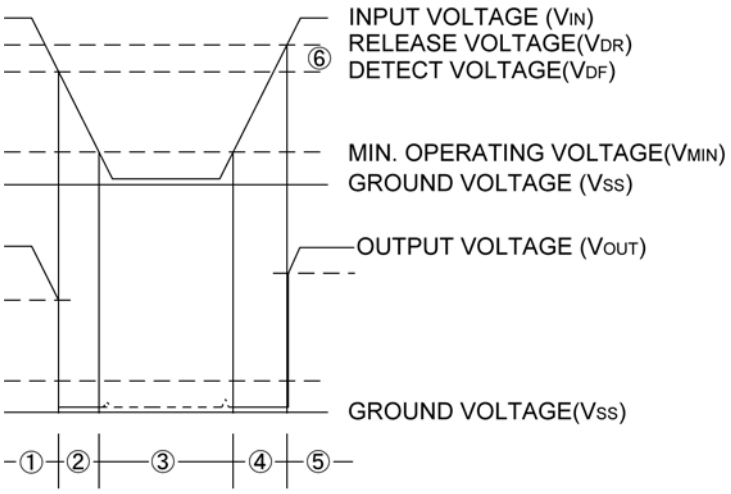
③ When input voltage (V_{IN}) falls to a level below that of the minimum operating voltage (V_{MIN}), output will become unstable. In this condition, V_{IN} will equal the pulled-up output (should output be pulled-up.)

④ When input voltage (V_{IN}) rises above the ground voltage (V_{SS}) level, output will be unstable at levels below the minimum operating voltage (V_{MIN}). Between the V_{MIN} and detect release voltage (V_{DR}) levels, the ground voltage (V_{SS}) level will be maintained.

⑤ When input voltage (V_{IN}) rises above detect release voltage (V_{DR}), output voltage (V_{OUT}) will be equal to V_{IN}.
(A condition of high impedance exists with N-ch open drain output configurations.)

⑥ The difference between V_{DR} and V_{DF} represents the hysteresis range.

●Timing Chart



■NOTES ON USE

1. Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.
2. When a resistor is connected between the VIN pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at RIN if load current (IOUT) exists. (refer to the Oscillation Description (1) below)
3. When a resistor is connected between the VIN pin and the input with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (IOUT) does not exist. (refer to the Oscillation Description (2) below)
4. With a resistor connected between the VIN pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the VIN pin.
5. In order to stabilize the IC's operations, please ensure that VIN pin's input frequency's rise and fall times are more than several μ sec / V.
6. Please use N-ch open drains configuration, when a resistor RIN is connected between the VIN pin and power source. In such cases, please ensure that RIN is less than 10kΩ and that C is more than 0.1μF.

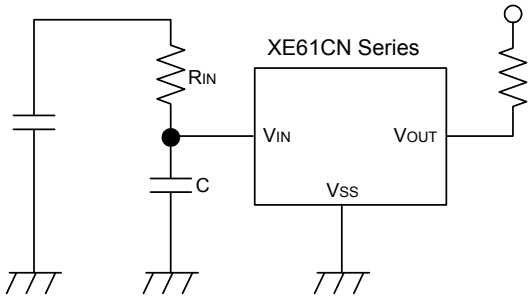


Figure 1: Circuit using an input resistor

●Oscillation Description

(1) Output current oscillation with the CMOS output configuration

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (IOUT) will flow at RL. Because a voltage drop (RIN x IOUT) is produced at the RIN resistor, located between the input (IN) and the VIN pin, the load current will flow via the IC's VIN pin. The voltage drop will also lead to a fall in the voltage level at the VIN pin. When the VIN pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at RIN will disappear, the voltage level at the VIN pin will rise and release operations will begin over again.

Oscillation may occur with this " release - detect - release " repetition.

Further, this condition will also appear via means of a similar mechanism during detect operations.

(2) Oscillation as a result of through current

Since the XE61C series are CMOS IC s, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (RIN) during release voltage operations. (refer to Figure 3)

Since hysteresis exists during detect operations, oscillation is unlikely to occur.

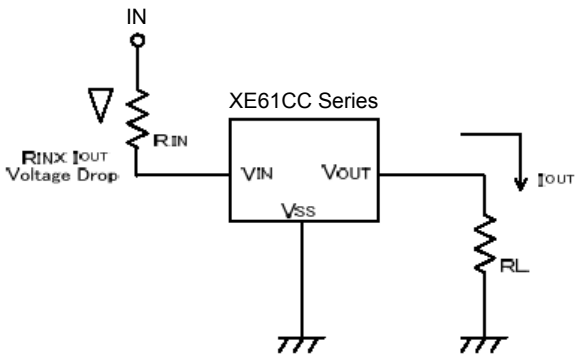


Figure 2: Oscillation in relation to output current

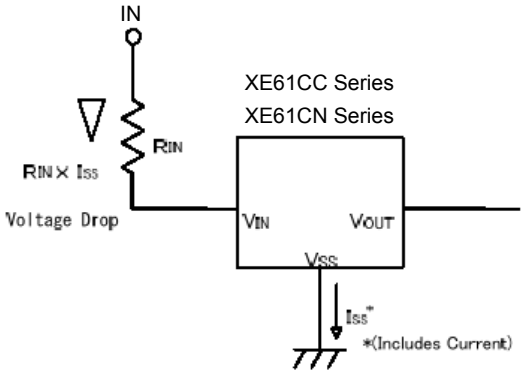
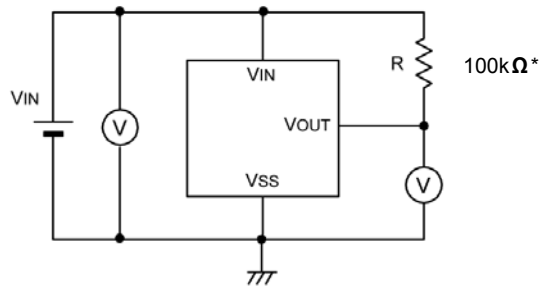


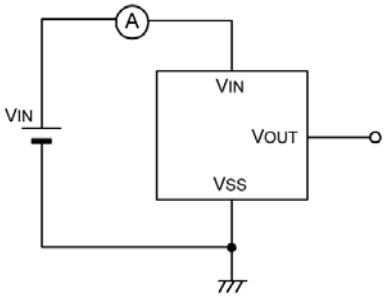
Figure 3: Oscillation in relation to through current

■ TEST CIRCUITS

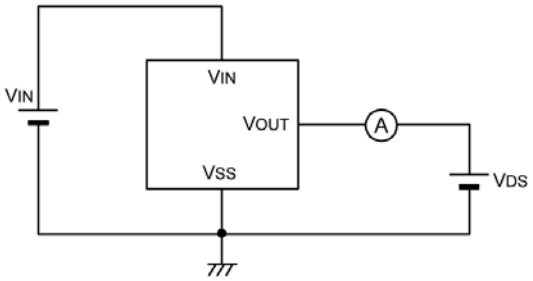
Circuit 1



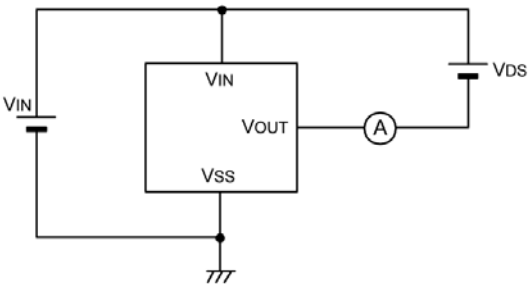
Circuit 2



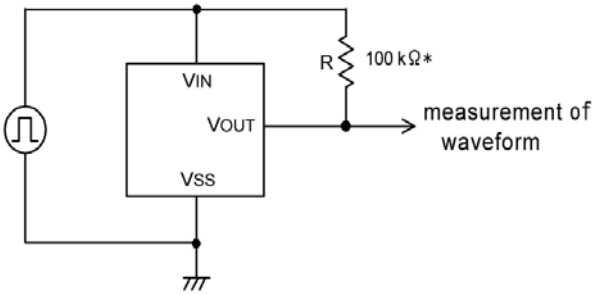
Circuit 3



Circuit 4



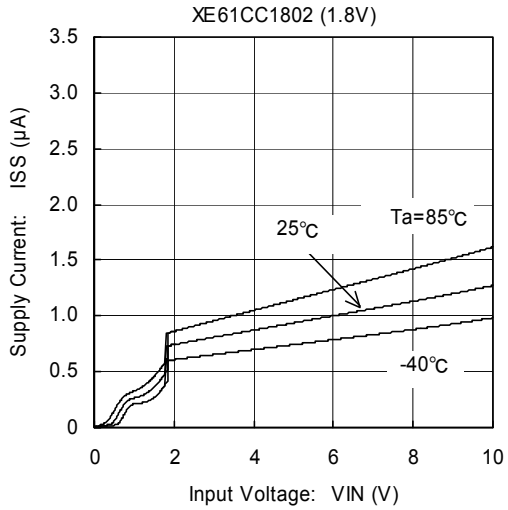
Circuit 5

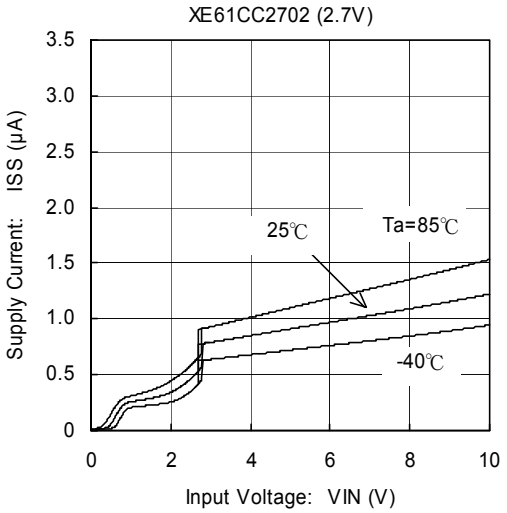


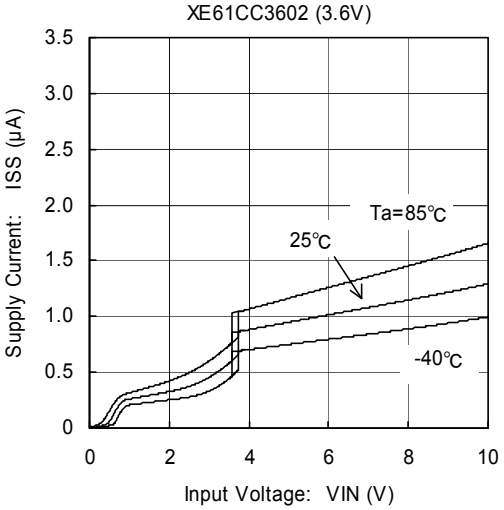
* : A resistor is not necessary with CMOS output products.

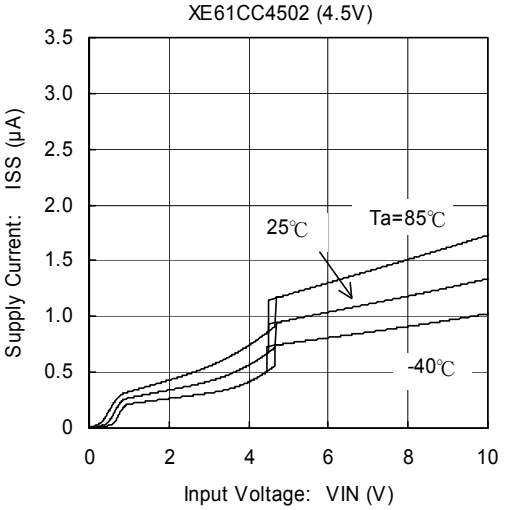
■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Supply Current vs. Input Voltage

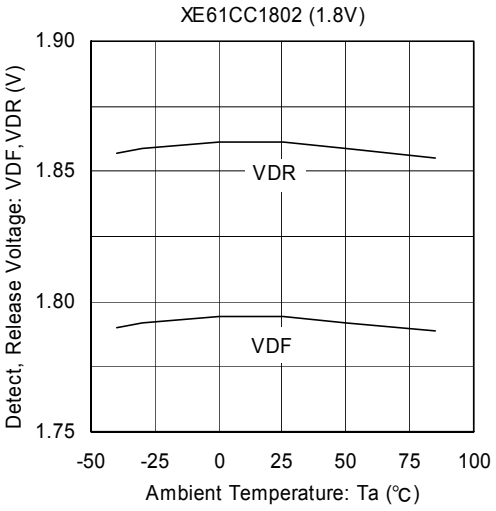


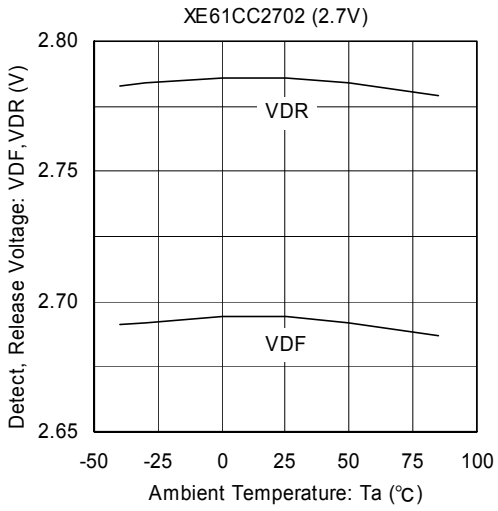






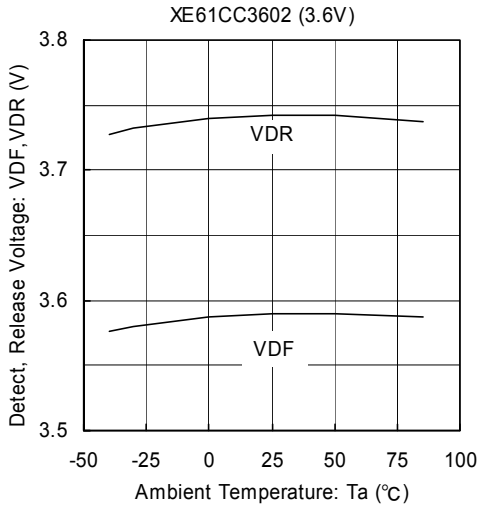
(2) Detect, Release Voltage vs. Ambient Temperature

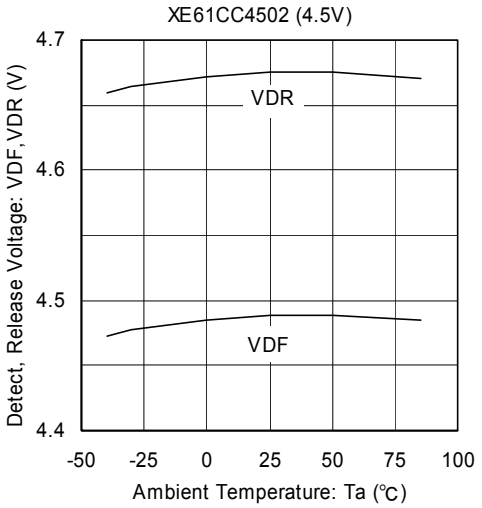




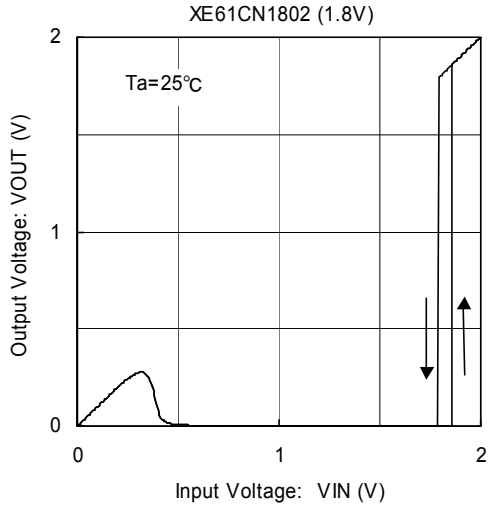
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

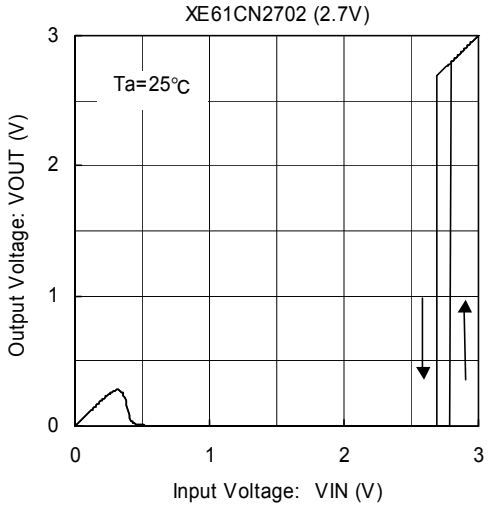
(2) Detect, Release Voltage vs. Ambient Temperature (Continued)

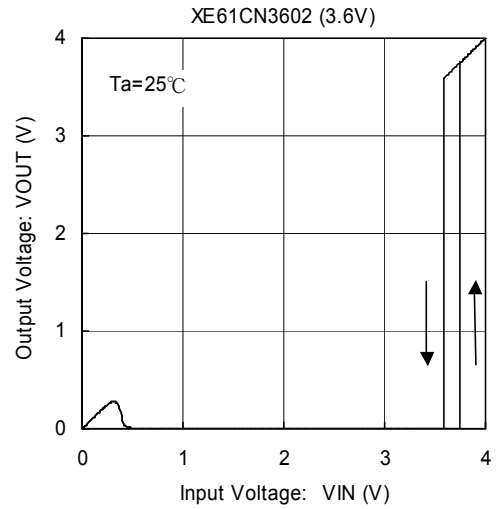


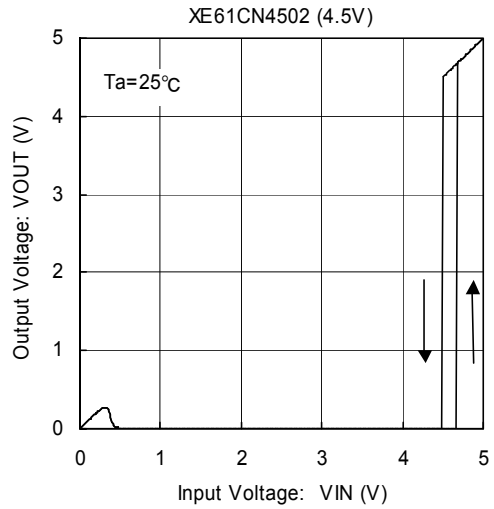


(3) Output Voltage vs. Input Voltage







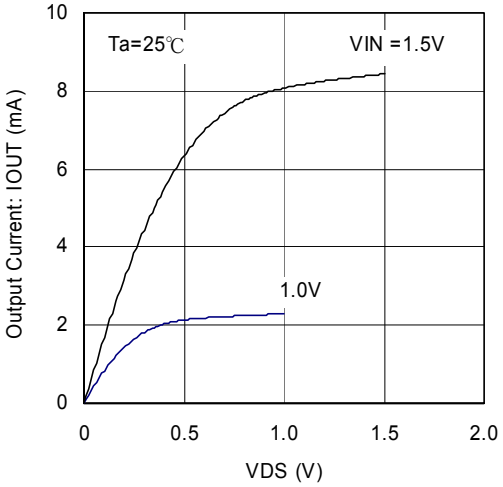


* Unless otherwise stated, the pull-up resistor's value of the N-ch open drain output type is 100kΩ.

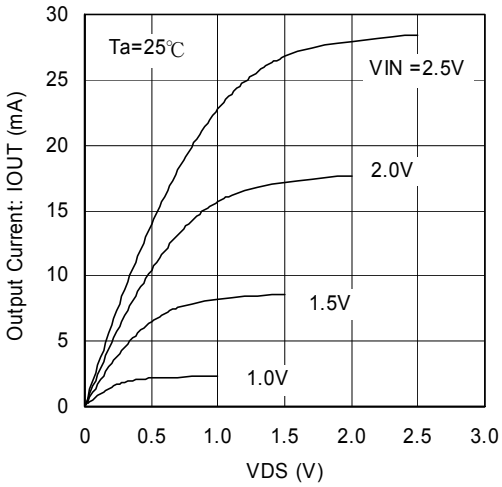
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(4) N-ch Driver Output Current vs. VDS Characteristics

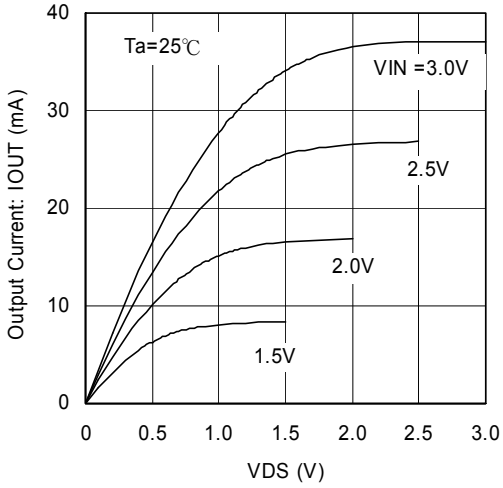
XE61CC1802 (1.8V)



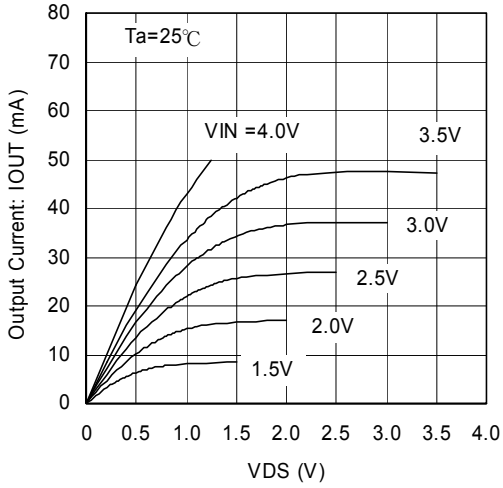
XE61CC2702 (2.7V)



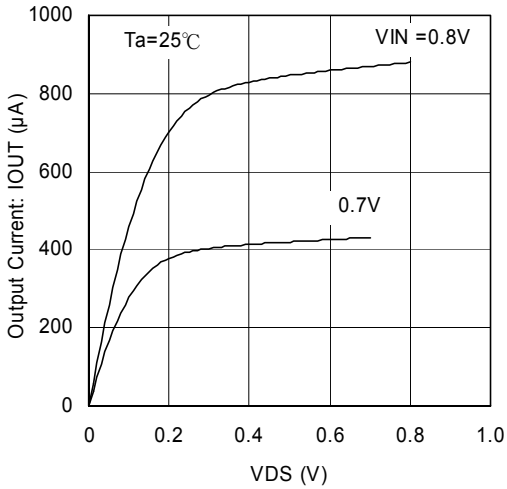
XE61CC3602 (3.6V)



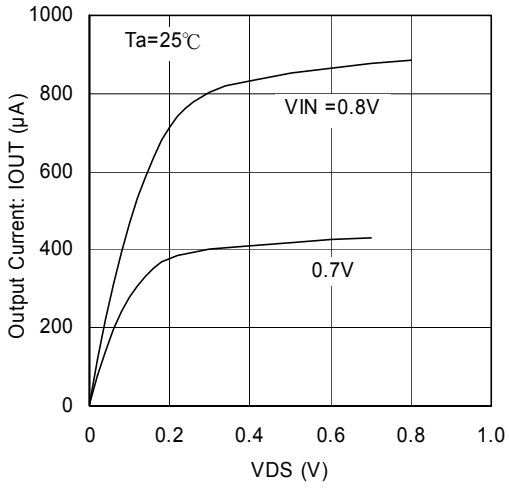
XE61CC4502 (4.5V)



XE61CC1802 (1.8V)

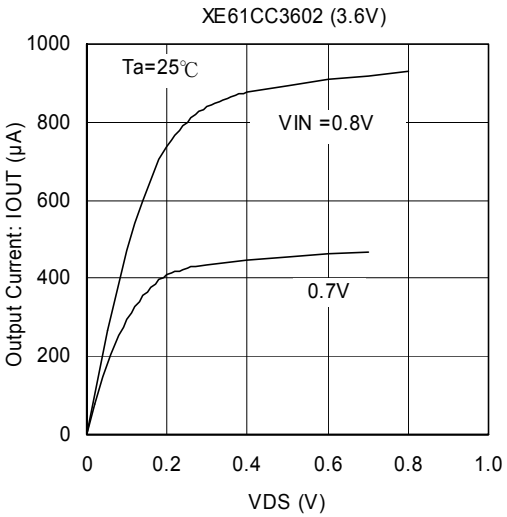


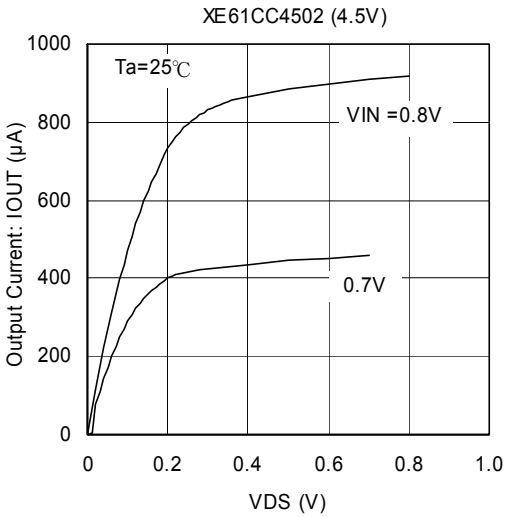
XE61CC2802 (2.7V)



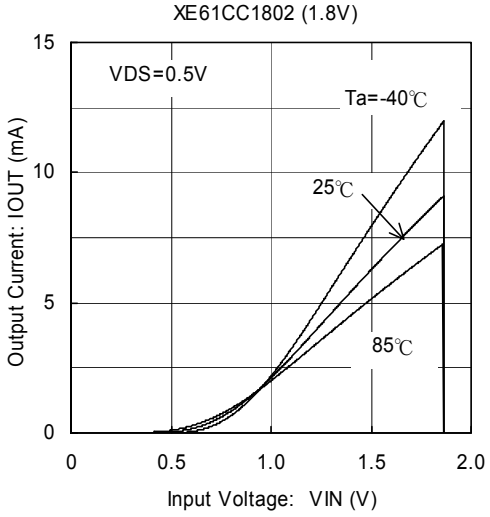
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

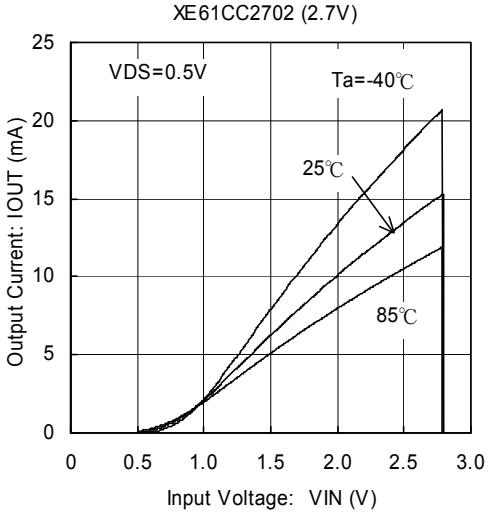
(4) N-ch Driver Output Current vs. V_{DS} Characteristics (Continued)

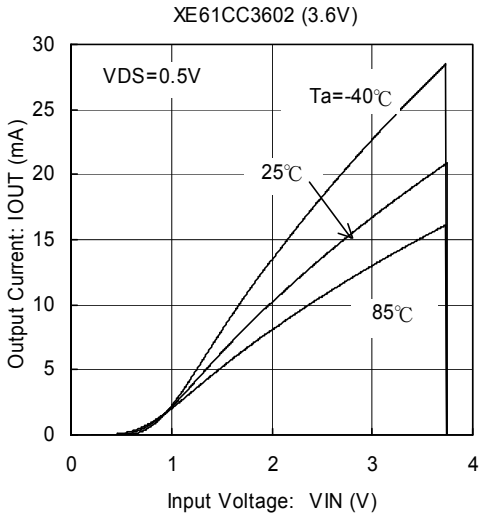


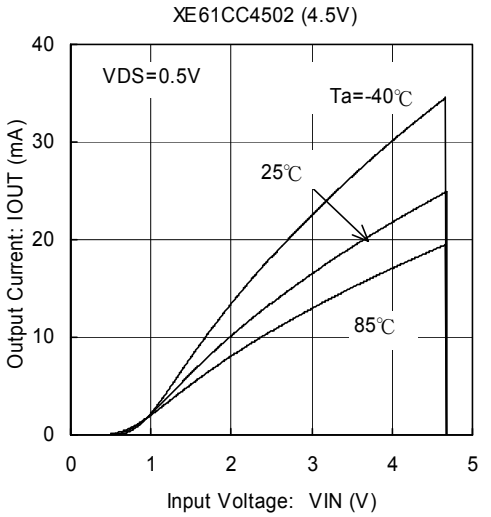


(5) N-ch Driver Output Current vs. Input Voltage





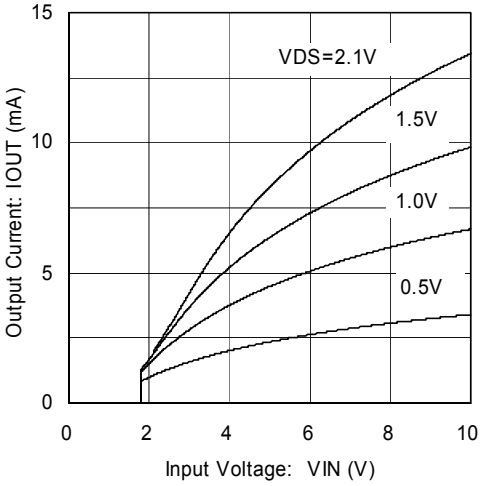




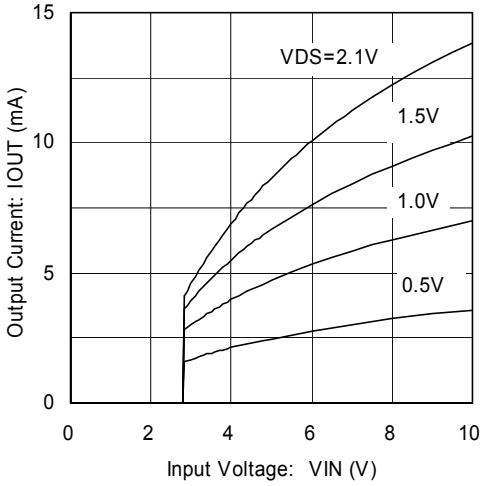
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(6) P-ch Driver Output Current vs. Input Voltage

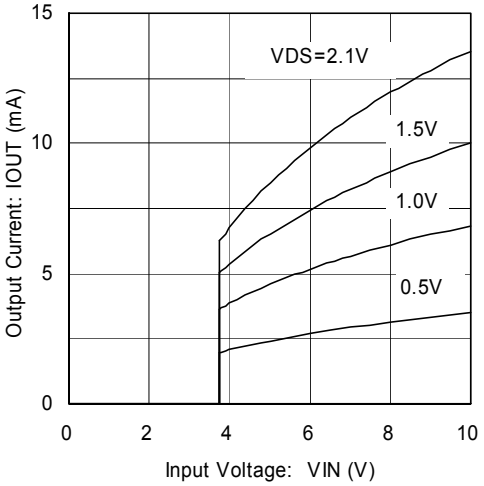
XE61CC1802 (1.8V)



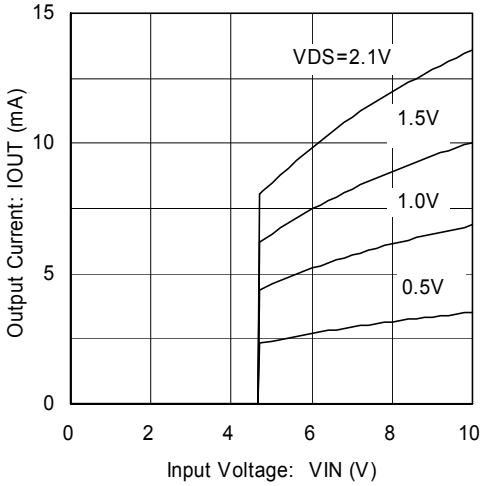
XE61CC2702 (2.7V)



XE61CC3602 (3.6V)



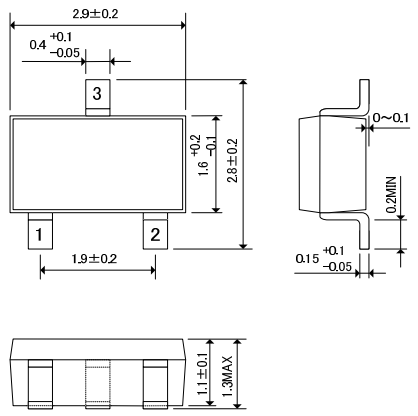
XE61CC4502 (4.5V)



■PACKAGING INFORMATION

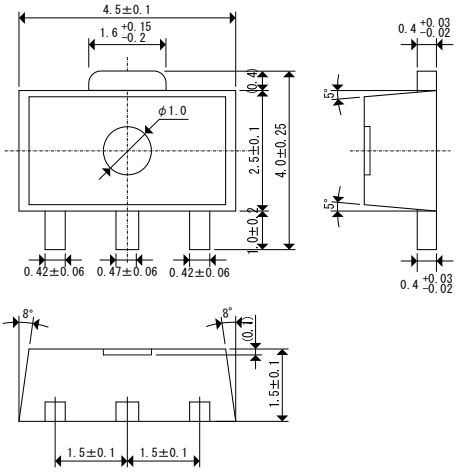
●SOT-23

(unit : mm)



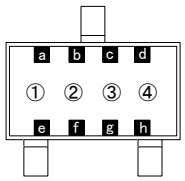
●SOT-89

(unit : mm)

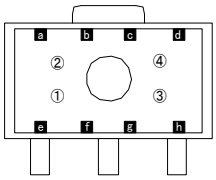


■MARKING RULE

●SOT-23, SOT-89



SOT-23
(TOP VIEW)



SOT-89
(TOP VIEW)

① represents integer of output configuration and detect voltage

XE61CC Series (CMOS Output)

MARK	VOLTAGE (V)	PRODUCT SEIRES
B	1.x	XE61CC1xxxxx
C	2.x	XE61CC2xxxxx
D	3.x	XE61CC3xxxxx
E	4.x	XE61CC4xxxxx
F	5.x	XE61CC5xxxxx
H	6.x	XE61CC6xxxxx

XE61CN Series (N-ch Open Drain Output)

MARK	VOLTAGE (V)	PRODUCT SERIES
L	1.x	XE61CN1xxxxx
M	2.x	XE61CN2xxxxx
N	3.x	XE61CN3xxxxx
P	4.x	XE61CN4xxxxx
R	5.x	XE61CN5xxxxx
S	6.x	XE61CN6xxxxx

② represents decimal number of detect voltage

MARK	VOLTAGE (V)	PRODUCT SEIRES
3	x.3	XE61Cxxx3xxx
0	x.0	XE61Cxxx0xxx

③ represents delay time

MARK	DELAY TIME	PRODUCT SERIES
3	No Delay	XE61Cxxxx0xx

④ represents production lot number

Based on internal standard. (G, I, J, O, Q, W excluded)

Bar Mark: a, b, c, d

PRODUCTION YEAR	a	b	c	d
xxx0	□	-	-	-
xxx1	-	□	-	-
xxx2	-	-	□	-
xxx3	-	-	-	□
xxx4	□	□	-	-
xxx5	□	-	□	-
xxx6	□	-	-	□
xxx7	-	□	□	-
xxx8	-	□	-	□
xxx9	-	-	□	□

Bar Mark: e, f, g, h

PRODUCTION MONTH	e	f	g	h
January	□	-	-	-
February	-	□	-	-
March	-	-	□	-
April	-	-	-	□
May	□	□	-	-
June	□	-	□	-
July	□	-	-	□
August	-	□	□	-
September	-	□	-	□
October	-	-	□	□
November	□	□	□	-
December	□	□	-	□

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4. The products in this datasheet are not developed, designed, or approved for use with such equipment whose failure of malfunction can be reasonably expected to directly endanger the life of, or cause significant injury to, the user.
   (e.g. Atomic energy; aerospace; transport; combustion and associated safety equipment thereof.)
5. Please use the products listed in this datasheet within the specified ranges.
   Should you wish to use the products under conditions exceeding the specifications, please consult us or our representatives.
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