SDIO PORT EXPANDER WITH VOLTAGE-LEVEL TRANSLATION

FEATURES

- **6-to-12 Demultiplexer/Multiplexer Allows SDIO Port Expansion**
- **Built-in Level Translator Eliminates Voltage Mismatch Between Baseband and SD Card or SDIO Peripheral**
- **V_{CCA}, V_{CCB0}, and V_{CCB1} Each Operate Over Full 1.1-V to 3.6-V Range**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance A Port**
  - **2000-V Human-Body Model (A114-B)**
  - **100-V Machine Model (A115-A)**
  - **1500-V Charged-Device Model (C101)**
- **±8-kV Contact Discharge IEC 61000-4-2 ESD Performance (B Port)**

DESCRIPTION/ORDERING INFORMATION

The TXS02612 is designed to interface the cell phone baseband with external SDIO peripherals. The device includes a 6-channel SPDT switch with voltage-level translation capability. This allows a single SDIO port to be interfaced with two SDIO peripherals. The TXS02612 has three separate supply rails that operate over the full range of 1.1 V to 3.6 V. This allows the baseband and SDIO peripherals to operate at different supply voltages if required.

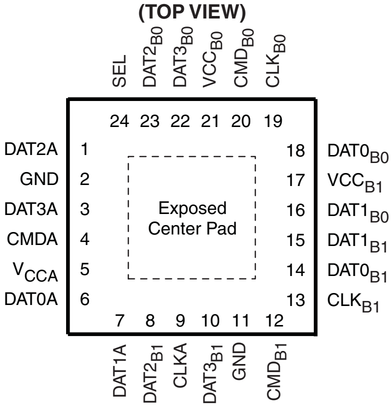
The select (SEL) input is used to choose between the B0 port and B1 port. When SEL = Low, B0 port is selected; when SEL = High, B1 port is selected. SEL is referenced to V_{CCA}. For the unselected B port, the clock output is held low, whereas the data and command I/Os are pulled high to their respective V_{CCB} through a 70-kΩ resistor (±30% tolerance).

ORDERING INFORMATION(1)

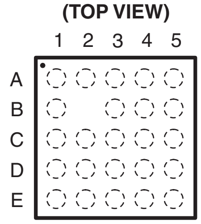
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	MicroStar Junior™ BGA (VFBGA) – ZQS	Reel of 3000	TXS02612ZQSR	YJ612
	QFN – RTW	Reel of 3000	TXS02612RTWR	YJ612

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

RTW PACKAGE (TOP VIEW)



ZQS PACKAGE (TOP VIEW)

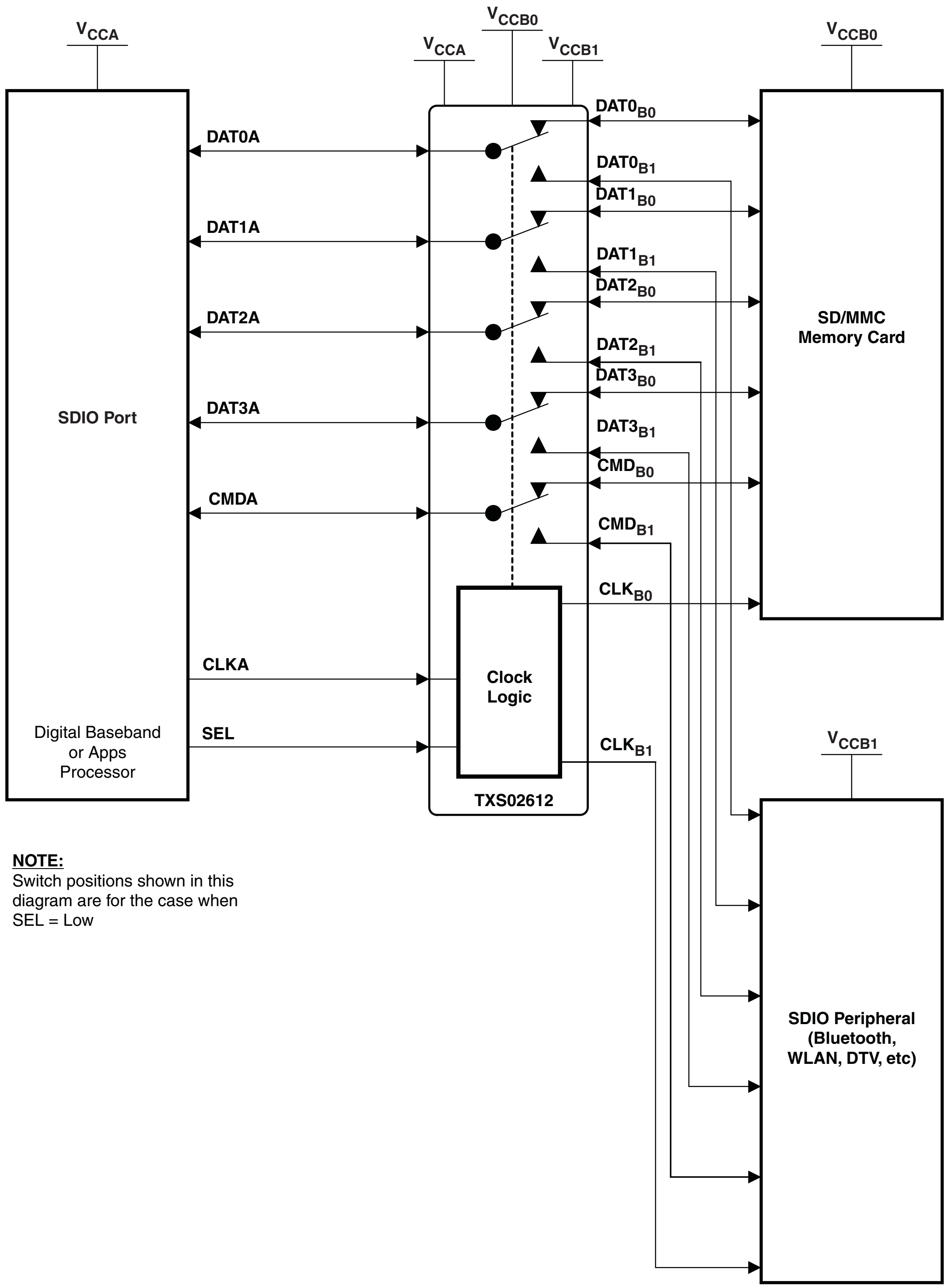


For RTW, if the exposed center pad is used, it must be connected to ground or electrically open.

Table 1. ZQS PACKAGE TERMINAL ASSIGNMENTS

	1	2	3	4	5
A	DAT2A	SEL	$DAT3_{B0}$	CMD_{B0}	CLK_{B0}
B	DAT3A		$DAT2_{B0}$	V_{CCB0}	$DAT0_{B0}$
C	CMDA	V_{CCA}	GND	$V_{CC\ B1}$	$DAT1_{B0}$
D	DAT0A	CLKA	GND	$DAT1_{B1}$	$DAT0_{B1}$
E	DAT1A	$DAT2_{B1}$	$DAT3_{B1}$	CMD_{B1}	CLK_{B1}

APPLICATION BLOCK DIAGRAM

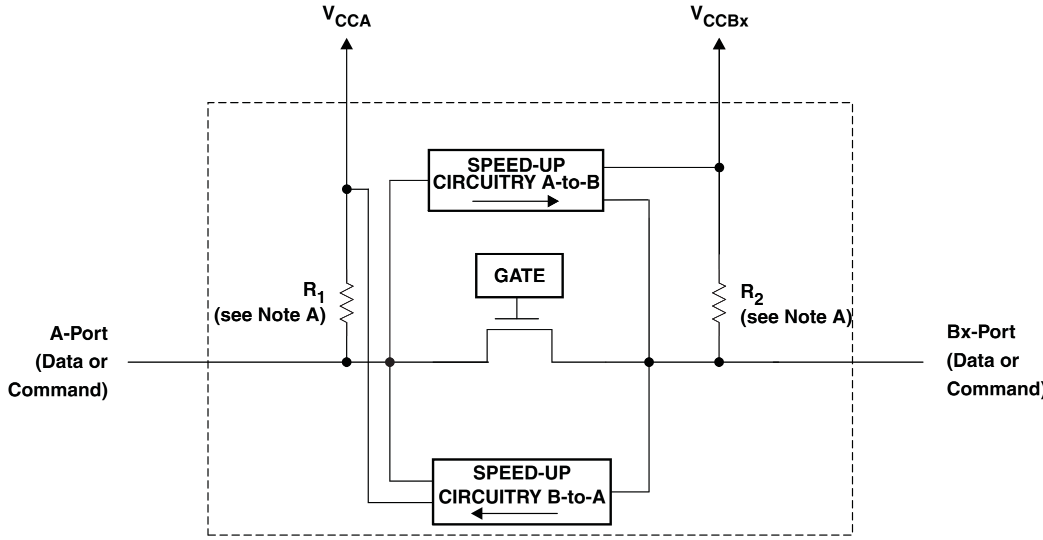


NOTE:
Switch positions shown in this diagram are for the case when SEL = Low

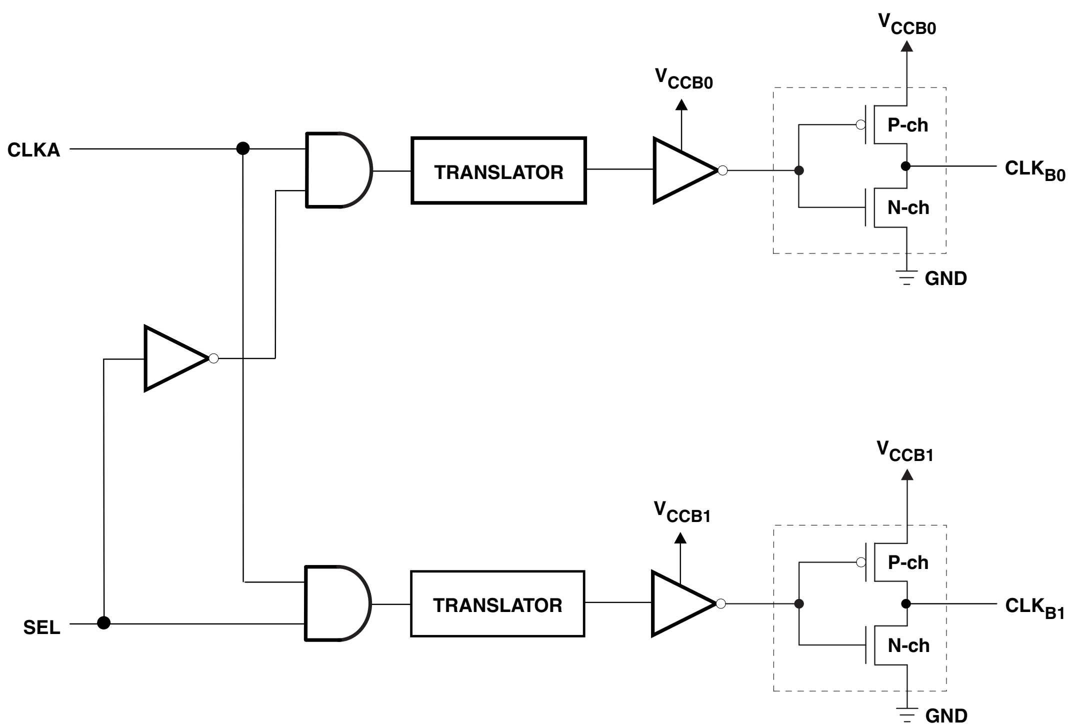
PIN ASSIGNMENTS

RTW PACKAGE PIN NO.	ZQS PACKAGE BALL NO.	NAME	FUNCTION	TYPE
1	A1	DAT2A	Data bit 2. Referenced to V_{CCA}.	I/O
3	B1	DAT3A	Data bit 3. Referenced to V_{CCA}.	I/O
4	C1	CMDA	Command bit. Referenced to V_{CCA}.	I/O
6	D1	DAT0A	Data bit 0. Referenced to V_{CCA}.	I/O
7	E1	DAT1A	Data bit 1. Referenced to V_{CCA}.	I/O
24	A2	SEL	Select pin to choose between B0 and B1. Referenced to V_{CCA}.	Input
	B2		Depopulated	
5	C2	V_{CCA}	A-port supply voltage. 1.1 V ≤ V_{CCA} ≤ 3.6 V.	Power
9	D2	CLKA	Clock input A. Referenced to V_{CCA}.	Input
8	E2	$DAT2_{B1}$	Data bit 2. Referenced to V_{CCB1}.	I/O
22	A3	$DAT3_{B0}$	Data bit 3. Referenced to V_{CCB0}.	I/O
23	B3	$DAT2_{B0}$	Data bit 2. Referenced to V_{CCB0}.	I/O
2	C3	GND	Ground	
11	D3	GND	Ground	
10	E3	$DAT3_{B1}$	Data bit 3. Referenced to V_{CCB1}.	I/O
20	A4	CMD_{B0}	Command bit. Referenced to V_{CCB0}.	I/O
21	B4	V_{CCB0}	B0-port supply voltage. 1.1 V ≤ V_{CCB0} ≤ 3.6 V.	Power
17	C4	V_{CCB1}	B1-port supply voltage. 1.1 V ≤ V_{CCB1} ≤ 3.6 V.	Power
15	D4	$DAT1_{B1}$	Data bit 1. Referenced to V_{CCB1}.	I/O
12	E4	CMD_{B1}	Command bit. Referenced to V_{CCB1}.	I/O
19	A5	CLK_{B0}	Clock output. Referenced to V_{CCB0}.	Output
18	B5	$DAT0_{B0}$	Data bit 0. Referenced to V_{CCB0}.	I/O
16	C5	$DAT1_{B0}$	Data bit 1. Referenced to V_{CCB0}.	I/O
14	D5	$DAT0_{B1}$	Data bit 0. Referenced to V_{CCB1}.	I/O
13	E5	CLK_{B1}	Clock output. Referenced to V_{CCB1}.	Output

SIMPLIFIED INTERNAL STRUCTURE



Simplified Architecture of Command and Each Data Path



Simplified Architecture of the Clock Path

A. R_1 and R_2 resistor values are determined based upon the logic level applied to the A port or B port, as follows:
R_1 and R_2 = 40 kΩ when a logic level low is applied to the A port or B port.
R_1 and R_2 = 4 kΩ when a logic level high is applied to the A port or B port.
R_1 and R_2 = 70 kΩ when the port is deselected.

FUNCTION TABLE

Clock Channel			
SEL	**CLKB0**	**CLKB1**	**OPERATION**
L	Active	Low	CLKA to CLKB0
H	Low	Active	CLKA to CLKB1

Data and Command Channel			
SEL	**DATxB0 or CMDxB0**	**DATxB1 or CMDxB1**	**OPERATION**
L	Active	Disabled, pulled to V_{CCB1} through 70 kΩ	DATxA to DATxB0, CMDA to CMDB0
H	Disabled, pulled to V_{CCB0} through 70 kΩ	Active	DATxA to DATxB1, CMDA to CMDB1

ABSOLUTE MAXIMUM RATINGS[(1)] [(2)]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB0} V_{CCB1}	Supply voltage range[(2)]		–0.5	4.6	V
V_I	Input voltage range	A port, B0 port, B1 port, control inputs	–0.5	V_{CCx} + 0.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port, B0 port, B1 port	–0.5	V_{CCx} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_{CC}/ I_{GND}	Continuous current through V_{CCA}, V_{CCB0}, V_{CCB1}, or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

PACKAGE THERMAL IMPEDANCE

PARAMETER				UNIT
θ_{JA}	Package thermal impedance	RTW package	66	°C/W
		ZQS package	171.6	

RECOMMENDED OPERATING CONDITIONS

			V_{CCA}	V_{CCBx} [(1)]	MIN	MAX	UNIT
V_{CCA} V_{CCB0} V_{CCB1}	Supply voltage				1.1	3.6	V
V_{IH}	High-level input voltage	A-port I/Os	1.1 V to 3.6 V	1.1 V to 3.6 V	V_{CCI} – 0.2	V_{CCI}	V
		B-port I/Os			V_{CCI} – 0.2	V_{CCI}	
		SEL, CLKA			V_{CCA} × 0.65 V	3.6	
V_{IL}	Low-level input voltage	A-port I/Os	1.1 V to 3.6 V	1.1 V to 3.6 V	0	0.15	V
		B-port I/Os			0	0.15	
		SEL, CLKA			0	V_{CCA} × 0.35	
Δt/Δv	Input transition rise or fall rate	CLK, SEL				10	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCBx} refers to V_{CCB0} and V_{CCB1}.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CCA}	V_{CCBx}	T_A = 25°C	T_A = –40°C to 85°C		UNIT
				TYP	MIN	MAX	
V_{OHA} (DATA & CMD)	I_{OH} = –20 μA, $V_{IBx} \geq V_{CCBx}$ – 0.2 V	1.1 V	1.1 V		0.74		V
		1.4 V	1.4 V		V_{CCA} × 0.67		
		1.65 V	1.65 V		V_{CCA} × 0.67		
		2.3 V	2.3 V		V_{CCA} × 0.67		
		3 V	3 V		V_{CCA} × 0.67		
V_{OLA} (DATA & CMD)	I_{OL} = 135 μA, $V_{IBx} \leq$ 0.15 V	1.1 V	1.1 V			0.35	V
	I_{OL} = 180 μA, $V_{IBx} \leq$ 0.15 V	1.4 V	1.4 V			0.35	
	I_{OL} = 220 μA, $V_{IBx} \leq$ 0.15 V	1.65 V	1.65 V			0.45	
	I_{OL} = 300 μA, $V_{IBx} \leq$ 0.15 V	2.3 V	2.3 V			0.55	
	I_{OL} = 620 μA, $V_{IBx} \leq$ 0.15 V	3 V	3 V			0.70	
V_{OHB} (DATA & CMD)	I_{OH} = –20 μA, $V_{IAx} \geq V_{CCAx}$ – 0.2 V	1.1 V	1.1 V		0.74		V
		1.4 V	1.4 V		V_{CCBx} × 0.67		
		1.65 V	1.65 V		V_{CCBx} × 0.67		
		2.3 V	2.3 V		V_{CCBx} × 0.67		
		3 V	3 V		V_{CCBx} × 0.67		
V_{OHCLKB}	I_{OH} = – 0.5 mA	1.1 V	1.1 V		0.74		V
	I_{OH} = – 1 mA	1.4 V	1.4 V		1.05		
	I_{OH} = – 2 mA	1.65 V	1.65 V		1.2		
	I_{OH} = – 4 mA	2.3 V	2.3 V		1.75		
	I_{OH} = – 8 mA	3 V	3 V		2.3		
V_{OLB} (DATA & CMD)	I_{OL} = 135 μA, $V_{IAx} \leq$ 0.15 V	1.1 V	1.1 V			0.35	V
	I_{OL} = 180 μA, $V_{IAx} \leq$ 0.15 V	1.4 V	1.4 V			0.35	
	I_{OL} = 220 μA, $V_{IAx} \leq$ 0.15 V	1.65 V	1.65 V			0.45	
	I_{OL} = 300 μA, $V_{IAx} \leq$ 0.15 V	2.3 V	2.3 V			0.55	
	I_{OL} = 620 μA, $V_{IAx} \leq$ 0.15 V	3 V	3 V			0.70	
V_{OLCLKB}	I_{OL} = 0.5 mA	1.1 V	1.1 V			0.35	V
	I_{OL} = 1 mA	1.4 V	1.4 V			0.35	
	I_{OL} = 2 mA	1.65 V	1.65 V			0.45	
	I_{OL} = 4 mA	2.3 V	2.3 V			0.55	
	I_{OL} = 8 mA	3 V	3 V			0.7	

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CCA}	V_{CCBx}	T_A = 25°C TYP	T_A = –40°C to 85°C MIN	T_A = –40°C to 85°C MAX	UNIT
I_I	SEL, CLKA	1.1 V to 3.6 V	1.1 V to 3.6 V	±1		±2	µA
	DAT, CMD			±1		±2	
I_{CCA}	$V_I = V_O$ = Open, I_O = 0, SEL, CLK = High or Low	1.1 V to 3.6 V	1.1 V to 3.6 V			12	µA
		3.6 V	0 V			12	
		0 V	3.6 V			–1	
I_{CCB0} or I_{CCB1}	$V_I = V_O$ = Open, I_O = 0, SEL, CLK = High or Low	1.1 V to 3.6 V	1.1 V to 3.6 V			24	µA
		3.6 V	0 V			–12	
		0 V	3.6 V			24	
C_i	SEL, CLKA	3.3 V	3.3 V	2.5		3.5	pF
C_{io}	A port	3.3 V	3.3 V	7		7.5	pF
	B port			9.5		10	

TIMING REQUIREMENTS

T_A = 25°C, V_{CCA} = 1.2 V

				V_{CCB} = 1.2 V TYP	V_{CCB} = 1.5 V TYP	V_{CCB} = 1.8 V TYP	V_{CCB} = 2.5 V TYP	V_{CCB} = 3.3 V TYP	UNIT
Data rate	Command	Push-pull driving		60	80	120	120	120	Mbps
		Open-drain driving		2	2	2	2	2	
	Clock	Push-pull driving		30	40	60	60	60	MHz
	Data	Push-pull driving		60	80	120	120	120	Mbps
t_w	Pulse duration	Push-pull driving	CLK	17	13	8	8	8	ns
		Open-drain driving	CMD	500	500	500	500	500	
		Push-pull driving	Data	17	13	8	8	8	
			CMD	17	13	8	8	8	

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

				V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Command	Push-pull driving		60		80		120		120		120	Mbps
		Open-drain driving		2		2		2		2		2	
	Clock	Push-pull driving		30		40		60		60		60	MHz
	Data	Push-pull driving		60		80		120		120		120	Mbps
t_w	Pulse duration	Push-pull driving	CLK	17	13		8		8		8		ns
		Open-drain driving	CMD	500	500		500		500		500		
		Push-pull driving	Data	17	13		8		8		8		
			CMD	17	13		8		8		8		

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

				V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Command	Push-pull driving		60		80		120		120		120	Mbps
		Open-drain driving		2		2		2		2		2	
	Clock	Push-pull driving		30		40		60		60		60	MHz
	Data	Push-pull driving		60		80		120		120		120	Mbps
t_w	Pulse duration	Push-pull driving	CLK	17	13		8		8		8		ns
		Open-drain driving	CMD	500	500		500		500		500		
		Push-pull driving	Data	17	13		8		8		8		
			CMD	17	13		8		8		8		

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

				V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Command	Push-pull driving		60		80		120		120		120	Mbps
		Open-drain driving		2		2		2		2		2	
	Clock	Push-pull driving		30		40		60		60		60	MHz
	Data	Push-pull driving		60		80		120		120		120	Mbps
t_w	Pulse duration	Push-pull driving	CLK	17	13		8		8		8		ns
		Open-drain driving	CMD	500	500		500		500		500		
		Push-pull driving	Data	17	13		8		8		8		
			CMD	17	13		8		8		8		

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

				V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Command	Push-pull driving		60		80		120		120		120	Mbps
		Open-drain driving		2		2		2		2		2	
	Clock	Push-pull driving		30		40		60		60		60	MHz
	Data	Push-pull driving		60		80		120		120		120	Mbps
t_w	Pulse duration	Push-pull driving	CLK	17	13		8		8		8		ns
		Open-drain driving	CMD	500	500		500		500		500		
		Push-pull driving	Data	17	13		8		8		8		
			CMD	17	13		8		8		8		

SWITCHING CHARACTERISTICS

T_A = 25°C, V_{CCA} = 1.2 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
t_{PD}	CMDA	CMDB	Push-pull driving	5.9	4.8	4.4	4	4.46	ns
			Open-drain driving	238	214	192	159	140	
	CMDB	CMDA	Push-pull driving	5.6	4.8	4.4	4.1	4	
			Open-drain driving	227	201	176	137	114	
	CLKA	CLKB	Push-pull driving	5.5	4.1	3.6	3.2	3	
	DATA	DATB	Push-pull driving	5.8	4.8	4.4	4.2	6.8	
	DATB	DATA		5.6	4.8	4.4	4.1	4	
	SEL	B-Port	Push-pull driving	13	11	10	9.4	9.1	
t_{rA}	A-port rise time		Push-pull driving	4.8	5.1	5.1	5.3	5.7	ns
t_{rB}	B-port rise time		Push-pull driving	6.1	3.8	2.9	1.9	1.5	
t_{rB}	CLKA	CLKB	Push-pull driving	5.2	3.4	2.6	1.7	1.3	
t_{fA}	A-port fall time		Push-pull driving	3.4	2.8	2.6	2.6	2.6	
t_{fB}	B-port fall time		Push-pull driving	4.2	3	2.3	1.7	1.5	
t_{fB}	CLKA	CLKB	Push-pull driving	3.1	2.1	1.6	1.2	1	
$t_{sk(O)}$	ChA-to-ChB skew		Push-pull driving	0.4	0.4	0.3	0.4	0.4	ns
	ChB-to-ChA skew		Push-pull driving	0.3	0.3	0.3	0.3	0.4	
	Channel-to-Clock skew		Push-pull driving	1.68	1.5	1.5	1.5	1.7	
Max data rate	Command		Push-pull driving	60	80	120	120	120	Mbps
			Open-drain driving	2	2	2	2	2	
	Clock		Push-pull driving	30	40	60	60	60	MHz
	Data		Push-pull driving	60	80	120	120	120	Mbps

SWITCHING CHARACTERISTICS

over operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PD}	CMDA	CMDB	Push-pull driving	5.1		13		9		8		7.5	ns
			Open-drain driving	210		777		756		684		758	
	CMDB	CMDA	Push-pull driving	4.5		10.6		9.2		8.5		8.2	
			Open-drain driving	200		616		560		433		375	
	CLKA	CLKB	Push-pull driving	4.7		13.1		9.8		6		5.2	
	DATA	DATB	Push-pull driving	5.1		13		9		8		7.8	
	DATB	DATA		4.5		11		9.3		8.8		8.4	
	SEL	B-Port	Push-pull driving	9.5		26		21		19		18	
t_{rA}	A-port rise time		Push-pull driving	2.7	1.5	5.8	1.7	5.9	1.7	6	1.8	6.1	ns
t_{rB}	B-port rise time		Push-pull driving	3.3	1.7	8.2	1.3	6.6	1	4.3	0.8	2.9	
t_{rB}	CLKA	CLKB	Push-pull driving	5.2	1.7	6.4	1.3	4.9	0.9	3.2	0.8	2.5	
t_{fA}	A-port fall time		Push-pull driving	2.4	1	3.9	0.9	3.4	0.9	3.2	1.3	3.3	ns
t_{fB}	B-port fall time		Push-pull driving	3.7	1.1	6.3	0.9	5.2	0.6	3.9	0.6	3.2	
t_{fB}	CLKA	CLKB	Push-pull driving	3.1	0.9	4.1	0.8	3.2	0.5	2.2	0.5	1.9	
$t_{sk(O)}$	ChA-to-ChB skew		Push-pull driving	0.32		0.47		0.58		0.63		0.63	ns
	ChB-to-ChA skew		Push-pull driving	0.27		0.24		0.23		0.22		0.22	
	Channel-to-Clock skew		Push-pull driving	1.47		1.66		1.68		1.82		1.77	
Max data rate	Command		Push-pull driving	60		80		120		120		120	Mbps
			Open-drain driving	2		2		2		2		2	
	Clock		Push-pull driving	30		40		60		60		60	MHz
	Data		Push-pull driving	60		80		120		120		120	Mbps

SWITCHING CHARACTERISTICS

over operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PD}	CMDA	CMDB	Push-pull driving	4.8		12		8		6		5.7	ns
			Open-drain driving	183		726		715		686		780	
	CMDB	CMDA	Push-pull driving	4		9		7		6.4		6	
			Open-drain driving	175		565		563		441		392	
	CLKA	CLKB	Push-pull driving	4.5		13		9		5.4		4.5	
	DATA	DATB	Push-pull driving	4.7		12		8.4		6		5.8	
	DATB	DATA		4.1		9		7.5		6.4		6.3	
	SEL	B-Port	Push-pull driving	8.2		22		17		14.8		14	
t_{rA}	A-port rise time		Push-pull driving	2	1.1	4	1.1	4.3	1.2	4.5	1.3	4.6	ns
t_{rB}	B-port rise time		Push-pull driving	6.2	1.7	7.9	1.2	6.2	1	4.3	0.8	3.1	
t_{rB}	CLKA	CLKB	Push-pull driving	5.2	1.7	6.4	1.3	4.9	0.9	3.2	0.8	2.5	
t_{fA}	A-port fall time		Push-pull driving	1.8	0.8	3.2	0.7	2.8	0.7	1.7	0.7	2.6	ns
t_{fB}	B-port fall time		Push-pull driving	3.5	1	5.6	0.9	3.5	0.6	1.9	0.6	3	
t_{fB}	CLKA	CLKB	Push-pull driving	3.1	0.9	4.1	0.8	3.2	0.5	2.2	0.5	1.9	
$t_{sk(O)}$	ChA-to-ChB skew		Push-pull driving	0.33		0.45		0.48		0.53		0.67	ns
	ChB-to-ChA skew		Push-pull driving	0.28		0.24		0.23		0.23		0.22	
	Channel-to-Clock skew		Push-pull driving	1.51		1.58		1.46		1.56		1.48	
Max data rate	Command		Push-pull driving	60		80		120		120		120	Mbps
			Open-drain driving	2		2		2		2		2	
	Clock		Push-pull driving	30		40		60		60		60	MHz
	Data		Push-pull driving	60		80		120		120		120	Mbps

SWITCHING CHARACTERISTICS

over operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PD}	CMDA	CMDB	Push-pull driving	4.4		11		7.4		4.4		3.8	ns
			Open-drain driving	143		544		596		605		669	
	CMDB	CMDA	Push-pull driving	3.8		7.6		5.5		4.2		3.7	
			Open-drain driving	137		434		444		414		372	
	CLKA	CLKB	Push-pull driving	4.1		12		8		4.8		3.8	
	DATA	DATB	Push-pull driving	4.4		11		7		4.5		3.8	
	DATB	DATA		4.4		8		5.5		4.1		3.7	
	SEL	B-Port	Push-pull driving	7		18		13		10.5		9	
t_{rA}	A-port rise time		Push-pull driving	1.4	0.75	2.2	0.74	2.2	1.06	2.6	0.7	2.8	ns
t_{rB}	B-port rise time		Push-pull driving	6.3	1.91	7.7	1.34	6.1	0.95	4.2	0.83	3.2	
t_{rB}	CLKA	CLKB	Push-pull driving	5.2	1.67	6.4	1.27	4.9	0.9	3.2	0.76	2.6	
t_{fA}	A-port fall time		Push-pull driving	1.1	0.58	1.9	0.58	2	0.61	1.9	0.57	1.9	ns
t_{fB}	B-port fall time		Push-pull driving	3.6	1.04	5.4	0.87	4.3	0.66	3.4	0.57	3	
t_{fB}	CLKA	CLKB	Push-pull driving	3.1	0.92	4.2	0.79	3.2	0.56	2.2	0.49	1.9	
$t_{sk(O)}$	ChA-to-ChB skew		Push-pull driving	0.41		0.43		0.39		0.59		0.68	ns
	ChB-to-ChA skew		Push-pull driving	0.41		0.24		0.2		0.19		0.18	
	Channel-to-Clock skew		Push-pull driving	2.11		1.47		1.3		1.25		1.21	
Max data rate	Command		Push-pull driving	60		80		120		120		120	Mbps
			Open-drain driving	2		2		2		2		2	
	Clock		Push-pull driving	30		40		60		60		60	MHz
	Data		Push-pull driving	60		80		120		120		120	Mbps

SWITCHING CHARACTERISTICS

over operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PD}	CMDA	CMDB	Push-pull driving	4.4		11		7		4.1		3.3	ns
t_{PD}	CMDA	CMDB	Open-drain driving	116		432		477		506		533	ns
t_{PD}	CMDB	CMDA	Push-pull driving	4.2		7.5		5.4		3.8		3	ns
t_{PD}	CMDB	CMDA	Open-drain driving	112		349		363		347		324	ns
t_{PD}	CLKA	CLKB	Push-pull driving	4.1		12		7.8		4.4		3.5	ns
t_{PD}	DATA	DATB	Push-pull driving	4.3		11		6.8		4		3.8	ns
t_{PD}	DATB	DATA	Push-pull driving	7.9		7.8		5.4		3.4		3	ns
t_{PD}	SEL	B-Port	Push-pull driving	6.4		16		11.5		8.8		7.6	ns
t_{rA}	A-port rise time		Push-pull driving	1.1	0.57	1.7	0.57	1.8	0.56	1.7	0.53	1.8	ns
t_{rB}	B-port rise time		Push-pull driving	6.2	1.96	7.7	1.43	6.1	0.95	4.2	0.71	3.1	ns
t_{rB}	CLKA	CLKB	Push-pull driving	5.2	1.67	6.4	1.26	4.9	0.91	3.3	0.76	2.5	ns
t_{fA}	A-port fall time		Push-pull driving	1	0.53	1.6	0.52	1.6	0.53	1.6	0.56	1.6	ns
t_{fB}	B-port fall time		Push-pull driving	3.4	0.95	5.2	0.8	4.1	0.63	3.2	0.58	2.9	ns
t_{fB}	CLKA	CLKB	Push-pull driving	3.1	0.92	4.1	0.79	3.2	0.56	2.2	0.49	1.9	ns
$t_{sk(O)}$	ChA-to-ChB skew		Push-pull driving	0.39		0.36		0.39		0.57		0.65	ns
$t_{sk(O)}$	ChB-to-ChA skew		Push-pull driving	0.45		0.3		0.19		0.19		0.18	ns
$t_{sk(O)}$	Channel-to-Clock skew		Push-pull driving	1.7		1.61		1.34		1.22		1.14	ns
Max data rate	Command		Push-pull driving	60		80		120		120		120	Mbps
Max data rate	Command		Open-drain driving	2		2		2		2		2	Mbps
Max data rate	Clock		Push-pull driving	30		40		60		60		60	MHz
Max data rate	Data		Push-pull driving	60		80		120		120		120	Mbps

OPERATING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

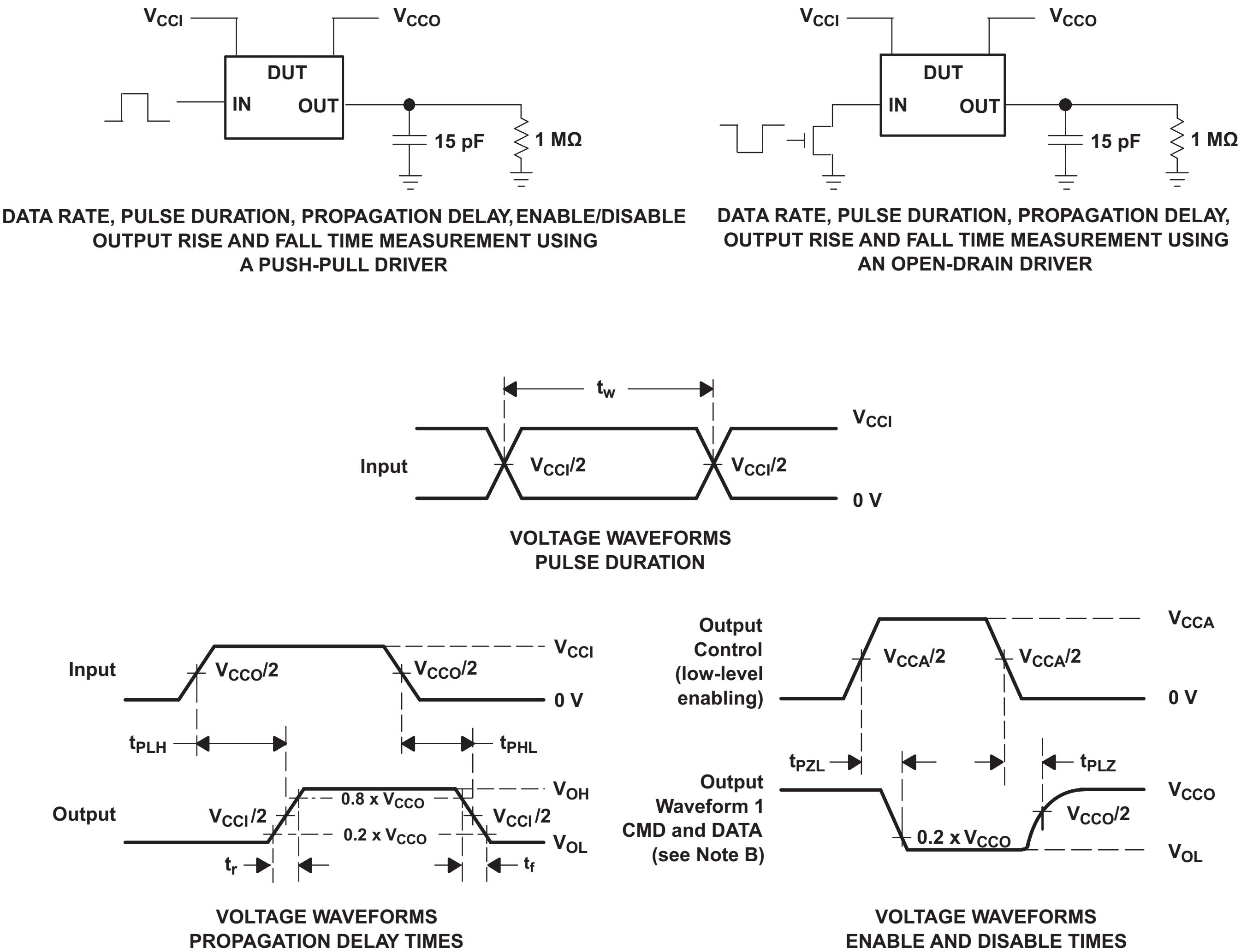
PARAMETER			TEST CONDITIONS	V_{CCA}					UNIT
				1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
				V_{CCB}					
				1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
				TYP	TYP	TYP	TYP	TYP	
Data and CMD	C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = outputs enabled	14.5	12.9	12.1	13.4	15	pF
Data and CMD	C_{pdA}	B-port input, A-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = outputs enabled	20.7	20.7	21	22	23.2	pF
Data and CMD	C_{pdB}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = outputs enabled	23.2	23.4	23.6	24.5	25.5	pF
Data and CMD	C_{pdB}	B-port input, A-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = outputs enabled	14.1	12.2	11.5	12.9	14.4	pF
Data and CMD	C_{pdB}	A-port input, B-port output	OE = outputs disabled	0.1	0.1	0.1	0.1	0.1	pF
Clock	C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = outputs enabled	0.4	0.4	0.4	0.5	0.7	pF
Clock	C_{pdB}	B-port input, A-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = outputs enabled	14	13.9	13.8	13.8	13.7	pF

POWER-UP CONSIDERATIONS

The following power-up sequence for this TXS02612 SDIO port expander with voltage-level translator should be followed to ensure proper operation and to avoid any unnecessary excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. The following power-up sequence should be used to safe-guard against these problems:

1. Connect the ground pin of the device first before any power-supply voltage is applied.
2. Connect and power up V_{CCA}, which internally powers up the SEL control logic of the TXS02612.
3. Depending on the port to be chosen, the SEL pin can be high or low. If SEL high is needed (i.e., A port to B_1 port), ramp the SEL pin with the V_{CCA} power supply. Otherwise, keep SEL Low.
4. Apply V_{CCB0} and V_{CCB1} only after the V_{CCA} power supply is applied.

PARAMETER MEASUREMENT INFORMATION



NOTES:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50Ω, dv/dt ≥ 1 V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. V_{CCI} is the V_{CC} associated with the input port.

I. V_{CCO} is the V_{CC} associated with the output port.

J. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TXS02612RTWR	ACTIVE	QFN	RTW	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TXS02612ZQSR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQS	24	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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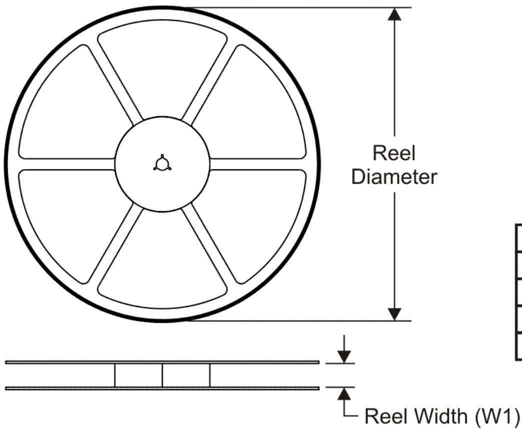
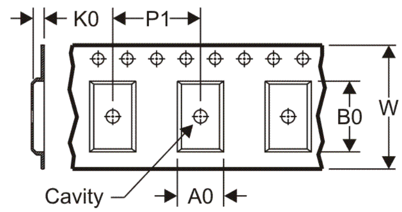
TAPE AND REEL INFORMATION

REEL DIMENSIONS

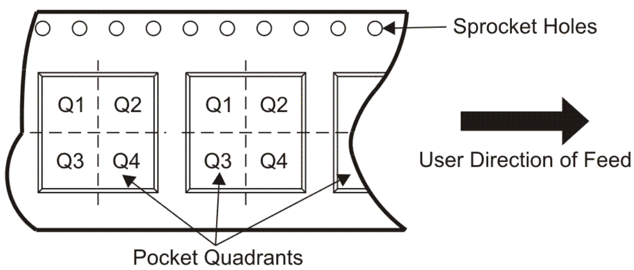


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

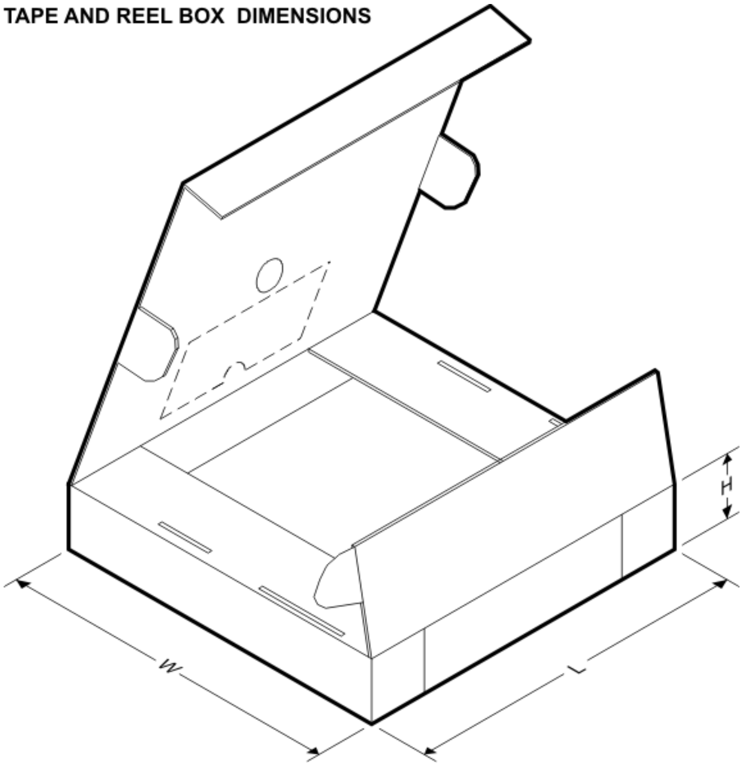
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS02612ZQSR	BGA MI CROSTA R JUNI OR	ZQS	24	2500	330.0	12.4	3.3	3.3	1.6	8.0	12.0	Q1

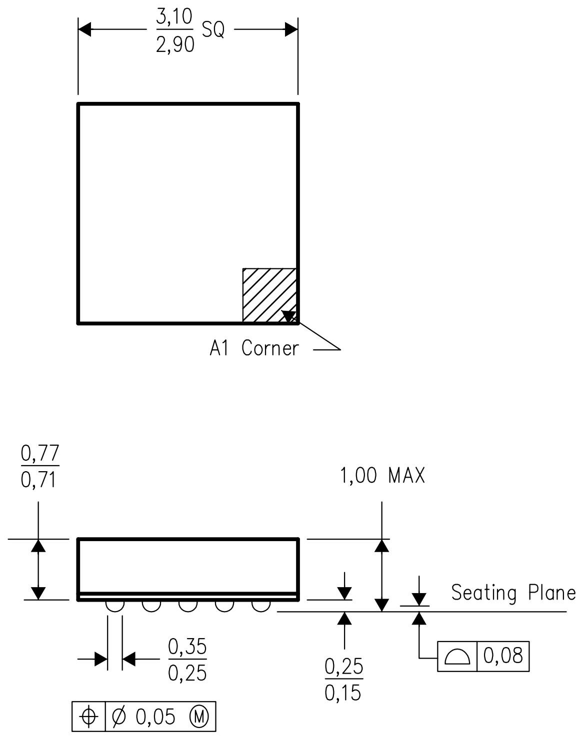
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS02612ZQSR	BGA MICROSTAR JUNIOR	ZQS	24	2500	340.5	338.1	20.6

ZQS (S–PBGA–N24) PLASTIC BALL GRID ARRAY



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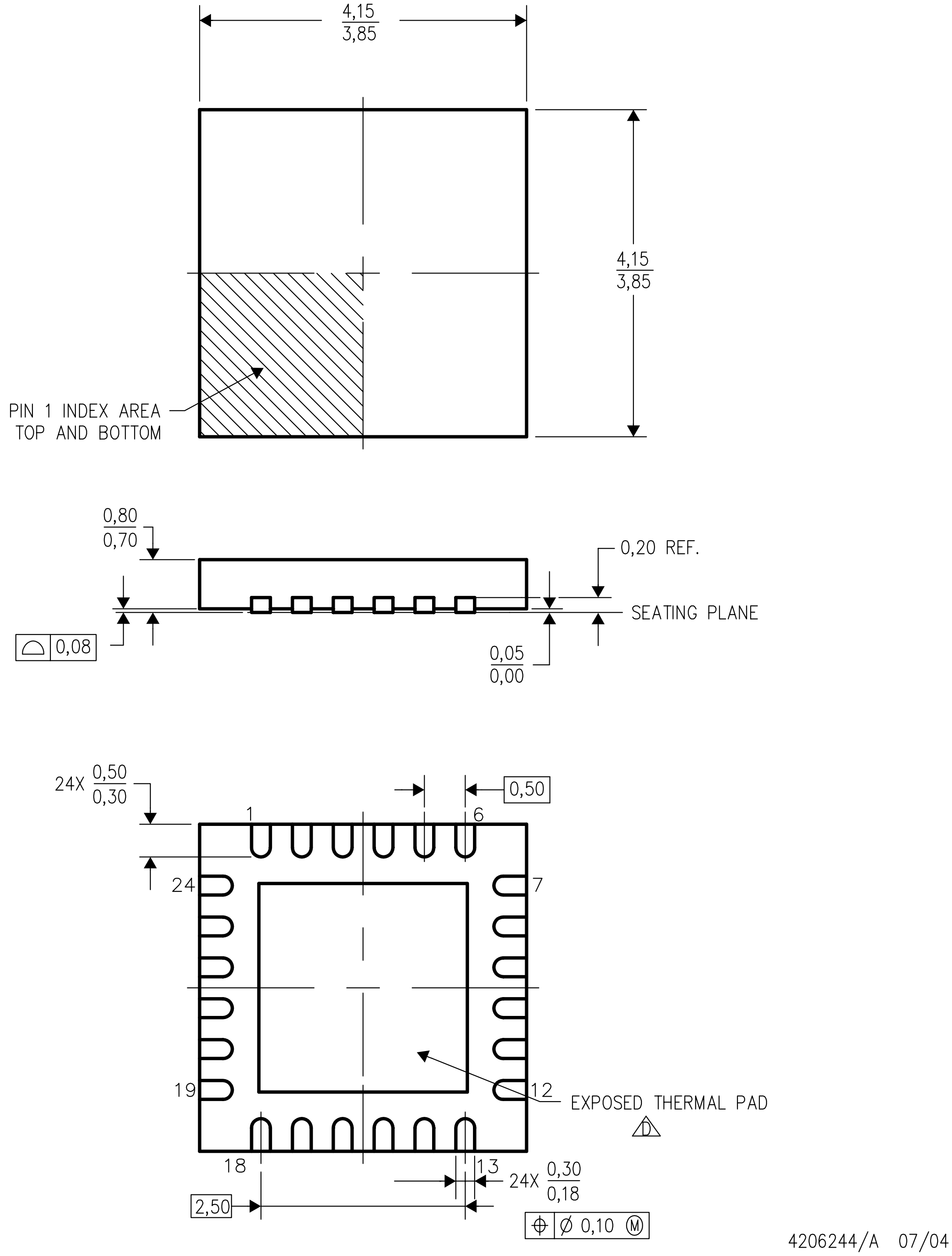
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO–225
- D. This package is lead–free.

RTW (S-PQFP-N24) PLASTIC QUAD FLATPACK



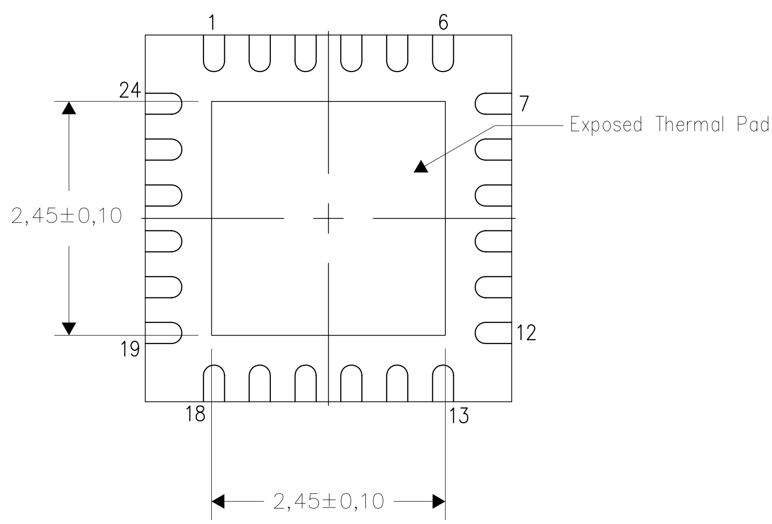
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

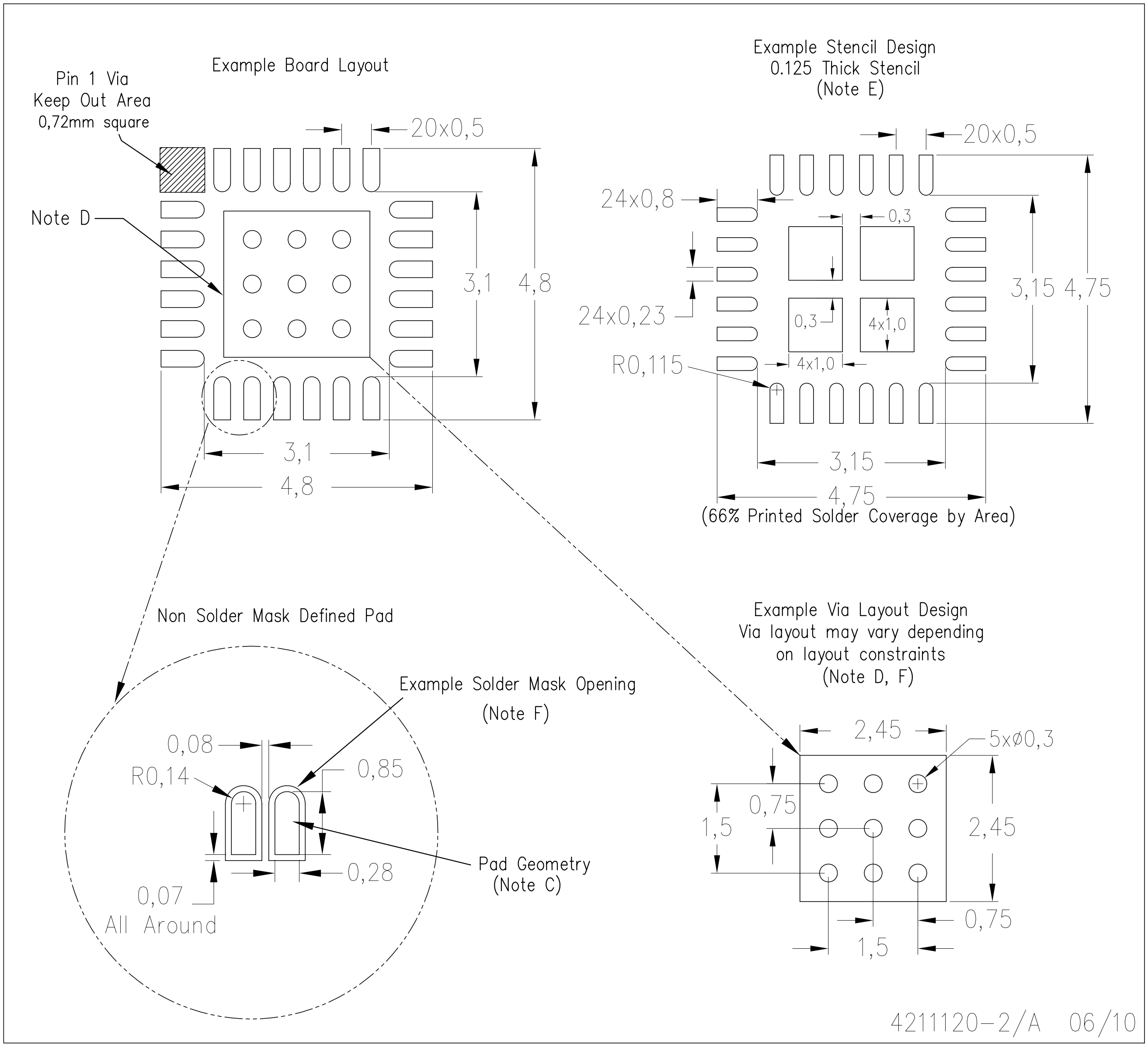


Bottom View

Exposed Thermal Pad Dimensions

NOTES:
1) All linear dimensions are in millimeters

RTW (S-PWQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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