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PI6050D Contact Image Sensor

Data Sheet

Key Features

- 600 or 1200 dots per inch (dpi) selectable resolutions
- 344 or 688 image sensor elements (pixels)
- 21.15μm (1200dpi) pixel center-to-center spacing (47.24 dots/mm)
- On-chip amplifier
- Single 5.0V power supply
- 3.3V input clocks
- 3.0 MHz maximum pixel rate
- Parallel / integrate and transfer
- Power down circuit
- High sensitivity
- Low power
- Low noise

General Description

Peripheral Imaging Corporation's PI6050D Contact Image sensor is a selectable 600 or 1200 dot per inch (dpi) resolution linear image sensor, which employs PIC's proprietary CMOS Image Sensing Technology. The sensor contains an on-chip output amplifier, power down circuitry and parallel transfer features that are uniquely combined with the present-day active-pixel-sensor technology. The image sensors are designed to be cascaded end-to-end on a printed circuit board (PCB) and packaged in an image sensing module. Applications for the sensor array includes facsimiles, PC scanners, check readers, and office automation equipment.

Figure 1 is a block diagram of the sensor. Each sensor consists of 688 active pixels, their associated multiplexing switches, buffers, and an output amplifier circuit with a power down feature. The sensors pixel-pixel spacing is approximately 21.15 μm. The size of each sensor without the scribe lines is 14560 μm by 425 μm.

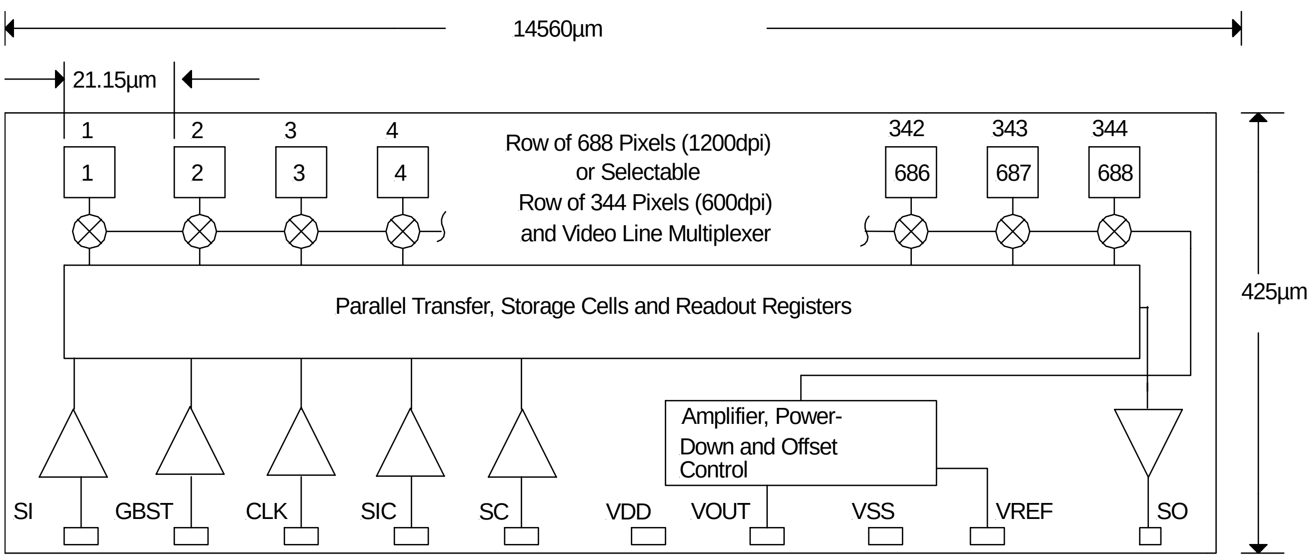


Figure 1. Sensor Block Diagram

PI6050D Unique Features

There are six unique features incorporated into the PI6050D which improve the sensor's performance.

1. Pixel-to-Pixel Offset Cancellation Circuit

The sensor employs a pixel-to-pixel offset cancellation circuit, which reduces the Fix Pattern Noise (FPN), and amplifier offsets. In addition, this innovative circuit design greatly improves the optical linearity and low noise sensitivity.

2. Parallel Integrate, Transfer and Hold

The sensor has a parallel integrate, transfer and hold feature, which allows the sensor to be read out while photon integration is taking place. These features are approached through the use of an integrate-and-hold cell, located at each pixel site. Each pixel's charge is read from its storage site as the sensor's shift register sequentially transfers each pixel's charge onto a common video line.

3. Dual Scan Initiation Inputs, GBST and SI

Each sensor has two scan initiation inputs, the Global Start Pulse (GBST) and the Start Pulse (SI), which are compatible with standard 3.3V CMOS clocks. These clocks help to reduce the sensor-to-sensor transition Fix Pattern Noise by initializing and preprocessing all sensors simultaneously before they start their readout scan. The internal shift register starts the scan after GBST is clocked in on the falling edge of the Clock input (CLK).

The Start Input Control (SIC) selects the first sensor in a sequence of cascaded sensors to operate with 55 clock cycles of delay by connecting it to Vdd and to Ground for all subsequent sensors. Then, only the first sensor clocks out 110 inactive pixels (55 clocks cycles) before accessing its first active pixel. During these 55 clock cycles, the first sensor and all of the subsequent cascaded sensors cycle through their pre-scan initialization process. After initialization, only the first sensor starts its read cycle with its first-active pixel appearing on the 56^{th} clock cycle. The second and subsequent sensors await the entry of their Start Pulse (SI). Furthermore, the first sensor's Start Pulse (SI) is left unconnected, while the subsequent sensors all have their Start Pulse's (SI) connected to the SO of their respective preceding sensor. The external scan Start Pulse (SI) is connected to all of the sensors' Global Start Pulse (GBST) inputs.

For example in the 1200 dpi mode, when the first sensor completes its scan, its End-Of-Scan (SO) appears on the falling edge of 389^{th} clock cycle after the entry of GBST and 20 pixels before its last pixel, in order to have a continuous pixel readout between sensors in a module. This SO enters as the SI clock of the second and subsequent sensors; hence all subsequent sensors will start their register scan after each of the preceding sensors completes its scan.

4. Power Saving

Each sensor incorporates a power-saving feature such that each chips amplifier is only turned on when its pixels are ready to be read out.

5. Common Reference Voltage between Cascaded Sensors

Each sensor has an input/output bias control (VREF), which serves as an offset voltage reference. Each bias control pad is connected to an internal bias source and tied to its own amplifier's reference bias input. In operation, these pads on every sensor are connected together. Each sensor then "shares" the same bias level to maintain a constant bias among all of the sensors.

6. Selectable Resolutions of 600 dpi or 1200 dpi

The Switch Control input (SC) is connected to Ground or to Vdd to set the sensor to operate in the 600 dpi or 1200 dpi mode, respectively. In the 1200 dpi mode, all 688 pixels are clocked out, whereas in the 600 dpi mode, pixels 1 and 2 are combined, 3 and 4 are combined and so on up to pixels 687 and 688 being combined. One half of the pixel amplifiers and one half of the scanning register are then disabled. As a result, sensitivity in the 600 dpi mode will be twice that of the 1200 dpi mode. The 600 dpi readout time will be approximately half of the 1200 dpi readout time. Unlike a CCD array, both the 600 dpi and 1200 dpi arrays can operate with the same clock frequency.

Functional Description

➢ **Input / Output Terminals**

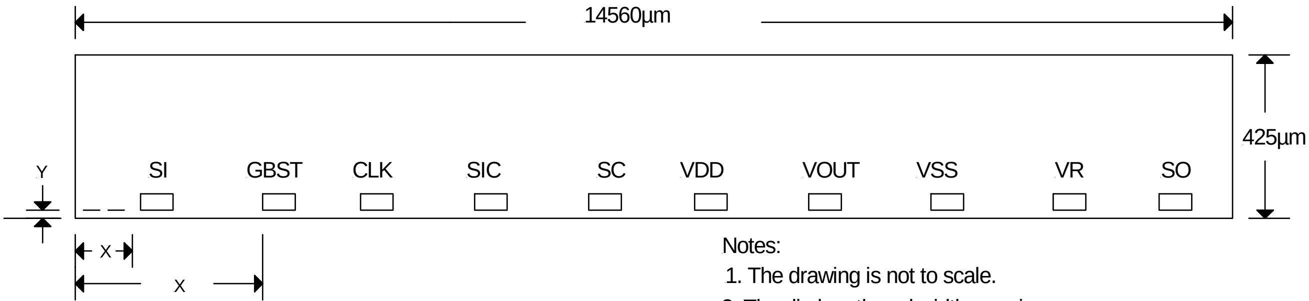
The PI6050D image sensor has 10 input and output (I/O) pads. Their symbols and function descriptions are listed in Table 1.

Signal	I/O	Description
SI	I	Start Pulse: Input to start a line scan. (See discussion of the sensors unique features for further details).
GBST	I	Global Start Pulse: Globally initializes the start inputs of all sensors and starts the scanning process of the first sensor. (See discussion of the sensors unique features for further details).
CLK	I	Clock: Clock input for the shift register.
SIC	I	Start Input Control: Input to control the Start Pulse to the first sensor. (See discussion of the sensors unique features for further details).
SC	I	Switch Control: Selects the 600 or 1200 dpi mode. (See discussion of the sensors unique features for further details).
VDD	I	Power Supply
VOUT	O	Video Output Voltage: Output video signal from the amplifier.
VSS	I	Ground
VREF	I/O	Reference Voltage: Reference input voltage for the amplifier output. Sets the output's reset (dark) level.
SO	O	End of Scan Pulse: Output from the shift register at the end of a scan.

Table 1. Input and Output Terminals

➢ Bonding Pad Layout Diagram

Figure 2 shows the bonding pad locations for the PI6050D sensor.

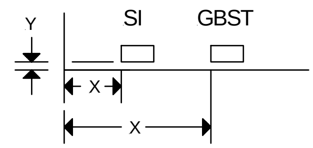


Pad Location Table

Pad	Location	Y	X
SI	Start Pulse	30	1000
GBST	Global Start Pulse	30	3442
CLK	Clock	30	4199
SIC	Start Input Control	30	4590
SC	Switch Control	30	4945
VDD	Power Supply	34	5414
VOUT	Video Output Voltage	30	5820
VSS	Ground	34	10549
VREF	Reference Voltage	30	10909
SO	End of Scan Pulse	30	13259

Notes:
1. The drawing is not to scale.
2. The die length and width are given in the above sensor die figure
3. Pad locations are listed in the Pad Location Table

eg.



4. Each pad is 120 x 80um
5. All dimensions are in um
6. Die size does not include the scribe line

Figure 2. PI6050D Bonding Pad Layout

➢ Wafer Scribe Line

Figure 3 outlines the scribe line dimensions surrounding the sensor die on a wafer.

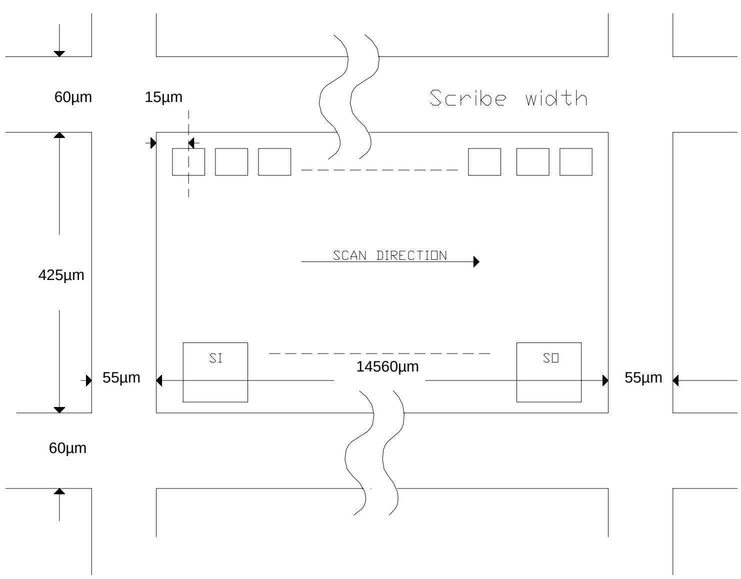


Figure 3. Wafer Scribe Line

Electro-Optical Specifications

Table 2 lists the electro-optical specifications of the PI6050D sensor at 25^{o}C and Vdd = 5.0 volts.

Parameter	Symbol	Min	Typ	Max	Units
Number of Pixels (1)		344 or 688		344 or 688	
Pixel-to-Pixel Spacing (1)		42.3 / 21.15		42.3 / 21.15	μm
Sensitivity @ 600 dpi (2) Sensitivity @ 1200 dpi	Sv		1220 610		V / uJ / cm2
Saturation Voltage (3)	VSat		1.65		Volts
Photo-Response Non-Uniformity (4)	Up			15	%
Adjacent Photo-Response Non-Uniformity (5)	Upn			15	%
Dark Output Voltage Level (6)	Vd		1.7		V
Dark Output Non-Uniformity (7)	Ud			100	mV
Random Thermal Noise (rms) (8)	Vno		3.0		mV
Sensor-to-Sensor Photo-Response Non-Uniformity (9)	Usensor			10	%
Photo Response Linearity (10)	PRL			2	%
Analog Output Drive Current	Iout		>1.0		mA

Table 2. Electro-Optical Specifications

- Notes for the above Table 2 are listed on the next page under “Definitions of Electro-Optical Specifications”.

Definitions of Electro-Optical Specifications

All electrical specifications are measured at a pixel rate of 2.5 MHz, a temperature of 25^{o}C, Vdd=5.0 volts, Vref=1.7V and at an integration time of 2.2ms for 600 dpi and 4.4ms for 1200 dpi. The average output voltage (Vpavg) is adjusted to approximately 1.0V, unless stated otherwise. The modules' internal Green LED (525 ± 20 nm) was used as the light source for measurements requiring illumination. As a guideline, the recommended load on the output should be 1KΩ<RL<10kΩ. All measurements were taken with a 2k ohm load on the output.

1. The Switch Control input (SC) is connected to Ground or to Vdd to set the sensor to operate in the 600 dpi or 1200 dpi mode, respectively. In the 1200 dpi mode, all 688 pixels are clocked out, whereas in the 600 dpi mode, pixels 1 and 2 are combined, 3 and 4 are combined and so on up to pixels 687 and 688 being combined. One half of the pixel amplifiers and one half of the scanning register are then disabled. As a result, sensitivity in the 600 dpi mode will be twice that of the 1200 dpi mode. The 600 dpi readout time will be approximately half of the 1200 dpi readout time.

2. Sensitivity (Sv) is defined as the slope of the Vpavg vs Exposure curve.

3. Saturation Voltage (VSat) is defined as the maximum video output voltage swing measured from the dark level to the saturation level. It is measured by using the module LED light source with the module imaging a uniform white target. The LED light level is increased until the output voltage no longer increases with an increase in the LED brightness. The dark level is set by the voltage on VREF and is recommended to be set externally to a voltage of 1.7V for optimal module operation.

4. Photo-Response Non-Uniformity (Up+, Up-, Up_total).
   Up+ = ((Vpmax-Vpavg)/Vpavg) x 100%, Up- = ((Vpavg-Vpmin)/Vpavg) x 100%, and Up_total is the absolute value of (Up+) + (Up-), where Vpmax is the maximum pixel output voltage in the light, Vpmin is the minimum pixel output voltage in the light and Vpavg is average output voltage of all pixels in the light.

5. Total Photo-Response Non-Uniformity (Up_total)

6. Adjacent Photo-Response Non-Uniformity (Upn).
   Upn = ABS(Max ((Vpn – Vpn+1) / Min (Vpn, Vpn+1))) x 100%, where Vpn is the pixel output voltage of pixel n in the light.

7. Dark Output Voltage (Vd).
   Vd is the average dark output level and is essentially the offset level of the video output in the dark. The dark level is set by the voltage on VREF and is recommended to be set externally to a voltage of 1.7V for optimal module operation.

8. Dark Output Non-Uniformity (Ud).
   Ud = Vdmax-Vdmin, where Vdmax is the maximum pixel output voltage in the dark and Vdmin is the minimum pixel output voltage in the dark.

9. Random Thermal Noise (rms), (Vno) is the standard deviation of n pixels in the dark. A sample size n = 64 was used. A 3 mV rms value has a peak-peak equivalent of 18 mV.

10. Sensor-to-Sensor Photo-Response Non-Uniformity (Usensor).
    Usensor = (Vpavg – Wavg) / Wavg), where Wavg is the average output of all sensors on the same wafer that pass all other specifications.

11. Photo-Response Linearity (PRL).
    Photo-Response Linearity is defined as the max deviation of response compared to a best fit line. The data points plotted are those that lie within 10% of the saturation level and 90% of the saturation level. Outside these ranges the module is approaching non-linearity.

Recommended Operating Conditions

Table 3 lists the recommended operating conditions @ 25°C.

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	Vdd	4.5	5.0	5.5	V
Clock Input Voltage high level (1)		3.1	3.3	3.5	V
Clock Input Voltage low level (1)		0	0	0.8	V
Power Supply Current	IDD (sensor selected) IDD (sensor not selected)		8 4	10 5	mA mA
Reference Voltage (2)	VREF	1.3	1.7	1.7	V
Clock Frequency (3)		0.25	1.25	1.5	MHz
Pixel Rate (4)		0.5	2.5	3.0	MHz
Integration Time (Line Scan Rate) (5) First Die Subsequent Die	Tint	248 230			μs μs / die
Clock Pulse Duty Cycle (6)			50		%

Table 3. Recommended Operating Conditions @ 25°C

Notes:

1. Applies to all clocks; GBST, SI and CLK. The CLK line having a capacitance of approximately 20 pF.

2. The dark level is set by the voltage on VREF and is recommended to be set externally to a voltage of 1.7V for optimal module operation.

3. Although the device will operate with a pixel rate of less than 500 KHz, it is recommended that the device be operated above 500 KHz to maintain performance characteristics. Operating below 500 KHz may result in leakage current degradation.

4. 2 pixels are clocked out for every clock cycle.

5. Tint is the integration time of a single sensor and is the time between two Start Pulses. The minimum integration time is the time it takes to clock out 55 inactive pixels and 688 active pixels for the 1200 dpi mode, or 55 inactive pixels and 344 active pixels for the 600 dpi mode, at a given frequency.

   However, if several sensors are cascaded together in a module then the minimum integration time for the 1200 dpi mode is the time it takes to clock out 55 inactive pixels and 688 active pixels from the first sensor and 688 pixels from each of all subsequent sensors, at a given frequency.

   Similarly, for cascaded sensors in the 600 dpi mode, the minimum integration time is the time it takes to clock out 55 inactive pixels and 344 active pixels from the first sensor and 344 pixels from each of all subsequent sensors, at a given frequency.

6. The clock duty cycle is defined as the ratio of the positive duration of the clock to its period.

Absolute Maximum Ratings

Table 4 lists the absolute maximum ratings.

Parameter	Max	Units
Power Supply Voltage (Vdd)	8	V
Clock Input Voltage high level [1]	Vdd + 0.5	V
Clock Input Voltage low level [1]	-0.5	V
Operating Temperature	-10 to +50	°C
Operating Humidity	+10 to +85	RH%
Storage Temperature	-25 to +75	°C
Storage Humidity	+10 to +90	RH%

Table 4. Absolute Maximum Ratings

Note

1. Applies to all clocks; GBST, SI and CLK.

2. Timing Requirements

Table 5 lists the timing requirements for the 600 and 1200 dpi modes, and their associated timing diagrams are shown in figures 4-9.

Parameter	Symbol	Min	Typ	Max	Units
Clock (CLK) Period	CLKp	666	800	4000	ns
Clock (CLK) Pulse Width	CLKpw		400		ns
Clock (CLK) Duty Cycle			50		%
Data Setup Time (1)	Tset	20			ns
Data Hold Time (1)	Thold	25			ns
Clock (CLK) Rise Time (2)	CLKrt	70			ns
Clock (CLK) Fall Time (2)	CLKft	70			ns
End of Scan (SO) Rise Time (2)	SOrt			50	ns
End of Scan (SO) Fall Time (2)	SOft			50	ns
Global Start (GBST) Rise Time (3)	GBSTrt	70			ns
Global Start (GBST) Fall Time (3)	GBSTft	70			ns
Pixel Rise Time (4,5)	Prt			100	ns
Pixel Fall Time (4,5)	Pft			30	ns

Table 5. Timing Requirements

Notes:

1. The shift register will load on all falling CLK edges, so setup and hold times (Tset, Thold) are needed to prevent the loading of multiple start pulses. This would occur if the GBST remains high during two fallings edges of the CLK signal. See Figure 7 Timing Diagram.

2. SI starts the register scanning and the first active pixel is read out on the 56^{th} clock of the CLK signal. However, when multiple sensors are sequentially scanned, as in CIS modules, the SO from the predecessor sensor becomes the SI to the subsequent sensor, hence the SI clock = the SO clock.

3. As discussed under the third unique feature, the GBST starts the initialization process and preprocesses all sensors simultaneously in the first 55 clock cycles (110 pixels) before the first pixel is scanned onto the video line from the first sensor.

4. The transition between pixels does not always reach the dark offset level as shown in the timing diagrams, see Vout. The timing diagrams show the transition doing so for illustration purposes; however a stable pixel sampling point does exist for every pixel.

5. The pixel rise time is defined as the time from when the CLK’s rising edge has reached 50% of its maximum amplitude to the point when a pixel has reached 90% of its maximum amplitude. The pixel fall time is defined as the time from when a pixel’s charge begins to decrease from its maximum amplitude to within 10% of the lowest point before the next pixel begins to rise.

Figures 4 and 5 show the initialization of the first sensor in relation to its subsequent cascaded sensors. The Start Input Control (SIC) selects the first sensor to operate with 55 clock cycles of delay by connecting it to Vdd on the first sensor and to Ground for all of the subsequent sensors. Hence the first sensor will operate with 110 inactive pixels being clocked out before its first active pixel is clocked out.

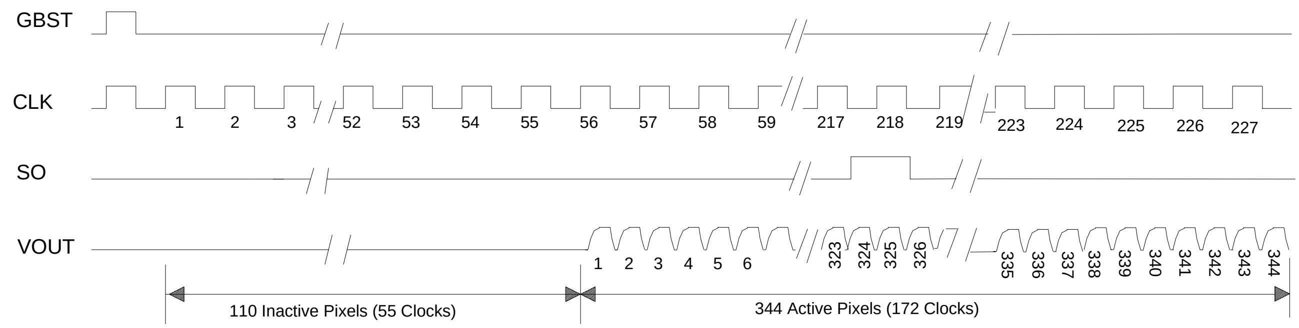


Figure 4. Overall Timing Diagram for the 600 dpi mode

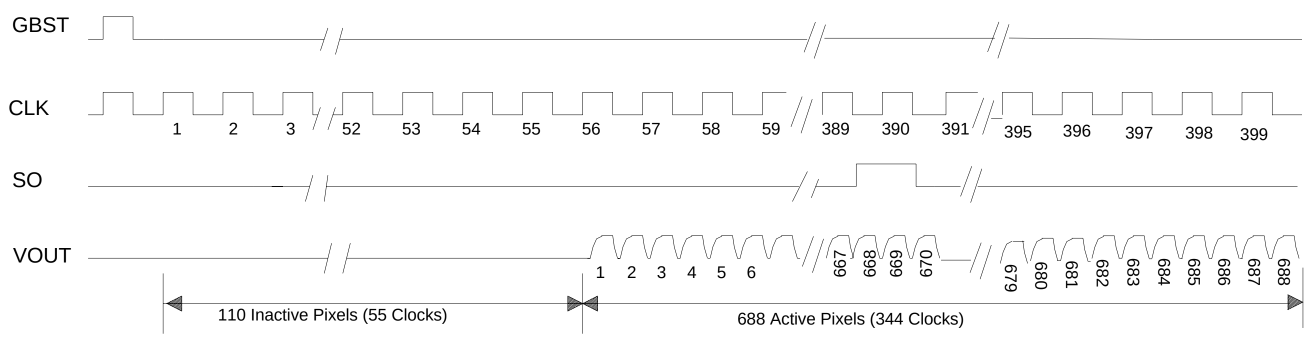


Figure 5. Overall Timing Diagram for the 1200 dpi mode

Figures 6 and 7 detail the timing of the CLK, GBST, Vout and SI/SO signals in further detail, which have the same timing requirements for both the 600 and 1200 dpi modes. The rise and fall times are listed in table 5 above. In Figure 7, note that pixel 111 is the first active pixel.

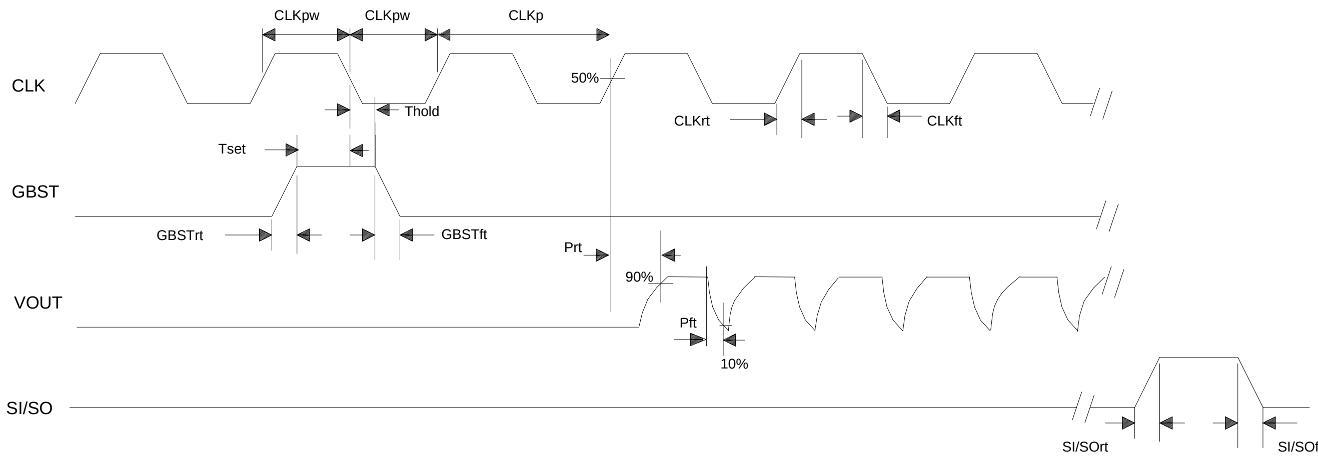


Figure 6. Rise and Fall Times for both the 600/1200 dpi modes

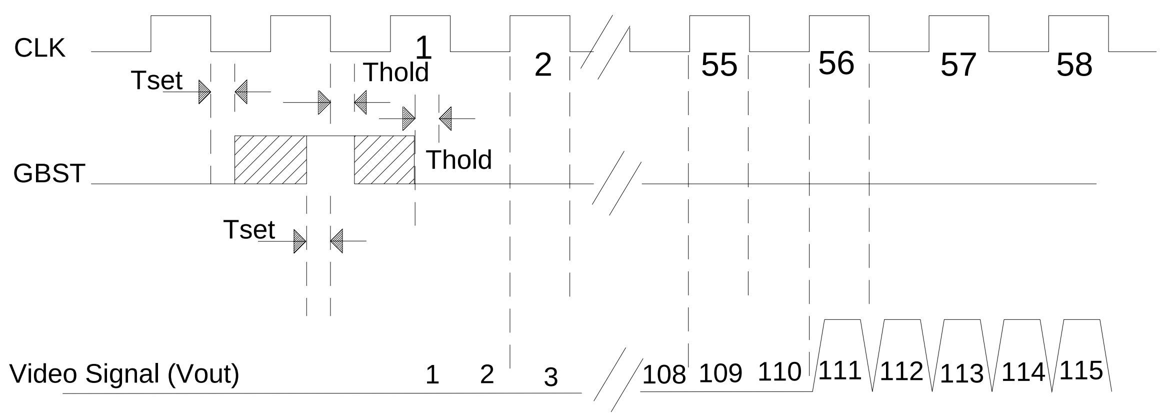


Figure 7. Timing of GBST-to-First Pixel of the First Sensor for both the 600/1200 dpi Modes.

Figures 8 and 9 show the timing of the End of Scan Pulse (SI/SO), which comes out in line with the 324th pixel for the 600 dpi mode and with the 668th pixel for the 1200 dpi mode. The SO from the first sensor enters as the SI clock of the second and subsequent sensors; hence all subsequent sensors will start their register scan after each of the preceding sensors completes its scan.

The last active pixel of each sensor is the 344th pixel for the 600 dpi mode and 688th pixel for the 1200 dpi mode.

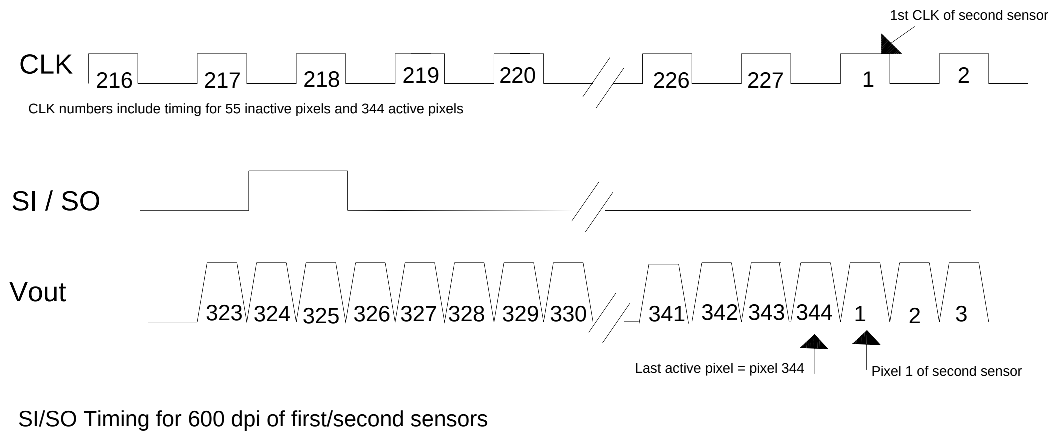


Figure 8. Timing of SI/SO Clock for the 600 dpi Mode.

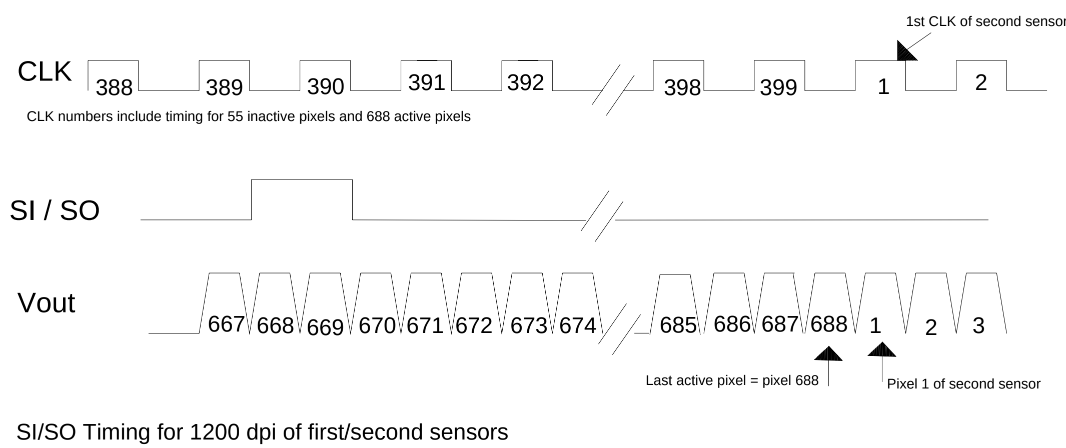


Figure 9. Timing of SI/SO Clock for the 1200 dpi Mode.

Example of a CIS Module using cascaded PI6050D Image Sensors

Figure 10 shows a typical schematic of a CIS module with 15 PI6050D image sensors serially cascaded together.

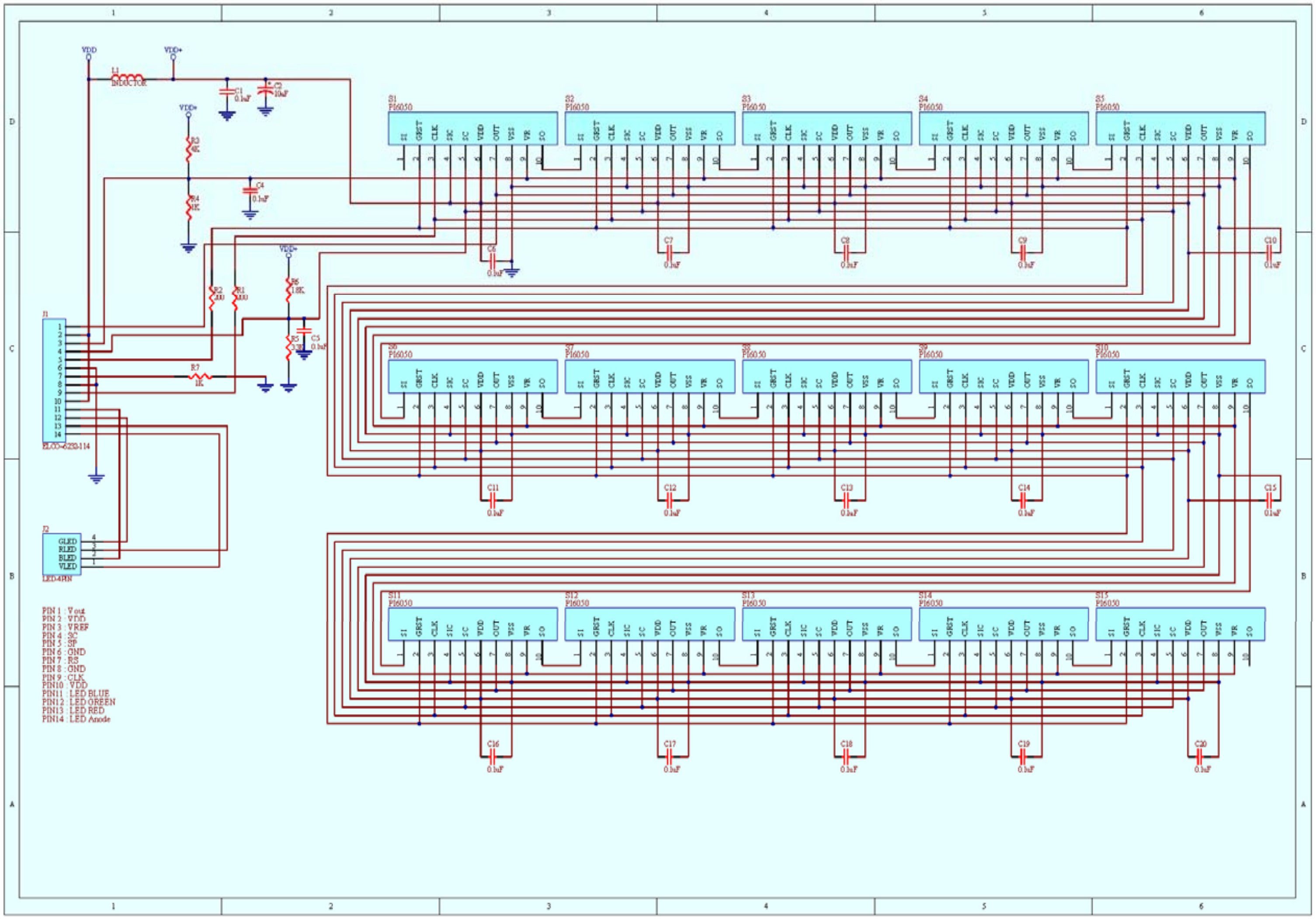


Figure 10. CIS Module with PI6050D Image Sensors