Dual LVTTL/LVCMOS to Differential HSTL Translator

FEATURES:

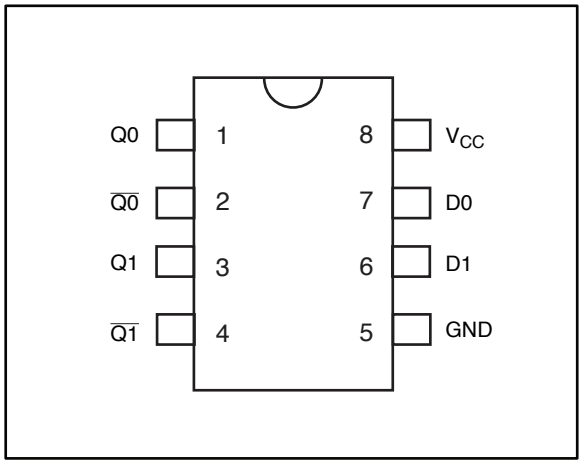
- Patented Technology
- HSTL differential outputs
- LVTTL/LVCMOS to Differential HSTL Translator
- Operating frequency up to 1.65GHz with 5pf load
- Operating frequency up to 500MHz with 15pf load
- Very low output pin to pin skew < 100ps
- Propagation delay < 1.4ns max with 15pf load
- 1.65V to 3.6V power supply
- Industrial temperature range: –40°C to 85°C
- Available in 8-pin SOIC package
- Available in 8-pin TSSOP package

DESCRIPTION:

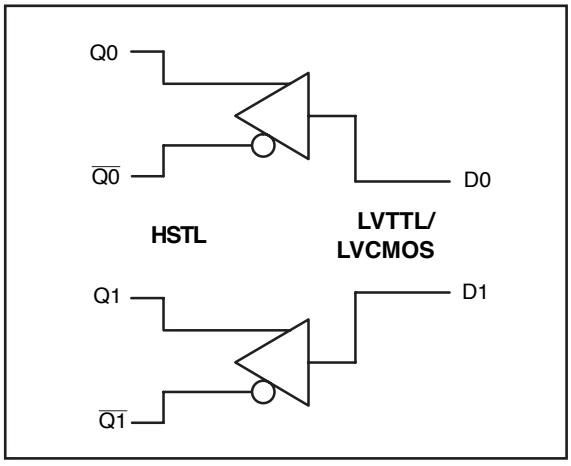
Potato Semiconductor's PO100HSTL22A is designed for world top performance using submicron CMOS technology to achieve 1.65GHz HSTL output frequency with less than 1.4ns propagation delay.

The PO100HSTL22A is a low-skew, LVTTL/LVCMOS to Differential HSTL Translator. The small outline 8 pin package and the low skew design to make it ideal for applications which require the translation of a clock or a data signal.

Pin Configuration



Logic Block Diagram



Pin Description

PIN	FUNCTION
Qn, $\overline{Qn}$	HSTL Differential Outputs
D0, D1	LVTTL/LVCMOS Inputs
V_{CC}	Positive Supply
GND	Ground

Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:
stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=V_{IH} or V_{IL}, I_{OH}= -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	Vcc=3V Vin=V_{IH} or V_{IL}, I_{OH}=12mA	-	0.3	0.5	V
V_{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	Vcc	V
V_{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I_{IH}	Input High current	Vcc = 3.6V and Vin = 5.5V	-	-	1	uA
I_{IL}	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-1	uA
V_{IK}	Clamp diode voltage	Vcc = Min. And I_{IN} = -18mA	-	-0.7	-1.2	V

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA

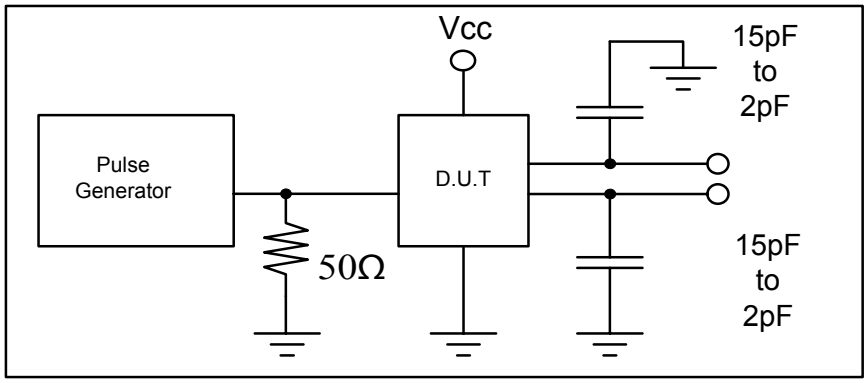
Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Switching Characteristics

Symbol	Description	Test Conditions (1)	Typ	Max	Unit
t_{PD}	Propagation Delay D to Output pair	CL = 15pF		1.4	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V		0.8	ns
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz		100	ps
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz		250	ps
tJITTER	Random Clock Jitter (RMS)	CL = 15pF, 125MHz	1.6		ps
fmax	Input Frequency	CL =15pF		500	MHz
fmax	Input Frequency	CL = 5pF		1.65	GHz

Notes:
1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

Test Circuit



Test Waveforms

FIGURE 1.
LVTTL/LVCMOS INPUT WAVEFORM DEFINITION

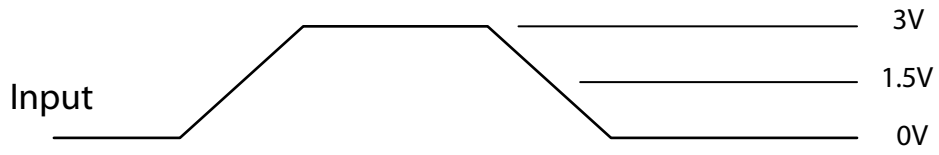


FIGURE 2.
HSTL OUTPUT

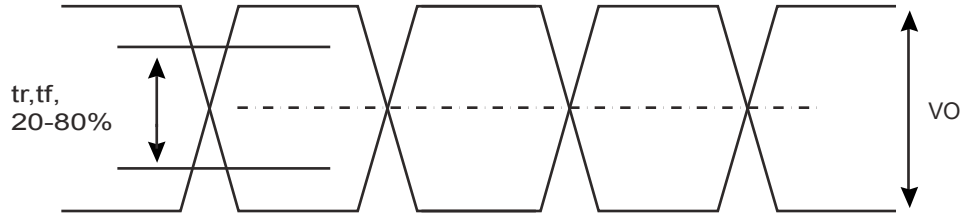
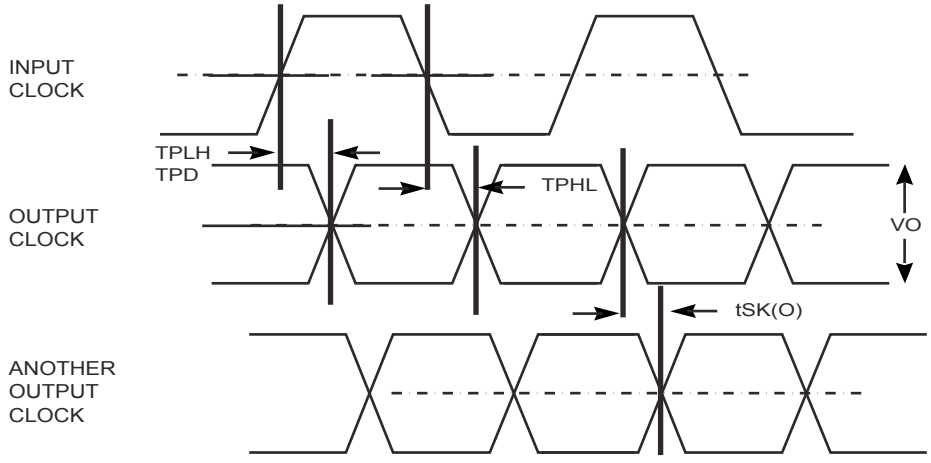
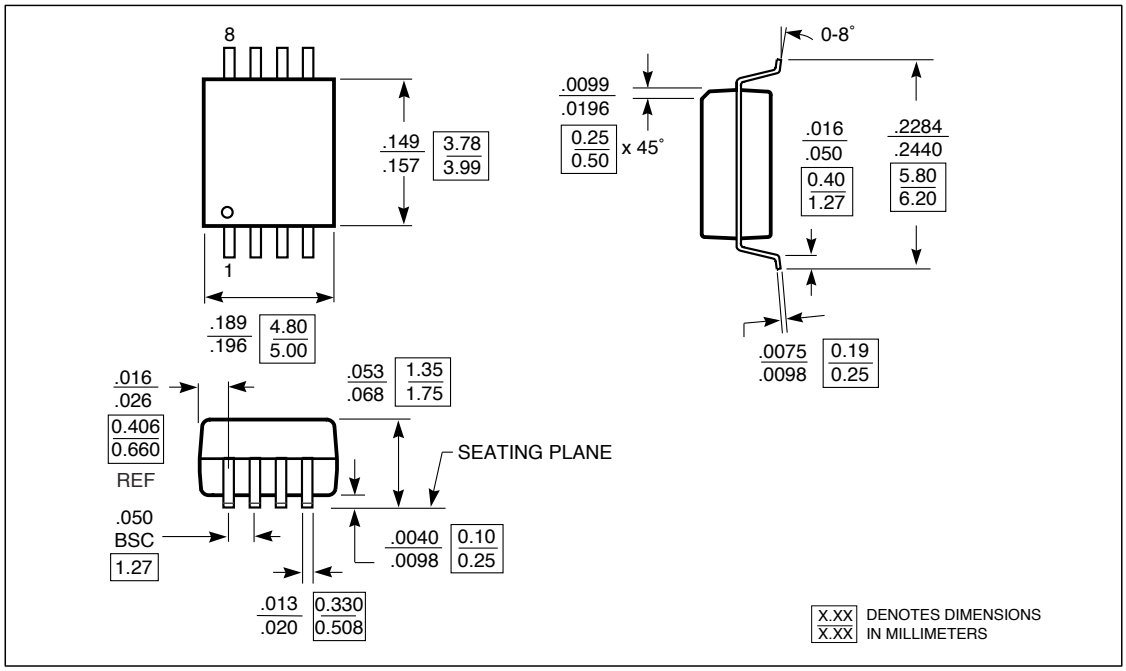


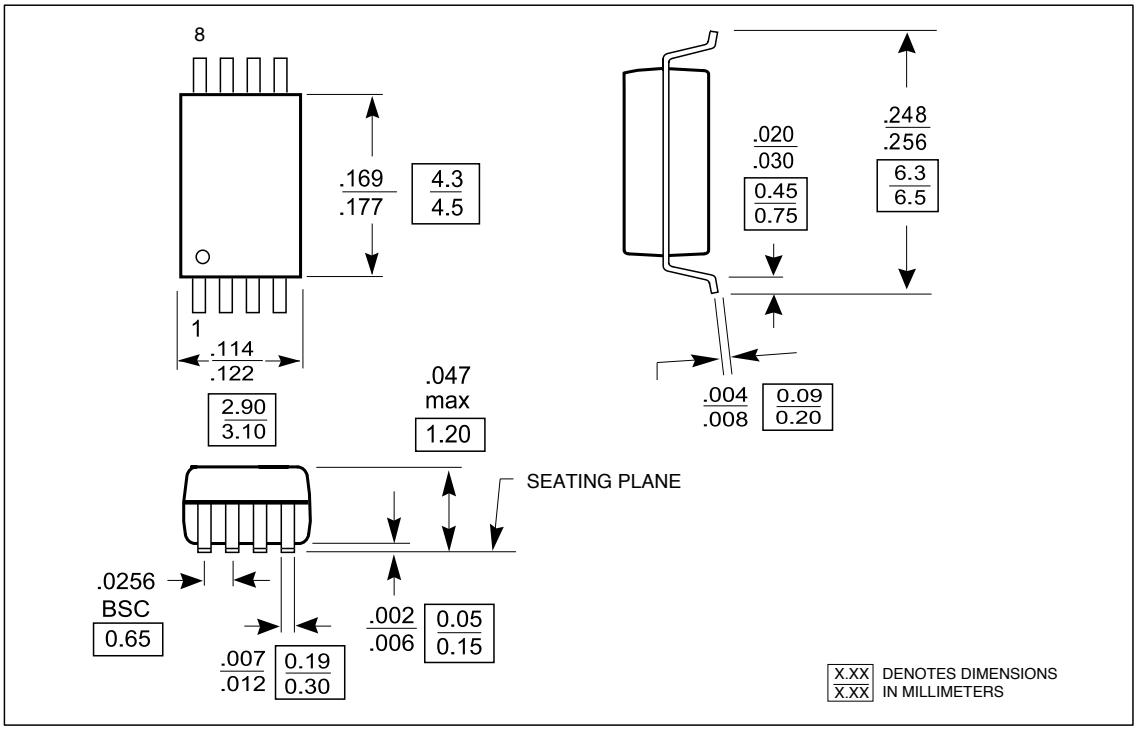
FIGURE 3.
Propogation Delay, Output pulse skew, and output-to-output skew for D to output pair



Packaging Mechanical Drawing: 8 pin SOIC



Packaging Mechanical Drawing: 8 pin TSSOP



Ordering Information

Ordering Code	Package			Top-Marking	T_A
PO100HSTL22ASU	8 pin SOIC	Tube	Pb-free & Green	PO100HSTL22AS	-40°C to 85°C
PO100HSTL22ASR	8 pin SOIC	Tape and reel	Pb-free & Green	PO100HSTL22AS	-40°C to 85°C
PO100HSTL22ATU	8 pin TSSOP	Tube	Pb-free & Green	PO100HSTL22TS	-40°C to 85°C
PO100HSTL22ATR	8 pin TSSOP	Tape and reel	Pb-free & Green	PO100HSTL22TS	-40°C to 85°C