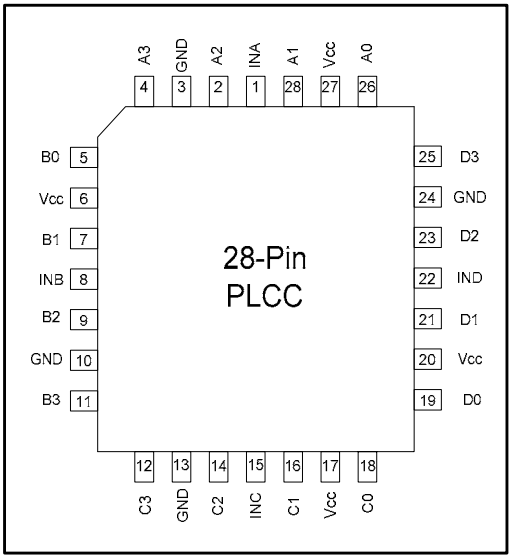
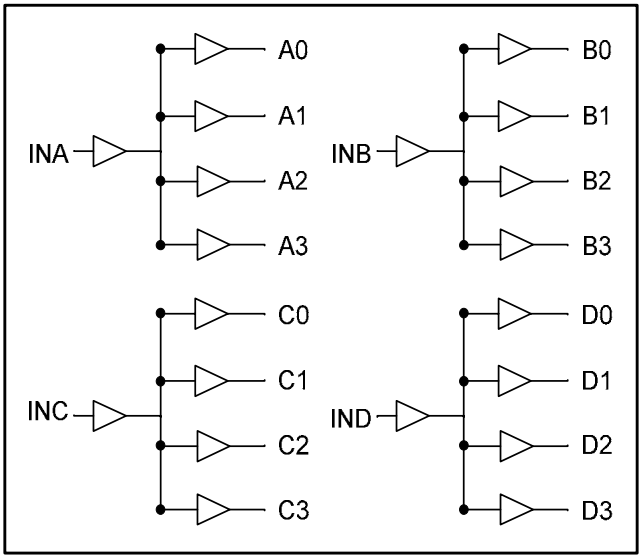
500MHz TTL/CMOS Potato Chip

FEATURES:	DESCRIPTION:
. Patented technology . Operating frequency up to 500MHz with 2pf load . Operating frequency up to 400MHz with 5pf load . Operating frequency up to 250MHz with 50pf load . Very low output pin to pin skew < 100ps . Very low pulse skew < 300ps . VCC = 1.65V to 3.6V . Propagation delay < 2.5ns max with 50pf load . Low input capacitance: 3pf typical . 4x1:4 fanout . Available in 28pin 50mil PLCC package	Potato Semiconductor's PO49FCT1816G is designed for world top performance using submicron CMOS technology to achieve 500MHz TTL output frequency with less than 100ps output pin to pin skew. PO49FCT1816G is a 1.65V to 3.3V CMOS 1 input to 4 outputs Buffered driver in 4 groups to achieve 500MHz output frequency. Typical applications are clock and signal distribution.

Pin Configuration



Logic Block Diagram



Pin Description

Pin Name	Description
INA, INB, INC, IND	Inputs
A[0-3], B[0-3], C[0-3], D[0-3]	Outputs

Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to Vcc+0.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:
stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -24mA	**2.46**		**-**	**V**
V_{OL}	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=24mA	**-**		**0.44**	**V**
V_{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	**2**	**-**	**Vcc**	**V**
V_{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	**-0.5**	**-**	**0.8**	**V**
I_{IH}	Input High current	Vcc = 3.6V and Vin = 3.6V	**-**	**-**	**1**	**uA**
I_{IL}	Input Low current	Vcc = 3.6V and Vin = 0V	**-**	**-**	**-1**	**uA**
V_{IK}	Clamp diode voltage	Vcc = Min. And IIN = -18mA	**-**	**-0.7**	**-1.2**	**V**

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

Capacitance

Parameters (1)	Description	Test Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0V	3	4	pF
Cout	Output Capacitance	Vout = 0V	-	6	pF

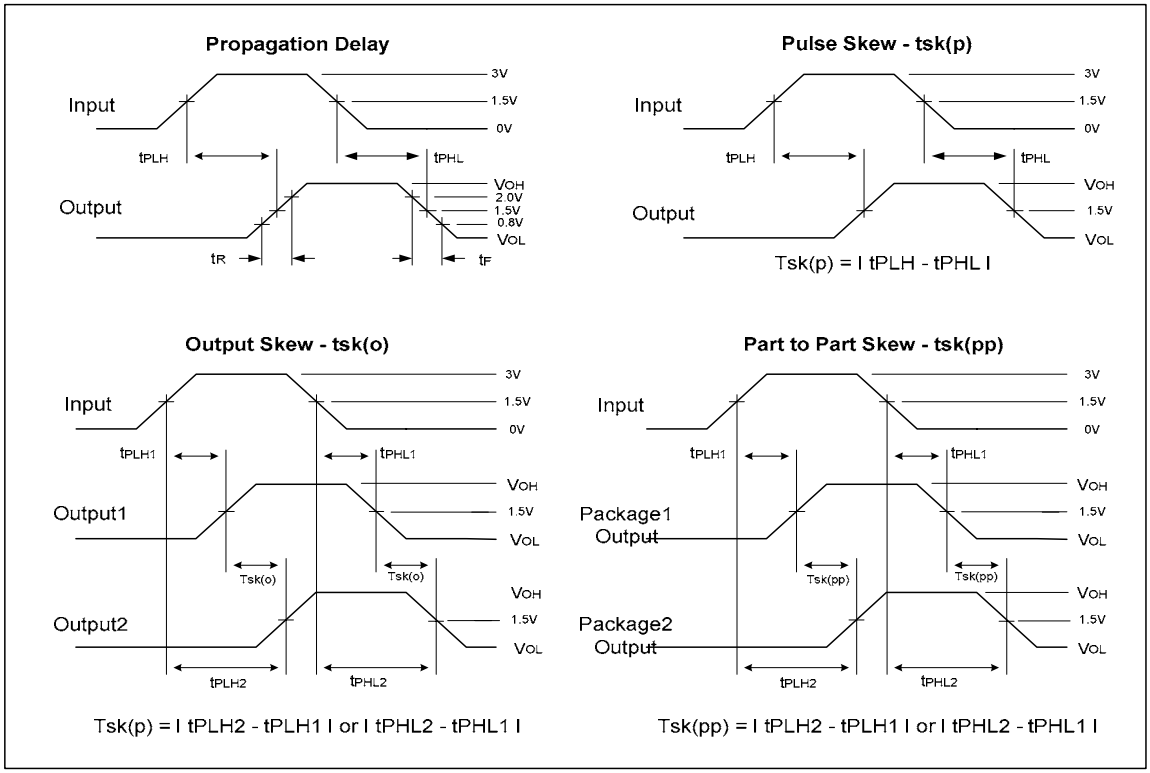
Notes:
1 This parameter is determined by device characterization but not production tested.

Switching Characteristics (Vcc = 3.3V±0.3V, T_A=85°C)

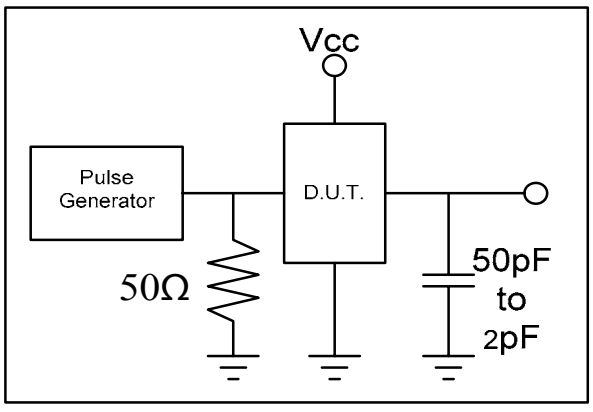
Symbol	Description	Test	Min	Max	Unit
t_{PLH}	Propagation Delay A to Bn	CL = 50pF		2.5	ns
t_{PHL}	Propagation Delay A to Bn	CL = 50pF		2.5	ns
tr/tf	Rise/Fall Time Measured between 0.8V – 2.0V	CL = 50pf		2.0	ns
tsk(p)	Pulse Skew (Same Package)	CL = 50pF		0.3	ns
tsk(o)	Output Pin to Pin Skew (Same Bank)	CL = 50pF		0.1	ns
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 50pF		0.15	ns
tsk(pp)	Output Skew (Different Package)	CL = 50pF		0.4	ns
t_{LOW}/t_{HIGH}	Pulse Width Duration	CL = 50pF	5		ns
t_{DC}	Duty Cycle	CL = 50pF	45	55	%
fmax	Input Frequency	CL = 50pF		250	MHz
fmax	Input Frequency	CL = 5pF		400	MHz
fmax	Input Frequency	CL = 2pF		500	MHz

Notes:
1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

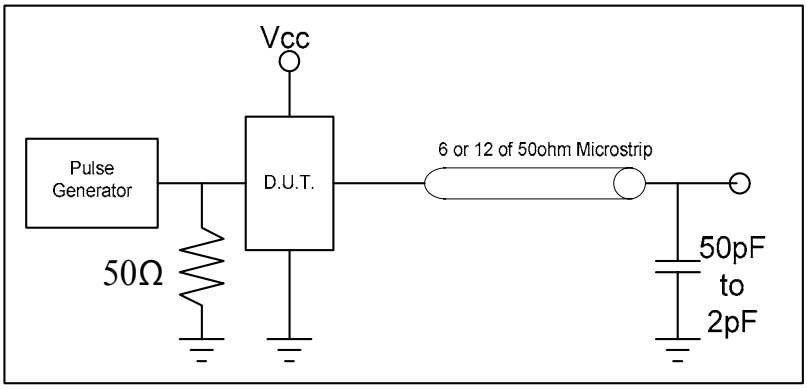
Test Waveforms



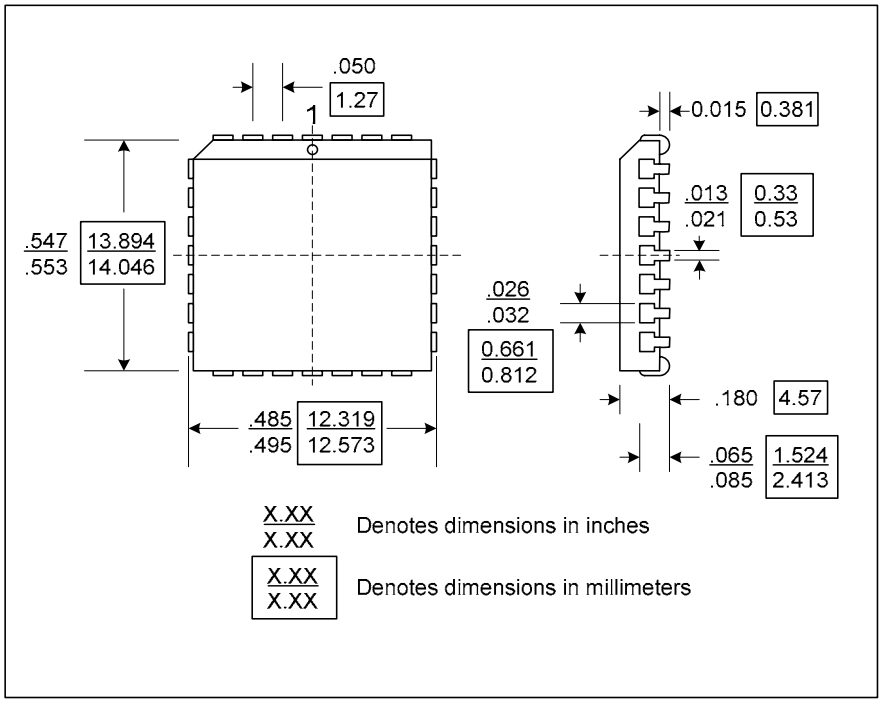
Test Circuit 1



Test Circuit 2



Packaging Mechanical Drawing: 28 pin PLCC



Ordering Information

Ordering Code	Package Code	Package Description
PO49FCT1816P	P	Pb-free & Green, 28-pin PLCC