

PS21869/-A

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21869



INTEGRATED POWER FUNCTIONS

600V/50A low-loss CSTBT inverter bridge for 3 phase
DC-to-AC power conversion

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

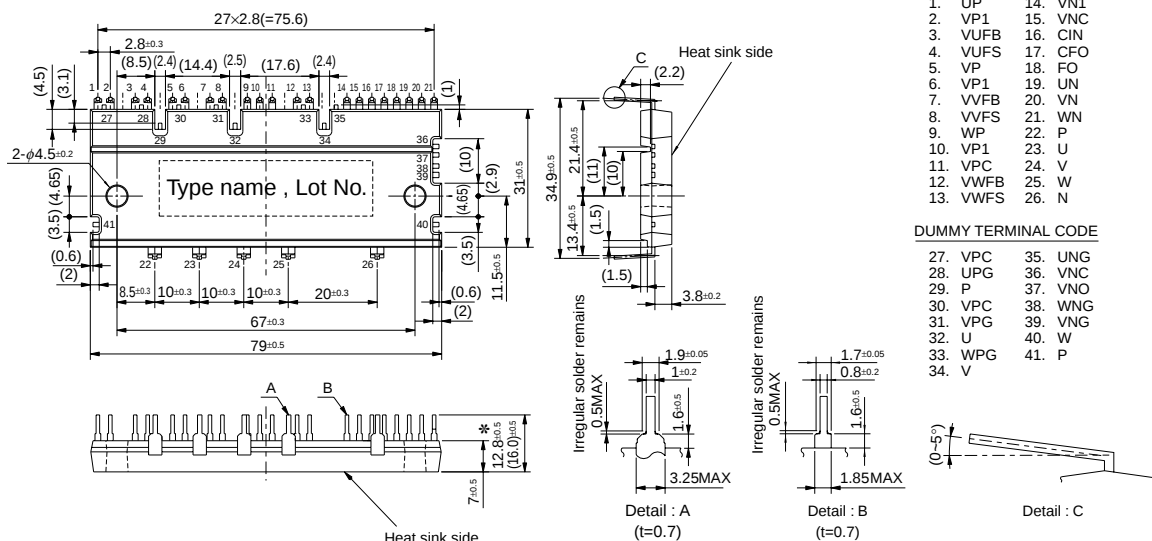
- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC). (Fig.3)
- Fault signaling : Corresponding to an SC fault (Lower-side IGBT) or a UV fault (Lower-side supply).
- Input interface : 5V line CMOS/TTL compatible. (High Active)
- UL Approved : Yellow Card No. E80276

APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES

Dimensions in mm



* -A : Long terminal type (16.0mm)

Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

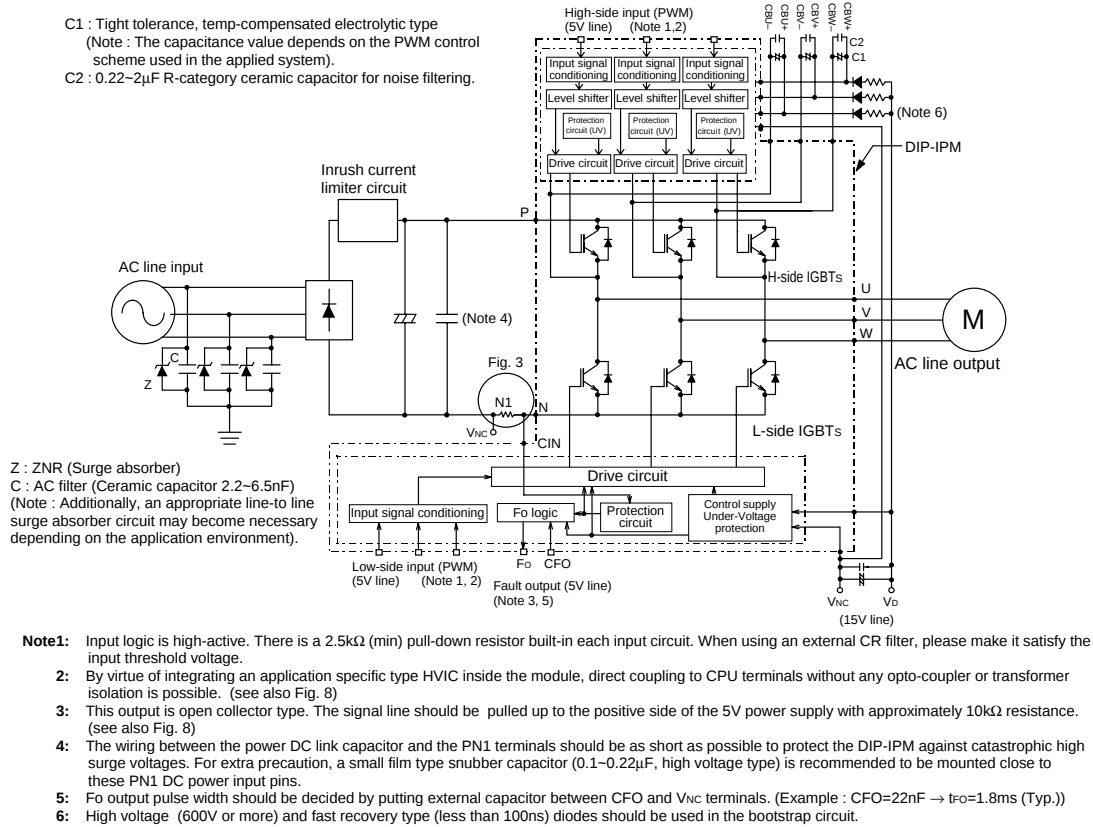
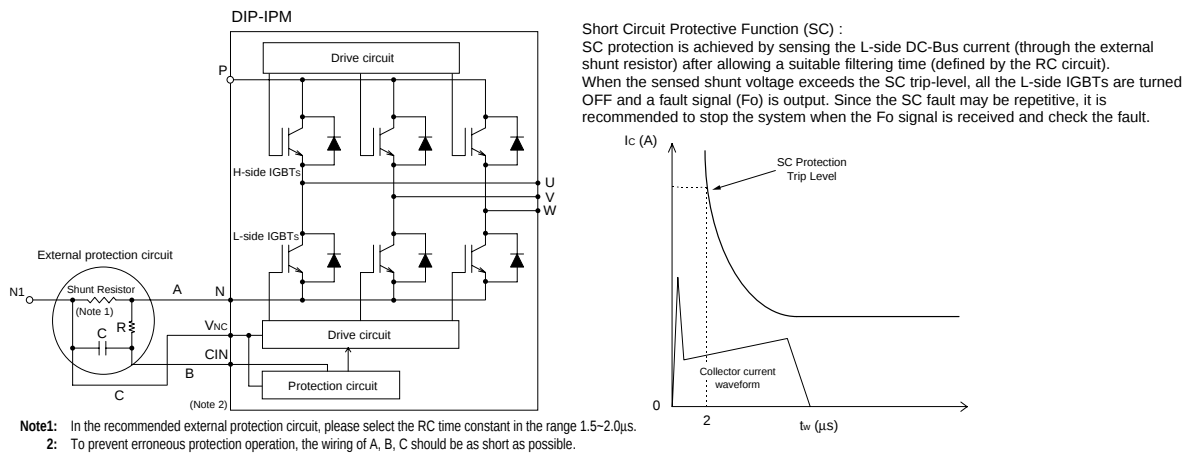


Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT



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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CC}	Supply voltage	Applied between P-N	450	V
V _{CC(surge)}	Supply voltage (surge)	Applied between P-N	500	V
V _{CES}	Collector-emitter voltage		600	V
±I _C	Each IGBT collector current	$T_f = 25^\circ\text{C}$	50	A
±I _{CP}	Each IGBT collector current (peak)	$T_f = 25^\circ\text{C}$, less than 1ms	100	A
P _C	Collector dissipation	$T_f = 25^\circ\text{C}$, per 1 chip	70.4	W
T _j	Junction temperature	(Note 1)	-20~+125	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ $T_f \leq 100^\circ\text{C}$) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(\text{ave})} \leq 125^\circ\text{C}$ (@ $T_f \leq 100^\circ\text{C}$).

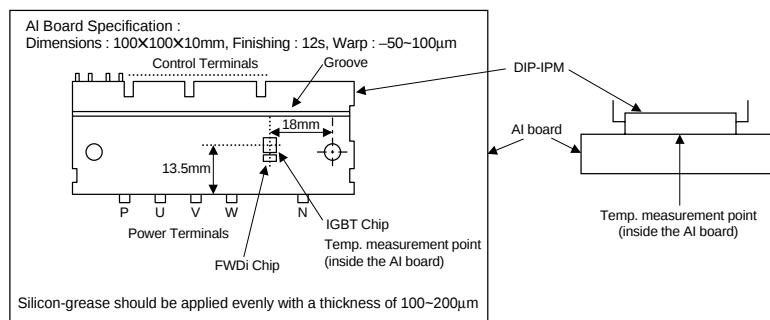
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Control supply voltage	Applied between VP1-VPC, VN1-VNC	20	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V _{IN}	Input voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC	-0.5~V _D +0.5	V
V _{FO}	Fault output supply voltage	Applied between Fo-VNC	-0.5~V _D +0.5	V
I _{FO}	Fault output current	Sink current at Fo terminal	1	mA
V _{SC}	Current sensing input voltage	Applied between CIN-VNC	-0.5~V _D +0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(Prot)}	Self protection supply voltage limit (short circuit protection capability)	V _D = 13.5~16.5V, Inverter part $T_j = 125^\circ\text{C}$, non-repetitive, less than 2 μs	400	V
T _f	Module case operation temperature	(Note 2)	-20~+100	°C
T _{stg}	Storage temperature		-40~+125	°C
V _{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	2500	V _{rms}

Note 2 : T_f MEASUREMENT POINT



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Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-f)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	1.42	°C/W
$R_{th(j-f)F}$		Inverter FWDi part (per 1/6 module)	—	—	2.00	°C/W

Note 3: Grease with good thermal conductivity should be applied evenly with about +100 μ m~+200 μ m on the contacting surface of DIP-IPM and heat-sink.

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB} = 15\text{V}$ $V_{IN} = 5\text{V}$	—	1.50	2.00	V
		$I_C = 50\text{A}$, $T_j = 25^\circ\text{C}$ $I_C = 50\text{A}$, $T_j = 125^\circ\text{C}$	—	1.60	2.10	
V_{EC}	FWDi forward voltage	$T_j = 25^\circ\text{C}$, $-I_C = 50\text{A}$, $V_{IN} = 0\text{V}$	—	1.70	2.20	V
t_{on}	Switching times	$V_{CC} = 300\text{V}$, $V_D = V_{DB} = 15\text{V}$ $I_C = 50\text{A}$, $T_j = 125^\circ\text{C}$, $V_{IN} = 0 \leftrightarrow 5\text{V}$ Inductive load (upper-lower arm)	0.70	1.30	1.90	μs
t_{rr}			—	0.30	—	μs
$t_{c(on)}$			—	0.40	0.60	μs
t_{off}			—	2.00	2.60	μs
$t_{c(off)}$			—	0.65	0.90	μs
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES}$	—	—	1	mA
		$T_j = 125^\circ\text{C}$	—	—	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
I_D	Circuit current	$V_D = V_{DB} = 15\text{V}$ $V_{IN} = 5\text{V}$	—	—	5.00	mA
		Total of V_{P1-VPC} , V_{N1-VNC} $V_{UFB-VUFS}$, $V_{VFB-VVFS}$, $V_{WFB-VWFS}$	—	—	0.40	
		$V_D = V_{DB} = 15\text{V}$ $V_{IN} = 0\text{V}$	—	—	7.00	mA
		Total of V_{P1-VPC} , V_{N1-VNC} $V_{UFB-VUFS}$, $V_{VFB-VVFS}$, $V_{WFB-VWFS}$	—	—	0.55	
V_{FOH}	Fault output voltage	$V_{SC} = 0\text{V}$, F_o circuit pull-up to 5V with 10k Ω	4.9	—	—	V
V_{FOL}		$V_{SC} = 1\text{V}$, $I_{FO} = 1\text{mA}$	—	—	0.95	V
$V_{SC(ref)}$	Short circuit trip level	$T_j = 25^\circ\text{C}$, $V_D = 15\text{V}$ (Note 4)	0.43	0.48	0.53	V
I_{IN}	Input current	$V_{IN} = 5\text{V}$	1.0	1.5	2.0	mA
UV_{DBt}	Supply circuit under-voltage protection	$T_j \leq 125^\circ\text{C}$	10.0	—	12.0	
UV_{DBr}			10.5	—	12.5	
UV_{Dt}			10.3	—	12.5	
UV_{Dr}			10.8	—	13.0	
t_{FO}	Fault output pulse width	$C_{FO} = 22\text{nF}$ (Note 5)	1.0	1.8	—	ms
$V_{th(on)}$	ON threshold voltage	Applied between U_P , V_P , W_P-V_{PC} , U_N , V_N , W_N-V_{NC}	2.1	2.3	2.6	V
$V_{th(off)}$	OFF threshold voltage		0.8	1.4	2.1	V

Note 4: Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 85 A.

5: Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : $C_{FO} = 12.2 \times 10^{-6} \times t_{FO}$ [F].

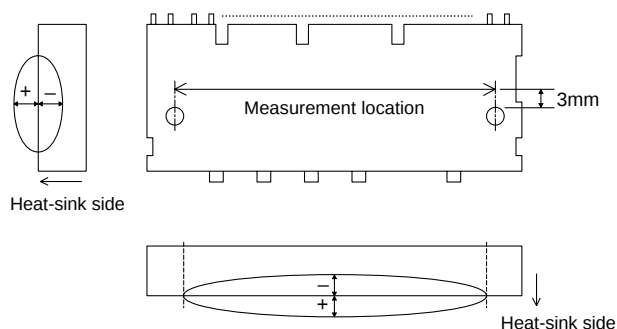
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MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4	Recommended 1.18 N·m	0.98	—	1.47	N·m
Weight			—	65	—	g
Heat-sink flatness	(Note 6)		-50	—	100	μm

Note 6: Measurement point of heat-sink flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage	Applied between P-N	0	300	400	V
V _D	Control supply voltage	Applied between V _{P1} -V _{PC} , V _{N1} -V _{NC}	13.5	15.0	16.5	V
V _{DB}	Control supply voltage	Applied between V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}	13.0	15.0	18.5	V
ΔV _D , ΔV _{DB}	Control supply variation		-1	—	1	V/μs
t _{dead}	Arm shoot-through blocking time	For each input signal, T _f ≤ 100°C	2	—	—	μs
f _{PWM}	PWM input frequency	T _f ≤ 100°C, T _j ≤ 125°C	—	5	—	kHz
I _O	Allowable r.m.s. current	V _{CC} = 300V, V _D = 15V, f _c = 5kHz P.F = 0.8, sinusoidal T _j ≤ 125°C, T _f ≤ 100°C (Note 7)	—	—	23	Arms
P _{WIN}	Minimum input pulse width	ON (Note 8)	300	—	—	ns
V _{NC}	V _{NC} variation	between V _{NC} -N (including surge)	-5.0	—	5.0	V

Note 7 : The allowable r.m.s. current value depends on the actual application conditions.

8 : The input pulse width less than P_{WIN} might make no response.

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Fig. 4 THE DIP-IPM INTERNAL CIRCUIT

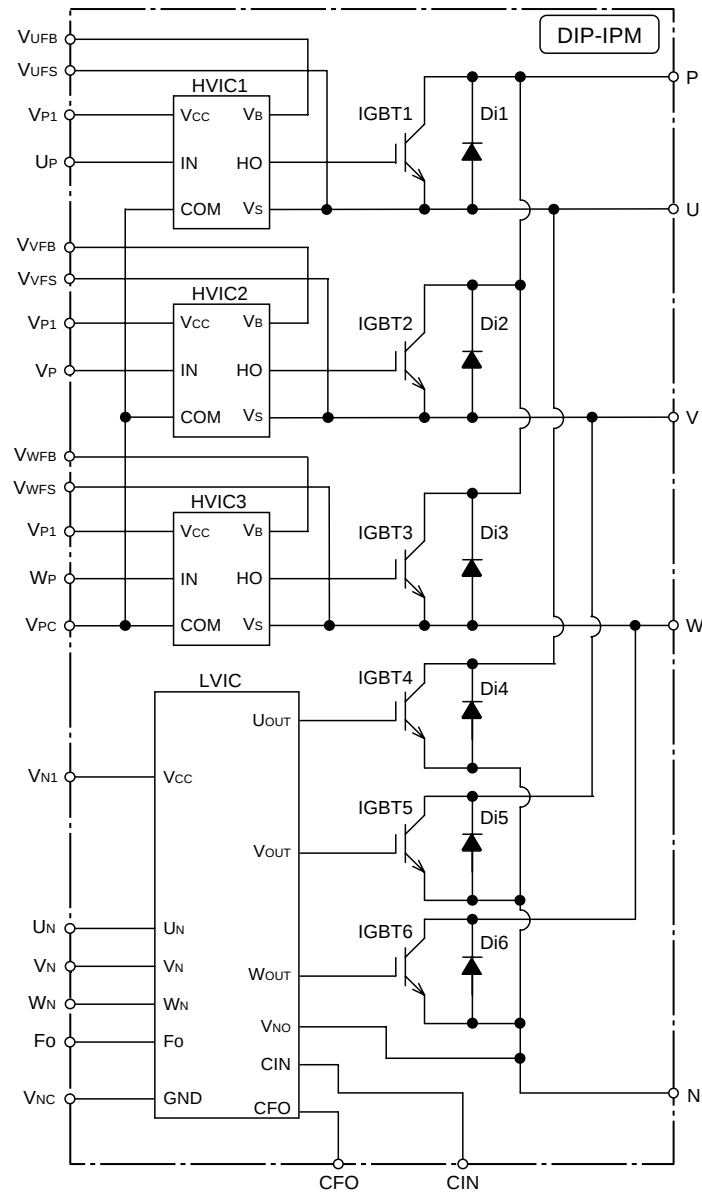
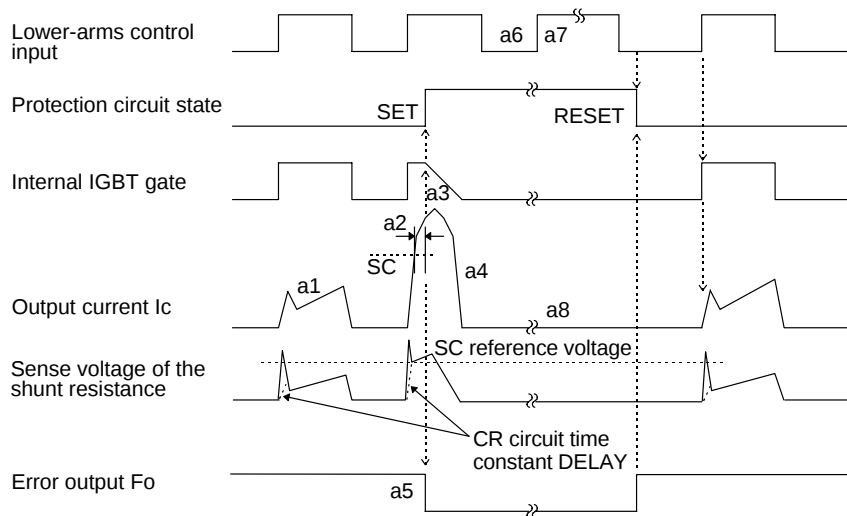


Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS**[A] Short-Circuit Protection (Lower-arms only)**

(With the external shunt resistance and CR connection)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
- a3. Hard IGBT gate interrupt.
- a4. IGBT turns OFF.
- a5. Fo timer operation starts : The pulse width of the Fo signal is set by the external capacitor C_{Fo}.
- a6. Input "L" : IGBT OFF state.
- a7. Input "H" : IGBT ON state, but during the Fo active signal period the IGBT doesn't turn ON.
- a8. IGBT OFF state.

**[B] Under-Voltage Protection (Lower-arm, UVd)**

- b1. Control supply voltage rises : After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied.
- b2. Normal operation : IGBT ON and carrying current.
- b3. Under voltage trip (UV_{Dt}).
- b4. IGBT OFF in spite of control input condition.
- b5. Fo operation starts.
- b6. Under voltage reset (UV_{Dr}).
- b7. Normal operation : IGBT ON and carrying current.

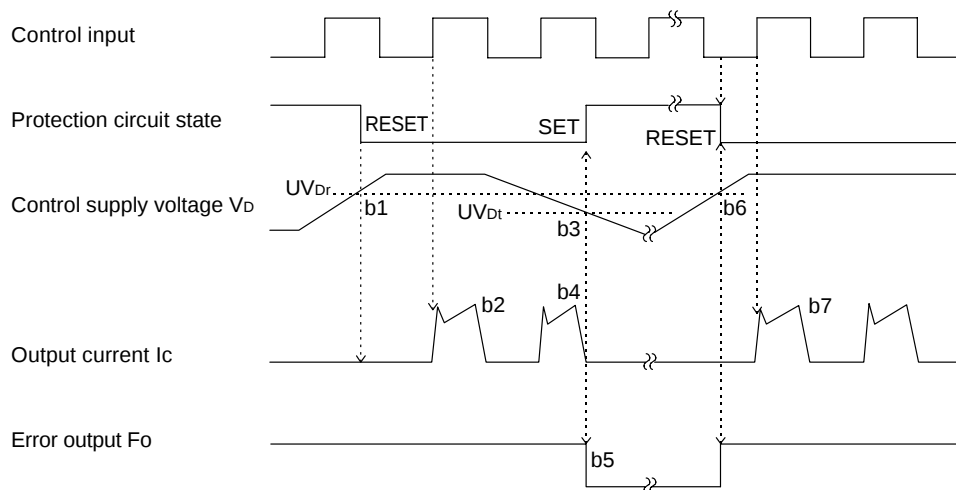
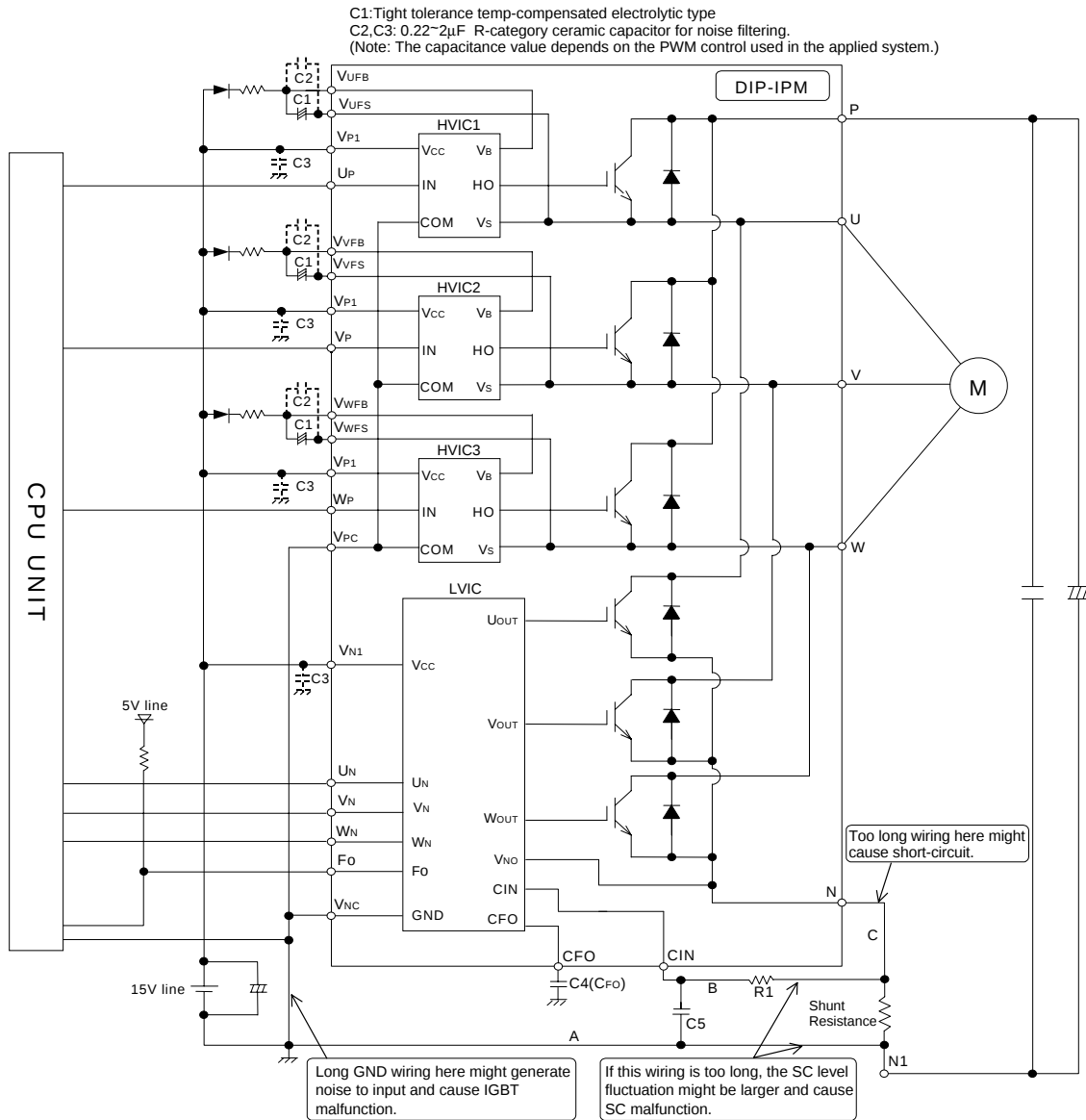


Fig. 8 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE



Note 1: To prevent the input signals oscillation, the wiring of each input should be as short as possible. (2cm~3cm or less)

2: By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

3: Fo output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 10kΩ resistor.

4: Fo output pulse width is determined by the external capacitor between CFO and VNC terminals (CFO). (Example : CFO = 22 nF → tFO = 1.8 ms (typ.))

5: The logic of input signal is high-active. The DIP-IPM input signal section integrates a 2.5kΩ (min) pull-down resistor. Therefore, when using external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.

6: To prevent malfunction of protection, The wiring of A, B, C should be as short as possible.

7: Please set the R1C5 time constant in the range 1.5~2μs.

8: Each capacitor should be located as nearby the pins of the DIP-IPM as possible.

9: To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 pins should be as short as possible. Approximately a 0.1~0.22μF snubber capacitor between the P&N1 pins is recommended.