

Features

- Low On-resistance: 60Ω typ, with ±5V Supplies, Minimizes Distortion
- On-Resistance Matching between channels better than 6Ω
- Guaranteed Low Leakage Currents: <0.1nA at +25°C
- Rail-to-Rail Analog Signal Range
- Low Distortion: <0.04% (600Ω)
- Low Crosstalk: -90dB @100kHz
- TTL/CMOS Compatible (with +5V or ±5V Supplies)
- Low Power Consumption.
- 16-pin Narrow SOIC and QSOP Packages save board area
- Pin-compatible upgrades for 74HC4051/4052/4053

Applications

- Audio and Video Switching and Routing
- Lab and Medical Instrumentation
- Low-Voltage Data-Acquisition and Process Control Systems
- Battery-Powered Communication Systems

Description

The PS4051/PS4052/PS4053 are precision low-voltage CMOS analog multiplexers/switches.

The PS4051 is an eight-channel single-ended mux designed to select one of eight inputs to a common output. What input is selected depends on the status of three address bits (ADDA-ADDC). The PS4052 is a differential four-channel mux, controlled by two address bits: ADDA, and ADDB. The PS4053 is a triple 2-to-1 mux (or triple SPDT, single-pole double-throw, switch).

The INH (inhibit) pin can be driven high, to open all switches regardless of address bit status. All control inputs are TTL compatible when V+ = +5V.

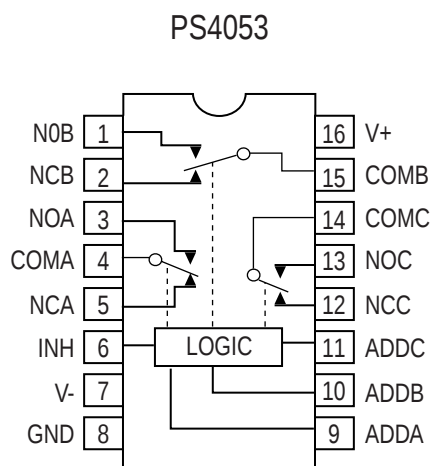
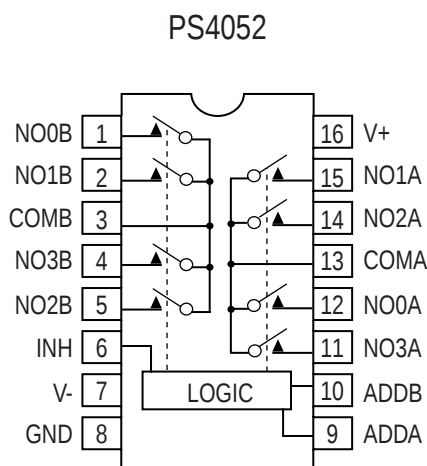
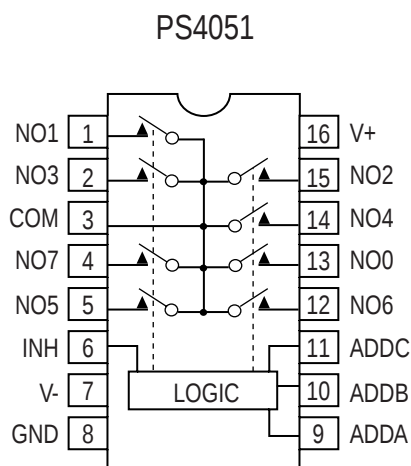
These devices are designed to operate with power supplies from ±2.7V to ±8V. Single-supply operation is possible from +2.7V to +16V.

When on, each switch conducts current equally well in either direction and can handle rail-to-rail analog signals. In the off-state each switch blocks voltages up to the power-supply rails. Off-leakage current is guaranteed to be less than 0.1nA at +25°C, and < 2.5nA at +85°C.

These devices are available in 16-pin DIP, Narrow SOIC, and QSOP packages for operation over the -40°C to +85°C temperature range.

Functional Block Diagrams and Pin Configurations

Top Views



Truth Tables

PS4051				
INH	ADDC	ADDB	ADDA	On Switch
1	X	X	X	None
0	0	0	0	NO0
0	0	0	1	NO1
0	0	1	0	NO2
0	0	1	1	NO3
0	1	0	0	NO4
0	1	0	1	NO5
0	1	1	0	NO6
0	1	1	1	NO7

PS4053						
INH	ADDC	ADDB	ADDA	On Switches		
1	X	X	X	None		
0	0	0	0	NOC	NOB	NOA
0	0	0	1	NOC	NOB	NCA
0	0	1	0	NOC	NCB	NOA
0	0	1	1	NOC	NCB	NCA
0	1	0	0	NCC	NOB	NOA
0	1	0	1	NCC	NOB	NCA
0	1	1	0	NCC	NCB	NOA
0	1	1	1	NCC	NCB	NCA

PS4052			
INH	ADDB	ADDA	On Switch
1	X	X	None
0	0	0	NO0A,B
0	0	1	NO1A,B
0	1	0	NO2A,B
0	1	1	NO3A,B

Logic “0”, $V_{AL} \leq 0.8V$
 Logic “1”, $V_{IH} \geq 2.4V$

Absolute Maximum Ratings

Voltages Referenced to V–

V+	–0.3V to + 17V
GND	–0.3V to + 17V
GND	–0.3V to (V+) + 0.3V
$V_{IN}, V_{COM}, V_{NO}^{(1)}$	(V–) –2V to (V+) + 2V or 30mA, whichever occurs first
Current (any terminal)	30mA
Peak Current, COM, NO, NC	
(pulsed at 1ms, 10% duty cycle)	100mA
ESD per method 3015.7	>2000V

Thermal Information

Continuous Power Dissipation

Plastic DIP (derate 10.5mW/°C above +70°C)	800mW
Narrow SO and QSOP	
(derate 8.7mW/°C above +70°C)	650mW
Storage Temperature	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1:

Signals on NO, COM, or logic inputs exceeding V+ or V– are clamped by internal diodes. Limit forward diode current to 30mA.

Caution: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Specifications - Dual Supplies

($V_{\pm} = \pm 5V \pm 10\%$, $GND = 0V$, $V_{AH} = V_{IH} = 2.4V$, $V_{AL} = V_{IL} = 0.8V$)

Parameter	Symbol	Conditions		Temp.(°C)	Min ⁽²⁾	Typ ⁽¹⁾	Max ⁽²⁾	Units
Analog Switch								
Analog Signal Range ⁽³⁾	V _{ANALOG}			Full	V _−		V ₊	V
On Resistance	R _{ON}	V ₊ = 5V, V _− = −5V, V _{COM} = ±3V, I _{NO} = 1mA		25		60	100	Ω
				Full			125	
On-Resistance Match Between Channels ⁽⁴⁾	ΔR _{ON}	V _{COM} or V _{NC} = ±3V, I _{NO} = 1mA, V ₊ = 5V, V _− = −5V		25			12	
				Full			18	
On-Resistance Flatness ⁽⁵⁾	R _{FLAT} (ON)	V ₊ = 5V, V _− = −5V, I _{NO} = 1mA, V _{COM} = ±3V, 0V		25			10	
				Full			15	
NO Off Leakage Current ⁽⁶⁾	I _{NO} (OFF)	V ₊ = 5.5V, V _− = −5.5V, V _{COM} = ±4.5V, V _{NO} = ∓4.5V		25	−0.1		50	nA
				Full	−1.0		100	
COM-Off Leakage Current ⁽⁶⁾	I _{COM} (OFF)	V ₊ = 5.5V, V _− = −5.5V, V _{COM} = ± 4.5V, V _{NO} = ∓4.5V	PS4051	25	−0.1		50	
				Full	−2.5		100	
			PS4052 PS4053	25	−0.1		50	
				Full	−1.5		100	
COM On Leakage Current ⁽⁷⁾	I _{COM} (ON)	V _{COM} = ∓4.5V	PS4051	25	−0.1		50	
				Full	−5		100	
			PS4052 PS4053	25	−0.1		50	
				Full	−2.5		100	
Logic Input								
Logic High Input Voltage	V _{AH} , V _{IH}			Full	2.4			V
Logic Low Input Voltage	V _{AL} , V _{IL}						0.8	
Input Current with Input Voltage High or Low	I _{IH} , I _{IL}	V _A = V _I = V ₊ , 0V				−0.1		0.1

Electrical Specifications - Dual Supplies (continued)

($V_{\pm} = \pm 5V \pm 10\%$, GND = 0V, $V_{AH} = V_{IH} = 2.4V$, $V_{AL} = V_{IL} = 0.8V$)

Parameter	Symbol	Conditions		Temp (°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
Dynamic								
Transition Time	t _{TRANS}	Figure 1		25		75	250	ns
Break-Before-Make TimeDelay	t _{OPEN}	Figure 3			2	10		
Turn-OnTime	t _{ON}	Figure 2				50	175	
Turn-Off Time	t _{OFF}	Figure 2		Full			225	
				25		40	150	
				Full			200	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _S = 0V, R _S = 0Ω,		25		2	10	pC
Off Isolation ⁽⁷⁾	OIRR	C _L = 15pF, V _{INH} = 5V, R _L = 50Ω, f = 100kHz,V _{NO} = 1V _{RMS}				−90		dB
Crosstalk	X _{TALK}	C _L = 15pF, R _L = 50Ω, f = 100kHz, Figure 6, V _{NO} = 1V _{RMS}				−92		
Logic Input Capacitance	C _{IN}	f=1MHz				8		pF
NO Off Capacitance	C _{NO (OFF)}	f=1MHz, V _{NO} = 0V				2		
COM Off Capacitance	C _{COM (OFF)}	f=1MHz, V _{COM} =0V	PS4051			2		
			PS4052 PS4053			2		
COM On Capacitance	C _{COM (ON)}	f=1MHz, V _{COM} = 0V	PS4051			8		
			PS4052 PS4053		8			
Supply								
Power-Supply Range				Full	±2.7		±8	V
Positive Supply Current	I+	V _{INH} = V _A = 0V or V+, V+ =5.5V, V− = −5.5V					10	μA
Negative Supply Current	I−				−10			

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON \max} - R_{ON \min}$
5. Flatness is defined as the difference between the maximum and minimum values of on-resistance measured over the specific analog signal range, i.e., $V_{NO} = 3V$ to 0 and 0V to $-3V$.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at $+25^\circ C$.
7. Off Isolation = $20 \log_{10} V_{COM} / V_{NO}$. See Figure 5.

Electrical Characteristics - Single 5V Supply

(V+ = +5V ±10%, V- = 0V, GND = 0V, V_{AH} = V_{IH} = 2.4V, V_{AL} = V_{IL} = 0.8V)

Parameter	Symbol	Conditions		Temp (°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
Switch								
Analog Signal Range ⁽³⁾	V _{ANALOG}			Full	0		V+	V
On Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = 3.5V, V+ = 4.5V		25		125	225	Ω
				Full			280	
NO-Off Leakage Current ⁽⁸⁾	I _{NO (OFF)}	V _{NO} = 0V, V _{COM} = 4.5V, V+ = 5.5V		25	−0.1		50	nA
				Full	−10		100	
COM-Off Leakage Current ⁽⁸⁾	I _{COM (OFF)}	V+ = 5.5V, V _{COM} = 4.5V, V _{NO} =0V, or V _{COM} = 0V, V _{NO} = 4.5V	PS4051	25	−1		50	
				Full	−10		100	
			PS4052 PS4053	25	−1		50	
				Full	−5		100	
COM-On Leakage Current ⁽⁸⁾	I _{COM (ON)}	V _{COM} = V _{NO} = 4.5V, V+ = 5.5V	PS4051	25	−1		50	
				Full	−10		100	
			PS4052 PS4053	25	−1		50	
				Full	−10		100	
Digital Logic Input								
Logic High Input Voltage	V _{AH} , V _{IH}			Full	2.4			V
Logic Low Input Voltage	V _{AL} , V _{IL}						0.8	
Input Current with Input Voltage High or Low	I _{IH} , I _{IL}	V _A = V _I = V +, 0V				−1		1
Supply								
Positive-Supply Current	I+	V _A = V _I = 0V or V+		25	−1.0		1.0	μA
				Full			10	

Electrical Characteristics - Single 5V(continued)

(V+ = +5V ±10%, V- = 0V, GND = 0V, V_{AH} = V_{IH} = 2.4V, V_{AL} = V_{IL} = 0.8V)

Parameter	Symbol	Conditions	Temp (°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
Dynamic							
Turn-OnTime	t _{ON}		25		90	200	ns
			Full			275	
Turn-Off Time	t _{OFF}		25		60	125	
			Full			175	
Break-Before-Make Interval	t _{OPEN}		25		30		pC
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _S = 0V, R _S = 0Ω			1.5	5	

Electrical Characteristics - Single 3V Supply

(V+ = +3.3V ±10%, V- = 0V, GND = 0V, V_{AH} = V_{IH} = +2.4V, V_{AL} = V_{IL} = +0.8V)

Parameter	Symbol	Conditions	Temp (°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}		Full	0		V+	V
On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = 1.5V, V+ = 3V	25		250	525	Ω
			Full			700	
Dynamic							
Transition Time ⁽³⁾	t _{TRANS}	Figure 1, V _{IN} = 2.4V V _{NO1} = 1.5V, V _{NO8} = 0V	25		230	575	ns
Turn-OnTime ⁽³⁾	t _{ON}	Figure 2, V _{INH} = 2.4V V _{INL} = 0V, V _{NO1} = 1.5V			200	500	
Turn-Off Time ⁽³⁾	t _{OFF}	Figure 2, V _{INH} = 2.4V V _{INL} = 0V, V _{NO1} = 1.5V			75	400	
Charge Injection ⁽³⁾	Q	C _L = 10nF, V _S = 0V, R _S = 0Ω			1	5	pC

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON \text{ max}} - R_{ON \text{ min}}$
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
7. Worst-case isolation is on channel 4 because of its proximity to the COM pin. Off isolation = $20\log V_{COM}/V_{NO}$, V_{COM} = output, V_{NO} = input to off switch
8. Leakage testing at single supply is guaranteed by testing with dual supplies.

Test Circuits/Timing Diagrams

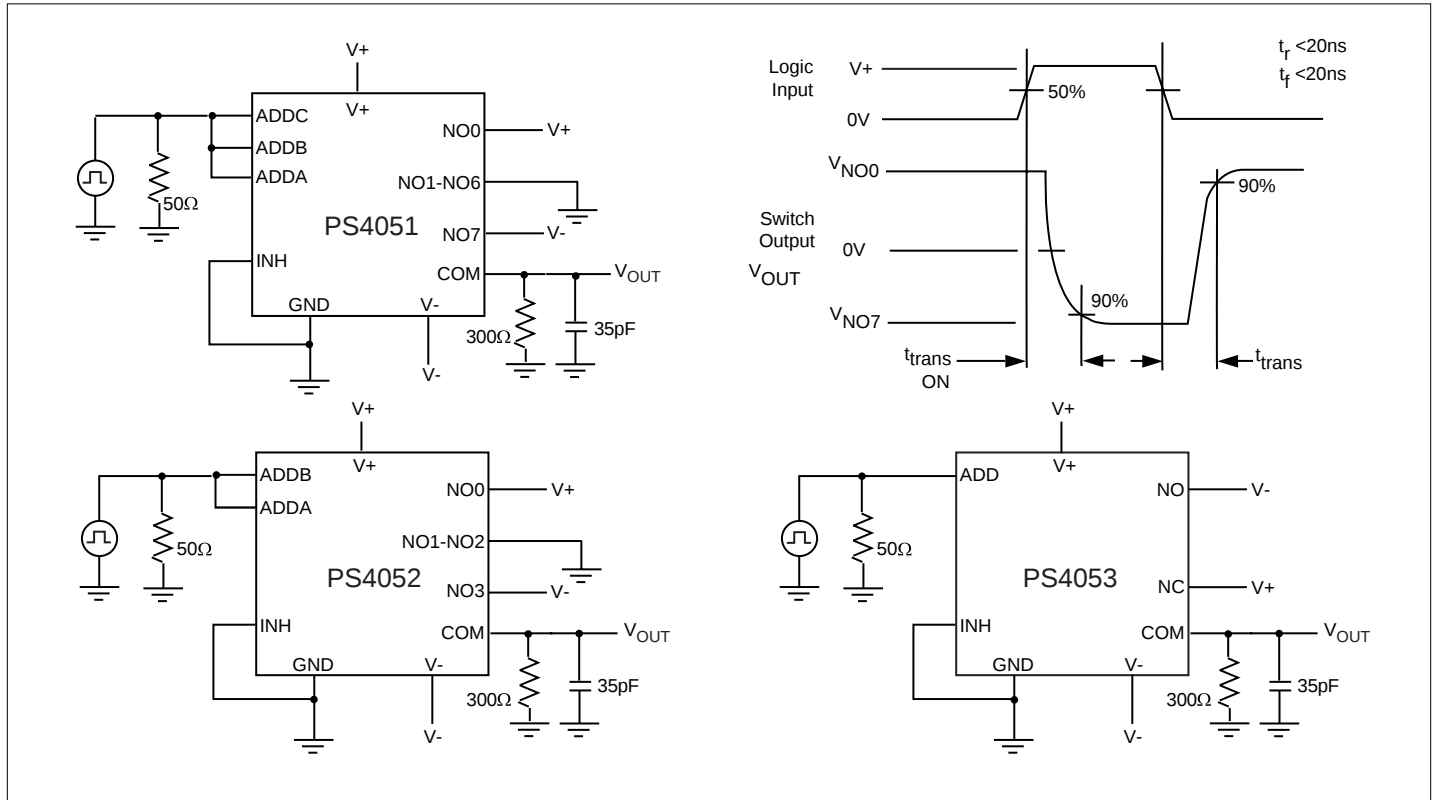


Figure 1. Transition Time

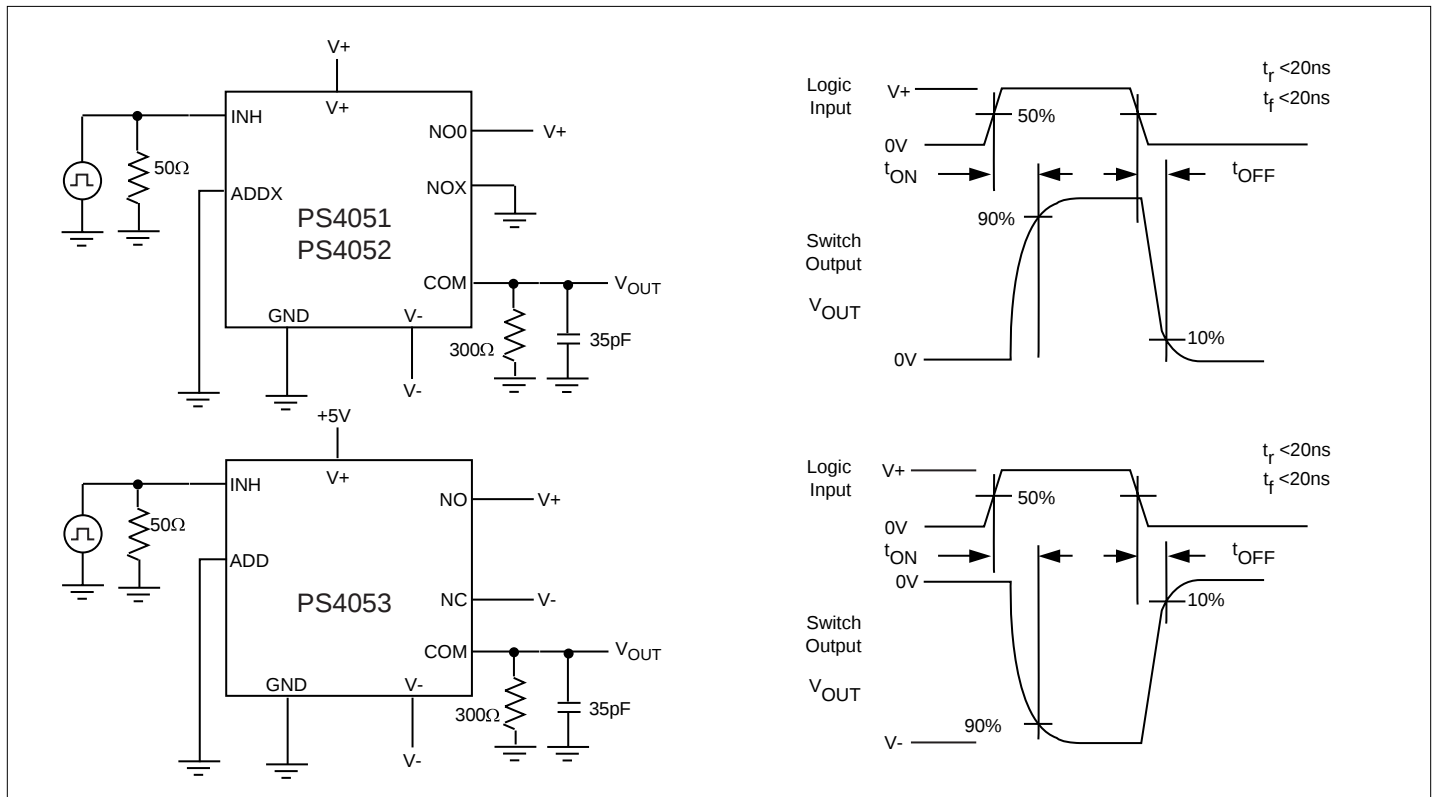


Figure 2. Switching Times

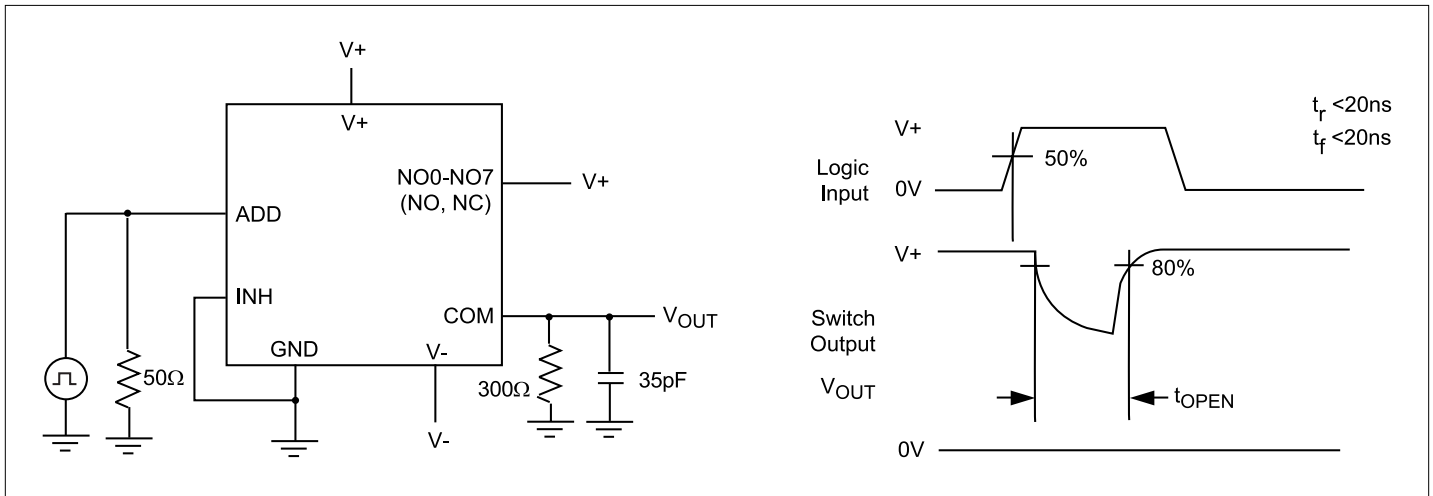


Figure 3. Break-Before-Make Interval

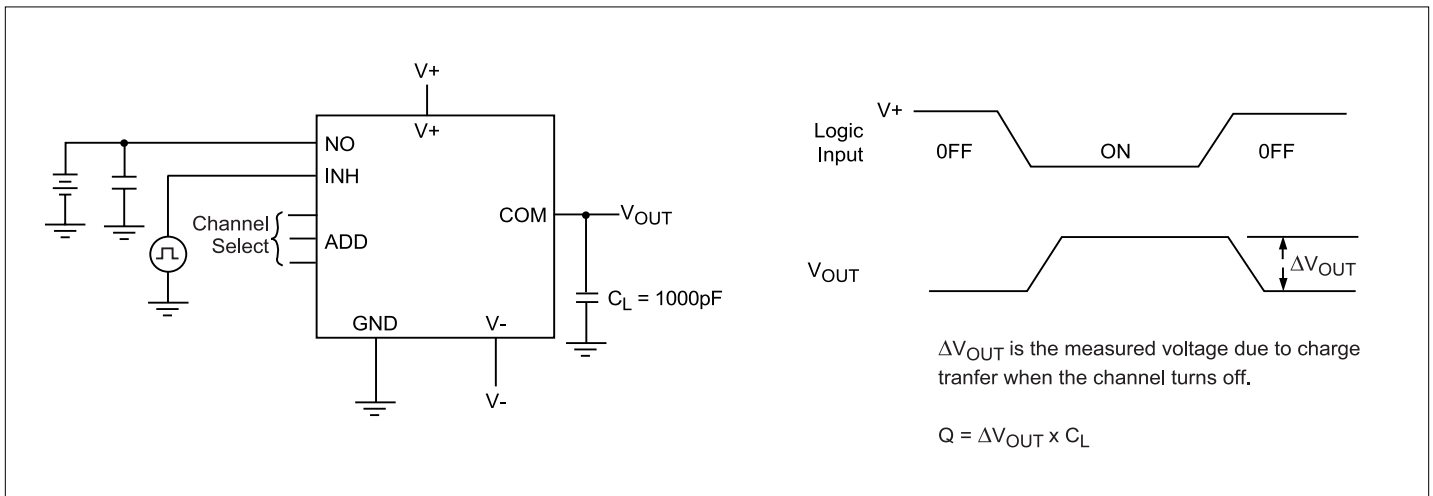


Figure 4. Charge Injection

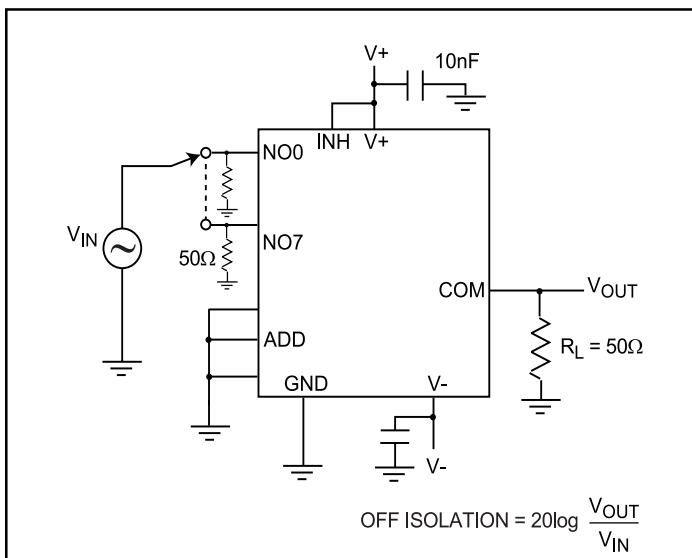


Figure 5. Off Isolation

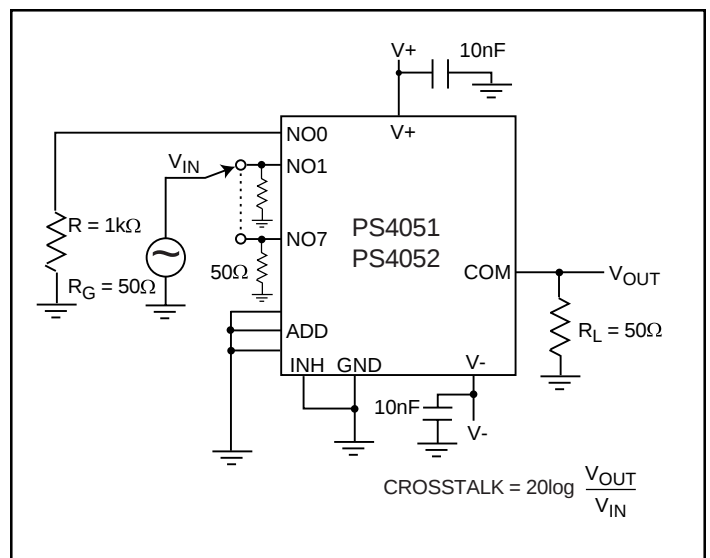


Figure 6. Crosstalk

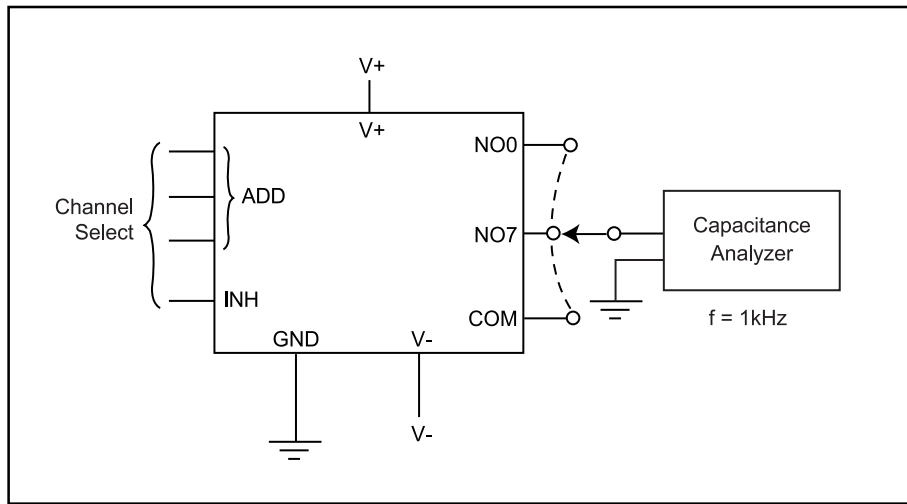


Figure 8. NO/COM Capacitance

Ordering Information

Part Number	Temperature	Package
PS4051CPE	0°C to +70°C	PDIP-16
PS4051CSE	0°C to +70°C	Narrow SOIC-16
PS4051CEE	0°C to +70°C	QSOP-16
PS4051EPE	-40°C to +85°C	PDIP-16
PS4051ESE	-40°C to +85°C	Narrow SOIC-16
PS4051EEE	-40°C to +85°C	QSOP-16
PS4052CPE	0°C to +70°C	PDIP-16
PS4052CSE	0°C to +70°C	Narrow SOIC-16
PS4052CEE	0°C to +70°C	QSOP-16

Part Number	Temperature	Package
PS4052EPE	-40°C to +85°C	PDIP-16
PS4052ESE	-40°C to +85°C	Narrow SOIC-16
PS4052EEE	-40°C to +85°C	QSOP-16
PS4053CPE	0°C to +70°C	PDIP-16
PS4053CSE	0°C to +70°C	Narrow SOIC-16
PS4053CEE	0°C to +70°C	QSOP-16
PS4053EPE	-40°C to +85°C	PDIP-16
PS4053ESE	-40°C to +85°C	Narrow SOIC-16
PS4053EEE	-40°C to +85°C	QSOP-16