DESCRIPTION

PT6355 is a Vacuum Fluorescent Display Controller driven 5/16, 6/16, 14/16 and 15/16 duty factors. Eight to Eighteen Segment Output Lines, Seven to Ten Grid Output Lines, Ten Segment/Grid Output Drive Lines, 8-bit x 6-channel A-D Converter, Built-in Noise Filter are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro-computer. PT6355 also provides 4 serial interfaces via the CS, SIN, SOUT, SCLK Pins. Housed in 44-pin, LQFP Package, PT6355's pin assignment and application circuit are optimized for easy PCB layout and cost saving benefits.

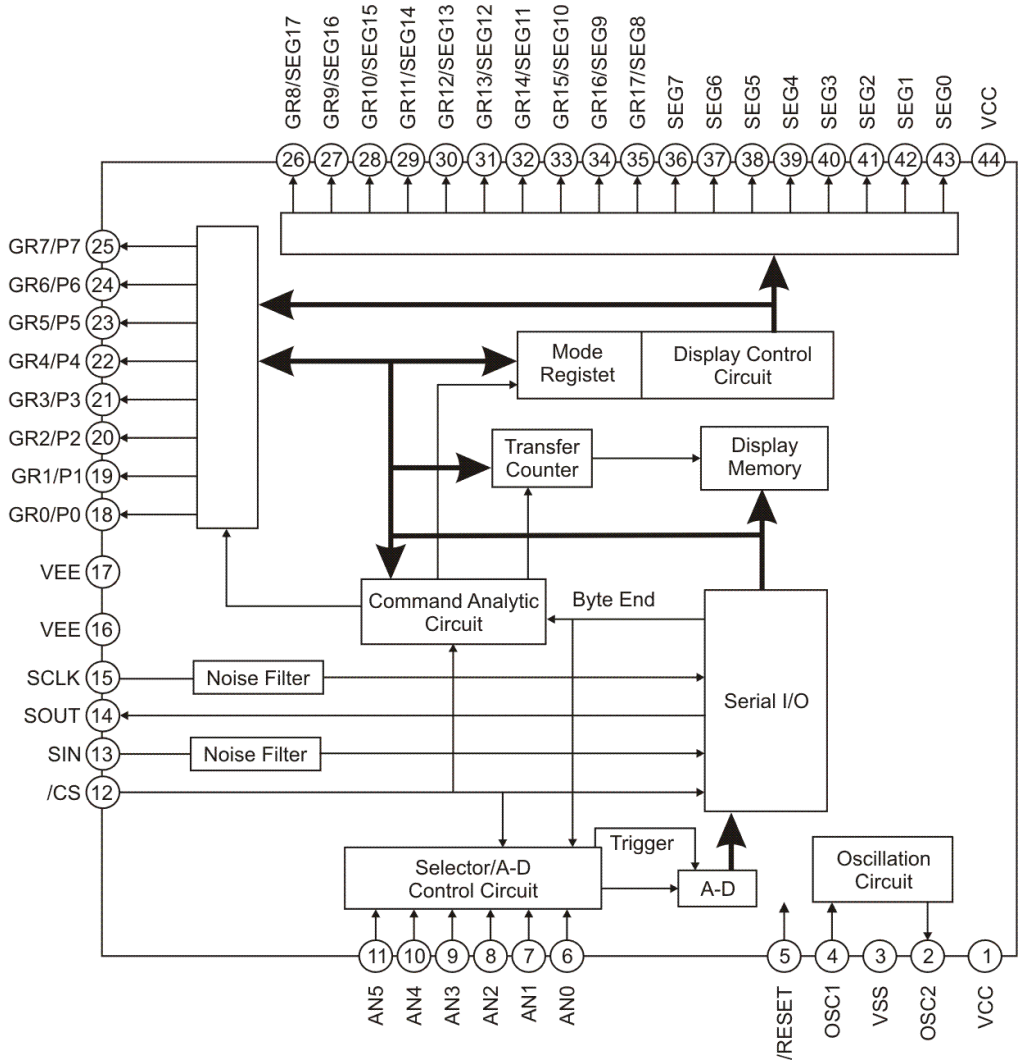
FEATURES

- CMOS Technology
- Internal Pull-Low Resistor
- 4-Step Dimming Circuitry
- 8 to 18 Segment Outputs
- 7 to 10 Grid Outputs
- Built-in Noise Filter in Serial Clock and Serial Input Pins with 2 MHz sampling
- 8-bit x 6 channels Analog-to-Digital Converter with +3LSB Accuracy
- Available in 44-pin, LQFP Package

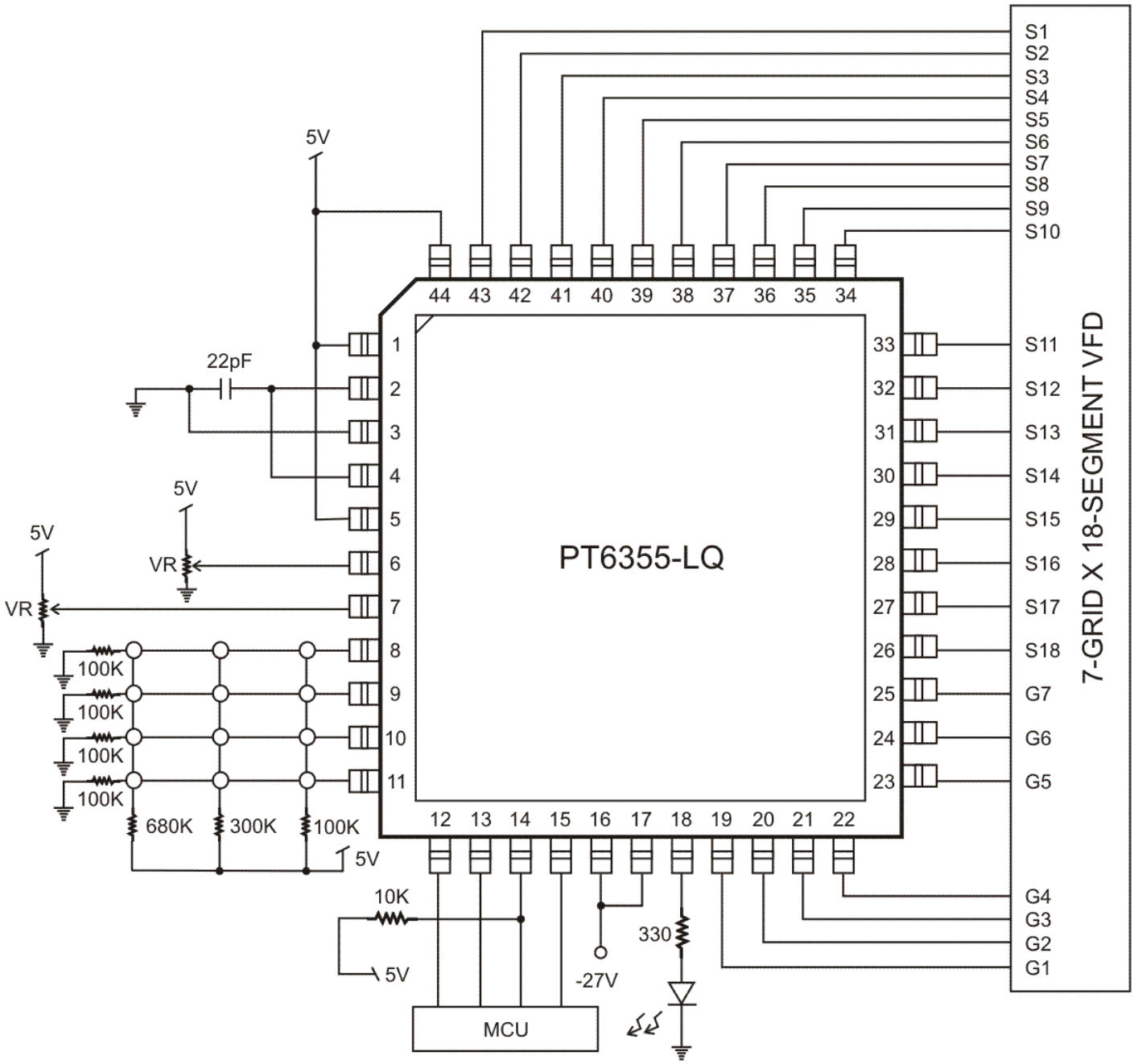
APPLICATION

- Micro-Computer Peripheral Device

BLOCK DIAGRAM



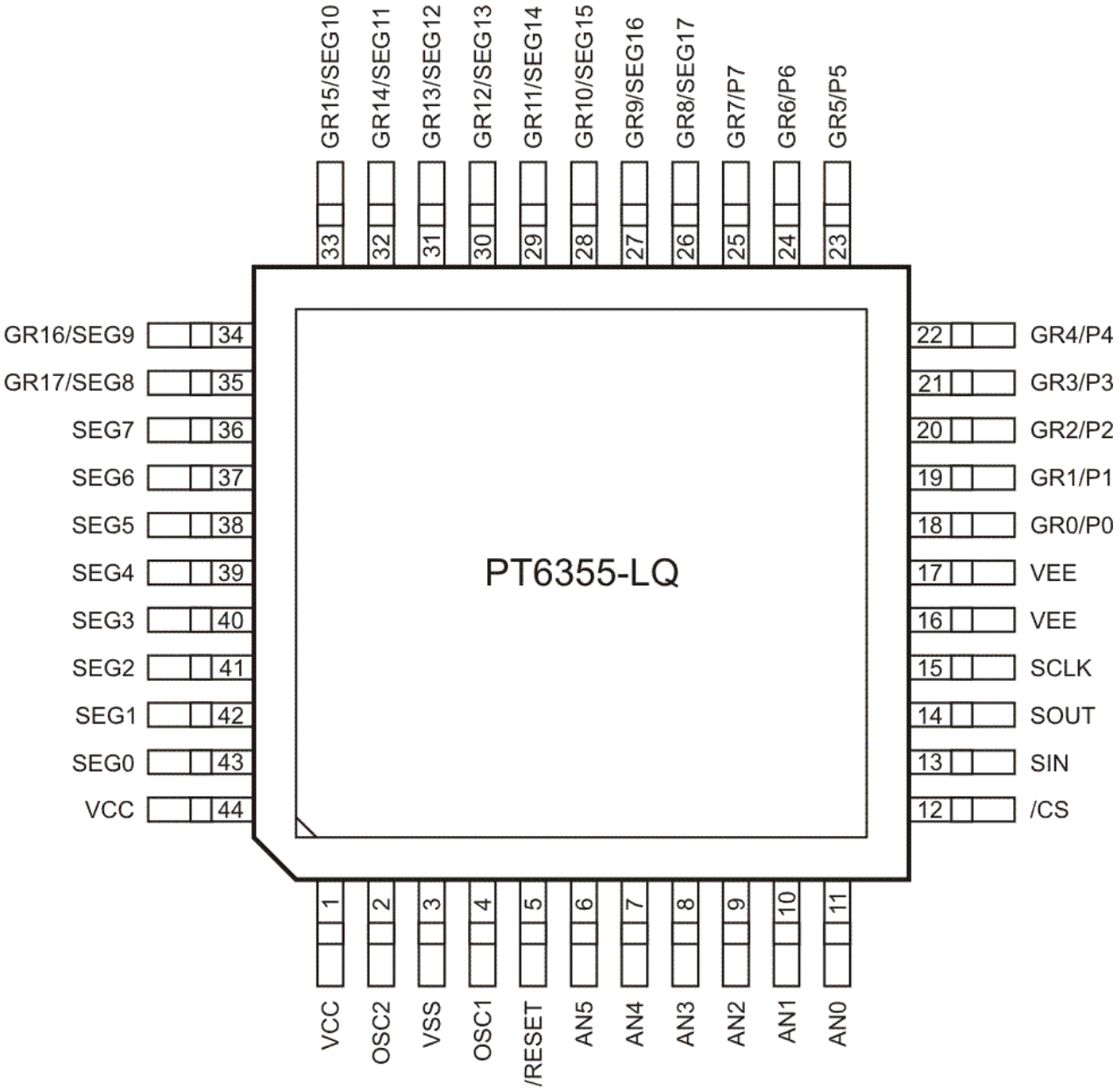
APPLICATION CIRCUIT



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6355-LQ/PT6355	44-pin, LQFP	PT6355-LQ/PT6355

PIN CONFIGURATION

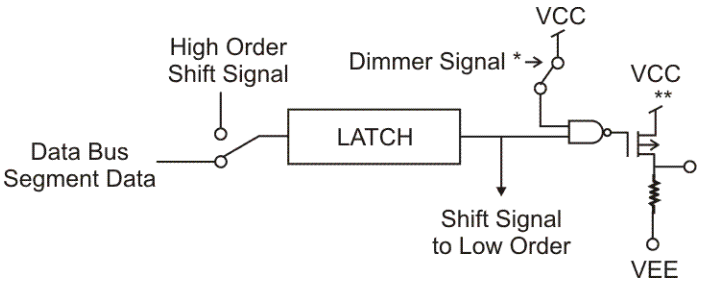


PIN DESCRIPTION

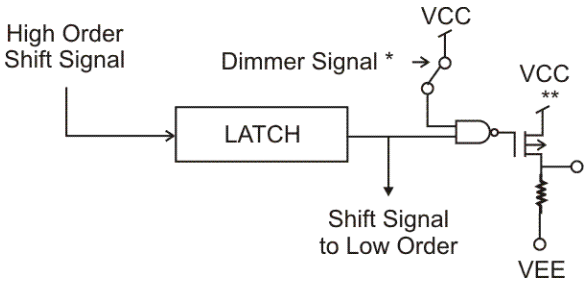
Pin Name	I/O	Description	Pin No.
VCC	-	Power supply	1, 44
OSC2	O	Oscillation output pin	2
VSS	-	Power supply	3
OSC1	I	Oscillation input pin	4
/Reset	I	Reset input pin Active ”L” Internal pull-high resistors are connected between this pin and the VCC pins.	5
AN5 to AN0	I	Analog to digital pin	6 to 11
/CS	I	Chip select	12
SIN	I	Serial input pin The clock is read twice with a 2MHz sampling rate in order to judge if the signal is a noise or not.	13
SOUT	O n-channel open drain	Serial output pin During the Reset condition, this pin is in high-impedance state.	14
SCLK	I	Serial clock input pin The clock is read twice with a 2MHz sampling rate in order to judge if the signal is a noise or not.	15
VEE	-	Pull-down power supply Supplies voltage to Pull-down resistors	16, 17
GR0/P0 to GR7/P7	O p-channel open drain	Grid/Port output pins This pin acts as either a Grid Output Pin or as an Ordinary Port Terminal. During the reset condition, this pin is set to VEE via a pull-down resistor.	18 to 25
GR8/SEG17 to GR17/SEG8	O p-channel open drain	Grid/Segment output pins This pin acts as either a Grid Output Pin or as an Segment Output Pin. During the reset condition, this pin is set to VEE via a pull-down resistor.	26 to 35
SEG0 to SEG7	O p-channel open drain	Segment output pin During the reset condition, this pin is set to VEE via a pull-down resistor.	43 to 36

PORT BLOCK DIAGRAM

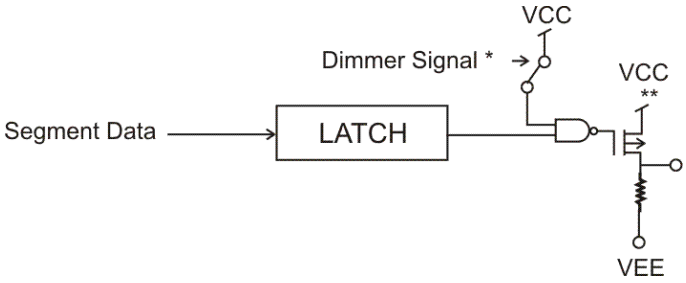
- **Grid/Port Pin & Grid/Segment Pin**



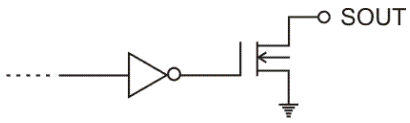
- **Grid Pin**



- **Segment Pin**



- **SOUT Pin**

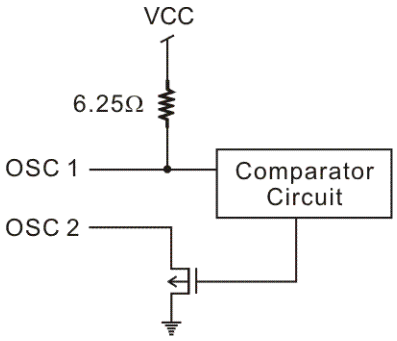


- **/CS Pin**

- **SIN, SCLK Pins**

- **A-D Input**

- **OSC1 & OSC2 Pins**

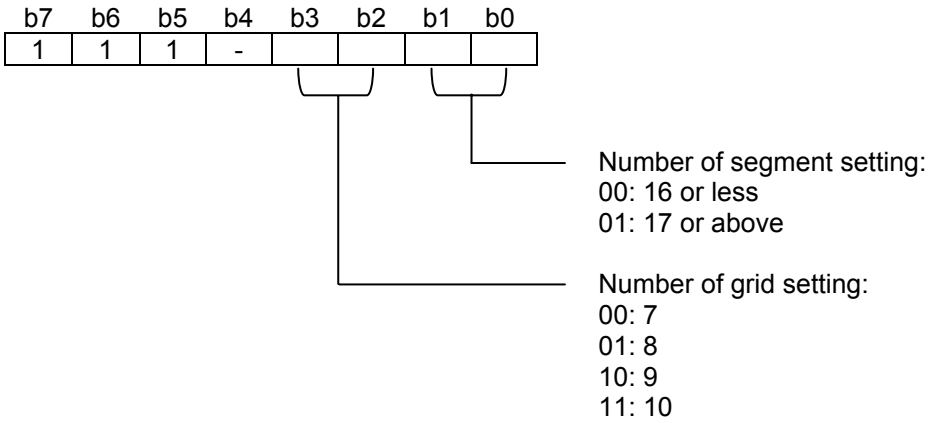


Notes:
1. * = Dimmer signal is for setting the T off time
2. ** = High-break down voltage P channel transistor

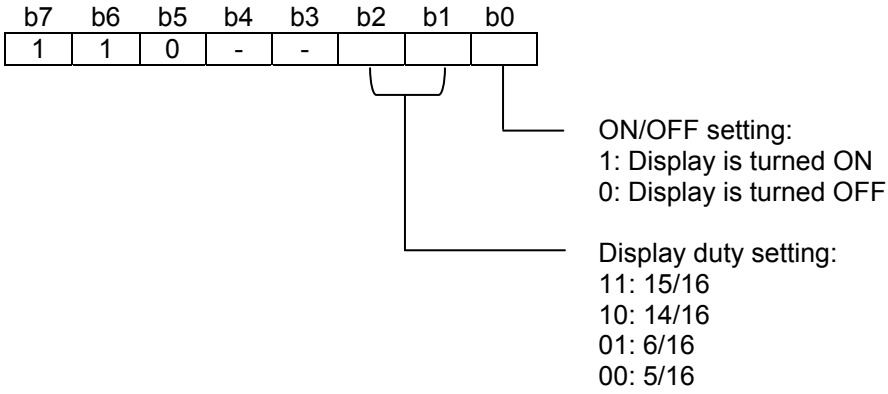
FUNCTION DESCRIPTION

COMMANDS

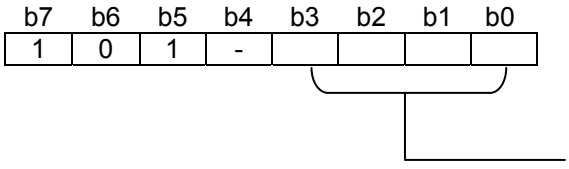
COMMAND 0: DISPLAY DATA SETTING



COMMAND 1: DISPLAY STATE SETTING

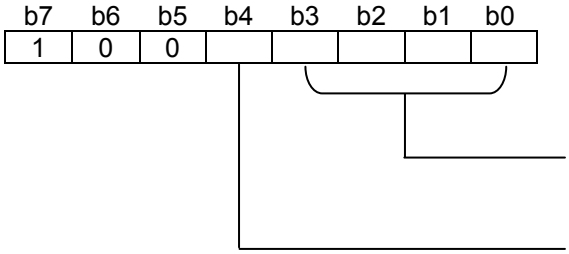


COMMAND 2: GRID SELECTION



Grid start pin settings:
0000: D17
0001: D16
0010: D15
0011: D14
0100: D13
0101: D12
0110: D11
0111: D10
1000: D9
1001: D8
1010: D7

COMMAND 3: PORT DATA SETTINGS



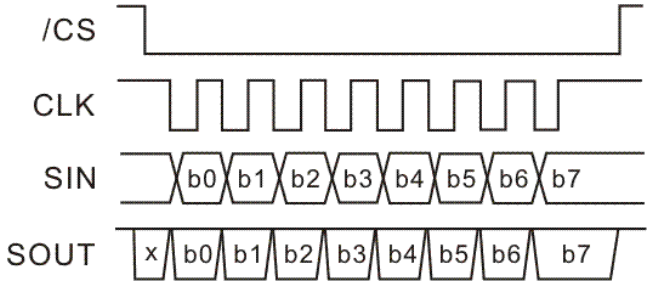
P3 to P0 / P7 to P4 output data

Port selection settings:
0: P3 to P0
1: P7 to P4

Note: In the event that a port has been selected (example: b4 = 0, P3 to P0 is selected), and at the same time the Grid Output Pin function is enabled, then the Grid Output having a higher priority than the Port Function will override the Port selection.

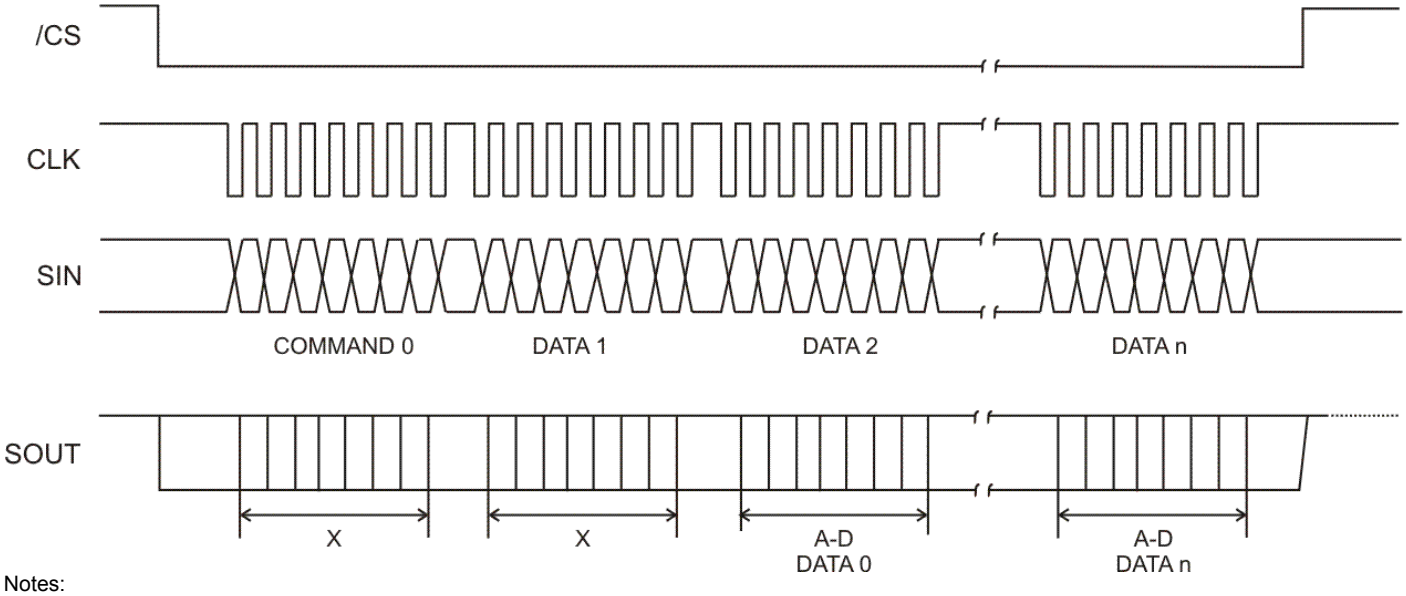
SERIAL INTERFACE PORTOCOL

BYTE PORTOCOL



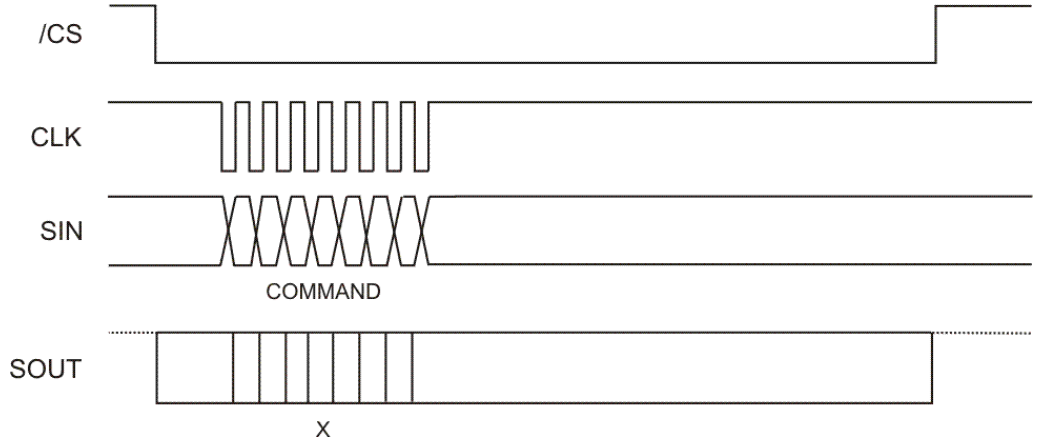
Note: When the CS Signal is “HIGH”, SOUT is in High-Impedance State.

COMMAND 0 POTOCOL



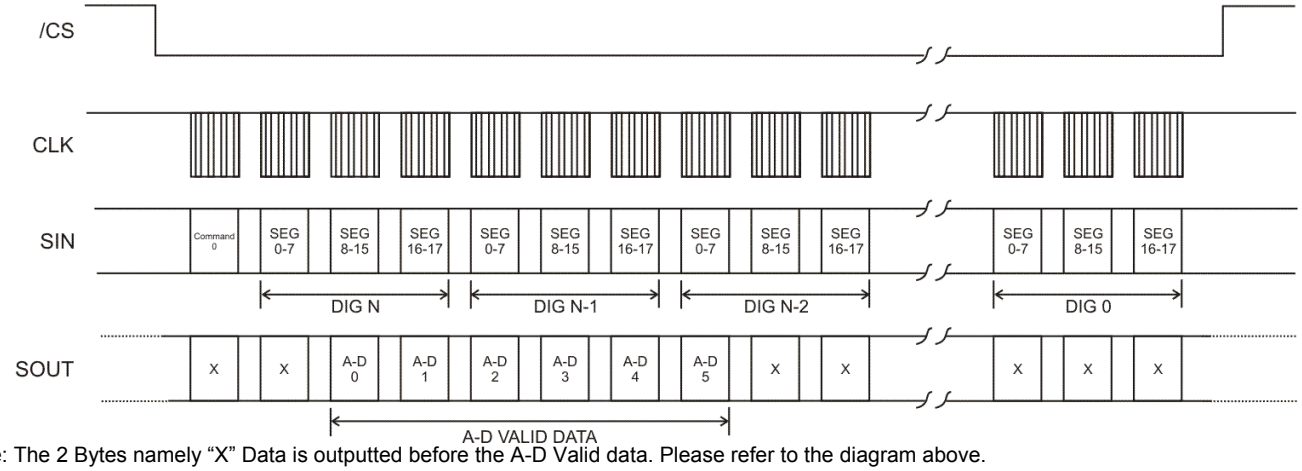
Notes:
1. The serial data which is transmitted after the execution of Command 0 is recognized as a Display Data. A-D Data 6 and above are defined as “x”.
2. After transferring a Display Data, the CS must be set to “HIGH” Level.

COMMANS 1 TO COMMAND 3



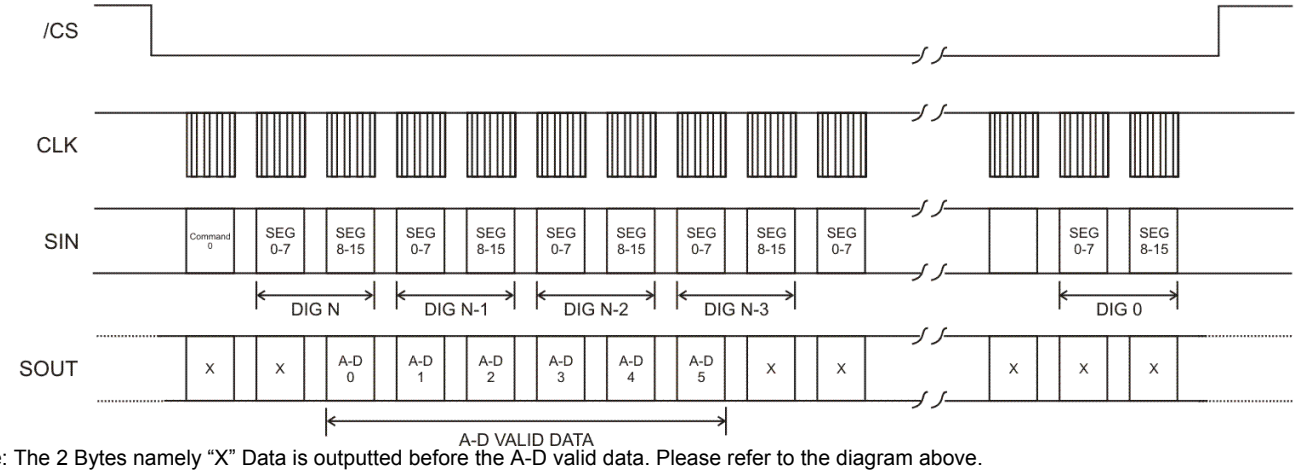
SERIAL COMMUNICATION FORMAT

3-BYTE TRANSFER: 17 SEGMENTS AND ABOVE



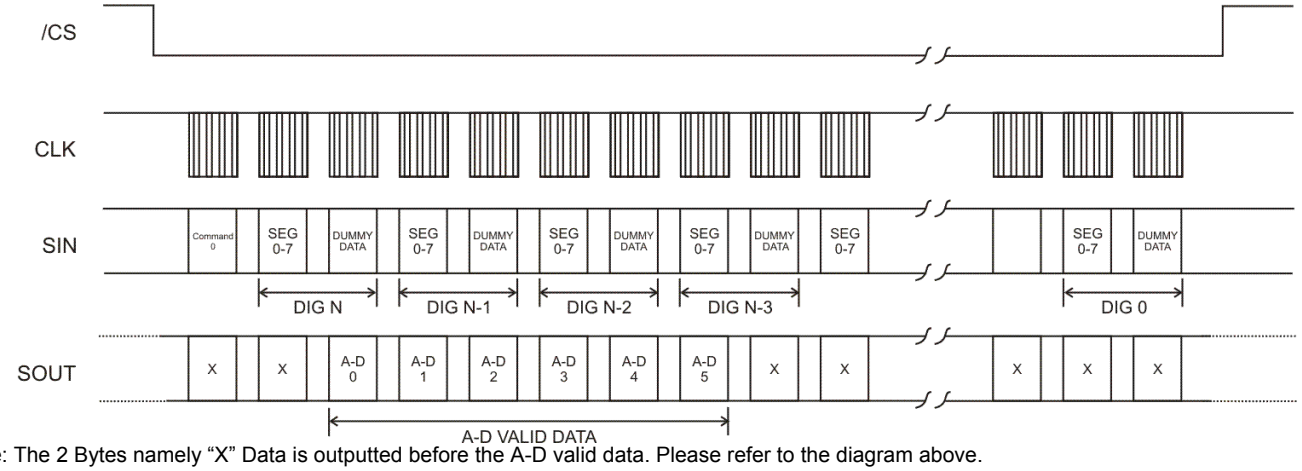
Note: The 2 Bytes namely “X” Data is outputted before the A-D Valid data. Please refer to the diagram above.

2-BYTE TRANSFER: 16 SEGMENTS OR BELOW



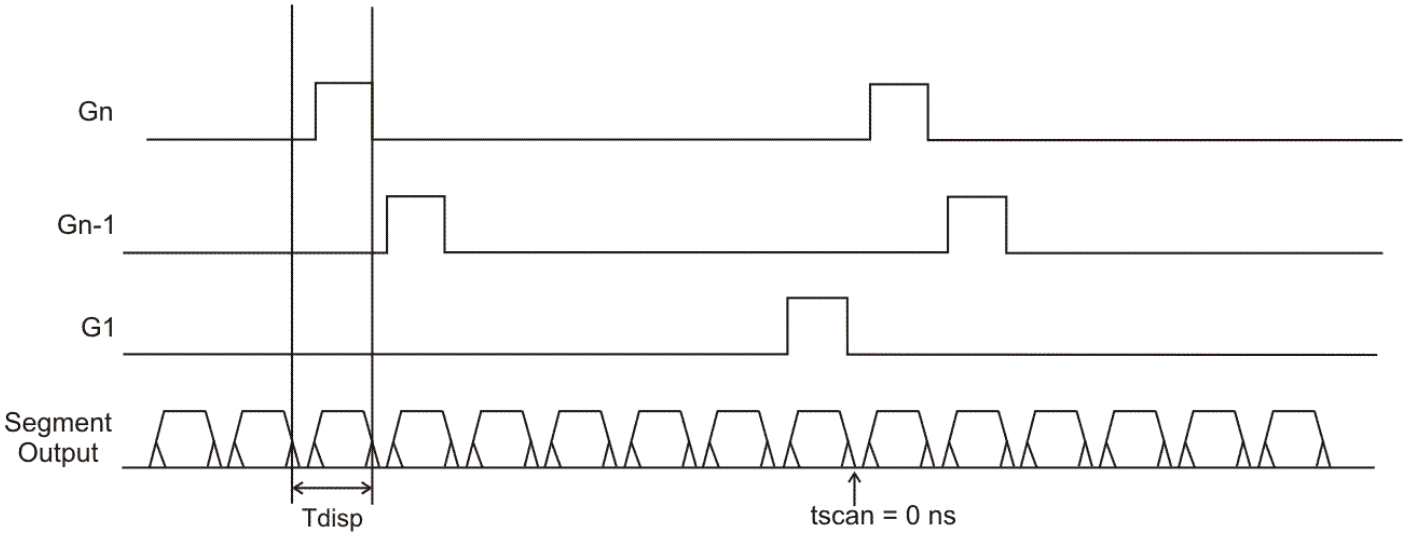
Note: The 2 Bytes namely “X” Data is outputted before the A-D valid data. Please refer to the diagram above.

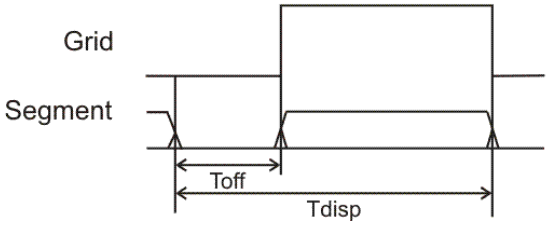
2-BYTE TRANSFER: 8 SEGMENTS OR LESS



Note: The 2 Bytes namely “X” Data is outputted before the A-D valid data. Please refer to the diagram above.

DISPLAY TIMING





Tdisp = 384 μs (oscillation frequency f(XIN) = 4.0 MHz)
Toff = 264 μs (5/16 x Tdisp)
240 μs (6/18 x Tdisp)
48 μs (14/16 x Tdisp)
24 μs (15/16 x Tdisp)

SEGMENT/GRID SETTING EXAMPLE

	Port	GR	SEG
1			SEG0
2			SEG1
3			SEG2
4			SEG3
5			SEG4
6			SEG5
7			SEG6
8			SEG7
9		GR17	SEG8
10		GR16	SEG9
11		GR15	SEG10
12		GR14	SEG11
13		GR13	SEG12
14		GR12	SEG13
15		GR11	SEG14
16		GR10	SEG15
17		GR9	SEG16
18		GR8	SEG17
19	P7	GR7	
20	P6	GR6	
21	P5	GR5	
22	P4	GR4	
23	P3	GR3	
24	P2	GR2	
25	P1	GR1	
26	P0	GR0	

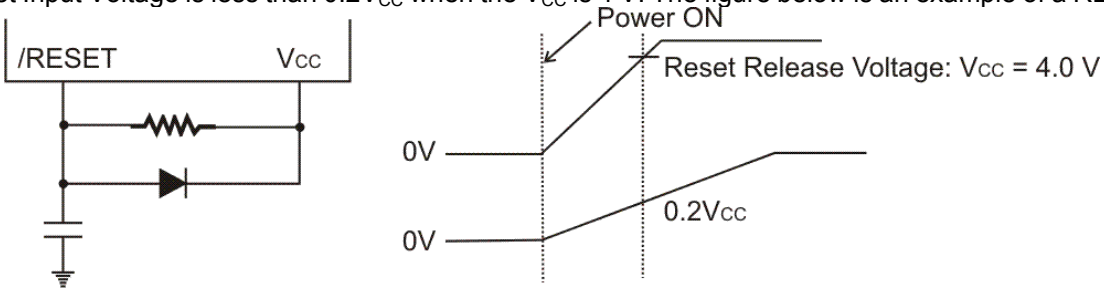
Grid: 7 Segment: 8	Grid: 10 Segment: 8	Grid: 10 Segment: 16	Grid: 7 Segment: 18
S1	S1	S1	S1
S2	S2	S2	S2
S3	S3	S3	S3
S4	S4	S4	S4
S5	S5	S5	S5
S6	S6	S6	S6
S7	S7	S7	S7
S8	S8	S8	S8
G7	G10	S9	S9
G6	G9	S10	S10
G5	G8	S11	S11
G4	G7	S12	S12
G3	G6	S13	S13
G2	G5	S14	S14
G1	G4	S15	S15
	G3	S16	S16
	G2	G10	S17
	G1	G9	S18
		G8	G7
		G7	G6
		G6	G5
		G5	G4
		G4	G3
		G3	G2
		G2	G1
		G1	

BIT ALLOCATION FOR DISPLAY MEMORY

Address	b7	b6	b5	b4	b3	b2	b1	b0	Grid
09_{16}							SEG17	SEG16	
$0A_{16}$	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	Grid 0
$0B_{16}$	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
$0D_{16}$							SEG17	SEG16	
$0E_{16}$	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	Grid 1
$0F_{16}$	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
11_{16}							SEG17	SEG16	
12_{16}	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	Grid 2
13_{16}	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
15_{16}							SEG17	SEG16	
16_{16}	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	Grid 3
17_{16}	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
19_{16}							SEG17	SEG16	
$1A_{16}$	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	Grid 4
$1B_{16}$	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
$1D_{16}$							SEG17	SEG16	
$1E_{16}$	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	Grid 5
$1F_{16}$	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
21_{16}							SEG17	SEG16	
22_{16}	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	Grid 6
23_{16}	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
25_{16}							SEG17	SEG16	
26_{16}	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	Grid 7
27_{16}	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
29_{16}							SEG17	SEG16	
$2A_{16}$	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	Grid 8
$2B_{16}$	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	
$2D_{16}$							SEG17	SEG16	
$2E_{16}$	SEG15	SEG14	SEG13	SEG12	SEG11	SEG10	SEG9	SEG8	Grid 9
$2F_{16}$	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	

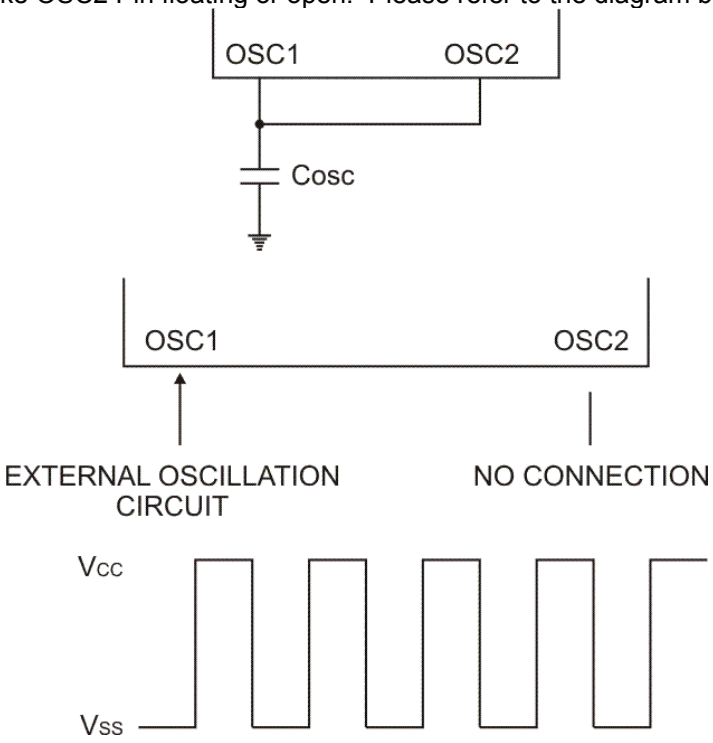
RESET FUNCTION

To enable the Reset Function of PT6355, the /RESET Pin must be set at "L" Level for 2 μs or more. After which the /RESET Pin reverts back to "H" Level and then the reset is released. The /RESET Pin returned to an "H" Level when the OSC1 oscillation is stable and the voltage of the power source is between 4.0 V and 5.5 V. It is very important to note that the Reset Input Voltage is less than $0.2V_{CC}$ when the V_{CC} is 4 V. The figure below is an example of a RESET Circuit.



OSCILLATION CIRCUIT

An oscillation circuit is constructed by connecting a capacitor between Oscillation pins -- OSC1 and OSC2 and V_{SS}. The Oscillation Pins -- OSC1 and OSC2 must be as "SHORT" as possible. If you are supplying a clock externally, apply the clock signal to OSC1 and make OSC2 Pin floating or open. Please refer to the diagram below.



SETTING UNUSED PINS

If a segment or grid pin will not be used, just leave it floating or open. The Analog Input Pin, however, must be connected to V_{CC} or V_{SS} via a resistor if it is not used. Please refer to the table below.

Pin Type	Connection
Segment	Open
Grid	Open
Analog Input	Connect to V_{CC} or V_{SS} via a resistor

ABSOLUTE MAXIMUMS RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Power source voltage	V_{CC}	All voltages are based on V_{SS} Output transistors are cut off.	-0.3 to 7.0	V
Pull-down power source voltage	VEE		V_{SS}-38 to V_{CC}+0.3	V
Input voltage (AN0~AN5)	Vi		-0.3 to V_{CC}+0.3	V
Input voltage (/CS, SIN, SCLK)	Vi		-0.3 to V_{CC}+0.3	V
Input voltage (/RESET)	Vi		-0.3 to V_{CC}+0.3	V
Output voltage (GR0~GR17) (SEG0~SEG17)	Vo	All voltages are based on V_{SS}. Output transistors are cut off. A waveform with frequency of 450 μs or more and a pulse width of 30 μs or less. Connect only capacitor load (CL = 200 pF)	V_{CC}-38 to V_{CC}+0.3	V
Output voltage (SOUT)	Vo	All voltage are based on Vss. Output transistors are cut off.	-0.3 to V_{CC}+0.3	V
Power dissipation	Pd	Ta=25℃	600	mW
Operating temperature	Topr	-	-40 to +85	℃
Storage temperature	Tstg	-	-65 to +150	℃

RECOMMENDED OPERATING CONDITIONS

(Unless otherwise specified, V_{CC} = 5 V, Ta = -20 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power source voltage	V_{CC}	4.5	5.0	5.5	V
Power source voltage	V_{SS}		0		V
Pull-down power source voltage	VEE	V_{CC}-35		V_{CC}	V
“H” input voltage (/CS, SIN, SCLK)	VIH	0.75V_{CC}		V_{CC}	V
“H” input voltage (/RESET)	VIH	0.8V_{CC}		V_{CC}	V
“L” input voltage (/CS, SIN, SCLK)	VIL	0		0.25V_{CC}	V
“L” input voltage (/RESET)	VIL	0		0.2V_{CC}	V

RECOMMENDED OPERATING CONDITIONS

(Unless otherwise specified, V_{CC} = 5 V, Ta = -20 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
“H” total peak output current[Note1] GR0~GR17, SEG0~SEG17	Σ IOH (peak)			-240	mA
“H” total peak output current GR0~GR17, SEG0~SEG17	Σ IOH (avg.)			-120	mA
“H” peak output current[Note2] GR0~GR17	IOH (peak)			-40	mA
“H” peak output current[Note2] SEG0~SEG7	IOH (peak)			-20	mA
“L” peak output current SOUT[Note2]	IOL (peak)			10	mA
“H” peak output current[Note3] GR0~GR17	IOH (avg.)			-18	mA
“H” peak output current[Note3] SEG0~SEG17	IOH (avg.)			-7	mA
“L” peak output current[Note3] SOUT	IOL (avg.)			5.0	mA
Main clock input oscillator[Note4] frequency	f (OSC1)		4.0	5.2	MHz
Serial I/O external clock frequency	f (SCLK))		250		KHz

Notes:
1. The total output current is the sum of all the current flowing through all the applicable ports. The total average current is the average/ or mean value measured over 100 ms. The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port.
3. The average output current is an average or mean value measured per 100 ms.
4. Under the condition that the oscillation frequency has a 50% duty cycle.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC} = 5 V, Ta = -20 to +85℃)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" output voltage	GR Output	VOH	IOH = -18 mA	V_{CC}-2			V
	SEG Output		IOH = -7 mA	V_{CC}-2			V
"L" output voltage	SOUT	VOL	IOL = 5 mA			2.0	V
Hysteresis	SIN,SCLK,/CS	VT+~VT-	V_{CC} = 5V		0.5		V
	/RESET,OSC1				0.5		V
"H" input current	SIN,SCLK,/CS	VIH	VI = V_{CC}			5.0	μA
	/RESET					5.0	μA
	OSC1				4.0		μA
"L" input current	SIN,SCLK,/CS	VIL	VI = V_{SS}			-5.0	μA
	/RESET				-150		μA
	OSC1[Note]				-0.8		mA
Output load current	GR0~GR17 SEG0~SEG17	ILOAD	VEE = V_{CC}-35 V, VOL = V_{CC}, Output Transistors OFF	250	500	750	μA
Output leakage current	GR0~GR17 SEG0~SEG17	ILEAK	VEE = V_{CC}-35 V, VOL = V_{CC}-35 V, Output Transistors OFF			-10	μA
RAM hold voltage		VRAM	When the clock is stopped	2.0		5.5	V
Power source current		ICC	V_{CC} = 5 V, f(OSC1) = 4 MHz, Output transistors OFF when A-D Converter is operating		0.5	1.0	mA

Note: See OSC1 & OSC2 Pins Port Diagram

A-D CONVERTER CHARACTERISTICS

(Unless otherwise specified, V_{CC} = 5 V, Ta = -20 to +85℃)

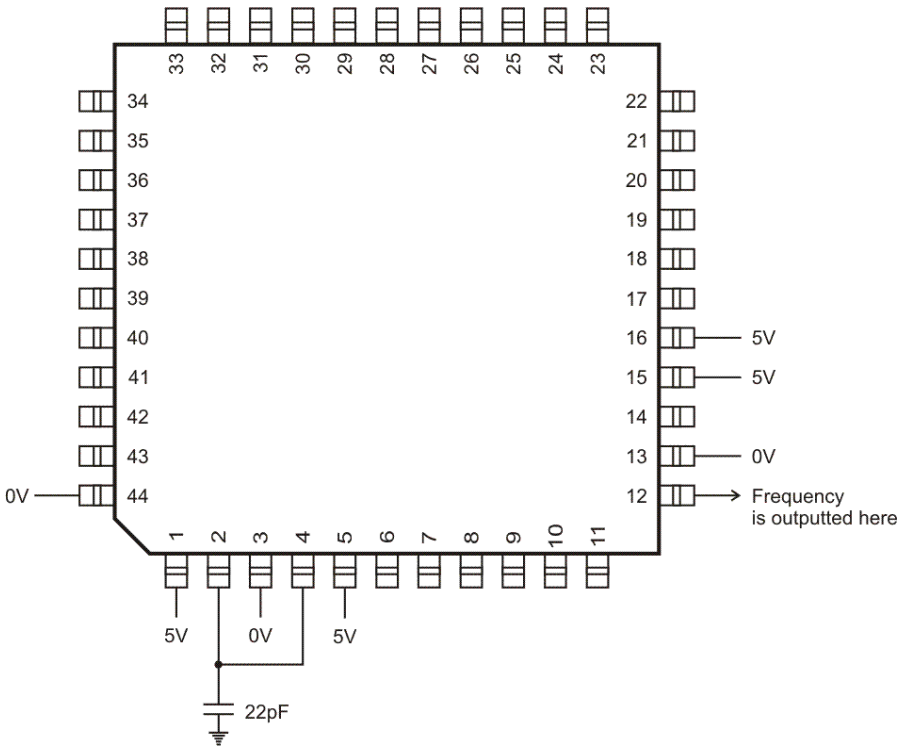
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution					8	Bits
Absolute accuracy (excluding quantization error)		V_{CC} = 5.12 V			+3	LSB
Conversion time	Tconv				100	tc (OSC1)
Analog input voltage	VIA		0		V_{CC}	V
Analog port input current	IIA			0.5	5.0	μA
Ladder resistor	Rladder			35		KΩ

TIMING REQUIRMENTS

(Unless otherwise specified, V_{CC} = 5 V, Ta = -20 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reset input "L" pulse width	tw (/RESET)	2			μs
Main clock input cycle time (OSC1 input)	tc (OSC1)	192			ns
Main clock input "H" pulse width (OSC1 Input)	twH (OSC1)	60			ns
Main clock input "L" pulse width (OSC1 Input)	twL (OSC1)	60			ns
Serial clock input cycle time Note2	tc (SCLK)	5			CLKs
Serial clock input "H" pulse width Note2	twH (SCLK)	2			CLKs
Serial clock input "L" pulse width Note2	twL (SCLK)	3			CLKs
Serial input set-up time Note2	tsu (SIN-SCLK)	2			CLKs
Serial input hold time Note2	th (SCLK-SIN)	3			CLKs
Serial input set-up time	tsu (/CS)	50tc (OSC1)			ns
Serial input hold time	th (/CS)	50tc (OSC1)			ns
Serial clock interval time	trec (SCLK)	50tc (OSC1)			ns

Notes:
1. tc (OSC1) = 1/fosc
2. The unit means the number of Noise Filter Sampling Clock [2 x tc (OSC1)]
3. Test Mode Frequency Measurement (refer to diagram):
   a. fosc= 2 x Frequency Value outputted by the CS Pin.
   b. twH (SCLK) = [(1/fosc) x 2] x 2
   c. twL (SCLK) = [(1/fosc) x 2] x 3
   d. trec (SCLK) = [50 x (1/fosc)]
   e. twH (SCLK), twL (SCLK) & trec (SCLK) are very important factors in writing the PT6355 software program.



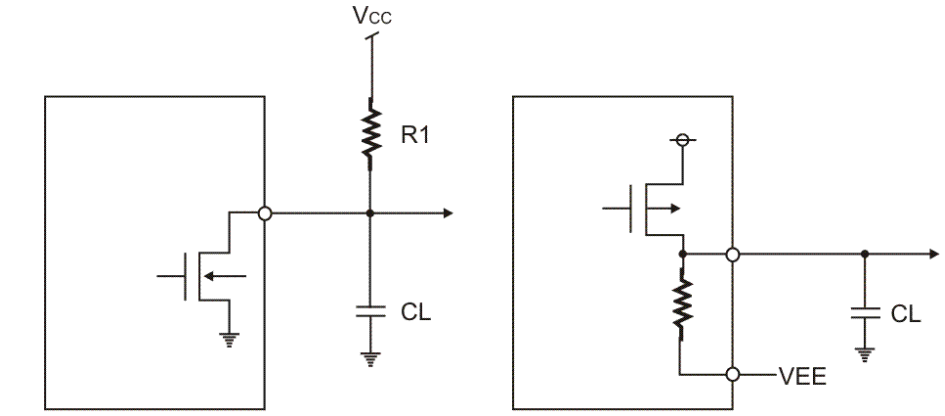
SWITCHING CHARACTERISTICS

(Unless otherwise specified, Vcc = 5 V, Ta = -20 to +85℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial I/O output delay time Note2	td (SCLK-SOUT)		4			CLKs
Serial I/O output valid time Note2	tv (SCLK-SOUT)		4			CLKs
High break down voltage P-Channel open drain output rising time	tr (Pch)	CL = 100 pF VEE = V_{CC}-35 V		1.8		µs
External capacitor size Note3	Cosc			22		pF

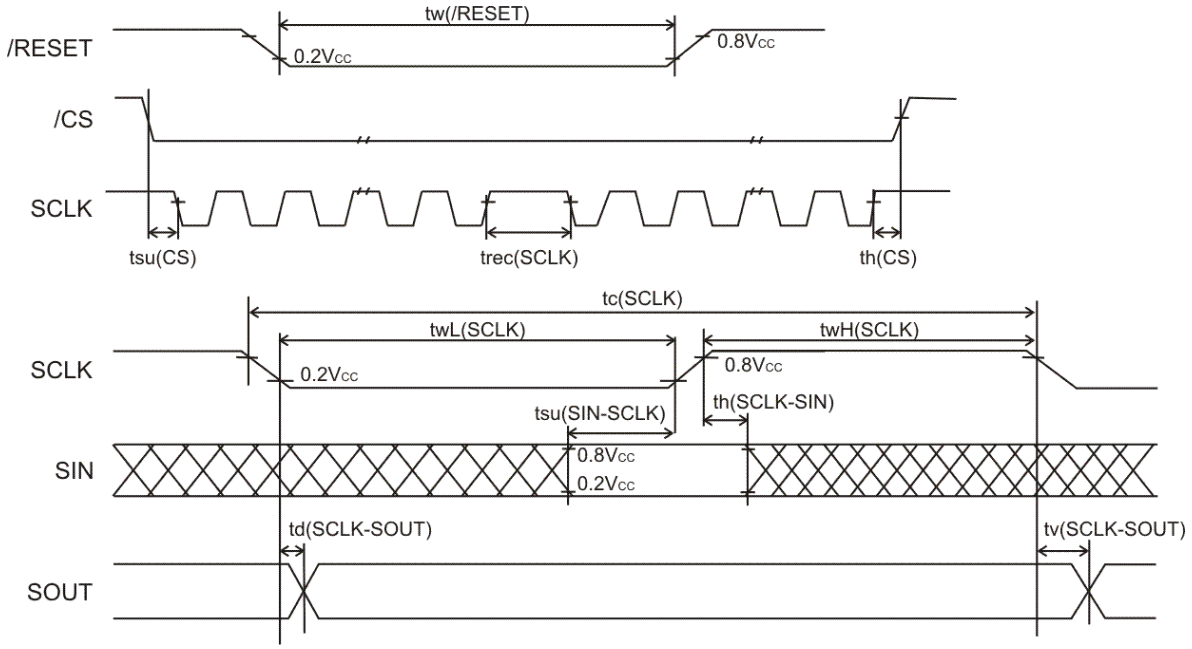
Notes:
1. tc(OSC1) = 1/fosc
2. The unit means the number of Noise Filter Sampling Clock (2 x tc(OSC1)).
3. An external capacitor size varies with a mounted condition.

OUTPUT SWITCHING CHARACTERISTICS MEASUREMENT APPLICATION CIRCUIT



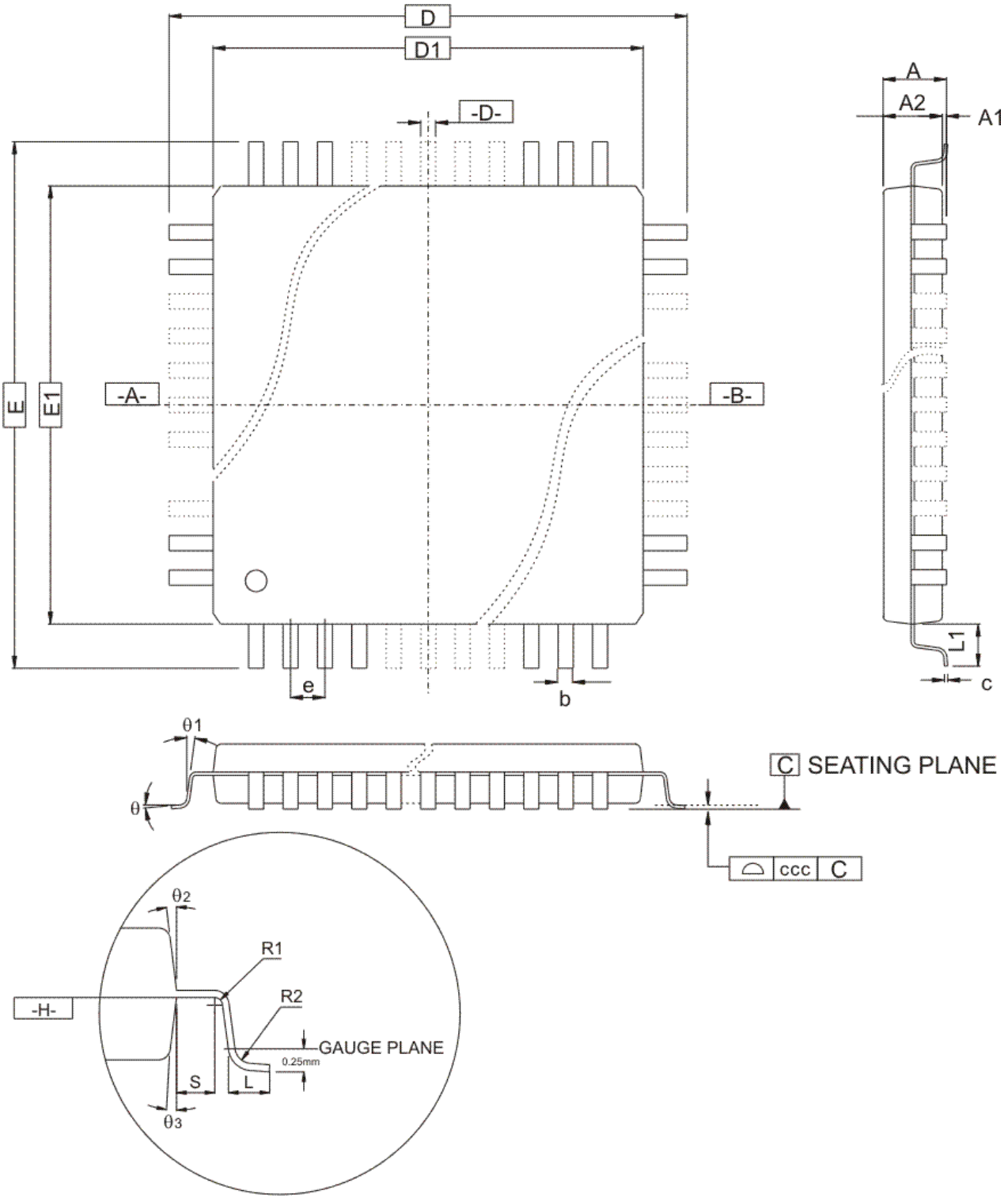
Serial I/O Clock Output Port　　P-Channel Output Port

TIMING DIAGRAM



PACKAGE INFORMATION

44-PIN, LQFP (BODY SIZE: 10 X 10 MM, PITCH SIZE: 0.8 MM, THK BODY: 1.40 MM)



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	-	0.20
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
e		0.80 BSC	
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
L	0.45	0.60	0.75
L1		1.00 REF	
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
ccc		0.10	

Notes:
1. All dimensions are in millimeters.
2. Refer to JEDEC MS-026 BCB.

IMPORTANT NOTICE

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