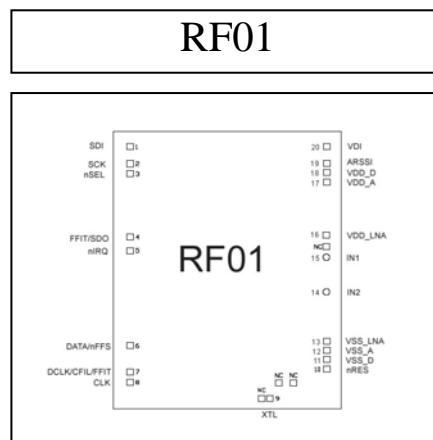


Universal ISM Band FSK Receiver RF01

DESCRIPTION:

Hope's RF01 is a single chip, low power, multi-channel FSK receiver designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 315, 433, 868, and 915 MHz bands. Used in conjunction with Hope's FSK transmitters, the RF01 is a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering are needed for operation.

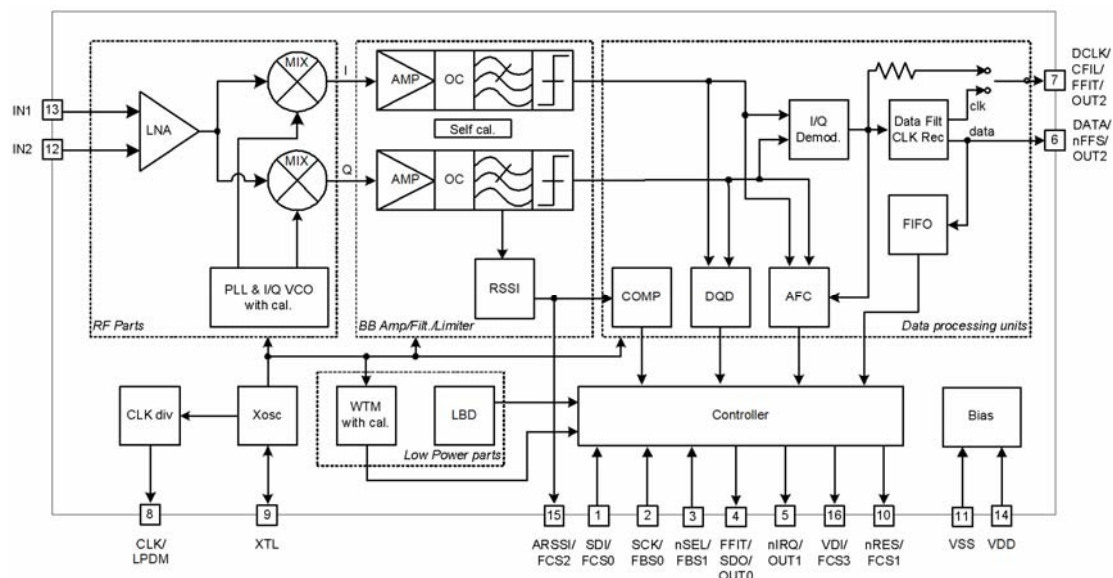


The RF01 has a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multi-path fading, and interference to achieve robust wireless links. The PLL's high resolution allows the usage of multiple channels in any of the bands. The baseband bandwidth (BW) is programmable to accommodate various deviation, data rate, and crystal tolerance requirements. The receiver employs the Zero-IF approach with I/Q demodulation, therefore no external components (except crystal and decoupling) are needed in a typical application. The RF01 is a complete analog RF and baseband receiver including a multi-band PLL synthesizer with an LNA, I/Q down converter mixers, baseband filters and amplifiers, and I/Q demodulator.

The chip dramatically reduces the load on the microcontroller with integrated digital data processing: data filtering, clock recovery, data pattern recognition and integrated FIFO. The automatic frequency control (AFC) feature allows using a low accuracy (low cost) crystal. To minimize the system cost, the chip can provide a clock signal for the microcontroller, avoiding the need for two crystals.

For low power applications, the device supports low duty-cycle operation based on the internal wake-up timer.

BLOCK DIAGRAM



FEATURES:

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- High bit rate (up to 115.2 kbps in digital mode and 256 kbps in analog mode)
- Direct differential antenna input
- Programmable baseband bandwidth (67 to 400 kHz)
- Analog and digital RSSI outputs
- Automatic frequency control (AFC)
- Data quality detection (DQD)
- Internal data filtering and clock recovery
- RX pattern recognition
- SPI compatible serial control interface
- Clock and reset signals for microcontroller
- 16 bit RX data FIFO
- Low power duty-cycle mode (less than 0.5 mA average supply current)
- Standard 10 MHz crystal reference
- Wake-up timer
- Low battery detector
- 2.2 to 5.4 V supply voltage
- Low power consumption (~9 mA in low bands)
- Low standby current (0.3 μ A)

TYPICAL APPLICATIONS

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED DESCRIPTION

General

The RF01 FSK receiver is the counterpart of the Hope's FSK transmitter. It covers the unlicensed frequency bands at 315, 433, 868, and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows for the use of multiple channels in any of the bands.

The receiver employs the Zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The RF01 consists of a fully integrated multi-band PLL synthesizer, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

The RF VCO in the PLL performs automatic calibration, which requires only a few microseconds. Calibration always occurs when the synthesizer begins. If temperature or supply voltage changes significantly, VCO recalibration can be invoked easily. Recalibration can be initiated at any time by switching the synthesizer off and back on again.

LNA

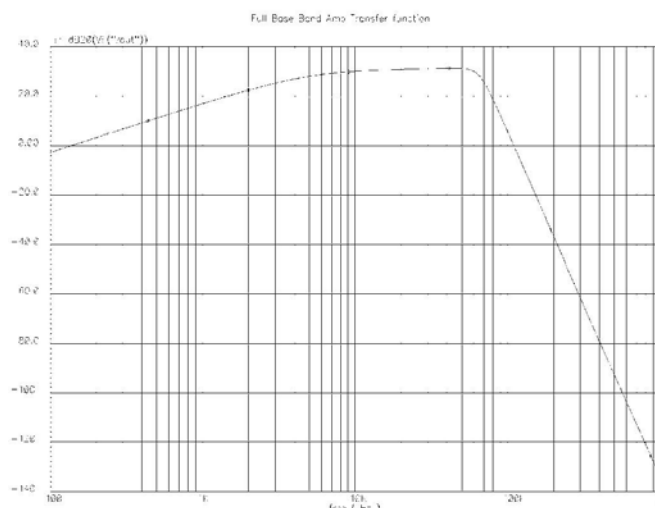
The LNA has 250 Ohm input impedance, which works well with the recommended antennas.

If the RF input of the chip is connected to 50 Ohm devices, an external matching circuit is required to provide the correct matching and to minimize the noise figure of the receiver.

The LNA gain (and linearity) can be selected (0, -6, -14, -20 dB relative to the highest gain) according to RF signal strength. This is useful in an environment with strong interferers.

Baseband Filters

The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. This allows setting up the receiver according to the characteristics of the signal to be received. An appropriate bandwidth can be selected to accommodate various FSK deviation, data rate, and crystal tolerance requirements. The filter structure is a 7-th order Butterworth low-pass with 40 dB suppression at 2*BW frequency. Offset cancellation is accomplished by using a high-pass filter with a cut-off frequency below 7 kHz.



Data Filtering and Clock Recovery

The output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

Analog operation:

The filter is an RC type low-pass filter and a Schmitt-trigger (St). The resistor (10k) and the St is integrated on the chip. An (external) capacitor can be chosen according to the actual bit-rate. In this mode the receiver can handle up to 256 kbps data rate.

Digital operation:

The data filter is a digital realization of an analog RC filter followed by a comparator with hysteresis. In this mode there is a clock recovery circuit (CR), which can provide synchronized clock to the data. With this clock the received data can fill the RX Data FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and requires more accurate data timing than in fast mode. In automatic mode the CR automatically changes between fast and slow modes. The CR starts in fast mode, then automatically switches to slow mode after locking.

(Only the data filter and the clock recovery use the bit-rate clock. Therefore, in analog mode, there is no need for setting the correct bit-rate.)

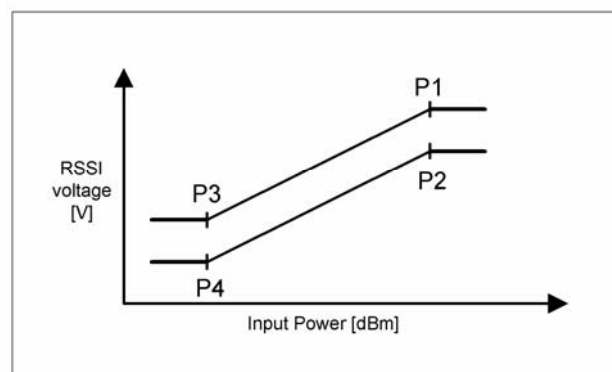
Data Validity Blocks

RSSI

A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given preprogrammed level. An analog RSSI signal is also available. The RSSI settling time depends on the filter capacitor used.

P1	-65 dBm	1300 mV
P2	-65 dBm	1000 mV
P3	-100 dBm	600 mV
P4	-100 dBm	300 mV

Voltage on ARSSI pin vs. Input RF power



DQD

The Data Quality Detector monitors the I/Q output of the baseband amplifier chain by counting the consecutive correct 0->1, 1->0 transitions. The DQD output indicates the quality of the signal to be demodulated. Using this method it is possible to "forecast" the probability of BER degradation. The programmable DQD parameter defines the threshold for signaling the good/bad data quality by the digital one-bit DQD output. In cases when the deviation is close to the bit rate, there should be four transitions during a single one bit period in the I/Q signals. As the bit rate decreases in comparison to the deviation, more and more transitions will happen during a bit period.

AFC

By using an integrated Automatic Frequency Control (AFC) feature, the receiver can synchronize its local oscillator to the received signal, allowing the use of:

- inexpensive, low accuracy crystals
- narrower receiver bandwidth (i.e. increased sensitivity)
- higher data rate

Crystal Oscillator

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet. The receiver can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal.

When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the Configuration Setting Command, the chip provides a fixed number (128) of further clock pulses ("clock tail") for the microcontroller to let it go to idle or sleep mode.

Low Battery Voltage Detector

The low battery detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 μ A typical) and can be programmed from 1 ms to several days with an accuracy of $\pm 5\%$.

It calibrates itself to the crystal oscillator at every startup, and then at every 30 seconds. When the crystal oscillator is switched off, the calibration circuit switches it back on only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing.

Event Handling

In order to minimize current consumption, the receiver supports the sleep mode. Active mode can be initiated by several wake-up events (wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up or receiving a request through the serial interface).

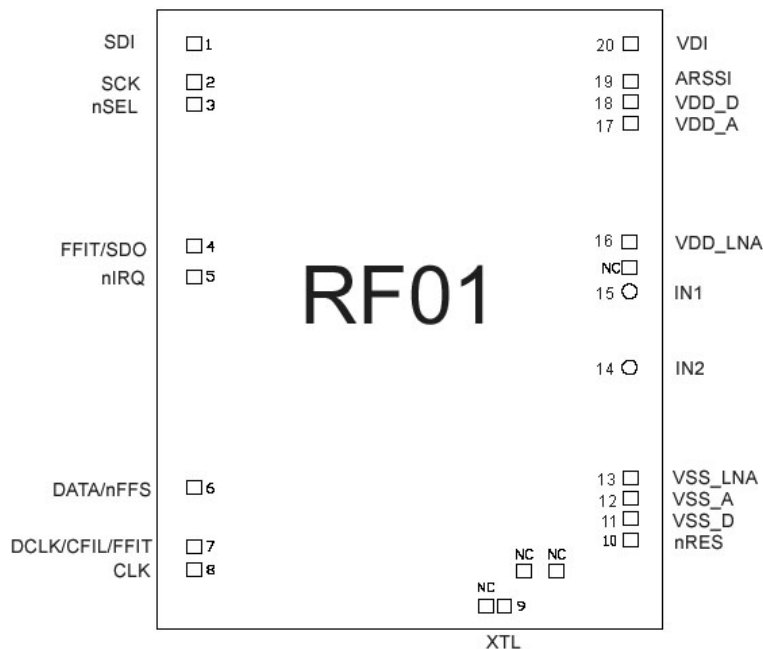
If any wake-up event occurs, the wake-up logic generates an interrupt signal which can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the receiver by the microcontroller through the SDO pin.

Interface and Controller

An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the receiver and the received data. It is also possible to store the received data bits into the 16bit RX FIFO register and read them out in a buffered mode. FIFO mode can be enabled through the SPI compatible interface by setting the fe bit to 1 in the Output and FIFO Mode Command.

PACKAGE PIN DEFINITIONS

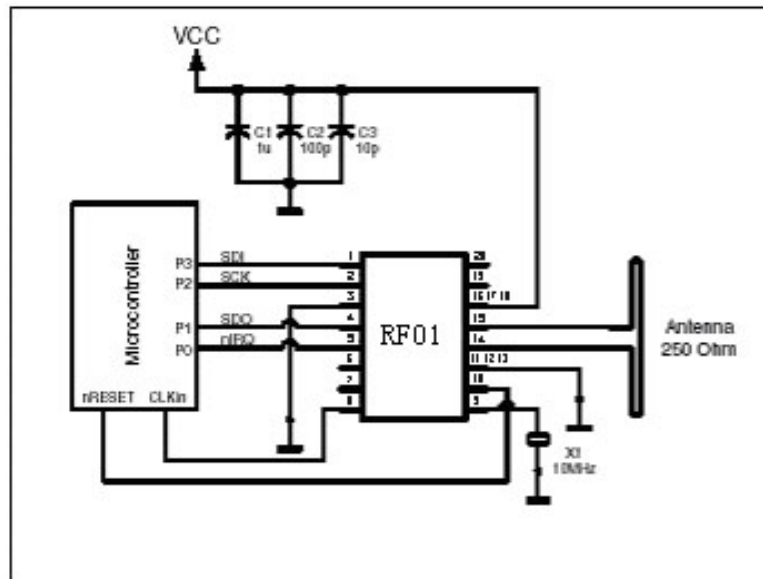
Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output



Pin	Name	Type	Function
1	SDI	DI	Data input of serial control interface
2	SCK	DI	Clock input of serial control interface
3	nSEL	DI	Chip select input of three-wire control interface (active low)
4	FFIT/SDO	DO	FIFO IT (active low) or serial data out for Status Read Command. Tristate with bushold cell if nSEL=H
5	nIRQ	DO	Interrupt request output, (active low)
6	DATA	DO	Received data output (FIFO not used)
	nFFS	DI	FIFO select input
7	DCLK	DO	Received data clock output (Digital filter used, FIFO not used)
	CFIL	AIO	External data filter capacitor connection (Analog filter used)
	FFIT	DO	FIFO IT (active high) FIFO empty function can be achieved when FIFO IT level is set to one
8	CLK	DO	Clock output for the microcontroller
9	XTL/REF	AIO	Crystal connection (other terminal of crystal to VSS) / External reference input
10	nRES	DO	Reset output (active low)
11	VSS_D	S	Digital VSS(connect to VSS)
12	VSS_A	S	Analog VSS(connect to VSS)
13	VSS_LNA	S	LNA VSS(connect to VSS)
14	IN2	AI	RF differential signal input
15	IN1	AI	RF differential signal input

16	VDD_LN	S	Positive supply voltage
17	VDD_A	S	Analog VDD(connect to VDD)
18	VDD_D	S	Digital VDD(connect to VDD)
19	ARSSI	AO	Analog RSSI output
20	VDI	DO	Valid Data Indicator output

Typical Application



GENERAL DEVICE SPECIFICATION

All voltages are referenced to V_{SS} , the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V _{dd}	Positive supply voltage	-0.5	6.0	V
V _{in}	Voltage on any pin	-0.5	V _{dd} +0.5	V
I _{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T _{st}	Storage temperature	-55	125	°C

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V _{dd}	Positive supply voltage	2.2	5.4	V
T _{op}	Ambient operating temperature	-40	85	°C

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range, typ conditions: $T_{op} = 27\text{ }^{\circ}\text{C}$;
 $V_{dd} = 2.7\text{ V}$)

DC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
I_{dd}	Supply current	315 and 433 MHz bands 868 MHz band 915 MHz band		9 10.5 12	11 12.5 14	mA
I_{pd}	Standby current	All blocks disabled		0.3		μA
I_{lb}	Low battery voltage detector current consumption			0.5		μA
I_{wt}	Wake-up timer current consumption (Note 1)			1.5		μA
I_x	Idle current	Crystal oscillator and base-band parts are ON		3.0	3.5	mA
V_{lb}	Low battery detect threshold	Programmable in 0.1 V steps	2.2		5.3	V
V_{lba}	Low battery detection accuracy			± 3		%
V_{il}	Digital input low level				$0.3 \cdot V_{dd}$	V
V_{ih}	Digital input high level		$0.7 \cdot V_{dd}$			V
I_{il}	Digital input current	$V_{il} = 0\text{ V}$	-1		1	μA
I_{ih}	Digital input current	$V_{ih} = V_{dd}$, $V_{dd} = 5.4\text{ V}$	-1		1	μA
V_{ol}	Digital output low level	$I_{ol} = 2\text{ mA}$			0.4	V
V_{oh}	Digital output high level	$I_{oh} = -2\text{ mA}$	$V_{dd}-0.4$			V

Note: Using the internal wake-up timer and counter reduces the overall current consumption, which should permit approximately 6 months operation from a 1500mAh battery.

AC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{LO}	Receiver frequency	315 MHz band, 2.5 kHz resolution 433 MHz band, 2.5 kHz resolution 868 MHz band, 5.0 kHz resolution 915 MHz band, 7.5 kHz resolution	310.24 430.24 860.48 900.72		319.75 439.75 879.51 929.27	MHz
BW	Receiver bandwidth	mode 0 mode 1 mode 2 mode 3 mode 4 mode 5	60 120 180 240 300 360	67 134 200 270 350 400	75 150 225 300 375 450	kHz
BR	FSK bit rate	With internal digital filters			115.2	kbps
BRA	FSK bit rate	With analog filter			256	kbps
P_{min}	Receiver Sensitivity	BER 10^{-3} , BW=67 kHz, BR=1.2 kbps (Note 1)		-109	-100	dBm
AFC_{range}	AFC locking range	δf_{FSK} : FSK deviation in the received signal		$0.8 \cdot \delta f_{FSK}$		
$IIP3_{inh}$	Input IP3	In band interferers in high bands		-21		dBm
$IIP3_{outh}$	Input IP3	Out of band interferers $f_{f_{LO}} > 4\text{ MHz}$		-18		dBm
$IIP3_{inl}$	IIP3 (LNA -6 dB gain)	In band interferers in low		-15		dBm

		bands				
IIP3 _{outl}	IIP3 (LNA –6 dB gain)	Out of band interferers $f - f_{LO} > 4\text{MHz}$		-12		dBm
CCR	Co-channel rejection	BER=10 ⁻² with continuous wave interferer in the channel		-7		dB
ACS	Adjacent channel selectivity	BER=10 ⁻² with continuous wave interferer in the adjacent channel, mode 0, channels at 134 kHz, BR=9.6 kbps, δf_{FSK} =30 kHz		23		dB
P _{max}	Maximum input power	LNA: high gain	0			dBm
R _{in}	RF input impedance real part (differential) (Note 2)	LNA gain (0, -14 dB) LNA gain (-6, -20 dB)		250 500		Ohm
C _{in}	RF input capacitance			1		pF
RS _a	RSSI accuracy			+/-5		dB
RSr	RSSI range			46		dB
C _{ARSSI}	Filter capacitance for ARSSI		1			nF
RS _{step}	RSSI programmable level steps			6		dB
RS _{resp}	DRSSI response time	Until the RSSI output goes high after the input signal exceeds the pre-programmed limit. CARRSI=5nF		500		μs

Note 1: See the BER diagrams in the measurement results section for detailed information.

Note 2: See matching circuit parameters and antenna design guide for information.

AC Characteristics (continued)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f _{ref}	PLL reference frequency	(Note 3)	8	10	12	MHz
f _{res}	PLL frequency resolution	Depends on selected bands	2.5		7.5	kHz
t _{lock}	PLL lock time	Frequency error < 1kHz after 10 MHz step		20		us
t _{st, P}	PLL startup time	With running crystal oscillator			250	us
C _{xl}	Crystal load capacitance, see crystal selection guide	Programmable in 0.5 pF steps, tolerance +/-10%	8.5		16	pF
t _{POR}	Internal POR pulse width (Note4)	After V _{dd} has reached 90% of final value		50	100	ms
t _{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ohms			5	ms
t _{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.96		1.08	ms
t _{wake-up}	Programmable wake-up time		1		5*10 ¹¹	ms
C _{in, D}	Digital input capacitance				2	pF
t _{r, f}	Digital output rise/fall time	15 pF pure capacitive load			10	ns

Note 3: Using other than a 10 MHz crystal is not recommended because the crystal referred timing and frequency parameters will change accordingly.

Note 4: During this period, commands are not accepted by the chip.

CONTROL INTERFACE

Commands to the receiver are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control registers.

The receiver will generate an interrupt request (IRQ) for the microcontroller on the following events:

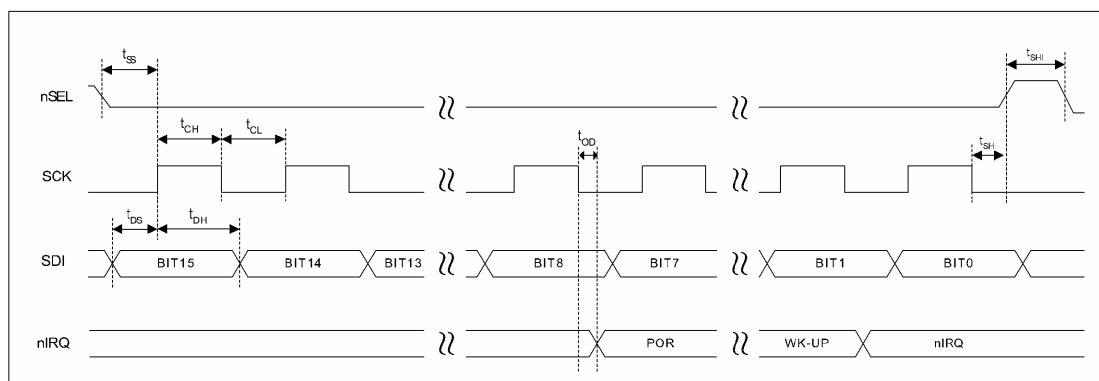
- Supply voltage below the preprogrammed value is detected (LBD)
- Wake-up timer timeout (WK-UP)
- FIFO received the preprogrammed amount of bits (FFIT)
- FIFO overflow (FFOV)

FFIT and FFOV are applicable only when the FIFO is enabled. To find out why the nIRQ was issued, the status bits should be read out.

Timing Specification

Symbol	Parameter	Minimum Value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Timing Diagram



Control Commands

Control Word	Related Parameters/Functions
Configuration Setting Command	Frequency band, crystal oscillator load capacitance, baseband filter bandwidth, etc.
Frequency Setting Command	Set the frequency of the local oscillator
Receiver Setting Command	Set VDI source, LNA gain, RSSI threshold,
Wake-up Timer Command	Wake-up time period
Low Duty-Cycle Command	Enable low duty cycle mode. Set duty-cycle.
Low Battery Detector and Clock Divider Command	Set LBD voltage and microcontroller clock division ratio
AFC Control Command	Set AFC parameters
Data Rate Command	Bit rate
Data Filter Command	Set data filter type, clock recovery parameters
Output and FIFO Command	Set FIFO IT level, FIFO start control, FIFO enable and FIFO fill enable

Note: In the following tables the POR column shows the default values of the command registers after power on.

Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	b1	b0	eb	et	ex	x3	x2	x1	x0	i2	i1	i0	dc	893Ah

b1	b0	Frequency Band [MHz]
0	0	315
0	1	433
1	0	868
1	1	915

i2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	67
1	1	1	reserved

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
.....				
1	1	1	0	15.5
1	1	1	1	16.0

Bits eb and et control the operation of the low battery detector and wake-up timer, respectively. They are enabled when the corresponding bit is set.

If ex is set the crystal is active during sleep mode.

When dc bit is set it disables the clock output

Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A680h

The 12-bit Frequency Setting Command <f11 : f0> has the value F. The value F should be in the range of 96 and 3903.

When F is out of range, the previous value is kept. The synthesizer center frequency f can be calculated as:

$$f_0 = 10 \text{ MHz} * C1 * (C2 + F/4000)$$

The constants C1 and C2 are determined by the selected band as:

Band [MHz]	C1	C2
315	1	31
433	1	43
868	2	43
915	3	30

Receiver Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d1	d0	g1	g0	r2	r1	r0	en	C0C1h

Bits 7-6 select the VDI (valid data indicator) signal:

d1	d0	VDI output
0	0	Digital RSSI Out (DRSSI)
0	1	Data Quality Detector Output (DQD)
1	0	Clock recovery lock
1	1	Always

Bits 5-4 LNA gain set:

g1	g0	GLNA (dB relative to max. G)
0	0	0
0	1	-14
1	0	-6
1	1	-20

Bits 3-1 control the threshold of the RSSI detector:

r2	r1	r0	RSSIsetth [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85
1	0	0	-79
1	0	1	-73
1	1	0	-67
1	0	1	-61

The RSSI threshold depends on the LNA gain, the real RSSI threshold can be calculated:

$$RSSI_{th} = RSSI_{setth} + G_{LNA}$$

Bit 0 (en) enables the whole receiver chain and crystal oscillator when set. Enable/disable of the wake-up timer and the low battery detector are not affected by this setting.

Note: Clock tail is not generated when the crystal oscillator is controlled by en bit.

Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up time period can be calculated by M <m7 : m0> and R <r4 : r0>:

$$T_{\text{wake-up}} = M * 2^R \text{ ms}$$

Low Duty-Cycle Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	d6	d5	d4	d3	d2	d1	d0	en	CCOEh

With this command Low Duty-Cycle operation can be set in order to decrease the average power consumption. The time cycle is determined by the Wake-Up Timer Command.

The Duty-Cycle is calculated by D <d6 : d0> and M. (M is parameter in a Wake-Up Timer Command.)

$$D.C. = (D * 2 + 1) / M * 100\%$$

Low Battery Detector and Microcontroller Clock Divider Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	d2	d1	d0	t4	t3	t2	t1	t0	C200h

The 5-bit value T of t4-t0 determines the threshold voltage of the threshold voltage V_{lb} of the detector:

$$V_{lb} = 2.2 \text{ V} + T * 0.1 \text{ V}$$

Clock divider configuration:

d2	d1	d0	Clock Output Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

AFC Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	a1	a0	r1	r0	st	fi	oe	en	C6F7h

Bit 0 (en) enables the calculation of the offset frequency by the AFC circuit (it allows the addition of the content of the output register to the frequency control word of the PLL).

Bit 1 (oe) when set, enables the output (frequency offset) register Bit 2 (fi) when set, switches the circuit to high accuracy (fine) mode. In this case the processing time is about four times longer, but the measurement uncertainty is less than half.

Bit 3 (st) strobe edge, when st goes to high, the actual latest calculated frequency error is stored into the output registers of the AFC block.

Bit 4-5 (r10, r11) range limit: Limits the value of the frequency offset register to the following values:

r11	r10	Max dev [f _{res}]
0	0	No restriction
0	1	+15/-16
1	0	+7/-8
1	1	+3/-4

f_{res}:

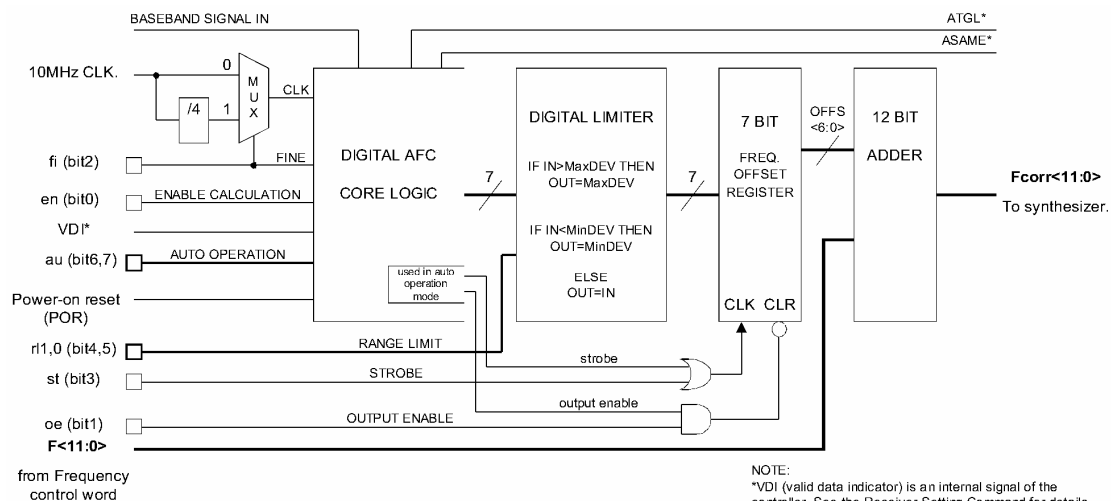
315, 433MHz bands: 2.5kHz

868MHz band: 5kHz

915MHz band: 7.5kHz

Bit 6-7 (a0, a1) Automatic operation mode selector:

a1	a0	
0	0	Auto mode off (Strobe is controlled by microcontroller)
0	1	Runs only once after each power-up
1	0	Keep the offset only during receiving (VDI=high)
1	1	Keep the offset value independently from the state of the VDI signal



In automatic operation mode (no strobe signal is needed from the microcontroller to update the output offset register), the AFC circuit is automatically enabled when VDI indicates a potential incoming signal during the whole measurement cycle and the circuit measures the same result in two subsequent cycles.

There are three operation modes, example from the possible application:

1, (a1=0, a0=1) The circuit measures the frequency offset only once after power up. This way, the extended TX/RX maximum distance can be achieved.

Possible application:

In the final application when the user is inserted the battery the circuit measures and compensate the frequency offset caused by the crystal tolerances. This method enables to use cheaper quartz in the application and provide quite good protection against locking in an interferer.

2a, (a1=1, a0=0) The circuit measures automatically the frequency offset during an initial low data rate pattern –easier to receive- (i.e.: 00110011) of the package and change the receiving frequency according that. The further part of the package can be received by the corrected frequency settings.

2b, (a1=1, a0=0) The transmitter must transmit the first part of the packet with a step higher deviation and later there is a possibility to reduce it.

In both cases (2a and 2b) when the VDI indicates poor receiving conditions (VDI goes low) the output register is automatically cleared. It's suggested to use when one receiver receives signal from more than one transmitter.

3, (a1=1, a0=1) It is similar to the 2a and 2b modes, but 3 is suggested to use when a receiver operates with only one transmitter. After a complete measuring cycle, the measured value is held independently of the state of VDI signal.

Data Filter Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	a1	m1	1	s1	s0	f2	f1	f0	C42Ch

Bit 7 <a1>: Clock recovery (CR) auto lock control if set. It means that the CR start in fast mode after locking it automatically switches to slow mode.

Bit 6 <m1>: Clock recovery lock control 1: fast mode, fast attack and fast release 0: slow mode, slow attack and slow release Using the slower one requires more accurate bit timing (see Data Rate Command).

Bit3-4<s0 : s1>: Select the type of the data filter:

s1	s0	Filter Type
0	0	Reserved
0	1	Digital
1	0	Reserved

Digital: this is a digital realization of an analog RC filter followed by a comparator with hysteresis. The time constant is automatically adjusted to the bit rate defined by the Data Rate Command.

Analog RC filter: the demodulator output is fed to the pin 7 over a 10 kOhm resistor. The filter characteristic is set by the external capacitor connected to this pin and VSS. (Suggested value for 9600 bps is 3.3 nF)

Bit 0-2 <f0 : f2>: DQD threshold parameter.

Note: To let the DQD report "good signal quality" the threshold parameter should be less than 4 in the case when the bit-rate is close to the deviation. At higher deviation/bit-rate settings higher threshold parameter can report "good signal quality" as well.

Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	cs	r6	r5	r4	r3	r2	r1	r0	C823h

The expected bit rate of the received data stream is determined by the 7-bit value R (bits r6 to r0) and the 1 bit cs.

$$BR = 10 \text{ MHz} / 29 / (R+1) / (1 + cs*7)$$

In the receiver set R according the next function:

$$R = (10 \text{ MHz} / 29 / (1 + cs*7) / BR) - 1$$

Apart from setting custom values, the standard bit rates from 600 bps to 115.2 kbps can be approximated with small error.

Data rate accuracy requirements:

Clock recovery in slow mode: $\Delta BR/BR < 1/(29 \cdot N_{\text{bit}})$

Clock recovery in fast mode: $\Delta BR/BR < 3/(29 \cdot N_{\text{bit}})$

BR is the bit rate set in the receiver and ΔBR is bit rate difference between the transmitter and the receiver. N is the maximal number of bit consecutive ones or zeros in the data stream. It is recommended for long data packets to include enough 1/0 and 0/1 transitions, and be careful to use the same division ratio in the receiver and in the transmitter.

ΔBR is a theoretical limit for the clock recovery circuit. Clock recovery will not work above this limit. The clock recovery circuit will always operate below this limit independently from process, temperature, or V_{dd} condition.

E.g. Supposing a maximum length of consecutive zeros or ones in the data stream is less than 5 bits, the necessary relative accuracy is 0.68% in slow mode and 2.1% in fast mode.

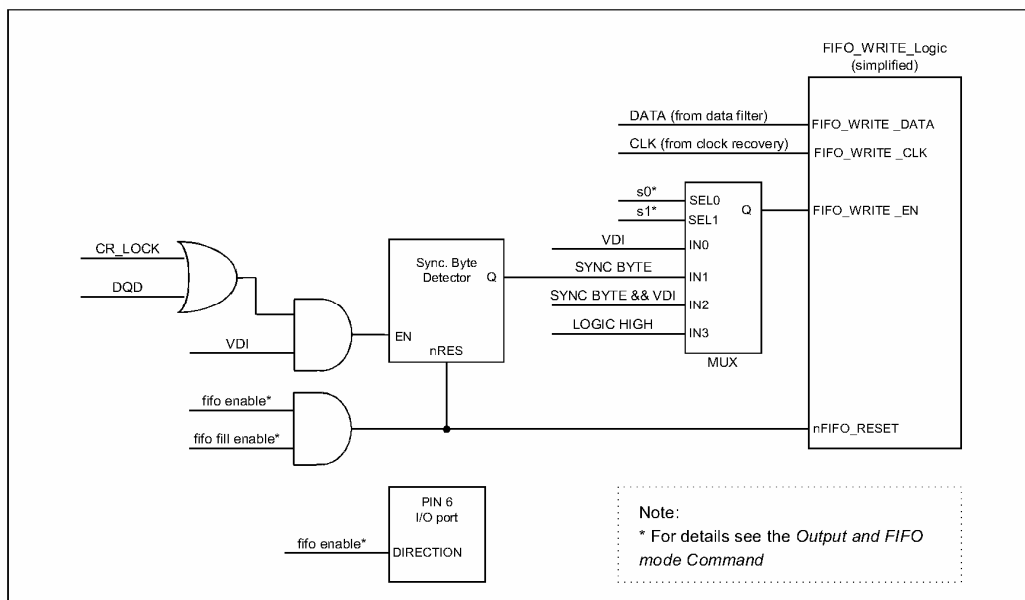
Output and FIFO Mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	f3	f2	f1	f0	s1	s0	ff	fe	CE85h

Bit 4-7 <f3:f0>: FIFO IT level. The FIFO generates IT when number of the received data bits reaches this level.

Bit 2-3 <s1:s0>: Set the input of the FIFO fill start condition:

s1	s0	
0	0	VDI
0	1	Sync. Word
1	0	reserved
1	1	Always



Note: VDI (Valid Data Indicator) see further details in *Receiver Control Word*.

Bit 1: <ff> Enables FIFO fill after synchron word reception. FIFO fill stops when this bit is cleared.

Bit 0: <fe> Enables the 16bit deep FIFO mode. To clear the FIFO's counter and content, it has to be set zero.

Note: To restart the synchron word reception bit 1 should be cleared and set. This action will initialize the

FIFO and clear its content. Bit 0 modifies the function of pin 6 and pin 7. Pin 6 (nFFS) will become input if f_e is set to 1. If the chip is used in FIFO mode, do not allow this to be a floating input.

Reset Mode Command

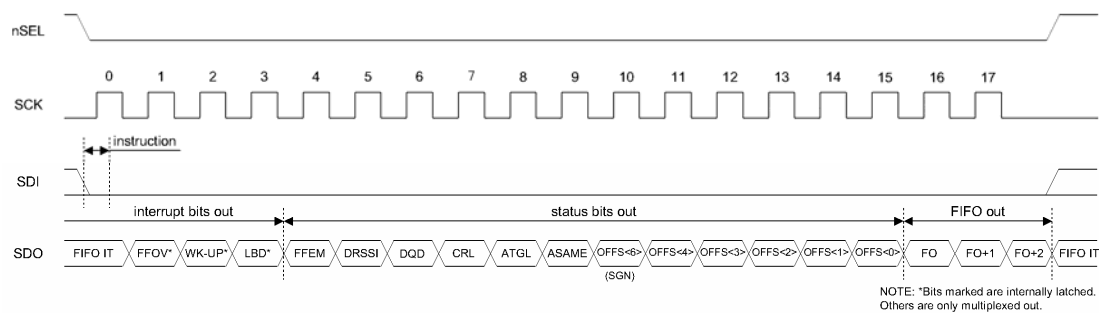
bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	dr	DAOOh

Bit 0 (*dr*): Disables the highly sensitive RESET mode. If this bit is cleared, a 600 mV glitch in the power supply may cause a system reset. For more detailed description see the *Reset modes* section.

Status Read Command:

The read command starts with a zero, whereas all other control commands start with a one. Therefore, after receiving the first bit of the control command the RF01 identifies it as a read command. So as the first bit of the command is received, the receiver starts to clock out the status bits on the SDO output as follows:

Status Register Read Sequence with FIFO Read Example



It is possible to read out the content of the FIFO after the reading of the status bits. The command can be aborted after any read bits by rising edge of the select signal.

Note: The FIFO IT bit behaves like a status bit, but generates nIRQ pulse if active. To check whether there is a sufficient amount of data in the FIFO, the SDO output can be tested. In extreme speed critical applications, it can be useful to read only the first four bits (FIFO IT -LBD) to clear the FFOV, WK-UP, and LBD bits. During the FIFO access the f_{SCK} cannot be higher than $f_{ref}/4$, where f_{ref} is the crystal oscillator frequency. If the FIFO is read in this mode the nFFS input must be connected to logic high level.

Definitions of the bits in the above timing diagram:

FIFO IT	Number of the data bits in the FIFO is reached the preprogrammed limit
FFOV	FIFO overflow
WK-UP	Wake-up timer overflow
LBD	Low battery detect, the power supply voltage is below the preprogrammed limit
FFEM	FIFO is empty
DRSSI	The strength of the incoming signal is above the preprogrammed limit
DQD	Data Quality Detector detected a good quality signal

CRL	Clock recovery lock
ATGL	Toggling in each AFC cycle
ASAME	AFC stabilized (measured twice the same offset value)
OFFS6, 4-0	Offset value to be add to the value of the Frequency control word

FIFO Buffered Data Read

In this operating mode, incoming data are clocked into a 16 bit FIFO buffer. The receiver starts to fill up the FIFO when the Valid Data Indicator (VDI) bit and/or the synchron word recognition circuit indicates potentially real incoming data. This prevents the FIFO from being filled with noise and overloading the external microcontroller.

For further details see the Receiver Setting Command and the Output and FIFO Command.

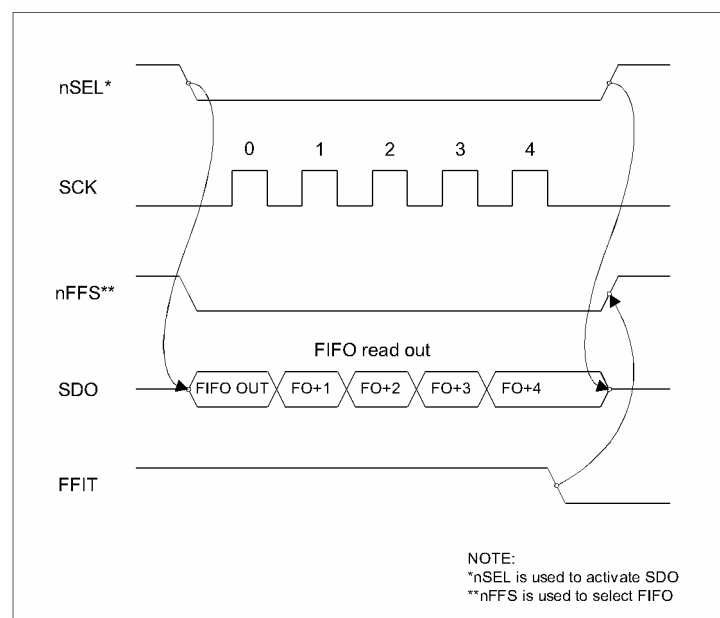
Polling Mode:

The nFFS signal selects the buffer directly and its content could be clocked out through pin SDO by SCK. Set the FIFO IT level to 1. In this case, as long as FFIT indicates received bits in the FIFO, the controller may continue to take the bits away. When FFIT goes low, no more bits need to be taken. An SPI read command is also available.

Interrupt Controlled Mode:

The user can define the FIFO level (the number of received bits) which will generate the nFFIT when exceeded. The status bits report the changed FIFO status in this case.

FIFO Read Example with FFIT Polling:



During FIFO access the f_{SCK} cannot be higher than $f_{ref}/4$, where f_{ref} is the crystal oscillator frequency.

RX-TX ALIGNMENT PROCEDURES

RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To

minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

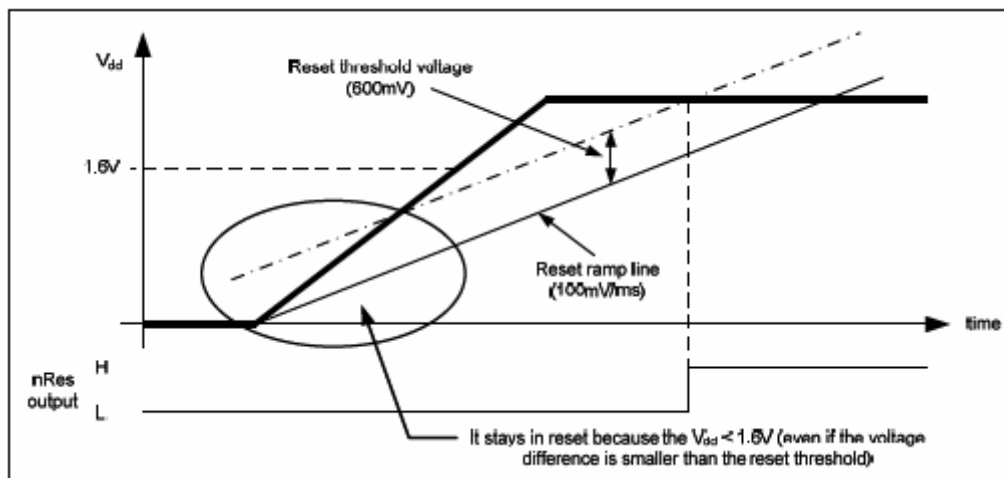
To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

Power-on reset

After power up the supply voltage starts to rise from 0V. The reset block has an internal ramping voltage reference (reset-ramp signal), which is rising at 100mV/ms (typical) rate. The chip remains in reset state while the voltage difference between the actual V_{dd} and the internal reset-ramp signal is higher than the reset threshold voltage, which is 600 mV (typical). As long as the V_{dd} voltage is less than 1.6V (typical) the chip stays in reset mode regardless the voltage difference between the V_{dd} and the internal ramp signal. The reset event can last up to 150ms supposing that the V_{dd} reaches 90% its final value within 1ms. During this period the chip does not accept control commands via the serial control interface.

Power-on reset example:



Power glitch reset

The internal reset block has two basic mode of operation: normal and sensitive reset. The default mode is sensitive, which can be changed by the appropriate control command (see *Related control commands* at the end of this section). In normal mode the power glitch detection circuit is disabled.

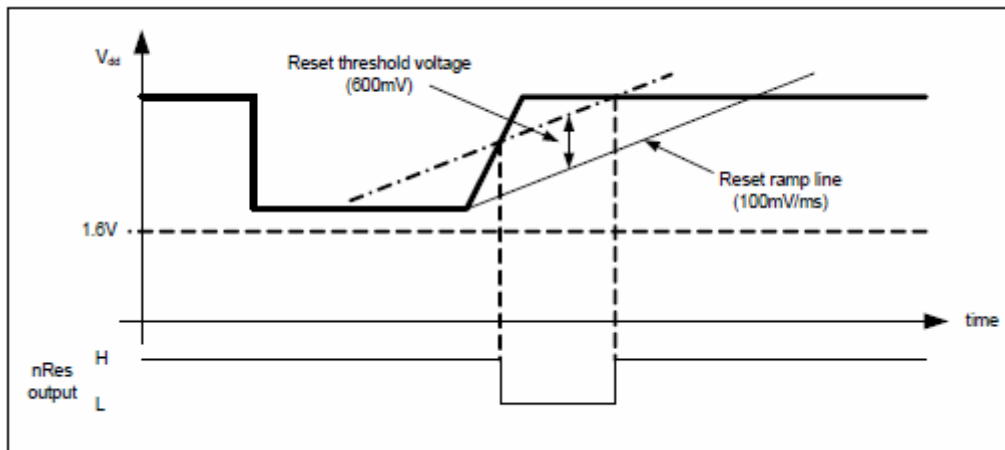
There can be spikes or glitches on the V_{dd} line if the supply filtering is not satisfactory or the internal resistance of the power supply is too high. In such cases if the sensitive reset is enabled an (unwanted) reset will be generated if the positive going edge of the V_{dd} has a rising rate greater than 100mV/ms and the voltage difference between the internal ramp signal and the V_{dd} reaches the reset threshold voltage (600 mV). Typical case when the battery is weak and due to its increased internal resistance a sudden decrease of the current consumption (for example turning off the power amplifier) might lead to an increase in supply voltage. If for some reason the sensitive reset cannot be disabled step-by-step decrease of the current consumption (by turning off the different stages one by one) can help to avoid this problem.

Any negative change in the supply voltage will not cause reset event unless the V_{dd} level reaches the reset threshold voltage (250mV in normal mode, 1.6V in sensitive reset mode).

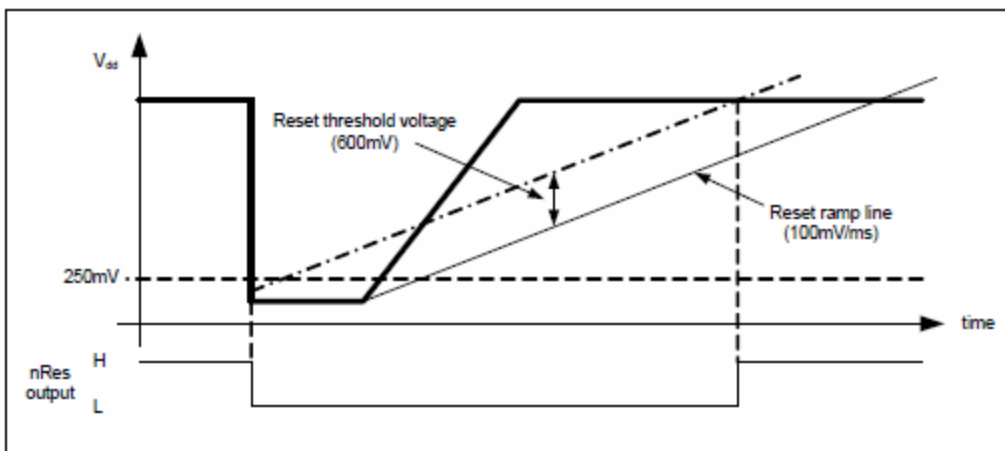
If the sensitive mode is disabled and the power supply turned off the V_{dd} must drop below 250mV in order to trigger a power-on reset event when the supply voltage is turned back on. If the decoupling capacitors keep their charges for a long time it could happen that no reset will be generated upon power-up because the power glitch detector circuit is disabled.

Note that the reset event reinitializes the internal registers, so the sensitive mode will be enabled again.

Sensitive Reset Enabled, Ripple on V_{dd} :



Sensitive reset disabled:



Software reset

Software reset can be issued by sending the appropriate control command (described at the end of the section) to the chip. The result of the command is the same as if power-on reset was occurred. When the nRES pin connected to the reset pin of the microcontroller, using the software reset command may cause unexpected problems.

V_{dd} line filtering

During the reset event (caused by power-on, fast positive spike on the supply line or software reset command) it is very important to keep the V_{dd} line as smooth as possible. Noise or periodic disturbing signal superimposed the supply voltage may prevent the part getting out from reset state. To avoid this phenomenon use adequate filtering on the power supply line to keep the level of the disturbing signal below 10mV_{p-p} in the DC – 50kHz range for 200ms from V_{dd} ramp start.. Typical example when a switch-mode regulator is used to supply the

radio, switching noise may be present on the V_{dd} line. Follow the manufacturer's recommendations how to decrease the ripple of the regulator IC and/or how to shift the switching frequency.

Related control commands

"Reset Mode Command"

Setting bit<0> to high will change the reset mode to normal from the default sensitive.

"SW Reset Command"

Issuing FF00h command will trigger software reset. See the Wake-up Timer Command.

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the RF01 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C_0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 300 ohms ESR (equivalent series loss resistance). However, lower C_0 and ESR values guarantee faster oscillator startup.

The crystal frequency is used as the reference of the PLL, which generates the local oscillator frequency (f_{LO}). Therefore f_{LO} is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable local oscillator frequency error.

Maximum XTAL Tolerances Including Temperature and Aging [ppm]

Bit Rate: 2.4kbps	Transmitter Deviation [± kHz]						
	30	60	90	120	150	180	210
315 MHz	30	75	100	100	100	100	100
433 MHz	20	50	75	100	100	100	100
868 MHz	10	25	40	60	75	100	100
915 MHz	10	25	40	50	75	75	100

Bit Rate: 9.6kbps	Transmitter Deviation [± kHz]						
	30	60	90	120	150	180	210
315 MHz	25	70	100	100	100	100	100
433 MHz	15	50	75	100	100	100	100
868 MHz	8	25	40	60	75	75	100
915 MHz	8	25	40	50	70	75	100

Bit Rate: 38.3kbps	Transmitter Deviation [± kHz]						
	30	60	90	120	150	180	210
315 MHz	don't use	30	75	100	100	100	100
433 MHz	don't use	20	50	75	100	100	100
868 MHz	don't use	10	30	40	60	75	100
915 MHz	don't use	10	25	40	60	75	75

Whenever a low frequency error is essential for the application, it is possible to "pull" the crystal to

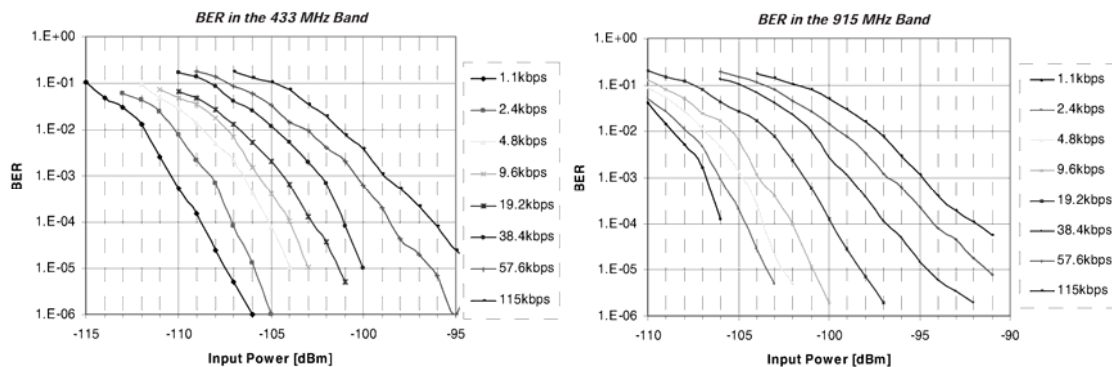
the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”, for example 16 pF. The “pull-ability” of the crystal is defined by its motional capacitance and C_0 .

The on chip AFC is capable to correct TX/RX carrier offsets as much as 80% of the deviation of the received FSK modulated signal.

Note: There may be other requirements for the TX carrier accuracy with regards to the requirements as defined by standards and/or channel separations.

MEASUREMENT RESULTS

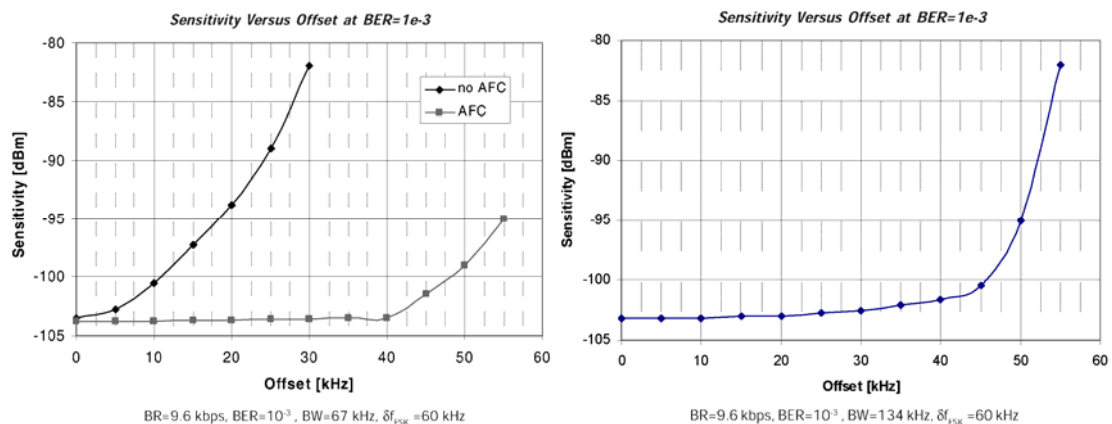
BER Measurement Results



1.134 kbps	2.4 kbps	4.8 kbps	9.6 kbps	19.2 kbps	38.4 kbps	57.6 kbps	115 kbps
BW=67 kHz	BW=67 kHz	BW=67 kHz	BW=67 kHz	BW=67 kHz	BW=134 kHz	BW=134 kHz	BW=200 kHz
$\delta f_{FSK} = 30$ kHz	$\delta f_{FSK} = 30$ kHz	$\delta f_{FSK} = 30$ kHz	$\delta f_{FSK} = 45$ kHz	$\delta f_{FSK} = 45$ kHz	$\delta f_{FSK} = 90$ kHz	$\delta f_{FSK} = 90$ kHz	$\delta f_{FSK} = 120$ kHz

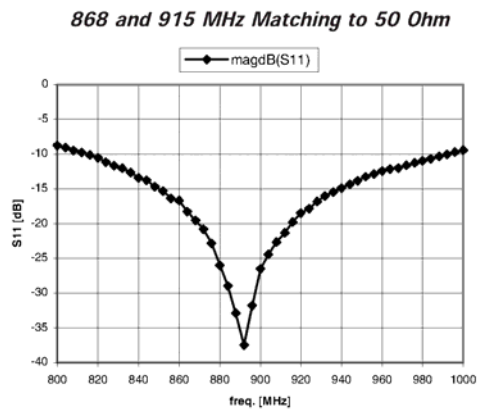
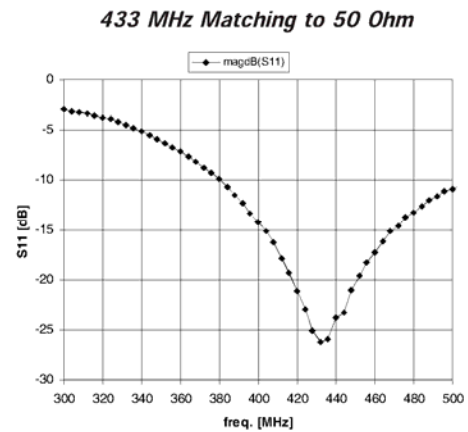
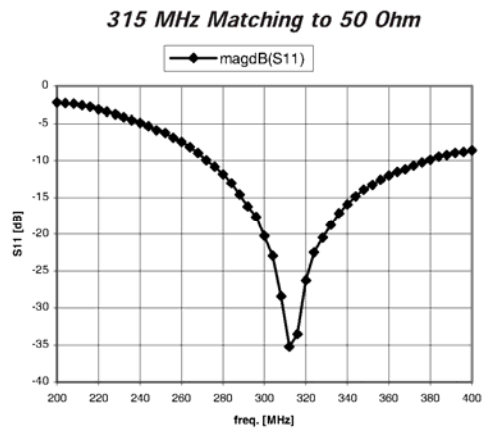
The table shows the optimal BW and δf_{FSK} selection for different data rates

Frequency Offset Effected Sensitivity Degradation



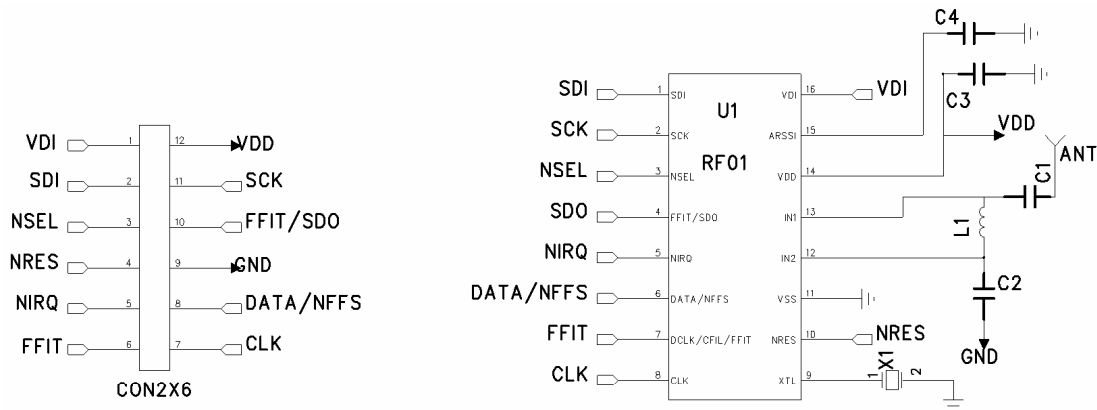
Input impedance

Measured input return loss on the demo boards with suggested matching circuit



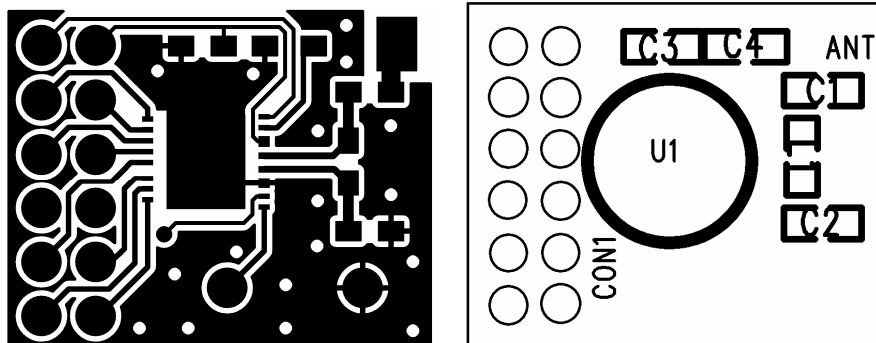
REFERENCE DESIGNS

Schematic

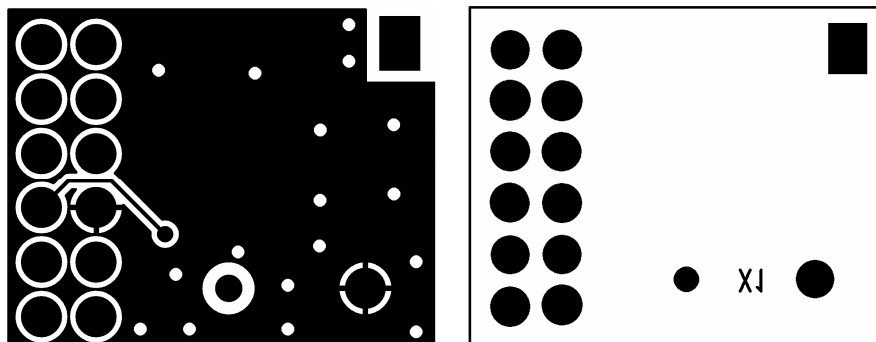


LOCATION BAND	C1	C2	L1	C3	C4
315	6PF	6PF	56nH	100nF	4.7nF
433	6PF	6PF	39nH	100nF	4.7nF
868	2.2PF	2.2PF	18nH	100nF	4.7nF
915	2.2PF	2.2PF	18nH	100nF	4.7nF

PCB layout

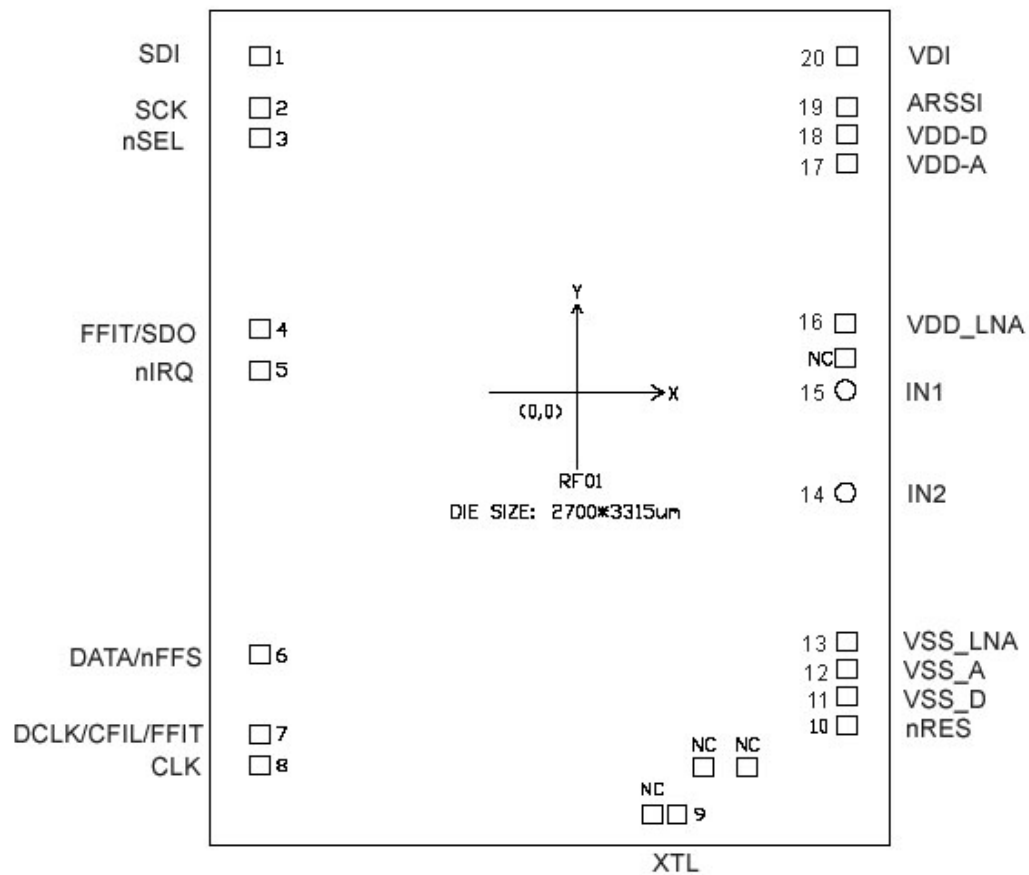


Top view



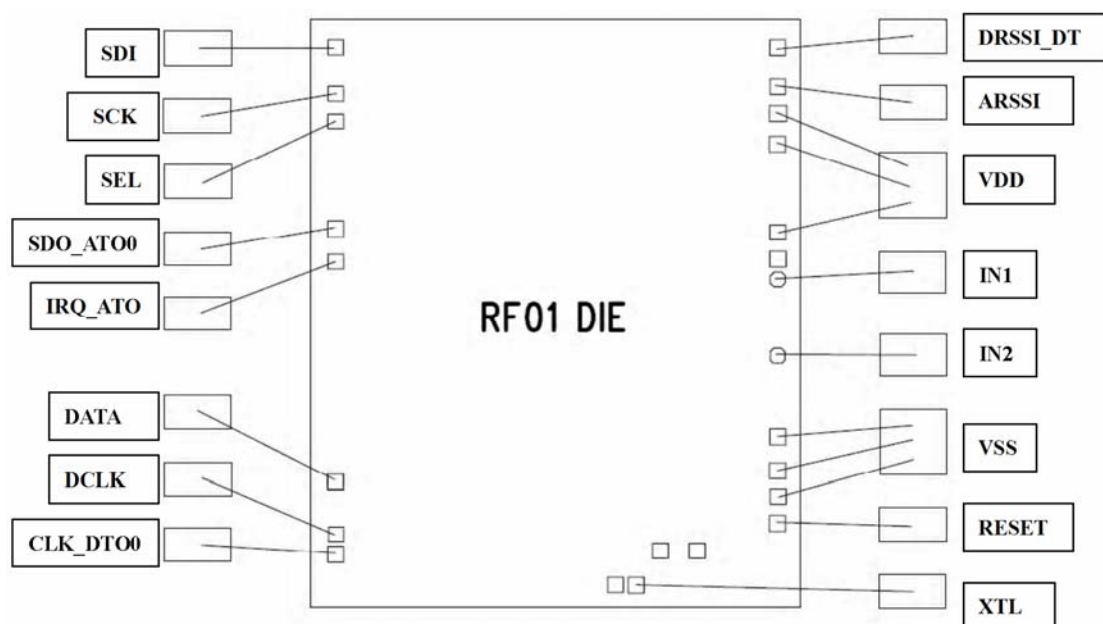
Bottom view

RF01 BONDING DIAGRAM



Pad Opening: 85 um square, except 76 um octagon pads (AN1, AN2)

Die Size: 2700 X 3315 um



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