

2.5V Drive Nch+Pch MOSFET

QS6M4

●Structure

Silicon P-channel MOSFET

Silicon N-channel MOSFET

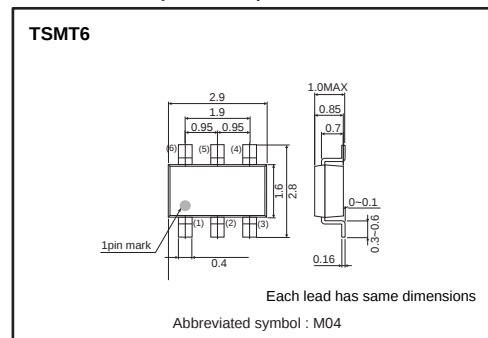
●Features

- 1) The QS6M4 combines Pch MOSFET with a Nch MOSFET in a single TSMT6 package.
- 2) Low on-state resistance with a fast switching.
- 3) Low voltage drive (2.5V).

●Applications

Load switch, inverter

●Dimensions (Unit : mm)



●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS6M4		○

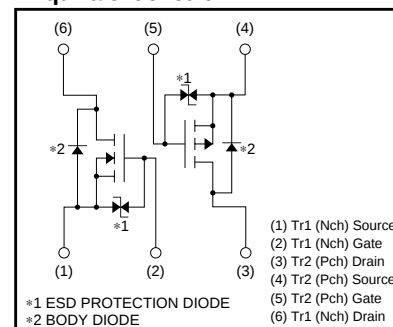
●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Nchannel	Pchannel	
Drain-source voltage	V_{DS}	30	-20	V
Gate-source voltage	V_{GS}	±12	±12	V
Drain current	Continuous	I_D	±1.5	A
	Pulsed	I_{DP}^{*1}	±6.0	A
Source current (Body diode)	Continuous	I_S	0.8	A
	Pulsed	I_{SP}^{*1}	6.0	A
Total power dissipation	P_D^{*2}	1.25		W / TOTAL
		0.9		W / ELEMENT
Channel temperature	Tch	150		°C
Storage temperature	Tstg	-55 to +150		°C

*1 $P_W \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board

●Equivalent circuit



●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th}(ch-a)^{*}$	100	°C / W / TOTAL
		139	°C / W / ELEMENT

* Mounted on a ceramic board

Transistors

●Electrical characteristics (Ta=25°C)

<Tr1. N-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	± 10	μA	$V_{GS}=\pm 12V / V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	30	—	—	V	$I_D=1mA / V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS}=30V / V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.5	—	1.5	V	$V_{DS}=10V / I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	170	230	m Ω	$I_D=1.5A / V_{GS}=4.5V$
		—	180	245		$I_D=1.5A / V_{GS}=4.0V$
		—	260	360		$I_D=1.0A / V_{GS}=2.5V$
Forward transfer admittance	$ Y_{fs} $ *	1.0	—	—	S	$V_{DS}=10V / I_D=1.0A$
Input capacitance	C_{iss}	—	80	—	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	—	25	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	—	15	—	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	7	—	ns	$I_D=1A, V_{DD} \div 15V$
Rise time	t_r *	—	18	—	ns	$V_{GS}=4.5V$
Turn-off delay time	$t_{d(off)}$ *	—	15	—	ns	$R_L=15\Omega / R_G=10\Omega$
Fall time	t_f *	—	15	—	ns	
Total gate charge	Q_g *	—	1.6	—	nC	$V_{DD} \div 15V \quad R_L=10\Omega$
Gate-source charge	Q_{gs} *	—	0.5	—	nC	$V_{GS}=4.5V \quad R_G=10\Omega$
Gate-drain charge	Q_{gd} *	—	0.9	—	nC	$I_D=1.5A$

*Pulsed

●Body diode characteristics (Source-Drain)

<Tr1. N-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	—	—	1.2	V	$I_S=3.2A / V_{GS}=0V$

*Pulsed

Transistors

●Electrical characteristics (Ta=25°C)

<Tr2. P-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 12V / V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	−20	—	—	V	$I_D = -1mA / V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	—	—	−1	μA	$V_{DS} = -20V / V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	−0.7	—	−2.0	V	$V_{DS} = -10V / I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	155	215	mΩ	$I_D = -1.5A / V_{GS} = -4.5V$
		—	170	235		$I_D = -1.5A / V_{GS} = -4.0V$
		—	310	430		$I_D = -0.75A / V_{GS} = -2.5V$
Forward transfer admittance	$ Y_{fs} $ *	1.0	—	—	S	$V_{DS} = -10V / I_D = -0.75A$
Input capacitance	C_{iss}	—	270	—	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	—	40	—	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	—	35	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	10	—	ns	$I_D = -0.75A, V_{DD} = -15V$
Rise time	t_r *	—	12	—	ns	$V_{GS} = -4.5V$
Turn-off delay time	$t_{d(off)}$ *	—	45	—	ns	$R_L = 20\Omega / R_G = 10\Omega$
Fall time	t_f *	—	20	—	ns	
Total gate charge	Q_g *	—	3.0	—	nC	$V_{DD} = -15V, R_L = 10\Omega$
Gate-source charge	Q_{gs} *	—	0.8	—	nC	$V_{GS} = -4.5V, R_G = 10\Omega$
Gate-drain charge	Q_{gd} *	—	0.85	—	nC	$I_D = -1.5A$

*Pulsed

●Body diode characteristics (Source-Drain)

<Tr2. P-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}	—	—	−1.2	V	$I_S = -0.75A / V_{GS} = 0V$

Transistors

N-ch

●Electrical characteristic curves

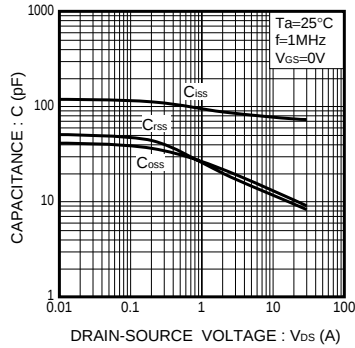


Fig.1 Typical Capacitance vs. Drain-Source Voltage

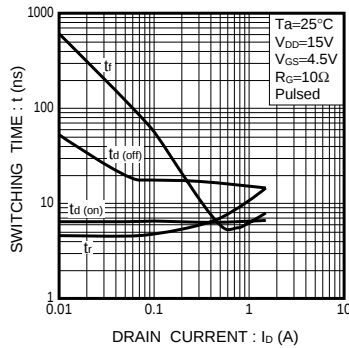


Fig.2 Switching Characteristics

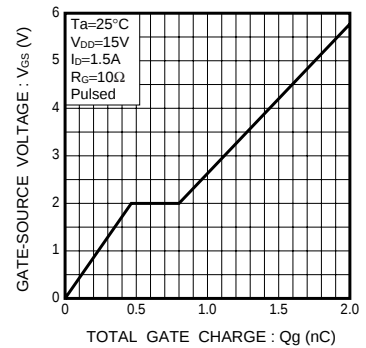


Fig.3 Dynamic Input Characteristics

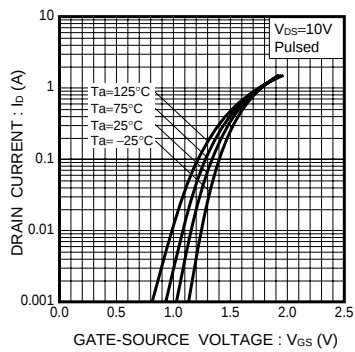


Fig.4 Typical Transfer Characteristics

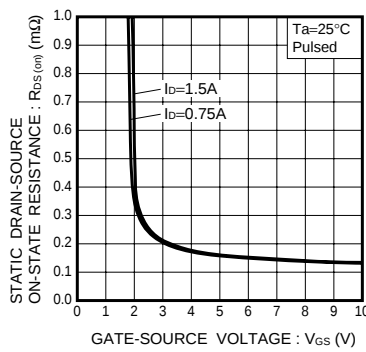


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

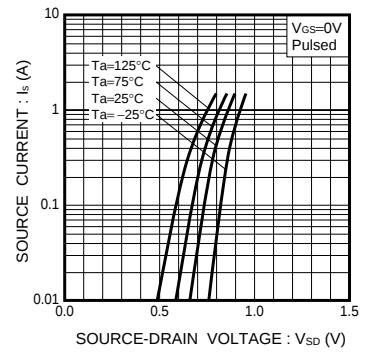


Fig.6 Source Current vs. Source-Drain Voltage

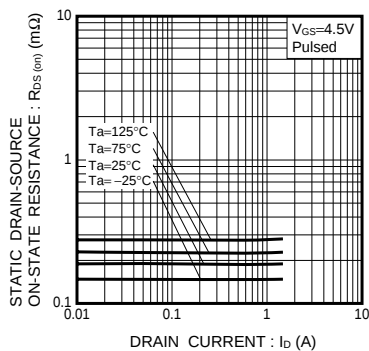


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

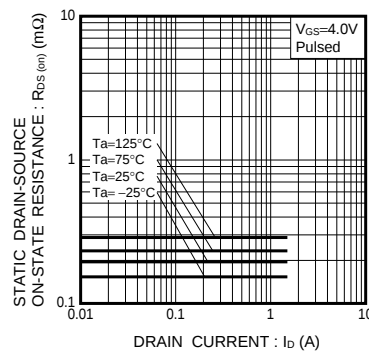


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

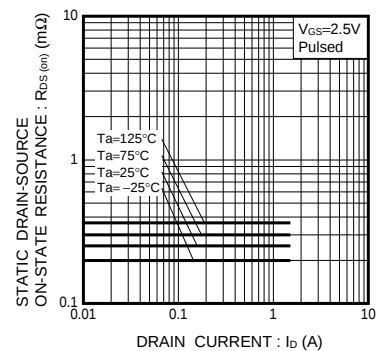


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

Transistors

P-ch

●Electrical characteristic curves

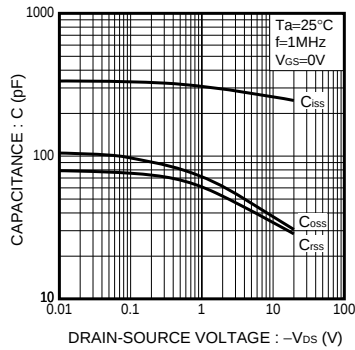


Fig.1 Typical Capacitance vs. Drain-Source Voltage

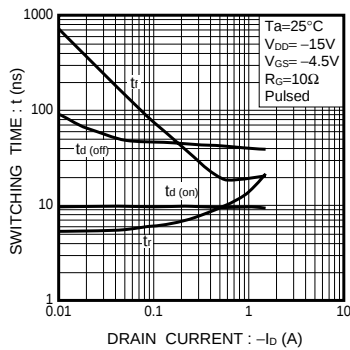


Fig.2 Switching Characteristics

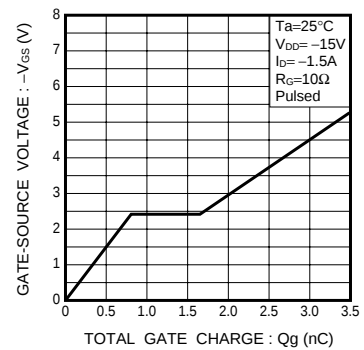


Fig.3 Dynamic Input Characteristics

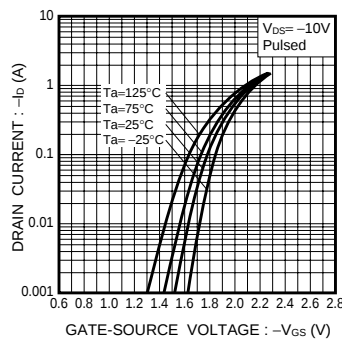


Fig.4 Typical Transfer Characteristics

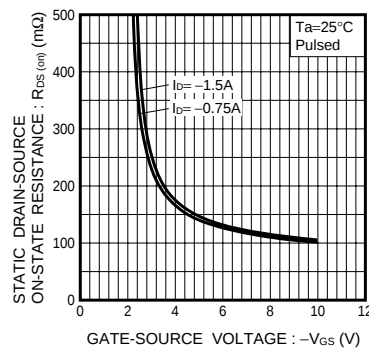


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

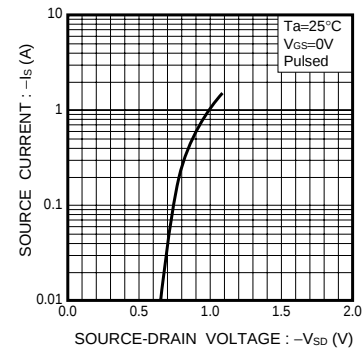


Fig.6 Source Current vs. Source-Drain Voltage

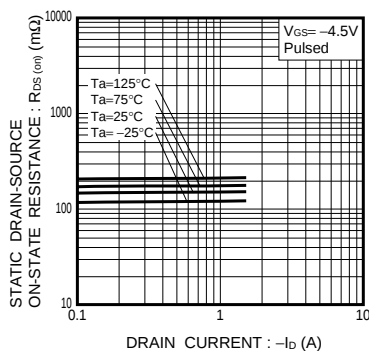


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

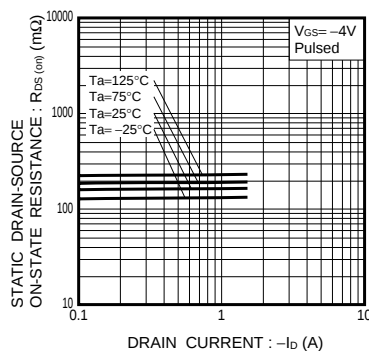


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

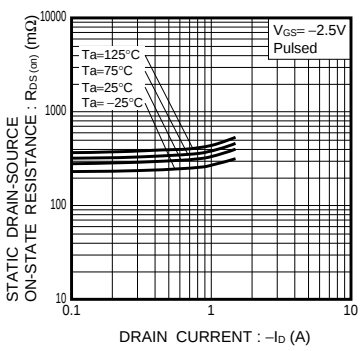


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

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