REJ09B0244-0300

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16

R8C/24 Group, R8C/25 Group
Hardware Manual

RENESAS 16-BIT SINGLE-CHIP MCU
R8C FAMILY / R8C/2x SERIES

Hardware Manual

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the R8C/24 Group, R8C/25 Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Technology Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	R8C/24 Group, R8C/25 Group Datasheet	REJ03B0117
Hardware manual	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	R8C/24 Group, R8C/25 Group Hardware Manual	This hardware manual
Software manual	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Technology Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

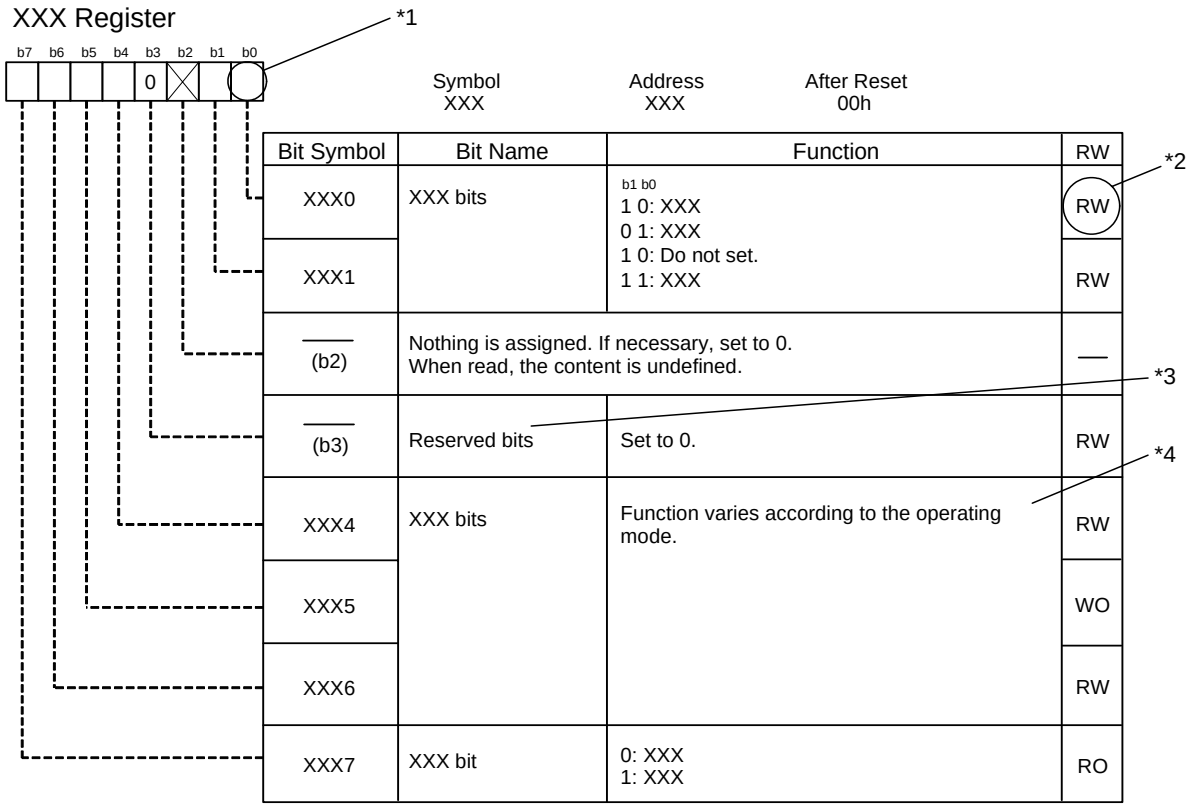
(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.



*1

Blank: Set to 0 or 1 according to the application.
0: Set to 0.
1: Set to 1.
X: Nothing is assigned.

*2

RW: Read and write.
RO: Read only.
WO: Write only.
–: Nothing is assigned.

*3

- Reserved bit
  Reserved bit. Set to specified value.

*4

- Nothing is assigned
  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value
  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.
  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Registers
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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SFR Page Reference

Address	Register	Symbol	Page
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	71
0005h	Processor Mode Register 1	PM1	71
0006h	System Clock Control Register 0	CM0	75
0007h	System Clock Control Register 1	CM1	76
0008h			
0009h			
000Ah	Protect Register	PRCR	100
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	77
000Dh	Watchdog Timer Reset Register	WDTR	129
000Eh	Watchdog Timer Start Register	WDTS	129
000Fh	Watchdog Timer Control Register	WDC	128
0010h	Address Match Interrupt Register 0	RMAD0	121
0011h			
0012h			
0013h	Address Match Interrupt Enable Register	AIER	121
0014h	Address Match Interrupt Register 1	RMAD1	121
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	129
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	78
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	78
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	79
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	80
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	79
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	79
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	79
0030h			
0031h	Voltage Detection Register 1	VCA1	36
0032h	Voltage Detection Register 2	VCA2	36, 80
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register	VW1C	38
0037h	Voltage Monitor 2 Circuit Control Register	VW2C	39
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0039h			
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003Bh			
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003Dh			
003Eh			
003Fh			

Address	Register	Symbol	Page
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	107
0049h	Timer RD1 Interrupt Control Register	TRD1IC	107
004Ah	Timer RE Interrupt Control Register	TREIC	106
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	106
004Eh	A/D Conversion Interrupt Control Register	ADIC	106
004Fh	SSU/IIC Interrupt Control Register	SSUIC/IICIC	107
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	106
0052h	UART0 Receive Interrupt Control Register	S0RIC	106
0053h	UART1 Transmit Interrupt Control Register	S1TIC	106
0054h	UART1 Receive Interrupt Control Register	S1RIC	106
0055h	INT2 Interrupt Control Register	INT2IC	108
0056h	Timer RA Interrupt Control Register	TRAIC	106
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	106
0059h	INT1 Interrupt Control Register	INT1IC	108
005Ah	INT3 Interrupt Control Register	INT3IC	108
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	108
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
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0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
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009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	291
00A1h	UART0 Bit Rate Register	U0BRG	291
00A2h	UART0 Transmit Buffer Register	U0TB	290
00A3h			
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	292
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	293
00A6h	UART0 Receive Buffer Register	U0RB	290
00A7h			
00A8h	UART1 Transmit/Receive Mode Register	U1MR	291
00A9h	UART1 Bit Rate Register	U1BRG	291
00AAh	UART1 Transmit Buffer Register	U1TB	290
00ABh			
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	292
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00AFh			
00B0h			
00B1h			
00B2h			
00B3h			
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00FAh	INT Input Filter Select Register	INTF	116
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00FDh	Pull-Up Control Register 1	PUR1	57
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00FFh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

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0100h	Timer RA Control Register	TRACR	135
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0130h			
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0146h	Timer RD Counter 0	TRD0	192, 207, 222, 233, 245, 258
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0150h	Timer RD Control Register 1	TRDCR1	188, 203, 219, 242
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015Eh	Timer RD General Register D1	TRDGRD1	193, 208, 223, 234, 245, 259
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0161h			
0162h			
0163h			
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0165h			
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0170h			
0171h			
0172h			
0173h			
0174h			
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01BDh			
01BEh			

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NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and are packaged in a 52-pin molded-plastic LQFP or a 64-pin molded-plastic FLGA. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.
Furthermore, the R8C/25 Group has on-chip data flash (1 KB x 2 blocks).
The difference between the R8C/24 Group and R8C/25 Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, etc.

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/24 Group and Table 1.2 outlines the Functions and Specifications for R8C/25 Group.

Table 1.1 Functions and Specifications for R8C/24 Group

Item			Specification
CPU	Number of fundamental instructions		89 instructions
	Minimum instruction execution time		50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)
	Operating mode		Single-chip
	Address space		1 Mbyte
	Memory capacity		Refer to **Table 1.3 Product Information for R8C/24 Group**
Peripheral Functions	Ports		I/O ports: 41 pins, Input port: 3 pins
	LED drive ports		I/O ports: 8 pins
	Timers		Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits × 2 channels (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function
	Serial interfaces		2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface		1 channel I²C bus Interface(1) Clock synchronous serial I/O with chip select
	LIN module		Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter		10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer		15 bits × 1 channel (with prescaler) Reset start selectable
	Interrupts		Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority levels: 7 levels
	Clock	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz)
			Real-time clock (timer RE)
	Oscillation stop detection function		XIN clock oscillation stop detection function
	Voltage detection circuit		On-chip
	Power-on reset circuit		On-chip
Electrical Characteristics	Supply voltage		VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz)
	Current consumption		Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 µA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 µA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage		VCC = 2.7 to 5.5 V
	Programming and erasure endurance		100 times
Operating Ambient Temperature			-20 to 85°C (N version)
			-40 to 85°C (D version)(2)
			-20 to 105°C (Y version)(3)
Package			52-pin molded-plastic LQFP
			64-pin molded-plastic FLGA

NOTES:
1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

Table 1.2 Functions and Specifications for R8C/25 Group

Item			Specification
CPU	Number of fundamental instructions		89 instructions
	Minimum instruction execution time		50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V)
	Operating mode		Single-chip
	Address space		1 Mbyte
	Memory capacity		Refer to **Table 1.4 Product Information for R8C/25 Group**
Peripheral Functions	Ports		I/O ports: 41 pins, Input port: 3 pins
	LED drive ports		I/O ports: 8 pins
	Timers		Timer RA: 8 bits × 1 channel Timer RB: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits × 2 channels (Input capture and output compare circuits) Timer RE: With real-time clock and compare match function
	Serial interface		2 channels (UART0, UART1) Clock synchronous serial I/O, UART
	Clock synchronous serial interface		1 channel I2C bus Interface(1) Clock synchronous serial I/O with chip select
	LIN module		Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter		10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer		15 bits × 1 channel (with prescaler) Reset start selectable
	Interrupts		Internal: 11 sources, External: 5 sources, Software: 4 sources, Priority levels: 7 levels
	Clock	Clock generation circuits	3 circuits • XIN clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has a frequency adjustment function • XCIN clock generation circuit (32 kHz)
			Real-time clock (timer RE)
	Oscillation stop detection function		XIN clock oscillation stop detection function
	Voltage detection circuit		On-chip
	Power-on reset circuit		On-chip
Electrical Characteristics	Supply voltage		VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz) VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz)
	Current consumption		Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 2.0 µA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz) Typ. 0.7 µA (VCC = 3.0 V, stop mode)
Flash memory	Programming and erasure voltage		VCC = 2.7 to 5.5 V
	Programming and erasure endurance		1,0000 times (data flash)
			1,000 times (program ROM)
Operating Ambient Temperature			-20 to 85°C (N version)
			-40 to 85°C (D version)(2)
			-20 to 105°C (Y version)(3)
Package			52-pin molded-plastic LQFP
			64-pin molded-plastic FLGA

NOTES:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

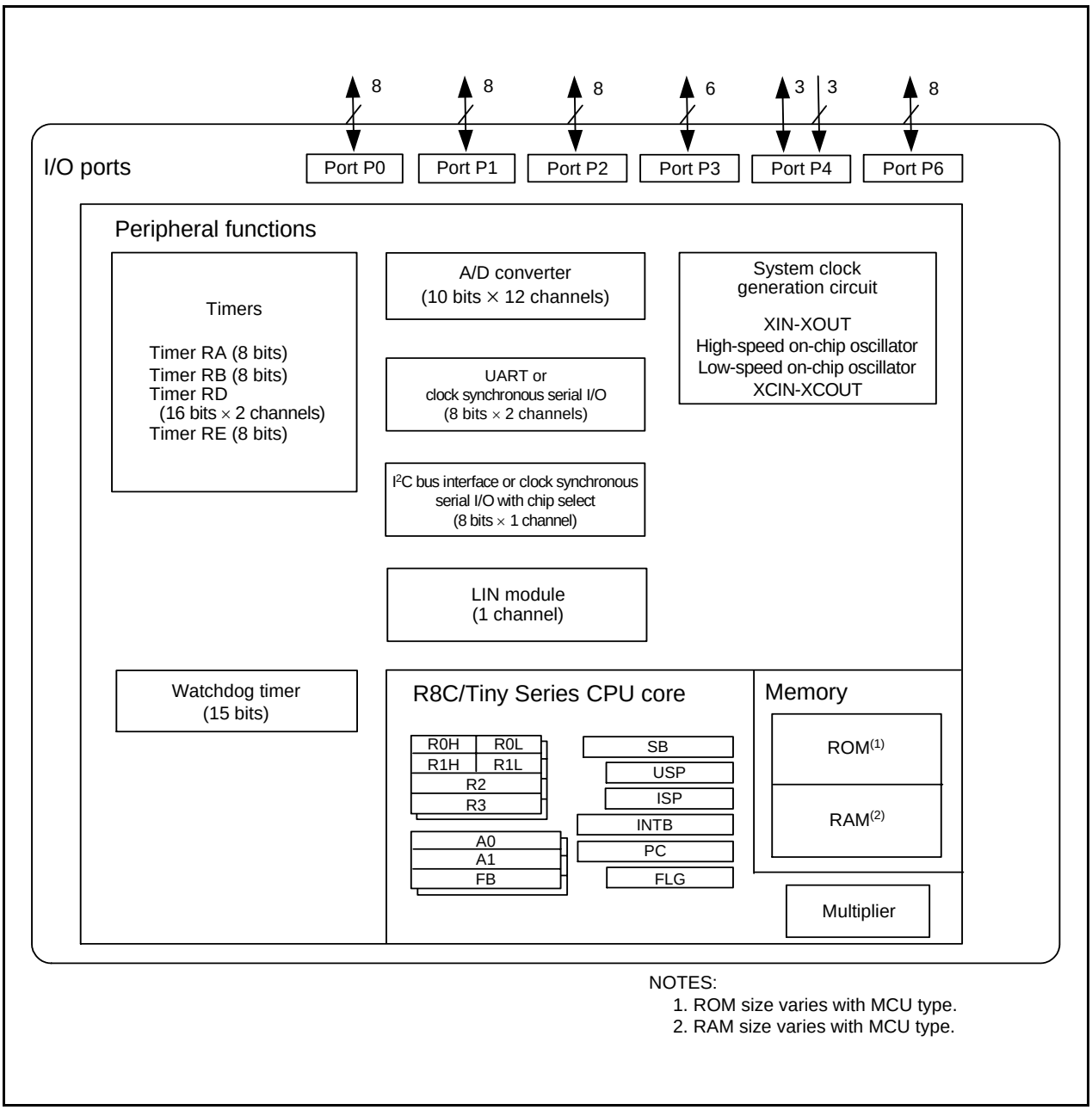


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information for R8C/24 Group and Table 1.4 lists the Product Information for R8C/25 Group.

Table 1.3 Product Information for R8C/24 Group **Current of Feb. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F21244SNFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Blank product
R5F21245SNFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	
R5F21244SDFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	D version Blank product
R5F21245SDFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	N version Factory programming product(1)
R5F21245SNXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SNXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SNXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SNXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	
R5F21244SNXXXLG	16 Kbytes	1 Kbyte	PTLG0064JA-A	
R5F21246SNXXXLG	32 Kbytes	2 Kbytes	PTLG0064JA-A	
R5F21244SDXXXFP	16 Kbytes	1 Kbyte	PLQP0052JA-A	D version Factory programming product(1)
R5F21245SDXXXFP	24 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21246SDXXXFP	32 Kbytes	2 Kbytes	PLQP0052JA-A	
R5F21247SDXXXFP	48 Kbytes	2.5 Kbytes	PLQP0052JA-A	
R5F21248SDXXXFP	64 Kbytes	3 Kbytes	PLQP0052JA-A	

NOTE:
1. The user ROM is programmed before shipment.

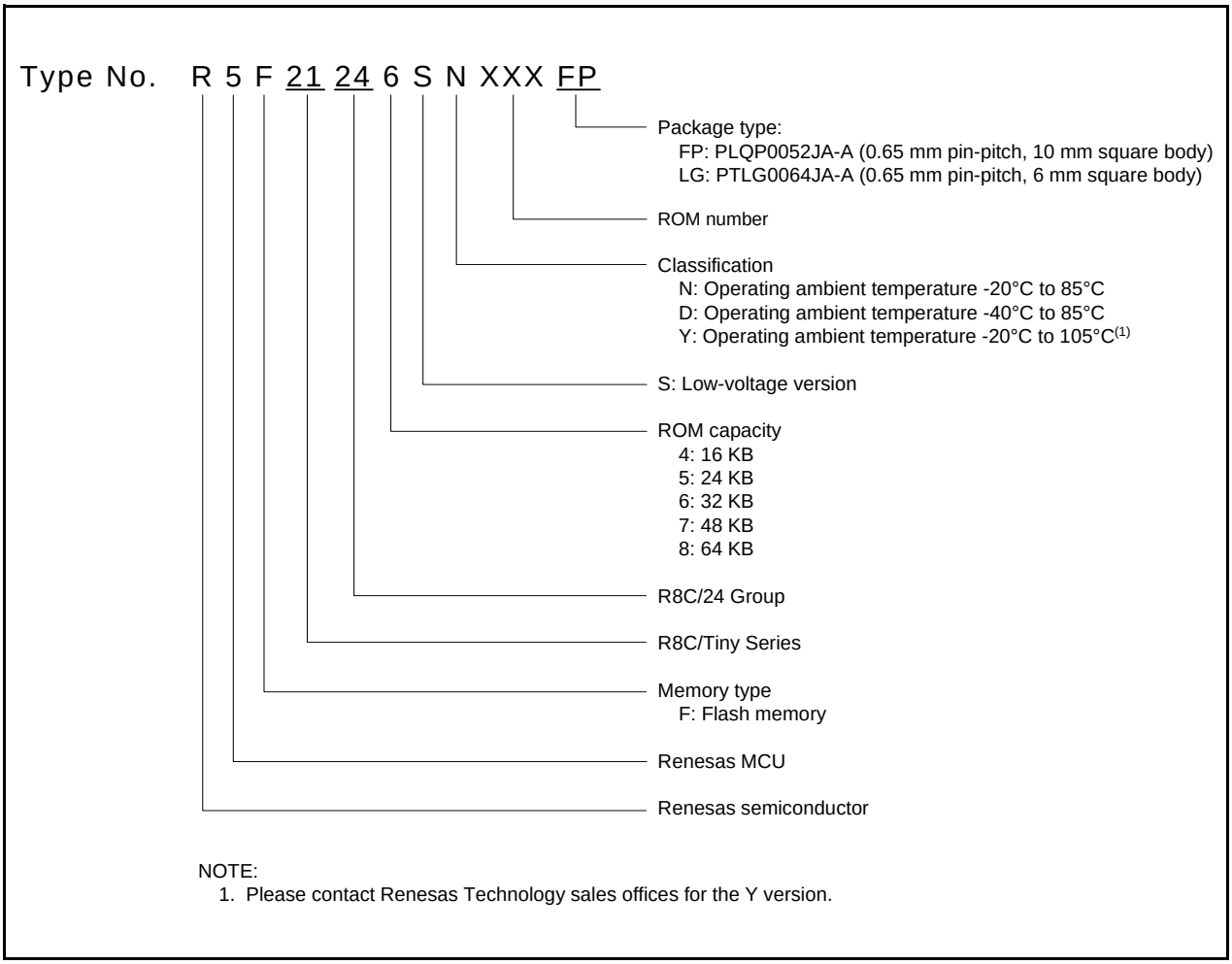


Figure 1.2 Type Number, Memory Size, and Package of R8C/24 Group

Table 1.4 Product Information for R8C/25 Group Current of Feb. 2008

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21254SNFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	N version Blank product
R5F21255SNFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SNFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SNFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SNFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNLG	16 Kbytes	1 Kbyte × 2	1 Kbyte	PTLG0064JA-A	
R5F21256SNLG	32 Kbytes	1 Kbyte × 2	2 Kbytes	PTLG0064JA-A	
R5F21254SDFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	D version Blank product
R5F21255SDFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SDFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SDFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SDFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	N version Factory programming product(1)
R5F21255SNXXXFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SNXXXFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SNXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SNXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	
R5F21254SNXXXLG	16 Kbytes	1 Kbyte × 2	1 Kbyte	PTLG0064JA-A	
R5F21256SNXXXLG	32 Kbytes	1 Kbyte × 2	2 Kbytes	PTLG0064JA-A	
R5F21254SDXXXFP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLQP0052JA-A	D version Factory programming product(1)
R5F21255SDXXXFP	24 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21256SDXXXFP	32 Kbytes	1 Kbyte × 2	2 Kbytes	PLQP0052JA-A	
R5F21257SDXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0052JA-A	
R5F21258SDXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0052JA-A	

NOTE:
1. The user ROM is programmed before shipment.

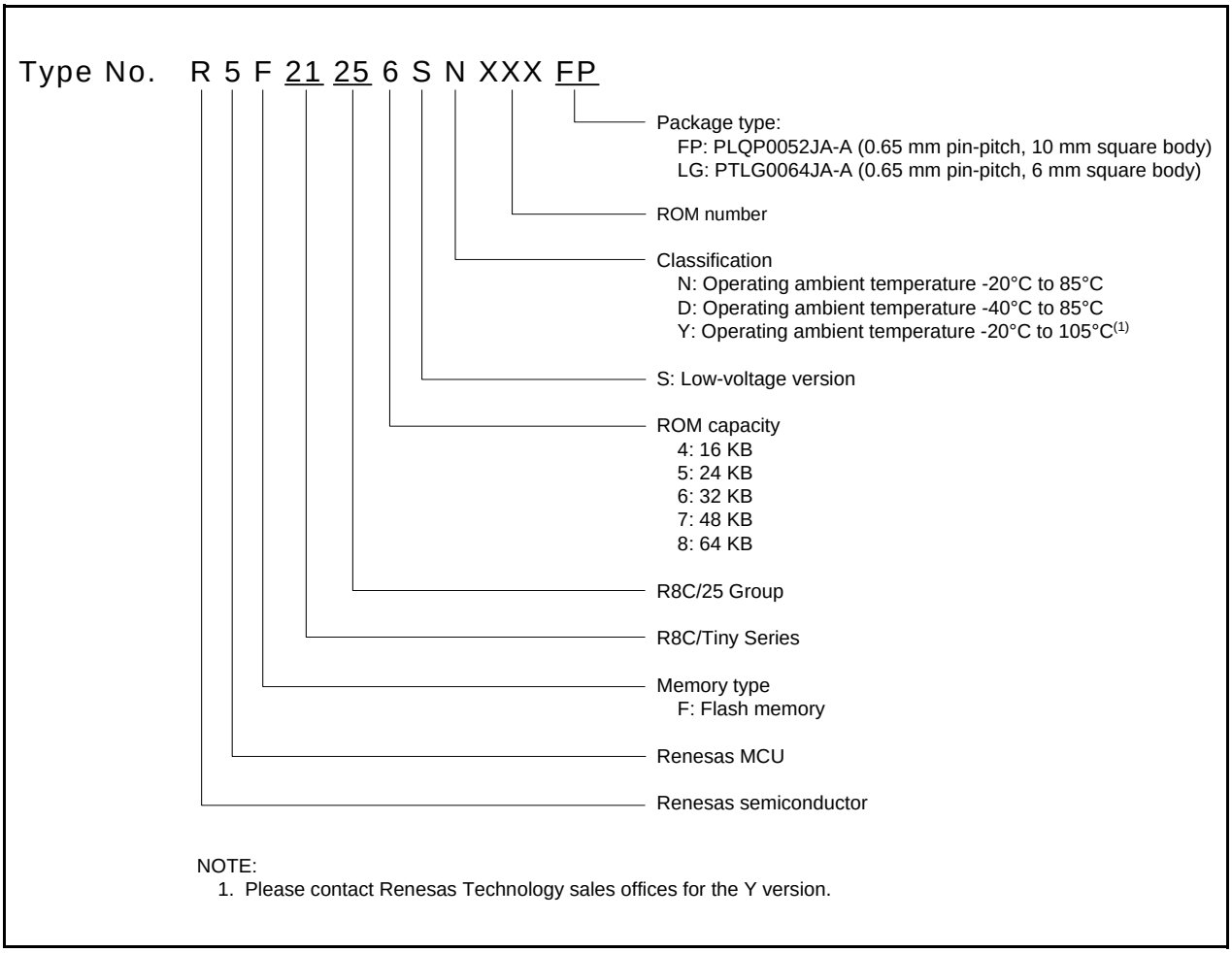
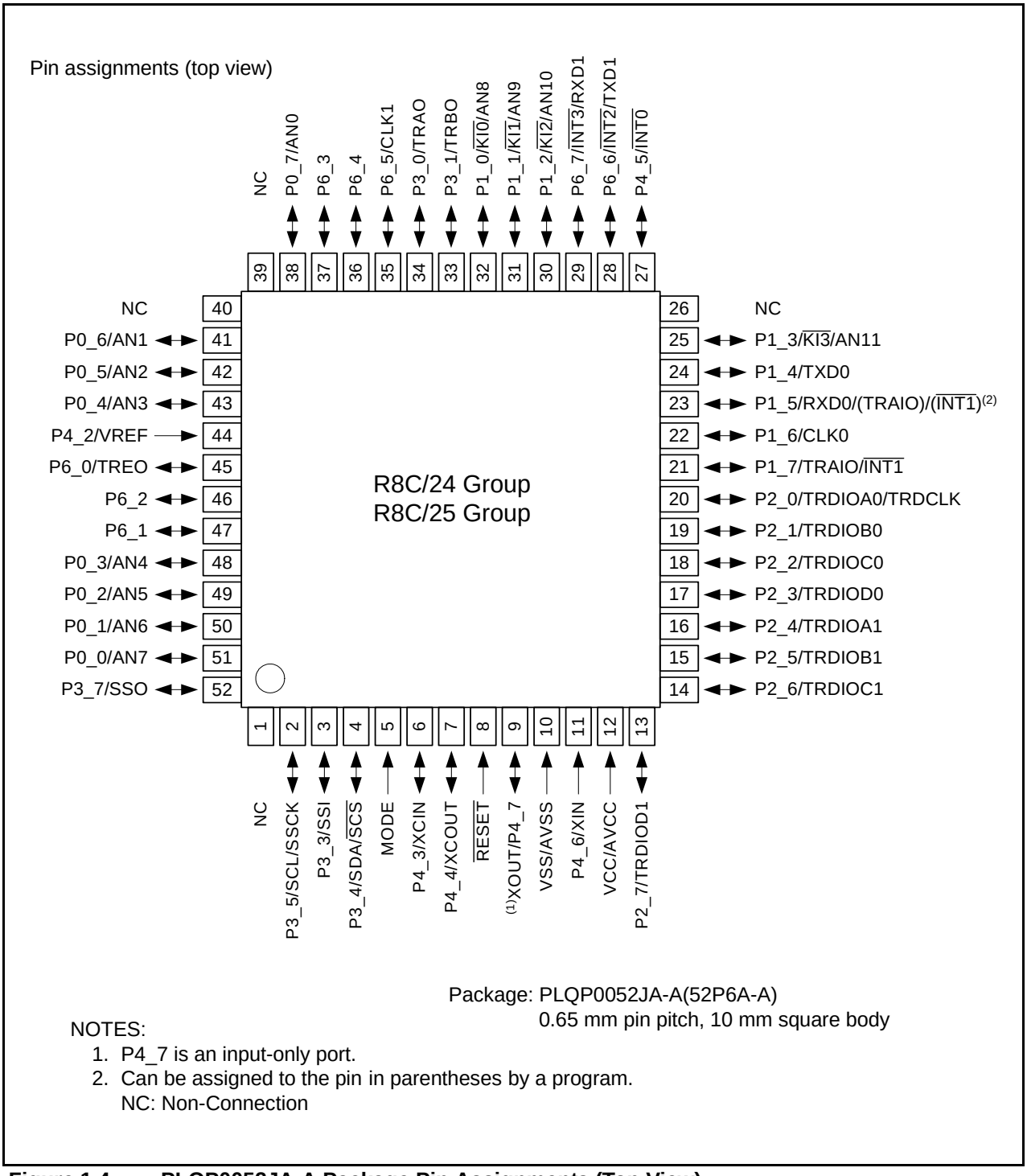


Figure 1.3 Type Number, Memory Size, and Package of R8C/25 Group

1.5 Pin Assignments

Figure 1.4 shows PLQP0052JA-A Package Pin Assignments (Top View). Figure 1.5 shows PTLG0064JA-A Package Pin Assignments.



Package: PLQP0052JA-A(52P6A-A)
0.65 mm pin pitch, 10 mm square body

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
   NC: Non-Connection

Figure 1.4 PLQP0052JA-A Package Pin Assignments (Top View)

Pin assignments (top perspective view)

	A	B	C	D	E	F	G	H	
8	3 P3_3/SSI	50 P0_1/AN6	48 P0_3/AN4	46 P6_2	45 P6_0/TREO	NC	36 P6_4	NC	8
7	4 P3_4/SDA/$\overline{\text{SCS}}$	51 P0_0/AN7	49 P0_2/AN5	NC	44 P4_2/VREF	34 P3_0/TRAO	35 P6_5/CLK1	NC	7
6	NC	5 MODE	52 P3_7/SSO	47 P6_1	43 P0_4/AN3	42 P0_5/AN2	NC	33 P3_1/TRBO	6
5	7 P4_4/XCOUT	NC	6 P4_3/XCIN	2 P3_5/SCL/SSCK	37 P6_3	NC	41 P0_6/AN1	38 P0_7/AN0	5
4	13 P2_7/TRDIOD1	12 VCC/AVCC	NC	9 XOUT/P4_7(1)	8 $\overline{\text{RESET}}$	32 P1_0/$\overline{\text{KI0}}$/AN8	31 P1_1/$\overline{\text{KI1}}$/AN9	NC	4
3	NC	10 VSS/AVSS	16 P2_4/TRDIOA1	19 P2_1/TRDIOB0	23 P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$)(2)	NC	NC	30 P1_2/$\overline{\text{KI2}}$/AN10	3
2	NC	11 XIN/P4_6	17 P2_3/TRDIOD0	20 P2_0/TRDIOA0/TRDCLK	NC	24 P1_4/TXD0	28 P6_6/$\overline{\text{INT2}}$/TXD1	NC	2
1	14 P2_6/TRDIOC1	15 P2_5/TRDIOB1	18 P2_2/TRDIOC0	21 P1_7/TRAIO/$\overline{\text{INT1}}$	22 P1_6/CLK0	25 P1_3/$\overline{\text{KI3}}$/AN11	27 P4_5/$\overline{\text{INT0}}$	29 P6_7/$\overline{\text{INT3}}$/RXD1	1
	A	B	C	D	E	F	G	H	

Package: PTLG0064JA-A(64F0G)
0.65 mm pin pitch, 6 mm square body

NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. In the figure, the numbers in circles are the pin numbers of the 52-pin LQFP package (PLQP0052JA-A).
   NC: Non-Connection

R5F21244S
NLG
JAPAN

Pin assignments (top view)

Figure 1.5 PTLG0064JA-A Package Pin Assignments

1.6 Pin Functions

Table 1.5 lists Pin Functions.

Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power supply input	VCC, VSS	I	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins. To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RD input pin. $\overline{\text{INT1}}$ is timer RA input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O ports
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Serial interface	CLK0, CLK1	I/O	Transfer clock I/O pin
	RXD0, RXD1	I	Serial data input pins
	TXD0, TXD1	O	Serial data output pins
I^2C bus interface	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
Clock synchronous serial I/O with chip select	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6_0 to P6_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

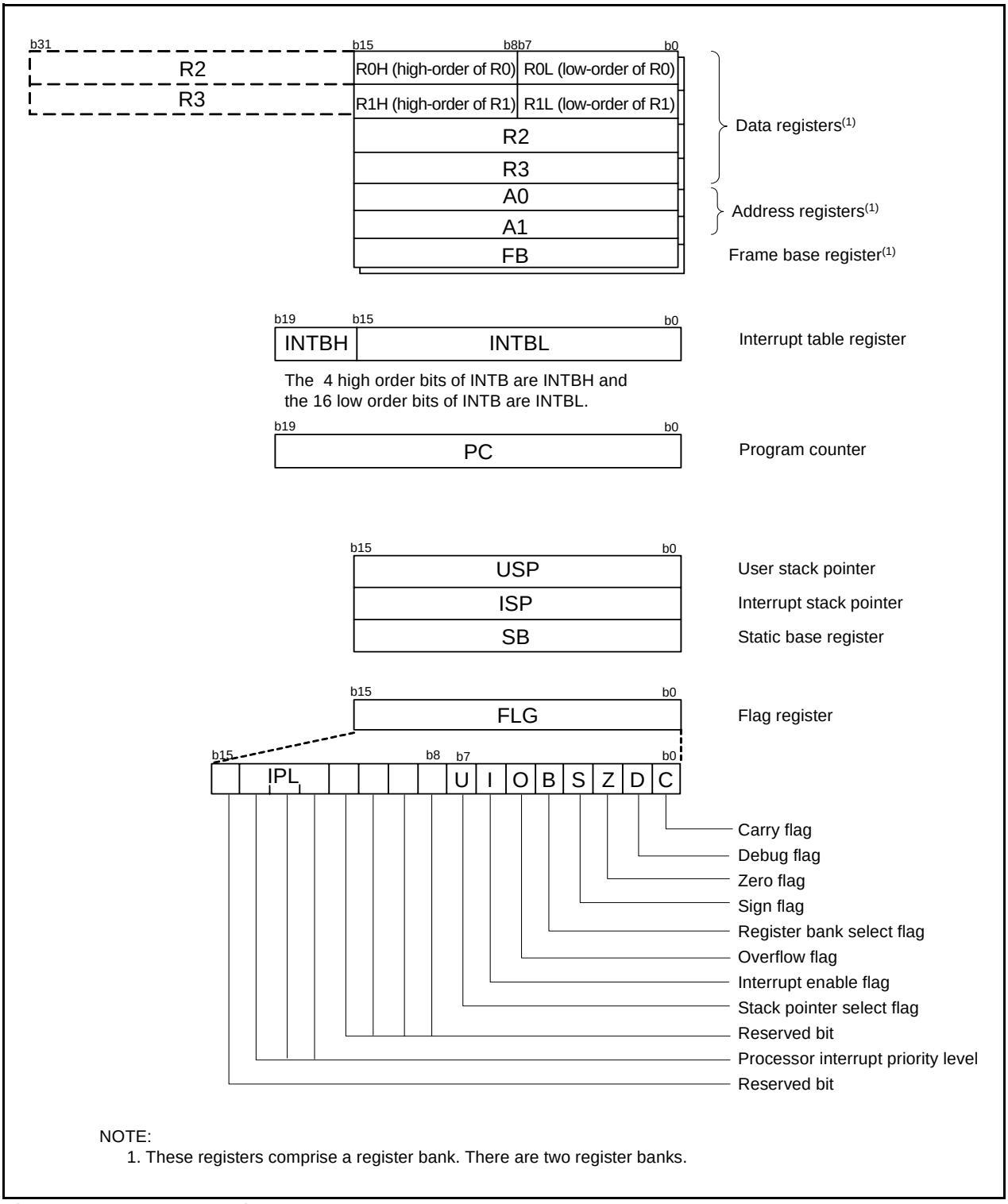
Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I^2C bus Interface	A/D Converter
2		P3_5				SSCK	SCL	
3		P3_3				SSI		
4		P3_4				$\overline{SCS}$	$\overline{SDA}$	
5	MODE							
6	XCIN	P4_3						
7	XCOUT	P4_4						
8	$\overline{RESET}$							
9	XOUT	P4_7						
10	VSS/AVSS							
11	XIN	P4_6						
12	VCC/AVCC							
13		P2_7		TRDIOD1				
14		P2_6		TRDIOC1				
15		P2_5		TRDIOB1				
16		P2_4		TRDIOA1				
17		P2_3		TRDIOD0				
18		P2_2		TRDIOC0				
19		P2_1		TRDIOB0				
20		P2_0		TRDIOA0/TRDCLK				
21		P1_7	$\overline{INT1}$	TRAIO				
22		P1_6			CLK0			
23		P1_5	$\overline{(INT1)}$(1)	(TRAIO)(1)	RXD0			
24		P1_4			TXD0			
25		P1_3	$\overline{KI3}$					AN11
27		P4_5	$\overline{INT0}$	$\overline{INT0}$				
28		P6_6	$\overline{INT2}$		TXD1			
29		P6_7	$\overline{INT3}$		RXD1			
30		P1_2	$\overline{KI2}$					AN10
31		P1_1	$\overline{KI1}$					AN9
32		P1_0	$\overline{KI0}$					AN8
33		P3_1		TRBO				
34		P3_0		TRAO				
35		P6_5			CLK1			
36		P6_4						
37		P6_3						
38		P0_7						AN0
41		P0_6						AN1
42		P0_5						AN2
43		P0_4						AN3
44	VREF	P4_2						
45		P6_0		TREO				
46		P6_2						
47		P6_1						
48		P0_3						AN4
49		P0_2						AN5
50		P0_1						AN6
51		P0_0						AN7
52		P3_7				SSO		

NOTE:
1. Can be assigned to the pin in parentheses by a program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



NOTE:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

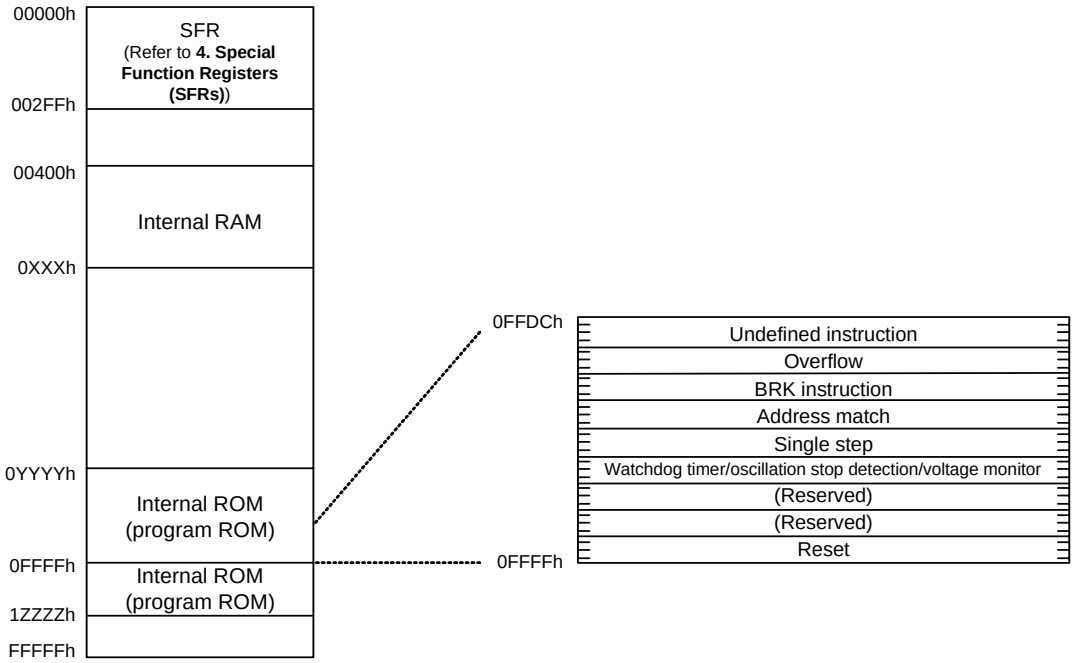
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/24 Group

Figure 3.1 is a Memory Map of R8C/24 Group. The R8C/24 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM area is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



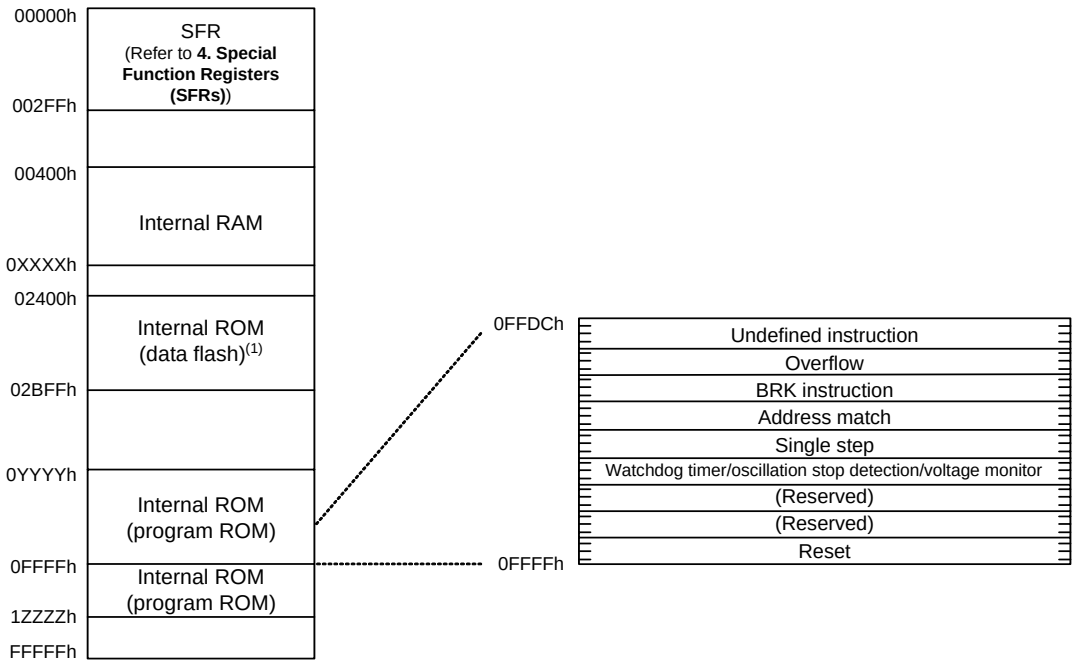
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address 1ZZZZh	Size	Address 0XXXXh
R5F21244SNFP, R5F21244SNXXXFP, R5F21244SDFP, R5F21244SDXXXFP, R5F21244SNLG, R5F21244SNXXXLG	16 Kbytes	0C000h	–	1 Kbyte	007FFh
R5F21245SNFP, R5F21245SNXXXFP, R5F21245SDFP, R5F21245SDXXXFP	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F21246SNFP, R5F21246SNXXXFP, R5F21246SDFP, R5F21246SDXXXFP, R5F21246SNLG, R5F21246SNXXXLG	32 Kbytes	08000h	–	2 Kbytes	00BFFh
R5F21247SNFP, R5F21247SNXXXFP, R5F21247SDFP, R5F21247SDXXXFP	48 Kbytes	04000h	–	2.5 Kbytes	00DFFh
R5F21248SNFP, R5F21248SNXXXFP, R5F21248SDFP, R5F21248SDXXXFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh

Figure 3.1 Memory Map of R8C/24 Group

3.2 R8C/25 Group

Figure 3.2 is a Memory Map of R8C/25 Group. The R8C/25 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 2-Kbyte internal RAM is allocated addresses 00400h to 00BFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address 1ZZZZh	Size	Address 0XXXXh
R5F21254SNFP, R5F21254SNXXXFP, R5F21254SDFP, R5F21254SDXXXFP, R5F21254SNLG, R5F21254SNXXXLG	16 Kbytes	0C000h	–	1 Kbyte	007FFh
R5F21255SNFP, R5F21255SNXXXFP, R5F21255SDFP, R5F21255SDXXXFP	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F21256SNFP, R5F21256SNXXXFP, R5F21256SDFP, R5F21256SDXXXFP, R5F21256SNLG, R5F21256SNXXXLG	32 Kbytes	08000h	–	2 Kbytes	00BFFh
R5F21257SNFP, R5F21257SNXXXFP, R5F21257SDFP, R5F21257SDXXXFP	48 Kbytes	04000h	–	2.5 Kbytes	00DFFh
R5F21258SNFP, R5F21258SNXXXFP, R5F21258SDFP, R5F21258SDXXXFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh

Figure 3.2 Memory Map of R8C/25 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b[6]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[2]	VCA2	00h[3] 00100000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register[5]	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register[5]	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register[2]	VW0C	0000X000b[3] 0100X001b[4]
0039h			
003Ah			
003Eh			
003Fh			

X: Undefined

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset or the LVD0ON bit in the OFS register is set to 0, and hardware reset.
5. Software reset, watchdog timer reset, and voltage monitor 1 reset or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

Table 4.2 SFR Information (2)[1]

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC Interrupt Control Register[2]	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.3 SFR Information (3)[1]

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H / IIC bus Control Register 1[2]	SSCRH / ICCR1	00h
00B9h	SS Control Register L / IIC bus Control Register 2[2]	SSCRL / ICCR2	01111101b
00BAh	SS Mode Register / IIC bus Mode Register[2]	SSMR / ICMR	00011000b
00BBh	SS Enable Register / IIC bus Interrupt Enable Register[2]	SSER / ICIER	00h
00BCh	SS Status Register / IIC bus Status Register[2]	SSSR / ICSR	00h / 0000X000b
00BDh	SS Mode Register 2 / Slave Address Register[2]	SSMR2 / SAR	00h
00BEh	SS Transmit Data Register / IIC bus Transmit Data Register[2]	SSTDR / ICDRT	FFh
00BFh	SS Receive Data Register / IIC bus Receive Data Register[2]	SSRDR / ICDRR	FFh

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.4 SFR Information (4)[1]

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P2 Drive Capacity Control Register	P2DRR	00h
00F5h	UART1 Function Select Register	U1SR	XXh
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX00XX00b
00FEh			
00FFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)[1]

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)(1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)(1)

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Resets

The following resets are implemented: hardware reset, power-on reset, voltage monitor 0 reset, voltage monitor 1 reset, voltage monitor 2 reset, watchdog timer reset, and software reset.
Table 5.1 lists the Reset Names and Sources.

Table 5.1 Reset Names and Sources

Reset Name	Source
Hardware reset	Input voltage of $\overline{\text{RESET}}$ pin is held “L”
Power-on reset	VCC rises
Voltage monitor 0 reset	VCC falls (monitor voltage: Vdet0)
Voltage monitor 1 reset	VCC falls (monitor voltage: Vdet1)
Voltage monitor 2 reset	VCC falls (monitor voltage: Vdet2)
Watchdog timer reset	Underflow of watchdog timer
Software reset	Write 1 to PM03 bit in PM0 register

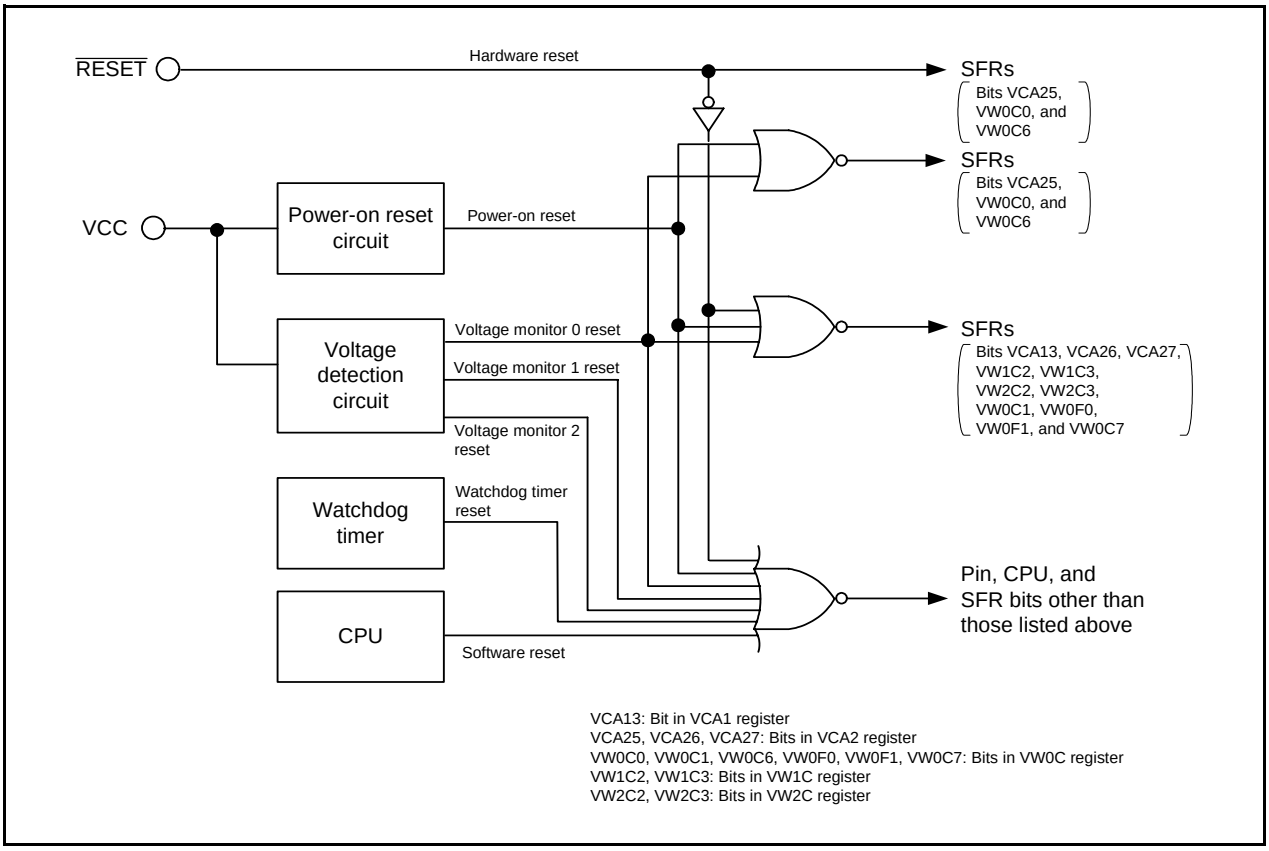


Figure 5.1 Block Diagram of Reset Circuit

Table 5.2 shows the Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”, Figure 5.2 shows the CPU Register Status after Reset, Figure 5.3 shows the Reset Sequence, and Figure 5.4 shows the OFS Register.

Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”

Pin Name	Pin Functions
P0, P1, P2	Input port
P3_0, P3_1, P3_3 to P3_5, P3_7	Input port
P4_2 to P4_7	Input port
P6	Input port

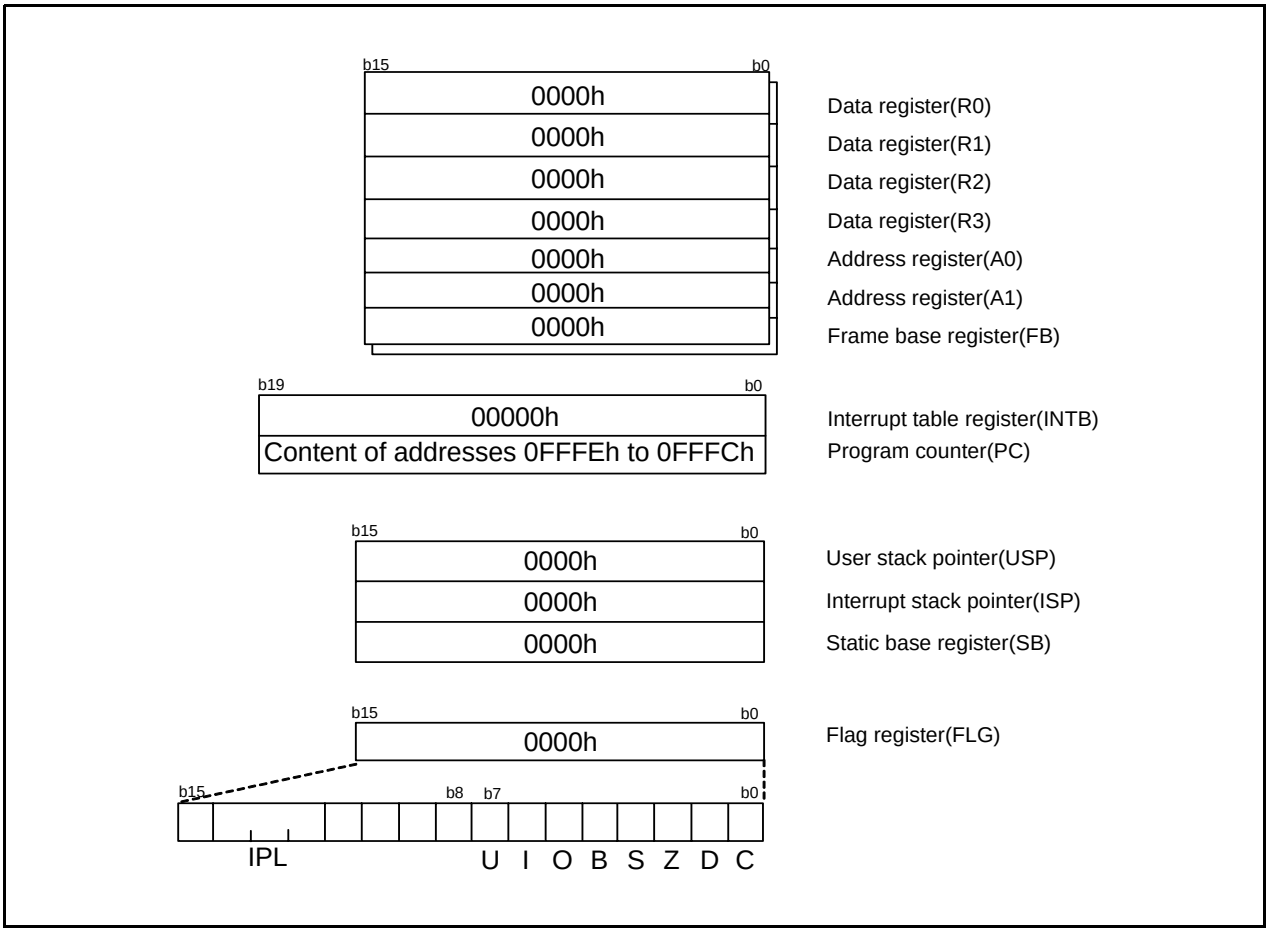
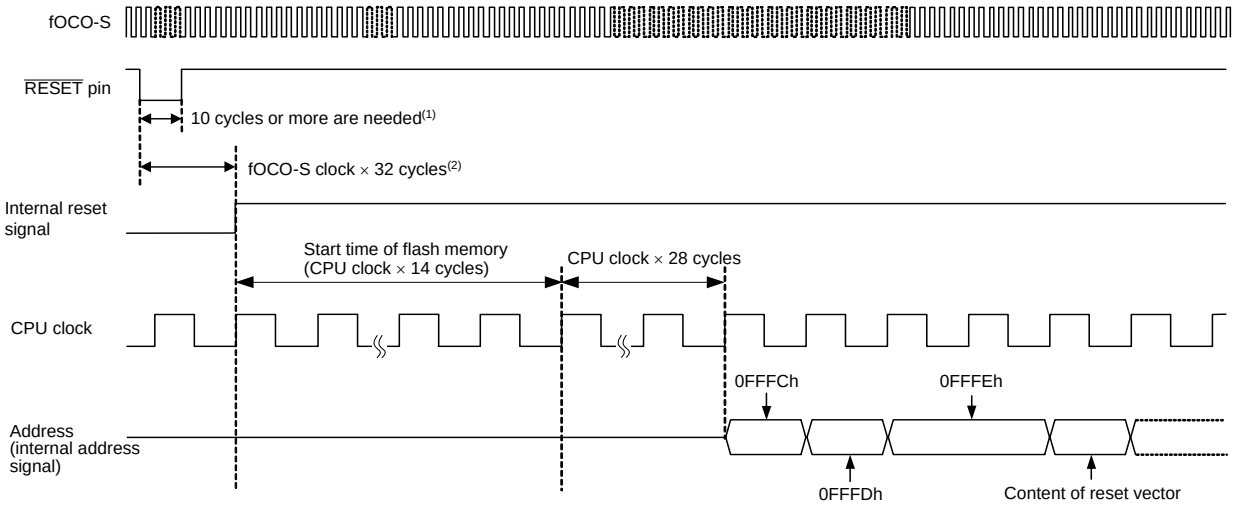


Figure 5.2 CPU Register Status after Reset



NOTES:
1. Hardware reset.
2. When the "L" input width to the RESET pin is set to fOCO-S clock × 32 cycles or more, setting the RESET pin to "H" also sets the internal reset signal to "H" at the same.

Figure 5.3 Reset Sequence

Option Function Select Register(1)

b7 b6 b5 b4 b3 b2 b1 b0: 1 1 1

Symbol: OFS | Address: 0FFFFh | When Shipping: FFh(3)

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Starts watchdog timer automatically after reset 1 : Watchdog timer is inactive after reset	RW
— (b1)	Reserved bit	Set to 1.	RW
ROMCR	ROM code protect disabled bit	0 : ROM code protect disabled 1 : ROMCP1 enabled	RW
ROMCP1	ROM code protect bit	0 : ROM code protect enabled 1 : ROM code protect disabled	RW
— (b4)	Reserved bit	Set to 1.	RW
LVD0ON	Voltage detection 0 circuit start bit(2)	0 : Voltage monitor 0 reset enabled after hardware reset 1 : Voltage monitor 0 reset disabled after hardware reset	RW
— (b6)	Reserved bit	Set to 1.	RW
CSPROINI	Count source protect mode after reset select bit	0 : Count source protect mode enabled after reset 1 : Count source protect mode disabled after reset	RW

NOTES:
1. The OFS register is on the flash memory. Write to the OFS register with a program. After writing is completed, do not write additions to the OFS register.
2. To use the power-on reset, set the LVD0ON bit to 0 (voltage monitor 0 reset enabled after reset).
3. If the block including the OFS register is erased, FFh is set to the OFS register.

Figure 5.4 OFS Register

5.1 Hardware Reset

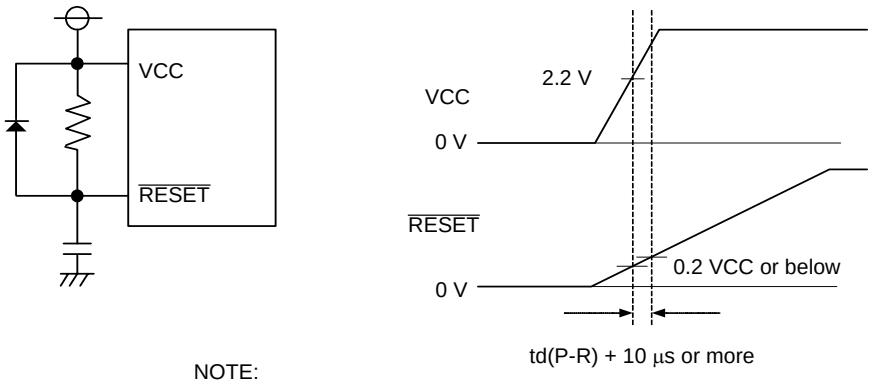
A reset is applied using the $\overline{\text{RESET}}$ pin. When an “L” signal is applied to the $\overline{\text{RESET}}$ pin while the supply voltage meets the recommended operating conditions, pins, CPU, and SFRs are all reset (refer to **Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”**). When the input level applied to the $\overline{\text{RESET}}$ pin changes from “L” to “H”, a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the state of the SFRs after reset.
The internal RAM is not reset. If the $\overline{\text{RESET}}$ pin is pulled “L” while writing to the internal RAM is in progress, the contents of internal RAM will be undefined.
Figure 5.5 shows an Example of Hardware Reset Circuit and Operation and Figure 5.6 shows an Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation.

5.1.1 When Power Supply is Stable

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 µs or more.
(3) Apply “H” to the $\overline{\text{RESET}}$ pin.

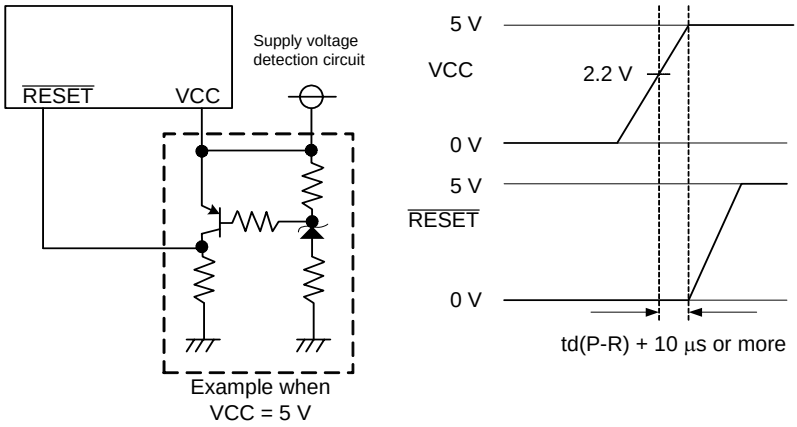
5.1.2 Power On

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Let the supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) or more to allow the internal power supply to stabilize (refer to **20. Electrical Characteristics**).
(4) Wait for 10 µs or more.
(5) Apply “H” to the $\overline{\text{RESET}}$ pin.



NOTE:
1. Refer to **20. Electrical Characteristics.**

Figure 5.5 Example of Hardware Reset Circuit and Operation



NOTE:
1. Refer to **20. Electrical Characteristics.**

Figure 5.6 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation

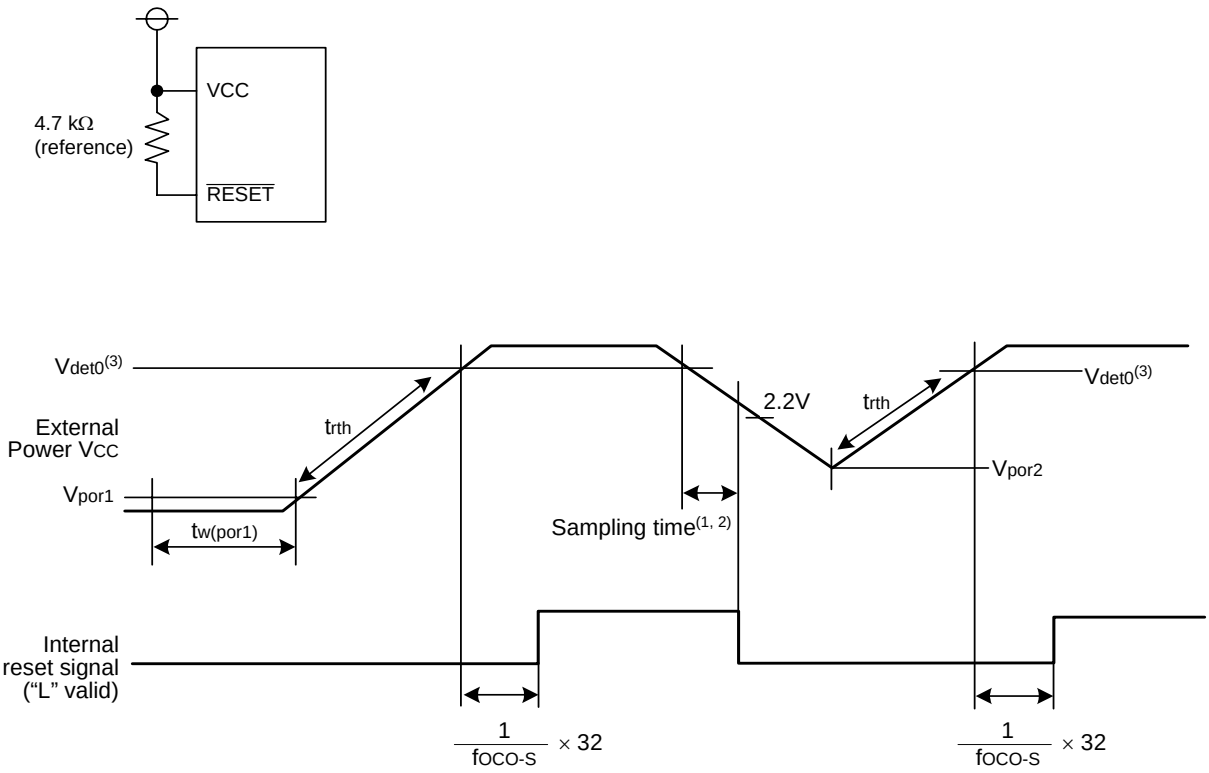
5.2 Power-On Reset Function

When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a pull-up resistor, and the VCC pin voltage level rises while the rise gradient is trth or more, the power-on reset function is enabled and the MCU resets its pins, CPU, and SFR. When a capacitor is connected to the $\overline{\text{RESET}}$ pin, too, always keep the voltage to the $\overline{\text{RESET}}$ pin 0.8VCC or more. When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held "H" and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock after reset.

Refer to **4. Special Function Registers (SFRs)** for the states of the SFR after power-on reset.

The voltage monitor 0 reset is enabled after power-on reset.

Figure 5.7 shows an Example of Power-On Reset Circuit and Operation.



NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
3. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
4. Refer to **20. Electrical Characteristics.**
5. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.

Figure 5.7 Example of Power-On Reset Circuit and Operation

5.3 Voltage Monitor 0 Reset

A reset is applied using the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet0.

When the input voltage to the VCC pin reaches the Vdet0 level or below, the pins, CPU, and SFR are reset.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock start counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held “H” and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock after reset.

The LVD0ON bit in the OFS register can be used to enable or disable voltage monitor 0 reset after a hardware reset. Setting the LVD0ON bit is only valid after a hardware reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.

The LVD0ON bit cannot be changed by a program. To set the LVD0ON bit, write 0 (voltage monitor 0 reset enabled after hardware reset) or 1 (voltage monitor 0 reset disabled after hardware reset) to bit 5 of address 0FFFFh using a flash programmer.

Refer to **Figure 5.4 OFS Register** for details of the OFS register.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFR after voltage monitor 0 reset.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet0 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 0 reset.

5.4 Voltage Monitor 1 Reset

A reset is applied using the on-chip voltage detection 1 circuit. The voltage detection 1 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet1.

When the input voltage to the VCC pin reaches the Vdet1 level or below, the pins, CPU, and SFR are reset and a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock.

The voltage monitor 1 does not reset some portions of the SFR. Refer to **4. Special Function Registers (SFRs)** for details.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet1 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 1 reset.

5.5 Voltage Monitor 2 Reset

A reset is applied using the on-chip voltage detection 2 circuit. The voltage detection 2 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet2.

When the input voltage to the VCC pin reaches the Vdet2 level or below, the pins, CPU, and SFR are reset and the program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock.

The voltage monitor 2 does not reset some SFRs. Refer to **4. Special Function Registers (SFRs)** for details.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet2 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 2 reset.

5.6 Watchdog Timer Reset

When the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows), the MCU resets its pins, CPU, and SFR if the watchdog timer underflows. Then the program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock.
The watchdog timer reset does not reset some SFRs. Refer to **4. Special Function Registers (SFRs)** for details.
The internal RAM is not reset. When the watchdog timer underflows, the contents of internal RAM are undefined.
Refer to **13. Watchdog Timer** for details of the watchdog timer.

5.7 Software Reset

When the PM03 bit in the PM0 register is set to 1 (MCU reset), the MCU resets its pins, CPU, and SFR. The program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected for the CPU clock.
The software reset does not reset some SFRs. Refer to **4. Special Function Registers (SFRs)** for details.
The internal RAM is not reset.

6. Voltage Detection Circuit

The voltage detection circuit monitors the input voltage to the VCC pin. This circuit can be used to monitor the VCC input voltage by a program. Alternately, voltage monitor 0 reset, voltage monitor 1 interrupt, voltage monitor 1 reset, voltage monitor 2 interrupt, and voltage monitor 2 reset can also be used.
Table 6.1 lists the Specifications of Voltage Detection Circuit and Figures 6.1 to 6.4 show the Block Diagrams. Figures 6.5 to 6.8 show the Associated Registers.

Table 6.1 Specifications of Voltage Detection Circuit

Item		Voltage Detection 0	Voltage Detection 1	Voltage Detection 2
VCC Monitor	Voltage to monitor	Vdet0	Vdet1	Vdet2
	Detection target	Whether passing through Vdet0 by rising or falling	Passing through Vdet1 by rising or falling	Passing through Vdet2 by rising or falling
	Monitor	None	VW1C3 bit in VW1C register	VCA13 bit in VCA1 register
			Whether VCC is higher or lower than Vdet1	Whether VCC is higher or lower than Vdet2
Process When Voltage is Detected	Reset	Voltage monitor 0 reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset at Vdet0 > VCC; restart CPU operation at VCC > Vdet0	Reset at Vdet1 > VCC; restart CPU operation after a specified time	Reset at Vdet2 > VCC; restart CPU operation after a specified time
	Interrupt	None	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Interrupt request at Vdet1 > VCC and VCC > Vdet1 when digital filter is enabled; interrupt request at Vdet1 > VCC or VCC > Vdet1 when digital filter is disabled	Interrupt request at Vdet2 > VCC and VCC > Vdet2 when digital filter is enabled; interrupt request at Vdet2 > VCC or VCC > Vdet2 when digital filter is disabled
Digital Filter	Switch enabled/disabled	Available	Available	Available
	Sampling time	(Divide-by-n of fOCO-S) × 4 n: 1, 2, 4, and 8	(Divide-by-n of fOCO-S) × 4 n: 1, 2, 4, and 8	(Divide-by-n of fOCO-S) × 4 n: 1, 2, 4, and 8

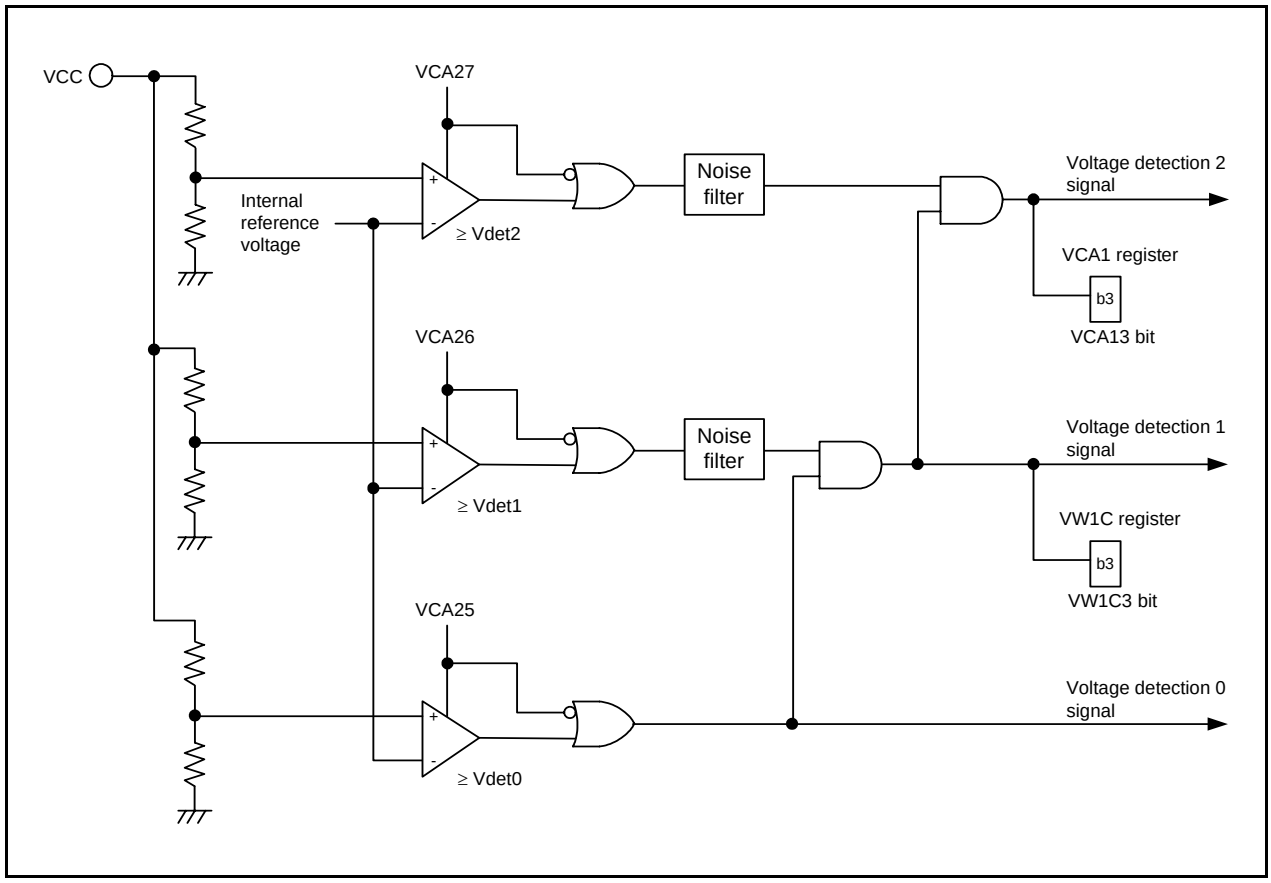


Figure 6.1 Block Diagram of Voltage Detection Circuit

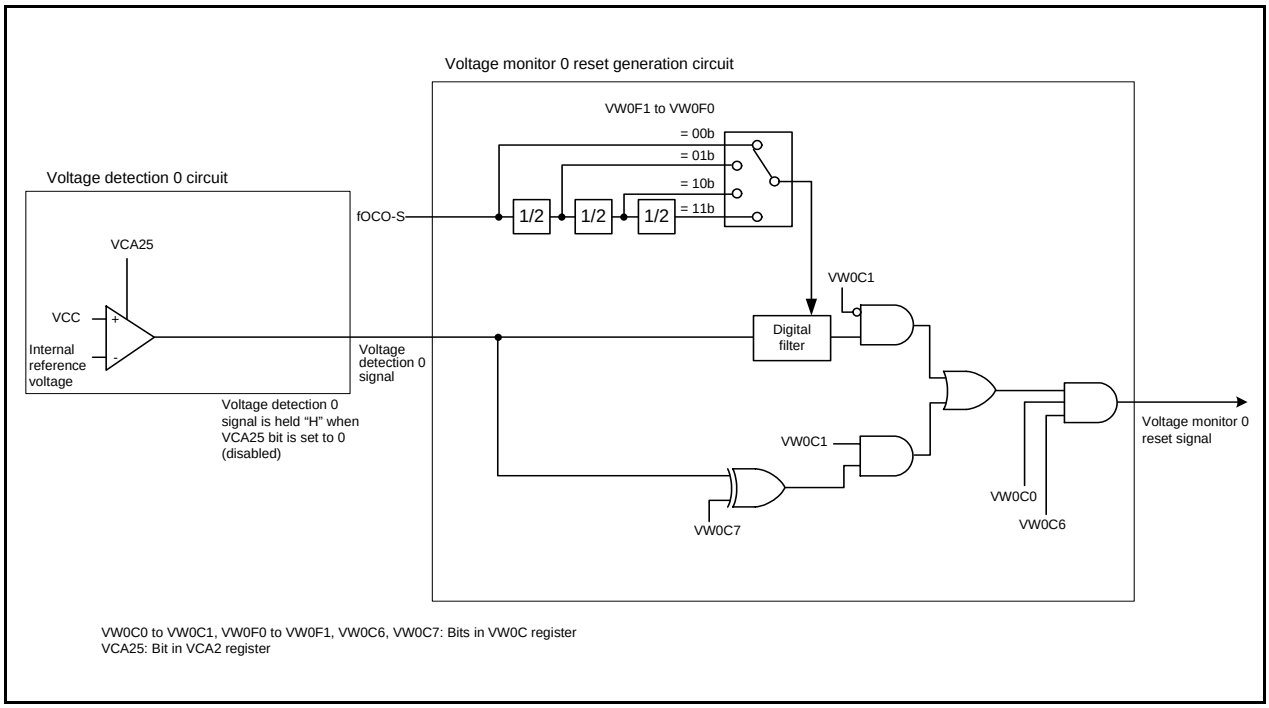


Figure 6.2 Block Diagram of Voltage Monitor 0 Reset Generation Circuit

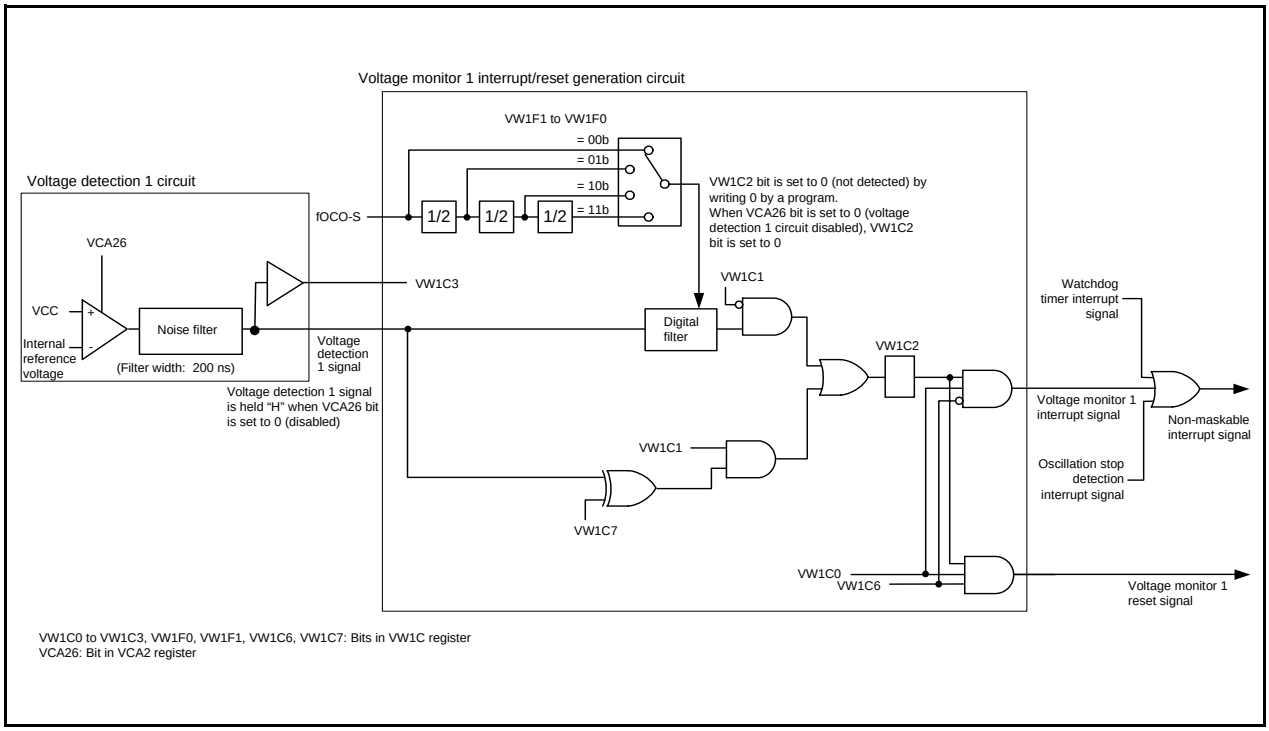


Figure 6.3 Block Diagram of Voltage Monitor 1 Interrupt/Reset Generation Circuit

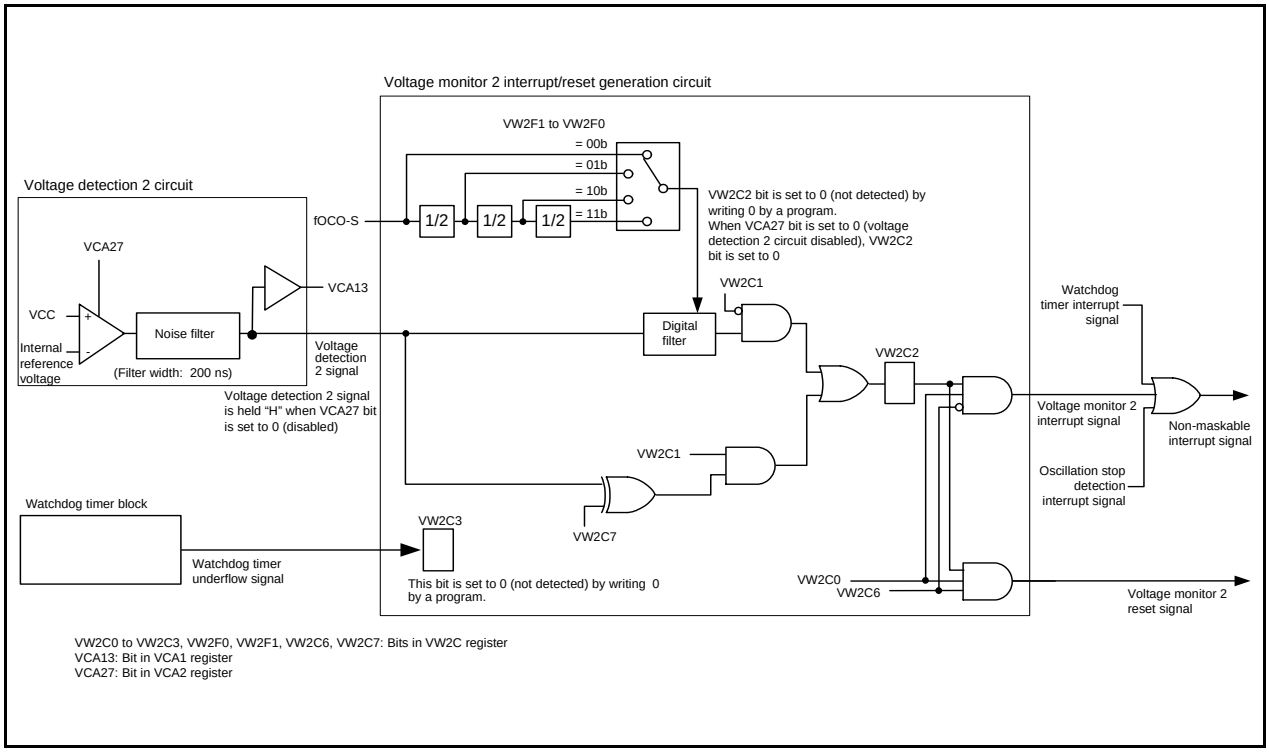
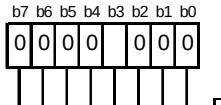


Figure 6.4 Block Diagram of Voltage Monitor 2 Interrupt/Reset Generation Circuit

Voltage Detection Register 1

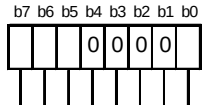


Symbol	Address	After Reset(2)
VCA1	0031h	00001000b

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0.	RW
VCA13	Voltage detection 2 signal monitor flag(1)	0 : VCC < Vdet2 1 : VCC ≥ Vdet2 or voltage detection 2 circuit disabled	RO
— (b7-b4)	Reserved bits	Set to 0.	RW

NOTES:
1. The VCA13 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). The VCA13 bit is set to 1 (VCC ≥ Vdet 2) when the VCA27 bit in the VCA2 register is set to 0 (voltage detection 2 circuit disabled).
2. The software reset, watchdog timer reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect this register.

Voltage Detection Register 2(1)



Symbol	Address	After Reset(5)
VCA2	0032h	The LVD0ON bit in the OFS register is set to 1 and hardware reset : 00h Power-on reset, voltage monitor 0 reset or LVD0ON bit in the OFS register is set to 0, and hardware reset : 00100000b

Bit Symbol	Bit Name	Function	RW
VCA20	Internal power low consumption enable bit(6)	0 : Disables low consumption 1 : Enables low consumption	RW
— (b4-b1)	Reserved bits	Set to 0.	RW
VCA25	Voltage detection 0 enable bit(2)	0 : Voltage detection 0 circuit disabled 1 : Voltage detection 0 circuit enabled	RW
VCA26	Voltage detection 1 enable bit(3)	0 : Voltage detection 1 circuit disabled 1 : Voltage detection 1 circuit enabled	RW
VCA27	Voltage detection 2 enable bit(4)	0 : Voltage detection 2 circuit disabled 1 : Voltage detection 2 circuit enabled	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enable) before writing to the VCA2 register.
2. To use the voltage monitor 0 reset, set the VCA25 bit to 1.
   After the VCA25 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
3. To use the voltage monitor 1 interrupt/reset or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1.
   After the VCA26 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
4. To use the voltage monitor 2 interrupt/reset or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1.
   After the VCA27 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect this register.
6. Use the VCA20 bit only when entering to wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 10.9 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit**.

Figure 6.5 Registers VCA1 and VCA2

Voltage Monitor 0 Circuit Control Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
					0		

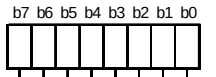
Symbol	Address	After Reset(2)
VW0C	0038h	The LVD0ON bit in the OFS register is set to 1 and hardware reset : 0000X000b Power-on reset, voltage monitor 0 reset or LVD0ON bit in the OFS register is set to 0, and hardware reset : 0100X001b

Bit Symbol	Bit Name	Function	RW
VW0C0	Voltage monitor 0 reset enable bit(3)	0 : Disable 1 : Enable	RW
VW0C1	Voltage monitor 0 digital filter disable mode select bit	0 : Digital filter enabled mode (digital filter circuit enabled) 1 : Digital filter disabled mode (digital filter circuit disabled)	RW
VW0C2	Reserved bit	Set to 0.	RW
— (b3)	Reserved bit	When read, the content is undefined.	RO
VW0F0	Sampling clock select bits	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW0F1			RW
VW0C6	Voltage monitor 0 circuit mode select bit	When the VW0C0 bit is set to 1 (voltage monitor 0 reset enabled), set to 1.	RW
VW0C7	Voltage monitor 0 reset generation condition select bit(4)	When the VW0C1 bit is set to 1 (digital filter disabled mode), set to 1.	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enable) before writing to the VW0C register.
2. The value remains unchanged after a software reset, watchdog timer reset, voltage monitor 1 reset, and voltage monitor 2 reset.
3. The VW0C0 bit is enabled when the VCA25 bit in the VCA2 register is set to 1 (voltage detection 0 circuit enabled). Set the VW0C0 bit to 0 (disable), when the VCA25 bit is set to 0 (voltage detection 0 circuit disabled).
4. The VW0C7 bit is enabled when the VW0C1 bit set to 1 (digital filter disabled mode).

Figure 6.6 VW0C Register

Voltage Monitor 1 Circuit Control Register(1)



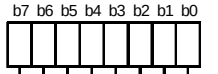
Symbol	Address	After Reset(8)
VW1C	0036h	00001000b

Bit Symbol	Bit Name	Function	RW
VW1C0	Voltage monitor 1 interrupt/reset enable bit(6)	0 : Disable 1 : Enable	RW
VW1C1	Voltage monitor 1 digital filter disable mode select bit(2)	0 : Digital filter enabled mode (digital filter circuit enabled) 1 : Digital filter disabled mode (digital filter circuit disabled)	RW
VW1C2	Voltage change detection flag(3, 4, 8)	0 : Not detected 1 : Vdet1 crossing detected	RW
VW1C3	Voltage detection 1 signal monitor flag(3, 8)	0 : VCC < Vdet1 1 : VCC ≥ Vdet1 or voltage detection 1 circuit disabled	RO
VW1F0	Sampling clock select bits	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW1F1			RW
VW1C6	Voltage monitor 1 circuit mode select bit(5)	0 : Voltage monitor 1 interrupt mode 1 : Voltage monitor 1 reset mode	RW
VW1C7	Voltage monitor 1 interrupt/reset generation condition select bit(7, 9)	0 : When VCC reaches Vdet1 or above 1 : When VCC reaches Vdet1 or below	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (rew rite enable) before w riting to the VW1C register.
2. To use the voltage monitor 1 interrupt to exit stop mode and to return again, w rite 0 to the VW1C1 bit before w riting 1.
3. Bits VW1C2 and VW1C3 are enabled w hen the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled).
4. Set this bit to 0 by a program. When 0 is w ritten by a program, it is set to 0 (and remains unchanged even if 1 is w ritten to it).
5. The VW1C6 bit is enabled w hen the VW1C0 bit is set to 1 (voltage monitor 1 interrupt/enabled reset).
6. The VW1C0 bit is enabled w hen the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disable) w hen the VCA26 bit is set to 0 (voltage detection 1 circuit disabled).
7. The VW1C7 bit is enabled w hen the VW1C1 bit is set to 1 (digital filter disabled mode).
8. Bits VW1C2 and VW1C3 remain unchanged after a softw are reset, w atchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset.
9. When the VW1C6 bit is set to 1 (voltage monitor 1 reset mode), set the VW1C7 bit to 1 (w hen VCC reaches Vdet1 or below). (Do not set to 0.)

Figure 6.7 VW1C Register

Voltage Monitor 2 Circuit Control Register(1)



Symbol	Address	After Reset(8)
VW2C	0037h	00h

Bit Symbol	Bit Name	Function	RW
VW2C0	Voltage monitor 2 interrupt/reset enable bit(6)	0 : Disable 1 : Enable	RW
VW2C1	Voltage monitor 2 digital filter disable mode select bit(2)	0 : Digital filter enabled mode (digital filter circuit enabled) 1 : Digital filter disabled mode (digital filter circuit disabled)	RW
VW2C2	Voltage change detection flag(3, 4, 8)	0 : Not detected 1 : VCC has crossed Vdet2	RW
VW2C3	WDT detection flag(4, 8)	0 : Not detected 1 : Detected	RW
VW2F0	Sampling clock select bits	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW2F1			RW
VW2C6	Voltage monitor 2 circuit mode select bit(5)	0 : Voltage monitor 2 interrupt mode 1 : Voltage monitor 2 reset mode	RW
VW2C7	Voltage monitor 2 interrupt/reset generation condition select bit(7, 9)	0 : When VCC reaches Vdet2 or above 1 : When VCC reaches Vdet2 or below	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enable) before writing to the VW2C register.
2. To use the voltage monitor 2 interrupt to exit stop mode and to return again, write 0 to the VW2C1 bit before writing 1.
3. The VW2C2 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled).
4. Set this bit to 0 by a program. When 0 is written by a program, it is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW2C6 bit is enabled when the VW2C0 bit is set to 1 (voltage monitor 2 interrupt/enables reset).
6. The VW2C0 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disable) when the VCA27 bit is set to 0 (voltage detection 2 circuit disabled).
7. The VW2C7 bit is enabled when the VW2C1 bit is set to 1 (digital filter disabled mode).
8. Bits VW2C2 and VW2C3 remain unchanged after a software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset.
9. When the VW2C6 bit is set to 1 (voltage monitor 2 reset mode), set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below). (Do not set to 0.)

Figure 6.8 VW2C Register

6.1 VCC Input Voltage

6.1.1 Monitoring Vdet0

Vdet0 cannot be monitored.

6.1.2 Monitoring Vdet1

Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled). After td(E-A) has elapsed (refer to **20. Electrical Characteristics**), Vdet1 can be monitored by the VW1C3 bit in the VW1C register.

6.1.3 Monitoring Vdet2

Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled). After td(E-A) has elapsed (refer to **20. Electrical Characteristics**), Vdet2 can be monitored by the VCA13 bit in the VCA1 register.

6.2 Voltage Monitor 0 Reset

Table 6.2 lists the Procedure for Setting Bits Associated with Voltage Monitor Reset and Figure 6.9 shows an Example of Voltage Monitor 0 Reset Operation. To use the voltage monitor 0 reset to exit stop mode, set the VW0C1 bit in the VW0C register to 1 (digital filter disabled).

Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor Reset

Step	When Using Digital Filter	When Not Using Digital Filter
1	Set the VCA25 bit in the VCA2 register to 1 (voltage detection 0 circuit enabled)	
2	Wait for td(E-A)	
3	Select the sampling clock of the digital filter by the VW0F0 to VW0F1 bits in the VW0C register	Set the VW0C7 bit in the VW0C register to 1
4(1)	Set the VW0C1 bit in the VW0C register to 0 (digital filter enabled)	Set the VW0C1 bit in the VW0C register to 1 (digital filter disabled)
5(1)	Set the VW0C6 bit in the VW0C register to 1 (voltage monitor 0 reset mode)	
6	Set the VW0C2 bit in the VW0C register to 0	
7	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	–
8	Wait for 4 cycles of the sampling clock of the digital filter	– (No wait time required)
9	Set the VW0C0 bit in the VW0C register to 1 (voltage monitor 0 reset enabled)	

NOTE:
1. When the VW0C0 bit is set to 0, steps 3, 4, and 5 can be executed simultaneously (with 1 instruction).

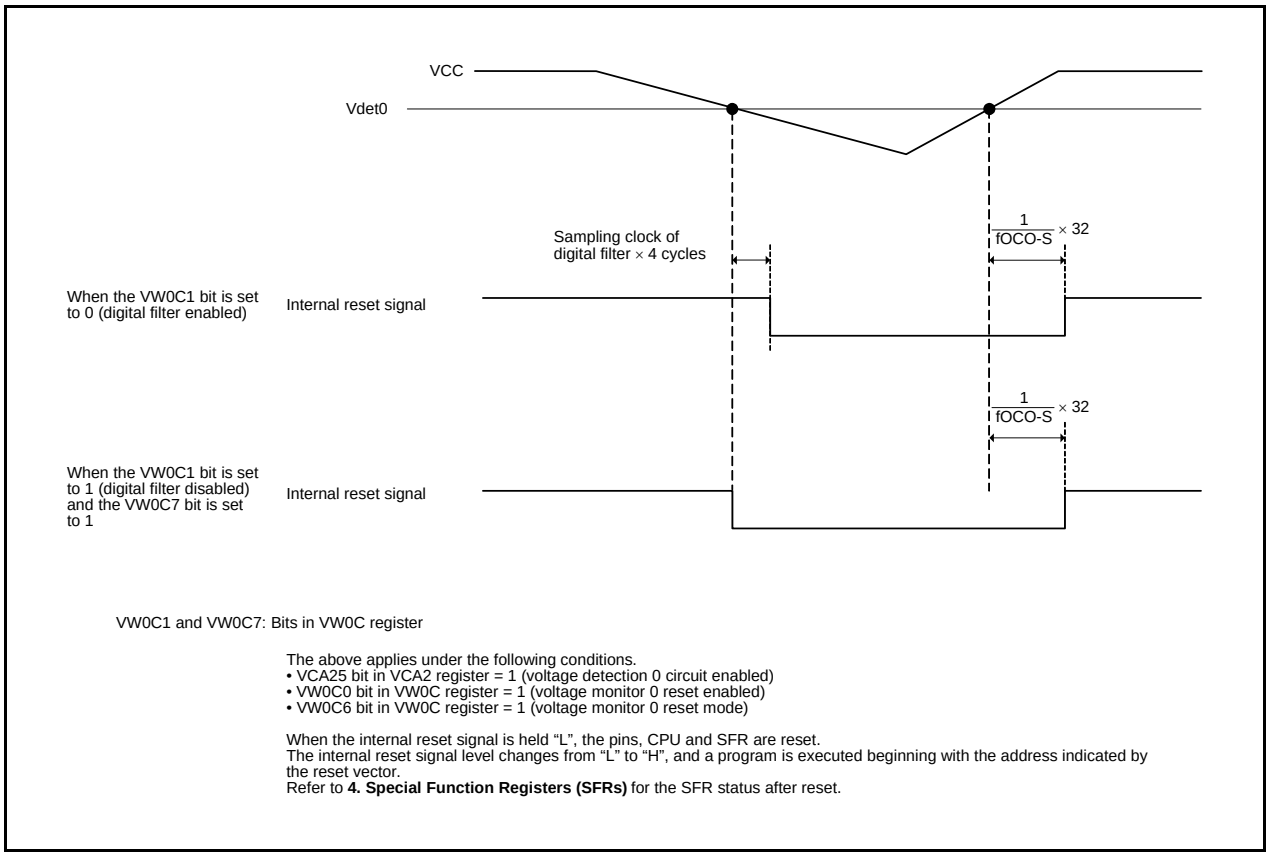


Figure 6.9 Example of Voltage Monitor 0 Reset Operation

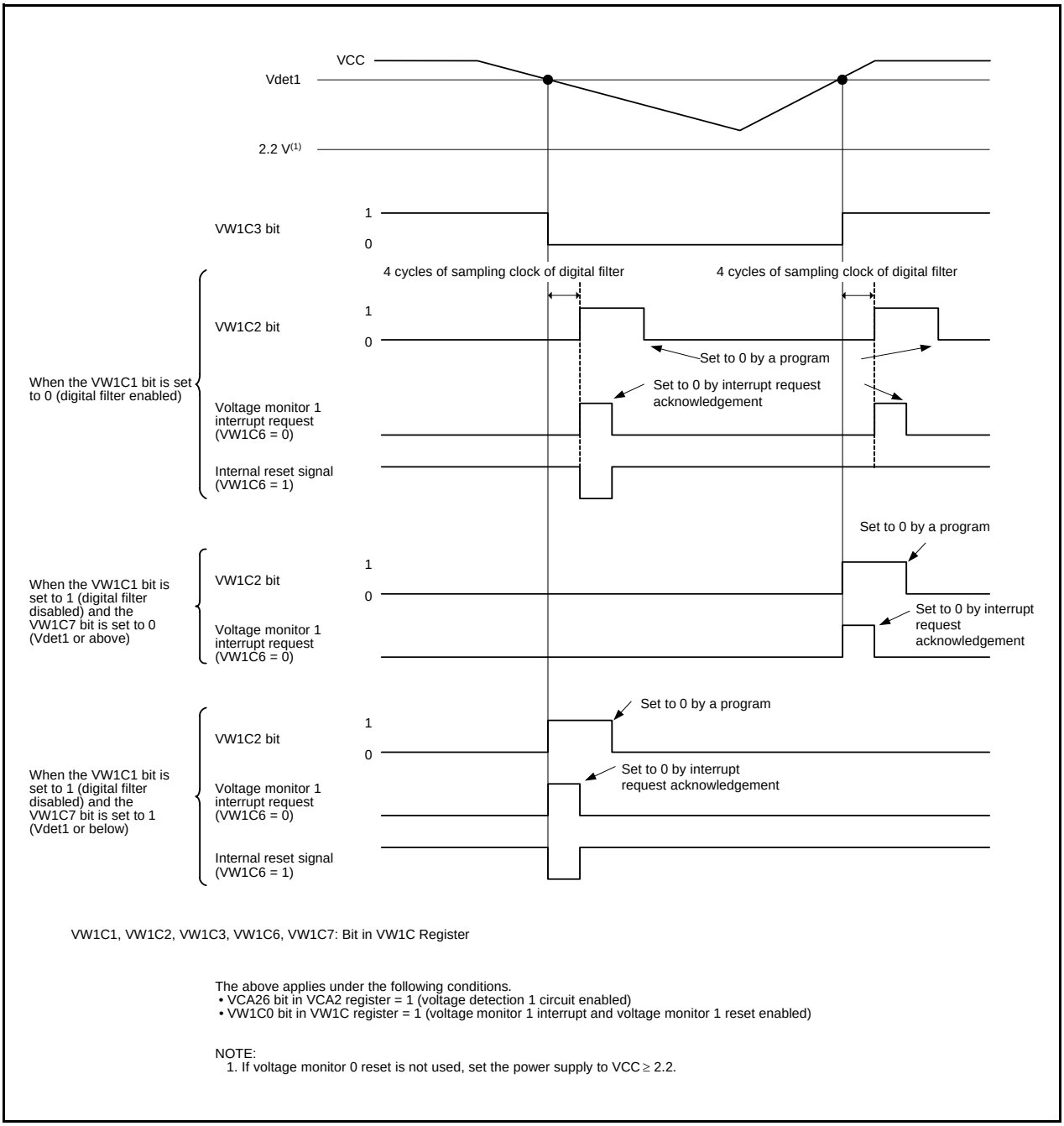
6.3 Voltage Monitor 1 Interrupt and Voltage Monitor 1 Reset

Table 6.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt and Reset. Figure 6.10 shows an Example of Voltage Monitor 1 Interrupt and Voltage Monitor 1 Reset Operation. To use the voltage monitor 1 interrupt or voltage monitor 1 reset to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).

Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt and Reset

Step	When Using Digital Filter		When Not Using Digital Filter	
	Voltage Monitor 1 Interrupt	Voltage Monitor 1 Reset	Voltage Monitor 1 Interrupt	Voltage Monitor 1 Reset
1	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled)			
2	Wait for td(E-A)			
3	Select the sampling clock of the digital filter by the VW1F0 to VW1F1 bits in the VW1C register		Select the timing of the interrupt and reset request by the VW1C7 bit in the VW1C register(1)	
4(2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled)		Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled)	
5(2)	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt mode)	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset mode)	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt mode)	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset mode)
6	Set the VW1C2 bit in the VW1C register to 0 (passing of Vdet1 is not detected)			
7	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)		–	
8	Wait for 4 cycles of the sampling clock of the digital filter		– (No wait time required)	
9	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt/reset enabled)			

NOTES:
1. Set the VW1C7 bit to 1 (when VCC reaches Vdet1 or below) for the voltage monitor 1 reset.
2. When the VW1C0 bit is set to 0, steps 3, 4, and 5 can be executed simultaneously (with 1 instruction).



VW1C1, VW1C2, VW1C3, VW1C6, VW1C7: Bit in VW1C Register

The above applies under the following conditions.
- VCA26 bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage monitor 1 interrupt and voltage monitor 1 reset enabled)

NOTE:
1. If voltage monitor 0 reset is not used, set the power supply to VCC ≥ 2.2.

Figure 6.10 Example of Voltage Monitor 1 Interrupt and Voltage Monitor 1 Reset Operation

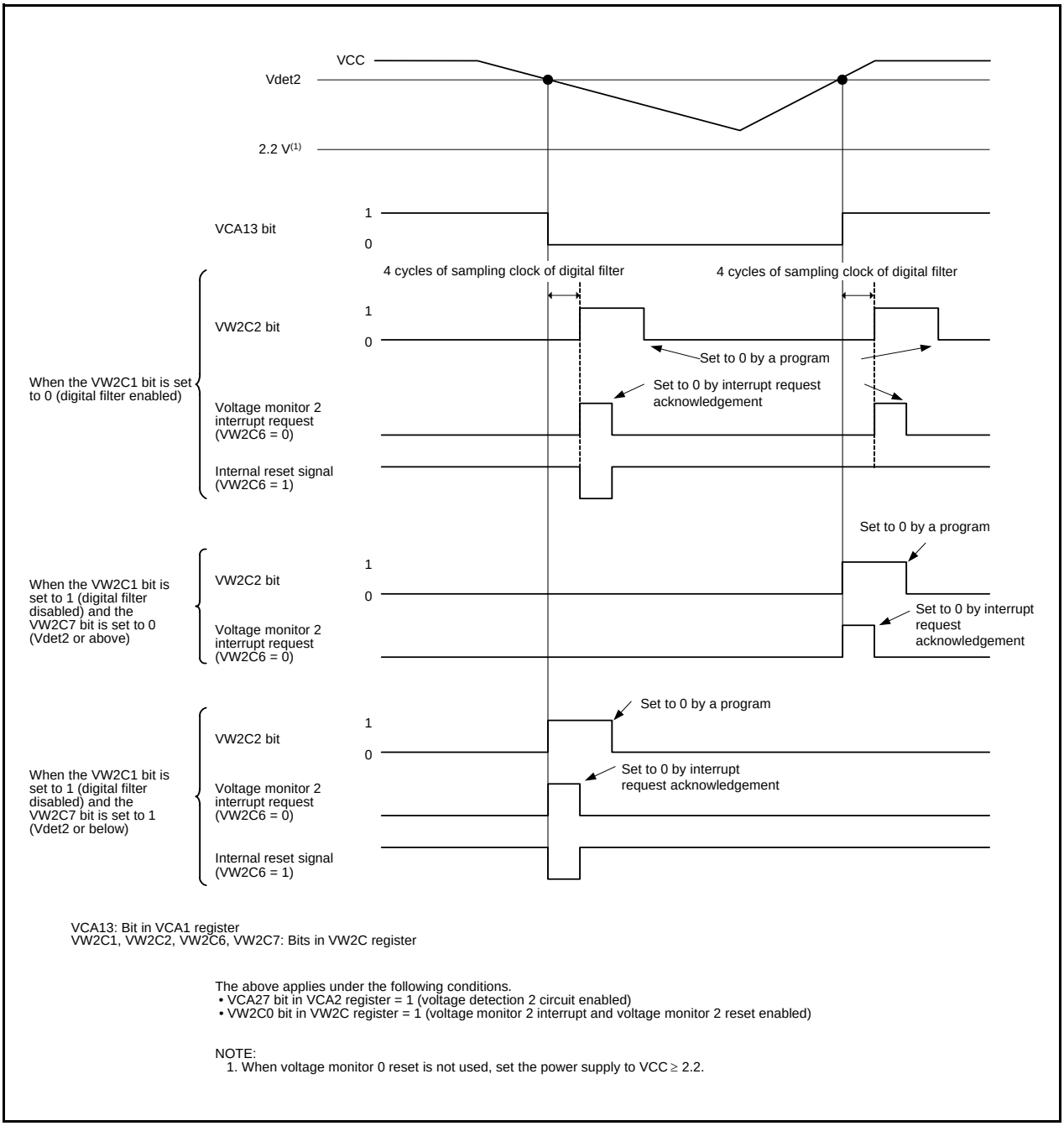
6.4 Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset

Table 6.4 lists the Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt and Reset. Figure 6.11 shows an Example of Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset Operation. To use the voltage monitor 2 interrupt or voltage monitor 2 reset to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

Table 6.4 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt and Reset

Step	When Using Digital Filter		When Not Using Digital Filter	
	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset
1	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled)			
2	Wait for td(E-A)			
3	Select the sampling clock of the digital filter by the VW2F0 to VW2F1 bits in the VW2C register		Select the timing of the interrupt and reset request by the VW2C7 bit in the VW2C register(1)	
4	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled)		Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled)	
5(2)	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode)	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode)	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode)	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode)
6	Set the VW2C2 bit in the VW2C register to 0 (passing of Vdet2 is not detected)			
7	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)		–	
8	Wait for 4 cycles of the sampling clock of the digital filter		– (No wait time required)	
9	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt/reset enabled)			

NOTES:
1. Set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below) for the voltage monitor 2 reset.
2. When the VW2C0 bit is set to 0, steps 3, 4, and 5 can be executed simultaneously (with 1 instruction).



VCA13: Bit in VCA1 register
VW2C1, VW2C2, VW2C6, VW2C7: Bits in VW2C register

The above applies under the following conditions.
- VCA27 bit in VCA2 register = 1 (voltage detection 2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (voltage monitor 2 interrupt and voltage monitor 2 reset enabled)

NOTE:
1. When voltage monitor 0 reset is not used, set the power supply to VCC ≥ 2.2.

Figure 6.11 Example of Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset Operation

7. Programmable I/O Ports

There are 41 programmable Input/Output ports (I/O ports) P0 to P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, and P6. Also, P4_6 and P4_7 can be used as input-only ports if the XIN clock oscillation circuit is not used, and the P4_2 can be used as an input-only port if the A/D converter is not used.
Table 7.1 lists an Overview of Programmable I/O Ports.

Table 7.1 Overview of Programmable I/O Ports

Ports	I/O	Type of Output	I/O Setting	Internal Pull-Up Resister
P0 to P2, P6	I/O	CMOS3 State	Set per bit	Set every 4 bits(1)
P3_0, P3_1, P3_3 to P3_4, P3_5, P3_7	I/O	CMOS3 State	Set per bit	Set every 3 bits(1)
P4_3	I/O	CMOS3 State	Set per bit	Set every bit(1)
P4_4, P4_5	I/O	CMOS3 State	Set per bit	Set every 2 bits(1)
P4_2(2) P4_6, P4_7(3)	I	(No output function)	None	None

NOTES:
1. In input mode, whether an internal pull-up resistor is connected or not can be selected by registers PUR0 and PUR1.
2. When the A/D converter is not used, this port can be used as the input-only port.
3. When the XIN clock oscillation circuit is not used, these ports can be used as the input-only ports.

7.1 Functions of Programmable I/O Ports

The PDi_j (j = 0 to 7) bit in the PDi (i = 0 to 4, 6) register controls I/O of the ports P0 to P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, and P6. The Pi register consists of a port latch to hold output data and a circuit to read pin states.
Figures 7.1 to 7.7 show the Configurations of Programmable I/O Ports. Table 7.2 lists the Functions of Programmable I/O Ports. Also, Figure 7.9 shows the PDi (i = 0 to 4 and 6) Registers. Figure 7.10 shows the Pi (i = 0 to 4 and 6) Registers, Figure 7.11 shows Registers PUR0 and PUR1, Figure 7.12 shows the PMR Register, Figure 7.13 shows the P2DRR Register.

Table 7.2 Functions of Programmable I/O Ports

Operation When Accessing Pi Register	Value of PDi_j Bit in PDi Register(1)	
	When PDi_j Bit is Set to 0 (Input Mode)	When PDi_j Bit is Set to 1 (Output Mode)
Reading	Read pin input level	Read the port latch
Writing	Write to the port latch	Write to the port latch. The value written to the port latch is output from the pin.

i = 0 to 4, 6 j = 0 to 7
NOTE:
1. Nothing is assigned to bits PD3_2, PD3_6, PD4_0 to PD4_2, PD4_6, and PD4_7.

7.2 Effect on Peripheral Functions

Programmable I/O ports function as I/O ports for peripheral functions (Refer to **Table 1.6 Pin Name Information by Pin Number**).
Table 7.3 lists the Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0 to 4, 6 j = 0 to 7). Refer to the description of each function for information on how to set peripheral functions.

Table 7.3 Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0 to 4, 6 j = 0 to 7)

I/O of Peripheral Functions	PDi_j Bit Settings for Shared Pin Functions
Input	Set this bit to 0 (input mode).
Output	This bit can be set to either 0 or 1 (output regardless of the port setting)

7.3 Pins Other than Programmable I/O Ports

Figure 7.8 shows the Configuration of I/O Pins.

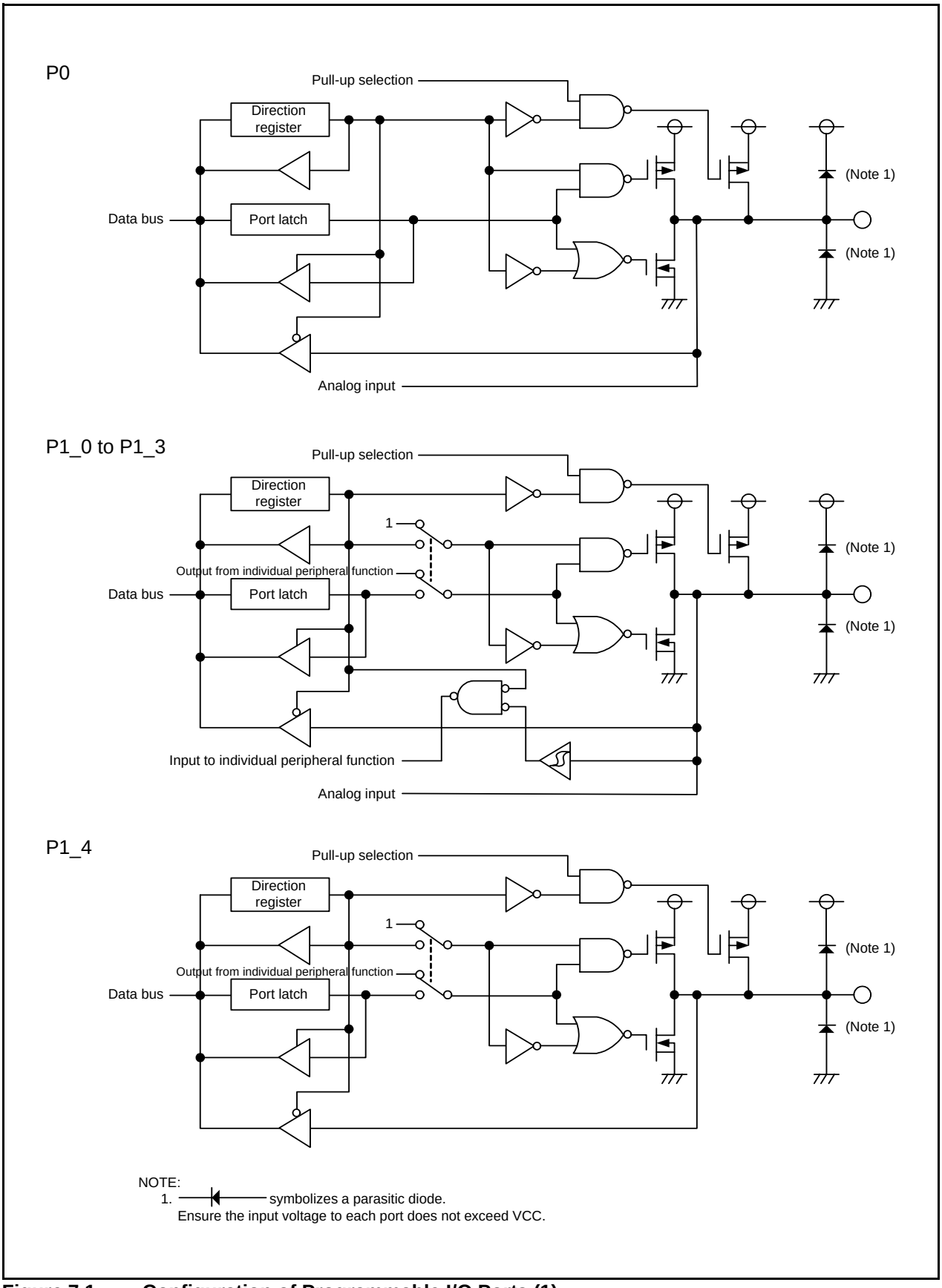


Figure 7.1 Configuration of Programmable I/O Ports (1)

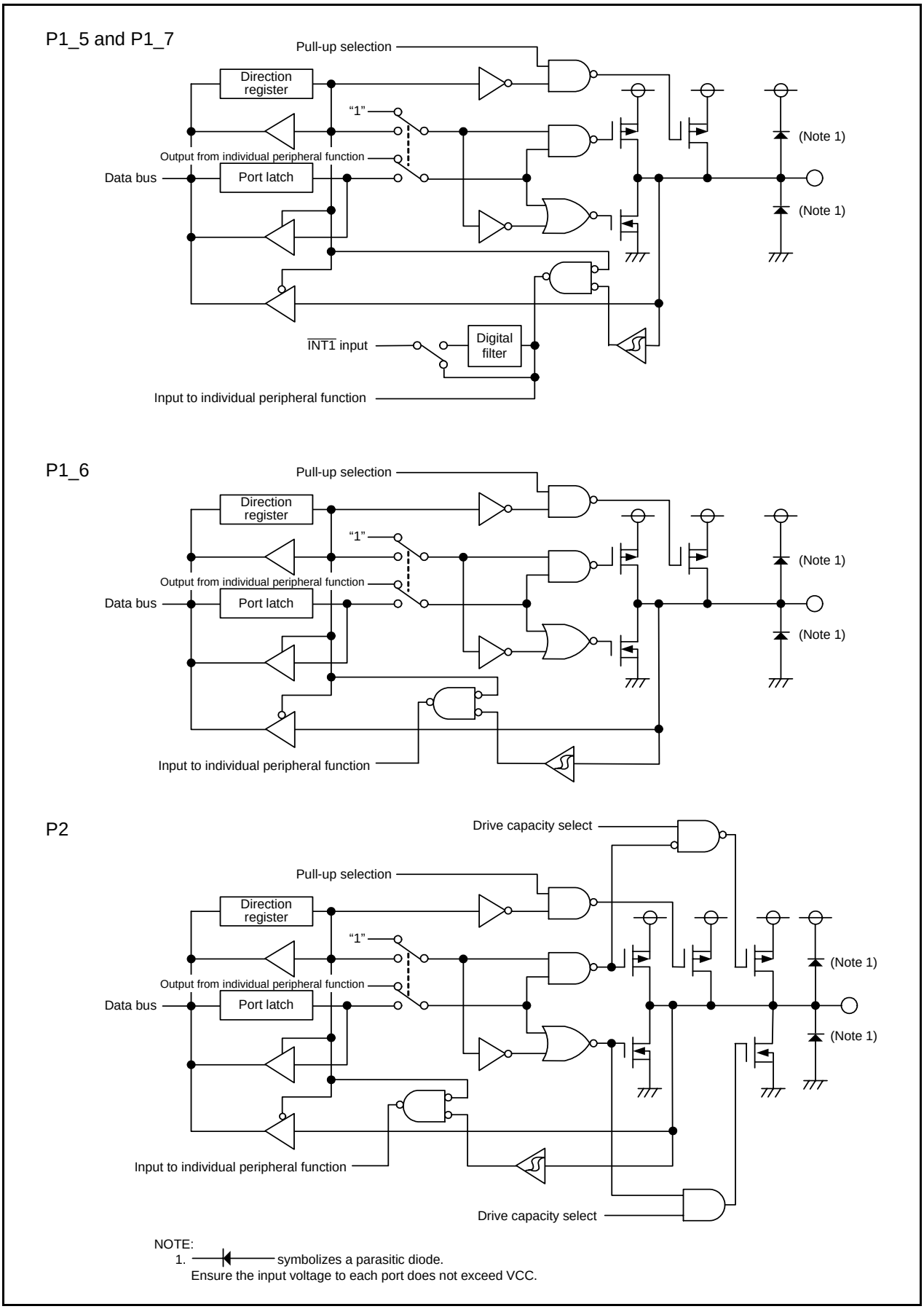


Figure 7.2 Configuration of Programmable I/O Ports (2)

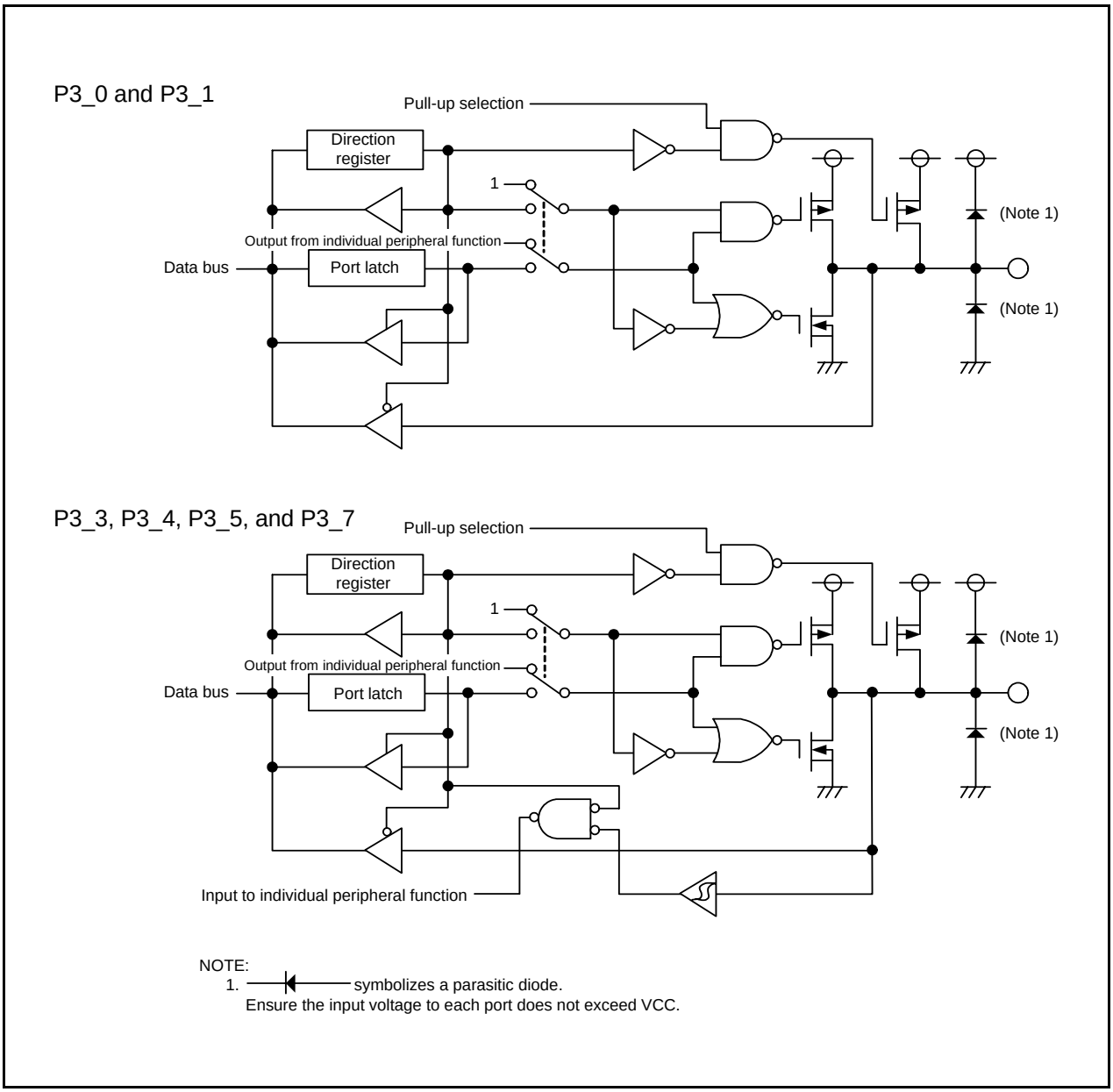


Figure 7.3 Configuration of Programmable I/O Ports (3)

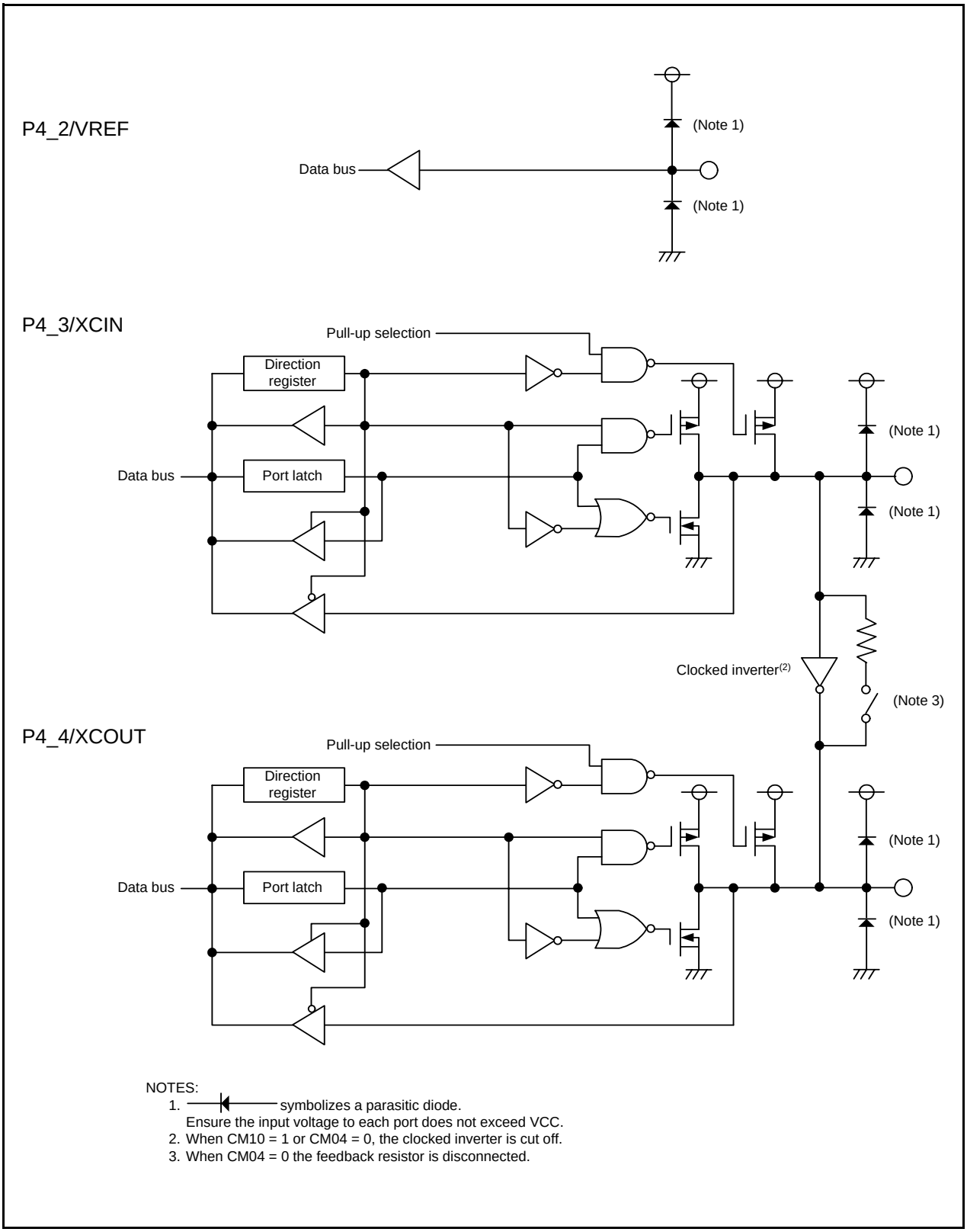


Figure 7.4 Configuration of Programmable I/O Ports (4)

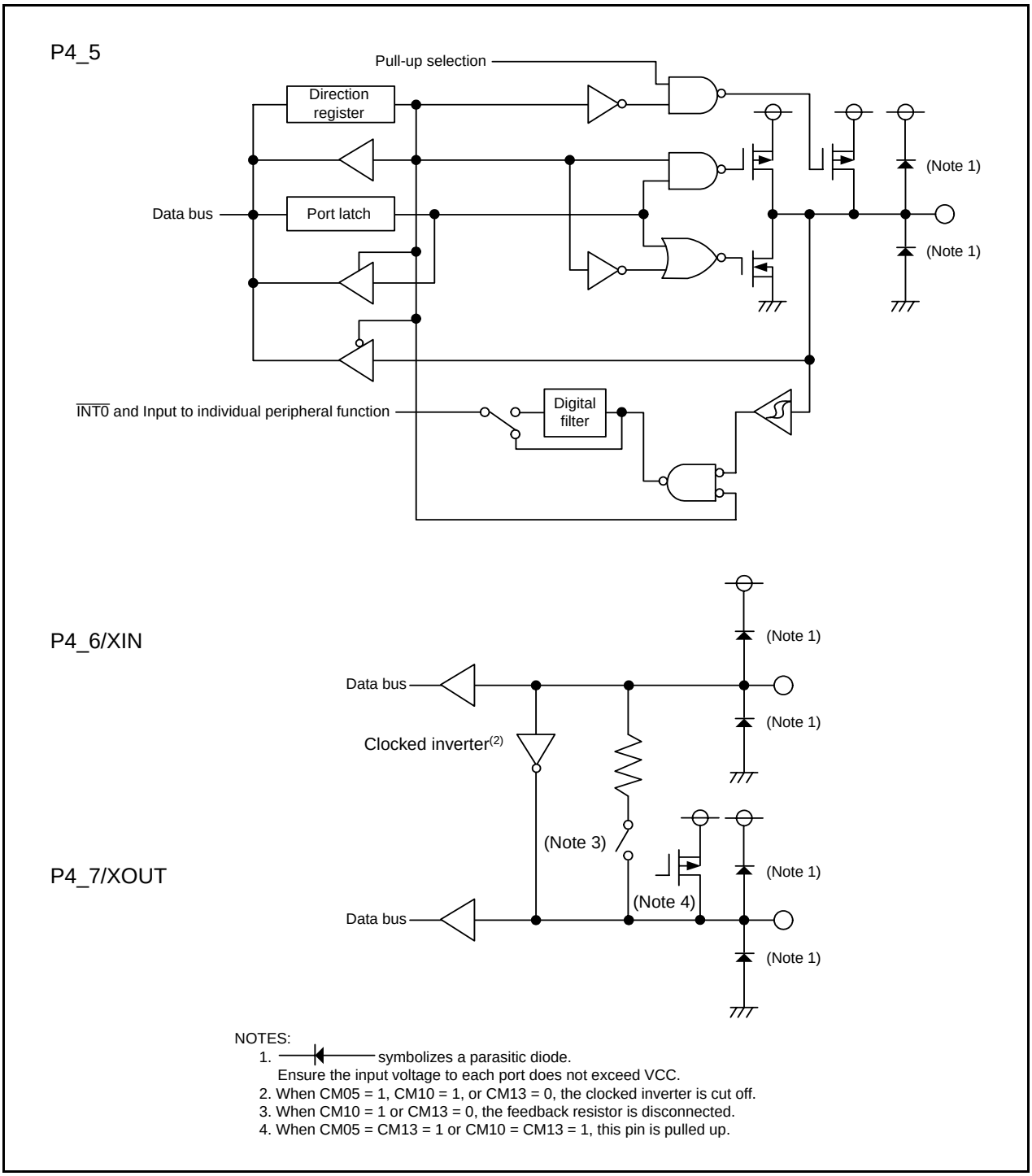
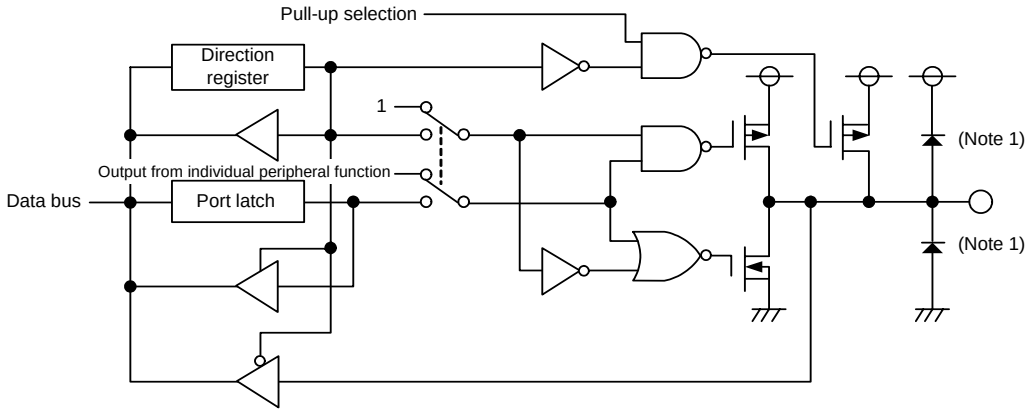
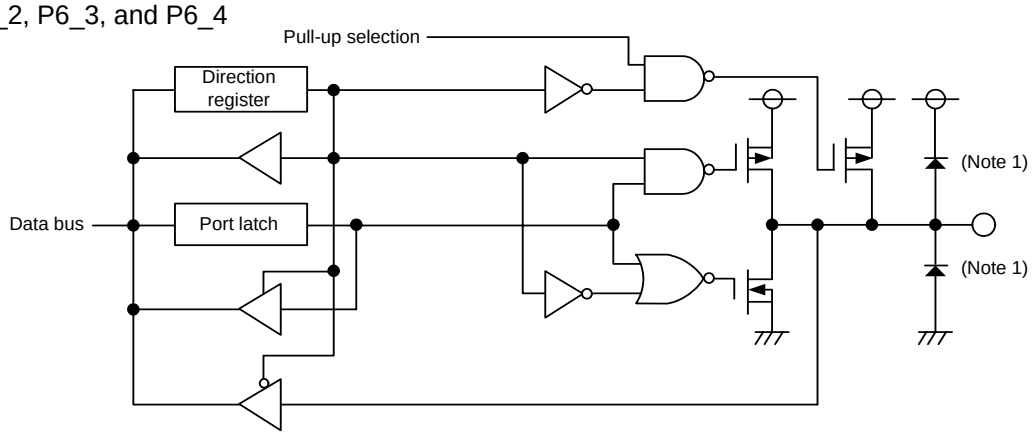


Figure 7.5 Configuration of Programmable I/O Ports (5)

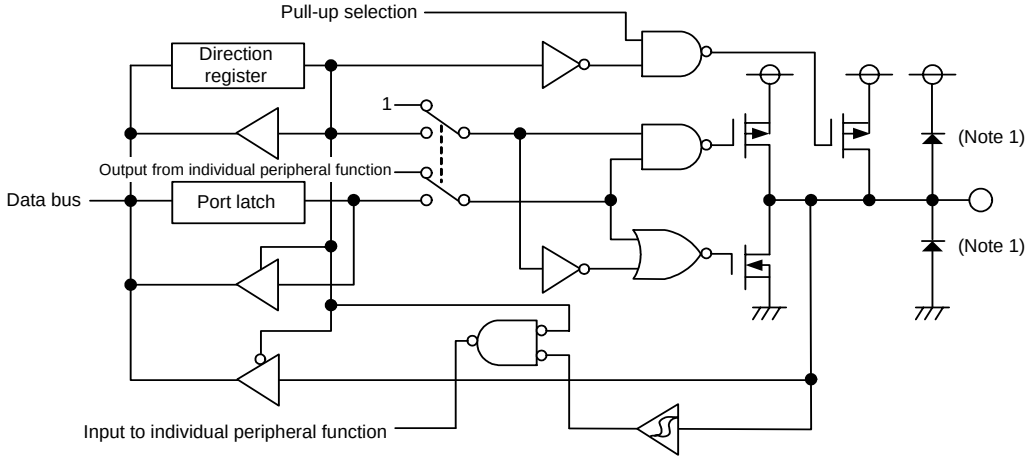
P6_0



P6_1, P6_2, P6_3, and P6_4



P6_5



NOTE:
1. ——|◄—— symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

Figure 7.6 Configuration of Programmable I/O Ports (6)

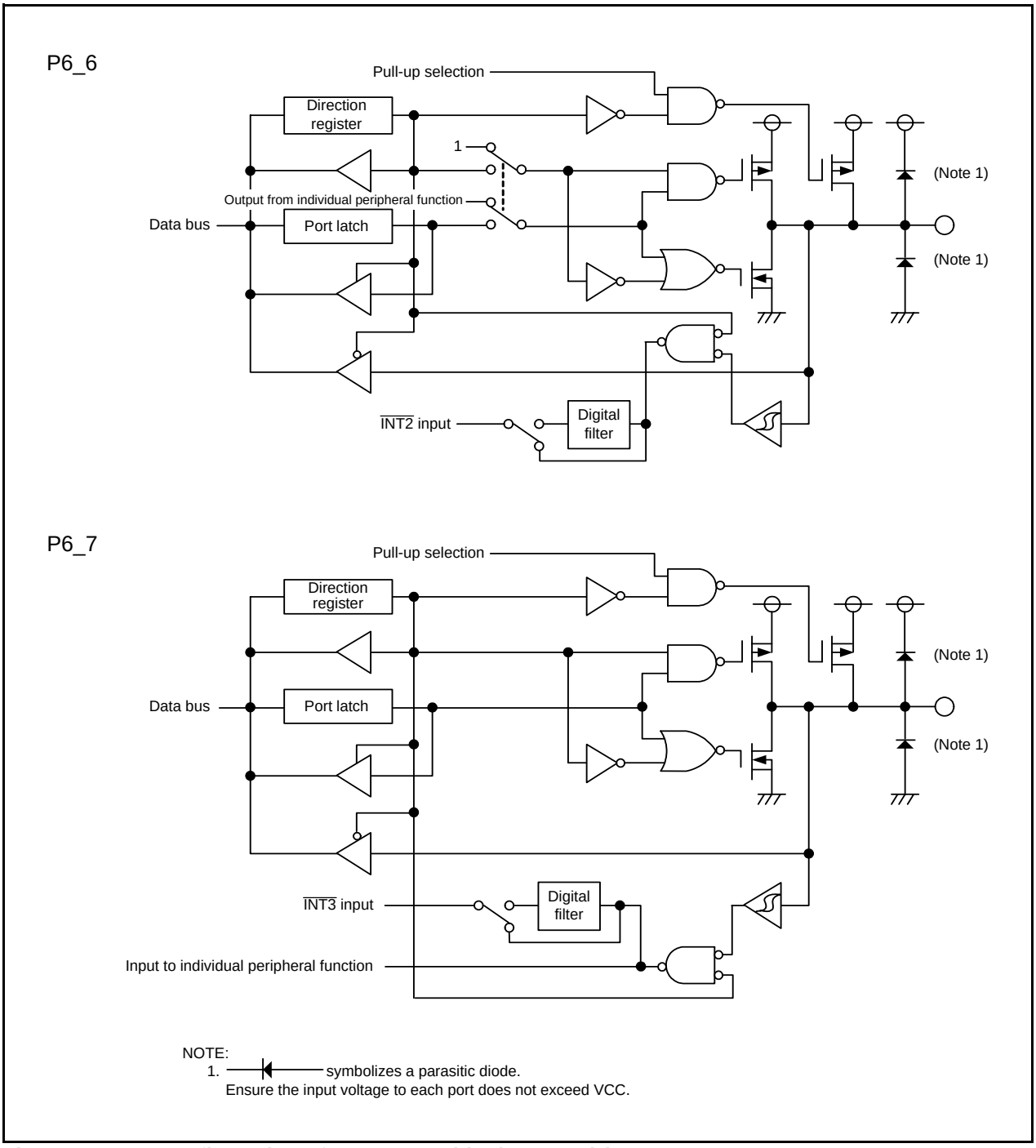


Figure 7.7 Configuration of Programmable I/O Ports (7)

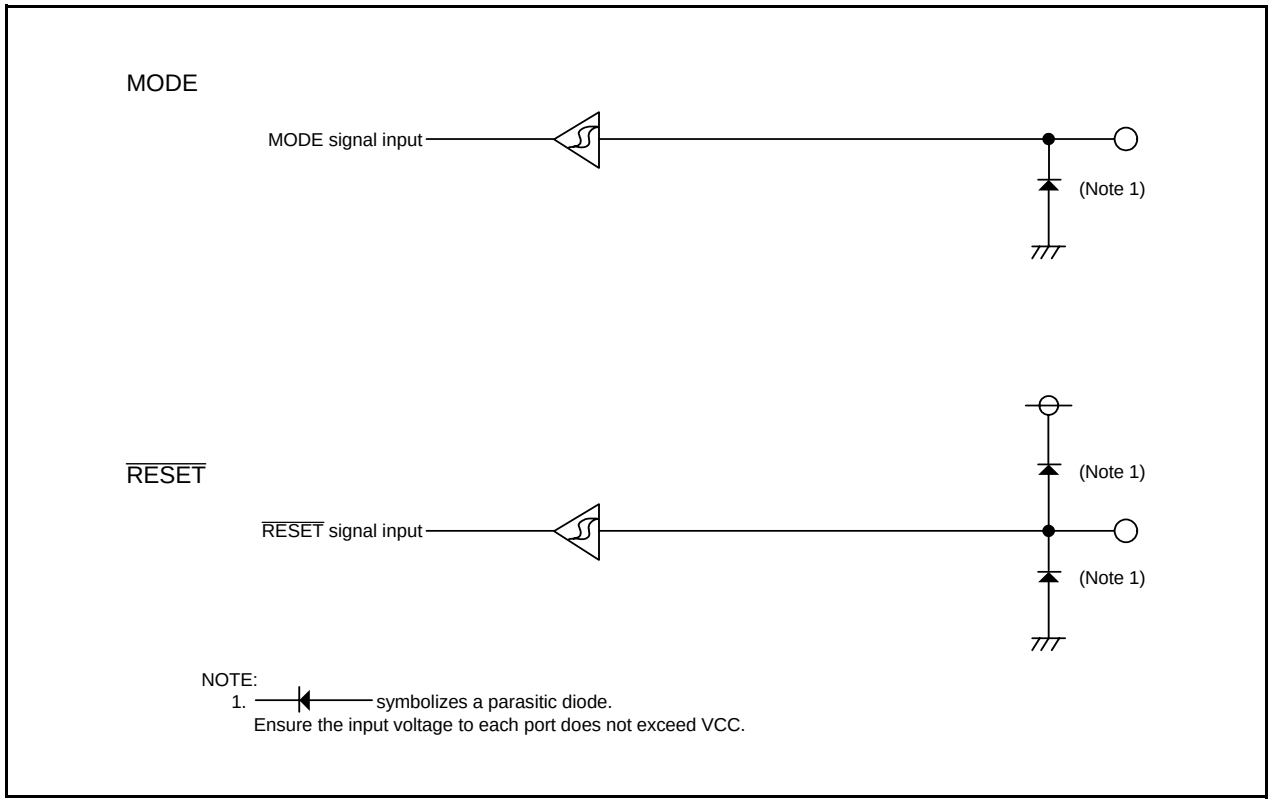
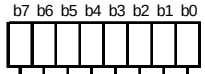


Figure 7.8 Configuration of I/O Pins

Port Pi Direction Register (i = 0 to 4, 6)(1, 2)



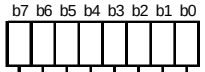
Symbol	Address	After Reset
PD0(3)	00E2h	00h
PD1	00E3h	00h
PD2	00E6h	00h
PD3	00E7h	00h
PD4	00EAh	00h
PD6	00EEh	00h

Bit Symbol	Bit Name	Function	RW
PDi_0	Port Pi_0 direction bit	0 : Input mode (functions as an input port) 1 : Output mode (functions as an output port)	RW
PDi_1	Port Pi_1 direction bit		RW
PDi_2	Port Pi_2 direction bit		RW
PDi_3	Port Pi_3 direction bit		RW
PDi_4	Port Pi_4 direction bit		RW
PDi_5	Port Pi_5 direction bit		RW
PDi_6	Port Pi_6 direction bit		RW
PDi_7	Port Pi_7 direction bit		RW

NOTES:
1. Bits PD3_2 and PD3_6 in the PD3 register are unavailable on this MCU.
   If it is necessary to set bits PD3_2 and PD3_6, set to 0 (input mode). When read, the content is 0.
2. Bits PD4_0 to PD4_2, PD4_6, and PD4_7 in the PD4 register are unavailable on this MCU.
   If it is necessary to set bits PD4_0 to PD4_2, PD4_6 and PD4_7 in the PD4 register, set to 0 (input mode). When read, the content is 0.
3. Write to the PD0 register with the next instruction after that used to set the PRC2 bit in the PRCR register to 1 (write enabled).

Figure 7.9 PDi (i = 0 to 4 and 6) Registers

Port Pi Register (i = 0 to 4, 6)(1, 2)



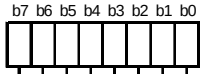
Symbol	Address	After Reset
P0	00E0h	Undefined
P1	00E1h	Undefined
P2	00E4h	Undefined
P3	00E5h	Undefined
P4	00E8h	Undefined
P6	00ECh	Undefined

Bit Symbol	Bit Name	Function	RW
Pi_0	Port Pi_0 bit	The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register. 0 : "L" level 1 : "H" level	RW
Pi_1	Port Pi_1 bit		RW
Pi_2	Port Pi_2 bit		RW
Pi_3	Port Pi_3 bit		RW
Pi_4	Port Pi_4 bit		RW
Pi_5	Port Pi_5 bit		RW
Pi_6	Port Pi_6 bit		RW
Pi_7	Port Pi_7 bit		RW

NOTES:
1. Bits P3_2 and P3_6 in the P3 register are unavailable on this MCU.
   If it is necessary to set bits P3_2 and P3_6, set to 0 ("L" level). When read, the content is 0.
2. Bits P4_0 and P4_1 in the P4 register are unavailable on this MCU.
   If it is necessary to set bits P4_0 and P4_1, set to 0 ("L" level). When read, the content is 0.

Figure 7.10 Pi (i = 0 to 4 and 6) Registers

Pull-Up Control Register 0

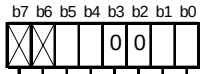


Symbol	Address	After Reset
PUR0	00FCh	00h

Bit Symbol	Bit Name	Function	RW
PU00	P0_0 to P0_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU01	P0_4 to P0_7 pull-up(1)		RW
PU02	P1_0 to P1_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU03	P1_4 to P1_7 pull-up(1)		RW
PU04	P2_0 to P2_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU05	P2_4 to P2_7 pull-up(1)		RW
PU06	P3_0, P3_1, and P3_3 pll-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU07	P3_4 to P3_5, and P3_7 pll-up(1)	0 : Not pulled up 1 : Pulled up	RW

NOTE:
1. When this bit is set to 1 (pulled up), the pin w hose direction bit is set to 0 (input mode) is pulled up.

Pull-Up Control Register 1



Symbol	Address	After Reset
PUR1	00FDh	XX00XX00b

Bit Symbol	Bit Name	Function	RW
PU10	P4_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU11	P4_4 and P4_5 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
— (b3-b2)	Reserved bits	Set to 0.	RW
PU14	P6_0 to P6_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU15	P6_4 to P6_7 pull-up(1)		RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When this bit is set to 1 (pulled up), the pin w hose direction bit is set to 0 (input mode) is pulled up.

Figure 7.11 Registers PUR0 and PUR1

Port Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
	0	0		0	0	0	0

Symbol	Address	After Reset
PMR	00F8h	00h

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Reserved bits	Set to 0.	—
U1PINSEL	Port CLK1/TXD1/RXD1 switch bit	0 : I/O ports P6_5, P6_6, P6_7 1 : CLK1, TXD1, RXD1	RW
— (b6-b5)	Reserved bits	Set to 0.	—
IICSEL	SSU / I²C bus switch bit	0 : Selects SSU function 1 : Selects I²C bus function	RW

Figure 7.12 PMR Register

Port P2 Drive Capacity Control Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
P2DRR	00F4h	00h

Bit Symbol	Bit Name	Function	RW
P2DRR0	P2_0 drive capacity	Set P2 output transistor drive capacity 0 : Low 1 : High(1)	RW
P2DRR1	P2_1 drive capacity		RW
P2DRR2	P2_2 drive capacity		RW
P2DRR3	P2_3 drive capacity		RW
P2DRR4	P2_4 drive capacity		RW
P2DRR5	P2_5 drive capacity		RW
P2DRR6	P2_6 drive capacity		RW
P2DRR7	P2_7 drive capacity		RW

NOTE:
1. Both “H” and “L” output are set to high drive capacity.

Figure 7.13 P2DRR Register

7.4 Port settings

Tables 7.4 to 7.47 list the port settings.

Table 7.4 Port P0_0/AN7

Register	PD0	ADCON0				Function
Bit	PD0_0	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	1	1	1	0	A/D converter input (AN7)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.

Table 7.5 Port P0_1/AN6

Register	PD0	ADCON0				Function
Bit	PD0_1	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	1	1	0	0	A/D converter input (AN6)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.

Table 7.6 Port P0_2/AN5

Register	PD0	ADCON0				Function
Bit	PD0_2	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	1	0	1	0	A/D converter input (AN5)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.

Table 7.7 Port P0_3/AN4

Register	PD0	ADCON0				Function
Bit	PD0_3	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	1	0	0	0	A/D converter input (AN4)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.

Table 7.8 Port P0_4/AN3

Register	PD0	ADCON0				Function
Bit	PD0_4	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	0	1	1	0	A/D converter input (AN3)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.9 Port P0_5/AN2

Register	PD0	ADCON0				Function
Bit	PD0_5	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	0	1	0	0	A/D converter input (AN2)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.10 Port P0_6/AN1

Register	PD0	ADCON0				Function
Bit	PD0_6	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	0	0	1	0	A/D converter input (AN1)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.11 Port P0_7/AN0

Register	PD0	ADCON0				Function
Bit	PD0_7	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	Input port(1)
	1	X	X	X	X	Output port
	0	0	0	0	0	A/D converter input (AN0)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.12 Port P1_0/$\overline{\text{KI0}}$/AN8

Register	PD1	KIEN	ADCON0				Function
Bit	PD1_0	KI0EN	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	X	Input port(1)
	1	X	X	X	X	X	Output port
	0	1	X	X	X	X	$\overline{\text{KI0}}$ input
	0	X	1	0	0	1	A/D converter input (AN8)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 7.13 Port P1_1/$\overline{\text{KI1}}$/AN9

Register	PD1	KIEN	ADCON0				Function
Bit	PD1_1	KI1EN	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	X	Input port(1)
	1	X	X	X	X	X	Output port
	0	1	X	X	X	X	$\overline{\text{KI1}}$ input
	0	X	1	0	1	1	A/D converter input (AN9)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 7.14 Port P1_2/$\overline{KI2}$/AN10

Register	PD1	KIEN	ADCON0				Function
Bit	PD1_2	KI2EN	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	X	Input port(1)
	1	X	X	X	X	X	Output port
	0	1	X	X	X	X	$\overline{KI2}$ input
	0	X	1	1	0	1	A/D converter input (AN10)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 7.15 Port P1_3/$\overline{KI3}$/AN11

Register	PD1	KIEN	ADCON0				Function
Bit	PD1_3	KI3EN	CH2	CH1	CH0	ADGSEL0	
Setting Value	0	X	X	X	X	X	Input port(1)
	1	X	X	X	X	X	Output port
	0	1	X	X	X	X	$\overline{KI3}$ input
	0	X	1	1	1	1	A/D converter input (AN11)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 7.16 Port P1_4/TXD0

Register	PD1	U0MR			Function
Bit	PD1_4	SMD2	SMD1	SMD0	
Setting Value	0	0	0	0	Input port(1)
	1	0	0	0	Output port
	X	0	0	1	TXD0 output(2)
		1	0	0	
		1	0	1	
		1	1	0	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. N-channel open drain output by setting the NCH bit in the U0C0 register to 1.

Table 7.17 Port P1_5/RXD0/(TRAIO)/($\overline{INT1}$)

Register	PD1	TRAIOC		TRAMR			INTEN	Function
Bit	PD1_5	TIOSEL	TOPCR	TMOD2	TMOD1	TMOD0	INT1EN	
Setting Value	0	0	X	X	X	X	X	Input port(1)
		X	1	X	X	X		
		X	X	Other than 001b				
	1	0	X	X	X	X	X	Output port
		X	1	X	X	X		
		X	X	Other than 001b				
	0	X	X	Other than 001b			X	RXD0 input
		0		0	0	1		
	0	1	X	Other than 001b			X	TRAIO input
	0	1	X	Other than 001b			1	TRAIO/$\overline{INT1}$ input
	X	1	0	0	0	1	X	TRAIO pulse output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.

Table 7.18 Port P1_6/CLK0

Register	PD1	U0MR				Function
Bit	PD1_6	SMD2	SMD1	SMD0	CKDIR	
Setting Value	0	Other than 001b			X	Input port(1)
		X	X	X	1	
	1	Other than 001b			X	Output port
	0	X	X	X	1	CLK0 (external clock) input
	X	0	0	1	0	CLK0 (internal clock) output

X: 0 or 1

NOTE:

1. Pulled up by setting the PU03 bit in the PUR0 register to 1.

Table 7.19 Port P1_7/TRAIO/$\overline{\text{INT1}}$

Register	PD1	TRAIOC		TRAMR			INTEN	Function
Bit	PD1_7	TIOSEL	TOPCR	TMOD2	TMOD1	TMOD0	INT1EN	
Setting Value	0	1	X	X	X	X	X	Input port(1)
		X	1	X	X	X		
		X	X	Other than 001b				
	1	1	X	X	X	X	X	Output port
		X	1	X	X	X		
		X	X	Other than 001b				
	0	0	X	Other than 001b			X	TRAIO input
	0	0	X	Other than 001b			1	TRAIO/$\overline{\text{INT1}}$ input
	X	0	0	0	0	1	X	TRAIO pulse output

X: 0 or 1

NOTE:

1. Pulled up by setting the PU03 bit in the PUR0 register to 1.

Table 7.20 Port P2_0/TRDIOA0/TRDCLK

Register	PD2	TRDOER1	TRDFCR				TRDIORA0			Function
Bit	PD2_0	EA0	CMD1	CMD0	STCLK	PWM3	IOA2	IOA1	IOA0	
Setting Value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port(2)
	0	X	0	0	0	1	1	X	X	Timer mode (input capture function)
	0	X	X	X	1	1	0	0	0	External clock input (TRDCLK)
	X	0	0	0	0	0	X	X	X	PWM3 mode waveform output(2)
	X	0	0	0	0	1	0	0	1	Timer mode waveform output (output compare function)(2)
							0	1	X	

X: 0 or 1

NOTES:

1. Pulled up by setting the PU04 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P2DRR0 bit in the P2DRR register to 1.

Table 7.21 Port P2_1/TRDIOB0

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORA0			Function
Bit	PD2_1	EB0	CMD1	CMD0	PWM3	PWMB0	IOB2	IOB1	IOB0	
Setting Value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port(2)
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	X	0	0	0	0	X	X	X	X	PWM3 mode waveform output(2)
	X	0	0	0	1	1	X	X	X	PWM mode waveform output(2)
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)(2)
							0	1	X	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU04 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P2DRR1 bit in the P2DRR register to 1.

Table 7.22 Port P2_2/TRDIOC0

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORC0			Function
Bit	PD2_2	EC0	CMD1	CMD0	PWM3	PWMC0	IOC2	IOC1	IOC0	
Setting Value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port(2)
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output(2)
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output(2)
	X	0	0	0	1	1	X	X	X	PWM mode waveform output(2)
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)(2)
							0	1	X	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU04 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P2DRR2 bit in the P2DRR register to 1.

Table 7.23 Port P2_3/TRDIOD0

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORC0			Function
Bit	PD2_3	ED0	CMD1	CMD0	PWM3	PWMD0	IOD2	IOD1	IOD0	
Setting Value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port(2)
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output(2)
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output(2)
	X	0	0	0	1	1	X	X	X	PWM mode waveform output(2)
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)(2)
							0	1	X	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU04 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P2DRR3 bit in the P2DRR register to 1.

Table 7.24 Port P2_4/TRDIOA1

Register	PD2	TRDOER1	TRDFCR			TRDIORA1			Function
Bit	PD2_4	EA1	CMD1	CMD0	PWM3	IOA2	IOA1	IOA0	
Setting Value	0	1	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	Output port(2)
	0	X	0	0	1	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	Complementary PWM mode waveform output(2)
			1	1					
	X	0	0	1	X	X	X	X	Reset synchronous PWM mode waveform output(2)
	X	0	0	0	1	0	0	1	Timer mode waveform output (output compare function)(2)
						0	1	X	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU05 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P2DRR4 bit in the P2DRR register to 1.

Table 7.25 Port P2_5/TRDIOB1

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORA1			Function
Bit	PD2_5	EB1	CMD1	CMD0	PWM3	PWMB1	IOB2	IOB1	IOB0	
Setting Value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port(2)
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output(2)
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output(2)
	X	0	0	0	1	1	X	X	X	PWM mode waveform output(2)
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)(2)
							0	1	X	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU05 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P2DRR5 bit in the P2DRR register to 1.

Table 7.26 Port P2_6/TRDIOC1

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORC1			Function
Bit	PD2_6	EC1	CMD1	CMD0	PWM3	PWMC1	IOC2	IOC1	IOC0	
Setting Value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port(2)
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output(2)
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output(2)
	X	0	0	0	1	1	X	X	X	PWM mode waveform output(2)
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)(2)
							0	1	X	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU05 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P2DRR6 bit in the P2DRR register to 1.

Table 7.27 Port P2_7/TRDIOD1

Register	PD2	TRDOER1	TRDFCR			TRDPMR	TRDIORC1			Function
Bit	PD2_7	ED1	CMD1	CMD0	PWM3	PWMD1	IOD2	IOD1	IOD0	
Setting Value	0	1	X	X	X	X	X	X	X	Input port(1)
	1	1	X	X	X	X	X	X	X	Output port(2)
	0	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	X	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output(2)
			1	1						
	X	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output(2)
	X	0	0	0	1	1	X	X	X	PWM mode waveform output(2)
	X	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)(2)
							0	1	X	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU05 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P2DRR7 bit in the P2DRR register to 1.

Table 7.28 Port P3_0/TRAO

Register	PD3	TRAIOC	Function
Bit	PD3_0	TOENA	
Setting Value	0	0	Input port(1)
	1	0	Output port
	X	1	TRAO output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.

Table 7.29 Port P3_1/TRBO

Register	PD3	TRBMR		TRBIOC	Function
Bit	PD3_1	TMOD1	TMOD0	TOCNT	
Setting Value	0	0	0	X	Input port(1)
	1	0	0	X	Output port
	X	01b		1	
	X	Other than 00b		0	TRBO output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.

Table 7.30 Port P3_3/SSI

Register	PD3	Clock Synchronous Serial I/O with Chip Select (Refer to **Table 16.4 Association between Communication Modes and I/O Pins**.)		PMR	Function
Bit	PD3_3	SSI output control	SSI input control	IICSEL	
Setting Value	0	0	0	0	Input port(1)
		X	X	1	
	1	0	0	0	Output port(2)
		X	X	1	
	X	0	1	0	SSI input
	X	1	0	0	SSI output(2)

X: 0 or 1
NOTES:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. N-channel open drain output by setting the SOOS bit in the SSMR2 register to 1 when this pin functions as output.

Table 7.31 Port P3_4/SDA/$\overline{SCS}$

Register	PD3	SSMR2		PMR	ICCR1	Function
Bit	PD3_4	CSS1	CSS0	IICSEL	ICE	
Setting Value	0	0	0	0	X	Input port(1)
	0	0	0	X	0	
	1	0	0	0	X	Output port(2)
	1	0	0	X	0	
	X	0	1	0	X	$\overline{SCS}$ input
	X	1	0	0	X	$\overline{SCS}$ output(2)
		1	1			
	X	X	X	1	1	SDA input/output

X: 0 or 1
NOTES:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. N-channel open drain output by setting the CSOS bit in the SSMR2 register to 1 when this pin functions as output.

Table 7.32 Port P3_5/SCL/SSCK

Register	PD3	Clock Synchronous Serial I/O with Chip Select (Refer to **Table 16.4 Association between Communication Modes and I/O Pins**.)		PMR	ICCR1	Function
Bit	PD3_5	SSCK output control	SSCK input control	IICSEL	ICE	
Setting Value	0	0	0	0	X	Input port(1)
	0	0	0	X	0	
	1	0	0	0	X	Output port(2)
	1	0	0	X	0	
	X	0	1	0	0	SSCK input
	X	1	0	0	0	SSCK output(2)
	X	1	0	1	1	SCL input/output

X: 0 or 1
NOTES:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. N-channel open drain output by setting the CSOS bit in the SSMR2 register to 1 when this pin functions as output.

Table 7.33 Port P3_7/SSO

Register	PD3	Clock Synchronous Serial I/O with Chip Select (Refer to **Table 16.4 Association between Communication Modes and I/O Pins**.)		SSMR2	PMR	Function
Bit	PD3_7	SSO output control	SSO input control	SOOS	IICSEL	
Setting Value	0	0	0	X	0	Input port(1)
	0	X	X	X	1	
	1	0	0	0	0	Output port
	1	X	X	0	1	
	X	0	1	0	0	SSO input
	X	1	0	0	0	SSO output (CMOS output)
	X	1	0	1	0	SSO output (N-channel open-drain output)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.

Table 7.34 Port P4_2/VREF

Register	ADCON1	Function
Bit	VCUT	
Setting Value	0	Input port
	1	Input port/VREF input

Table 7.35 Port P4_3/XCIN

Register	PD4	CM0	CM1		Circuit specifications		Function
Bit	PD4_3	CM04	CM10	CM12	Oscillation buffer	Feedback resistor	
Setting Value	0	0	X	X	OFF	OFF	Input port(1)
	1	0	X	X	OFF	OFF	Output port
	X	1	0	0	ON	ON	XCIN-XCOUT oscillation (on-chip feedback resistor enabled)
	X	1	0	1	ON	OFF	XCIN-XCOUT oscillation (on-chip feedback resistor disabled)
	X	1	1	0	OFF	ON	XCIN-XCOUT oscillation stop
				1	OFF	OFF	
	X	1	0	0	ON	ON	External XCIN input
				1	ON	OFF	

X: 0 or 1

NOTE:

1. Pulled up by setting the PU10 bit in the PUR1 register to 1.

Table 7.36 Port P4_4/XCOUT

Register	PD4	CM0	CM1		Circuit specifications		Function
Bit	PD4_4	CM04	CM10	CM12	Oscillation buffer	Feedback resistor	
Setting Value	0	0	X	X	OFF	OFF	Input port(1)
	1	0	X	X	OFF	OFF	Output port
	X	1	0	0	ON	ON	XCIN-XCOUT oscillation (on-chip feedback resistor enabled)
	X	1	0	1	ON	OFF	XCIN-XCOUT oscillation (on-chip feedback resistor disabled)
	X	1	1	0	OFF	ON	XCIN-XCOUT oscillation stop
				1	OFF	OFF	
	X	1	0	0	ON	ON	External XCOUT output (inverted output of XCIN)(2)
				1	ON	OFF	

X: 0 or 1

NOTES:

1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Since the XCIN-XCOUT oscillation buffer operates with internal step-down power, the XCOUT output level cannot be used as the CMOS level signal directly.

Table 7.37 Port P4_5/$\overline{\text{INT0}}$

Register	PD4	INTEN	Function
Bit	PD4_5	INT0EN	
Setting Value	0	X	Input port(1)
	1	X	Output port
	0	1	$\overline{\text{INT0}}$ input

X: 0 or 1

NOTE:

1. Pulled up by setting the PU11 bit in the PUR1 register to 1.

Table 7.38 Port P4_6/XIN

Register	CM1		CM0	Circuit specifications		Function
Bit	CM13	CM10	CM05	Oscillation buffer	Feedback resistor	
Setting Value	0	X	X	OFF	OFF	Input port
	1	0	0	ON	ON	XIN-XOUT oscillation
	1	0	1	OFF	ON	External XIN input
	1	1	0	OFF	OFF	XIN-XOUT oscillation stop
	1	1	1	OFF	OFF	XIN-XOUT oscillation stop

X: 0 or 1

Table 7.39 Port P4_7/XOUT

Register	CM1		CM0	Circuit specifications		Function
Bit	CM13	CM10	CM05	Oscillation buffer	Feedback resistor	
Setting Value	0	X	X	OFF	OFF	Input port
	1	0	0	ON	ON	XIN-XOUT oscillation
	1	0	1	OFF	ON	XOUT is “H” pull-up
	1	1	0	OFF	OFF	XIN-XOUT oscillation stop
	1	1	1	OFF	OFF	XIN-XOUT oscillation stop

X: 0 or 1

Table 7.40 Port P6_0/TREO

Register	PD6	TRECR1	Function
Bit	PD6_0	TOENA	
Setting Value	0	0	Input port(1)
	1	0	Output port
	X	1	TREO output

X: 0 or 1

NOTE:

1. Pulled up by setting the PU14 bit in the PUR1 register to 1.

Table 7.41 Port P6_1

Register	PD6	Function
Bit	PD6_1	
Setting Value	0	Input port(1)
	1	Output port

NOTE:

1. Pulled up by setting the PU14 bit in the PUR1 register to 1.

Table 7.42 Port P6_2

Register	PD6	Function
Bit	PD6_2	
Setting Value	0	Input port(1)
	1	Output port

NOTE:

1. Pulled up by setting the PU14 bit in the PUR1 register to 1.

Table 7.43 Port P6_3

Register	PD6	Function
Bit	PD6_3	
Setting Value	0	Input port(1)
	1	Output port

NOTE:

1. Pulled up by setting the PU14 bit in the PUR1 register to 1.

Table 7.44 Port P6_4

Register	PD6	Function
Bit	PD6_4	
Setting Value	0	Input port(1)
	1	Output port

NOTE:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.

Table 7.45 Port P6_5/CLK1

Register	PD6	PMR	U1MR				Function
Bit	PD6_5	U1PINSEL	SMD2	SMD1	SMD0	CKDIR	
Setting Value	0	X	Other than 001b			X	Input port(1)
		0	X	X	X	X	
		X	X	X	X	1	
	1	X	Other than 001b			X	Output port
		0	X	X	X		
		X	X	X	X	0	
	0	1	X	X	X	1	CLK1 (external clock) input
	X	1	0	0	1	0	CLK1 (internal clock) output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.

Table 7.46 Port P6_6/$\overline{\text{INT2}}$/TXD1

Register	PD6	PMR	U1MR			U1C0	INTEN	Function
Bit	PD6_6	U1PINSEL	SMD2	SMD1	SMD0	NCH	INT2EN	
Setting Value	0	X	0	0	0	X	X	Input port(1)
		0	X	X	X			
	1	X	0	0	0	X	X	Output port
		0	X	X	X			
	0	X	X	X	X	X	1	$\overline{\text{INT2}}$ input
	X	1	0	0	1	0	X	TXD1 output (CMOS output)
			1	0	0			
			1	0	1			
			1	1	0			
	X	1	0	0	1	1	X	TXD1 output (N-channel open-drain output)
			1	0	0			
			1	0	1			
			1	1	0			

X: 0 or 1
NOTE:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.

Table 7.47 Port P6_7/$\overline{\text{INT3}}$/RXD1

Register	PD6	PMR	INTEN	Function
Bit	PD6_7	U1PINSEL	INT3EN	
Setting Value	0	X	X	Input port(1)
	1	X	X	Output port
	0	X	1	$\overline{\text{INT3}}$ input
	0	1	X	RXD1 input

X: 0 or 1
NOTE:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.

7.5 Unassigned Pin Handling

Table 7.48 lists the Unassigned Pin Handling.

Table 7.48 Unassigned Pin Handling

Pin Name	Connection
Ports P0 to P2, P3_0, P3_1, P3_3 to P3_7, P4_3 to P4_5, P6	• After setting to input mode, connect each pin to VSS via a resistor (pull-down) or connect each pin to VCC via a resistor (pull-up).(2) • After setting to output mode, leave these pins open.(1,2)
Ports P4_6, P4_7	Connect to VCC via a pull-up resistor(2)
Port P4_2, VREF	Connect to VCC
$\overline{\text{RESET}}$ (3)	Connect to VCC via a pull-up resistor(2)
NC	Open or Connect to VCC and VSS

NOTES:
1. If these ports are set to output mode and left open, they remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be undefined and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. In order to enhance program reliability, the program should periodically repeat the setting of the direction registers.
2. Connect these unassigned pins to the MCU using the shortest wire length (2 cm or less) possible.
3. When the power-on reset function is in use.

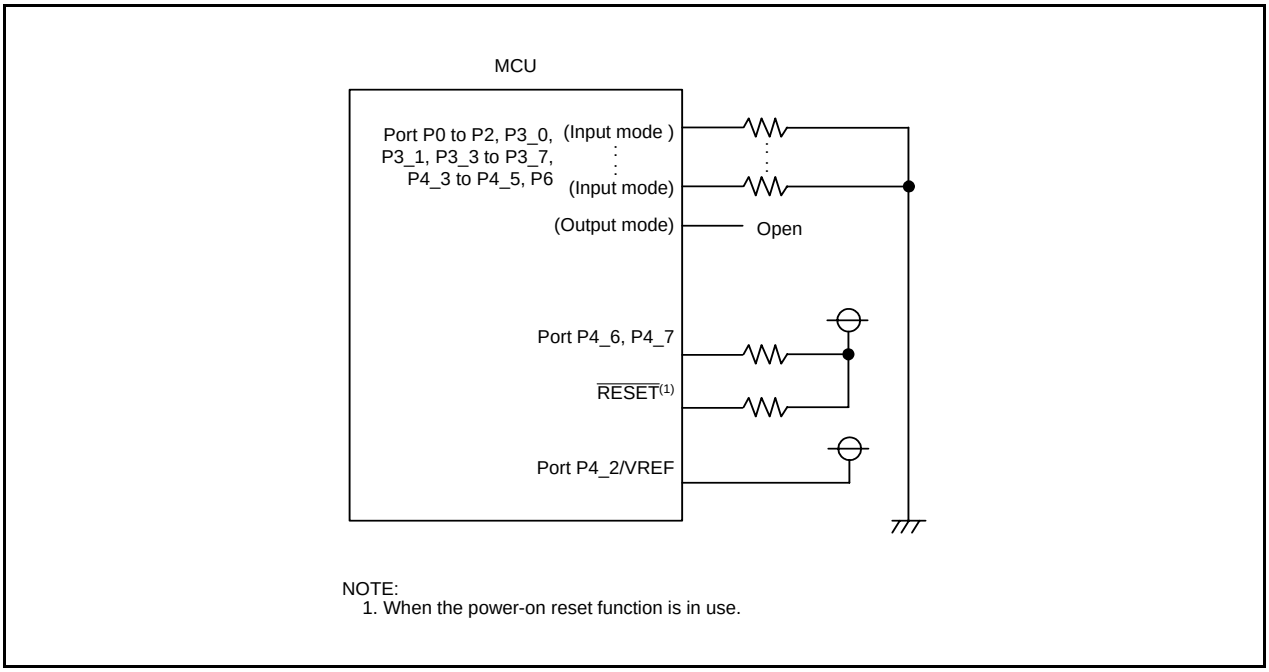


Figure 7.14 Unassigned Pin Handling

8. Processor Mode

8.1 Processor Modes

Single-chip mode can be selected as the processor mode.
Table 8.1 lists Features of Processor Mode. Figure 8.1 shows the PM0 Register and Figure 8.2 shows the PM1 Register.

Table 8.1 Features of Processor Mode

Processor Mode	Accessible Areas	Pins Assignable as I/O Port Pins
Single-chip mode	SFR, internal RAM, internal ROM	All pins are I/O ports or peripheral function I/O pins

Processor Mode Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	0	0	0

Symbol	Address	After Reset
PM0	0004h	00h

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0.	RW
PM03	Software reset bit	The MCU is reset when this bit is set to 1. When read, the content is 0.	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Set the PRC1 bit in the PRCR register to 1 (write enable) before rewriting the PM0 register.

Figure 8.1 PM0 Register

Processor Mode Register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	X	X	X	X	X	0	0

Symbol	Address	After Reset
PM1	0005h	00h

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0.	RW
PM12	WDT interrupt/reset switch bit	0 : Watchdog timer interrupt 1 : Watchdog timer reset(2)	RW
— (b6-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
— (b7)	Reserved bit	Set to 0.	RW

NOTES:
1. Set the PRC1 bit in the PRCR register to 1 (write enable) before rewriting the PM1 register.
2. The PM12 bit is set to 1 by a program (and remains unchanged even if 0 is written to it).
When the CSPRO bit in the CSPR register is set to 1 (count source protect mode enabled), the PM12 bit is automatically set to 1.

Figure 8.2 PM1 Register

9. Bus

The bus cycles differ when accessing ROM/RAM, and when accessing SFR.
Table 9.1 lists Bus Cycles by Access Space of the R8C/24 Group and Table 9.2 lists Bus Cycles by Access Space of the R8C/25 Group.
ROM/RAM and SFR are connected to the CPU by an 8-bit bus. When accessing in word (16-bit) units, these areas are accessed twice in 8-bit units.
Table 9.3 lists Access Units and Bus Operations.

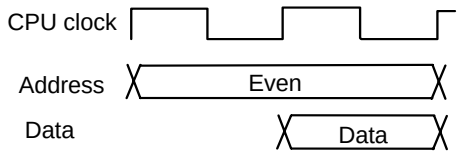
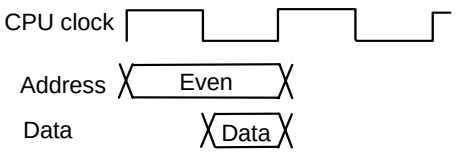
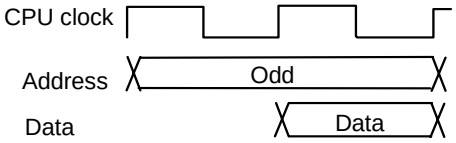
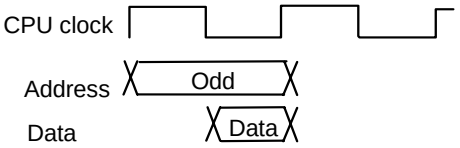
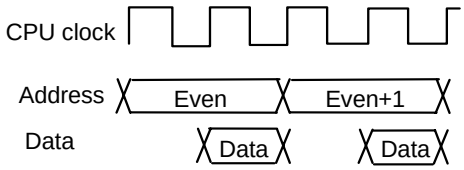
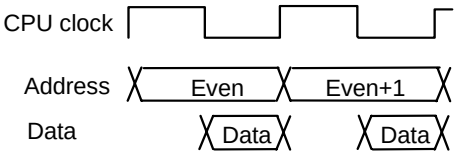
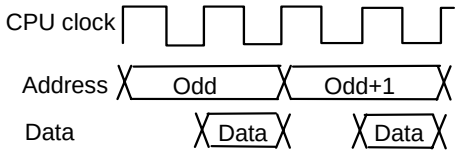
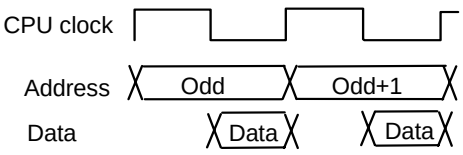
Table 9.1 Bus Cycles by Access Space of the R8C/24 Group

Access Area	Bus Cycle
SFR	2 cycles of CPU clock
ROM/RAM	1 cycle of CPU clock

Table 9.2 Bus Cycles by Access Space of the R8C/25 Group

Access Area	Bus Cycle
SFR/Data flash	2 cycles of CPU clock
Program ROM/RAM	1 cycle of CPU clock

Table 9.3 Access Units and Bus Operations

Area	SFR, data flash	ROM (program ROM), RAM
Even address Byte access		
Odd address Byte access		
Even address Word access		
Odd address Word access		

However, only following SFRs are connected with the 16-bit bus:
Timer RD: registers TRDi (i = 0,1), TRDGRAi, TRDGRBi, TRDGRCi, and TRDGRDi
Therefore, they are accessed once in 16-bit units. The bus operation is the same as “Area: SFR, data flash, even address byte access” in Table 9.3 Access Units and Bus Operations, and 16-bit data is accessed at a time.

10. Clock Generation Circuit

The clock generation circuit has:

- XIN clock oscillation circuit
- XCIN clock oscillation circuit
- Low-speed on-chip oscillator
- High-speed on-chip oscillator

Table 10.1 lists the Specifications of Clock Generation Circuit. Figure 10.1 shows a Clock Generation Circuit. Figures 10.2 to 10.8 show clock associated registers. Figure 10.9 shows the Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit.

Table 10.1 Specifications of Clock Generation Circuit

Item	XIN Clock Oscillation Circuit	XCIN Clock Oscillation Circuit	On-Chip Oscillator	
			High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator
Applications	• CPU clock source • Peripheral function clock source	• CPU clock source • Timer RA and timer RE clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when XIN clock stops oscillating	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when XIN clock stops oscillating
Clock frequency	0 to 20 MHz	32.768 kHz	Approx. 40 MHz(4)	Approx. 125 kHz
Connectable oscillator	• Ceramic resonator • Crystal oscillator	• Crystal oscillator	–	–
Oscillator connect pins	XIN, XOUT(1)	XCIN, XCOUT(2)	–(1)	–(1)
Oscillation stop, restart function	Usable	Usable	Usable	Usable
Oscillator status after reset	Stop	Stop	Stop	Oscillate
Others	Externally generated clock can be input(3)	• Externally generated clock can be input • On-chip feedback resistor Rf (connected/ not connected, selectable)	–	–

NOTES:

1. These pins can be used as P4_6 or P4_7 when using the on-chip oscillator clock as the CPU clock while the XIN clock oscillation circuit is not used.
2. These pins can be used as P4_3 and P4_4 when using the XIN clock oscillation circuit and on-chip oscillator clock for a CPU clock while the XCIN clock oscillation circuit is not used.
3. Set the CM05 bit in the CM0 register to 1 (XIN clock stopped) and the CM13 bit in the CM1 register to 1 (XIN-XOUT pin) when an external clock is input.
4. The clock frequency is automatically set to up to 20 MHz by a divider when using the high-speed on-chip oscillator as the CPU clock source.

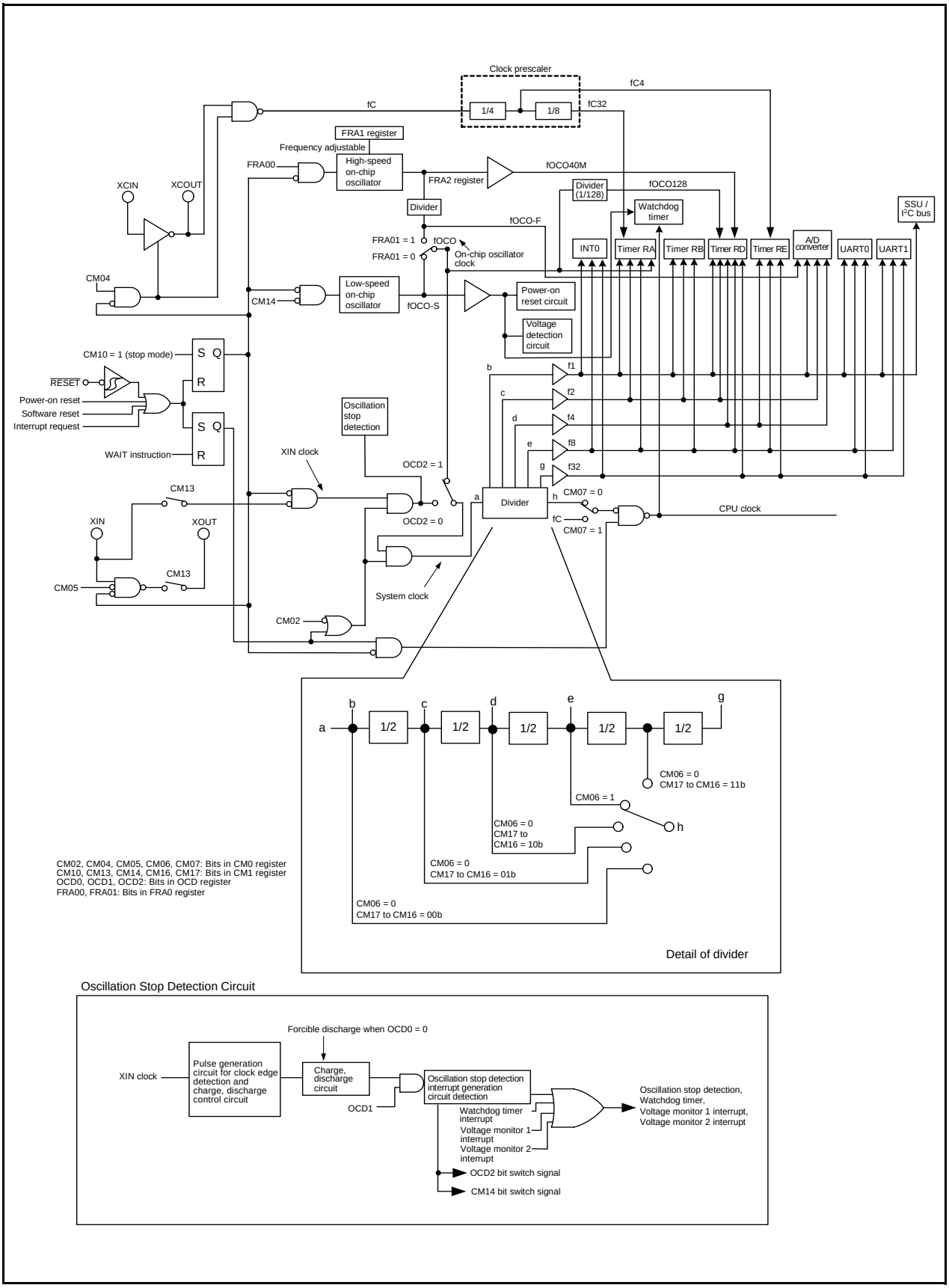
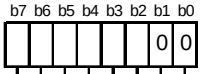


Figure 10.1 Clock Generation Circuit

System Clock Control Register 0(1)



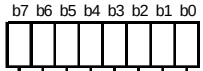
Symbol	Address	After Reset
CM0	0006h	01101000b

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0.	RW
CM02	WAIT peripheral function clock stop bit	0 : Peripheral function clock does not stop in wait mode 1 : Peripheral function clock stops in wait mode	RW
CM03	XCIN-XCOUT drive capacity select bit(9)	0 : Low 1 : High	RW
CM04	Port, XCIN-XCOUT switch bit(6)	0 : I/O port P4_3, P4_4 1 : XCIN-XCOUT pin(7)	RW
CM05	XIN clock (XIN-XOUT) stop bit(2, 4)	0 : XIN clock oscillates 1 : XIN clock stops(3)	RW
CM06	System clock division select bit 0(5)	0 : CM16, CM17 enabled 1 : Divide-by-8 mode	RW
CM07	CPU clock select bit(8)	0 : System clock 1 : XCIN clock	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the CM0 register.
2. The CM05 bit stops the XIN clock when the high-speed on-chip oscillator mode, low-speed on-chip oscillator mode is selected. Do not use this bit to detect whether the XIN clock is stopped. To stop the XIN clock, set the bits in the following order:
   (a) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (b) Set the OCD2 bit to 1 (selects on-chip oscillator clock).
3. During external clock input, only the clock oscillation buffer is turned off and clock input is acknowledged.
4. When the CM05 bit is set to 1 (XIN clock stopped) and the CM13 bit in the CM1 register is set to 0 (P4_6, P4_7), P4_6 and P4_7 can be used as input ports.
5. When entering stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
6. The CM04 bit can be set to 1 by a program but cannot be set to 0.
7. To use the XCIN clock, set the CM04 bit to 1. Also, set ports P4_3 and P4_4 as input ports without pull-up.
8. Set the CM07 bit to 1 from 0 (XCIN clock) after setting the CM04 bit to 1 (XCIN-XCOUT pin) and allowing XCIN clock oscillation to stabilize.
9. The MCU enters stop mode, the CM03 bit is set to 1 (high). Rewrite the CM03 bit while the XCIN clock oscillation stabilizes.

Figure 10.2 CM0 Register

System Clock Control Register 1(1)



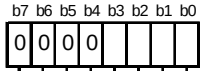
Symbol	Address	After Reset
CM1	0007h	00100000b

Bit Symbol	Bit Name	Function	RW
CM10	All clock stop control bit(4, 7, 8)	0 : Clock operates 1 : Stops all clocks (stop mode)	RW
CM11	XIN-XOUT on-chip feedback resistor select bit	0 : On-chip feedback resistor enabled 1 : On-chip feedback resistor disabled	RW
CM12	XCIN-XCOUT on-chip feedback resistor select bit	0 : On-chip feedback resistor enabled 1 : On-chip feedback resistor disabled	RW
CM13	Port XIN-XOUT switch bit(7, 9)	0 : Input ports P4_6, P4_7 1 : XIN-XOUT pin	RW
CM14	Low-speed on-chip oscillation stop bit(5, 6, 8)	0 : Low-speed on-chip oscillator on 1 : Low-speed on-chip oscillator off	RW
CM15	XIN-XOUT drive capacity select bit(2)	0 : Low 1 : High	RW
CM16	System clock division select bits 1(3)	b7 b6 0 0 : No division mode 0 1 : Divide-by-2 mode 1 0 : Divide-by-4 mode 1 1 : Divide-by-16 mode	RW
CM17			RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the CM1 register.
2. When entering stop mode, the CM15 bit is set to 1 (drive capacity high).
3. When the CM06 bit is set to 0 (bits CM16, CM17 enabled), bits CM16 to CM17 are enabled.
4. If the CM10 bit is set to 1 (stop mode), the on-chip feedback resistor is disabled.
5. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit is set to 1 (low-speed on-chip oscillator stopped). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
6. When using the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when using the digital filter), set the CM14 bit to 0 (low-speed on-chip oscillator on).
7. When the CM10 bit is set to 1 (stop mode) and the CM13 bit is set to 1 (XIN-XOUT pin), the XOUT (P4_7) pin goes “H”. When the CM13 bit is set to 0 (input ports, P4_6, P4_7), P4_7 (XOUT) enters input mode.
8. In count source protect mode (Refer to **13.2 Count Source Protection Mode Enabled**), the value remains unchanged even if bits CM10 and CM14 are set.
9. Once the CM13 bit is set to 1 by a program, it cannot be set to 0.

Figure 10.3 CM1 Register

Oscillation Stop Detection Register(1)



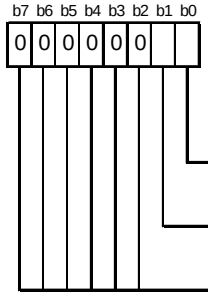
Symbol	Address	After Reset
OCD	000Ch	00000100b

Bit Symbol	Bit Name	Function	RW
OCD0	Oscillation stop detection enable bit(7)	0 : Oscillation stop detection function disabled(2) 1 : Oscillation stop detection function enabled	RW
OCD1	Oscillation stop detection interrupt enable bit	0 : Disabled(2) 1 : Enabled	RW
OCD2	System clock select bit(4)	0 : Selects XIN clock(7) 1 : Selects on-chip oscillator clock(3)	RW
OCD3	Clock monitor bit(5, 6)	0 : XIN clock oscillates 1 : XIN clock stops	RO
— (b7-b4)	Reserved bits	Set to 0.	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting to the OCD register.
2. Set bits OCD1 to OCD0 to 00b before entering stop mode, high-speed on-chip oscillator mode, or low-speed on-chip oscillator mode (XIN clock stops).
3. The CM14 bit is set to 0 (low-speed on-chip oscillator on) if the OCD2 bit is set to 1 (on-chip oscillator clock selected).
4. The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) if a XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. If the OCD3 bit is set to 1 (XIN clock stopped), the OCD2 bit remains unchanged even when set to 0 (XIN clock selected).
5. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled).
6. The OCD3 bit remains 0 (XIN clock oscillates) if bits OCD1 to OCD0 are set to 00b.
7. Refer to **Figure 10.16 Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock** for the switching procedure when the XIN clock re-oscillates after detecting an oscillation stop.

Figure 10.4 OCD Register

High-Speed On-Chip Oscillator Control Register 0(1)



Symbol	Address	After Reset
FRA0	0023h	00h

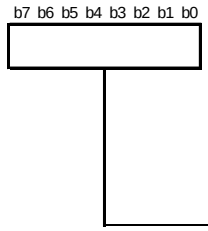
Bit Symbol	Bit Name	Function	RW
FRA00	High-speed on-chip oscillator enable bit	0 : High-speed on-chip oscillator off 1 : High-speed on-chip oscillator on	RW
FRA01	High-speed on-chip oscillator select bit(2)	0 : Selects low-speed on-chip oscillator(3) 1 : Selects high-speed on-chip oscillator	RW
— (b7-b2)	Reserved bits	Set to 0.	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the FRA0 register.
2. Change the FRA01 bit under the following conditions.
   • FRA00 = 1 (high-speed on-chip oscillation)
   • The CM14 bit in the CM1 register = 0 (low-speed on-chip oscillator on)
   • Bits FRA22 to FRA20 in the FRA2 register:

All divide ratio mode settings are supported when VCC = 3.0 V to 5.5 V	000b to 111b
Divide ratio of 4 or more when VCC = 2.7 V to 5.5 V	010b to 111b (divide by 4 or more)
Divide ratio of 8 or more when VCC = 2.2 V to 5.5 V	110b to 111b (divide by 8 or more)

3. When setting the FRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) at the same time.
   Set the FRA00 bit to 0 after setting the FRA01 bit to 0.

High-Speed On-Chip Oscillator Control Register 1(1)



Symbol	Address	After Reset
FRA1	0024h	When Shipping

Function	RW
The frequency of the high-speed on-chip oscillator is adjusted with bits 0 to 7. High-speed on-chip oscillator frequency = 40 MHz (FRA1 register = value when shipping) Setting the FRA1 register to a lower value results in a higher frequency. Setting the FRA1 register to a higher value results in a lower frequency.(2)	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the FRA1 register.
2. When changing the values of the FRA1 register, adjust the FRA1 register so that the frequency of the high-speed on-chip oscillator clock will be 40 MHz or less.

Figure 10.5 Registers FRA0 and FRA1

High-Speed On-Chip Oscillator Control Register 2(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0			

Symbol	Address	After Reset
FRA2	0025h	00h

Bit Symbol	Bit Name	Function	RW
FRA20	High-speed on-chip oscillator frequency switching bits	Selects the dividing ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode 0 0 1: Divide-by-3 mode 0 1 0: Divide-by-4 mode 0 1 1: Divide-by-5 mode 1 0 0: Divide-by-6 mode 1 0 1: Divide-by-7 mode 1 1 0: Divide-by-8 mode 1 1 1: Divide-by-9 mode	RW
FRA21			RW
FRA22			RW
— (b7-b3)	Reserved bits	Set to 0.	RW

NOTE:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the FRA2 register.

High-Speed On-Chip Oscillator Control Register 4

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
FRA4	0029h	When Shipping

Function	RW
Stores data for frequency correction when VCC = 2.7 to 5.5 V. (The value is the same as that of the FRA1 register after a reset.) Optimal frequency correction to match the voltage conditions can be achieved by transferring this value to the FRA1 register.	RO

High-Speed On-Chip Oscillator Control Register 6

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
FRA6	002Bh	When Shipping

Function	RW
Stores data for frequency correction when VCC = 2.2 to 5.5 V. Optimal frequency correction to match the voltage conditions can be achieved by transferring this value to the FRA1 register.	RO

High-Speed On-Chip Oscillator Control Register 7

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
FRA7	002Ch	When Shipping

Function	RW
36.864 MHz frequency correction data is stored. The oscillation frequency of the high-speed on-chip oscillator can be adjusted to 36.864 MHz by transferring this value to the FRA1 register.	RO

Figure 10.6 Registers FRA2, FRA4, FRA6 and FRA7

Clock Prescaler Reset Flag

b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	0	0	0	0

Symbol	Address	After Reset
CPSRF	0028h	00h

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Reserved bits	Set to 0.	RW
CPSR	Clock prescaler reset flag(1)	Setting this bit to 1 initializes the clock prescaler. (When read, the content is 0)	RW

NOTE:
1. Only write 1 to this bit when selecting the XCIN clock as the CPU clock, .

Figure 10.7 CPSRF Register

Voltage Detection Register 2(1)

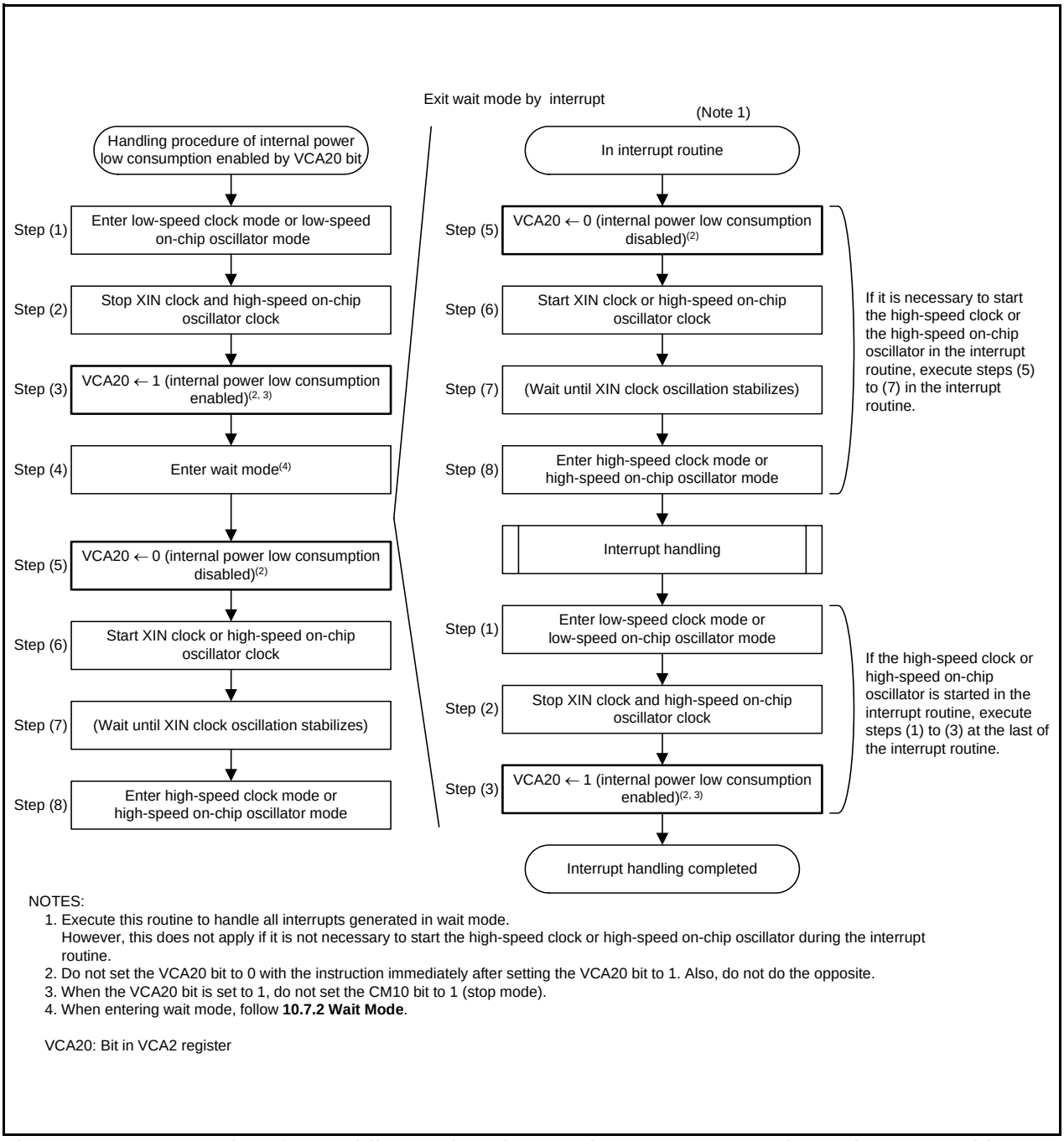
b7	b6	b5	b4	b3	b2	b1	b0
			0	0	0	0	

Symbol	Address	After Reset(5)
VCA2	0032h	The LVD0ON bit in the OFS register is set to 1 and hardware reset : 00h Power-on reset, voltage monitor 0 reset or LVD0ON bit in the OFS register is set to 0, and hardware reset : 00100000b

Bit Symbol	Bit Name	Function	RW
VCA20	Internal power low consumption enable bit(6)	0 : Disables low consumption 1 : Enables low consumption	RW
— (b4-b1)	Reserved bits	Set to 0.	RW
VCA25	Voltage detection 0 enable bit(2)	0 : Voltage detection 0 circuit disabled 1 : Voltage detection 0 circuit enabled	RW
VCA26	Voltage detection 1 enable bit(3)	0 : Voltage detection 1 circuit disabled 1 : Voltage detection 1 circuit enabled	RW
VCA27	Voltage detection 2 enable bit(4)	0 : Voltage detection 2 circuit disabled 1 : Voltage detection 2 circuit enabled	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enable) before writing to the VCA2 register.
2. To use the voltage monitor 0 reset, set the VCA25 bit to 1.
   After the VCA25 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
3. To use the voltage monitor 1 interrupt/reset or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1.
   After the VCA26 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
4. To use the voltage monitor 2 interrupt/reset or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1.
   After the VCA27 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect this register.
6. Use the VCA20 bit only when entering to wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 10.9 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit**.

Figure 10.8 VCA2 Register



NOTES:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the high-speed clock or high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When entering wait mode, follow **10.7.2 Wait Mode**.

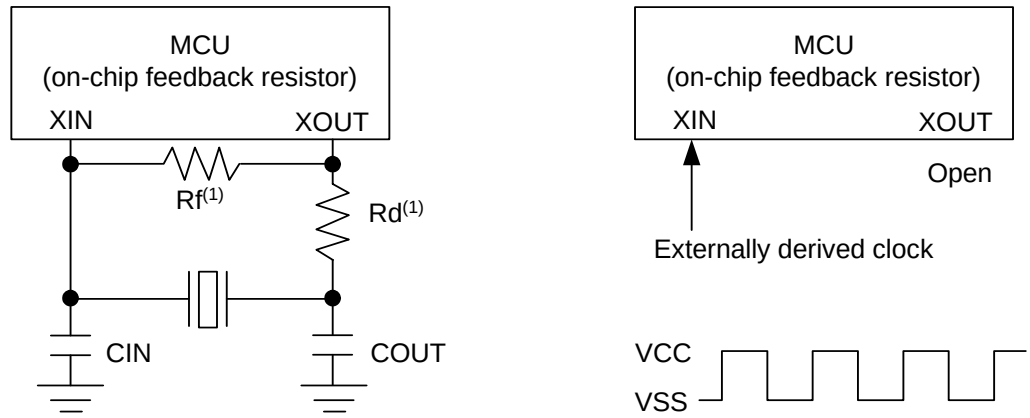
VCA20: Bit in VCA2 register

Figure 10.9 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit

The clocks generated by the clock generation circuits are described below.

10.1 XIN Clock

This clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XIN clock oscillation circuit is configured by connecting a resonator between the XIN and XOUT pins. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The XIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XIN pin.
Figure 10.10 shows Examples of XIN Clock Connection Circuit.
In reset and after reset, the XIN clock stops.
The XIN clock starts oscillating when the CM05 bit in the CM0 register is set to 0 (XIN clock oscillates) after setting the CM13 bit in the CM1 register to 1 (XIN- XOUT pin).
To use the XIN clock for the CPU clock source, set the OCD2 bit in the OCD register to 0 (select XIN clock) after the XIN clock is oscillating stably.
The power consumption can be reduced by setting the CM05 bit in the CM0 register to 1 (XIN clock stops) if the OCD2 bit is set to 1 (select on-chip oscillator clock).
When an external clock is input to the XIN pin are input, the XIN clock does not stop if the CM05 bit is set to 1. If necessary, use an external circuit to stop the clock.
In stop mode, all clocks including the XIN clock stop. Refer to **10.5 Power Control** for details.



NOTE:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity setting. Use the value recommended by the manufacturer of the oscillator. Use high drive when oscillation starts and, if it is necessary to switch the oscillation drive capacity, do so after oscillation stabilizes.
When the oscillation drive capacity is set to low, check that oscillation is stable. Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.
To use this MCU with supply voltage below VCC = 2.7 V, it is recommended to set the CM11 bit in the CM1 register to 1 (on-chip feedback resistor disabled), the CM15 bit to 1 (high drive capacity), and connect the feedback resistor to the chip externally.

Figure 10.10 Examples of XIN Clock Connection Circuit

10.2 On-Chip Oscillator Clocks

These clocks are supplied by the on-chip oscillators (high-speed on-chip oscillator and a low-speed on-chip oscillator). The on-chip oscillator clock is selected by the FRA01 bit in the FRA0 register.

10.2.1 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, and fOCO-S.
After reset, the on-chip oscillator clock generated by the low-speed on-chip oscillator divided by 8 is selected as the CPU clock.
If the XIN clock stops oscillating when bits OCD1 to OCD0 in the OCD register are set to 11b, the low-speed on-chip oscillator automatically starts operating, supplying the necessary clock for the MCU.
The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operating ambient temperature. Application products must be designed with sufficient margin to allow for frequency changes.

10.2.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fOCO-F, and fOCO40M.
To use the high-speed on-chip oscillator clock as the clock source for the CPU clock, peripheral clock, fOCO, and fOCO-F, set bits FRA20 to FRA22 in the FRA2 register as follows:

- All divide ratio mode settings are supported when VCC = 3.0 V to 5.5 V 000b to 111b
- Divide ratio of 4 or more when VCC = 2.7 V to 5.5 V 010b to 111b (divide by 4 or more)
- Divide ratio of 8 or more when VCC = 2.2 V to 5.5 V 110b to 111b (divide by 8 or more)

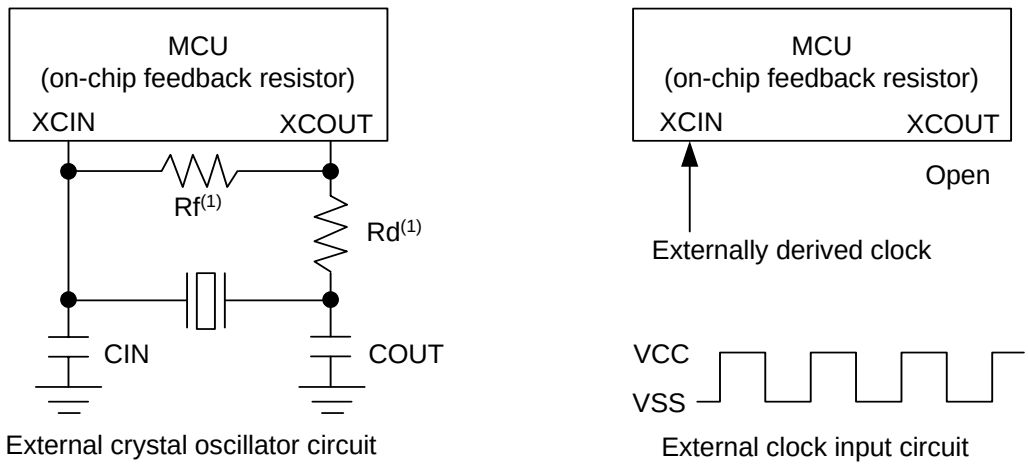
After reset, the on-chip oscillator clock generated by the high-speed on-chip oscillator stops. Oscillation is started by setting the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on). The frequency can be adjusted by registers FRA1 and FRA2.

The frequency correction data (the value is the same as that of the FRA1 register after a reset) corresponding to the supply voltage ranges VCC = 2.7 V to 5.5 V is stored in FRA4 register. Furthermore, the frequency correction data corresponding to the supply voltage ranges VCC = 2.2 V to 5.5 V is stored in FRA6 register. To use separate correction values to match these voltage ranges, transfer them from FRA4 or FRA6 register to the FRA1 register.
The frequency correction data of 36.864 MHz is stored in the FRA7 register. To set the frequency of the high-speed on-chip oscillator to 36.864 MHz, transfer the correction value in the FRA7 register to the FRA1 register before use. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode (refer to **Table 15.7 Bit Rate Setting Example in UART Mode (Internal Clock Selected)**).

Since there are differences in the amount of frequency adjustment among the bits in the FRA1 register, make adjustments by changing the settings of individual bits. Adjust the FRA1 register so that the frequency of the high-speed on-chip oscillator clock will be 40 MHz or less.

10.3 XCIN Clock

This clock is supplied by the XCIN clock oscillation circuit. This clock is used as the clock source for the CPU clock, timer RA, and timer RE. The XCIN clock oscillation circuit is configured by connecting a resonator between the XCIN and XCOUT pins. The XCIN clock oscillation circuit includes an on-chip a feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed in the chip. The XCIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XCIN pin.
Figure 10.11 shows Examples of XCIN Clock Connection Circuits.
During and after reset, the XCIN clock stops.
The XCIN clock starts oscillating when the CM04 bit in the CM0 register is set to 1 (XCIN-XCOUT pin).
To use the XCIN clock for the CPU clock source, set the CM07 bit in the CM0 register to 1 (XCIN clock) after the XCIN clock is oscillating stably. To input an external clock to the XCIN pin, set the CM04 bit in the CM0 register to 1 (XCIN-XCOUT pin) and leave the XCOUT pin open.
This MCU has an on-chip feedback resistor and on-chip resistor disable/enable switching is possible by the CM12 bit in the CM1 register.
In stop mode, all clocks including the XCIN clock stop. Refer to **10.5 Power Control** for details.



NOTE:
1. Insert a damping resistor and feedback resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity setting. Use the value recommended by the manufacturer of the oscillator.
When the oscillation drive capacity is set to low, check that oscillation is stable. Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XCIN and XCOUT following the instructions.

Figure 10.11 Examples of XCIN Clock Connection Circuits

10.4 CPU Clock and Peripheral Function Clock

There are a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions. Refer to **Figure 10.1 Clock Generation Circuit**.

10.4.1 System Clock

The system clock is the clock source for the CPU and peripheral function clocks. Either the XIN clock or the on-chip oscillator clock can be selected.

10.4.2 CPU Clock

The CPU clock is an operating clock for the CPU and watchdog timer.
When the CM07 bit in the CM0 register is set to 0 (system clock), the system clock can be divided by 1 (no division), 2, 4, 8, or 16 to produce the CPU clock. Use the CM06 bit in the CM0 register and bits CM16 to CM17 in the CM1 register to select the value of the division.
When the CM07 bit in the CM0 register is set to 1 (XCIN clock), the XCIN clock is used for the CPU clock.
Use the XCIN clock while the XCIN clock oscillation stabilizes.
After reset, the low-speed on-chip oscillator clock divided by 8 provides the CPU clock.
When entering stop mode from high-speed clock mode, the CM06 bit is set to 1 (divide-by-8 mode).

10.4.3 Peripheral Function Clock (f1, f2, f4, f8, and f32)

The peripheral function clock is the operating clock for the peripheral functions.
The clock fi (i = 1, 2, 4, 8, and 32) is generated by the system clock divided by i. The clock fi is used for timers RA, RB, RD, and RE, the serial interface and the A/D converter.
When the WAIT instruction is executed after setting the CM02 bit in the CM0 register to 1 (peripheral function clock stops in wait mode), the clock fi stop.

10.4.4 fOCO

fOCO is an operating clock for the peripheral functions.
fOCO runs at the same frequency as the on-chip oscillator clock and can be used as the source for timer RA.
When the WAIT instruction is executed, the clocks fOCO does not stop.

10.4.5 fOCO40M

fOCO40M is used as the count source for timer RD. fOCO40M is generated by the high-speed on-chip oscillator and supplied by setting the FRA00 bit to 1.
When the WAIT instruction is executed, the clock fOCO40M does not stop.
fOCO40M can be used with supply voltage VCC = 3.0 to 5.5 V.

10.4.6 fOCO-F

fOCO-F is used as the count source for the A/D converter. fOCO-F is generated by the high-speed on-chip oscillator and supplied by setting the FRA00 bit to 1.
When the WAIT instruction is executed, the clock fOCO-F does not stop.

10.4.7 fOCO-S

fOCO-S is an operating clock for the watchdog timer and voltage detection circuit. fOCO-S is supplied by setting the CM14 bit to 0 (low-speed on-chip oscillator on) and uses the clock generated by the low-speed on-chip oscillator. When the WAIT instruction is executed or in count source protect mode of the watchdog timer, fOCO-S does not stop.

10.4.8 fOCO128

fOCO128 is generated by fOCO divided by 128.
The clock fOCO128 is used for capture signal of timer RD (channel 0).

10.4.9 fC4 and fC32

The clock fC4 and fC32 are used for timer RA and timer RE.
Use fC4 and fC32 while the XCIN clock oscillation stabilizes.

10.5 Power Control

There are three power control modes. All modes other than wait mode and stop mode are referred to as standard operating mode.

10.5.1 Standard Operating Mode

Standard operating mode is further separated into four modes.
In standard operating mode, the CPU clock and the peripheral function clock are supplied to operate the CPU and the peripheral function clocks. Power consumption control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. When unnecessary oscillator circuits stop, power consumption is further reduced.
Before the clock sources for the CPU clock can be switched over, the new clock source needs to be oscillating and stable. If the new clock source is the XIN clock or XCIN clock, allow sufficient wait time in a program until oscillation is stabilized before exiting.

Table 10.2 Settings and Modes of Clock Associated Bits

Modes		OCD Register	CM1 Register			CM0 Register				FRA0 Register	
		OCD2	CM17, CM16	CM14	CM13	CM07	CM06	CM05	CM04	FRA01	FRA00
High-speed clock mode	No division	0	00b	–	1	0	0	0	–	–	–
	Divide-by-2	0	01b	–	1	0	0	0	–	–	–
	Divide-by-4	0	10b	–	1	0	0	0	–	–	–
	Divide-by-8	0	–	–	1	0	1	0	–	–	–
	Divide-by-16	0	11b	–	1	0	0	0	–	–	–
Low-speed clock mode	No division	–	–	–	–	1	–	–	1	–	–
High-speed on-chip oscillator mode	No division	1	00b	–	–	0	0	–	–	1	1
	Divide-by-2	1	01b	–	–	0	0	–	–	1	1
	Divide-by-4	1	10b	–	–	0	0	–	–	1	1
	Divide-by-8	1	–	–	–	0	1	–	–	1	1
	Divide-by-16	1	11b	–	–	0	0	–	–	1	1
Low-speed on-chip oscillator mode	No division	1	00b	0	–	0	0	–	–	0	–
	Divide-by-2	1	01b	0	–	0	0	–	–	0	–
	Divide-by-4	1	10b	0	–	0	0	–	–	0	–
	Divide-by-8	1	–	0	–	0	1	–	–	0	–
	Divide-by-16	1	11b	0	–	0	0	–	–	0	–

X: can be 0 or 1, no change in outcome

10.5.1.1 High-Speed Clock Mode

The XIN clock divided by 1 (no division), 2, 4, 8, or 16 provides the CPU clock. Set the CM06 bit to 1 (divide-by-8 mode) when transiting to high-speed on-chip oscillator mode, low-speed on-chip oscillator mode. If the CM14 bit is set to 0 (low-speed on-chip oscillator on) or the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on), fOCO can be used as timer RA. When the FRA00 bit is set to 1, fOCO40M can be used as timer RD. When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the watchdog timer and voltage detection circuit.

10.5.1.2 Low-Speed Clock Mode

The XCIN clock divided by 1 (no division) provides the CPU clock.
In this mode, stopping the XIN clock and high-speed on-chip oscillator, and setting the FMR47 bit in the FMR4 register to 1 (flash memory low consumption current read mode enabled) enables low consumption operation.
When the FRA00 bit is set to 1, fOCO40M can be used as timer RD. When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the watchdog timer and voltage detection circuit.
To enter wait mode from low-speed clock mode, setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled) enables lower consumption current in wait mode.
When enabling reduced internal power consumption using the VCA20 bit, follow **Figure 10.13 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit**.

10.5.1.3 High-Speed On-Chip Oscillator Mode

The high-speed on-chip oscillator is used as the on-chip oscillator clock when the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 1. The on-chip oscillator divided by 1 (no division), 2, 4, 8, or 16 provides the CPU clock. Set the CM06 bit to 1 (divide-by-8 mode) when transiting to high-speed clock mode. If the FRA00 bit is set to 1, fOCO40M can be used as timer RD. When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the watchdog timer and voltage detection circuit.

10.5.1.4 Low-Speed On-Chip Oscillator Mode

If the CM14 bit in the CM1 register is set to 0 (low-speed on-chip oscillator on) or the FRA01bit in the FRA0 register is set to 0, the low-speed on-chip oscillator provides the on-chip oscillator clock.
The on-chip oscillator clock divided by 1 (no division), 2, 4, 8 or 16 provides the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks. Set the CM06 bit to 1 (divide-by-8 mode) when transiting to high-speed clock mode. When the FRA00 bit is set to 1, fOCO40M can be used as timer RD. When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used as the watchdog timer and voltage detection circuit.
In this mode, stopping the XIN clock and high-speed on-chip oscillator, and setting the FMR47 bit in the FMR4 register to 1 (flash memory low consumption current read mode enabled) enables low consumption operation.
To enter wait mode from low-speed on-chip oscillator mode, setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled) enables lower consumption current in wait mode.
When enabling reduced internal power consumption using the VCA20 bit, follow **Figure 10.13 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit**.

10.5.2 Wait Mode

Since the CPU clock stops in wait mode, the CPU, which operates using the CPU clock, and the watchdog timer, when count source protection mode is disabled, stop. The XIN clock, XCIN clock, and on-chip oscillator clock do not stop and the peripheral functions using these clocks continue operating.

10.5.2.1 Peripheral Function Clock Stop Function

If the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the f1, f2, f4, f8, and f32 clocks stop in wait mode. This reduces power consumption.

10.5.2.2 Entering Wait Mode

The MCU enters wait mode when the WAIT instruction is executed.
When the OCD2 bit in the OCD register is set to 1 (on-chip oscillator selected as system clock), set the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before executing the WAIT instruction.
If the MCU enters wait mode while the OCD1 bit is set to 1 (oscillation stop detection interrupt enabled), current consumption is not reduced because the CPU clock does not stop.

10.5.2.3 Pin Status in Wait Mode

The I/O port is the status before wait mode was entered is maintained.

10.5.2.4 Exiting Wait Mode

The MCU exits wait mode by a reset or a peripheral function interrupt.
The peripheral function interrupts are affected by the CM02 bit. When the CM02 bit is set to 0 (peripheral function clock does not stop in wait mode), all peripheral function interrupts can be used to exit wait mode. When the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the peripheral functions using the peripheral function clock stop operating and the peripheral functions operated by external signals or on-chip oscillator clock can be used to exit wait mode.
Table 10.3 lists Interrupts to Exit Wait Mode and Usage Conditions.

Table 10.3 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02 = 0	CM02 = 1
Serial interface interrupt	Usable when operating with internal or external clock	Usable when operating with external clock
Clock synchronous serial I/O with chip select interrupt / I^2C bus interface interrupt	Usable in all modes	(Do not use)
Key input interrupt	Usable	Usable
A/D conversion interrupt	Usable in one-shot mode	(Do not use)
Timer RA interrupt	Usable in all modes	Can be used if there is no filter in event counter mode. Usable by selecting fOCO or fC32 as count source.
Timer RB interrupt	Usable in all modes	(Do not use)
Timer RD interrupt	Usable in all modes	Usable by selecting fOCO40M as count source
Timer RE interrupt	Usable in all modes	Usable when operating in real time clock mode
$\overline{\text{INT}}$ interrupt	Usable	Usable ($\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ can be used if there is no filter.)
Voltage monitor 1 interrupt	Usable	Usable
Voltage monitor 2 interrupt	Usable	Usable
Oscillation stop detection interrupt	Usable	(Do not use)

Figure 10.12 shows the Time from Wait Mode to Interrupt Routine Execution.
When using a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting wait mode.

When exiting by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the CM07 bit in the CM0 register, as described in Figure 10.12.
The CPU clock, when exiting wait mode by a peripheral function interrupt, is the same clock as the CPU clock when the WAIT instruction is executed.

FMR0 Register FMSTP Bit	CM0 Register CM07 Bit	Time until Flash Memory is Activated (T1)	Time until CPU Clock is Supplied (T2)	Time for Interrupt Sequence (T3)	Remarks
0 (flash memory operates)	0 (system clock)	Period of system clock × 12 cycles + 30 μs (max.)	Period of CPU clock × 6 cycles	Period of CPU clock × 20 cycles	Following total time is the time from wait mode until an interrupt routine is executed.
	1 (XCIN clock)	Period of XCIN clock × 12 cycles + 30 μs (max.)	Same as above	Same as above	
1 (flash memory stops)	0 (system clock)	Period of system clock × 12 cycles	Same as above	Same as above	
	1 (XCIN clock)	Period of XCIN clock × 12 cycles	Same as above	Same as above	

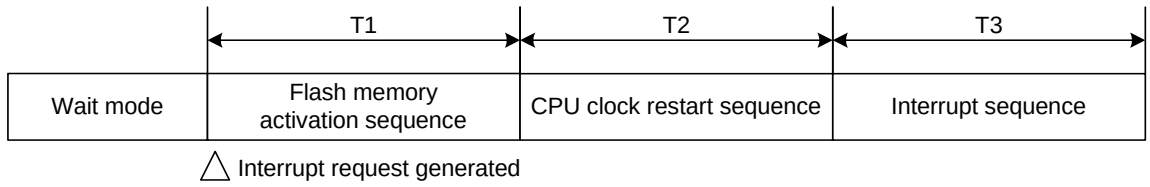
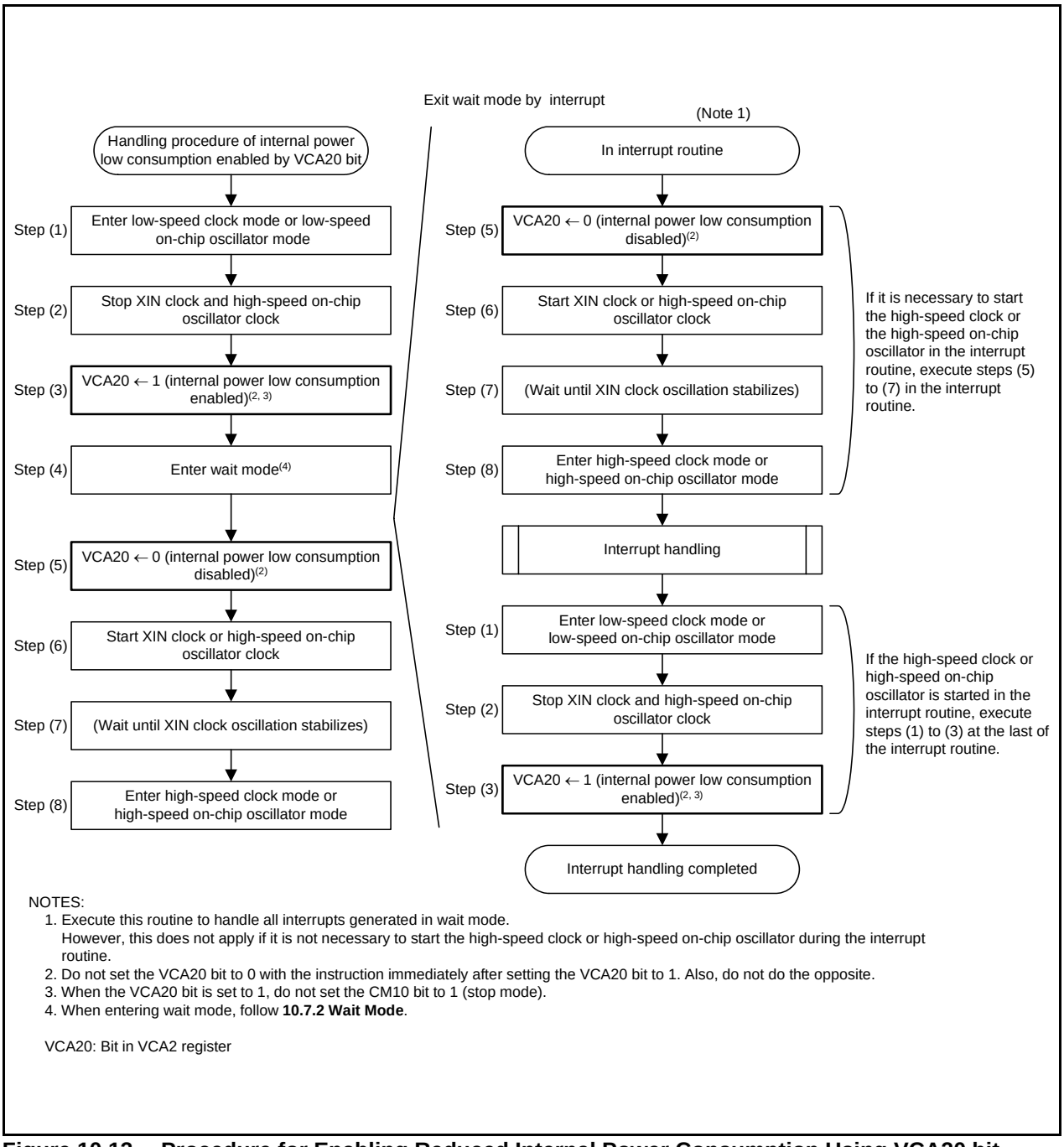


Figure 10.12 Time from Wait Mode to Interrupt Routine Execution

10.5.2.5 Reducing Internal Power Consumption

Internal power consumption can be reduced by using low-speed clock mode or low-speed on-chip oscillator mode. Figure 10.13 shows the Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit. When enabling reduced internal power consumption using the VCA20 bit, follow **Figure 10.13 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit**.



NOTES:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the high-speed clock or high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When entering wait mode, follow **10.7.2 Wait Mode**.

VCA20: Bit in VCA2 register

Figure 10.13 Procedure for Enabling Reduced Internal Power Consumption Using VCA20 bit

10.5.3 Stop Mode

Since the oscillator circuits stop in stop mode, the CPU clock and peripheral function clock stop and the CPU and peripheral functions that use these clocks stop operating. The least power required to operate the MCU is in stop mode. If the voltage applied to the VCC pin is VRAM or more, the contents of internal RAM is maintained.
The peripheral functions clocked by external signals continue operating.
Table 10.4 lists Interrupts to Exit Stop Mode and Usage Conditions.

Table 10.4 Interrupts to Exit Stop Mode and Usage Conditions

Interrupt	Usage Conditions
Key input interrupt	–
$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ interrupt	Can be used if there is no filter
Timer RA interrupt	Can be used if there is no filter when external pulse is counted in event counter mode
Serial interface interrupt	When external clock is selected
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (VW1C1 bit in VW1C register is set to 1)
Voltage monitor 2 interrupt	Usable in digital filter disabled mode (VW2C1 bit in VW2C register is set to 1)

10.5.3.1 Entering Stop Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1 (all clocks stop). At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode) and the CM15 bit in the CM1 register is set to 1 (XIN clock oscillator circuit drive capacity high).
When using stop mode, set bits OCD1 to OCD0 to 00b before entering stop mode.

10.5.3.2 Pin Status in Stop Mode

The status before wait mode was entered is maintained.
However, when the CM13 bit in the CM1 register is set to 1 (XIN-XOUT pins), the XOUT(P4_7) pin is held “H”. When the CM13 bit is set to 0 (input ports P4_6 and P4_7), the P4_7(XOUT pin) is held in input status.

10.5.3.3 Exiting Stop Mode

The MCU exits stop mode by a reset or peripheral function interrupt.
Figure 10.14 shows the Time from Stop Mode to Interrupt Routine Execution.
When using a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to 1.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operates the peripheral function to be used for exiting stop mode.
When exiting by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply is started.

If the clock used immediately before stop mode is a system clock and stop mode is exited by a peripheral function interrupt, the CPU clock becomes the previous system clock divided by 8.

FMR0 Register FMSTP Bit	CM0 Register CM07 Bit	Time until Flash Memory is Activated (T2)	Time until CPU Clock is Supplied (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	0 (system clock)	Period of system clock × 12 cycles + 30 µs (max.)	Period of CPU clock × 6 cycles	Period of CPU clock × 20 cycles	Following total time of T0 to T4 is the time from stop mode until an interrupt handling is executed.
	1 (XCIN clock)	Period of XCIN clock × 12 cycles + 30 µs (max.)	Same as above	Same as above	
1 (flash memory stops)	0 (system clock)	Period of system clock × 12 cycles	Same as above	Same as above	
	1 (XCIN clock)	Period of XCIN clock × 12 cycles	Same as above	Same as above	

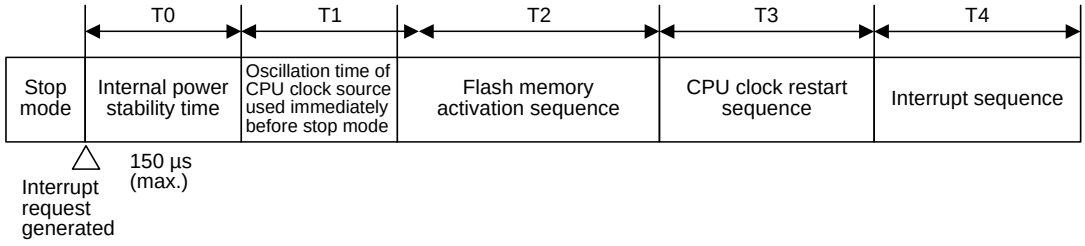


Figure 10.14 Time from Stop Mode to Interrupt Routine Execution

Figure 10.15 shows the State Transitions in Power Control Mode.

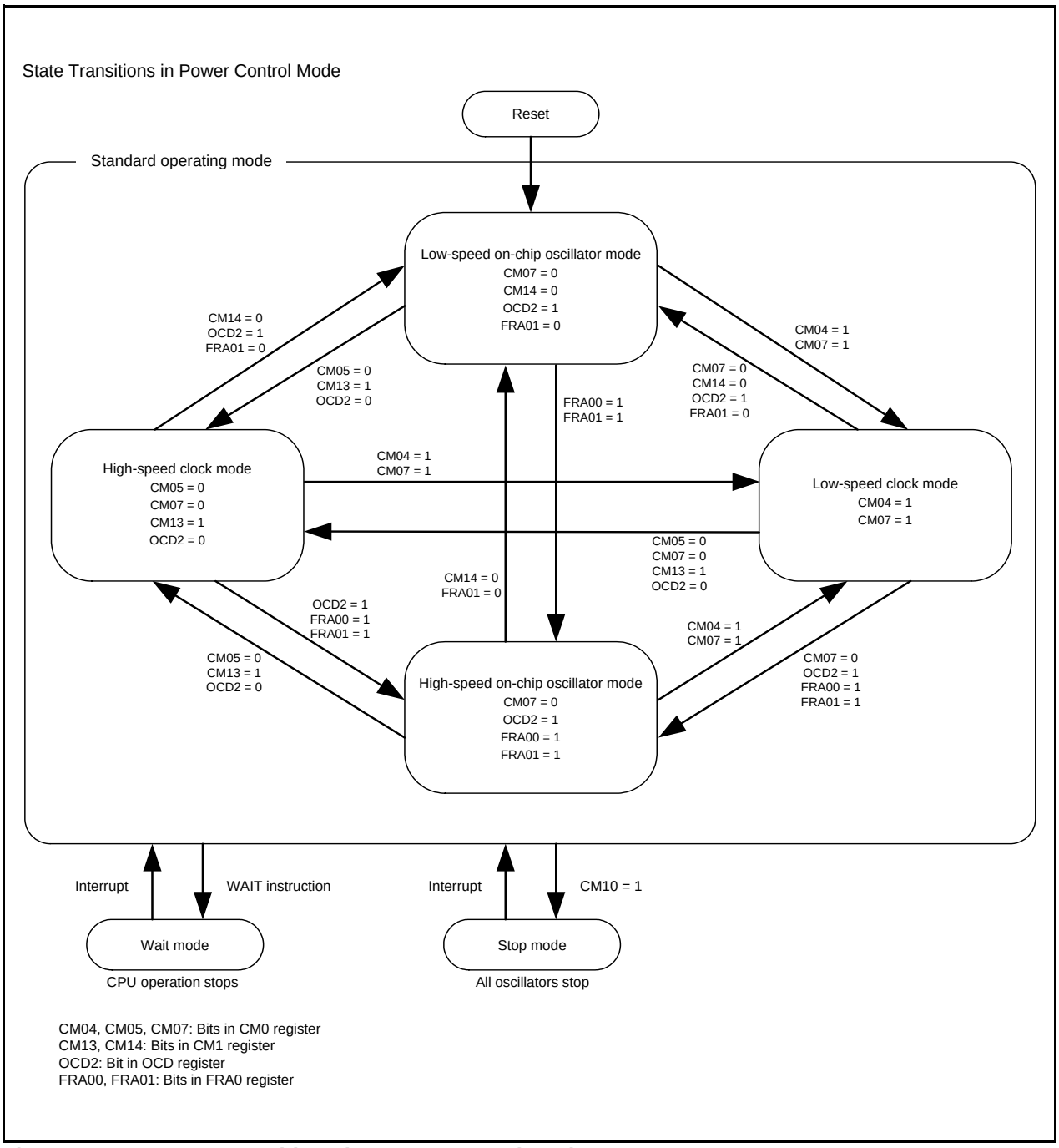


Figure 10.15 State Transitions in Power Control Mode

10.6 Oscillation Stop Detection Function

The oscillation stop detection function detects the stop of the XIN clock oscillating circuit. The oscillation stop detection function can be enabled and disabled by the OCD0 bit in the OCD register.
Table 10.5 lists the Specifications of Oscillation Stop Detection Function.

When the XIN clock is the CPU clock source and bits OCD1 to OCD0 are set to 11b, the system is placed in the following state if the XIN clock stops.

- OCD2 bit in OCD register = 1 (on-chip oscillator clock selected)
- OCD3 bit in OCD register = 1 (XIN clock stops)
- CM14 bit in CM1 register = 0 (low-speed on-chip oscillator oscillates)
- Oscillation stop detection interrupt request is generated.

Table 10.5 Specifications of Oscillation Stop Detection Function

Item	Specification
Oscillation stop detection clock and frequency bandwidth	f(XIN) ≥ 2 MHz
Enabled condition for oscillation stop detection function	Set bits OCD1 to OCD0 to 11b
Operation at oscillation stop detection	Oscillation stop detection interrupt is generated

10.6.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the voltage monitor 1 interrupt, the voltage monitor 2 interrupt, and the watchdog timer interrupt. When using the oscillation stop detection interrupt and watchdog timer interrupt, the interrupt source needs to be determined.
  Table 10.6 lists the Determining Interrupt Source for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, and Voltage Monitor 2 Interrupts. Figure 10.17 shows an Example of Determining Interrupt Source for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt.
- When the XIN clock restarts after oscillation stop, switch the XIN clock to the clock source of the CPU clock and peripheral functions by a program.
  Figure 10.16 shows the Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock.
- To enter wait mode while using the oscillation stop detection function, set the CM02 bit to 0 (peripheral function clock does not stop in wait mode).
- Since the oscillation stop detection function is a function for cases where the XIN clock is stopped by an external cause, set bits OCD1 to OCD0 to 00b when the XIN clock stops or is started by a program, (stop mode is selected or the CM05 bit is changed).
- This function cannot be used when the XIN clock frequency is 2 MHz or below. In this case, set bits OCD1 to OCD0 to 00b.
- To use the low-speed on-chip oscillator clock for the CPU clock and clock sources of peripheral functions after detecting the oscillation stop, set the FRA01 bit in the FRA0 register to 0 (low-speed on-chip oscillator selected) and bits OCD1 to OCD0 to 11b.
  To use the high-speed on-chip oscillator clock for the CPU clock and clock sources of peripheral functions after detecting the oscillation stop, set the FRA00 bit to 1 (high-speed on-chip oscillator on) and the FRA01 bit to 1 (high-speed on-chip oscillator selected) and then set bits OCD1 to OCD0 to 11b.

Table 10.6 Determining Interrupt Source for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, and Voltage Monitor 2 Interrupts

Generated Interrupt Source	Bit Showing Interrupt Cause
Oscillation stop detection ((a) or (b))	(a) OCD3 bit in OCD register = 1
	(b) OCD1 to OCD0 bits in OCD register = 11b and OCD2 bit = 1
Watchdog timer	VW2C3 bit in VW2C register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1
Voltage monitor 2	VW2C2 bit in VW2C register = 1

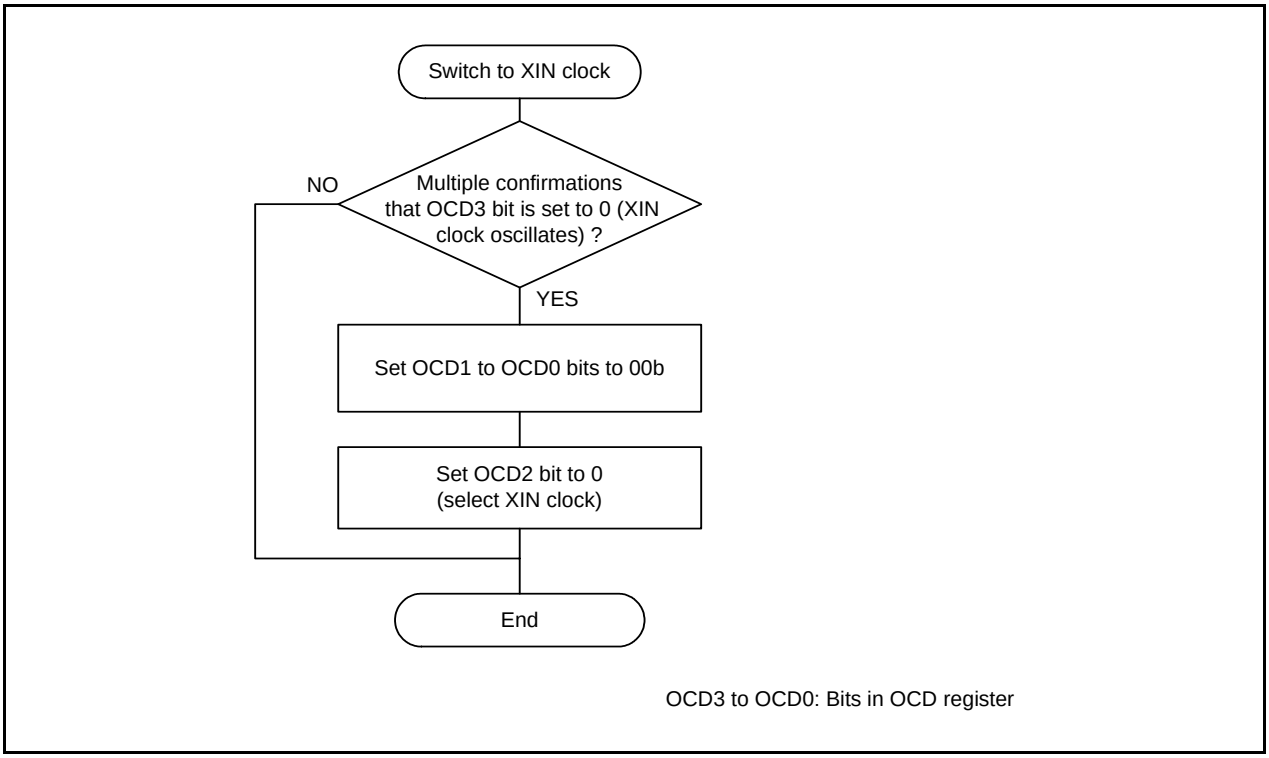
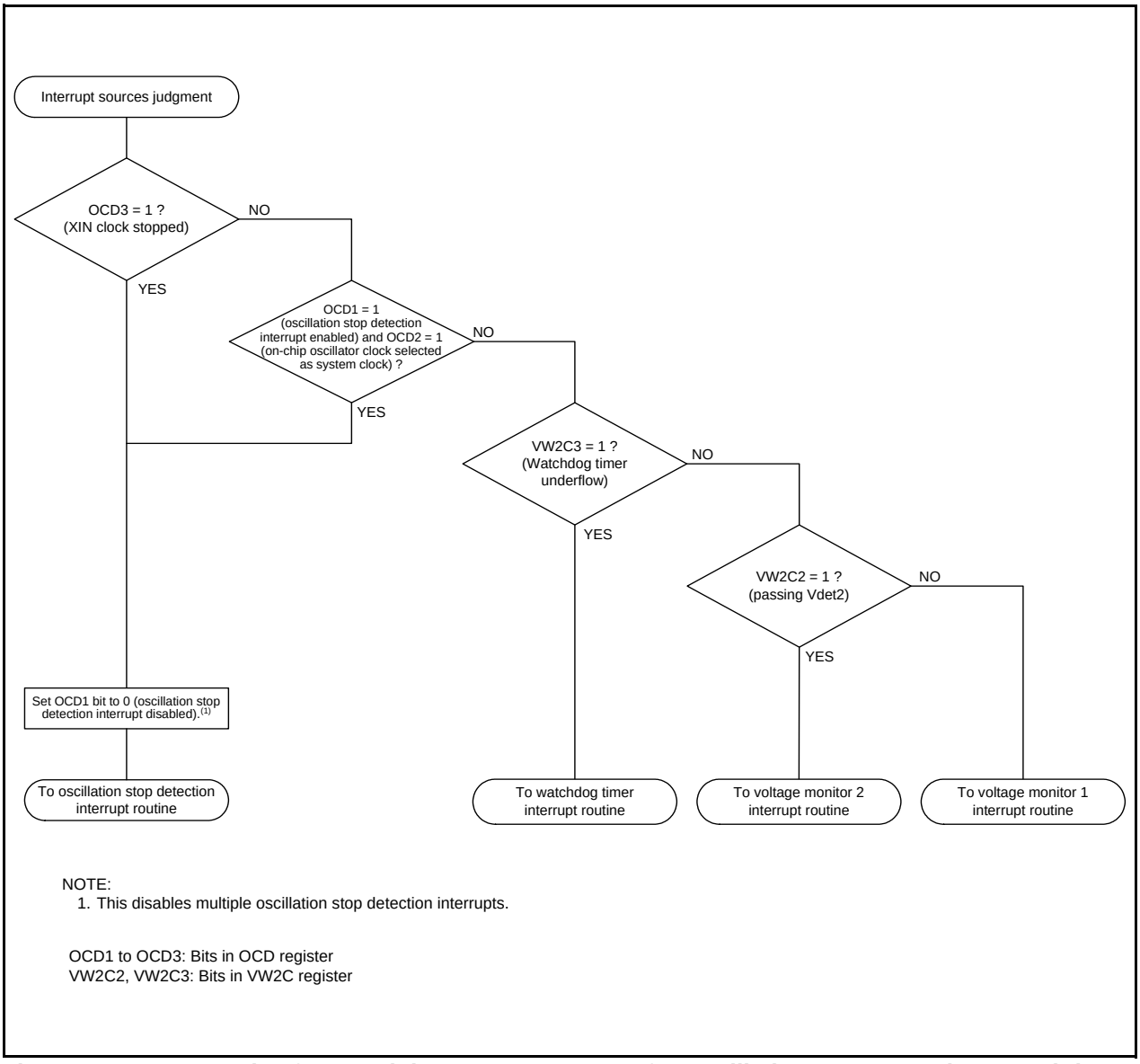


Figure 10.16 Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock



NOTE:
1. This disables multiple oscillation stop detection interrupts.

OCD1 to OCD3: Bits in OCD register
VW2C2, VW2C3: Bits in VW2C register

Figure 10.17 Example of Determining Interrupt Source for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

10.7 Notes on Clock Generation Circuit

10.7.1 Stop Mode

When entering stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least 4 NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

• Program example to enter stop mode

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        BSET    0,PRCR          ; Protect disabled
        FSET    I               ; Enable interrupt
        BSET    0,CM1           ; Stop mode
        JMP.B   LABEL_001
LABEL_001 :
        NOP
        NOP
        NOP
        NOP
```

10.7.2 Wait Mode

When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the WAIT instruction and the program stops. Insert at least 4 NOP instructions after the WAIT instruction.

• Program example to execute the WAIT instruction

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        FSET    I               ; Enable interrupt
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

10.7.3 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is 2 MHz or below, set bits OCD1 to OCD0 to 00b.

10.7.4 Oscillation Circuit Constants

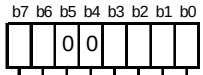
Ask the manufacturer of the oscillator to specify the best oscillation circuit constants for your system.
To use this MCU with supply voltage below VCC = 2.7 V, it is recommended to set the CM11 bit in the CM1 register to 1 (on-chip feedback resistor disabled), the CM15 bit to 1 (high drive capacity), and connect the feedback resistor to the chip externally.

11. Protection

The protection function protects important registers from being easily overwritten when a program runs out of control. Figure 11.1 shows the PRCR Register. The registers protected by the PRCR register are listed below.

- Registers protected by PRC0 bit: Registers CM0, CM1, OCD, FRA0, FRA1, and FRA2
- Registers protected by PRC1 bit: Registers PM0 and PM1
- Registers protected by PRC2 bit: PD0 register
- Registers protected by PRC3 bit: Registers VCA2, VW0C, VW1C, and VW2C

Protect Register



Symbol: PRCR | Address: 000Ah | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
PRC0	Protect bit 0	Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 is enabled. 0 : Disables writing 1 : Enables writing	RW
PRC1	Protect bit 1	Writing to registers PM0 and PM1 is enabled. 0 : Disables writing 1 : Enables writing	RW
PRC2	Protect bit 2	Writing to the PD0 register is enabled. 0 : Disables writing 1 : Enables writing(1)	RW
PRC3	Protect bit 3	Writing to registers VCA2, VW0C, VW1C, and VW2C is enabled. 0 : Disables writing 1 : Enables writing	RW
— (b5-b4)	Reserved bits	Set to 0.	RW
— (b7-b6)	Reserved bits	When read, the content is 0.	RO

NOTE:
1. This bit is set to 0 after writing 1 to the PRC2 bit and executing a write to any address. Since the other bits are not set to 0, set them to 0 by a program.

Figure 11.1 PRCR Register

12. Interrupts

12.1 Interrupt Overview

12.1.1 Types of Interrupts

Figure 12.1 shows the Types of Interrupts.

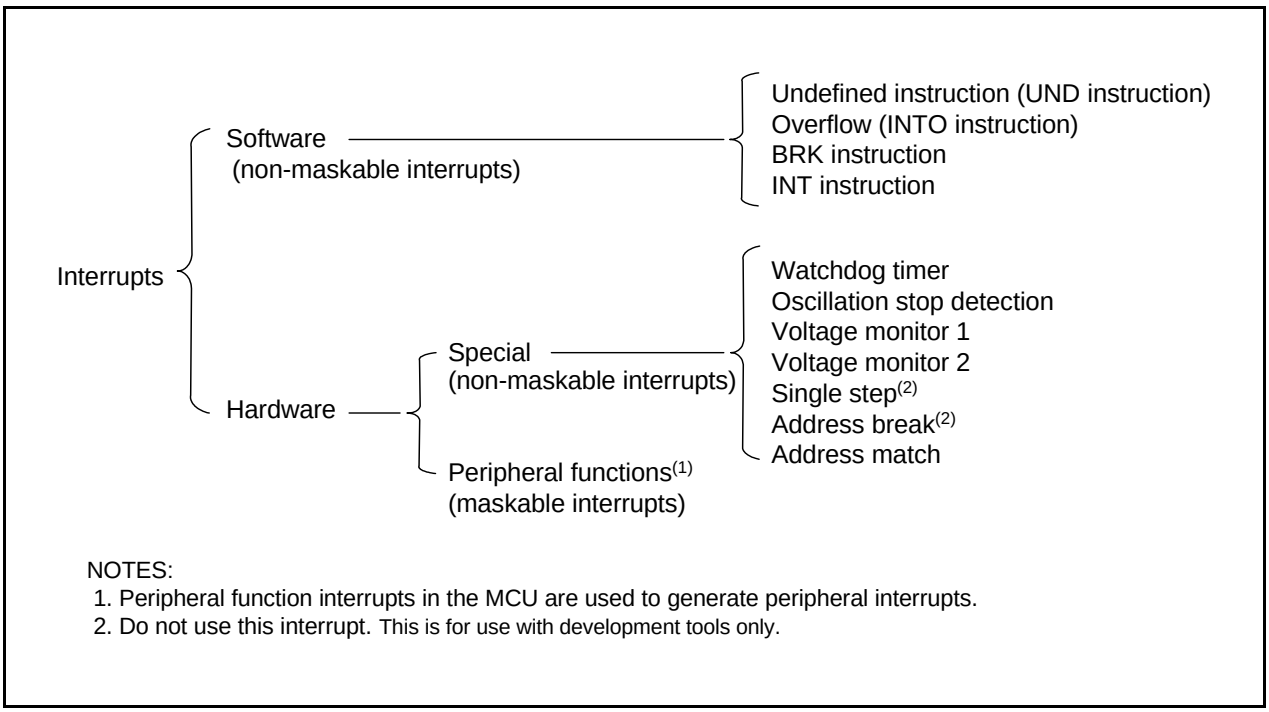


Figure 12.1 Types of Interrupts

- Maskable Interrupts: The interrupt enable flag (I flag) enables or disables these interrupts. The interrupt priority order can be changed based on the interrupt priority level.
- Non-Maskable Interrupts: The interrupt enable flag (I flag) does not enable or disable these interrupts. The interrupt priority order cannot be changed based on interrupt priority level.

12.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. Software interrupts are non-maskable.

12.1.2.1 Undefined Instruction Interrupt

The undefined instruction interrupt is generated when the UND instruction is executed.

12.1.2.2 Overflow Interrupt

The overflow interrupt is generated when the O flag is set to 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that set the O flag are: ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.

12.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

12.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. The INT instruction can select software interrupt numbers 0 to 63. Software interrupt numbers 3 to 31 are assigned to the peripheral function interrupt. Therefore, the MCU executes the same interrupt routine when the INT instruction is executed as when a peripheral function interrupt is generated. For software interrupt numbers 0 to 31, the U flag is saved to the stack during instruction execution and the U flag is set to 0 (ISP selected) before the interrupt sequence is executed. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

12.1.3 Special Interrupts

Special interrupts are non-maskable.

12.1.3.1 Watchdog Timer Interrupt

The watchdog timer interrupt is generated by the watchdog timer. For details, refer to **13. Watchdog Timer**.

12.1.3.2 Oscillation Stop Detection Interrupt

The oscillation stop detection interrupt is generated by the oscillation stop detection function. For details of the oscillation stop detection function, refer to **10. Clock Generation Circuit**.

12.1.3.3 Voltage Monitor 1 Interrupt

The voltage monitor 1 interrupt is generated by the voltage detection circuit. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

12.1.3.4 Voltage Monitor 2 Interrupt

The voltage monitor 2 interrupt is generated by the voltage detection circuit. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

12.1.3.5 Single-Step Interrupt, and Address Break Interrupt

Do not use these interrupts. They are for use by development tools only.

12.1.3.6 Address Match Interrupt

The address match interrupt is generated immediately before executing an instruction that is stored at an address indicated by registers RMAD0 to RMAD1 when the AIER0 or AIER1 bit in the AIER register is set to 1 (address match interrupt enable). For details of the address match interrupt, refer to **12.4 Address Match Interrupt**.

12.1.4 Peripheral Function Interrupt

The peripheral function interrupt is generated by the internal peripheral function of the MCU and is a maskable interrupt. Refer to **Table 12.2 Relocatable Vector Tables** for sources of the peripheral function interrupt. For details of peripheral functions, refer to the descriptions of individual peripheral functions.

12.1.5 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the starting address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 12.2 shows an Interrupt Vector.

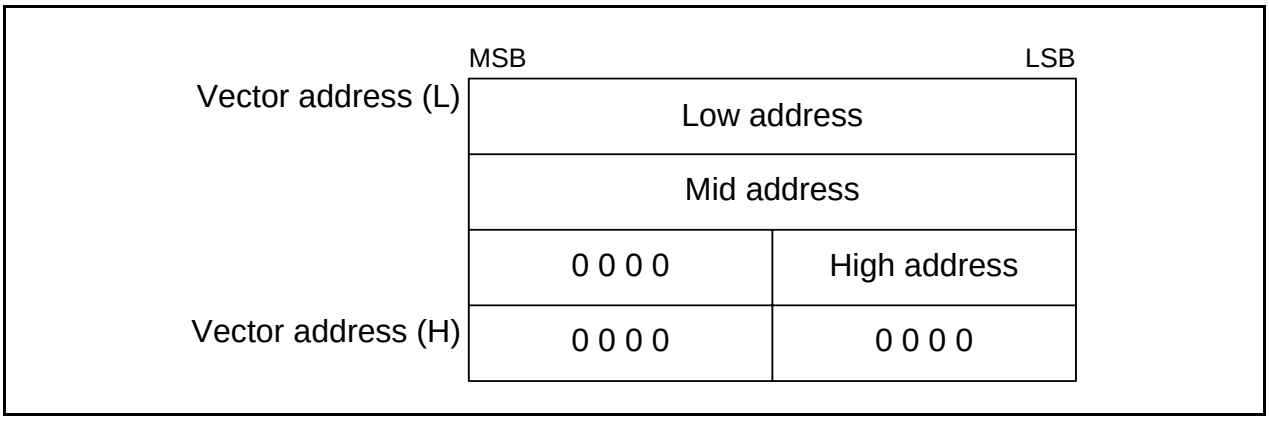


Figure 12.2 Interrupt Vector

12.1.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses 0FFDCh to 0FFFFh.
Table 12.1 lists the Fixed Vector Tables. The vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **19.3 Functions to Prevent Rewriting of Flash Memory**.

Table 12.1 Fixed Vector Tables

Interrupt Source	Vector Addresses Address (L) to (H)	Remarks	Reference
Undefined instruction	0FFDCh to 0FFDFh	Interrupt on UND instruction	R8C/Tiny Series Software Manual
Overflow	0FFE0h to 0FFE3h	Interrupt on INTO instruction	
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE7h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	0FFE8h to 0FFEBh		12.4 Address Match Interrupt
Single step(1)	0FFECh to 0FFEFh		
Watchdog timer, Oscillation stop detection, Voltage monitor 1, Voltage monitor 2	0FFF0h to 0FFF3h		13. Watchdog Timer 10. Clock Generation Circuit 6. Voltage Detection Circuit
Address break(1)	0FFF4h to 0FFF7h		
(Reserved)	0FFF8h to 0FFFBh		
Reset	0FFFCh to 0FFFFh		5. Resets

NOTE:
1. Do not use these interrupts. They are for use by development tools only.

12.1.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes beginning from the starting address set in the INTB register. Table 12.2 lists the Relocatable Vector Tables.

Table 12.2 Relocatable Vector Tables

Interrupt Source	Vector Addresses(1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
BRK instruction(3)	+0 to +3 (0000h to 0003h)	0	–	R8C/Tiny Series Software Manual
(Reserved)		1 to 2	–	–
(Reserved)		3 to 7	–	–
Timer RD (channel 0)	+32 to +35 (0020h to 0023h)	8	TRD0IC	14.3 Timer RD
Timer RD (channel 1)	+36 to +39 (0024h to 0027h)	9	TRD1IC	
Timer RE	+40 to +43 (0028h to 002Bh)	10	TREIC	14.4 Timer RE
(Reserved)		11 to 12	–	–
Key input	+52 to +55 (0034h to 0037h)	13	KUPIC	12.3 Key Input Interrupt
A/D	+56 to +59 (0038h to 003Bh)	14	ADIC	18. A/D Converter
Clock synchronous serial I/O with chip select / I^2C bus interface(2)	+60 to +63 (003Ch to 003Fh)	15	SSUIC/IICIC	16.2 Clock Synchronous Serial I/O with Chip Select (SSU), 16.3 I^2C bus Interface
(Reserved)		16	–	–
UART0 transmit	+68 to +71 (0044h to 0047h)	17	S0TIC	15. Serial Interface
UART0 receive	+72 to +75 (0048h to 004Bh)	18	S0RIC	
UART1 transmit	+76 to +79 (004Ch to 004Fh)	19	S1TIC	
UART1 receive	+80 to +83 (0050h to 0053h)	20	S1RIC	
$\overline{INT2}$	+84 to +87 (0054h to 0057h)	21	INT2IC	12.2 $\overline{INT}$ Interrupt
Timer RA	+88 to +91 (0058h to 005Bh)	22	TRAIC	14.1 Timer RA
(Reserved)		23	–	–
Timer RB	+96 to +99 (0060h to 0063h)	24	TRBIC	14.2 Timer RB
$\overline{INT1}$	+100 to +103 (0064h to 0067h)	25	INT1IC	12.2 $\overline{INT}$ Interrupt
$\overline{INT3}$	+104 to +107 (0068h to 006Bh)	26	INT3IC	
(Reserved)		27	–	–
(Reserved)		28	–	–
$\overline{INT0}$	+116 to +119 (0074h to 0077h)	29	INT0IC	12.2 $\overline{INT}$ Interrupt
(Reserved)		30	–	–
(Reserved)		31	–	–
Software interrupt(3)	+128 to +131 (0080h to 0083h) to +252 to +255 (00FCh to 00FFh)	32 to 63	–	R8C/Tiny Series Software Manual

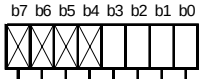
NOTES:
1. These addresses are relative to those in the INTB register.
2. The IICSEL bit in the PMR register switches functions.
3. The I flag does not disable these interrupts.

12.1.6 Interrupt Control

The following describes enabling and disabling the maskable interrupts and setting the priority for acknowledgement. The explanation does not apply to nonmaskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in each interrupt control register to enable or disable maskable interrupts. Whether an interrupt is requested is indicated by the IR bit in each interrupt control register.
Figure 12.3 shows the Interrupt Control Register, Figure 12.4 shows Registers TRD0IC, TRD1IC, SSUIC, and IICIC and Figure 12.5 shows the INTiIC Register.

Interrupt Control Register(2)

Symbol	Address	After Reset
TREIC	004Ah	XXXXX000b
KUPIC	004Dh	XXXXX000b
ADIC	004Eh	XXXXX000b
S0TIC	0051h	XXXXX000b
S0RIC	0052h	XXXXX000b
S1TIC	0053h	XXXXX000b
S1RIC	0054h	XXXXX000b
TRAIC	0056h	XXXXX000b
TRBIC	0058h	XXXXX000b



Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bits	b2 b1 b0 0 0 0 : Level 0 (interrupt disable) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0 : Requests no interrupt 1 : Requests interrupt	RW(1)
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

NOTES:
1. Only 0 can be written to the IR bit. Do not write 1.
2. Rewrite the interrupt control register when the interrupt request which is applicable for the register is not generated. Refer to **12.6.5 Changing Interrupt Control Register Contents**.

Figure 12.3 Interrupt Control Register

Interrupt Control Register(1)

Symbol	Address	After Reset
TRD0IC	0048h	XXXXX000b
TRD1IC	0049h	XXXXX000b
SSUIC/IICIC(2)	004Fh	XXXXX000b

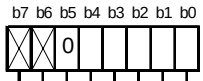
Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bits	b2 b1 b0 0 0 0 : Level 0 (interrupt disable) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0 : Requests no interrupt 1 : Requests interrupt	RO
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

NOTES:
1. Rewrite the interrupt control register when the interrupt request which is applicable for the register is not generated. Refer to **12.6.5 Changing Interrupt Control Register Contents**.
2. The IICSEL bit in the PMR register switches functions.

Figure 12.4 Registers TRD0IC, TRD1IC, SSUIC, and IICIC

INTi Interrupt Control Register (i=0 to 3)(2)

Symbol	Address	After Reset
INT2IC	0055h	XX00X000b
INT1IC	0059h	XX00X000b
INT3IC	005Ah	XX00X000b
INT0IC	005Dh	XX00X000b



Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bits	b2 b1 b0 0 0 0 : Level 0 (interrupt disable) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0 : Requests no interrupt 1 : Requests interrupt	RW(1)
POL	Polarity switch bit(4)	0 : Selects falling edge 1 : Selects rising edge(3)	RW
— (b5)	Reserved bit	Set to 0.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

NOTES:
1. Only 0 can be written to the IR bit. (Do not write 1.)
2. Rewrite the interrupt control register when the interrupt request which is applicable for the register is not generated. Refer to **12.6.5 Changing Interrupt Control Register Contents**.
3. If the INTiPL bit in the INTEN register is set to 1 (both edges), set the POL bit to 0 (selects falling edge).
4. The IR bit may be set to 1 (requests interrupt) when the POL bit is rewritten. Refer to **12.6.4 Changing Interrupt Sources.**

Figure 12.5 INTiIC Register

12.1.6.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

12.1.6.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. Then, when the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (= interrupt not requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.
However, the IR bit operations of the timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupt and the I^2C bus Interface Interrupt are different. Refer to **12.5 Timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupts, and I^2C bus Interface Interrupt (Interrupts with Multiple Interrupt Request Sources)**.

12.1.6.3 Bits ILVL2 to ILVL0 and IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 12.3 lists the Settings of Interrupt Priority Levels and Table 12.4 lists the Interrupt Priority Levels Enabled by IPL.

The following are conditions under which an interrupt is acknowledged:

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

Table 12.3 Settings of Interrupt Priority Levels

ILVL2 to ILVL0 Bits	Interrupt Priority Level	Priority Order
000b	Level 0 (interrupt disabled)	–
001b	Level 1	Low
010b	Level 2	↓
011b	Level 3	↓
100b	Level 4	↓
101b	Level 5	↓
110b	Level 6	↓
111b	Level 7	High

Table 12.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Levels
000b	Interrupt level 1 and above
001b	Interrupt level 2 and above
010b	Interrupt level 3 and above
011b	Interrupt level 4 and above
100b	Interrupt level 5 and above
101b	Interrupt level 6 and above
110b	Interrupt level 7 and above
111b	All maskable interrupts are disabled

12.1.6.4 Interrupt Sequence

An interrupt sequence is performed between an interrupt request acknowledgement and interrupt routine execution.

When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, or RMPA instruction if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence. The interrupt sequence is performed as indicated below.

Figure 12.6 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU gets interrupt information (interrupt number and interrupt request level) by reading address 00000h. The IR bit for the corresponding interrupt is set to 0 (interrupt not requested).(2)

(2) The FLG register is saved to a temporary register(1) in the CPU immediately before entering the interrupt sequence.

(3) The I, D and U flags in the FLG register are set as follows:
The I flag is set to 0 (interrupts disabled).
The D flag is set to 0 (single-step interrupt disabled).
The U flag is set to 0 (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt number 32 to 63 is executed.

(4) The CPU's internal temporary register(1) is saved to the stack.

(5) The PC is saved to the stack.

(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.

(7) The starting address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the starting address of the interrupt routine.

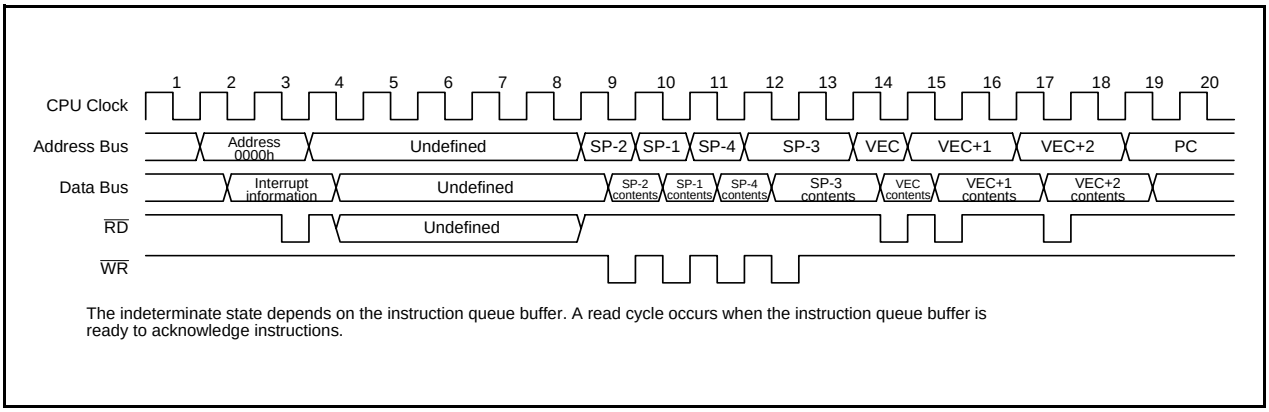


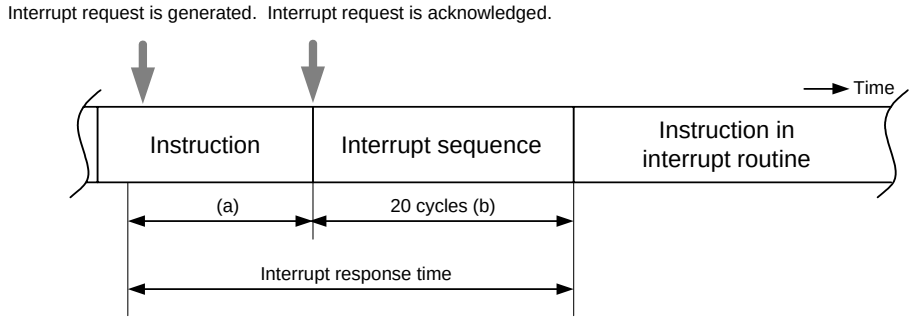
Figure 12.6 Time Required for Executing Interrupt Sequence

NOTES:

1. This register cannot be accessed by the user.
2. Refer to **12.5 Timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupts, and I²C bus Interface Interrupt (Interrupts with Multiple Interrupt Request Sources)** for the IR bit operations of the timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupt, and the I²C bus Interface Interrupt.

12.1.6.5 Interrupt Response Time

Figure 12.7 shows the Interrupt Response Time. The interrupt response time is the period between an interrupt request generation and the execution of the first instruction in the interrupt routine. The interrupt response time includes the period between interrupt request generation and the completion of execution of the instruction (refer to (a) in **Figure 12.7**) and the period required to perform the interrupt sequence (20 cycles, refer to (b) in **Figure 12.7**).



(a) Period between interrupt request generation and the completion of execution of an instruction. The length of time varies depending on the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (assuming no wait states and that a register is set as the divisor).
(b) 21 cycles for address match and single-step interrupts.

Figure 12.7 Interrupt Response Time

12.1.6.6 IPL Change when Interrupt Request is Acknowledged

When an interrupt request of a maskable interrupt is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.
When a software interrupt or special interrupt request is acknowledged, the level listed in Table 12.5 is set in the IPL.
Table 12.5 lists the IPL Value When Software or Special Interrupt Is Acknowledged.

Table 12.5 IPL Value When Software or Special Interrupt Is Acknowledged

Interrupt Source	Value Set in IPL
Watchdog timer, oscillation stop detection, voltage monitor 1, voltage monitor 2, Address break	7
Software, address match, single-step	Not changed

12.1.6.7 Saving a Register

In the interrupt sequence, the FLG register and PC are saved to the stack.
After an extended 16 bits, 4 high-order bits in the PC and 4 high-order (IPL) and 8 low-order bits in the FLG register, are saved to the stack, the 16 low-order bits in the PC are saved.
Figure 12.8 shows the Stack State Before and After Acknowledgement of Interrupt Request.
The other necessary registers are saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used(1) with a single instruction.

NOTE:
1. Selectable from registers R0, R1, R2, R3, A0, A1, SB, and FB.

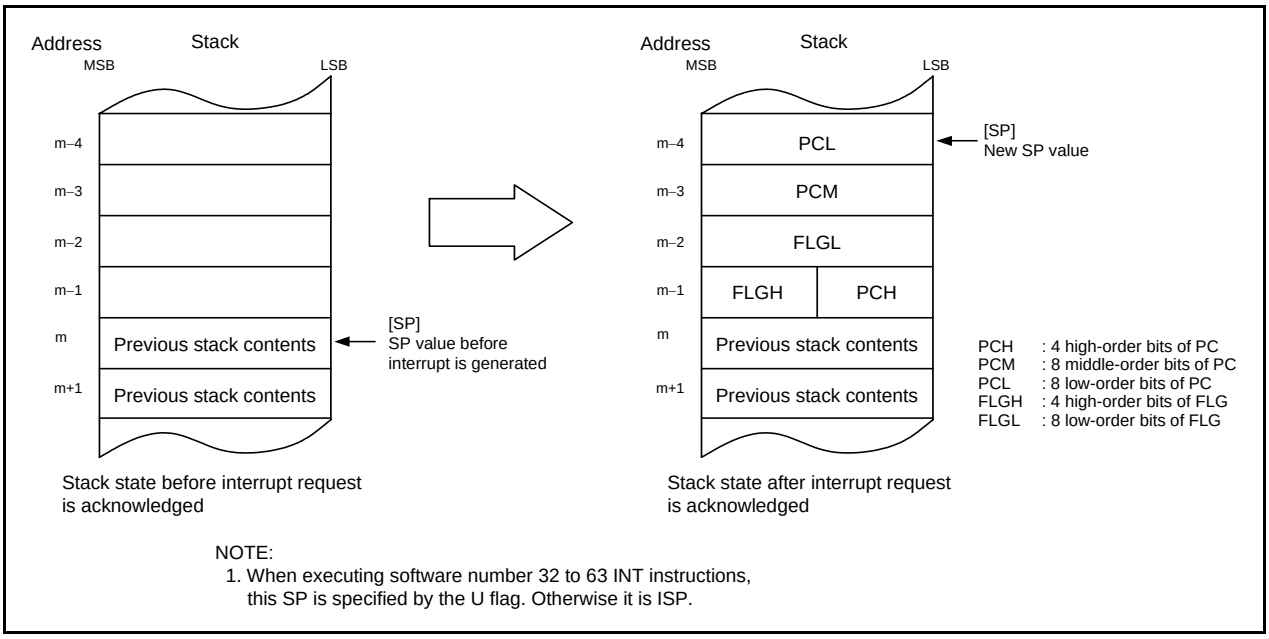


Figure 12.8 Stack State Before and After Acknowledgement of Interrupt Request

The register saving operation, which is performed as part of the interrupt sequence, saved in 8 bits at a time in four steps.
Figure 12.9 shows the Register Saving Operation.

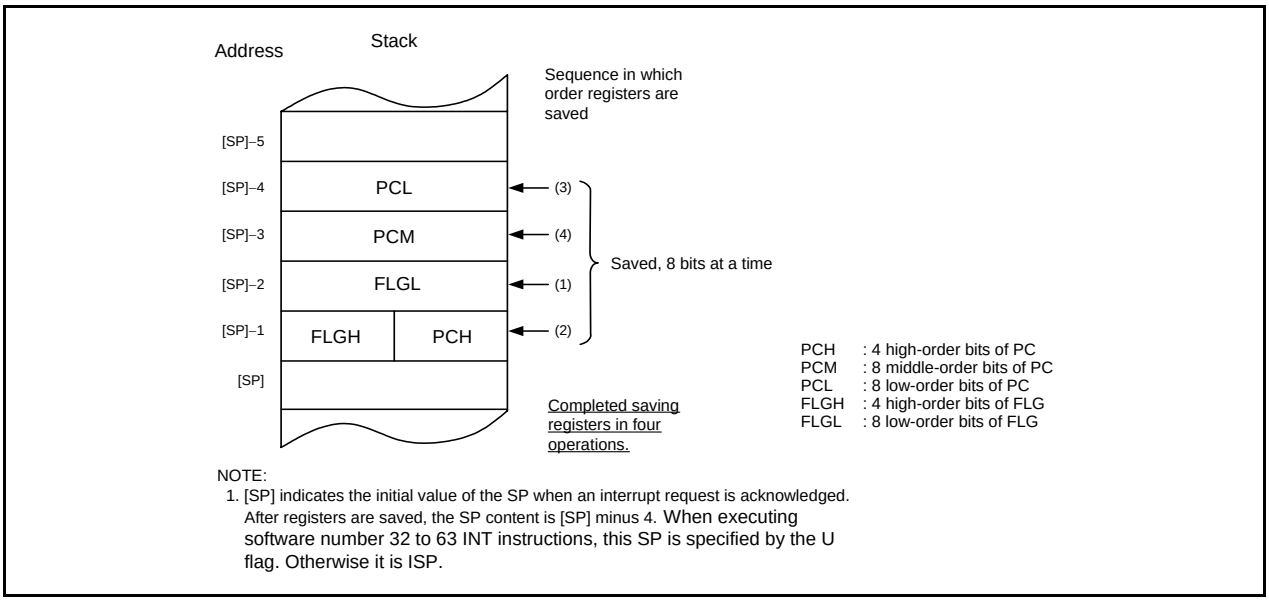


Figure 12.9 Register Saving Operation

12.1.6.8 Returning from an Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved to the stack, are automatically restored. The program, that was running before the interrupt request was acknowledged, starts running again.

Restore registers saved by a program in an interrupt routine using the POPM instruction or others before executing the REIT instruction.

12.1.6.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Set bits ILVL2 to ILVL0 to select the desired priority level for maskable interrupts (peripheral functions). However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, and the higher priority interrupts acknowledged.

The priority levels of special interrupts, such as reset (reset has the highest priority) and watchdog timer, are set by hardware.

Figure 12.10 shows the Priority Levels of Hardware Interrupts.

The interrupt priority does not affect software interrupts. The MCU jumps to the interrupt routine when the instruction is executed.

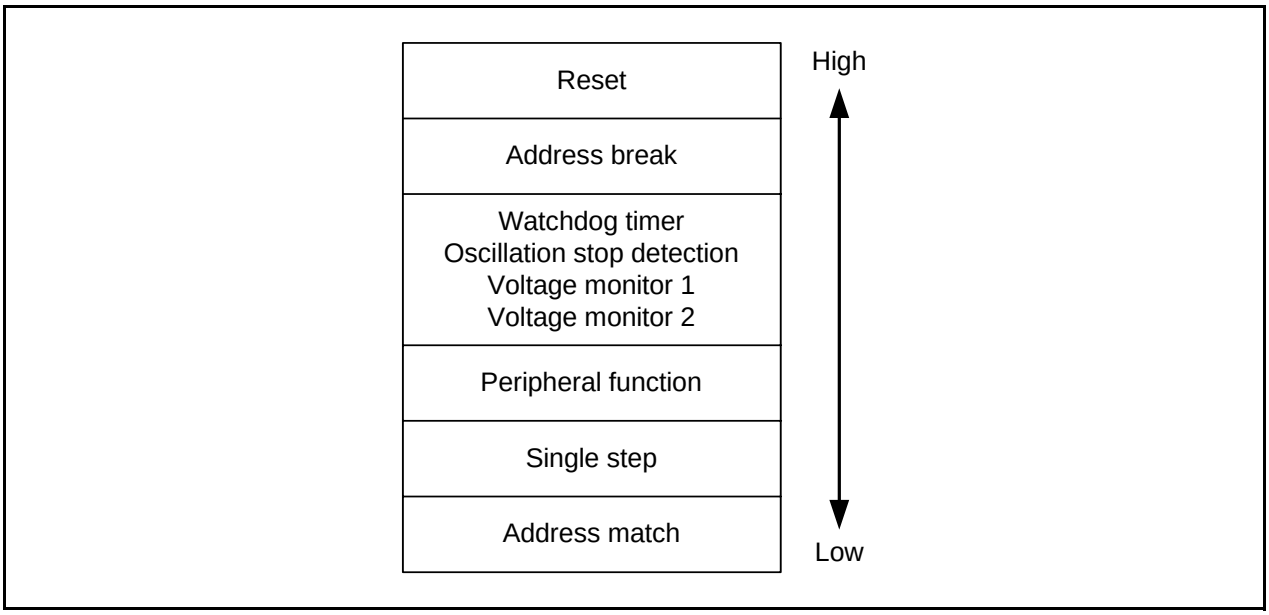


Figure 12.10 Priority Levels of Hardware Interrupts

12.1.6.10 Interrupt Priority Judgement Circuit

The interrupt priority judgement circuit selects the highest priority interrupt, as shown in Figure 12.11.

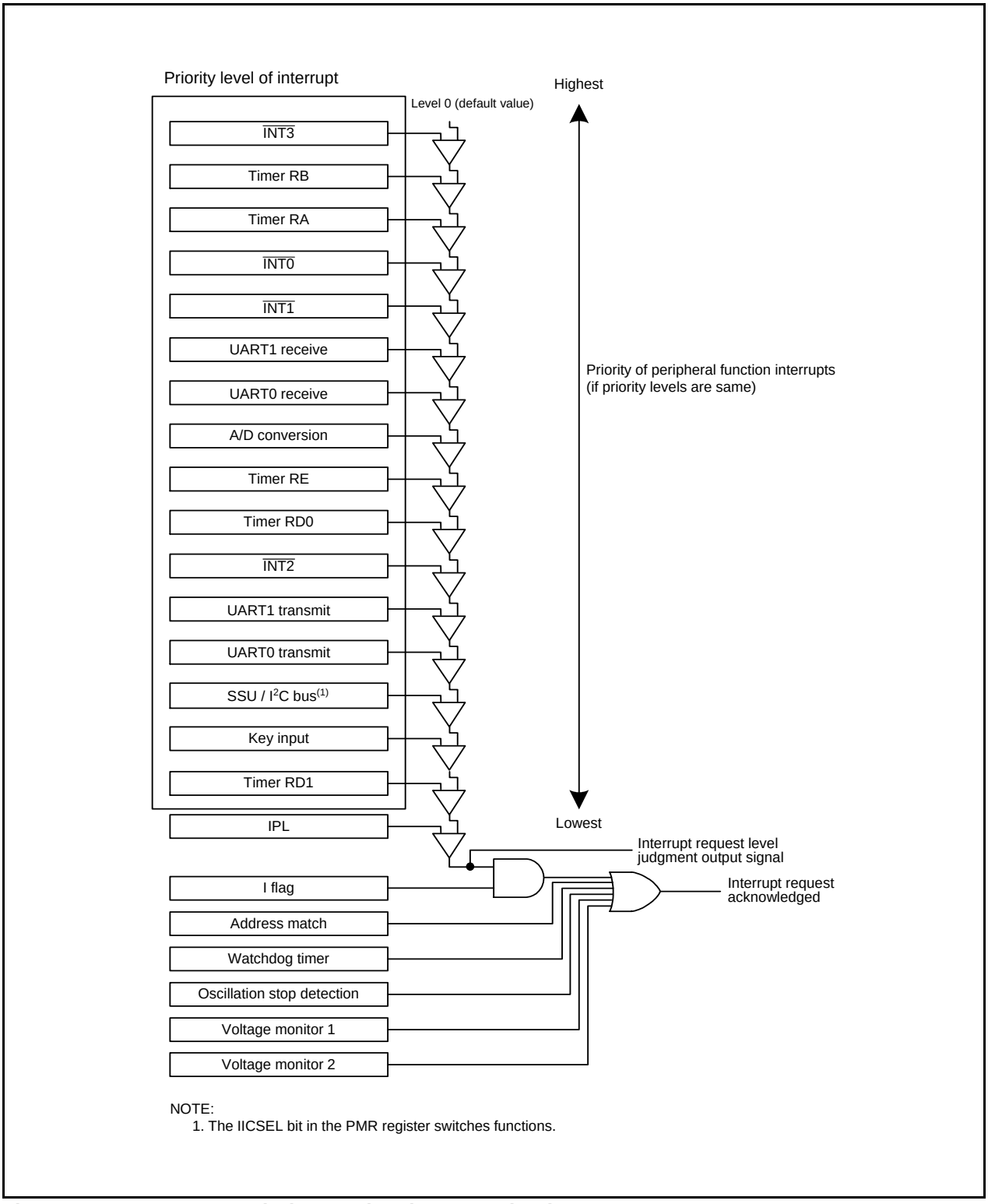


Figure 12.11 Interrupt Priority Level Judgement Circuit

12.2 $\overline{\text{INT}}$ Interrupt

12.2.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 3)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. When using the $\overline{\text{INTi}}$ interrupt, the INTiEN bit in the INTEN register is set to 1 (enable). The edge polarity is selected using the INTiPL bit in the INTEN register and the POL bit in the INTiIC register.
Inputs can be passed through a digital filter with three different sampling clocks.
The $\overline{\text{INT0}}$ pin is shared with the pulse output forced cutoff of timer RD and the external trigger input of timer RB.
Figure 12.12 shows the INTEN Register. Figure 12.13 shows the INTF Register.

External Input Enable Register

b7 b6 b5 b4 b3 b2 b1 b0

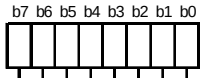
Symbol	Address	After Reset
INTEN	00F9h	00h

Bit Symbol	Bit Name	Function	RW
INT0EN	$\overline{\text{INT0}}$ input enable bit	0 : Disable 1 : Enable	RW
INT0PL	$\overline{\text{INT0}}$ input polarity select bit(1,2)	0 : One edge 1 : Both edges	RW
INT1EN	$\overline{\text{INT1}}$ input enable bit	0 : Disable 1 : Enable	RW
INT1PL	$\overline{\text{INT1}}$ input polarity select bit(1,2)	0 : One edge 1 : Both edges	RW
INT2EN	$\overline{\text{INT2}}$ input enable bit	0 : Disable 1 : Enable	RW
INT2PL	$\overline{\text{INT2}}$ input polarity select bit(1,2)	0 : One edge 1 : Both edges	RW
INT3EN	$\overline{\text{INT3}}$ input enable bit	0 : Disable 1 : Enable	RW
INT3PL	$\overline{\text{INT3}}$ input polarity select bit(1,2)	0 : One edge 1 : Both edges	RW

NOTES:
1. When setting the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (selects falling edge).
2. The IR bit in the INTiIC register may be set to 1 (requests interrupt) when the INTiPL bit is rewritten. Refer to **12.6.4 Changing Interrupt Sources.**

Figure 12.12 INTEN Register

$\overline{INT0}$ Input Filter Select Register



Symbol: INTF | Address: 00FAh | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
INT0F0	$\overline{INT0}$ input filter select bits	b1 b0 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
INT0F1			RW
INT1F0	$\overline{INT1}$ input filter select bits	b3 b2 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
INT1F1			RW
INT2F0	$\overline{INT2}$ input filter select bits	b5 b4 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
INT2F1			RW
INT3F0	$\overline{INT3}$ input filter select bits	b7 b6 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
INT3F1			RW

Figure 12.13 INTF Register

12.2.2 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3)

The $\overline{\text{INTi}}$ input contains a digital filter. The sampling clock is selected by bits INTiF1 to INTiF0 in the INTF register.

The $\overline{\text{INTi}}$ level is sampled every sampling clock cycle and if the sampled input level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).

Figure 12.14 shows the Configuration of $\overline{\text{INTi}}$ Input Filter. Figure 12.15 shows an Operating Example of $\overline{\text{INTi}}$ Input Filter.

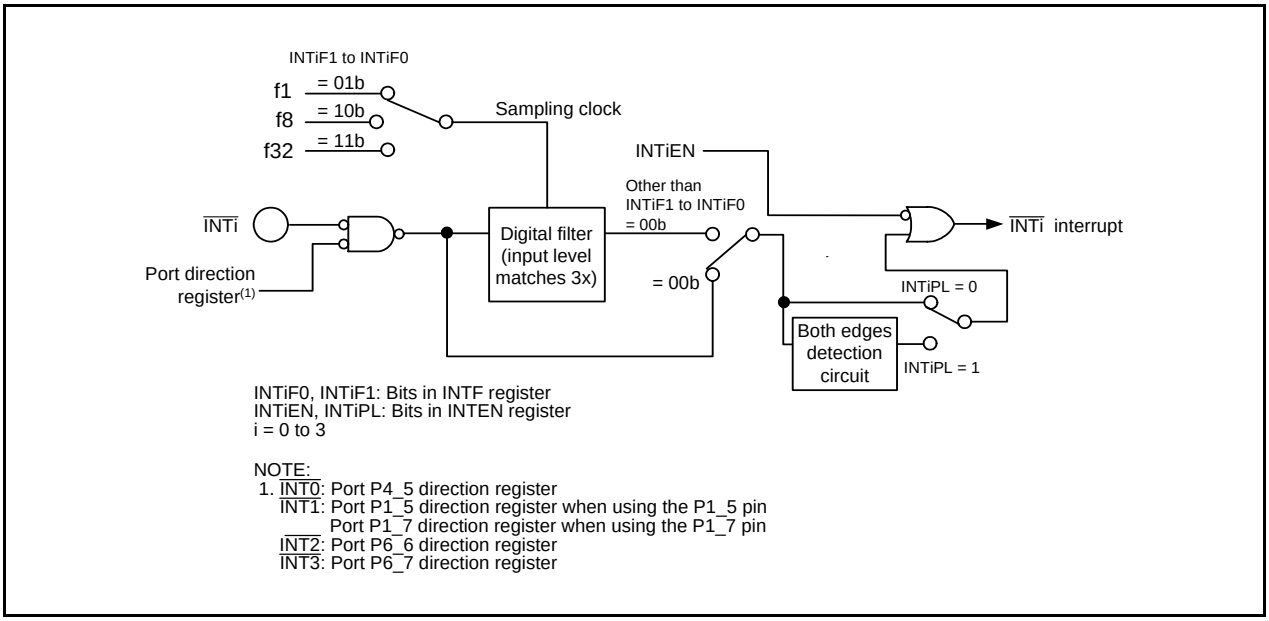


Figure 12.14 Configuration of $\overline{\text{INTi}}$ Input Filter

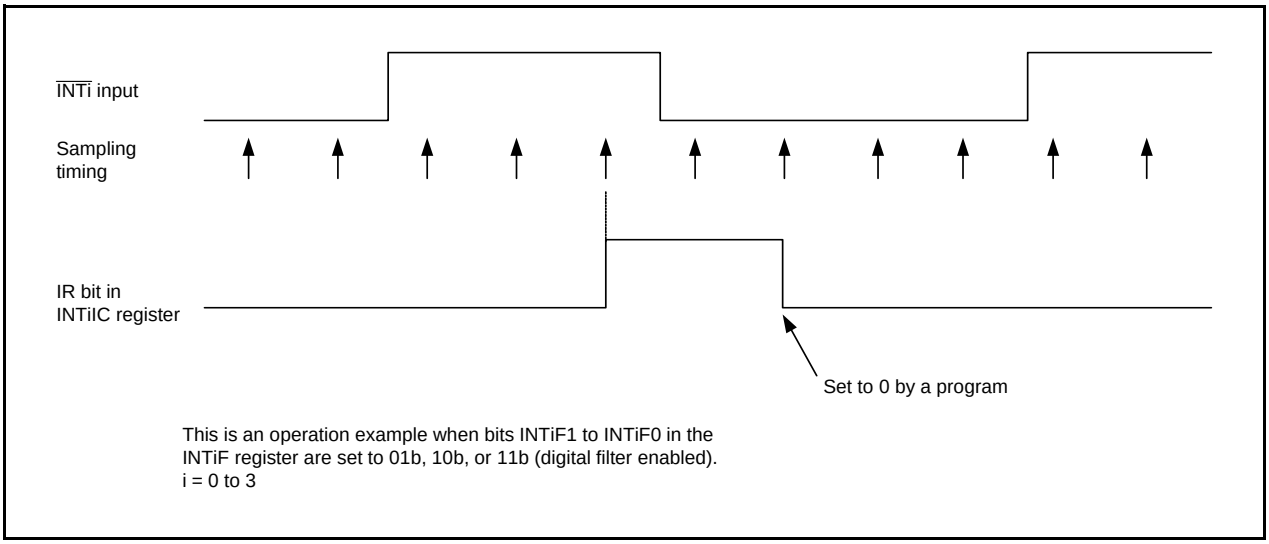


Figure 12.15 Operating Example of $\overline{\text{INTi}}$ Input Filter

12.3 Key Input Interrupt

A key input interrupt request is generated by one of the input edges of pins $\overline{K10}$ to $\overline{K13}$. The key input interrupt can be used as a key-on wake-up function to exit wait or stop mode.

The KIiEN (i = 0 to 3) bit in the KIEN register can select whether or not the pins are used as $\overline{KIi}$ input. The KIiPL bit in the KIEN register can select the input polarity.

When inputting "L" to the $\overline{KIi}$ pin which sets the KIiPL bit to 0 (falling edge), the input of the other pins $\overline{K10}$ to $\overline{K13}$ is not detected as interrupts. Also, when inputting "H" to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), the input of the other pins $\overline{K10}$ to $\overline{K13}$ is not detected as interrupts.

Figure 12.16 shows a Block Diagram of Key Input Interrupt.

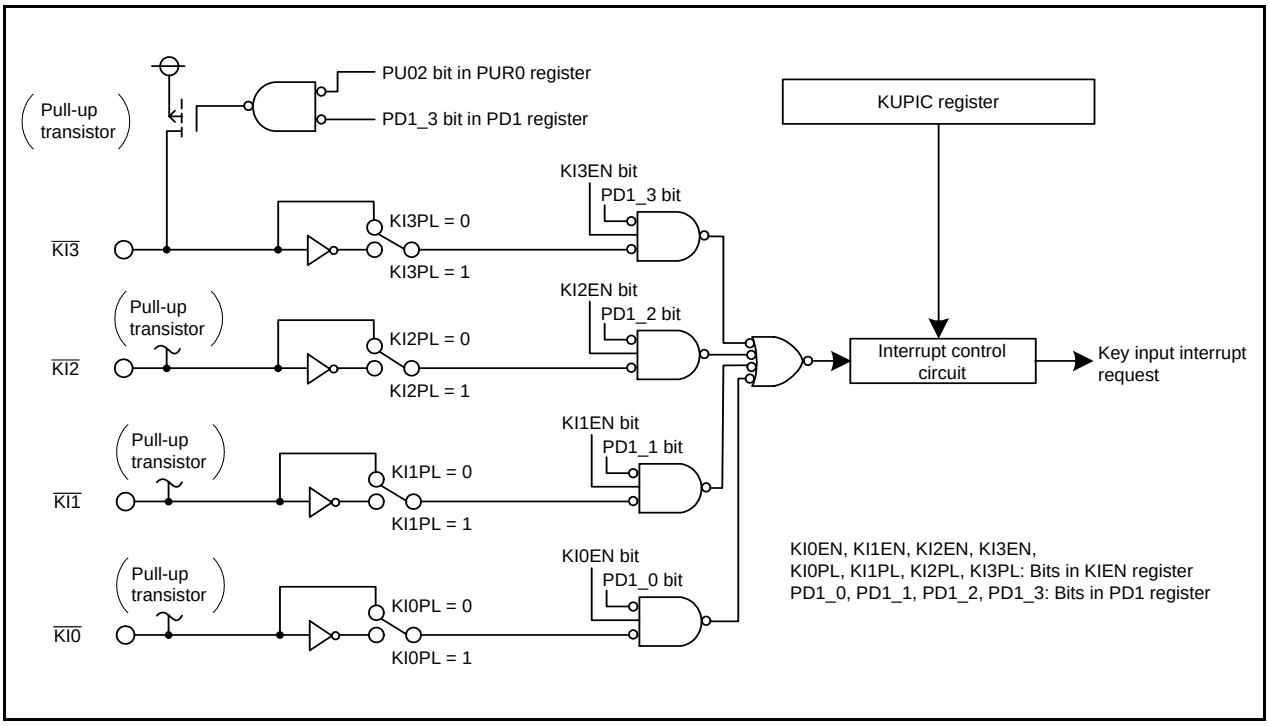


Figure 12.16 Block Diagram of Key Input Interrupt

Key Input Enable Register(1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
KIEN	00FBh	00h

Bit Symbol	Bit Name	Function	RW
KI0EN	KI0 input enable bit	0 : Disable 1 : Enable	RW
KI0PL	KI0 input polarity select bit	0 : Falling edge 1 : Rising edge	RW
KI1EN	KI1 input enable bit	0 : Disable 1 : Enable	RW
KI1PL	KI1 input polarity select bit	0 : Falling edge 1 : Rising edge	RW
KI2EN	KI2 input enable bit	0 : Disable 1 : Enable	RW
KI2PL	KI2 input polarity select bit	0 : Falling edge 1 : Rising edge	RW
KI3EN	KI3 input enable bit	0 : Disable 1 : Enable	RW
KI3PL	KI3 input polarity select bit	0 : Falling edge 1 : Rising edge	RW

NOTE:
1. The IR bit in the KUPIC register may be set to 1 (requests interrupt) when the KIEN register is rewritten. Refer to **12.6.4 Changing Interrupt Sources.**

Figure 12.17 KIEN Register

12.4 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the RMADi register (i = 0 or 1). This interrupt is used as a break function by the debugger. When using the on-chip debugger, do not set an address match interrupt (registers of AIER, RMAD0, and RMAD1 and fixed vector tables) in a user system.

Set the starting address of any instruction in the RMADi register. Bits AIER0 and AIER1 in the AIER0 register can be used to select enable or disable of the interrupt. The I flag and IPL do not affect the address match interrupt.
The value of the PC (Refer to **12.1.6.7 Saving a Register** for the value of the PC) which is saved to the stack when an address match interrupt is acknowledged varies depending on the instruction at the address indicated by the RMADi register. (The appropriate return address is not saved on the stack.) When returning from the address match interrupt, return by one of the following means:

- Change the content of the stack and use the REIT instruction.
- Use an instruction such as POP to restore the stack as it was before the interrupt request was acknowledged. Then use a jump instruction.

Table 12.6 lists the Values of PC Saved to Stack when Address Match Interrupt is Acknowledged.
Figure 12.18 shows Registers AIER and RMAD0 to RMAD1.

Table 12.6 Values of PC Saved to Stack when Address Match Interrupt is Acknowledged

Address Indicated by RMADi Register (i = 0 or 1)	PC Value Saved(1)
• Instruction with 2-byte operation code(2) • Instruction with 1-byte operation code(2) ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest STNZ #IMM8,dest STZX #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by RMADi register + 2
• Instructions other than the above	Address indicated by RMADi register + 1

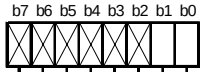
NOTES:

1. Refer to the **12.1.6.7 Saving a Register** for the PC value saved.
2. Operation code: Refer to the **R8C/Tiny Series Software Manual** (REJ09B0001).
   Chapter 4. Instruction Code/Number of Cycles contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 12.7 Correspondence Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER0	RMAD0
Address match interrupt 1	AIER1	RMAD1

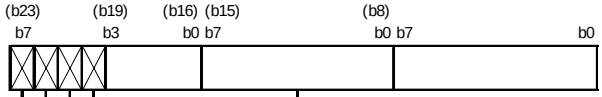
Address Match Interrupt Enable Register



Symbol	Address	After Reset
AIER	0013h	00h

Bit Symbol	Bit Name	Function	RW
AIER0	Address match interrupt 0 enable bit	0 : Disable 1 : Enable	RW
AIER1	Address match interrupt 1 enable bit	0 : Disable 1 : Enable	RW
— (b7-b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Address Match Interrupt Register i (i = 0 or 1)



Symbol	Address	After Reset
RMAD0	0012h-0010h	000000h
RMAD1	0016h-0014h	000000h

Function		Setting Range	RW
Address setting register for address match interrupt		00000h to FFFFFh	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 12.18 Registers AIER and RMAD0 to RMAD1

12.5 Timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupts, and I²C bus Interface Interrupt (Interrupts with Multiple Interrupt Request Sources)

The timer RD (channel 0) interrupt, timer RD (channel 1) interrupt, clock synchronous serial I/O with chip select interrupt, and I²C bus interface interrupt each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request factors and is reflected in the IR bit in the corresponding interrupt control register. Therefore, each of these peripheral functions has its own interrupt request source status register (status register) and interrupt request source enable register (enable register) to control the generation of interrupt requests (change the IR bit in the interrupt control register). Table 12.8 lists the Registers Associated with Timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupt, and I²C bus Interface Interrupt and Figure 12.19 shows a Block Diagram of Timer RD Interrupt.

Table 12.8 Registers Associated with Timer RD Interrupt, Clock Synchronous Serial I/O with Chip Select Interrupt, and I²C bus Interface Interrupt

		Status Register of Interrupt Request Source	Enable Register of Interrupt Request Source	Interrupt Control Register
Timer RD	Channel 0	TRDSR0	TRDIER0	TRD0IC
	Channel 1	TRDSR1	TRDIER1	TRD1IC
Clock synchronous serial I/O with chip select		SSSR	SSER	SSUIC
I²C bus interface		ICSR	ICIER	IICIC

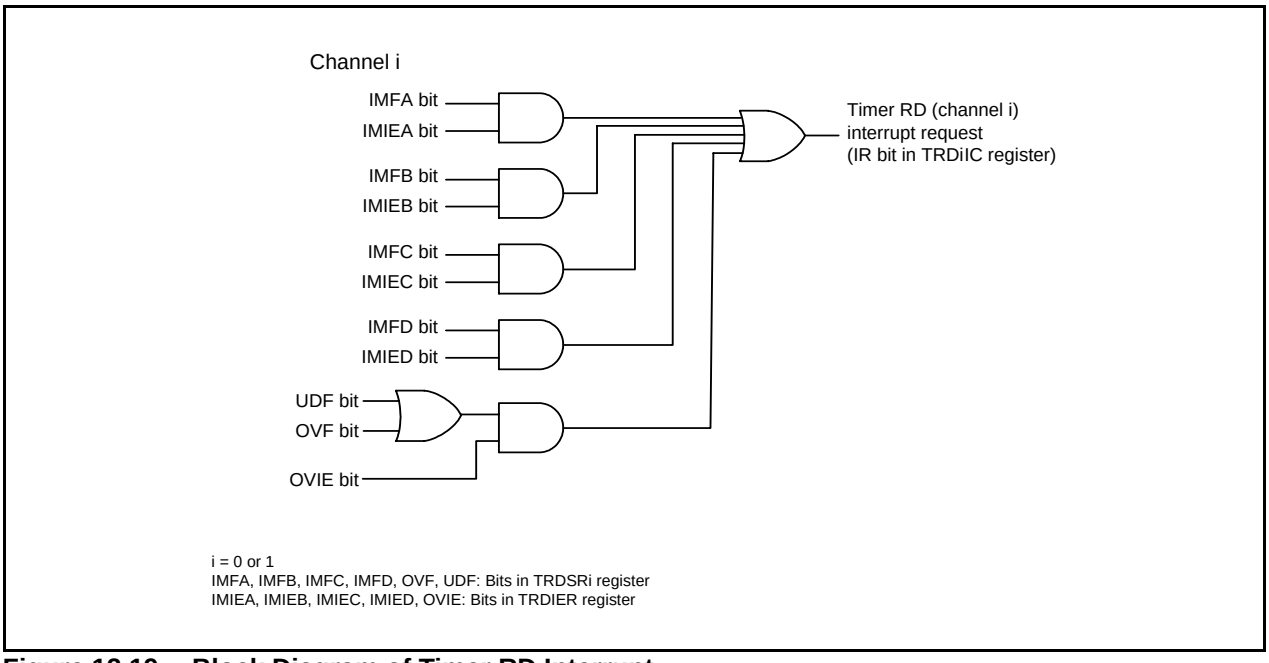


Figure 12.19 Block Diagram of Timer RD Interrupt

As with other maskable interrupts, the timer RD (channel 0) interrupt, timer RD (channel 1) interrupt, clock synchronous serial I/O with chip select interrupt, and I^2C bus interface interrupt are controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since each interrupt source is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the enable register corresponding to bits set to 1 in the status register are set to 1 (enable interrupt), the IR bit in the interrupt control register is set to 1 (interrupt requested).
- When either bits in the status register or bits in the enable register corresponding to bits in the status register, or both, are set to 0, the IR bit is set to 0 (interrupt not requested). Basically, even though the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be maintained. Also, the IR bit is not set to 0 even if 0 is written to the IR bit.
- Individual bits in the status register are not automatically set to 0 even if the interrupt is acknowledged. Therefore, the IR bit is also not automatically set to 0 when the interrupt is acknowledged. Set each bit in the status register to 0 in the interrupt routine. Refer to the status register figure for how to set individual bits in the status register to 0.
- When multiple bits in the enable register are set to 1 and other request sources are generated after the IR bit is set to 1, the IR bit remains 1.
- When multiple bits in the enable register are set to 1, determine by the status register which request source causes an interrupt.

Refer to chapters of the individual peripheral functions (**14.3 Timer RD**, **16.2 Clock Synchronous Serial I/O with Chip Select (SSU)** and **16.3 I^2C bus Interface**) for the status register and enable register.
Refer to **12.1.6 Interrupt Control** for the interrupt control register.

12.6 Notes on Interrupts

12.6.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the acknowledged interrupt IR bit is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

12.6.2 SP Setting

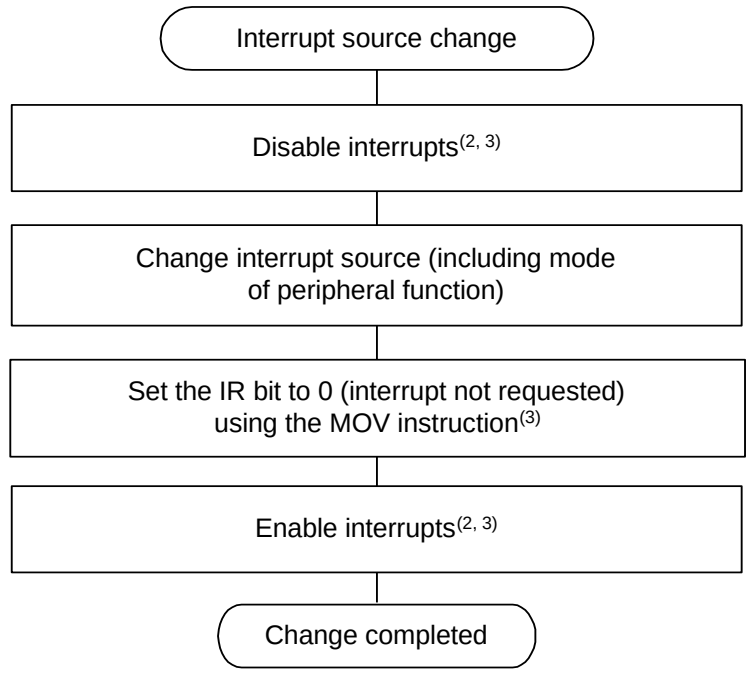
Set any value in the SP before an interrupt is acknowledged. The SP is set to 0000h after reset. Therefore, if an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

12.6.3 External Interrupt and Key Input Interrupt

Either “L” level or an “H” level of width shown in the Electrical Characteristics is necessary for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, regardless of the CPU clock.
For details, refer to **Table 20.21** (VCC = 5V), **Table 20.27** (VCC = 3V), **Table 20.33** (VCC = 2.2V) **External Interrupt $\overline{\text{INT}}$i (i = 0 to 3) Input**.

12.6.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. When using an interrupt, set the IR bit to 0 (no interrupt requested) after changing the interrupt source. In addition, changes of interrupt sources include all factors that change the interrupt sources assigned to individual software interrupt numbers, polarities, and timing. Therefore, if a mode change of a peripheral function involves interrupt sources, edge polarities, and timing, set the IR bit to 0 (no interrupt requested) after the change. Refer to the individual peripheral function for its related interrupts.
Figure 12.20 shows an Example of Procedure for Changing Interrupt Sources.



IR bit: The interrupt control register bit of an interrupt whose source is changed.

NOTES:
1. Execute the above settings individually. Do not execute two or more settings at once (by one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled. If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 of the interrupt whose source is changed.
3. Refer to **12.6.5 Changing Interrupt Control Register Contents** for the instructions to be used and usage notes.

Figure 12.20 Example of Procedure for Changing Interrupt Sources

12.6.5 Changing Interrupt Control Register Contents

(a) The contents of an interrupt control register can only be changed while no interrupt requests corresponding to that register are generated. If interrupt requests may be generated, disable interrupts before changing the interrupt control register contents.

(b) When changing the contents of an interrupt control register after disabling interrupts, be careful to choose appropriate instructions.
Changing any bit other than IR bit
If an interrupt request corresponding to a register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt request may be ignored. If this causes a problem, use the following instructions to change the register: AND, OR, BCLR, BSET
Changing IR bit
If the IR bit is set to 0 (interrupt not requested), it may not be set to 0 depending on the instruction used. Therefore, use the MOV instruction to set the IR bit to 0.

(c) When disabling interrupts using the I flag, set the I flag as shown in the sample programs below. Refer to (b) regarding changing the contents of interrupt control registers by the sample programs.

Sample programs 1 to 3 are for preventing the I flag from being set to 1 (interrupts enabled) before the interrupt control register is changed for reasons of the internal bus or the instruction queue buffer.

Example 1: Use NOP instructions to prevent I flag from being set to 1 before interrupt control register is changed

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use dummy read to delay FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use POPC instruction to change I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

13. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system. The watchdog timer contains a 15-bit counter and allows selection of count source protection mode enable or disable.
Table 13.1 lists information on the Count Source Protection Mode.
Refer to **5.6 Watchdog Timer Reset** for details on the watchdog timer.
Figure 13.1 shows the Block Diagram of Watchdog Timer. Figure 13.2 shows the Registers OFS and WDC, Figure 13.3 shows Registers WDTR, WDTS, and CSPR.

Table 13.1 Count Source Protection Mode

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Low-speed on-chip oscillator clock
Count operation	Decrement	
Count start condition	Either of the following can be selected • After reset, count starts automatically • Count starts by writing to WDTS register	
Count stop condition	Stop mode, wait mode	None
Reset condition of watchdog timer	• Reset • Write 00h to the WDTR register before writing FFh • Underflow	
Operation at the time of underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset

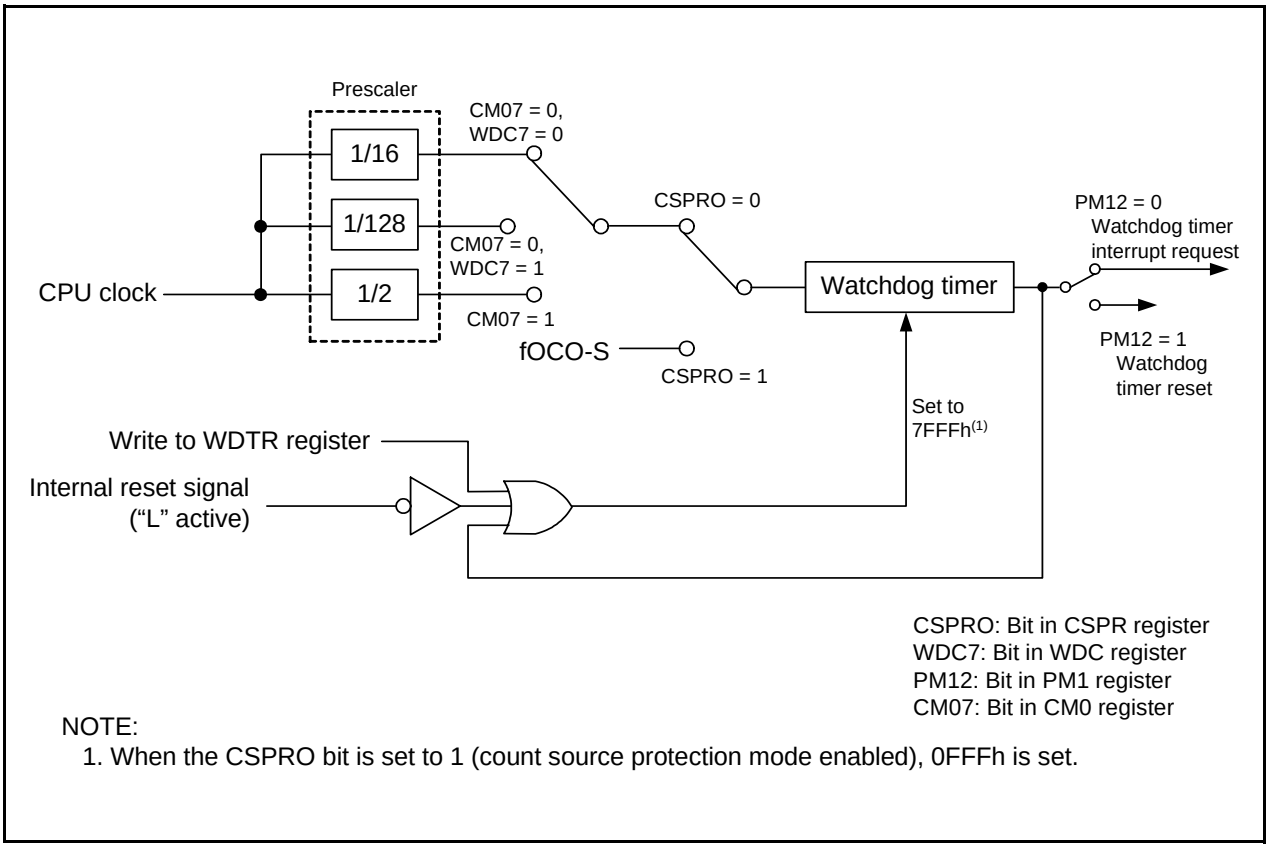


Figure 13.1 Block Diagram of Watchdog Timer

Option Function Select Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
	1		1			1	

Symbol	Address	When Shipping
OFS	0FFFFh	FFh(3)

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Starts watchdog timer automatically after reset 1 : Watchdog timer is inactive after reset	RW
— (b1)	Reserved bit	Set to 1.	RW
ROMCR	ROM code protect disabled bit	0 : ROM code protect disabled 1 : ROMCP1 enabled	RW
ROMCP1	ROM code protect bit	0 : ROM code protect enabled 1 : ROM code protect disabled	RW
— (b4)	Reserved bit	Set to 1.	RW
LVD0ON	Voltage detection 0 circuit start bit(2)	0 : Voltage monitor 0 reset enabled after hardware reset 1 : Voltage monitor 0 reset disabled after hardware reset	RW
— (b6)	Reserved bit	Set to 1.	RW
CSPROINI	Count source protect mode after reset select bit	0 : Count source protect mode enabled after reset 1 : Count source protect mode disabled after reset	RW

NOTES:
1. The OFS register is on the flash memory. Write to the OFS register with a program. After writing is completed, do not write additions to the OFS register.
2. To use the power-on reset, set the LVD0ON bit to 0 (voltage monitor 0 reset enabled after reset).
3. If the block including the OFS register is erased, FFh is set to the OFS register.

Watchdog Timer Control Register

b7	b6	b5	b4	b3	b2	b1	b0
	0	0					

Symbol	Address	After Reset
WDC	000Fh	00X11111b

Bit Symbol	Bit Name	Function	RW
— (b4-b0)	High-order bits of watchdog timer		RO
— (b5)	Reserved bit	Set to 0. When read, the content is undefined.	RW
— (b6)	Reserved bit	Set to 0.	RW
WDC7	Prescaler select bit	0 : Divide-by-16 1 : Divide-by-128	RW

Figure 13.2 Registers OFS and WDC

Watchdog Timer Reset Register

b7 b0

Symbol	Address	After Reset
WDTR	000Dh	Undefined

Function	RW
When 00h is written before writing FFh, the watchdog timer is reset.(1) The default value of the watchdog timer is 7FFFh when count source protection mode is disabled and 0FFFh when count source protection mode is enabled.(2)	WO

NOTES:
1. Do not generate an interrupt between when 00h and FFh are written.
2. When the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled), 0FFFh is set in the watchdog timer.

Watchdog Timer Start Register

b7 b0

Symbol	Address	After Reset
WDTS	000Eh	Undefined

Function	RW
The watchdog timer starts counting after a write instruction to this register.	WO

Count Source Protection Mode Register

b7 b6 b5 b4 b3 b2 b1 b0
0 0 0 0 0 0 0

Symbol	Address	After Reset(1)
CSPR	001Ch	00h

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Reserved bits	Set to 0.	RW
CSPRO	Count source protection mode select bit(2)	0 : Count source protection mode disabled 1 : Count source protection mode enabled	RW

NOTES:
1. When 0 is written to the CSPROINI bit in the OFS register, the value after reset is 10000000b.
2. Write 0 before writing 1 to set the CSPRO bit to 1. 0 cannot be set by a program.

Figure 13.3 Registers WDTR, WDTS, and CSPR

13.1 Count Source Protection Mode Disabled

The count source of the watchdog timer is the CPU clock when count source protection mode is disabled. Table 13.2 lists the Watchdog Timer Specifications (with Count Source Protection Mode Disabled).

Table 13.2 Watchdog Timer Specifications (with Count Source Protection Mode Disabled)

Item	Specification
Count source	CPU clock
Count operation	Decrement
Period	$\frac{\text{Division ratio of prescaler (n)} \times \text{count value of watchdog timer (32768)}^{(1)}}{\text{CPU clock}}$ n: 16 or 128 (selected by WDC7 bit in WDC register) Example: When the CPU clock frequency is 16 MHz and prescaler divided by 16, the period is approximately 32.8 ms
Count start condition	The WDTON bit(2) in the OFS register (0FFFFh) selects the operation of the watchdog timer after a reset • When the WDTON bit is set to 1 (watchdog timer is in stop state after reset) The watchdog timer and prescaler stop after a reset and the count starts when the WDTS register is written to • When the WDTON bit is set to 0 (watchdog timer starts automatically after exiting) The watchdog timer and prescaler start counting automatically after a reset
Reset condition of watchdog timer	• Reset • Write 00h to the WDTR register before writing FFh • Underflow
Count stop condition	Stop and wait modes (inherit the count from the held value after exiting modes)
Operation at time of underflow	• When the PM12 bit in the PM1 register is set to 0 Watchdog timer interrupt • When the PM12 bit in the PM1 register is set to 1 Watchdog timer reset (refer to **5.6 Watchdog Timer Reset**)

NOTES:
1. The watchdog timer is reset when 00h is written to the WDTR register before FFh. The prescaler is reset after the MCU is reset. Some errors in the period of the watchdog timer may be caused by the prescaler.
2. The WDTON bit cannot be changed by a program. To set the WDTON bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.

13.2 Count Source Protection Mode Enabled

The count source of the watchdog timer is the low-speed on-chip oscillator clock when count source protection mode is enabled. If the CPU clock stops when a program is out of control, the clock can still be supplied to the watchdog timer.
Table 13.3 lists the Watchdog Timer Specifications (with Count Source Protection Mode Enabled).

Table 13.3 Watchdog Timer Specifications (with Count Source Protection Mode Enabled)

Item	Specification
Count source	Low-speed on-chip oscillator clock
Count operation	Decrement
Period	Count value of watchdog timer (4096) Low-speed on-chip oscillator clock Example: Period is approximately 32.8 ms when the low-speed on-chip oscillator clock frequency is 125 kHz
Count start condition	The WDTON bit(1) in the OFS register (0FFFFh) selects the operation of the watchdog timer after a reset. • When the WDTON bit is set to 1 (watchdog timer is in stop state after reset) The watchdog timer and prescaler stop after a reset and the count starts when the WDTS register is written to • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset) The watchdog timer and prescaler start counting automatically after a reset
Reset condition of watchdog timer	• Reset • Write 00h to the WDTR register before writing FFh • Underflow
Count stop condition	None (The count does not stop in wait mode after the count starts. The MCU does not enter stop mode.)
Operation at time of underflow	Watchdog timer reset (Refer to **5.6 Watchdog Timer Reset.**)
Registers, bits	• When setting the CSPPRO bit in the CSPR register to 1 (count source protection mode is enabled)(2), the following are set automatically - Set 0FFFh to the watchdog timer - Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on) - Set the PM12 bit in the PM1 register to 1 (The watchdog timer is reset when watchdog timer underflows) • The following conditions apply in count source protection mode - Writing to the CM10 bit in the CM1 register is disabled (It remains unchanged even if it is set to 1. The MCU does not enter stop mode.) - Writing to the CM14 bit in the CM1 register is disabled (It remains unchanged even if it is set to 1. The low-speed on-chip oscillator does not stop.)

NOTES:
1. The WDTON bit cannot be changed by a program. To set the WDTON bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
2. Even if 0 is written to the CSPROINI bit in the OFS register, the CSPRO bit is set to 1.
The CSPROINI bit cannot be changed by a program. To set the CSPROINI bit, write 0 to bit 7 of address 0FFFFh with a flash programmer.

14. Timers

The MCU has two 8-bit timers with 8-bit prescalers, two 16-bit timers, and a timer with a 4-bit counter and an 8-bit counter. The two 8-bit timers with 8-bit prescalers are timer RA and timer RB. These timers contain a reload register to store the default value of the counter. The 16-bit timer is timer RD, and has input capture and output compare functions. The 4 and 8-bit counters are timer RE, and has an output compare function. All the timers operate independently.
Table 14.1 lists Functional Comparison of Timers.

Table 14.1 Functional Comparison of Timers

Item		Timer RA	Timer RB	Timer RD	Timer RE
Configuration		8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	16-bit free-run timer × 2 (with input capture and output compare)	4-bit counter 8-bit counter
Count		Decrement	Decrement	Increment/Decrement	Increment
Count sources		• f1 • f2 • f8 • fOCO • fC32	• f1 • f2 • f8 • Timer RA underflow	• f1 • f2 • f4 • f8 • f32 • fOCO40M • TRDIOA0	• f4 • f8 • f32 • fC4
Function	Timer mode	Provided	Provided	Provided (input capture function, output compare function)	Not provided
	Pulse output mode	Provided	Not provided	Not provided	Not provided
	Event counter mode	Provided	Not provided	Not provided	Not provided
	Pulse width measurement mode	Provided	Not provided	Not provided	Not provided
	Pulse period measurement mode	Provided	Not provided	Not provided	Not provided
	Programmable waveform generation mode	Not provided	Provided	Not provided	Not provided
	Programmable one-shot generation mode	Not provided	Provided	Not provided	Not provided
	Programmable wait one-shot generation mode	Not provided	Provided	Not provided	Not provided
	Input capture mode	Not provided	Not provided	Provided	Not provided
	Output compare mode	Not provided	Not provided	Provided	Provided
	PWM mode	Not provided	Not provided	Provided	Not provided
	Reset synchronized PWM mode	Not provided	Not provided	Provided	Not provided
	Complementary PWM mode	Not provided	Not provided	Provided	Not provided
	PWM3 mode	Not provided	Not provided	Provided	Not provided
	Real-time clock mode	Not provided	Not provided	Not provided	Provided
Input pin		TRAIO	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$, TRDCLK, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	–
Output pin		$\overline{\text{TRAO}}$ TRAIO	TRBO	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	TREO
Related interrupt		$\overline{\text{Timer}}$ RA interrupt INT1 interrupt	$\overline{\text{Timer}}$ RB interrupt INT0 interrupt	Compare match/input Capture A0 to D0 interrupt Compare match/input Capture A1 to D1 interrupt Overflow interrupt $\overline{\text{Under}}$flow interrupt(1) INT0 interrupt	Timer RE interrupt
Timer stop		Provided	Provided	Provided	Provided

NOTE:
1. The underflow interrupt can be set to channel 1.

14.1 Timer RA

Timer RA is an 8-bit timer with an 8-bit prescaler.
The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAPRE and TRA (refer to **Tables 14.2 to 14.6 the Specifications of Each Mode**).
The count source for timer RA is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 14.1 shows a Block Diagram of Timer RA. Figures 14.2 and 14.3 show the registers associated with Timer RA.

Timer RA has the following five operating modes:

- Timer mode: The timer counts the internal count source.
- Pulse output mode: The timer counts the internal count source and outputs pulses of which polarity inverted by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.

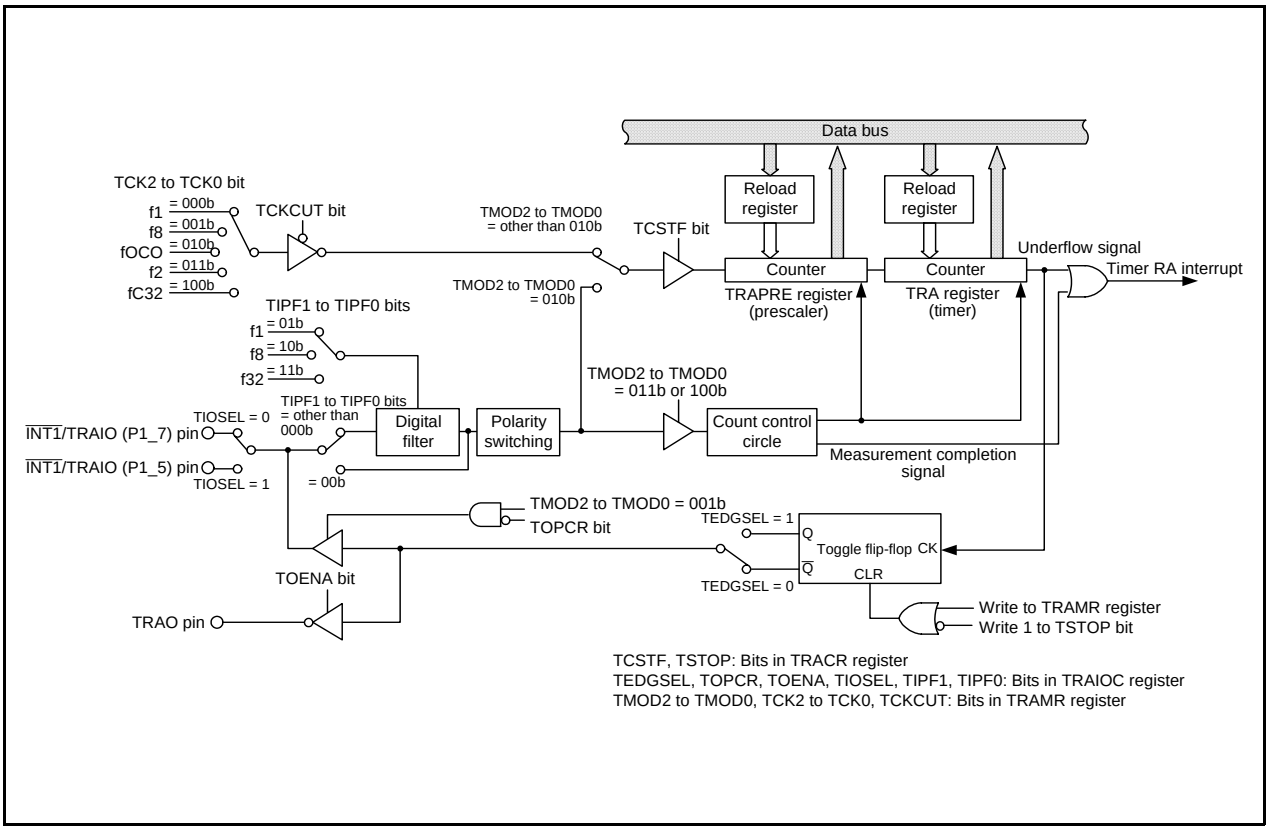
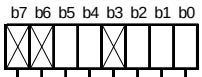


Figure 14.1 Block Diagram of Timer RA

Timer RA Control Register(4)

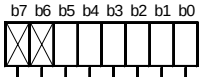


Symbol	Address	After Reset
TRACR	0100h	00h

Bit Symbol	Bit Name	Function	RW
TSTART	Timer RA count start bit(1)	0 : Count stops 1 : Count starts	RW
TCSTF	Timer RA count status flag(1)	0 : Count stops 1 : During count	RO
TSTOP	Timer RA count forcible stop bit(2)	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TEDGF	Active edge judgment flag(3, 5)	0 : Active edge not received 1 : Active edge received (end of measurement period)	RW
TUNDF	Timer RA underflow flag(3, 5)	0 : No underflow 1 : Underflow	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Refer to **14.1.6 Notes on Timer RA**.
2. When the TSTOP bit is set to 1, bits TSTART and TCSTF and registers TPRAPRE and TRA are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRACR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.
5. Set to 0 in timer mode, pulse output mode, and event counter mode.

Timer RA I/O Control Register

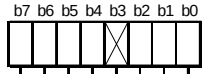


Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	Function varies depending on operating mode.	RW
TOPCR	TRAIO output control bit		RW
TOENA	TRAO output enable bit		RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit		RW
TIPF0 TIPF1	TRAIO input filter select bits		RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 14.2 Registers TRACR and TRAIOC

Timer RA Mode Register(1)

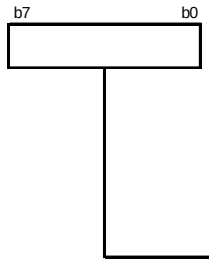


Symbol	Address	After Reset
TRAMR	0102h	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Timer RA operating mode select bits	b2 b1 b0 0 0 0 : Timer mode 0 0 1 : Pulse output mode 0 1 0 : Event counter mode 0 1 1 : Pulse width measurement mode 1 0 0 : Pulse period measurement mode 1 0 1 : 1 1 0 : Do not set. 1 1 1 :	RW
TMOD1			RW
TMOD2			RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCK0	Timer RA count source select bits	b6 b5 b4 0 0 0 : f1 0 0 1 : f8 0 1 0 : fOCO 0 1 1 : f2 1 0 0 : fC32 1 0 1 : 1 1 0 : Do not set. 1 1 1 :	RW
TCK1			RW
TCK2			RW
TCKCUT	Timer RA count source cutoff bit	0 : Provides count source 1 : Cuts off count source	RW

NOTE:
1. When both the TSTART and TCSTF bits in the TRACR register are set to 0 (count stops), rewrite this register.

Timer RA Prescaler Register

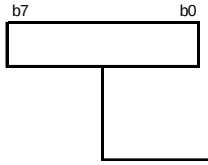


Symbol	Address	After Reset
TRAPRE	0103h	FFh(1)

Mode	Function	Setting Range	RW
Timer mode	Counts an internal count source	00h to FFh	RW
Pulse output mode	Counts an internal count source	00h to FFh	RW
Event counter mode	Counts an external count source	00h to FFh	RW
Pulse width measurement mode	Counts internal count source	00h to FFh	RW
Pulse period measurement mode		00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRACR register is set to 1, the TRAPRE register is set to FFh.

Timer RA Register



Symbol	Address	After Reset
TRA	0104h	FFh(1)

Mode	Function	Setting Range	RW
All modes	Counts on underflow of timer RA prescaler register	00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRACR register is set to 1, the TRA register is set to FFh.

Figure 14.3 Registers TRAMR, TRAPRE, and TRA

14.1.1 Timer Mode

In this mode, the timer counts an internally generated count source (refer to **Table 14.2 Timer Mode Specifications**).
Figure 14.4 shows the TRAIOC Register in Timer Mode.

Table 14.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
$\overline{\text{INT1}}$/TRAIO pin function	Programmable I/O port, or $\overline{\text{INT1}}$ interrupt input
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **14.1.1.1 Timer Write Control during Count Operation**).

Timer RA I/O Control Register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	0	0		0	0	0

Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	RW
TOPCR	TRAIO output control bit		RW
TOENA	TRAO output enable bit		RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0 : $\overline{\text{INT1}}$/TRAIO pin (P1_7) 1 : $\overline{\text{INT1}}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits	Set to 0 in timer mode.	RW
TIPF1			
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

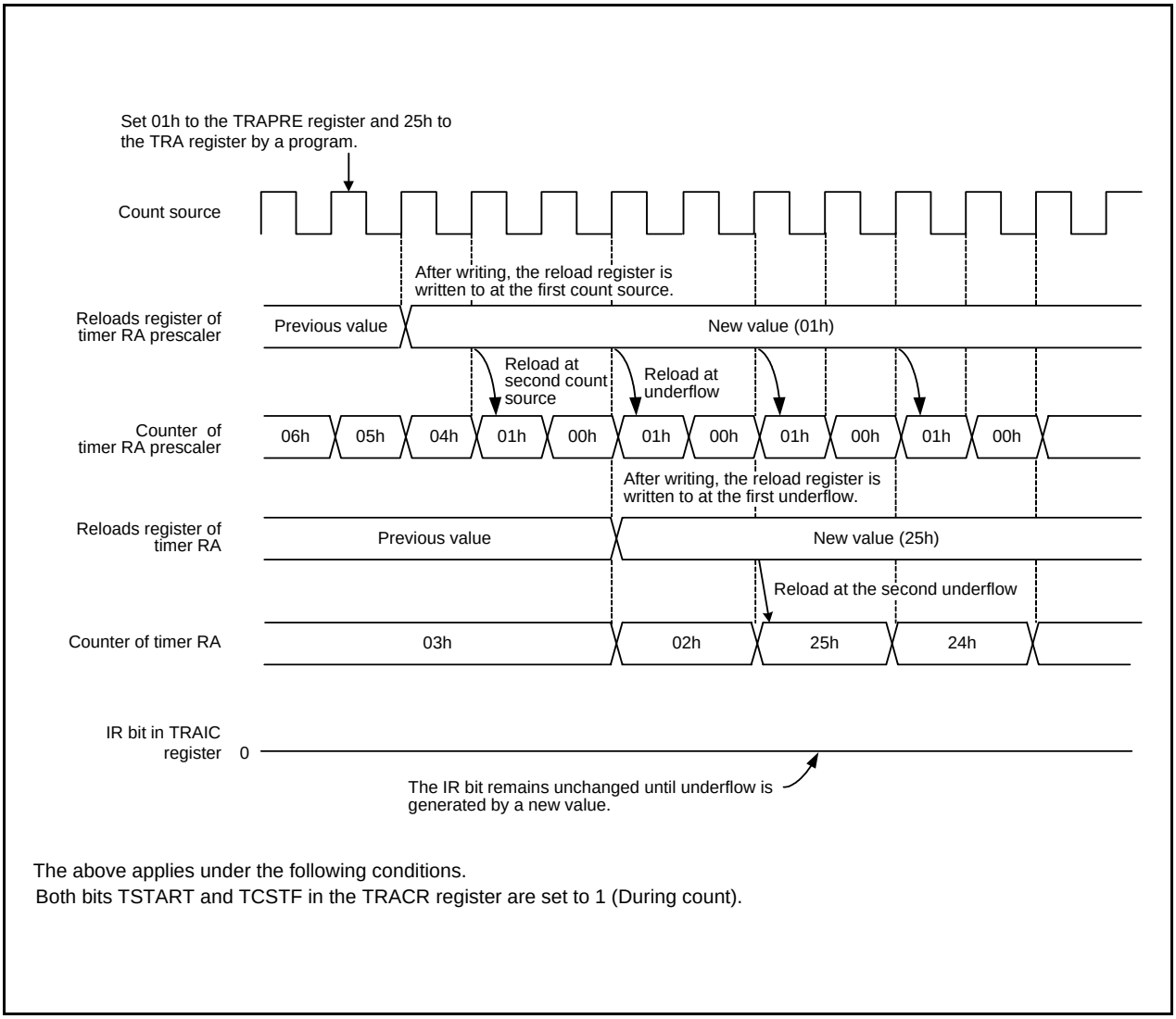
Figure 14.4 TRAIOC Register in Timer Mode

14.1.1.1 Timer Write Control during Count Operation

Timer RA has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. When writing to the prescaler or timer, values are written to both the reload register and counter.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, if the prescaler or timer is written to when count operation is in progress, the counter value is not updated immediately after the WRITE instruction is executed.

Figure 14.5 shows an Operating Example of Timer RA when Counter Value is Rewritten during Count Operation.



The above applies under the following conditions.
Both bits TSTART and TCSTF in the TRACR register are set to 1 (During count).

Figure 14.5 Operating Example of Timer RA when Counter Value is Rewritten during Count Operation

14.1.2 Pulse Output Mode

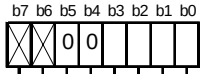
In pulse output mode, the internally generated count source is counted, and a pulse with inverted polarity is output from the TRAIO pin each time the timer underflows (refer to **Table 14.3 Pulse Output Mode Specifications**).
Figure 14.6 shows the TRAIOC Register in Pulse Output Mode.

Table 14.3 Pulse Output Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32
Count operations	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
$\overline{\text{INT1}}$/TRAIO pin function	Pulse output, programmable output port, or $\overline{\text{INT1}}$ interrupt(1)
TRAO pin function	Programmable I/O port or inverted output of TRAIO(1)
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **14.1.1.1 Timer Write Control during Count Operation**).
Select functions	• TRAIO output polarity switch function The TEDGSEL bit in the TRAIOC register selects the level at the start of pulse output.(1) • TRAO output function Pulses inverted from the TRAIO output polarity can be output from the TRAO pin (selectable by the TOENA bit in the TRAIOC register). • Pulse output stop function Output from the TRAIO pin is stopped by the TOPCR bit in the TRAIOC register. • $\overline{\text{INT1}}$/TRAIO pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register.

NOTE:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

Timer RA I/O Control Register



Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : TRAIO output starts at “H” 1 : TRAIO output starts at “L”	RW
TOPCR	TRAIO output control bit	0 : TRAIO output 1 : Port P1_7 or P1_5	RW
TOENA	TRAO output enable bit	0 : Port P3_0 1 : TRAO output (inverted TRAIO output from P3_0)	RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0 : $\overline{\text{INT1}}$/TRAIO pin (P1_7) 1 : $\overline{\text{INT1}}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits	Set to 0 in pulse output mode.	RW
TIPF1			RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 14.6 TRAIOC Register in Pulse Output Mode

14.1.3 Event Counter Mode

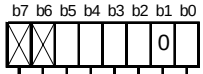
In event counter mode, external signal inputs to the $\overline{INT1}$/TRAIO pin are counted (refer to **Table 14.4 Event Counter Mode Specifications**).
Figure 14.7 shows the TRAIOC Register in Event Counter Mode.

Table 14.4 Event Counter Mode Specifications

Item	Specification
Count source	External signal which is input to TRAIO pin (active edge selectable by a program)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: setting value of TRAPRE register, m: setting value of TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows [timer RA interrupt].
$\overline{INT1}$/TRAIO pin function	Count source input ($\overline{INT1}$ interrupt input)
TRAO pin function	Programmable I/O port or pulse output(1)
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **14.1.1.1 Timer Write Control during Count Operation**).
Select functions	• $\overline{NT1}$ input polarity switch function The TEDGSEL bit in the TRAIOC register selects the active edge of the count source. • Count source input pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register. • Pulse output function Pulses of inverted polarity can be output from the TRAO pin each time the timer underflows (selectable by the TOENA bit in the TRAIOC register).(1) • Digital filter function Bits TIPF0 and TIPF1 in the TRAIOC register enable or disable the digital filter and select the sampling frequency.

NOTE:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

Timer RA I/O Control Register



Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : Starts counting at rising edge of the TRAIO input or TRAIO starts output at "L" 1 : Starts counting at falling edge of the TRAIO input or TRAIO starts output at "H"	RW
TOPCR	TRAIO output control bit	Set to 0 in event counter mode.	RW
TOENA	TRAO output enable bit	0 : Port P3_0 1 : TRAO output	RW
TIOSEL	$\overline{INT1}$/TRAIO select bit	0 : $\overline{INT1}$/TRAIO pin (P1_7) 1 : $\overline{INT1}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits(1)	b5 b4 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
TIPF1			
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

Figure 14.7 TRAIOC Register in Event Counter Mode

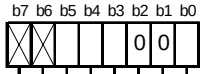
14.1.4 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the $\overline{\text{INT1}}$/TRAIO pin is measured (refer to **Table 14.5 Pulse Width Measurement Mode Specifications**).
Figure 14.8 shows the TRAIOC Register in Pulse Width Measurement Mode and Figure 14.9 shows an Operating Example of Pulse Width Measurement Mode.

Table 14.5 Pulse Width Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32
Count operations	• Decrement • Continuously counts the selected signal only when measurement pulse is “H” level, or conversely only “L” level. • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
$\overline{\text{INT1}}$/TRAIO pin function	Measured pulse input ($\overline{\text{INT1}}$ interrupt input)
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **14.1.1.1 Timer Write Control during Count Operation**).
Select functions	• Measurement level select The TEDGSEL bit in the TRAIOC register selects the “H” or “L” level period. • Measured pulse input pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register. • Digital filter function Bits TIPF0 and TIPF1 in the TRAIOC register enable or disable the digital filter and select the sampling frequency.

Timer RA I/O Control Register



Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : TRAIO input starts at “L” 1 : TRAIO input starts at “H”	RW
TOPCR	TRAIO output control bit	Set to 0 in pulse width measurement mode.	RW
TOENA	TRAO output enable bit		RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0 : $\overline{\text{INT1}}$/TRAIO pin (P1_7) 1 : $\overline{\text{INT1}}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits(1)	b5 b4 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
TIPF1			
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

Figure 14.8 TRAIOC Register in Pulse Width Measurement Mode

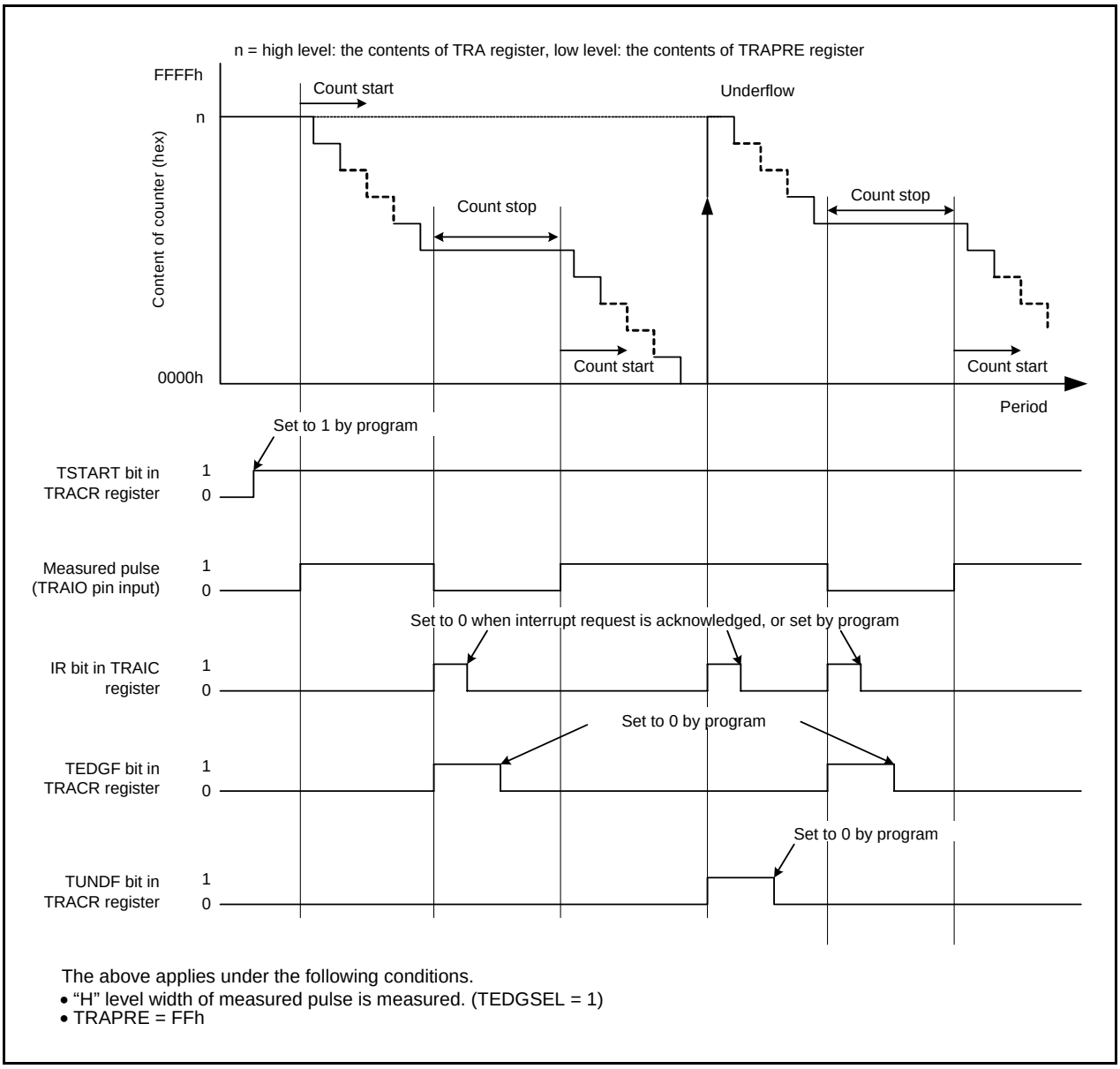


Figure 14.9 Operating Example of Pulse Width Measurement Mode

14.1.5 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the $\overline{\text{INT1}}$/TRAIO pin is measured (refer to **Table 14.6 Pulse Period Measurement Mode Specifications**).
Figure 14.10 shows the TRAIOC Register in Pulse Period Measurement Mode and Figure 14.11 shows an Operating Example of Pulse Period Measurement Mode.

Table 14.6 Pulse Period Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32
Count operations	• Decrement • After the active edge of the measured pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RA prescaler. Then timer RA reloads the contents in the reload register at the second underflow of timer RA prescaler and continues counting.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows or reloads [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
$\overline{\text{INT1}}$/TRAIO pin function	Measured pulse input(1) ($\overline{\text{INT1}}$ interrupt input)
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **14.1.1.1 Timer Write Control during Count Operation**).
Select functions	• Measurement period select The TEDGSEL bit in the TRAIOC register selects the measurement period of the input pulse. • Measured pulse input pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register. • Digital filter function Bits TIPF0 and TIPF1 in the TRAIOC register enable or disable the digital filter and select the sampling frequency.

NOTE:
1. Input a pulse with a period longer than twice the timer RA prescaler period. Input a pulse with a longer “H” and “L” width than the timer RA prescaler period. If a pulse with a shorter period is input to the TRAIO pin, the input may be ignored.

Timer RA I/O Control Register

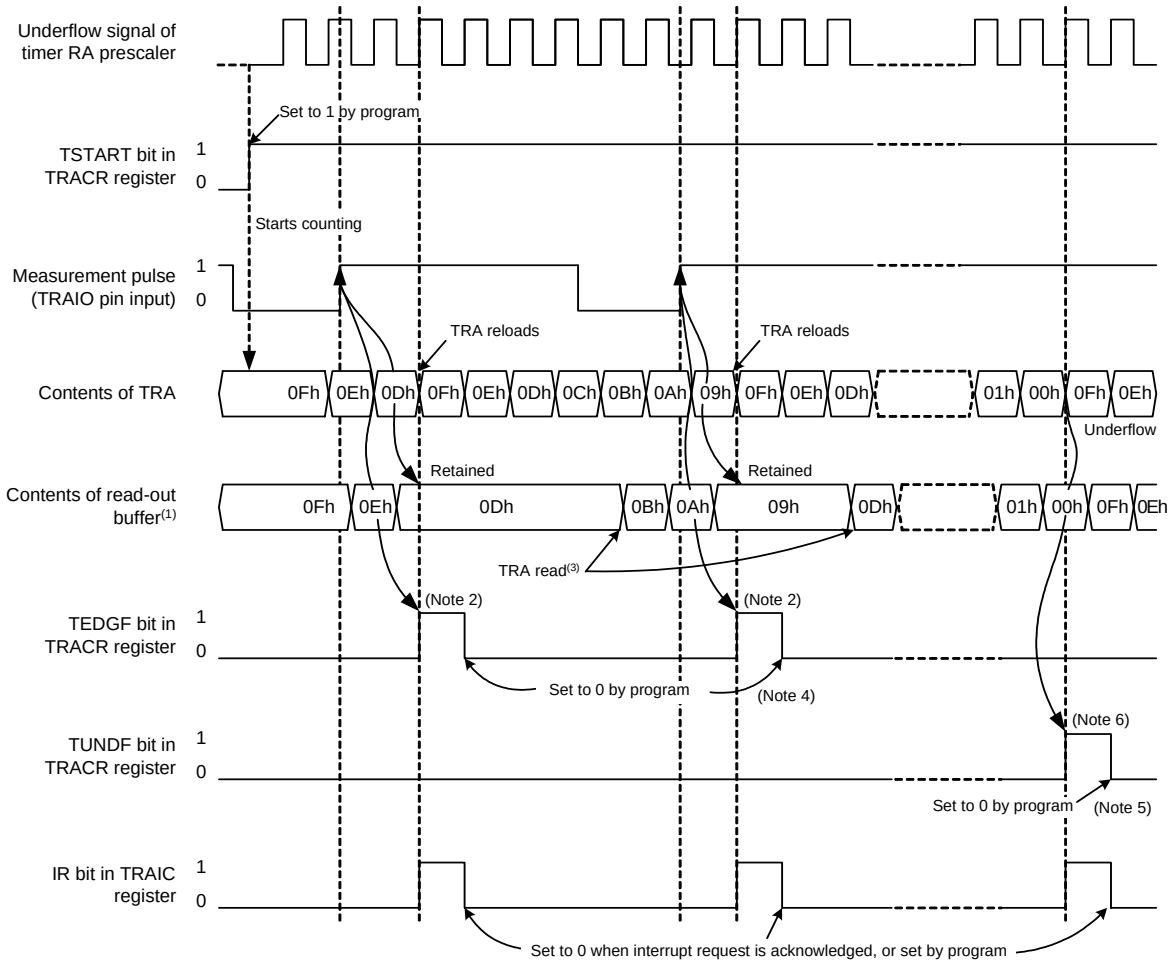
b7	b6	b5	b4	b3	b2	b1	b0
X	X				0	0	

Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : Measures measurement pulse from one rising edge to next rising edge 1 : Measures measurement pulse from one falling edge to next falling edge	RW
TOPCR	TRAIO output control bit	Set to 0 in pulse period measurement mode.	RW
TOENA	TRAO output enable bit		RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0 : $\overline{\text{INT1}}$/TRAIO pin (P1_7) 1 : $\overline{\text{INT1}}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits(1)	b5 b4 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
TIPF1			
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

Figure 14.10 TRAIOC Register in Pulse Period Measurement Mode



Conditions: The period from one rising edge to the next rising edge of the measured pulse is measured (TEDGSEL = 0) with the default value of the TRA register as 0Fh.

NOTES:
1. The contents of the read-out buffer can be read by reading the TRA register in pulse period measurement mode.
2. After an active edge of the measured pulse is input, the TEDGF bit in the TRACR register is set to 1 (active edge found) when the timer RA prescaler underflows for the second time.
3. The TRA register should be read before the next active edge is input after the TEDGF bit is set to 1 (active edge found). The contents in the read-out buffer are retained until the TRA register is read. If the TRA register is not read before the next active edge is input, the measured result of the previous period is retained.
4. To set to 0 by a program, use a MOV instruction to write 0 to the TEDGF bit in the TRACR register. At the same time, write 1 to the TUNDF bit in the TRACR register.
5. To set to 0 by a program, use a MOV instruction to write 0 to the TUNDF bit. At the same time, write 1 to the TEDGF bit.
6. Bits TUNDF and TEDGF are both set to 1 if timer RA underflows and reloads on an active edge simultaneously.

Figure 14.11 Operating Example of Pulse Period Measurement Mode

14.1.6 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after The TCSTF bit is set to 1 (during count).

  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.

  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

14.2 Timer RB

Timer RB is an 8-bit timer with an 8-bit prescaler.
The prescaler and timer each consist of a reload register and counter (refer to **Tables 14.7 to 14.10 the Specifications of Each Mode**).
Timer RB has timer RB primary and timer RB secondary as reload registers.
The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 14.12 shows a Block Diagram of Timer RB. Figures 14.13 to 14.15 show the registers associated with timer RB.

Timer RB has four operation modes listed as follows:

- Timer mode: The timer counts an internal count source (peripheral function clock or timer RA underflows).
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs a delayed one-shot pulse.

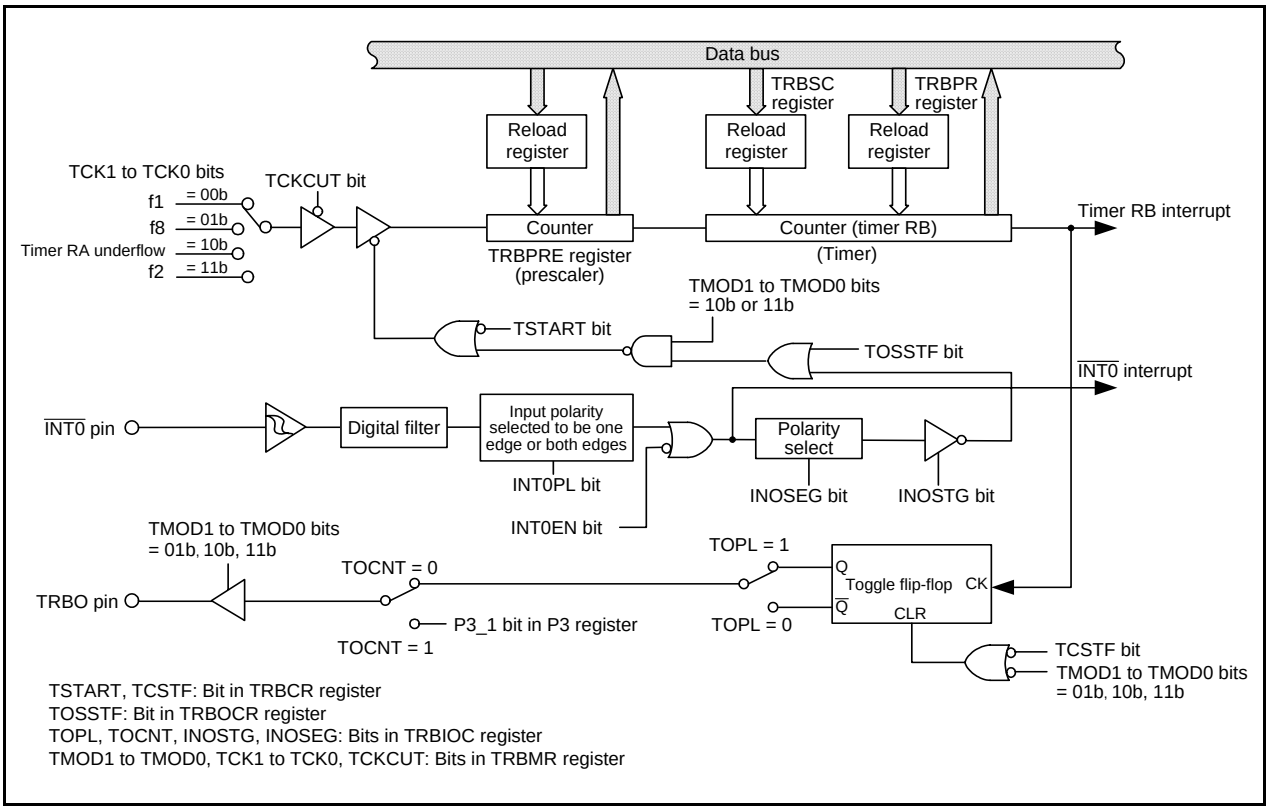
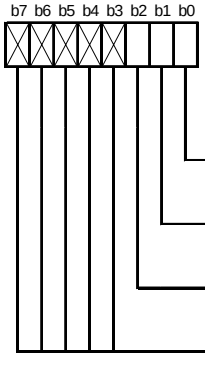


Figure 14.12 Block Diagram of Timer RB

Timer RB Control Register

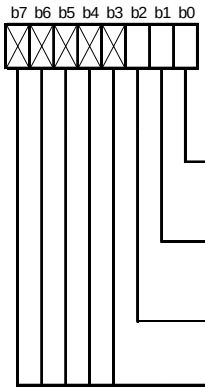


Symbol	Address	After Reset
TRBCR	0108h	00h

Bit Symbol	Bit Name	Function	RW
TSTART	Timer RB count start bit(1)	0 : Count stops 1 : Count starts	RW
TCSTF	Timer RB count status flag(1)	0 : Count stops 1 : During count(3)	RO
TSTOP	Timer RB count forcible stop bit(1, 2)	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	RW
— (b7-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Refer to **14.2.5 Notes on Timer RB**.
2. When the TSTOP bit is set to 1, registers TRBPRE, TRBSC, TRBPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable w aveform mode. In programmable one-shot generation mode or programmable w ait one-shot generation mode, indicates that a one-shot pulse trigger has been acknow ledged.

Timer RB One-Shot Control Register(2)



Symbol	Address	After Reset
TRBOCR	0109h	00h

Bit Symbol	Bit Name	Function	RW
TOSST	Timer RB one-shot start bit	When this bit is set to 1, one-shot trigger generated. When read, its content is 0.	RW
TOSSP	Timer RB one-shot stop bit	When this bit is set to 1, counting of one-shot pulses (including programmable w ait one-shot pulses) stops. When read, its content is 0.	RW
TOSSTF	Timer RB one-shot status flag(1)	0 : One-shot stopped 1 : One-shot operating (Including w ait period)	RO
— (b7-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. When 1 is set to the TSTOP bit in the TRBCR register, the TOSSTF bit is set to 0.
2. This register is enabled w hen bits TMOD1 to TMOD0 in the TRBMR register is set to 10b (programmable one-shot generation mode) or 11b (programmable w ait one-shot generation mode).

Figure 14.13 Registers TRBCR and TRBOCR

Timer RB I/O Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	Function varies depending on operating mode.	RW
TOCNT	Timer RB output switch bit		RW
INOSTG	One-shot trigger control bit		RW
INOSEG	One-shot trigger polarity select bit		RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Timer RB Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRBMR	010Bh	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Timer RB operating mode select bits(1)	b1 b0 0 0 : Timer mode 0 1 : Programmable waveform generation mode 1 0 : Programmable one-shot generation mode 1 1 : Programmable wait one-shot generation mode	RW
TMOD1			RW
— (b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TWRC	Timer RB write control bit(2)	0 : Write to reload register and counter 1 : Write to reload register only	RW
TCK0	Timer RB count source select bits(1)	b5 b4 0 0 : f1 0 1 : f8 1 0 : Timer RA underflow 1 1 : f2	RW
TCK1			RW
— (b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCKCUT	Timer RB count source cutoff bit(1)	0 : Provides count source 1 : Cuts off count source	RW

NOTES:
1. Change bits TMOD1 and TMOD0; TCK1 and TCK0; and TCKCUT when both the TSTART and TCSTF bits in the TRBCR register set to 0 (count stops).
2. The TWRC bit can be set to either 0 or 1 in timer mode. In programmable waveform generation mode, programmable one-shot generation mode, or programmable wait one-shot generation mode, the TWRC bit must be set to 1 (write to reload register only).

Figure 14.14 Registers TRBIOC and TRBMR

Timer RB Prescaler Register(1)

b7 b0

Symbol	Address	After Reset
TRBPRE	010Ch	FFh

Mode	Function	Setting Range	RW
Timer mode	Counts an internal count source or timer RA underflows	00h to FFh	RW
Programmable waveform generation mode	Counts an internal count source or timer RA underflows	00h to FFh	RW
Programmable one-shot generation mode	Counts an internal count source or timer RA underflows	00h to FFh	RW
Programmable wait one-shot generation mode	Counts an internal count source or timer RA underflows	00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRBCR register is set to 1, the TRBPRE register is set to FFh.

Timer RB Secondary Register(3, 4)

b7 b0

Symbol	Address	After Reset
TRBSC	010Dh	FFh

Mode	Function	Setting Range	RW
Timer mode	Disabled	00h to FFh	—
Programmable waveform generation mode	Counts timer RB prescaler underflows(1)	00h to FFh	WO(2)
Programmable one-shot generation mode	Disabled	00h to FFh	—
Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	WO(2)

NOTES:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. The count value can be read out by reading the TRBPR register even when the secondary period is being counted.
3. When the TSTOP bit in the TRBCR register is set to 1, the TRBSC register is set to FFh.
4. To write to the TRBSC register, perform the following steps.
   (1) Write the value to the TRBSC register.
   (2) Write the value to the TRBPR register. (If the value does not change, write the same value second time.)

Timer RB Primary Register(2)

b7 b0

Symbol	Address	After Reset
TRBPR	010Eh	FFh

Mode	Function	Setting Range	RW
Timer mode	Counts timer RB prescaler underflows	00h to FFh	RW
Programmable waveform generation mode	Counts timer RB prescaler underflows(1)	00h to FFh	RW
Programmable one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	RW
Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (wait period width is counted)	00h to FFh	RW

NOTES:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. When the TSTOP bit in the TRBCR register is set to 1, the TRBPR register is set to FFh.

Figure 14.15 Registers TRBPRE, TRBSC, and TRBPR

14.2.1 Timer Mode

In timer mode, a count source which is internally generated or timer RA underflows are counted (refer to **Table 14.7 Timer Mode Specifications**). Registers TRBOCR and TRBSC are not used in timer mode.
Figure 14.16 shows the TRBIOC Register in Timer Mode.

Table 14.7 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the reload register contents before the count continues (when timer RB underflows, the contents of timer RB primary reload register is reloaded).
Divide ratio	1/(n+1)(m+1) n: setting value in TRBPRE register, m: setting value in TRBPR register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	When timer RB underflows [timer RB interrupt].
TRBO pin function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written to while count operation is in progress: If the TWRC bit in the TRBMR register is set to 0, the value is written to both the reload register and the counter. If the TWRC bit is set to 1, the value is written to the reload register only. (Refer to **14.2.1.1 Timer Write Control during Count Operation**.)

Timer RB I/O Control Register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	0	0	0	0

Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	Set to 0 in timer mode.	RW
TOCNT	Timer RB output switch bit		RW
INOSTG	One-shot trigger control bit		RW
INOSEG	One-shot trigger polarity select bit		RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 14.16 TRBIOC Register in Timer Mode

14.2.1.1 Timer Write Control during Count Operation

Timer RB has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. In addition, if the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted if the prescaler value changes. Figure 14.17 shows an Operating Example of Timer RB when Counter Value is Rewritten during Count Operation.

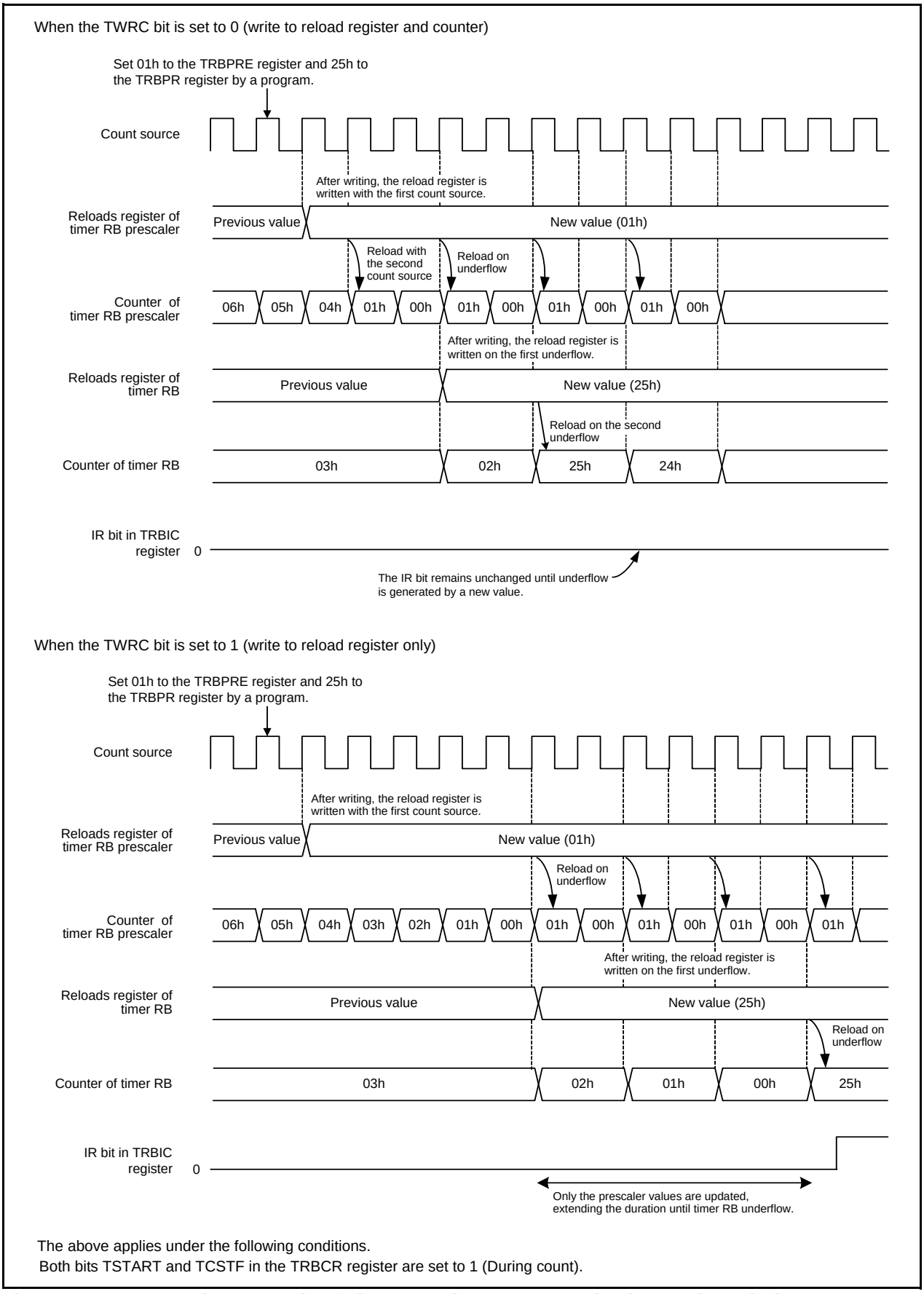


Figure 14.17 Operating Example of Timer RB when Counter Value is Rewritten during Count Operation

14.2.2 Programmable Waveform Generation Mode

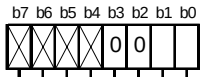
In programmable waveform generation mode, the signal output from the TRBO pin is inverted each time the counter underflows, while the values in registers TRBPR and TRBSC are counted alternately (refer to **Table 14.8 Programmable Waveform Generation Mode Specifications**). Counting starts by counting the setting value in the TRBPR register. The TRBOCR register is unused in this mode.
Figure 14.18 shows the TRBIOC Register in Programmable Waveform Generation Mode. Figure 14.19 shows an Operating Example of Timer RB in Programmable Waveform Generation Mode.

Table 14.8 Programmable Waveform Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.
Width and period of output waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: Count source frequency n: Value set in TRBPRE register m: Value set in TRBPR register p: Value set in TRBSC register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	In half a cycle of the count source, after timer RB underflows during the secondary period (at the same time as the TRBO output change) [timer RB interrupt]
TRBO pin function	Programmable output port or pulse output
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE(1).
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only.(2)
Select functions	• Output level select function The TOPL bit in the TRBIOC register selects the output level during primary and secondary periods. • TRBO pin output switch function Timer RB pulse output or P3_1 latch output is selected by the TOCNT bit in the TRBIOC register.(3)

NOTES:
1. Even when counting the secondary period, the TRBPR register may be read.
2. The set values are reflected in the waveform output beginning with the following primary period after writing to the TRBPR register.
3. The value written to the TOCNT bit is enabled by the following.
   - When count starts.
   - When a timer RB interrupt request is generated.
   The contents after the TOCNT bit is changed are reflected from the output of the following primary period.

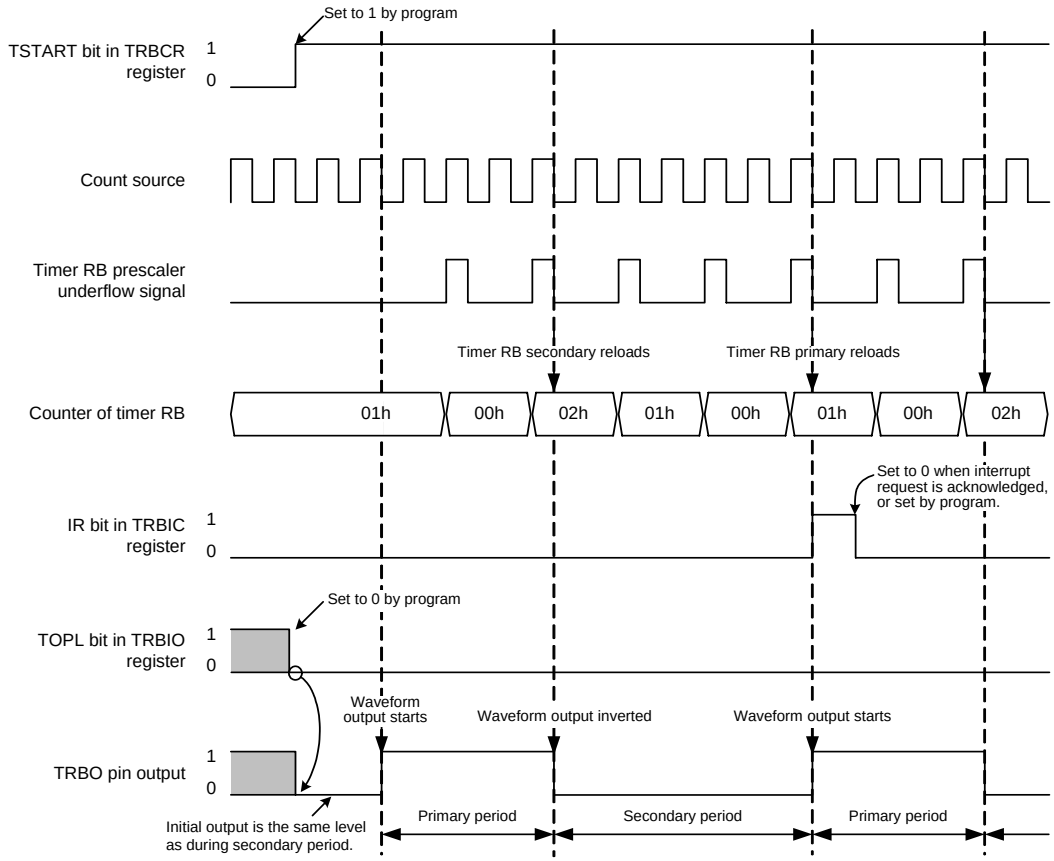
Timer RB I/O Control Register



Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	0 : Outputs “H” for primary period Outputs “L” for secondary period Outputs “L” when the timer is stopped 1 : Outputs “L” for primary period Outputs “H” for secondary period Outputs “H” when the timer is stopped	RW
TOCNT	Timer RB output switch bit	0 : Outputs timer RB waveform 1 : Outputs value in P3_1 port latch	RW
INOSTG	One-shot trigger control bit	Set to 0 in programmable waveform generation mode.	RW
INOSEG	One-shot trigger polarity select bit		RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 14.18 TRBIOC Register in Programmable Waveform Generation Mode



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 02h
TRBIOC register TOCNT = 0 (timer RB waveform is output from the TRBO pin)

Figure 14.19 Operating Example of Timer RB in Programmable Waveform Generation Mode

14.2.3 Programmable One-shot Generation Mode

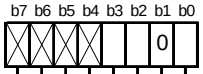
In programmable one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the INT0 pin) (refer to **Table 14.9 Programmable One-Shot Generation Mode Specifications**). When a trigger is generated, the timer starts operating from the point only once for a given period equal to the set value in the TRBPR register. The TRBSC register is not used in this mode.
Figure 14.20 shows the TRBIOC Register in Programmable One-Shot Generation Mode. Figure 14.21 shows an Operating Example of Programmable One-Shot Generation Mode.

Table 14.9 Programmable One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement the setting value in the TRBPR register • When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
One-shot pulse output time	(n+1)(m+1)/fi fi: Count source frequency, n: Setting value in TRBPRE register, m: Setting value in TRBPR register(2)
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated. • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts) • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during primary period. • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops). • When the TSTART bit in the TRBCR register is set to 0 (count stops). • When the TSTOP bit in the TRBCR register is set to 1 (count forcibly stops).
Interrupt request generation timing	In half a cycle of the count source, after the timer underflows (at the same time as the TRBO output ends) [timer RB interrupt]
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written during the count, values are written to the reload register only (the data is transferred to the counter at the following reload).(1)
Select functions	• Output level select function The TOPL bit in the TRBIOC register selects the output level of the one-shot pulse waveform. • One-shot trigger select function Refer to **14.2.3.1 One-Shot Trigger Selection**.

NOTES:
1. The set value is reflected at the following one-shot pulse after writing to the TRBPR register.
2. Do not set both the TRBPRE and TRBPR registers to 00h.

Timer RB I/O Control Register

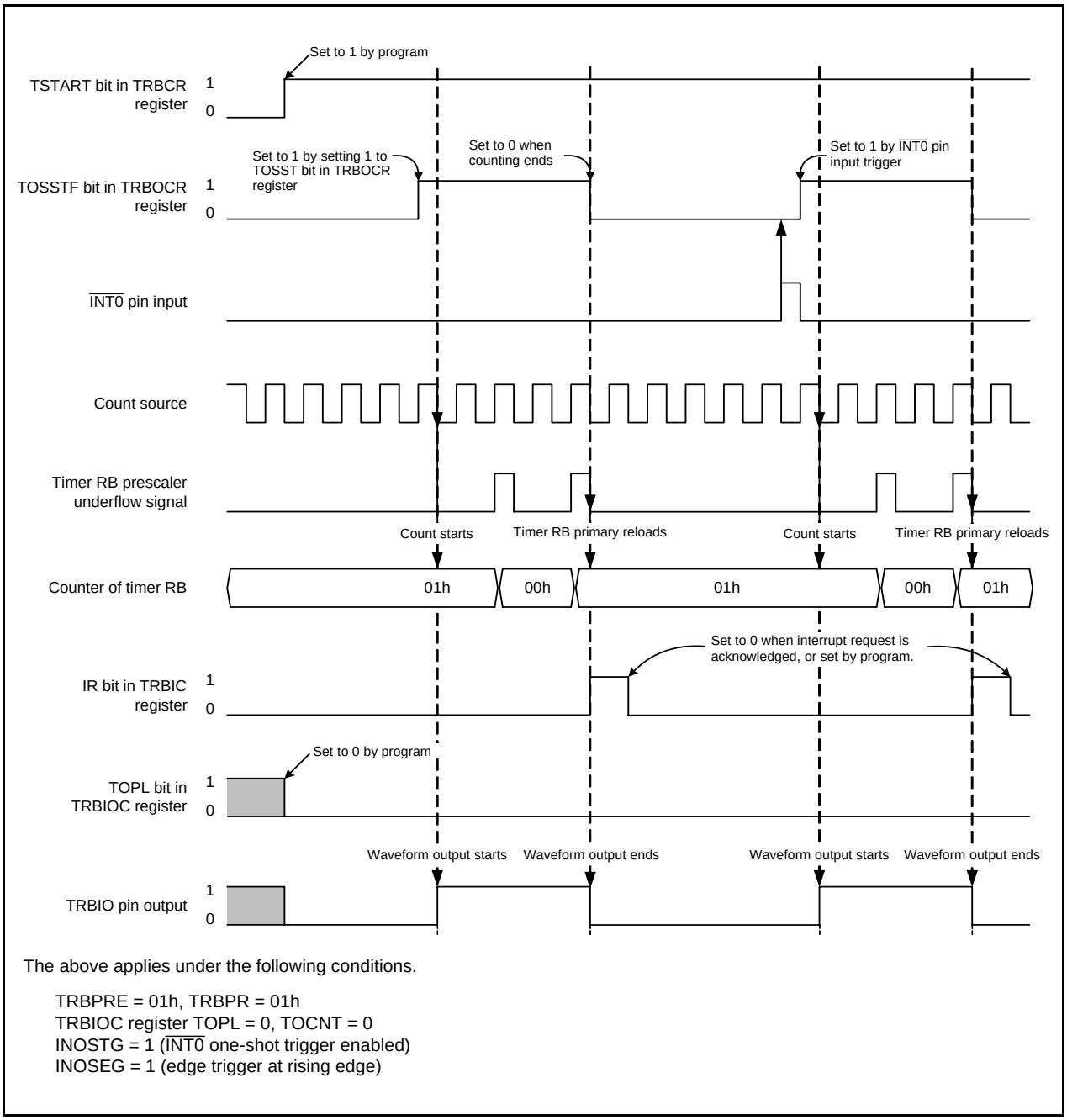


Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB Output Level Select Bit	0 : Outputs one-shot pulse “H” Outputs “L” when the timer is stopped 1 : Outputs one-shot pulse “L” Outputs “H” when the timer is stopped	RW
TOCNT	Timer RB Output Switch Bit	Set to 0 in programmable one-shot generation mode.	RW
INOSTG	One-Shot Trigger Control Bit(1)	0 : $\overline{INT0}$ pin one-shot trigger disabled 1 : $\overline{INT0}$ pin one-shot trigger enabled	RW
INOSEG	One-Shot Trigger Polarity Select Bit(1)	0 : Falling edge trigger 1 : Rising edge trigger	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, its content is 0.		—

NOTE:
1. Refer to **14.2.3.1 One-shot Trigger Selection**.

Figure 14.20 TRBIOC Register in Programmable One-Shot Generation Mode



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h
TRBIOC register TOPL = 0, TOCNT = 0
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at rising edge)

Figure 14.21 Operating Example of Programmable One-Shot Generation Mode

14.2.3.1 One-Shot Trigger Selection

In programmable one-shot generation mode and programmable wait one-shot generation mode, operation starts when a one-shot trigger is generated while the TCSTF bit in the TRBCR register is set to 1 (count starts).
A one-shot trigger can be generated by either of the following causes:

- 1 is written to the TOSST bit in the TRBOCR register by a program.
- Trigger input from the $\overline{\text{INT0}}$ pin.

When a one-shot trigger occurs, the TOSSTF bit in the TRBOCR register is set to 1 (one-shot operation in progress) after one or two cycles of the count source have elapsed. Then, in programmable one-shot generation mode, count operation begins and one-shot waveform output starts. (In programmable wait one-shot generation mode, count operation starts for the wait period.) If a one-shot trigger occurs while the TOSSTF bit is set to 1, no retriggering occurs.

To use trigger input from the $\overline{\text{INT0}}$ pin, input the trigger after making the following settings:

- Set the PD4_5 bit in the PD4 register to 0 (input port).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F1 and INT0F0 in the INTF register.
- Select both edges or one edge with the INT0PL bit in INTEN register. If one edge is selected, further select falling or rising edge with the INOSEG bit in TRBIOC register.
- Set the INT0EN bit in the INTEN register to 0 (enabled).
- After completing the above, set the INOSTG bit in the TRBIOC register to 1 ($\overline{\text{INT}}$ pin one-shot trigger enabled).

Note the following points with regard to generating interrupt requests by trigger input from the $\overline{\text{INT0}}$ pin.

- Processing to handle the interrupts is required. Refer to **12. Interrupts**, for details.
- If one edge is selected, use the POL bit in the INT0IC register to select falling or rising edge. (The INOSEG bit in the TRBIOC register does not affect $\overline{\text{INT0}}$ interrupts).
- If a one-shot trigger occurs while the TOSSTF bit is set to 1, timer RB operation is not affected, but the value of the IR bit in the INT0IC register changes.

14.2.4 Programmable Wait One-Shot Generation Mode

In programmable wait one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to **Table 14.10 Programmable Wait One-Shot Generation Mode Specifications**). When a trigger is generated from that point, the timer outputs a pulse only once for a given length of time equal to the setting value in the TRBSC register after waiting for a given length of time equal to the setting value in the TRBPR register.

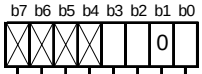
Figure 14.22 shows the TRBIOC Register in Programmable Wait One-Shot Generation Mode. Figure 14.23 shows an Operating Example of Programmable Wait One-Shot Generation Mode.

Table 14.10 Programmable Wait One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement the timer RB primary setting value. • When a count of the timer RB primary underflows, the timer reloads the contents of timer RB secondary before the count continues. • When a count of the timer RB secondary underflows, the timer reloads the contents of timer RB primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
Wait time	(n+1)(m+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, m Value set in the TRBPR register(2)
One-shot pulse output time	(n+1)(p+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, p: Value set in the TRBSC register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated. • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts). • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during secondary period. • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops). • When the TSTART bit in the TRBCR register is set to 0 (count starts). • When the TSTOP bit in the TRBCR register is set to 1 (count forcibly stops).
Interrupt request generation timing	In half a cycle of the count source after timer RB underflows during secondary period (complete at the same time as waveform output from the TRBO pin) [timer RB interrupt].
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count stops, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only.(1)
Select functions	• Output level select function The TOPL bit in the TRBIOC register selects the output level of the one-shot pulse waveform. • One-shot trigger select function Refer to **14.2.3.1 One-Shot Trigger Selection**.

NOTES:
1. The set value is reflected at the following one-shot pulse after writing to registers TRBSC and TRBPR.
2. Do not set both the TRBPRE and TRBPR registers to 00h.

Timer RB I/O Control Register

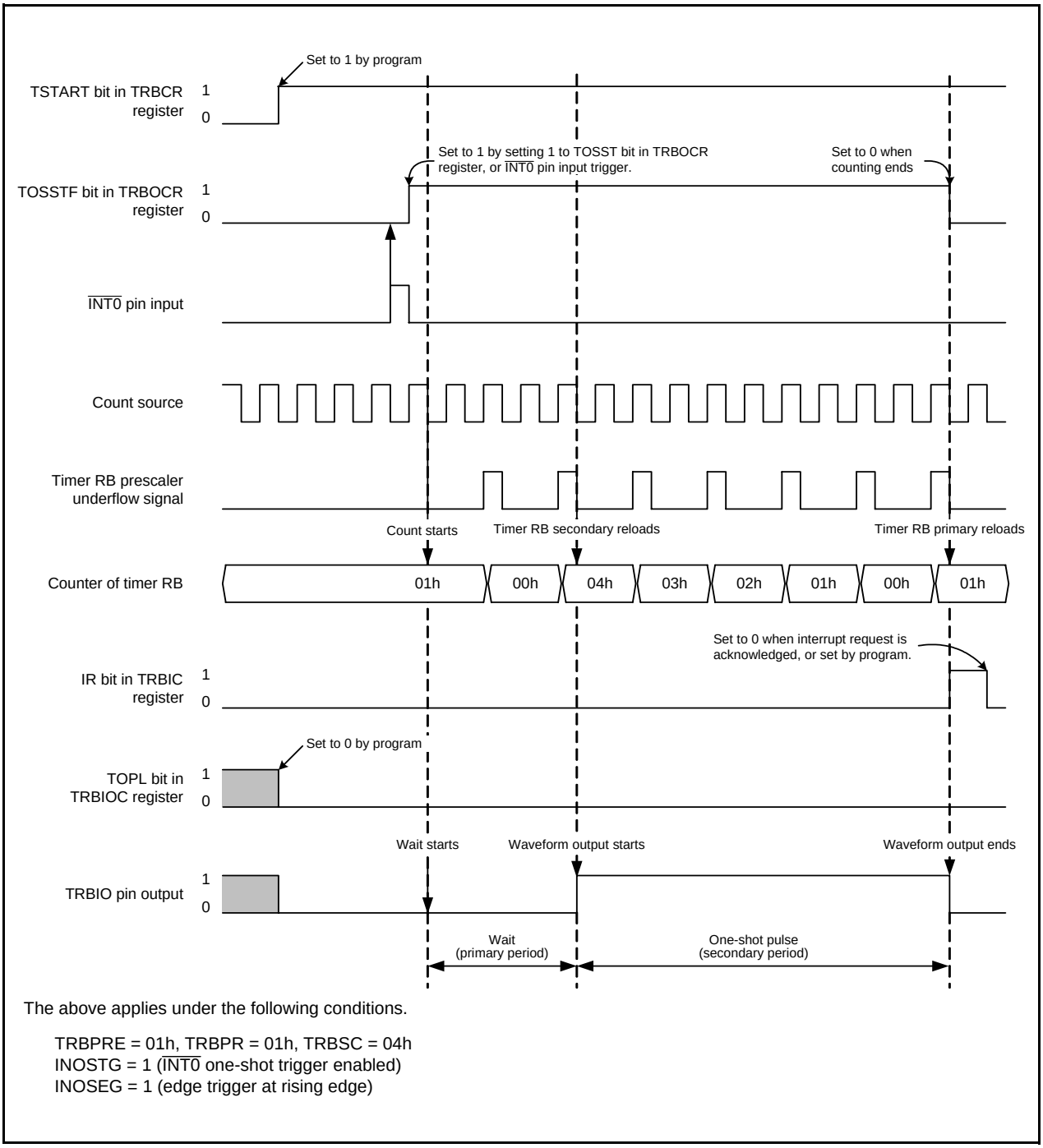


Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	0 : Outputs one-shot pulse “H”. Outputs “L” when the timer stops or during wait. 1 : Outputs one-shot pulse “L”. Outputs “H” when the timer stops or during wait.	RW
TOCNT	Timer RB output switch bit	Set to 0 in programmable wait one-shot generation mode.	RW
INOSTG	One-shot trigger control bit(1)	0 : $\overline{INT0}$ pin one-shot trigger disabled 1 : $\overline{INT0}$ pin one-shot trigger enabled	RW
INOSEG	One-shot trigger polarity select bit(1)	0 : Falling edge trigger 1 : Rising edge trigger	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Refer to **14.2.3.1 One-shot Trigger Selection**.

Figure 14.22 TRBIOC Register in Programmable Wait One-Shot Generation Mode



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 04h
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at rising edge)

Figure 14.23 Operating Example of Programmable Wait One-Shot Generation Mode

14.2.5 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (count stops) or setting the TOSSP bit in the TRBOCR register to 1 (one-shot stops), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB(1) other than the TCSTF bit.
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.

14.2.5.1 Timer mode

The following workaround should be performed in timer mode.
To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

14.2.5.2 Programmable waveform generation mode

The following three workarounds should be performed in programmable waveform generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) To change registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), synchronize the TRBO output cycle using a timer RB interrupt, etc. This operation should be preformed only once in the same output cycle. Also, make sure that writing to the TRBPR register does not occur during period A shown in Figures 14.24 and 14.25.

The following shows the detailed workaround examples.

- Workaround example (a):
  As shown in Figure 14.24, write to registers TRBSC and TRBPR in the timer RB interrupt routine. These write operations must be completed by the beginning of period A.

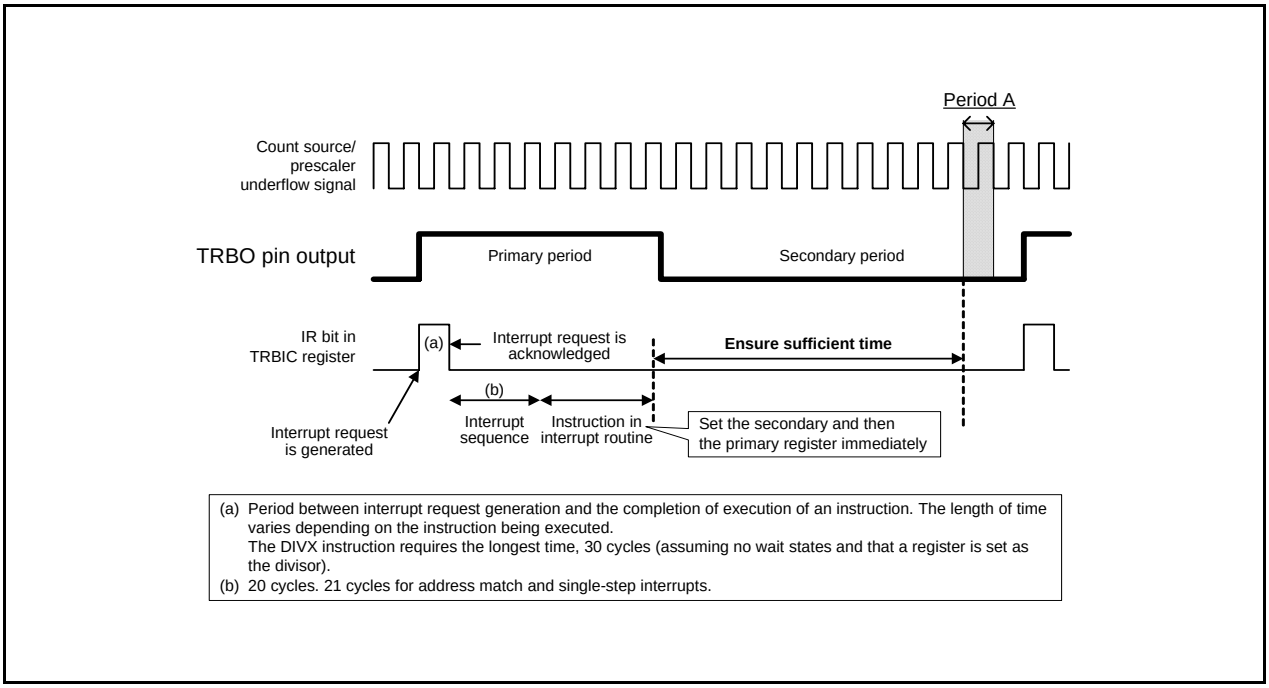


Figure 14.24 Workaround Example (a) When Timer RB interrupt is Used

• Workaround example (b):
As shown in Figure 14.25 detect the start of the primary period by the TRBO pin output level and write to registers TRBSC and TRBPR. These write operations must be completed by the beginning of period A.
If the port register's bit value is read after the port direction register's bit corresponding to the TRBO pin is set to 0 (input mode), the read value indicates the TRBO pin output value.

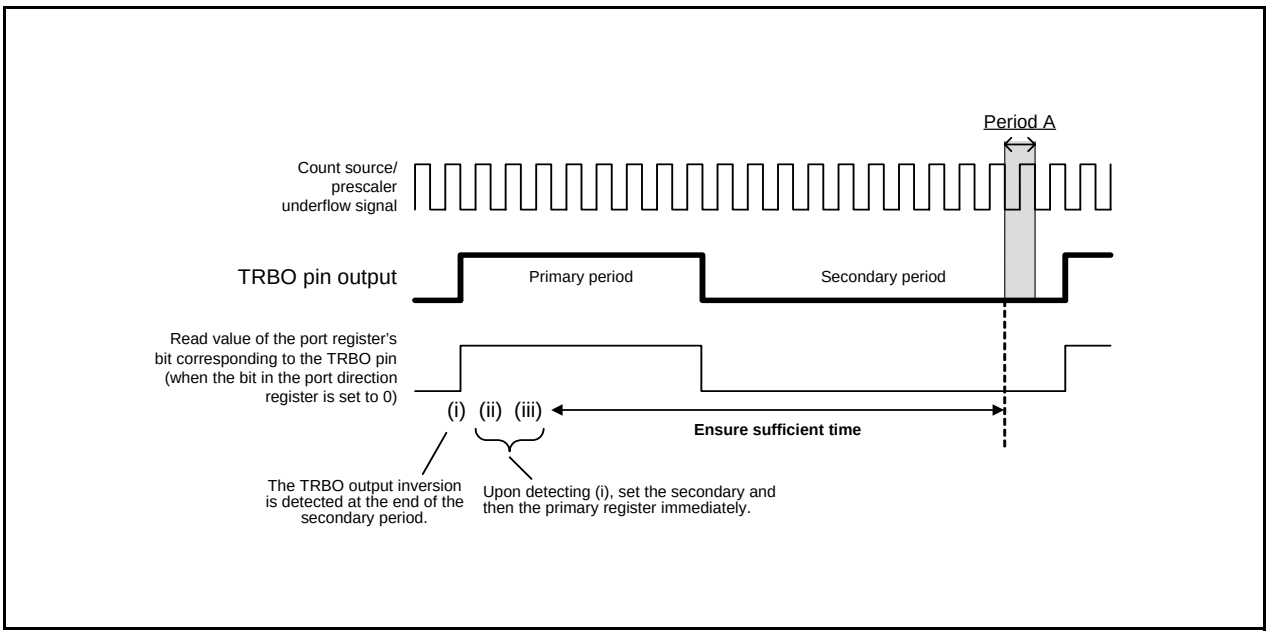


Figure 14.25 Workaround Example (b) When TRBO Pin Output Value is Read

(3) To stop the timer counting in the primary period, use the TSTOP bit in the TRBCR register. In this case, registers TRBPRE and TRBPR are initialized and their values are set to the values after reset.

14.2.5.3 Programmable one-shot generation mode

The following two workarounds should be performed in programmable one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

• When the TRBPRE register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.

• When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

14.2.5.4 Programmable wait one-shot generation mode

The following three workarounds should be performed in programmable wait one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

(3) Set registers TRBSC and TRBPR using the following procedure.

(a) To use "$\overline{\text{INT0}}$ pin one-shot trigger enabled" as the count start condition
Set the TRBSC register and then the TRBPR register. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before trigger input from the $\overline{\text{INT0}}$ pin.

(b) To use "writing 1 to TOSST bit" as the start condition
Set the TRBSC register, the TRBPR register, and then TOSST bit. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before writing to the TOSST bit.

14.3 Timer RD

Timer RD has 2 16-bit timers (channels 0 and 1). Each channel has 4 I/O pins.
The operation clock of timer RD is f1 or fOCO40M. Table 14.11 lists the Timer RD Operation Clocks.

Table 14.11 Timer RD Operation Clocks

Condition	Operation Clock of Timer RD
The count source is f1, f2, f4, f8, f32, or TRDCLK input (bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to a value from 000b to 101b).	f1
The count source is fOCO40M (bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to 110b).	fOCO40M

Figure 14.26 shows a Block Diagram of Timer RD. Timer RD has 5 modes:

- Timer mode
  - Input capture function — Transfer the counter value to a register with an external signal as the trigger
  - Output compare function — Detect register value matches with a counter (Pin output can be changed at detection)

The following 4 modes use the output compare function.

- PWM mode — Output pulse of any width continuously
- Reset synchronous PWM mode — Output three-phase waveforms (6) without sawtooth wave modulation and dead time
- Complementary PWM mode — Output three-phase waveforms (6) with triangular wave modulation and dead time
- PWM3 mode — Output PWM waveforms (2) with a fixed period

In the input capture function, output compare function, and PWM mode, channels 0 and 1 have the equivalent functions, and functions or modes can be selected individually for each pin. Also, a combination of these functions and modes can be used in 1 channel.
In reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, a waveform is output with a combination of counters and registers in channels 0 and 1.

Tables 14.12 to 14.20 list the Pin Functions of timer RD.

Table 14.12 Pin Functions TRDIOA0/TRDCLK(P2_0)

Register	TRDOER1	TRDFCR			TRDIORA0		Function
Bit	EA0	PWM3	STCLK	CMD1, CMD0	IOA3	IOA2_IOA0	
Setting value	0	0	0	00b	X	XXXb	PWM3 mode waveform output
	0	1	0	00b	1	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	0	00b	X	1XXb	Timer mode trigger input (input capture function)(1)
		1	1	XXb	X	000b	External clock input (TRDCLK)(1)
	Other than above						I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_0 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function) and external clock input (TRDCLK).

Table 14.13 Pin Functions TRDIOB0(P2_1)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORA0	Function
Bit	EB0	PWM3	CMD1, CMD0	PWMB0	IOB2_IOB0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	0	00b	X	XXXb	PWM3 mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_1 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.14 Pin Functions TRDIOC0(P2_2)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC0	Function
Bit	EC0	PWM3	CMD1, CMD0	PWMC0	IOC2_IOC0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_2 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.15 Pin Functions TRDIOD0(P2_3)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC0	Function
Bit	ED0	PWM3	CMD1, CMD0	PWMD0	IOD2_IOD0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_3 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.16 Pin Functions TRDIOA1(P2_4)

Register	TRDOER1	TRDFCR		TRDIORA1	Function
Bit	EA1	PWM3	CMD1, CMD0	IOA2_IOA0	
Setting value	0	X	1Xb	XXXb	Complementary PWM mode waveform output
	0	X	01b	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above				I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_4 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.17 Pin Functions TRDIOB1(P2_5)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORA1	Function
Bit	EB1	PWM3	CMD1, CMD0	PWMB1	IOB2_IOB0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_5 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.18 Pin Functions TRDIOC1(P2_6)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC1	Function
Bit	EC1	PWM3	CMD1, CMD0	PWMC1	IOC2_IOC0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_6 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.19 Pin Functions TRDIOD1(P2_7)

Register	TRDOER1	TRDFCR		TRDPMR	TRDIORC1	Function
Bit	ED1	PWM3	CMD1, CMD0	PWMD1	IOD2_IOD0	
Setting value	0	X	1Xb	X	XXXb	Complementary PWM mode waveform output
	0	X	01b	X	XXXb	Reset synchronous PWM mode waveform output
	0	1	00b	1	XXXb	PWM mode waveform output
	0	1	00b	0	001b, 01Xb	Timer mode waveform output (output compare function)
	X	1	00b	0	1XXb	Timer mode trigger input (input capture function)(1)
	Other than above					I/O port

X: can be 0 or 1, no change in outcome
NOTE:
1. Set the PD2_7 bit in the PD2 register to 0 (input mode) at timer mode trigger input (input capture function).

Table 14.20 Pin Functions $\overline{\text{INT0}}$(P4_5)

Register	TRDOER2	INTEN		PD4	Function
Bit	PTO	INT0PL	INT0EN	PD4_5	
Setting value	1	0	1	0	Pulse output forced cutoff signal input
	Other than above				I/O port or $\overline{\text{INT0}}$ interrupt input

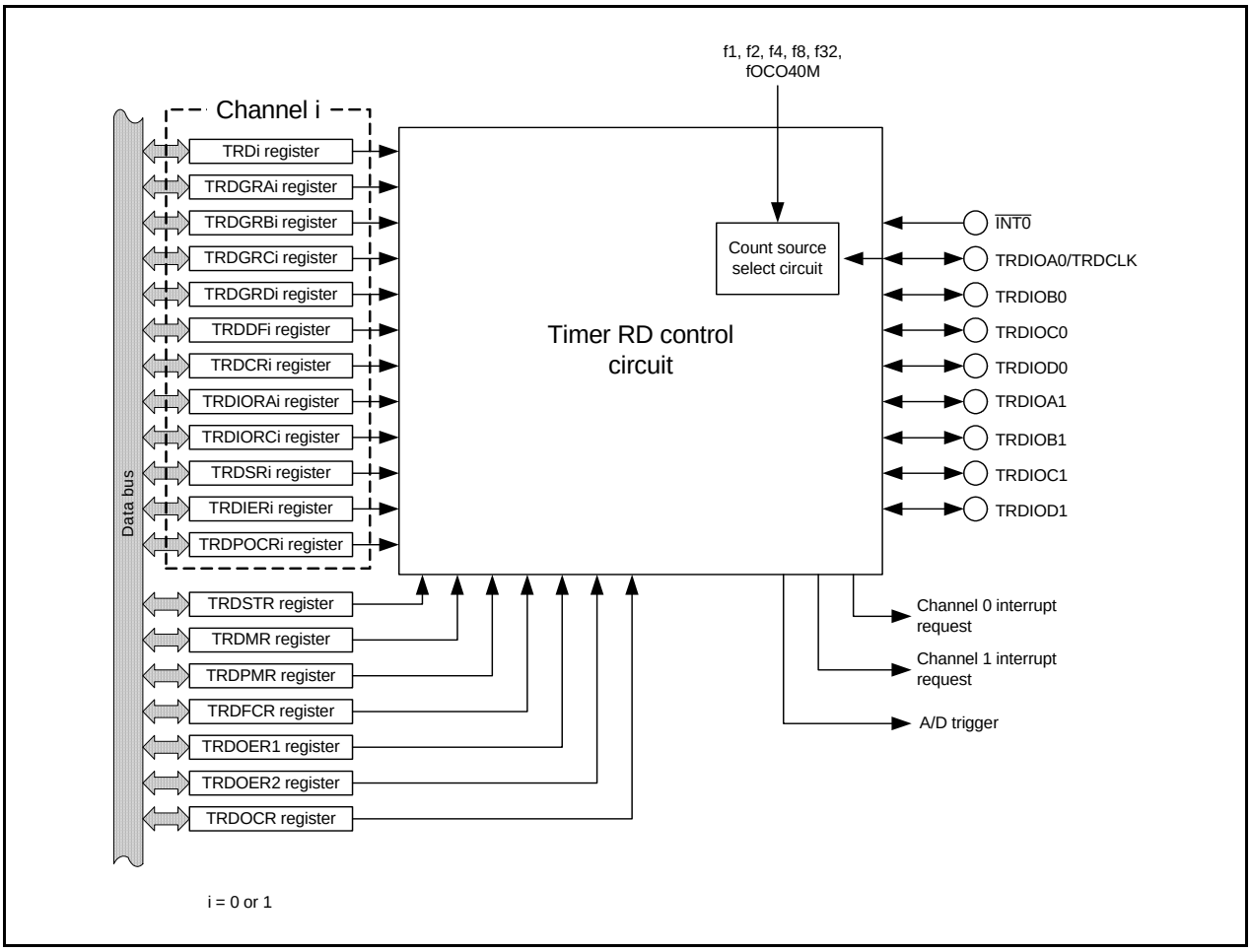


Figure 14.26 Block Diagram of Timer RD

14.3.1 Count Sources

The count source selection method is the same in all modes. However, in PWM3 mode, the external clock cannot be selected.

Table 14.21 Count Source Selection

Count Source	Selection
f1, f2, f4, f8, f32	The count source is selected by bits TCK2 to TCK0 in the TRDCRi register.
fOCO40M(1)	The FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator frequency). Bits TCK2 to TCK0 in the TRDCRi register is set to 110b (fOCO40M).
External signal input to TRDCLK pin	The STCLK bit in the TRDFCR register is set to 1 (external clock input enabled). Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (count source: external clock). The valid edge is selected by bits CKEG1 to CKEG0 in the TRDCRi register. The PD2_0 bit in the PD2 register is set to 0 (input mode).

i = 0 or 1

NOTE:

1. The count source fOCO40M can be used with VCC = 3.0 to 5.5 V.

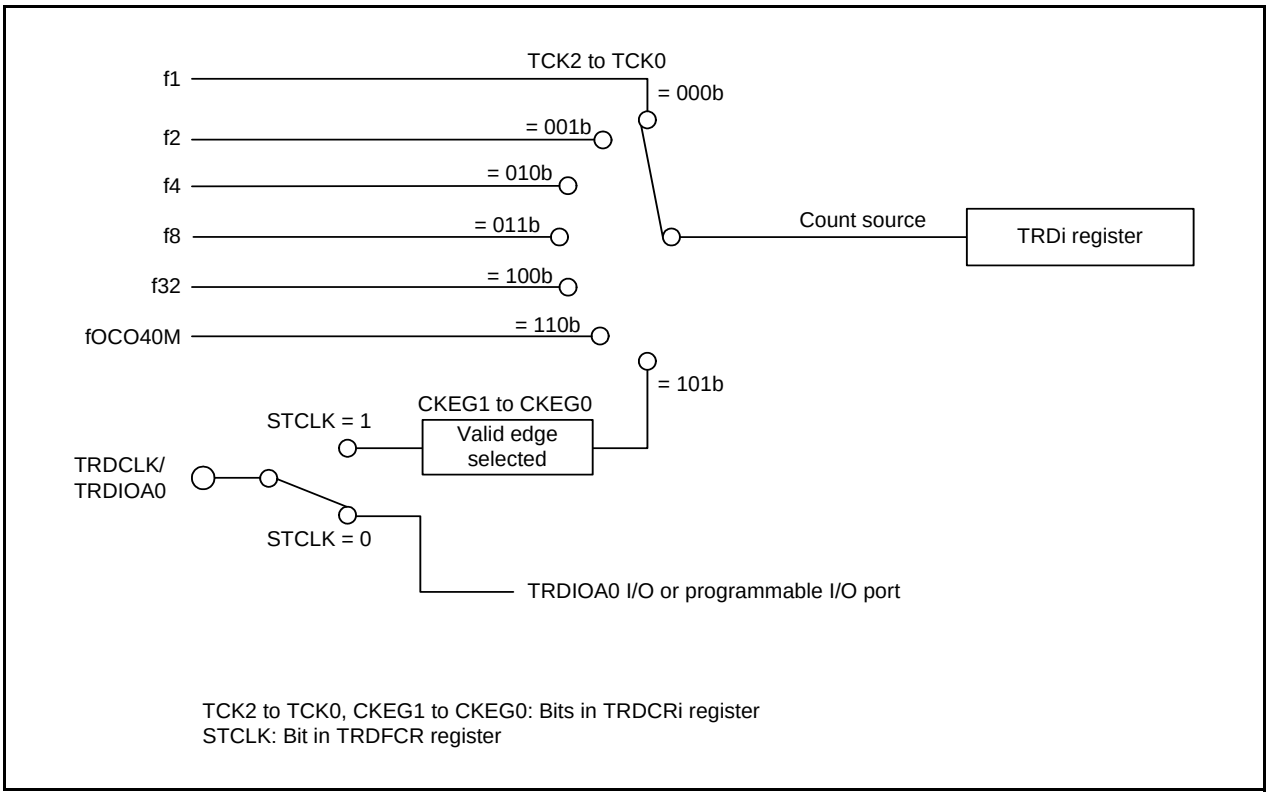


Figure 14.27 Block Diagram of Count Source

Set the pulse width of the external clock which inputs to the TRDCLK pin to 3 cycles or above of the operation clock of timer RD (refer to **Table 14.11 Timer RD Operation Clocks**).

When selecting fOCO40M for the count source, set the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on) before setting bits TCK2 to TCK0 in the TRDCRi register (i = 0 or 1) to 110b (fOCO40M).

14.3.2 Buffer Operation

The TRDGRCi (i = 0 or 1) register can be used as the buffer register of the TRDGRAi register, and the TRDGRDi register can be used as the buffer register of the TRDGRBi register by means of bits BFCi and BFDi in the TRDMR register.

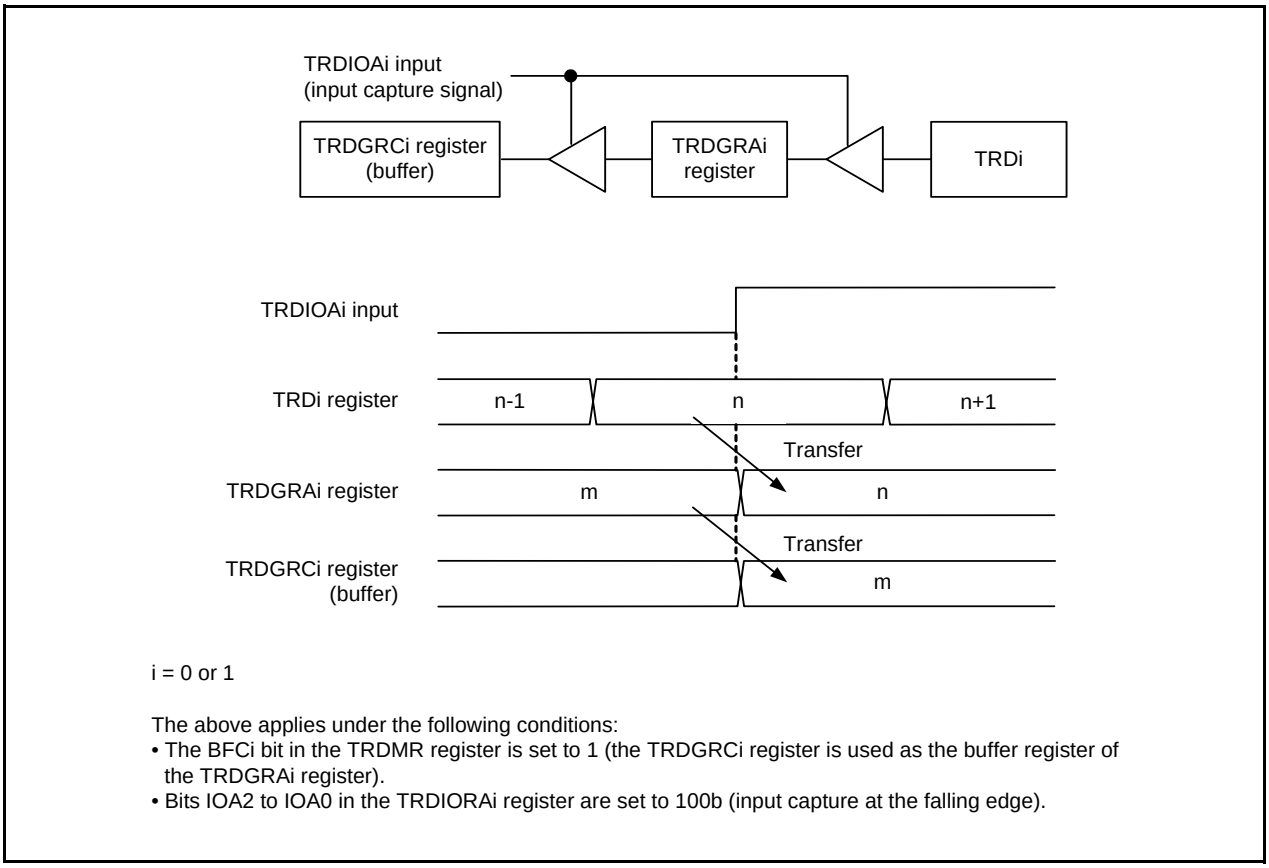
- TRDGRAi buffer register: TRDGRCi register
- TRDGRBi buffer register: TRDGRDi register

Buffer operation depends on the mode. Table 14.22 lists the Buffer Operation in Each Mode.
Figure 14.28 shows the Buffer Operation in Input Capture Function, and Figure 14.29 shows the Buffer Operation in Output Compare Function.

Table 14.22 Buffer Operation in Each Mode

Function and Mode	Transfer Timing	Transfer Register
Input capture function	Input capture signal input	Transfer content in TRDGRAi (TRDGRBi) register to buffer register
Output compare function PWM mode	Compare match with TRDi register and TRDGRAi (TRDGRBi) register	Transfer content in buffer register to TRDGRAi (TRDGRBi) register
Reset synchronous PWM mode	Compare match withTRD0 register and TRDGRA0 register	Transfer content in buffer register to TRDGRAi (TRDGRBi) register
Complementary PWM mode	• Compare match with TRD0 register and TRDGRA0 register • TRD1 register underflow	Transfer content in buffer register to registers TRDGRB0, TRDGRA1, and TRDGRB1
PWM3 mode	Compare match with TRD0 register and TRDGRA0 register	Transfer content in buffer register to registers TRDGRA0, TRDGRB0, TRDGRA1, and TRDGRB1

i = 0 or 1



i = 0 or 1

The above applies under the following conditions:
- The BFCi bit in the TRDMR register is set to 1 (the TRDGRCi register is used as the buffer register of the TRDGRAi register).
- Bits IOA2 to IOA0 in the TRDIORAi register are set to 100b (input capture at the falling edge).

Figure 14.28 Buffer Operation in Input Capture Function

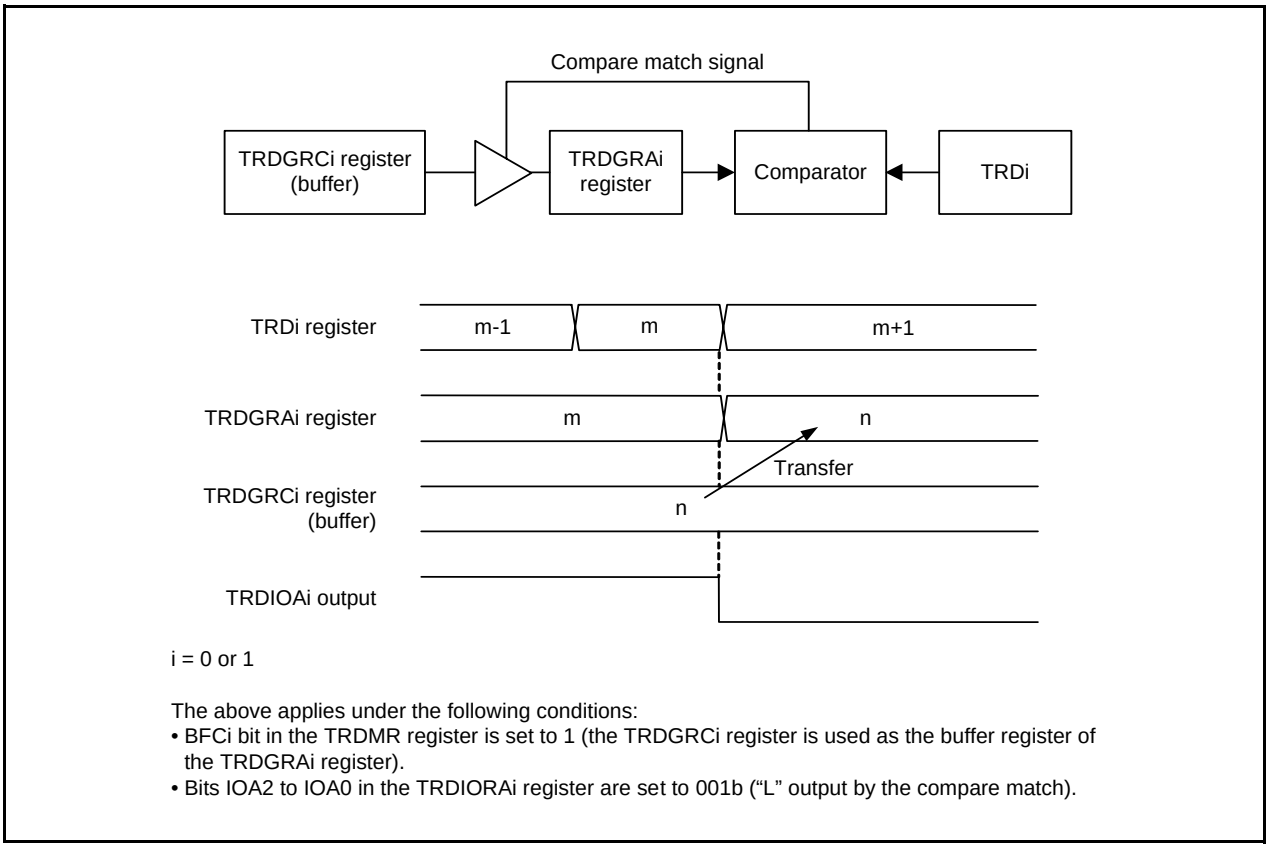


Figure 14.29 Buffer Operation in Output Compare Function

Perform the following for the timer mode (input capture and output compare functions).
When using the TRDGRCi (i = 0 or 1) register as the buffer register of the TRDGRAi register

- Set the IOC3 bit in the TRDIORCi register to 1 (general register or buffer register).
- Set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.

When using the TRDGRDi register as the buffer register of the TRDGRBi register

- Set the IOD3 bit in the TRDIORDi register to 1 (general register or buffer register).
- Set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

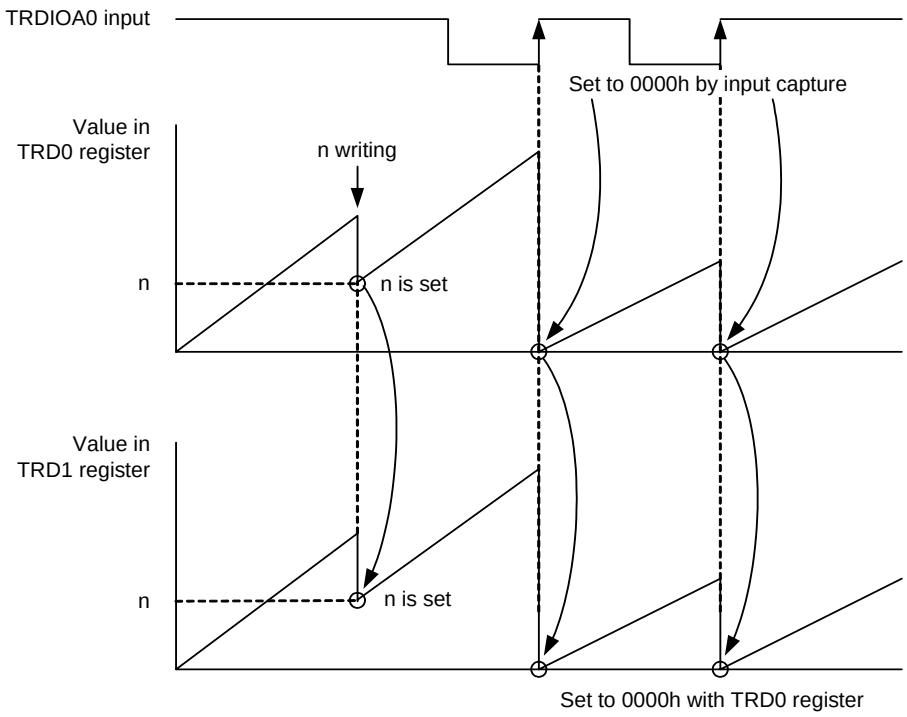
Bits IMFC and IMFD in the TRDSRi register are set to 1 at the input edge of the TRDIOCi pin when also using registers TRDGRCi and TRDGRDi as the buffer register in the input capture function.

When also using registers TRDGRCi and TRDGRDi as buffer registers for the output compare function, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, bits IMFC and IMFD in the TRDSRi register are set to 1 by a compare match with the TRDi register.

14.3.3 Synchronous Operation

The TRD1 register is synchronized with the TRD0 register.

- Synchronous preset
  When the SYNC bit in the TRDMR register is set to 1 (synchronous operation), the data is written to both the TRD0 and TRD1 registers after writing to the TRDi register.
- Synchronous clear
  When the SYNC bit in the TRDMR register is set to 1 and bits CCLR2 to CCLR0 in the TRDCRi register are set to 011b (synchronous clear), the TRD0 register is set to 0000h at the same time as the TRD1 register is set to 0000h.
  Also, when the SYNC bit in the TRDMR register is set to 1 and bits CCLR2 to CCLR0 in the TRDCRi register are set to 011b (synchronous clear), the TRD1 register is set to 0000h at the same time as the TRD0 register is set to 0000h.



The above applies under the following conditions:

- The SYNC bit in the TRDMR register is set to 1 (synchronous operation).
- Bits CCLR2 to CCLR0 in the TRDCR0 register are set to 001b (set the TRD0 register to 0000h in input capture).
  Bits CCLR2 to CCLR0 in the TRDCR1 register are set to 011b (set the TRD1 register to 0000h synchronizing with the TRD0 register).
- Bits IOA2 to IOA0 in the TRDIORA0 register are set to 100b.
- Bits CMD1 to CMD0 in the TRDFCR register are set to 00b.
  The PWM 3 bit in the TRDFCR register is set to 1.

} (Input capture at the rising edge of the TRDIOA0 input)

Figure 14.30 Synchronous Operation

14.3.4 Pulse Output Forced Cutoff

In the output compare function, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, the TRDIOji (i = 0 or 1, j = either A, B, C, or D) output pin can be forcibly set to a programmable I/O port by the $\overline{\text{INT0}}$ pin input, and pulse output can be cut off.
The pins used for output in these functions or modes can function as the output pin of timer RD when the applicable bit in the TRDOER1 register is set to 0 (enable timer RD output). When the PTO bit in the TRDOER2 register to 1 ($\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled), all bits in the TRDOER1 register are set to 1 (disable timer RD output, the TRDIOji output pin is used as the programmable I/O port) after "L" is applied to the $\overline{\text{INT0}}$ pin. The TRDIOji output pin is set to the programmable I/O port after "L" is applied to the $\overline{\text{INT0}}$ pin and waiting for 1 to 2 cycles of the timer RD operation clock (refer to **Table 14.11 Timer RD Operation Clocks**).

Set as below when using this function:

- Set the pin status (high impedance, "L" or "H" output) to pulse output forced cutoff by registers P2 and PD2.
- Set the INT0EN bit in the INTEN register to 1 (enable $\overline{\text{INT0}}$ input) and the INT0PL bit to 0 (one edge).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Set the $\overline{\text{INT0}}$ digital filter by bits INT0F1 to INT0F0 in the INTF register.
- Set the PTO bit in the TRDOER2 register to 1 (enable pulse output forced cutoff signal input $\overline{\text{INT0}}$).

According to the selection of the POL bit in the INT0IC register and change of the $\overline{\text{INT0}}$ pin input, the IR bit in the INT0IC register is set to 1 (interrupt request). Refer to **12. Interrupts** for details of interrupts.

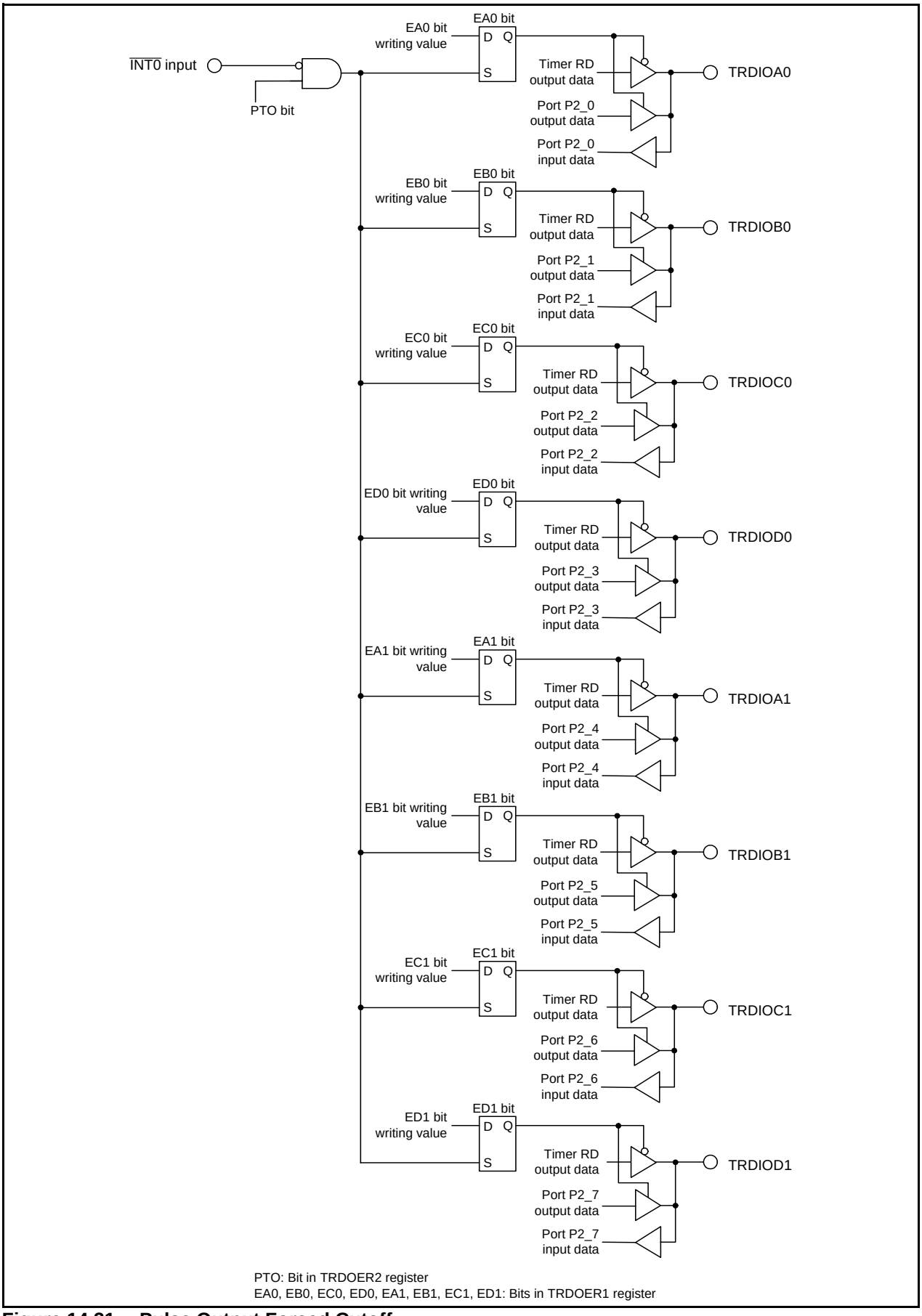


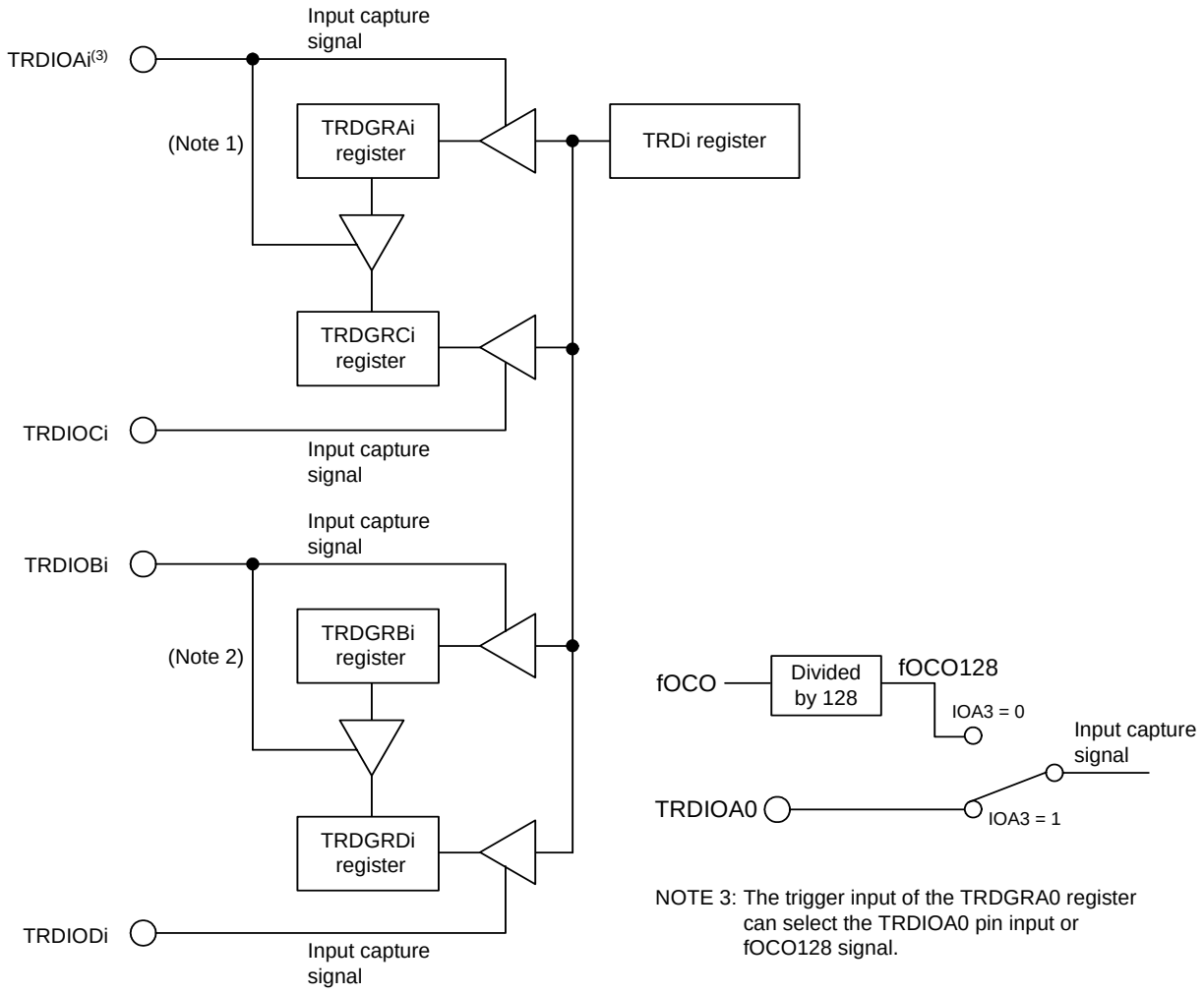
Figure 14.31 Pulse Output Forced Cutoff

14.3.5 Input Capture Function

The input capture function measures the external signal width and period. The content of the TRDi register (counter) is transferred to the TRDGRji register as a trigger of the TRDIOji (i = 0 or 1, j = either A, B, C, or D) pin external signal (input capture). Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the input capture function, or any other mode or function, can be selected for each individual pin.

The TRDGRA0 register can also select fOCO128 signal as input-capture trigger input.

Figure 14.32 shows a Block Diagram of Input Capture Function, Table 14.23 lists the Input Capture Function Specifications. Figures 14.33 to 14.43 show the Registers Associated with Input Capture Function, and Figure 14.44 shows an Operating Example of Input Capture Function.



i = 0 or 1

NOTE 1: When the BFCi bit in the TRDMR register is set to 1 (the TRDGRCi register is used as the buffer register of the TRDGRAi register).
NOTE 2: When the BFDi bit in the TRDMR register is set to 1 (the TRDGRDi register is used as the buffer register of the TRDGRBi register).

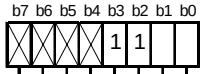
Figure 14.32 Block Diagram of Input Capture Function

Table 14.23 Input Capture Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program)
Count operations	Increment
Count period	When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000b (free-running operation). 1/fk × 65536 fk: Frequency of count source
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop condition	0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1.
Interrupt request generation timing	• Input capture (valid edge of TRDIOji input or fOCO128 signal edge) • TRDi register overflows
TRDIOA0 pin function	Programmable I/O port, input-capture input, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin functions	Programmable I/O port, or input-capture input (selectable by pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	• When the SYNC bit in the TRDMR register is set to 0 (channels 0 and 1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (channels 0 and 1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Select functions	• Input-capture input pin selected Either 1 pin or multiple pins among TRDIOAi, TRDIOBi, TRDIOCi, or TRDIODi. • Input-capture input valid edge selected The rising edge, falling edge, or both the rising and falling edges • The timing when the TRDi register is set to 0000h At overflow or input capture • Buffer operation (Refer to **14.3.2 Buffer Operation.**) • Synchronous operation (Refer to **14.3.3 Synchronous Operation.**) • Digital filter The TRDIOji input is sampled, and when the sampled input level match as 3 times, the level is determined. • Input-capture trigger selected fOCO128 can be selected for input-capture trigger input of the TRDGRA0 register.

i = 0 or 1, j = either A, B, C, or D

Timer RD Start Register(1)

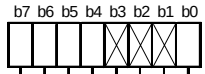


Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag	0 : Count stops 1 : Count starts	RW
TSTART1	TRD1 count start flag	0 : Count stops 1 : Count starts	RW
CSEL0	TRD0 count operation select bit	Set to 1 in the input capture function.	RW
CSEL1	TRD1 count operation select bit	Set to 1 in the input capture function.	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTE:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of **Notes on Timer RD.**

Timer RD Mode Register



Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	0 : Registers TRD0 and TRD1 operate independently 1 : Registers TRD0 and TRD1 operate synchronously	RW
— (b3-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function select bit	0 : General register 1 : Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function select bit	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function select bit	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function select bit	0 : General register 1 : Buffer register of TRDGRB1 register	RW

Figure 14.33 Registers TRDSTR and TRDMR in Input Capture Function

Timer RD PWM Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
X	0	0	0	X	0	0	0

Symbol	Address	After Reset
TRDPMR	0139h	10001000b

Bit Symbol	Bit Name	Function	RW
PWMB0	PWM mode of TRDIOB0 select bit	Set to 0 (timer mode) in the input capture function.	RW
PWMC0	PWM mode of TRDIOC0 select bit	Set to 0 (timer mode) in the input capture function.	RW
PWMD0	PWM mode of TRDIOD0 select bit	Set to 0 (timer mode) in the input capture function.	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PWMB1	PWM mode of TRDIOB1 select bit	Set to 0 (timer mode) in the input capture function.	RW
PWMC1	PWM mode of TRDIOC1 select bit	Set to 0 (timer mode) in the input capture function.	RW
PWMD1	PWM mode of TRDIOD1 select bit	Set to 0 (timer mode) in the input capture function.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.34 TRDPMR Register in Input Capture Function

Timer RD Function Control Register

b7	b6	b5	b4	b3	b2	b1	b0
1						0	0

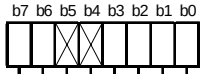
Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode select bits(1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in the input capture function.	RW
CMD1			RW
OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the input capture function.	RW
OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the input capture function.	RW
ADTRG	A/D trigger enable bit (in complementary PWM mode)	This bit is disabled in the input capture function.	RW
ADEG	A/D trigger edge select bit (in complementary PWM mode)	This bit is disabled in the input capture function.	RW
STCLK	External clock input select bit	0 : External clock input disabled 1 : External clock input enabled	RW
PWM3	PWM3 mode select bit(2)	Set this bit to 1 (other than PWM3 mode) in the input capture function.	RW

NOTES:
1. Set bits CMD1 to CMD0 w hen both the TSTART0 and TSTART1 bits are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.35 TRDFCR Register in Input Capture Function

Timer RD Digital Filter Function Select Register i (i = 0 or 1)



Symbol	Address	After Reset
TRDDF0	013Eh	00h
TRDDF1	013Fh	00h

Bit Symbol	Bit Name	Function	RW
DFA	TRDIOA pin digital filter function select bit	0 : Function is not used 1 : Function is used	RW
DFB	TRDIOB pin digital filter function select bit	0 : Function is not used 1 : Function is used	RW
DFC	TRDIOC pin digital filter function select bit	0 : Function is not used 1 : Function is used	RW
DFD	TRDIOD pin digital filter function select bit	0 : Function is not used 1 : Function is used	RW
— (b5-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
DFCK0	Clock select bits for digital filter function	b7 b6 0 0 : f32 0 1 : f8 1 0 : f1 1 1 : Count source (clock selected by bits TCK2 to TCK0 in the TRDCRi register)	RW
DFCK1			RW

Figure 14.36 Registers TRDDF0 to TRDDF1 in Input Capture Function

Timer RD Control Register i (i = 0 or 1)

b7 b6 b5 b4 b3 b2 b1 b0

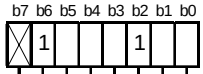
Symbol	Address	After Reset
TRDCR0	0140h	00h
TRDCR1	0150h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source select bits	b2 b1 b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : TRDCLK input(1) 1 1 0 : fOCO40M 1 1 1 : Do not set.	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge select bits(2)	b4 b3 0 0 : Count at the rising edge 0 1 : Count at the falling edge 1 0 : Count at both edges 1 1 : Do not set.	RW
CKEG1			RW
CCLR0	TRDi counter clear select bits	b7 b6 b5 0 0 0 : Disable clear (free-running operation) 0 0 1 : Clear by input capture in the TRDGRAi register 0 1 0 : Clear by input capture in the TRDGRBi register 0 1 1 : Synchronous clear (clear simultaneously with other channel counter)(3) 1 0 0 : Do not set. 1 0 1 : Clear by input capture in the TRDGRCi register 1 1 0 : Clear by input capture in the TRDGRDi register 1 1 1 : Do not set.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This setting is enabled when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. Bits CKEG1 to CKEG0 are enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
3. This setting is enabled when the SYNC bit in the TRDMR register is set to 1 (registers TRD0 and TRD1 operate synchronously).

Figure 14.37 Registers TRDCR0 to TRDCR1 in Input Capture Function

Timer RD I/O Control Register Ai (i = 0 or 1)



Symbol	Address	After Reset
TRDIORA0	0141h	10001000b
TRDIORA1	0151h	10001000b

Bit Symbol	Bit Name	Function	RW
IOA0	TRDGRA control bits	b1 b0 0 0 : Input capture to the TRDGRAi register at the rising edge 0 1 : Input capture to the TRDGRAi register at the falling edge 1 0 : Input capture to the TRDGRAi register at both edges 1 1 : Do not set.	RW
IOA1			RW
IOA2	TRDGRA mode select bit(1)	Set to 1 (input capture) in the input capture function.	RW
IOA3	Input capture input switch bit(3, 4)	0 : fOCO128 Signal 1 : TRDIOA0 pin input	RW
IOB0	TRDGRB control bits	b5 b4 0 0 : Input capture to the TRDGRBi register at the rising edge 0 1 : Input capture to the TRDGRBi register at the falling edge 1 0 : Input capture to the TRDGRBi register at both edges 1 1 : Do not set.	RW
IOB1			RW
IOB2	TRDGRB mode select bit(2)	Set to 1 (input capture) in the input capture function.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. To select 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (the TRDGRDi register is used as a buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.
3. The IOA3 bit is enabled in the TRDIORA0 register only. Set to the IOA3 bit in TRDIORA1 to 1.
4. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

Figure 14.38 Registers TRDIORA0 to TRDIORA1 in Input Capture Function

Timer RD I/O Control Register Ci (i = 0 or 1)

b7	b6	b5	b4	b3	b2	b1	b0
1	1			1	1		

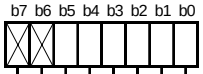
Symbol	Address	After Reset
TRDIORC0	0142h	10001000b
TRDIORC1	0152h	10001000b

Bit Symbol	Bit Name	Function	RW
IOC0	TRDGRC control bits	b1 b0 0 0 : Input capture to the TRDGRCi register at the rising edge 0 1 : Input capture to the TRDGRCi register at the falling edge 1 0 : Input capture to the TRDGRCi register at both edges 1 1 : Do not set.	RW
IOC1			RW
IOC2	TRDGRC mode select bit(1)	Set to 1 (input capture) in the input capture function.	RW
IOC3	TRDGRC register function select bit	Set to 1 (general register or buffer register) in the input capture function.	RW
IOD0	TRDGRD control bits	b5 b4 0 0 : Input capture to the TRDGRDi register at the rising edge 0 1 : Input capture to the TRDGRDi register at the falling edge 1 0 : Input capture to the TRDGRDi register at both edges 1 1 : Do not set.	RW
IOD1			RW
IOD2	TRDGRD mode select bit(2)	Set to 1 (input capture) in the input capture function.	RW
IOD3	TRDGRD register function select bit	Set to 1 (general register or buffer register) in the input capture function.	RW

NOTES:
1. To select 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (the TRDGRDi register is used as a buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

Figure 14.39 Registers TRDIORC0 to TRDIORC1 in Input Capture Function

Timer RD Status Register i (i = 0 or 1)



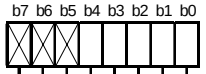
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read(2) [Source for setting this bit to 1] TRDSR0 register: fOCO128 signal edge when the IOA3 bit in the TRDIORA0 register is set to 0 (fOCO128 signal) TRDIOA0 pin input edge when the IOA3 bit in the TRDIORA0 register is set to 1 (TRDIOA0 input)(3) TRDSR1 register: Input edge of TRDIOA1 pin(3)	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read(2) [Source for setting this bit to 1] Input edge of TRDIOBi pin(3)	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read(2) [Source for setting this bit to 1] Input edge of TRDIOCi pin(4)	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read(2) [Source for setting this bit to 1] Input edge of TRDIODi pin(4)	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read(2) [Source for setting this bit to 1] When the TRDi register overflows	RW
UDF	Underflow flag(1)	This bit is disabled in the input capture function.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.
3. Edge selected by bits IOj1 to IOj0 (j = A or B) in the TRDIORAi register.
4. Edge selected by bits IOk1 to IOk0 (k = C or D) in the TRDIORCi register
   Including when the BFki bit in the TRDMR register is set to 1 (TRDGRki is used as the buffer register).

Figure 14.40 Registers TRDSR0 to TRDSR1 in Input Capture Function

Timer RD Interrupt Enable Register i (i = 0 or 1)

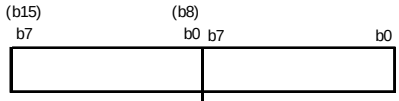


Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable interrupt (IMIA) by the IMFA bit 1 : Enable interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable interrupt (IMIB) by the IMFB bit 1 : Enable interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable interrupt (IMIC) by the IMFC bit 1 : Enable interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable interrupt (IMID) by the IMFD bit 1 : Enable interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0 : Disable interrupt (OVI) by the OVF bit 1 : Enable interrupt (OVI) by the OVF bit	RW
— (b7-b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.41 Registers TRDIER0 to TRDIER1 in Input Capture Function

Timer RD Counter i (i = 0 or 1)(1)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h
TRD1	0157h-0156h	0000h

Function	Setting Range	RW
Count the count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

Figure 14.42 Registers TRD0 to TRD1 in Input Capture Function

Timer RD General Registers Ai, Bi, Ci, and Di (i = 0 or 1)(1)

(b15) (b8) (b7) (b0)

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.24 TRDGRji Register Functions in Input Capture Function**.	RW

NOTE:
1. Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

Figure 14.43 Registers TRDGRAi, TRDGRBi, TRDGRCi, and TRDGRDi in Input Capture Function

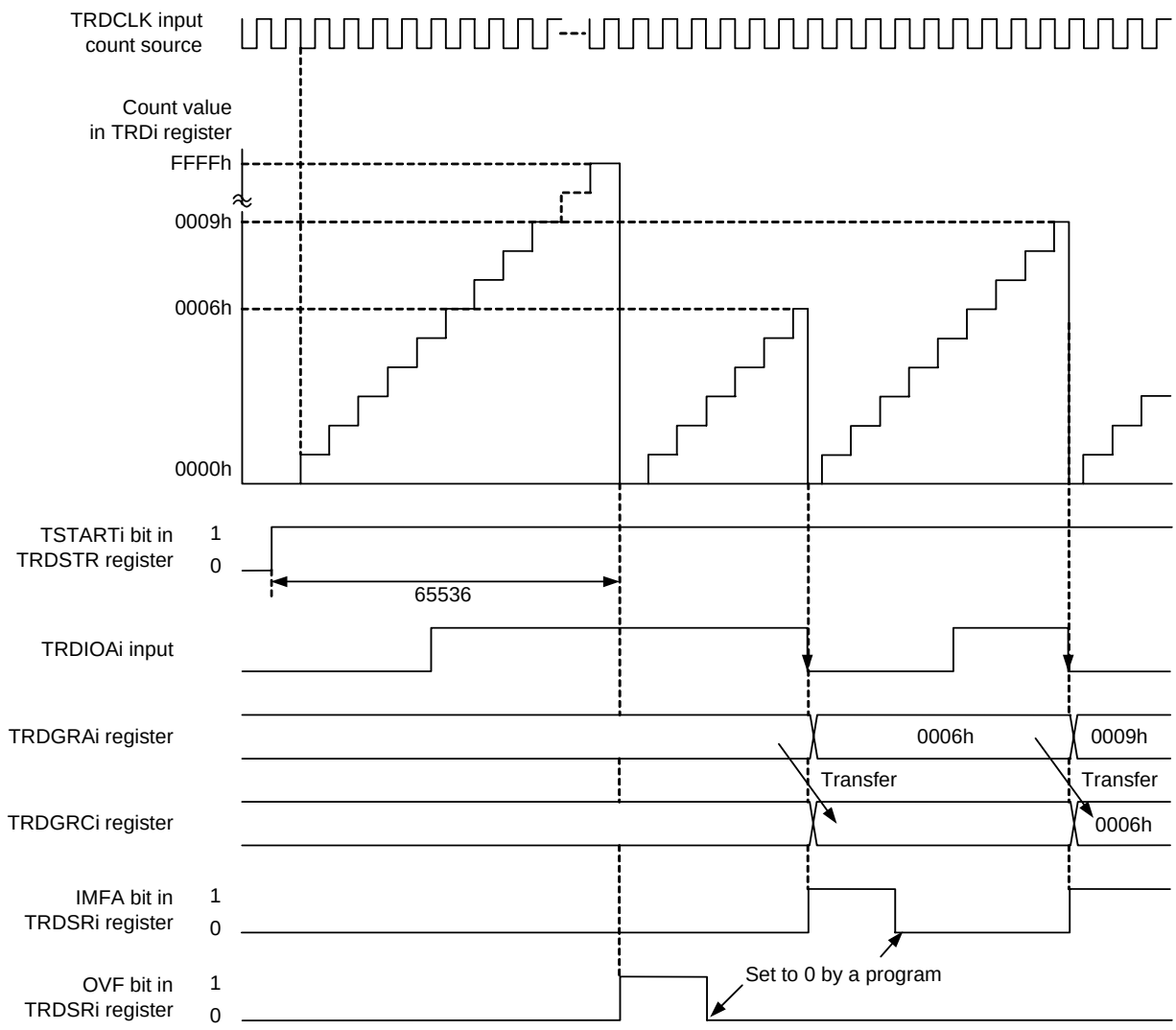
The following registers are disabled in the input capture function: TRDOER1, TRDOER2, TRDOCR, TRDPOCR0, and TRDPOCR1.

Table 14.24 TRDGRji Register Functions in Input Capture Function

Register	Setting	Register Function	Input-Capture Input Pin
TRDGRAi	–	General register The value in the TRDi register can be read at input capture.	TRDIOAi
TRDGRBi			TRDIOBi
TRDGRCi	BFCi = 0	General register The value in the TRDi register can be read at input capture.	TRDIOCi
TRDGRDi	BFDi = 0		TRDIODi
TRDGRCi	BFCi = 1	Buffer register The value in the TRDi register can be read at input capture. (Refer to **14.3.2 Buffer Operation**.)	TRDIOAi
TRDGRDi	BFDi = 1		TRDIOBi

i = 0 or 1, j = either A, B, C, or D
BFCi, BFDi: Bits in TRDMR register

Set the pulse width of the input capture signal applied to the TRDIOji pin to 3 cycles or more of the timer RD operation clock (refer to **Table 14.11 Timer RD Operation Clocks**) for no digital filter (the DFj bit in the TRDDFi register set to 0).



i = 0 or 1

The above applies under the following conditions:
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b. (the TRDi register set to 0000h by TRDGRAi register input capture).
Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (TRDCLK input for the count source).
Bits CKEG1 to CKEG0 in the TRDCRi register are set to 01b (count at the falling edge for the count source).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 101b (input capture at the falling edge of the TRDIOAi input).
The BFCi bit in the TRDMR register is set to 1 (the TRDGRCi register is used as the buffer register of the TRDGRAi register).

Figure 14.44 Operating Example of Input Capture Function

14.3.5.1 Digital Filter

The TRDIOji input is sampled, and when the sampled input level matches 3 times, its level is determined. Select the digital filter function and sampling clock by the TRDDFi register.

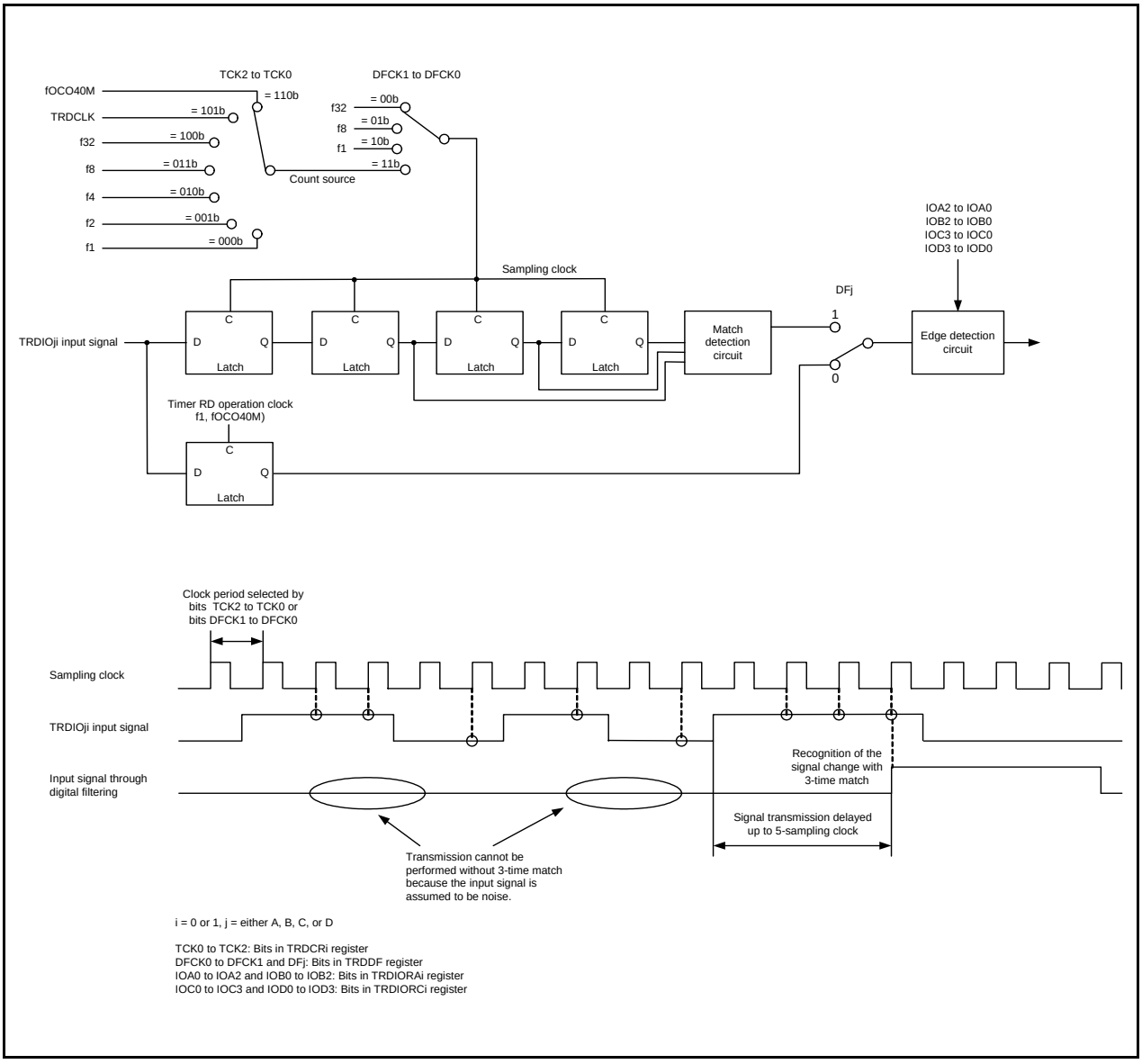


Figure 14.45 Block Diagram of Digital Filter

14.3.6 Output Compare Function

This function detects matches (compare match) between the content of the TRDGRji (j = either A, B, C, or D) register and the content of the TRDi (i = 0 or 1) register. When the content matches, a user-set level is output from the TRDIOji pin. Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the output compare function, or any other mode or function, can be selected for each individual pin. Figure 14.46 shows a Block Diagram of Output Compare Function, Table 14.25 lists the Output Compare Function Specifications. Figures 14.47 to 14.58 list the Registers Associated with Output Compare Function, and Figure 14.59 shows an Operating Example of Output Compare Function.

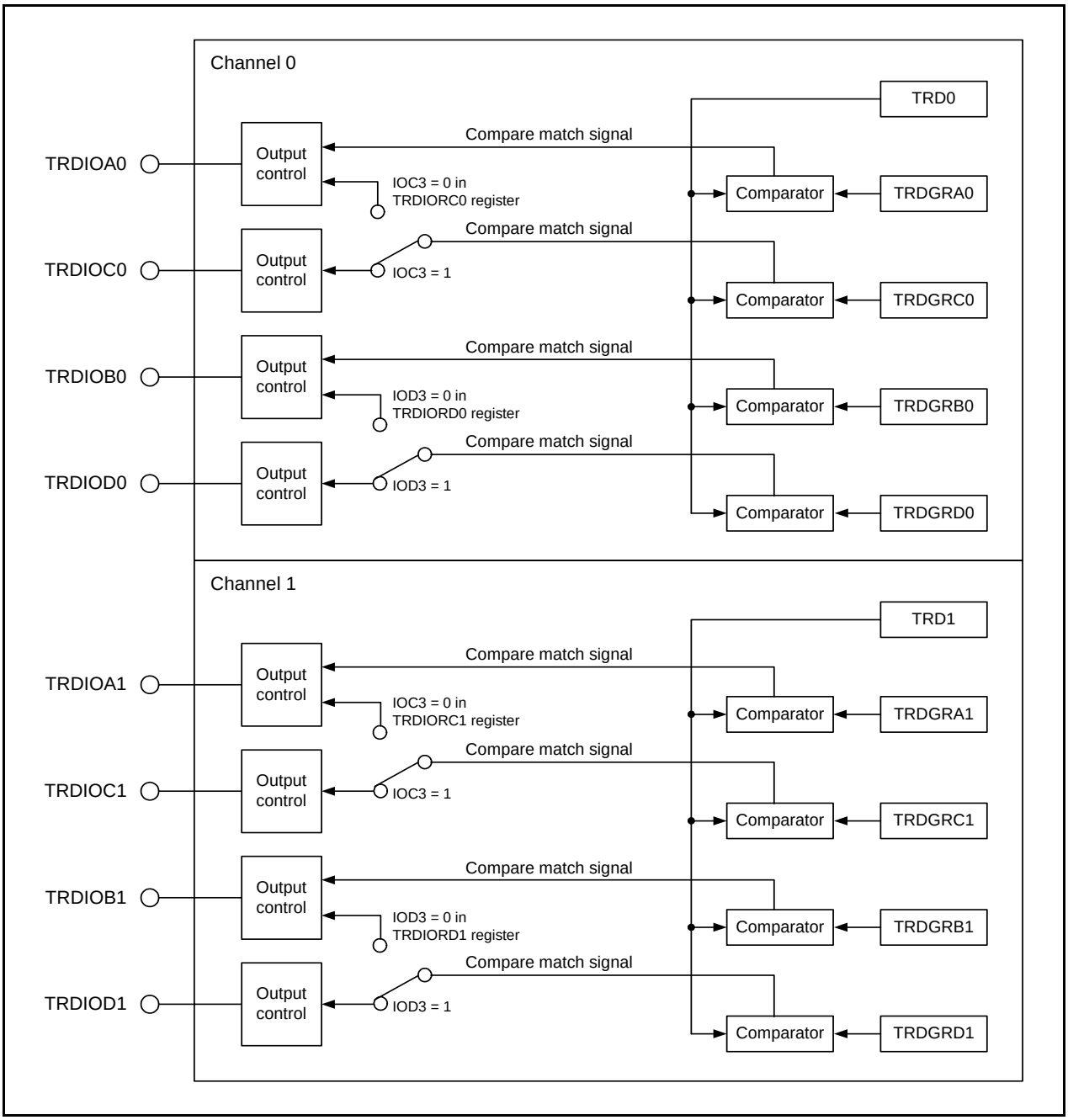


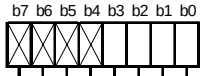
Figure 14.46 Block Diagram of Output Compare Function

Table 14.25 Output Compare Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program)
Count operations	Increment
Count period	• When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000b (free-running operation) 1/fk × 65536 fk: Frequency of count source • Bits CCLR1 to CCLR0 in the TRDCRi register are set to 01b or 10b (set the TRDi register to 0000h at the compare match in the TRDGRji register). Frequency of count source x (n+1) n: Setting value in the TRDGRji register
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The output compare output pin holds output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRAi register. The output compare output pin holds level after output change by the compare match.
Interrupt request generation timing	• Compare match (content of the TRDi register matches content of the TRDGRji register.) • TRDi register overflows
TRDIOA0 pin function	Programmable I/O port, output-compare output, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin functions	Programmable I/O port or output-compare output (Selectable by pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	• When the SYNC bit in the TRDMR register is set to 0 (channels 0 and 1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (channels 0 and 1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Select functions	• Output-compare output pin selected Either 1 pin or multiple pins among TRDIOAi, TRDIOBi, TRDIOCi, or TRDIODi. • Output level at the compare match selected “L” output, “H” output, or output level inversed • Initial output level selected Set the level at period from the count start to the compare match. • Timing to set the TRDi register to 0000h Overflow or compare match in the TRDGRAi register • Buffer operation (Refer to **14.3.2 Buffer Operation.**) • Synchronous operation (Refer to **14.3.3 Synchronous Operation.**) • Output pin in registers TRDGRCi and TRDGRDi changed The TRDGRCi register can be used as output control of the TRDIOAi pin and the TRDGRDi register can be used as output control of the TRDIOBi pin. • Pulse output forced cutoff signal input (Refer to **14.3.4 Pulse Output Forced Cutoff.**) • Timer RD can be used as the internal timer without output.

i = 0 or 1, j = either A, B, C, or D

Timer RD Start Register(1)

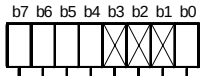


Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag(4)	0 : Count stops(2) 1 : Count starts	RW
TSTART1	TRD1 count start flag(5)	0 : Count stops(3) 1 : Count starts	RW
CSEL0	TRD0 count operation select bit	0 : Count stops at the compare match with the TRDGRA0 register 1 : Count continues at the compare match with the TRDGRA0 register	RW
CSEL1	TRD1 count operation select bit	0 : Count stops at the compare match with the TRDGRA1 register 1 : Count continues at the compare match with the TRDGRA1 register	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of **Notes on Timer RD**.
2. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
3. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
4. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
5. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Timer RD Mode Register



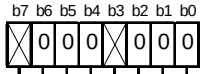
Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	0 : Registers TRD0 and TRD1 operate independently 1 : Registers TRD0 and TRD1 operate synchronously	RW
— (b3-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function select bit(1)	0 : General register 1 : Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function select bit(1)	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function select bit(1)	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function select bit(1)	0 : General register 1 : Buffer register of TRDGRB1 register	RW

NOTE:
1. When selecting 0 (change the TRDGRji register output pin) by the IOj3 (j = C or D) bit in the TRDIORCi (i = 0 or 1) register, set the BFji bit in the TRDMR register to 0.

Figure 14.47 Registers TRDSTR and TRDMR in Output Compare Function

Timer RD PWM Mode Register



Symbol	Address	After Reset
TRDPMR	0139h	10001000b

Bit Symbol	Bit Name	Function	RW
PWMB0	PWM mode of TRDIOB0 select bit	Set to 0 (timer mode) in the output compare function.	RW
PWMC0	PWM mode of TRDIOC0 select bit	Set to 0 (timer mode) in the output compare function.	RW
PWMD0	PWM mode of TRDIOD0 select bit	Set to 0 (timer mode) in the output compare function.	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PWMB1	PWM mode of TRDIOB1 select bit	Set to 0 (timer mode) in the output compare function.	RW
PWMC1	PWM mode of TRDIOC1 select bit	Set to 0 (timer mode) in the output compare function.	RW
PWMD1	PWM mode of TRDIOD1 select bit	Set to 0 (timer mode) in the output compare function.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.48 TRDPMR Register in Output Compare Function

Timer RD Function Control Register

b7	b6	b5	b4	b3	b2	b1	b0
1						0	0

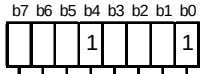
Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode select bits(1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in the output compare function.	RW
CMD1			RW
OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the output compare function.	RW
OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the output compare function.	RW
ADTRG	A/D trigger enable bit (in complementary PWM mode)	This bit is disabled in the output compare function.	RW
ADEG	A/D trigger edge select bit (in complementary PWM mode)	This bit is disabled in the output compare function.	RW
STCLK	External clock input select bit	0 : External clock input disabled 1 : External clock input enabled	RW
PWM3	PWM3 mode select bit(2)	Set this bit to 1 (other than PWM3 mode) in the output compare function.	RW

NOTES:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.49 TRDFCR Register in Output Compare Function

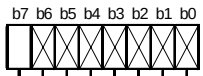
Timer RD Output Master Enable Register 1



Symbol	Address	After Reset
TRDOER1	013Bh	FFh

Bit Symbol	Bit Name	Function	RW
EA0	TRDIOA0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOA0 pin is used as a programmable I/O port.)	RW
EB0	TRDIOB0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	RW
EC0	TRDIOC0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC0 pin is used as a programmable I/O port.)	RW
ED0	TRDIOD0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD0 pin is used as a programmable I/O port.)	RW
EA1	TRDIOA1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOA1 pin is used as a programmable I/O port.)	RW
EB1	TRDIOB1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB1 pin is used as a programmable I/O port.)	RW
EC1	TRDIOC1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC1 pin is used as a programmable I/O port.)	RW
ED1	TRDIOD1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD1 pin is used as a programmable I/O port.)	RW

Timer RD Output Master Enable Register 2



Symbol	Address	After Reset
TRDOER2	013Ch	01111111b

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit(1)	0 : Pulse output forced cutoff input disabled 1 : Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when "L" is applied to the $\overline{\text{INT0}}$ pin.)	RW

NOTE:
1. Refer to **14.3.4 Pulse Output Forced Cutoff.**

Figure 14.50 Registers TRDOER1 to TRDOER2 in Output Compare Function

Timer RD Output Control Register(1, 2)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1					

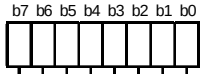
Symbol	Address	After Reset
TRDOCR	013Dh	00h

Bit Symbol	Bit Name	Function	RW
TOA0	TRDIOA0 output level select bit	0 : Initial output “L” 1 : Initial output “H”	RW
TOB0	TRDIOB0 output level select bit	0 : Initial output “L” 1 : Initial output “H”	RW
TOC0	TRDIOC0 initial output level select bit	0 : “L” 1 : “H”	RW
TOD0	TRDIOD0 initial output level select bit		RW
TOA1	TRDIOA1 initial output level select bit		RW
TOB1	TRDIOB1 initial output level select bit		RW
TOC1	TRDIOC1 initial output level select bit		RW
TOD1	TRDIOD1 initial output level select bit		RW

NOTES:
1. Write to the TRDOCR register when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stopped).
2. If the pin function is set for waveform output (refer to **Tables 14.12** to **14.19**), the initial output level is output when the TRDOCR register is set.

Figure 14.51 TRDOCR Register in Output Compare Function

Timer RD Control Register i (i = 0 or 1)



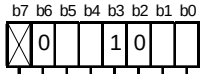
Symbol	Address	After Reset
TRDCR0	0140h	00h
TRDCR1	0150h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source select bits	b2 b1 b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : TRDCLK input(1) 1 1 0 : fOCO40M 1 1 1 : Do not set.	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge select bits(2)	b4 b3 0 0 : Count at the rising edge 0 1 : Count at the falling edge 1 0 : Count at both edges 1 1 : Do not set.	RW
CKEG1			RW
CCLR0	TRDi counter clear select bits	b7 b6 b5 0 0 0 : Disable clear (free-running operation) 0 0 1 : Clear by compare match with the TRDGRAi register 0 1 0 : Clear by compare match with the TRDGRBi register 0 1 1 : Synchronous clear (clear simultaneously with other channel counter)(3) 1 0 0 : Do not set. 1 0 1 : Clear by compare match with the TRDGRCi register 1 1 0 : Clear by compare match with the TRDGRDi register 1 1 1 : Do not set.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This setting is enabled when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. Bits CKEG1 to CKEG0 are enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
3. This setting is enabled when the SYNC bit in the TRDMR register is set to 1 (TRD0 and TRD1 operate synchronously).

Figure 14.52 Registers TRDCR0 to TRDCR1 in Output Compare Function

Timer RD I/O Control Register Ai (i = 0 or 1)



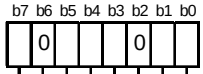
Symbol	Address	After Reset
TRDIORA0	0141h	10001000b
TRDIORA1	0151h	10001000b

Bit Symbol	Bit Name	Function	RW
IOA0	TRDGRA control bits	b1 b0 0 0 : Disable pin output by the compare match (TRDIOAi pin functions as programmable I/O port) 0 1 : "L" output at compare match with the TRDGRAi register 1 0 : "H" output at compare match with the TRDGRAi register 1 1 : Toggle output by compare match with the TRDGRAi register	RW
IOA1			RW
IOA2	TRDGRA mode select bit(1)	Set to 0 (output compare) in the output compare function.	RW
IOA3	Input capture input switch bit	Set to 1.	RW
IOB0	TRDGRB control bits	b5 b4 0 0 : Disable pin output by the compare match (TRDIOBi pin functions as programmable I/O port) 0 1 : "L" output at compare match with the TRDGRBi register 1 0 : "H" output at compare match with the TRDGRBi 1 1 : Toggle output by compare match with the TRDGRBi register	RW
IOB1			RW
IOB2	TRDGRB mode select bit(2)	Set to 0 (output compare) in the output compare function.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. To select 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (the TRDGRDi register is used as a buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

Figure 14.53 Registers TRDIORA0 to TRDIORA1 in Output Compare Function

Timer RD I/O Control Register Ci (i = 0 or 1)



Symbol	Address	After Reset
TRDIORC0	0142h	10001000b
TRDIORC1	0152h	10001000b

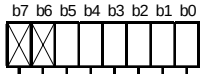
Bit Symbol	Bit Name	Function	RW
IOC0	TRDGRC control bits	b1 b0 0 0 : Disable pin output by compare match 0 1 : "L" output at compare match with the TRDGRCi register 1 0 : "H" output at compare match with the TRDGRCi register 1 1 : Toggle output by compare match with the TRDGRCi register	RW
IOC1			RW
IOC2	TRDGRC mode select bit(1)	Set to 0 (output compare) in the output compare function.	RW
IOC3	TRDGRC register function select bit	0 : TRDIOA output register (Refer to **14.3.6.1 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi.**) 1 : General register or buffer register	RW
IOD0	TRDGRD control bits	b5 b4 0 0 : Disable pin output by compare match 0 1 : "L" output at compare match with the TRDGRDi register 1 0 : "H" output at compare match with the TRDGRDi register 1 1 : Toggle output by compare match with the TRDGRDi register	RW
IOD1			RW
IOD2	TRDGRD mode select bit(2)	Set to 0 (output compare) in the output compare function.	RW
IOD3	TRDGRD register function select bit	0 : TRDIOB output register (Refer to **14.3.6.1 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi.**) 1 : General register or buffer register	RW

NOTES:

1. To select 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (the TRDGRDi register is used as a buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

Figure 14.54 Registers TRDIORC0 to TRDIORC1 in Output Compare Function

Timer RD Status Register i (i=0 or 1)



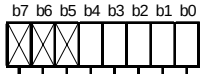
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register(3).	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register(3).	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the TRDi register overflows.	RW
UDF	Underflow flag(1)	This bit is disabled in the output compare function.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

Figure 14.55 Registers TRDSR0 to TRDSR1 in Output Compare Function

Timer RD Interrupt Enable Register i (i = 0 or 1)

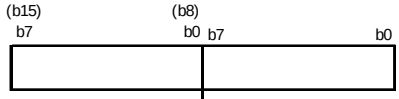


Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable interrupt (IMIA) by the IMFA bit 1 : Enable interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable interrupt (IMIB) by the IMFB bit 1 : Enable interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable interrupt (IMIC) by the IMFC bit 1 : Enable interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable interrupt (IMID) by the IMFD bit 1 : Enable interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0 : Disable interrupt (OVI) by the OVF bit 1 : Enable interrupt (OVI) by the OVF bit	RW
— (b7-b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.56 Registers TRDIER0 to TRDIER1 in Output Compare Function

Timer RD Counter i (i = 0 or 1)(1)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h
TRD1	0157h-0156h	0000h

Function	Setting Range	RW
Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

Figure 14.57 Registers TRD0 to TRD1 in Output Compare Function

Timer RD General Register Ai, Bi, Ci and Di (i = 0 or 1)(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.26 TRDGRji Register Function in Output Compare Function**.	RW

NOTE:
1. Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

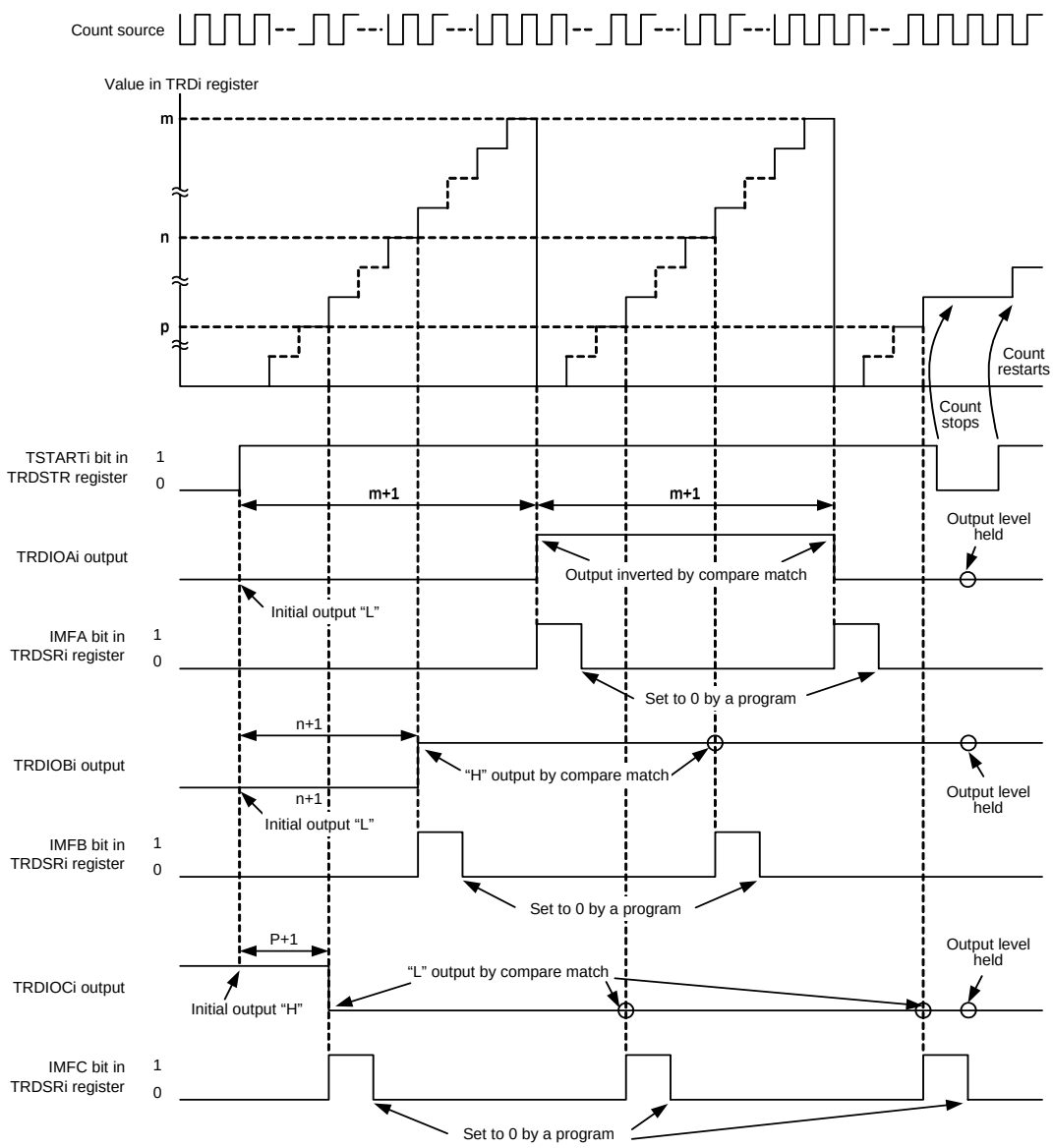
Figure 14.58 Registers TRDGRAi, TRDGRBi, TRDGRCi, and TRDGRDi in Output Compare Function

The following registers are disabled in the output compare function: TRDDF0, TRDDF1, TRDPOCR0, and TRDPOCR1.

Table 14.26 TRDGRji Register Function in Output Compare Function

Register	Setting		Register Function	Output-Compare Output Pin
	BFji	IOj3		
TRDGRAi	–	–	General register. Write the compare value.	TRDIOAi
TRDGRBi				TRDIOBi
TRDGRCi	0	1	General register. Write the compare value.	TRDIOCi
TRDGRDi				TRDIODi
TRDGRCi	1	1	Buffer register. Write the next compare value. (Refer to **14.3.2 Buffer Operation**.)	TRDIOAi
TRDGRDi				TRDIOBi
TRDGRCi	0	0	TRDIOAi output control. (Refer to **14.3.6.1 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**.)	TRDIOAi
TRDGRDi				TRDIOBi

i = 0 or 1, j = either A, B, C, or D
BFji: Bit in TRDMR register IOj3: Bit in TRDIORCi register



i = 0 or 1

M: Value set in TRDGRAi register
n: Value set in TRDGRBi register
p: Value set in TRDGRCi register

The above applies under the following conditions:
The CSELi bit in the TRDSTR register is set to 1 (the TRDi register is not stopped by compare match).
Bits BFCi and BFDi in the TRDMR register are set to 0 (registers TRDGRCi and TRDGRDi are not used as buffer registers).
Bits EAi, EBi, and ECi in the TRDOER1 register are set to 0 (enable the TRDIOAi, TRDIOBi and TRDIOCi pin outputs).
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (set the TRDi register to 000h by compare match in the TRDGRAi register).
Bits TOAi and TOBi in the TRDOCR register is set to 0 (initial output "L" to compare match), the TOCi bit is set to 1 (initial output "H" to compare match).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 011b (TRDIOAi output inverted at TRDGRAi register compare match).
Bits IOB2 to IOB0 in the TRDIORAi register are set to 010b (TRDIOBi "H" output at TRDGRBi register compare match).
Bits IOC3 to IOC0 in the TRDIORCi register are set to 1001b (TRDIOCi "L" output at TRDGRCi register compare match).
The IOD3 bit in the TRDIORCi register is set to 1 (TRDGRDi register does not control TRDIOBi pin output).

Figure 14.59 Operating Example of Output Compare Function

14.3.6.1 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi

The TRDGRCi register can be used for output control of the TRDIOAi pin, and the TRDGRDi register can be used for output control of the TRDIOBi pin. Therefore, each pin output can be controlled as follows:

- TRDIOAi output is controlled by the values in registers TRDGRAi and TRDGRCi.
- TRDIOBi output is controlled by the values in registers TRDGRBi and TRDGRDi.

Change output pins in registers TRDGRCi and TRDGRDi as follows:

- Select 0 (change TRDGRji register output pin) by the IOj3 (j = C or D) bit in the TRDIORCi register.
- Set the BFji bit in the TRDMR register to 0 (general register).
- Set different values in registers TRDGRCi and TRDGRAi. Also, set different values in registers TRDGRDi and TRDGRBi.

Figure 14.61 shows an Operating Example When TRDGRCi Register is Used for Output Control of TRDIOAi Pin and TRDGRDi Register is Used for Output Control of TRDIOBi Pin.

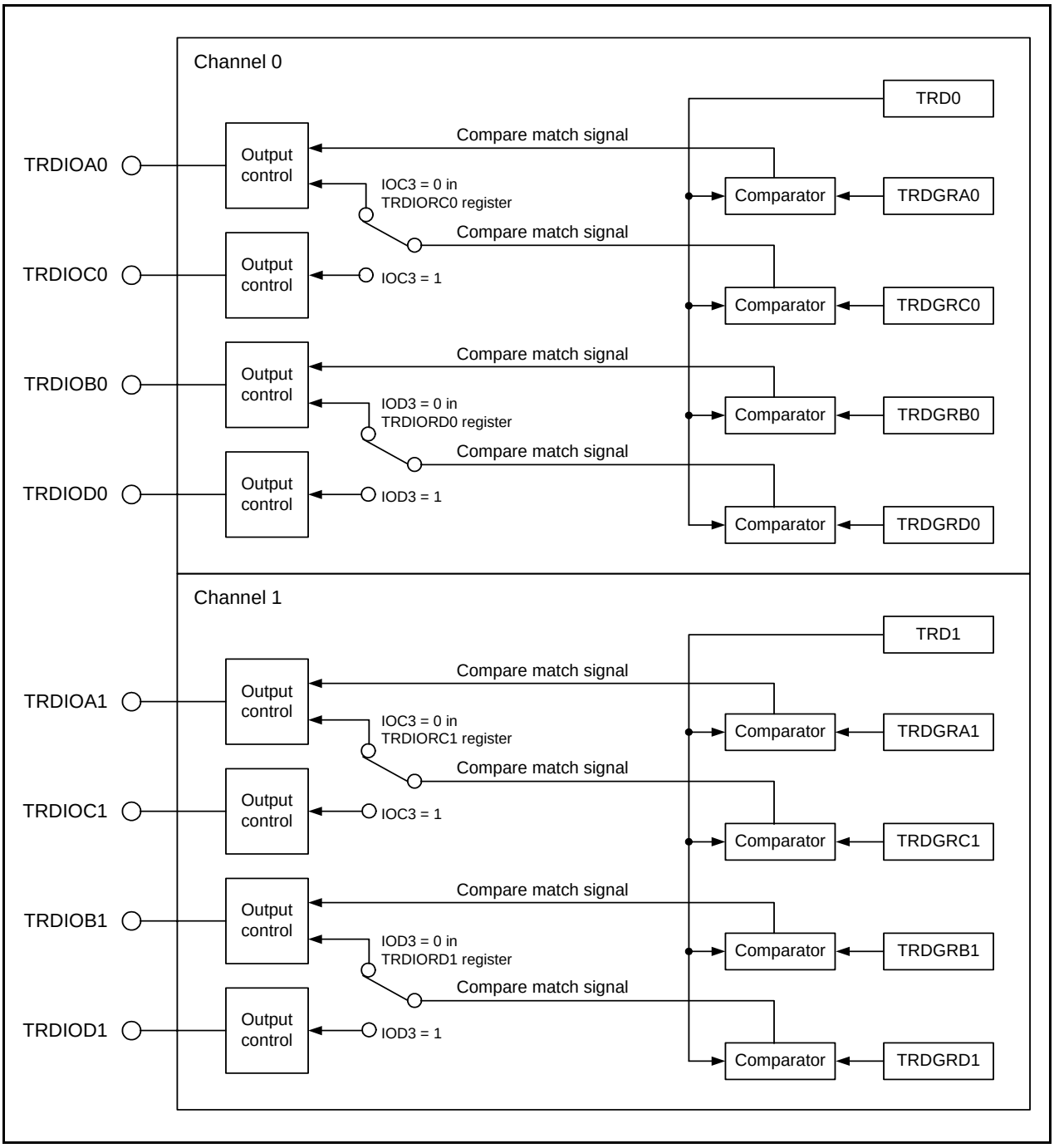
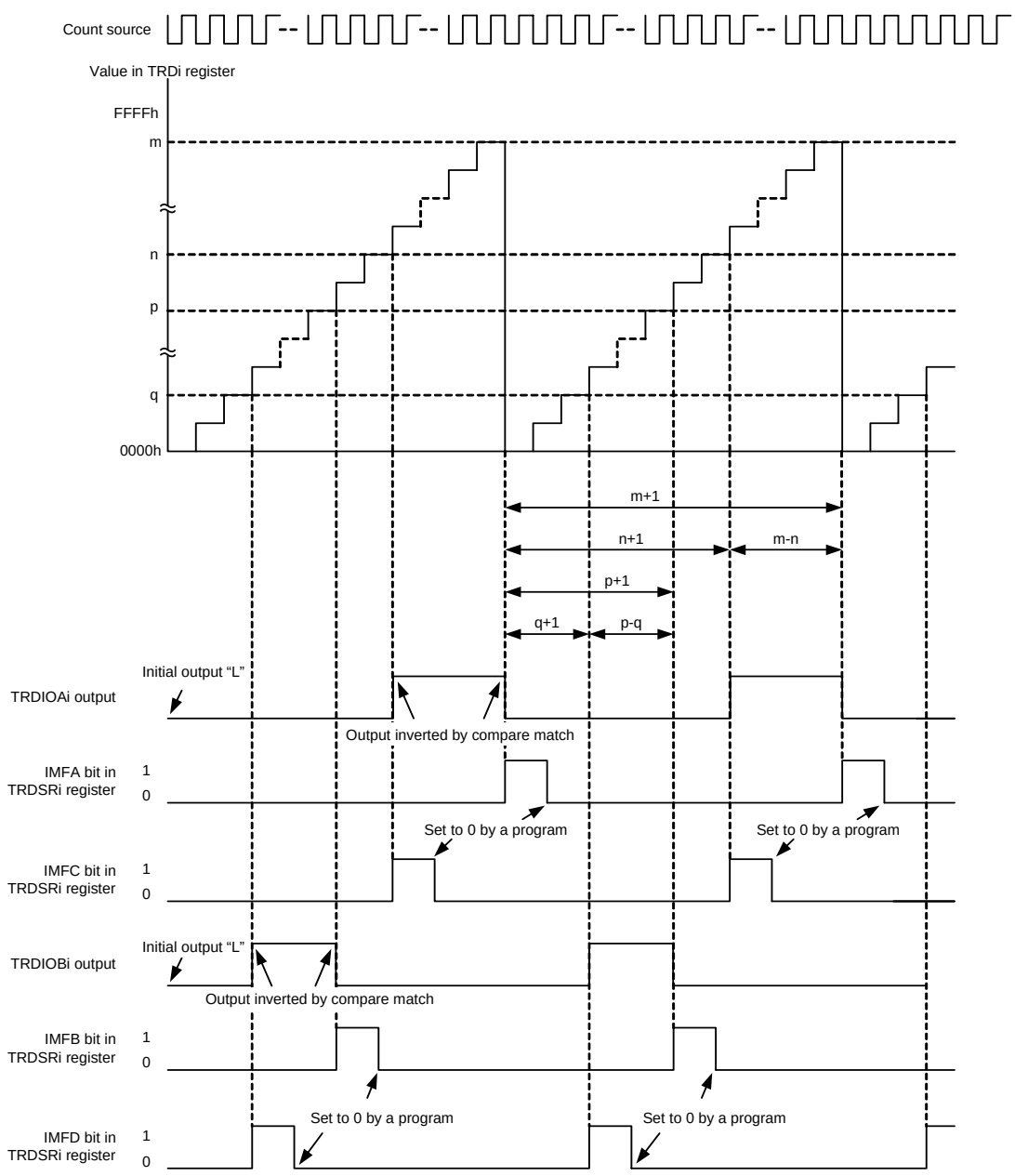


Figure 14.60 Changing Output Pins in Registers TRDGRCi and TRDGRDi



m: Value set in TRDGRAi register
n: Value set in TRDGRCi register
p: Value set in TRDGRBi register
q: Value set in TRDGRDi register

i = 0 or 1

The above applies under the following conditions:
The CSELi bit in the TRDSTR register is set to 1 (the TRDi register is not stopped by compare match).
Bits BFCi and BFDi in the TRDMR register are set to 0 (registers TRDGRCi and TRDGRDi are not used as buffer register).
Bits EAi and EBi in the TRDOER1 register are set to 0 (enable TRDIOAi and TRDIOBi pin outputs).
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (set the TRDi register to 0000h by compare match in the TRDGRAi register).
Bits TOAi and TOBi in the TRDOCR register are set to 0 (initial output "L" to compare match).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 011b (TRDIOAi output inverted at TRDGRAi register compare match).
Bits IOB2 to IOB0 in the TRDIORAi register are set to 011b (TRDIOBi output inverted at TRDGRBi register compare match).
Bits IOC3 to IOC0 in the TRDIORCi register are set to 0011b (TRDIOAi output inverted at TRDGRCi register compare match).
Bits IOD3 to IOD0 in the TRDIORCi register are set to 0011b (TRDIOBi output inverted at TRDGRDi register compare match).

Figure 14.61 Operating Example When TRDGRCi Register is Used for Output Control of TRDIOAi Pin and TRDGRDi Register is Used for Output Control of TRDIOBi Pin

14.3.7 PWM Mode

In PWM mode, a PWM waveform is output. Up to 3 PWM waveforms with the same period can be output by 1 channel. Also, up to 6 PWM waveforms with the same period can be output by synchronizing channels 0 and 1. Since this mode functions by a combination of the TRDIOji (i = 0 or 1, j = B, C, or D) pin and TRDGRji register, the PWM mode, or any other mode or function, can be selected for each individual pin. (However, since the TRDGRAi register is used when using any pin for PWM mode, the TRDGRAi register cannot be used for other modes.)

Figure 14.62 shows a Block Diagram of PWM Mode, and Table 14.27 lists the PWM Mode Specifications. Figures 14.63 to 14.72 show the Registers Associated with PWM Mode, and Figures 14.73 and 14.74 show Operating Examples of PWM Mode.

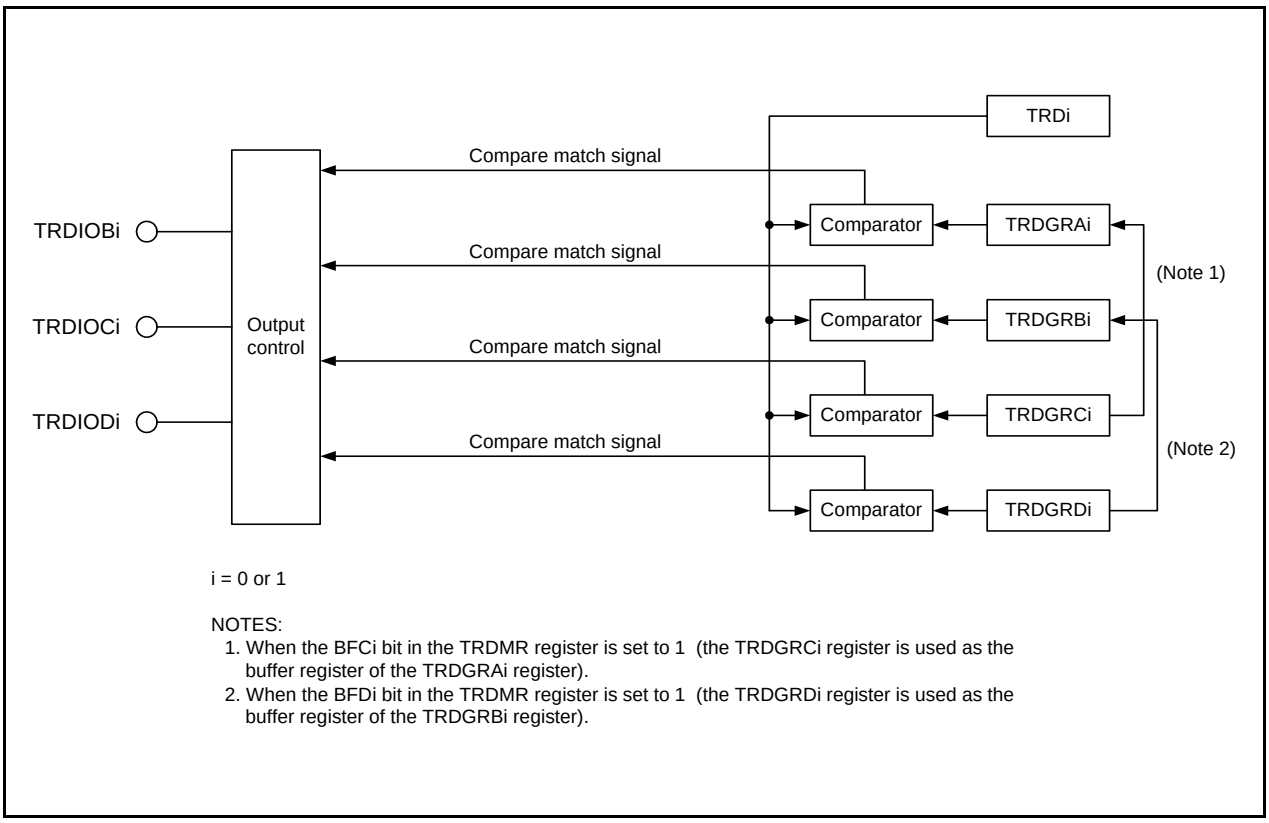
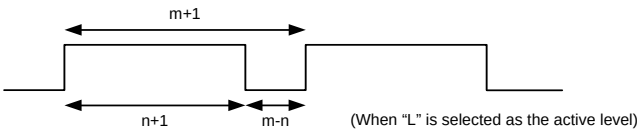


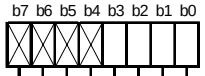
Figure 14.62 Block Diagram of PWM Mode

Table 14.27 PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program)
Count operations	Increment
PWM waveform	PWM period: 1/fk x (m+1) Active level width: 1/fk x (m-n) Inactive level width: 1/fk x (n+1) fk: Frequency of count source m: Value set in the TRDGRAi register n: Value set in the TRDGRji register 
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRAi register. The PWM output pin holds level after output change by compare match.
Interrupt request generation timing	• Compare match (The content of the TRDi register matches content of the TRDGRhi register.) • TRDi register overflows
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOA1 pin function	Programmable I/O port
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOB1, TRDIOC1, TRDIOD1 pin functions	Programmable I/O port or pulse output (selectable by pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	The value can be written to the TRDi register.
Select functions	• 1 to 3 PWM output pins selected per 1 channel Either 1 pin or multiple pins of the TRDIOBi, TRDIOCi or TRDIODi pin. • The active level selected by pin. • Initial output level selected by pin. • Synchronous operation (Refer to **14.3.3 Synchronous Operation**.) • Buffer operation (Refer to **14.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **14.3.4 Pulse Output Forced Cutoff**.)

i = 0 or 1
j = either B, C, or D
h = either A, B, C, or D

Timer RD Start Register(1)

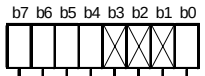


Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag(4)	0 : Count stops(2) 1 : Count starts	RW
TSTART1	TRD1 count start flag(5)	0 : Count stops(3) 1 : Count starts	RW
CSEL0	TRD0 count operation select bit	0 : Count stops at compare match with the TRDGRA0 register 1 : Count continues at compare match with the TRDGRA0 register	RW
CSEL1	TRD1 count operation select bit	0 : Count stops at compare match with the TRDGRA1 register 1 : Count continues at compare match with the TRDGRA1 register	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of **Notes on Timer RD**.
2. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
3. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
4. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
5. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Timer RD Mode Register

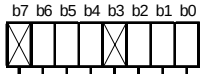


Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	0 : Registers TRD0 and TRD1 operate independently 1 : Registers TRD0 and TRD1 operate synchronously	RW
— (b3-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function select bit	0 : General register 1 : Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function select bit	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function select bit	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function select bit	0 : General register 1 : Buffer register of TRDGRB1 register	RW

Figure 14.63 Registers TRDSTR and TRDMR in PWM Mode

Timer RD PWM Mode Register



Symbol	Address	After Reset
TRDPMR	0139h	10001000b

Bit Symbol	Bit Name	Function	RW
PWMB0	PWM mode of TRDIOB0 select bit	0 : Timer mode 1 : PWM mode	RW
PWMC0	PWM mode of TRDIOC0 select bit	0 : Timer mode 1 : PWM mode	RW
PWMD0	PWM mode of TRDIOD0 select bit	0 : Timer mode 1 : PWM mode	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PWMB1	PWM mode of TRDIOB1 select bit	0 : Timer mode 1 : PWM mode	RW
PWMC1	PWM mode of TRDIOC1 select bit	0 : Timer mode 1 : PWM mode	RW
PWMD1	PWM mode of TRDIOD1 select bit	0 : Timer mode 1 : PWM mode	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.64 TRDPMR Register in PWM Mode

Timer RD Function Control Register

b7	b6	b5	b4	b3	b2	b1	b0
1						0	0

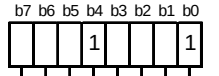
Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode select bits(1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in PWM mode.	RW
CMD1			RW
OLS0	Normal-phase output level select Bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM mode.	RW
OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM mode.	RW
ADTRG	A/D trigger enable bit (in complementary PWM mode)	This bit is disabled in PWM mode.	RW
ADEG	A/D trigger edge select bit (in complementary PWM mode)	This bit is disabled in PWM mode.	RW
STCLK	External clock input select bit	0 : External clock input disabled 1 : External clock input enabled	RW
PWM3	PWM3 mode select bit(2)	Set this bit to 1 (other than PWM3 mode) in PWM mode.	RW

NOTES:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.65 TRDFCR Register in PWM Mode

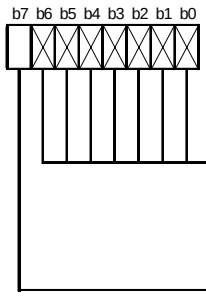
Timer RD Output Master Enable Register 1



Symbol	Address	After Reset
TRDOER1	013Bh	FFh

Bit Symbol	Bit Name	Function	RW
EA0	TRDIOA0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOA0 pin is used as a programmable I/O port.)	RW
EB0	TRDIOB0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	RW
EC0	TRDIOC0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC0 pin is used as a programmable I/O port.)	RW
ED0	TRDIOD0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD0 pin is used as a programmable I/O port.)	RW
EA1	TRDIOA1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOA1 pin is used as a programmable I/O port.)	RW
EB1	TRDIOB1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB1 pin is used as a programmable I/O port.)	RW
EC1	TRDIOC1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC1 pin is used as a programmable I/O port.)	RW
ED1	TRDIOD1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD1 pin is used as a programmable I/O port.)	RW

Timer RD Output Master Enable Register 2



Symbol	Address	After Reset
TRDOER2	013Ch	01111111b

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit(1)	0 : Pulse output forced cutoff input disabled 1 : Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when "L" is applied to the $\overline{\text{INT0}}$ pin.)	RW

NOTE:
1. Refer to **14.3.4 Pulse Output Forced Cutoff.**

Figure 14.66 Registers TRDOER1 to TRDOER2 in PWM Mode

Timer RD Output Control Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
			0				0

Symbol	Address	After Reset
TRDOCR	013Dh	00h

Bit Symbol	Bit Name	Function	RW
TOA0	TRDIOA0 output level select bit	Set this bit to 0 (enable output) in PWM mode.	RW
TOB0	TRDIOB0 output level select bit(2)	0 : Initial output is inactive level 1 : Initial output is active level	RW
TOC0	TRDIOC0 initial output level select bit(2)		RW
TOD0	TRDIOD0 initial output level select bit(2)		RW
TOA1	TRDIOA1 initial output level select bit	Set this bit to 0 (enable output) in PWM mode.	RW
TOB1	TRDIOB1 initial output level select bit(2)	0 : Inactive level 1 : Active level	RW
TOC1	TRDIOC1 initial output level select bit(2)		RW
TOD1	TRDIOD1 initial output level select bit(2)		RW

NOTES:
1. Write to the TRDOCR register when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **Tables 14.13** to **14.15** and **Tables 14.17** to **14.19**), the initial output level is output when the TRDOCR register is set.

Timer RD Control Register i (i = 0 or 1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1					

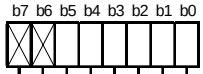
Symbol	Address	After Reset
TRDCR0	0140h	00h
TRDCR1	0150h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source select bits	b2 b1 b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : TRDCLK input(1) 1 1 0 : fOCO40M 1 1 1 : Do not set.	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge select bits(2)	b4 b3 0 0 : Count at the rising edge 0 1 : Count at the falling edge 1 0 : Count at both edges 1 1 : Do not set.	RW
CKEG1			RW
CCLR0	TRDi counter clear select bits	Set to 001b (the TRDi register cleared at compare match with TRDGRAi register) in PWM mode.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This setting is enabled when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. Bits CKEG1 to CKEG0 are enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

Figure 14.67 Registers TRDOCR and TRDCR0 to TRDCR1 in PWM Mode

Timer RD Status Register i (i=0 or 1)



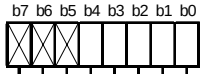
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register(3).	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register(3).	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the TRDi register overflows.	RW
UDF	Underflow flag(1)	This bit is disabled in PWM mode.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

Figure 14.68 Registers TRDSR0 to TRDSR1 in PWM Mode

Timer RD Interrupt Enable Register i (i = 0 or 1)

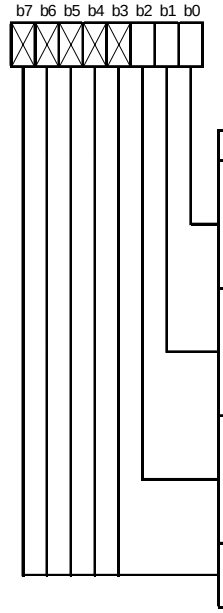


Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable interrupt (IMIA) by the IMFA bit 1 : Enable interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable interrupt (IMIB) by the IMFB bit 1 : Enable interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable interrupt (IMIC) by the IMFC bit 1 : Enable interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable interrupt (IMID) by the IMFD bit 1 : Enable interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0 : Disable interrupt (OVI) by the OVF bit 1 : Enable interrupt (OVI) by the OVF bit	RW
— (b7-b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.69 Registers TRDIER0 to TRDIER1 in PWM Mode

Timer RD PWM Mode Output Level Control Register i (i = 0 or 1)

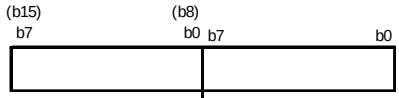


Symbol	Address	After Reset
TRDPOCR0	0145h	11111000b
TRDPOCR1	0155h	11111000b

Bit Symbol	Bit Name	Function	RW
POLB	PWM mode output level control bit B	0 : "L" active TRDIOBi output level is selected 1 : "H" active TRDIOBi output level is selected	RW
POLC	PWM mode output level control bit C	0 : "L" active TRDIOCi output level is selected 1 : "H" active TRDIOCi output level is selected	RW
POLD	PWM mode output level control bit D	0 : "L" active TRDIODi output level is selected 1 : "H" active TRDIODi output level is selected	RW
— (b7-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.70 Registers TRDPOCR0 to TRDPOCR1 in PWM Mode

Timer RD Counter i (i = 0 or 1)(1)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h
TRD1	0157h-0156h	0000h

Function	Setting Range	RW
Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

Figure 14.71 Registers TRD0 to TRD1 in PWM Mode

Timer RD General Registers Ai, Bi, Ci, and Di (i = 0 or 1)(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.28 TRDGRji Register Functions in PWM Mode.**	RW

NOTE:
1. Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

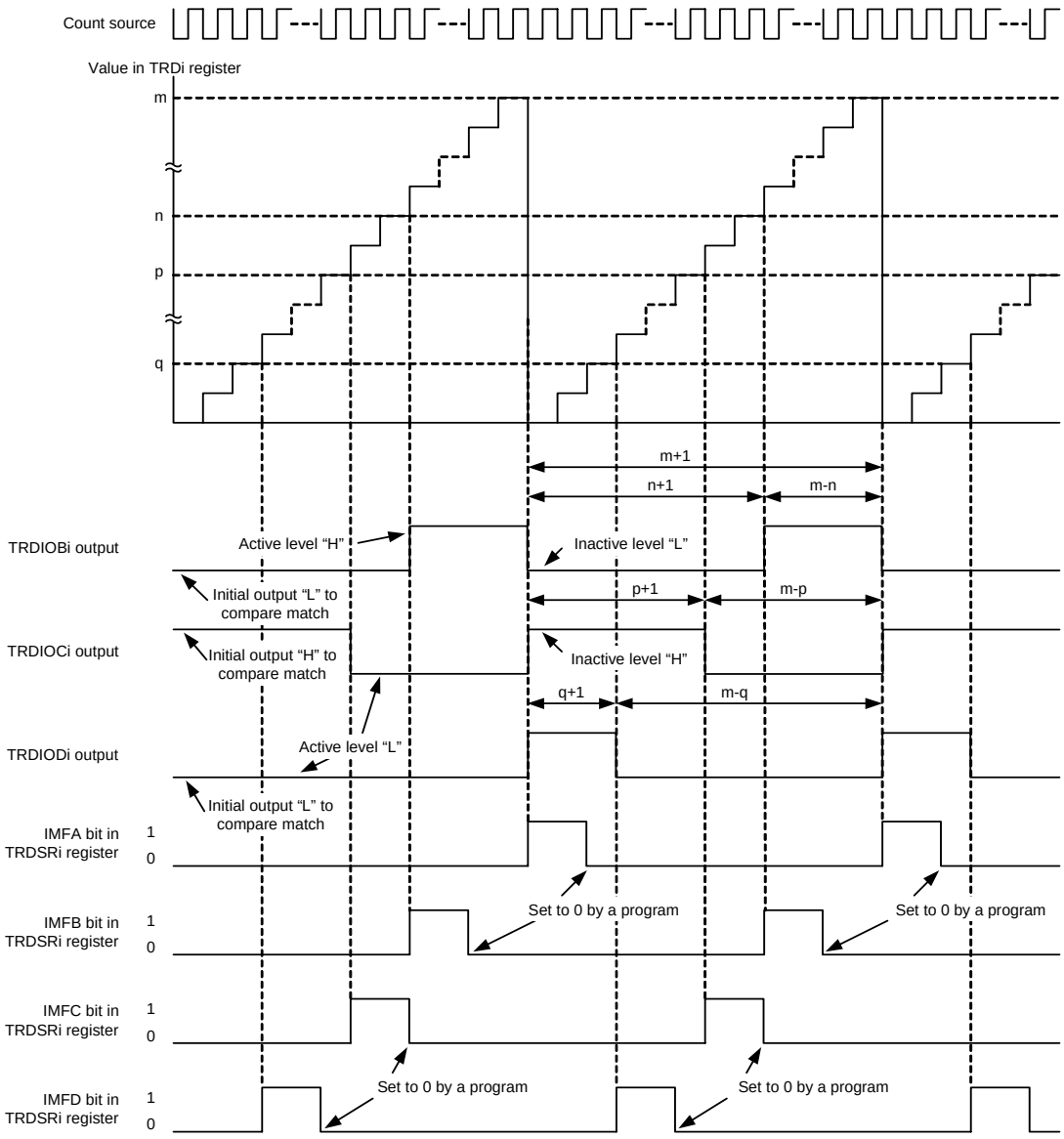
Figure 14.72 Registers TRDGRAi, TRDGRBi, TRDGRCi, and TRDGRDi in PWM Mode

The following registers are disabled in the PWM mode: TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDIORA1, and TRDIORC1.

Table 14.28 TRDGRji Register Functions in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRAi	–	General register. Set the PWM period	–
TRDGRBi	–	General register. Set the changing point of PWM output	TRDIOBi
TRDGRCi	BFCi = 0	General register. Set the changing point of PWM output	TRDIOCi
TRDGRDi	BFDi = 0		TRDIODi
TRDGRCi	BFCi = 1	Buffer register. Set the next PWM period. (Refer to **14.3.2 Buffer Operation**.)	–
TRDGRDi	BFDi = 1	Buffer register. Set the changing point of the next PWM output. (Refer to **14.3.2 Buffer Operation**.)	TRDIOBi

i = 0 or 1
BFCi, BFDi: Bits in TRDMR register



i = 0 or 1

m: Value set in TRDGRAi register
n: Value set in TRDGRBi register
p: Value set in TRDGRCi register
q: Value set in TRDGRDi register

The above applies under the following conditions:
Bits BFCi and BFDi in the TRDMR register are set to 0 (registers TRDGRCi and TRDGRDi are not used as buffer registers).
Bits EBi, ECi and EDi in the TRDOER1 register are set to 0 (enable TRDIOBi, TRDIOCi and TRDIODi pin outputs).
Bits TOBi and TOCi in the TRDOCR register are set to 0 (inactive level), the TODi bit is set to 1 (active level).
The POLB bit in the TRDPOCRi register is set to 1 (active level “H”), bits POLC and POLD are set to 0 (active level “L”).

Figure 14.73 Operating Example of PWM Mode

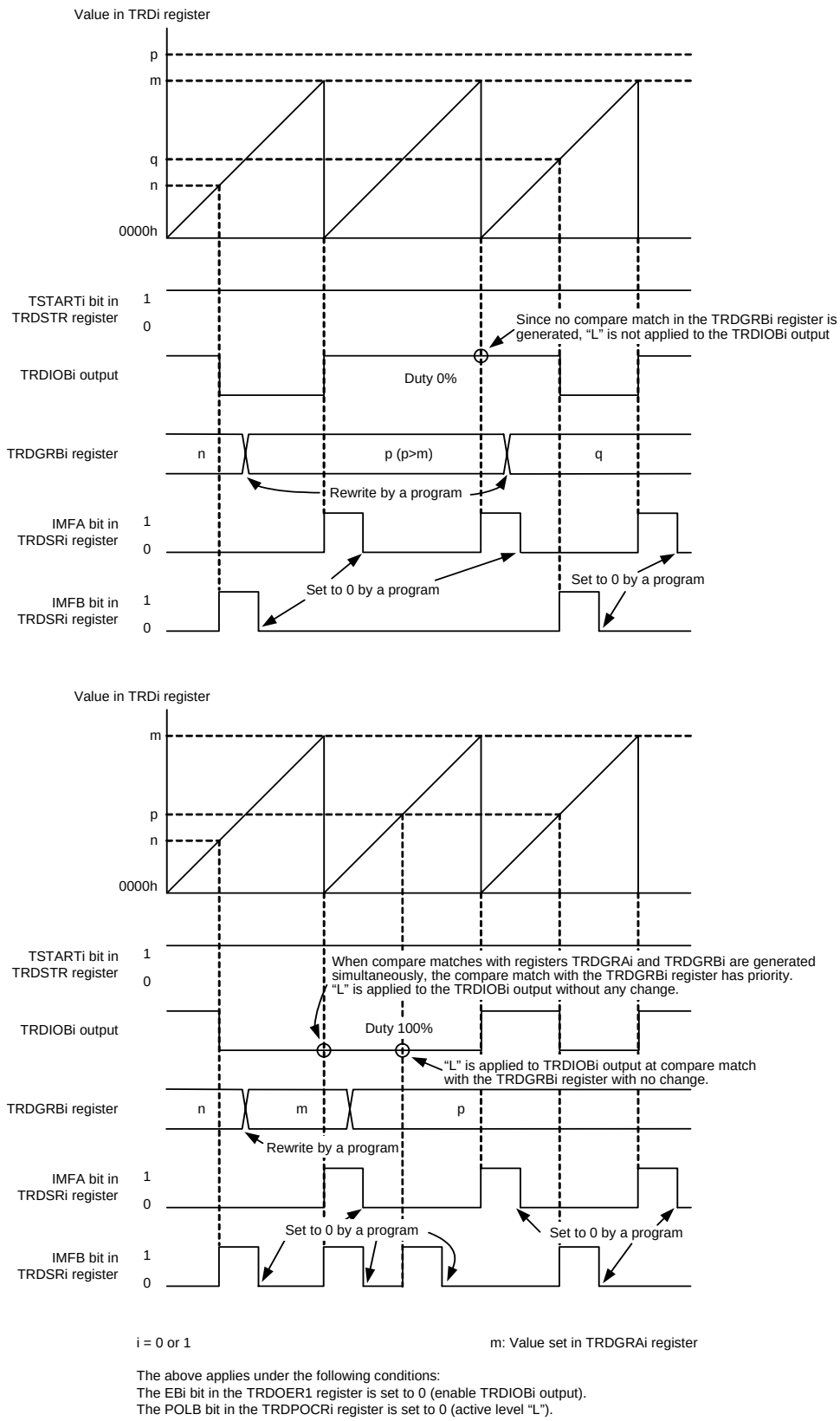
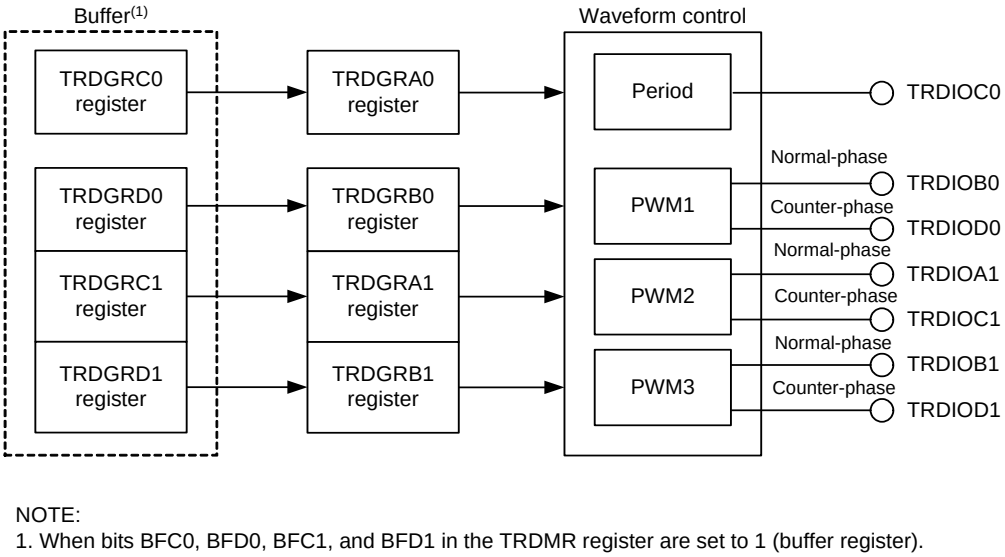


Figure 14.74 Operating Example of PWM Mode (Duty 0%, Duty 100%)

14.3.8 Reset Synchronous PWM Mode

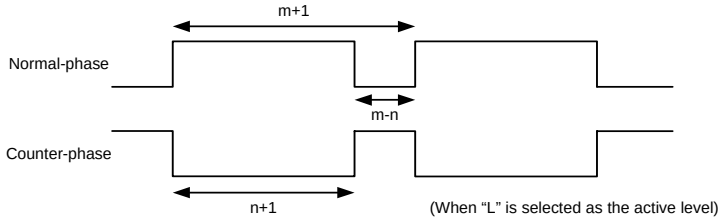
In this mode, 3 normal-phases and 3 counter-phases of the PWM waveform are output with the same period (three-phase, sawtooth wave modulation, and no dead time).
Figure 14.75 shows a Block Diagram of Reset Synchronous PWM Mode, and Table 14.29 lists the Reset Synchronous PWM Mode Specifications. Figures 14.76 to 14.83 show the Registers Associated with Reset Synchronous PWM Mode and Figure 14.84 shows an Operating Example of Reset Synchronous PWM Mode.
Refer to **Figure 14.74 Operating Example of PWM Mode (Duty 0%, Duty 100%)** for an operating example of PWM Mode with duty 0% and duty 100%.



NOTE:
1. When bits BFC0, BFD0, BFC1, and BFD1 in the TRDMR register are set to 1 (buffer register).

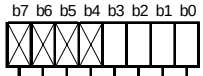
Figure 14.75 Block Diagram of Reset Synchronous PWM Mode

Table 14.29 Reset Synchronous PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program)
Count operations	The TRD0 register is incremented (the TRD1 register is not used).
PWM waveform	PWM period : 1/fk × (m+1) Active level width of normal-phase : 1/fk × (m-n) Active level width of counter-phase: 1/fk × (n+1) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output), Value set in the TRDGRA1 register (PWM2 output), Value set in the TRDGRB1 register (PWM3 output) 
Count start condition	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRA0 register. The PWM output pin holds level after output change at compare match.
Interrupt request generation timing	• Compare match (the content of the TRD0 register matches content of registers TRDGRj0, TRDGRA1, and TRDGRB1). • The TRD0 register overflows
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOB0 pin function	PWM1 output normal-phase output
TRDIOD0 pin function	PWM1 output counter-phase output
TRDIOA1 pin function	PWM2 output normal-phase output
TRDIOC1 pin function	PWM2 output counter-phase output
TRDIOB1 pin function	PWM3 output normal-phase output
TRDIOD1 pin function	PWM3 output counter-phase output
TRDIOC0 pin function	Output inverted every PWM period
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRD0 register.
Write to timer	The value can be written to the TRD0 register.
Select functions	• The active level of normal-phase and counter-phase and initial output level selected individually. • Buffer operation (Refer to **14.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **14.3.4 Pulse Output Forced Cutoff**.)

j = either A, B, C, or D

Timer RD Start Register(1)

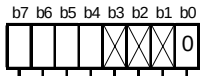


Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag(4)	0 : Count stops(2) 1 : Count starts	RW
TSTART1	TRD1 count start flag(5)	0 : Count stops(3) 1 : Count starts	RW
CSEL0	TRD0 count operation select bit	0 : Count stops at compare match with the TRDGRA0 register 1 : Count continues at compare match with the TRDGRA0 register	RW
CSEL1	TRD1 count operation select bit	0 : Count stops at compare match with the TRDGRA1 register 1 : Count continues at compare match with the TRDGRA1 register	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of **Notes on Timer RD**.
2. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
3. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
4. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
5. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Timer RD Mode Register



Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	Set this bit to 0 (registers TRD0 and TRD1 operate independently) in reset synchronous PWM mode.	RW
— (b3-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function select bit	0 : General register 1 : Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function select bit	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function select bit	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function select bit	0 : General register 1 : Buffer register of TRDGRB1 register	RW

Figure 14.76 Registers TRDSTR and TRDMR in Reset Synchronous PWM Mode

Timer RD Function Control Register

b7	b6	b5	b4	b3	b2	b1	b0
						0	1

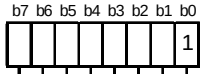
Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode select bits(1, 2)	Set to 01b (reset synchronous PWM mode) in reset synchronous PWM mode.	RW
CMD1			RW
OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	0 : Initial output “H” Active level “L” 1 : Initial output “L” Active level “H”	RW
OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	0 : Initial output “H” Active level “L” 1 : Initial output “L” Active level “H”	RW
ADTRG	A/D trigger enable bit (in complementary PWM mode)	This bit is disabled in reset synchronous PWM mode.	RW
ADEG	A/D trigger edge select bit (in complementary PWM mode)	This bit is disabled in reset synchronous PWM mode.	RW
STCLK	External clock input select bit	0 : External clock input disabled 1 : External clock input enabled	RW
PWM3	PWM3 mode select bit(3)	This bit is disabled in reset synchronous PWM mode.	RW

NOTES:
1. When bits CMD1 to CMD0 are set to 01b, 10b, or 11b, the MCU enters reset synchronous PWM mode or complementary PWM mode in spite of the setting of the TRDPMR register.
2. Set bits CMD1 to CMD0 w hen both the TSTART0 and TSTART1 bits are set to 0 (count stops).
3. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.77 TRDFCR Register in Reset Synchronous PWM Mode

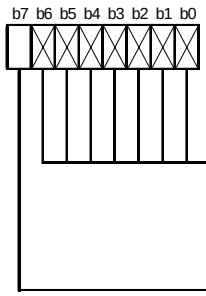
Timer RD Output Master Enable Register 1



Symbol	Address	After Reset
TRDOER1	013Bh	FFh

Bit Symbol	Bit Name	Function	RW
EA0	TRDIOA0 output disable bit	Set this bit to 1 (the TRDIOA0 pin is used as a programmable I/O port) in reset synchronous PWM mode.	RW
EB0	TRDIOB0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	RW
EC0	TRDIOC0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC0 pin is used as a programmable I/O port.)	RW
ED0	TRDIOD0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD0 pin is used as a programmable I/O port.)	RW
EA1	TRDIOA1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOA1 pin is used as a programmable I/O port.)	RW
EB1	TRDIOB1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB1 pin is used as a programmable I/O port.)	RW
EC1	TRDIOC1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC1 pin is used as a programmable I/O port.)	RW
ED1	TRDIOD1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD1 pin is used as a programmable I/O port.)	RW

Timer RD Output Master Enable Register 2



Symbol	Address	After Reset
TRDOER2	013Ch	01111111b

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit(1)	0 : Pulse output forced cutoff input disabled 1 : Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when "L" is applied to the $\overline{\text{INT0}}$ pin.)	RW

NOTE:
1. Refer to **14.3.4 Pulse Output Forced Cutoff.**

Figure 14.78 Registers TRDOER1 to TRDOER2 in Reset Synchronous PWM Mode

Timer RD Control Register 0(3)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1					

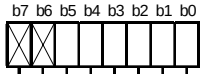
Symbol	Address	After Reset
TRDCR0	0140h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source select bits	b2 b1b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : TRDCLK input(1) 1 1 0 : fOCO40M 1 1 1 : Do not set.	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge select bits(2)	b4 b3 0 0 : Count at the rising edge 0 1 : Count at the falling edge 1 0 : Count at both edges 1 1 : Do not set.	RW
CKEG1			RW
CCLR0	TRD0 counter clear select bits	Set to 001b (TRD0 register cleared at compare match with TRDGRA0 register) in reset synchronous PWM mode.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This setting is enabled when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. Bits CKEG1 to CKEG0 are enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
3. The TRDCR1 register is not used in reset synchronous PWM mode.

Figure 14.79 TRDCR0 Register in Reset Synchronous PWM Mode

Timer RD Status Register i (i = 0 or 1)



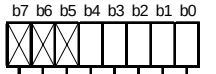
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0"] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register(3).	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register(3).	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the TRDi register overflows.	RW
UDF	Underflow flag(1)	This bit is disabled in reset synchronous PWM mode.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit (this bit remains 1 even if it is set to 1 from 0 after reading, and writing 0).
   - This bit remains unchanged if 1 is written to it.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

Figure 14.80 Registers TRDSR0 to TRDSR1 in Reset Synchronous PWM Mode

Timer RD Interrupt Enable Register i (i = 0 or 1)

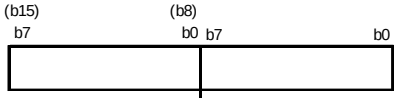


Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable interrupt (IMIA) by the IMFA bit 1 : Enable interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable interrupt (IMIB) by the IMFB bit 1 : Enable interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable interrupt (IMIC) by the IMFC bit 1 : Enable interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable interrupt (IMID) by the IMFD bit 1 : Enable interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0 : Disable interrupt (OVI) by the OVF bit 1 : Enable interrupt (OVI) by the OVF bit	RW
— (b7-b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.81 Registers TRDIER0 to TRDIER1 in Reset Synchronous PWM Mode

Timer RD Counter 0(1, 2)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h

Function	Setting Range	RW
Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	RW

NOTES:
1. Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.
2. The TRD1 register is not used in reset synchronous PWM mode.

Figure 14.82 TRD0 Registrar in Reset Synchronous PWM Mode

Timer RD General Registers Ai, Bi, Ci, and Di (i = 0 or 1)(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.30 TRDGRji Register Functions in Reset Synchronous PWM Mode.**	RW

NOTE:
1. Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

Figure 14.83 Registers TRDGRAi, TRDGRBi, TRDGRCi, and TRDGRDi in Reset Synchronous PWM Mode

The following registers are disabled in the reset synchronous PWM mode: TRDPMR, TRDOCR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1.

Table 14.30 TRDGRji Register Functions in Reset Synchronous PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period.	(Output inverted every PWM period and TRDIOC0 pin)
TRDGRB0	–	General register. Set the changing point of PWM1 output.	TRDIOB0 TRDIOD0
TRDGRC0	BFC0 = 0	(These registers are not used in reset synchronous PWM mode.)	–
TRDGRD0	BFD0 = 0		
TRDGRA1	–	General register. Set the changing point of PWM2 output.	TRDIOA1 TRDIOC1
TRDGRB1	–	General register. Set the changing point of PWM3 output.	TRDIOB1 TRDIOD1
TRDGRC1	BFC1 = 0	(These points are not used in reset synchronous PWM mode.)	–
TRDGRD1	BFD1 = 0		
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period. (Refer to **14.3.2 Buffer Operation.**)	(Output inversed every PWM period and TRDIOC0 pin)
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of the next PWM1 output. (Refer to **14.3.2 Buffer Operation**.)	TRDIOB0 TRDIOD0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of the next PWM2 output. (Refer to **14.3.2 Buffer Operation**.)	TRDIOA1 TRDIOC1
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of the next PWM3 output. (Refer to **14.3.2 Buffer Operation**.)	TRDIOB1 TRDIOD1

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

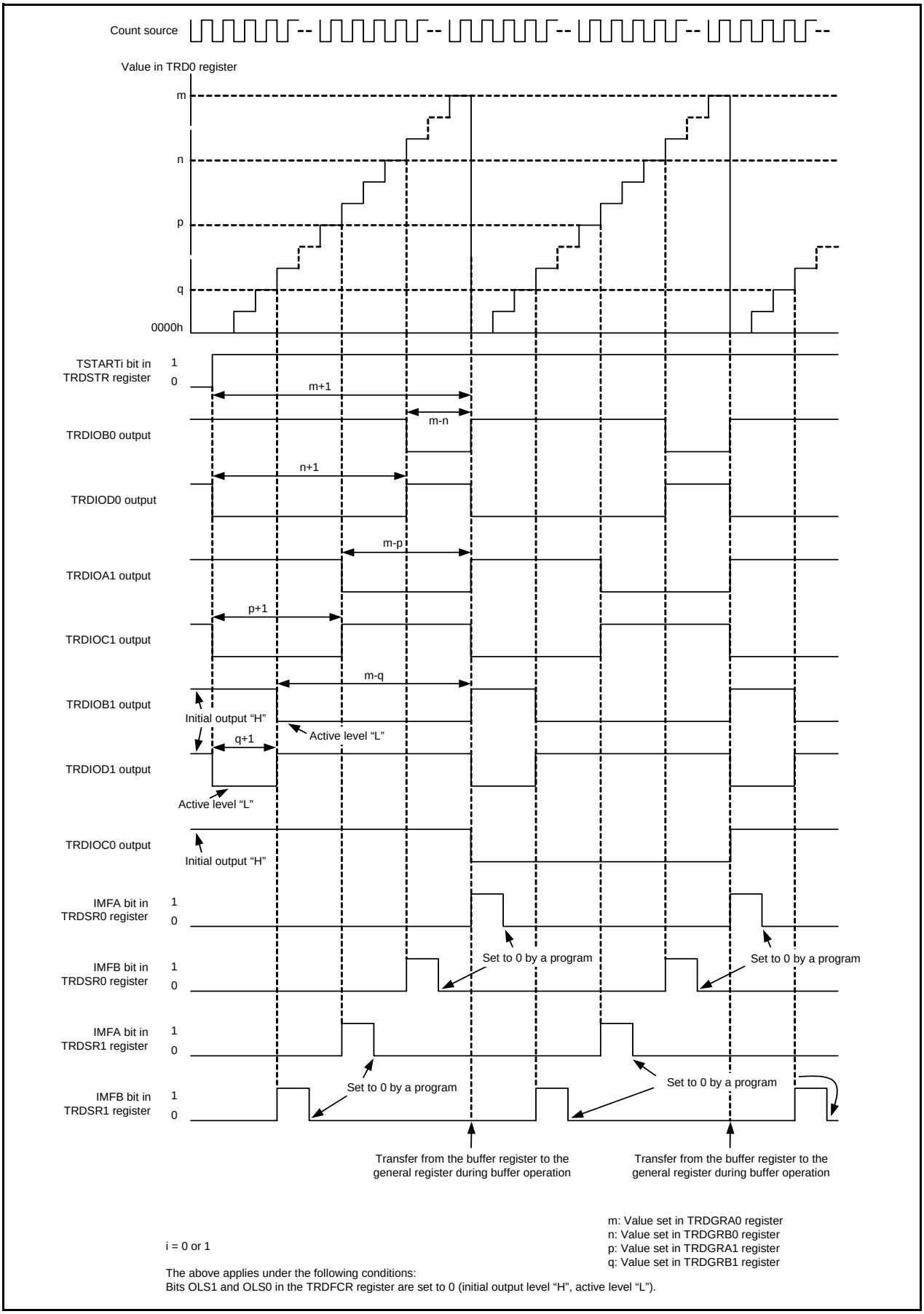


Figure 14.84 Operating Example of Reset Synchronous PWM Mode

14.3.9 Complementary PWM Mode

In this mode, 3 normal-phases and 3 counter-phases of the PWM waveform are output with the same period (three-phase, triangular wave modulation, and with dead time).
Figure 14.85 shows a Block Diagram of Complementary PWM Mode, and Table 14.31 lists the Complementary PWM Mode Specifications. Figures 14.86 to 14.94 show the Registers Associated with Complementary PWM Mode, Figure 14.95 shows the Output Model of Complementary PWM Mode, and Figure 14.96 shows an Operating Example of Complementary PWM Mode.

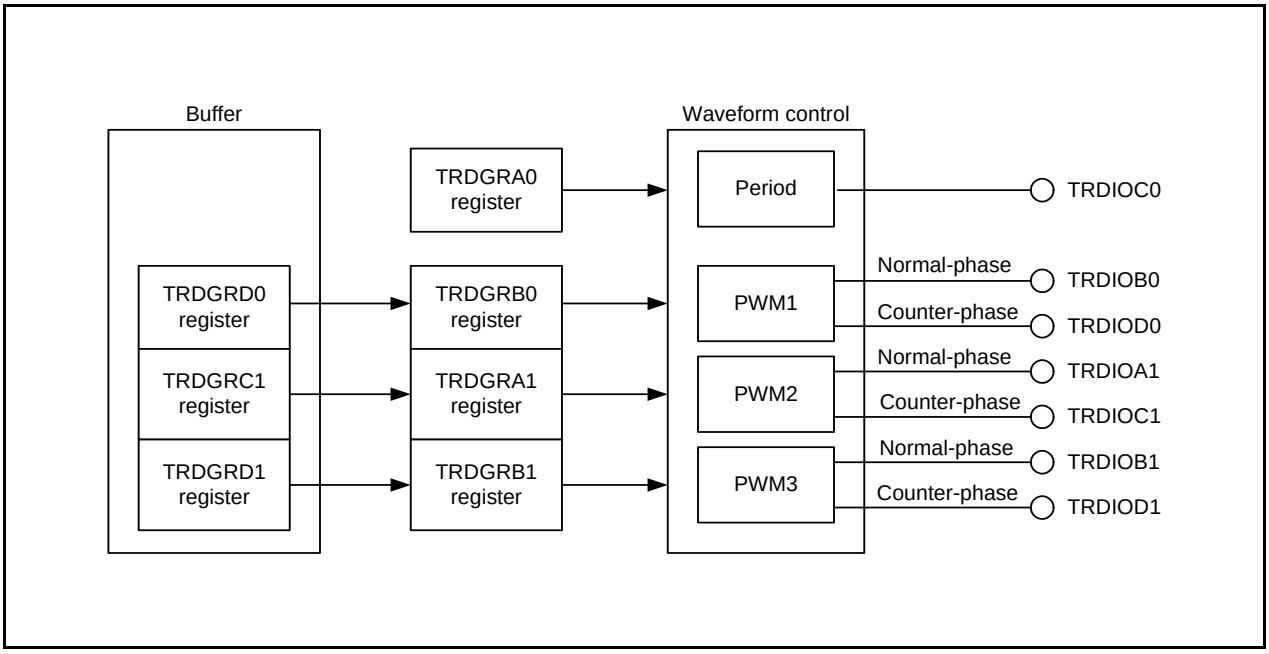
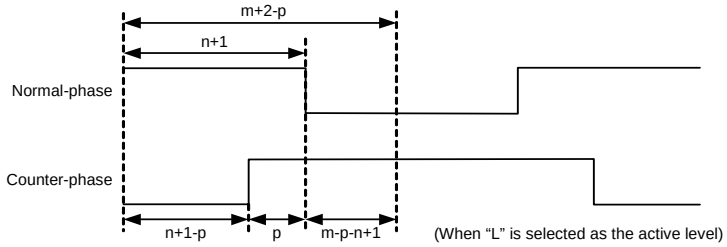


Figure 14.85 Block Diagram of Complementary PWM Mode

Table 14.31 Complementary PWM Mode Specifications

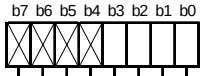
Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRDCLK pin (valid edge selected by a program) Set bits TCK2 to TCK0 in the TRDCR1 register to the same value (same count source) as bits TCK2 to TCK0 in the TRDCR0 register.
Count operations	Increment or decrement Registers TRD0 and TRD1 are decremented with the compare match in registers TRD0 and TRDGRA0 during increment operation. The TRD1 register value is changed from 0000h to FFFFh during decrement operation, and registers TRD0 and TRD1 are incremented.
PWM operations	PWM period: 1/fk × (m+2-p) × 2(1) Dead time: p Active level width of normal-phase: 1/fk × (m-n-p+1) × 2 Active level width of counter-phase: 1/fk × (n+1-p) × 2 fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output) Value set in the TRDGRA1 register (PWM2 output) Value set in the TRDGRB1 register (PWM3 output) p: Value set in the TRD0 register 
Count start condition	1 (count starts) is written to bits TSTART0 and TSTART1 in the TRDSTR register.
Count stop conditions	0 (count stops) is written to bits TSTART0 and TSTART1 in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin holds output level before the count stops.)
Interrupt request generation timing	• Compare match (The content of the TRDi register matches content of the TRDGRji register.) • The TRD1 register underflows
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOB0 pin function	PWM1 output normal-phase output
TRDIOD0 pin function	PWM1 output counter-phase output
TRDIOA1 pin function	PWM2 output normal-phase output
TRDIOC1 pin function	PWM2 output counter-phase output
TRDIOB1 pin function	PWM3 output normal-phase output
TRDIOD1 pin function	PWM3 output counter-phase output
TRDIOC0 pin function	Output inverted every 1/2 period of PWM
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	The value can be written to the TRDi register.
Select functions	• Pulse output forced cutoff signal input (Refer to **14.3.4 Pulse Output Forced Cutoff.**) • The active level of normal-phase and counter-phase and initial output level selected individually • Transfer timing from the buffer register selected • A/D trigger generated

i = 0 or 1, j = either A, B, C, or D

NOTE:

1. After a count starts, the PWM period is fixed.

Timer RD Start Register(1)



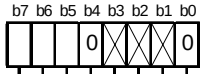
Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag(4)	0 : Count stops(2) 1 : Count starts	RW
TSTART1	TRD1 count start flag(5)	0 : Count stops(3) 1 : Count starts	RW
CSEL0	TRD0 count operation select bit	0 : Count stops at compare match with the TRDGRA0 register 1 : Count continues at compare match with the TRDGRA0 register	RW
CSEL1	TRD1 count operation select bit	0 : Count stops at compare match with the TRDGRA1 register 1 : Count continues at compare match with the TRDGRA1 register	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of **Notes on Timer RD**.
2. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
3. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
4. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
5. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Figure 14.86 TRDSTR Register in Complementary PWM Mode

Timer RD Mode Register

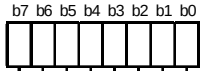


Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	Set this bit to 0 (registers TRD0 and TRD1 operate independently) in complementary PWM mode.	RW
— (b3-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function select bit	Set this bit to 0 (general register) in complementary PWM mode.	RW
BFD0	TRDGRD0 register function select bit	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function select bit	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function select bit	0 : General register 1 : Buffer register of TRDGRB1 register	RW

Figure 14.87 TRDMR Register in Complementary PWM Mode

Timer RD Function Control Register



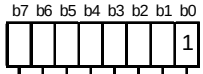
Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode select bits(1,2)	b1 b0 1 0 : Complementary PWM mode (transfer from the buffer register to the general register at the underflow in the TRD1 register) 1 1 : Complementary PWM mode (transfer from the buffer register to the general register at the compare match with registers TRD0 and TRDGRA0.) Other than above : Do not set.	RW
CMD1			RW
OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	0 : Initial output “H” Active level “L” 1 : Initial output “L” Active level “H”	RW
OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	0 : Initial output “H” Active level “L” 1 : Initial output “L” Active level “H”	RW
ADTRG	A/D trigger enable bit (in complementary PWM mode)	0 : Disable A/D trigger 1 : Enable A/D trigger(3)	RW
ADEG	A/D trigger edge select bit (in complementary PWM mode)	0 : A/D trigger is generated at compare match between registers TRD0 and TRDGRA0 1 : A/D trigger is generated at underflow in the TRD1 register	RW
STCLK	External clock input select bit	0 : External clock input disabled 1 : External clock input enabled	RW
PWM3	PWM3 mode select bit(4)	This bit is disabled in complementary PWM mode.	RW

NOTES:
1. When setting bits CMD1 to CMD0 to 10b or 11b, the MCU enters complementary PWM mode in spite of the setting of the TRDPMR register.
2. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits are set to 0 (count stops).
3. Set the ADCAP bit in the ADC0N0 register to 1 (starts by timer RD).
4. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.88 TRDFCR Register in Complementary PWM Mode

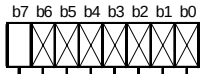
Timer RD Output Master Enable Register 1



Symbol	Address	After Reset
TRDOER1	013Bh	FFh

Bit Symbol	Bit Name	Function	RW
EA0	TRDIOA0 output disable bit	Set this bit to 1 (the TRDIOA0 pin is used as a programmable I/O port) in complementary PWM mode.	RW
EB0	TRDIOB0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	RW
EC0	TRDIOC0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC0 pin is used as a programmable I/O port.)	RW
ED0	TRDIOD0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD0 pin is used as a programmable I/O port.)	RW
EA1	TRDIOA1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOA1 pin is used as a programmable I/O port.)	RW
EB1	TRDIOB1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB1 pin is used as a programmable I/O port.)	RW
EC1	TRDIOC1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOC1 pin is used as a programmable I/O port.)	RW
ED1	TRDIOD1 output disable bit	0 : Enable output 1 : Disable output (The TRDIOD1 pin is used as a programmable I/O port.)	RW

Timer RD Output Master Enable Register 2



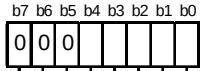
Symbol	Address	After Reset
TRDOER2	013Ch	01111111b

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit(1)	0 : Pulse output forced cutoff input disabled 1 : Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when “L” is applied to the $\overline{\text{INT0}}$ pin.)	RW

NOTE:
1. Refer to **14.3.4 Pulse Output Forced Cutoff.**

Figure 14.89 Registers TRDOER1 to TRDOER2 in Complementary PWM Mode

Timer RD Control Register i (i = 0 or 1)



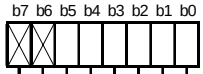
Symbol	Address	After Reset
TRDCR0	0140h	00h
TRDCR1	0150h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source select bits(2)	b2 b1 b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : TRDCLK input(1) 1 1 0 : fOCO40M 1 1 1 : Do not set.	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge select bits(2,3)	b4 b3 0 0 : Count at the rising edge 0 1 : Count at the falling edge 1 0 : Count at both edges 1 1 : Do not set.	RW
CKEG1			RW
CCLR0	TRDi counter clear select bits	Set to 000b (disable clearing (free-running operation)) in complementary PWM mode.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. This setting is enabled when the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. Set bits TCK2 to TCK0 and bits CKEG1 to CKEG0 in registers TRDCR0 and TRDCR1 to the same values.
3. Bits CKEG1 to CKEG0 are enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).

Figure 14.90 Registers TRDCR0 to TRDCR1 in Complementary PWM Mode

Timer RD Status Register i (i = 0 or 1)



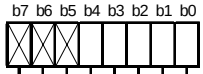
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register(3).	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register(3).	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the TRDi register overflows.	RW
UDF	Underflow flag(1)	[Source for setting this bit to 0] Write 0 after read(2). [Source for setting this bit to 1] When the TRD1 register underflows.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit (this bit remains 1 even if it is set to 1 from 0 after reading, and writing 0).
   - This bit remains unchanged if 1 is written to it.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

Figure 14.91 Registers TRDSR0 to TRDSR1 in Complementary PWM Mode

Timer RD Interrupt Enable Register i (i = 0 or 1)



Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable interrupt (IMIA) by the IMFA bit 1 : Enable interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable interrupt (IMIB) by the IMFB bit 1 : Enable interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable interrupt (IMIC) by the IMFC bit 1 : Enable interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable interrupt (IMID) by the IMFD bit 1 : Enable interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0 : Disable interrupt (OVI) by the OVF and UDF bits 1 : Enable interrupt (OVI) by the OVF and UDF bits	RW
— (b7-b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.92 Registers TRDIER0 to TRDIER1 in Complementary PWM Mode

Timer RD Counter 0(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRD0	0147h-0146h	0000h

Function	Setting Range	RW
Set the dead time. Count a count source. Count operation is incremented or decremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.

Timer RD Counter 1(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRD1	0157h-0156h	0000h

Function	Setting Range	RW
Select 0000h. Count a count source. Count operation is incremented or decremented. When an underflow occurs, the UDF bit in the TRDSR1 register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRD1 register in 16-bit units. Do not access it in 8-bit units.

Figure 14.93 Registers TRD0 to TRD1 in Complementary PWM Mode

Timer RD General Registers Ai, Bi, C1, and Di (i = 0 or 1)(1, 2)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.32 TRDGRji Register Functions in Complementary PWM Mode**.	RW

NOTES:
1. Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.
2. The TRDGRC0 register is not used in complementary PWM mode.

Figure 14.94 Registers TRDGRAi, TRDGRBi, TRDGRC1, and TRDGRDi in Complementary PWM Mode

The following registers are disabled in the complementary PWM mode: TRDPMR, TRDOCR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1.

Table 14.32 TRDGRji Register Functions in Complementary PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period at initialization. Setting range: Setting value or above in TRD0 register FFFFh - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	(Output inverted every half period of TRDIOC0 pin)
TRDGRB0	–	General register. Set the changing point of PWM1 output at initialization. Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOB0 TRDIOD0
TRDGRA1	–	General register. Set the changing point of PWM2 output at initialization. Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOA1 TRDIOC1
TRDGRB1	–	General register. Set the changing point of PWM3 output at initialization. Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOB1 TRDIOD1
TRDGRC0	–	This register is not used in complementary PWM mode.	–
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM1 output. (Refer to **14.3.2 Buffer Operation.**) Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRB0 register for initialization.	TRDIOB0 TRDIOD0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM2 output. (Refer to **14.3.2 Buffer Operation.**) Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRA1 register for initialization.	TRDIOA1 TRDIOC1
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM3 output. (Refer to **14.3.2 Buffer Operation.**) Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRB1 register for initialization.	TRDIOB1 TRDIOD1

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

Since values cannot be written to the TRDGRB0, TRDGRA1, or TRDGRB1 register directly after count operation starts (prohibited item), use the TRDGRD0, TRDGRC1, or TRDGRD1 register as a buffer register. However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).

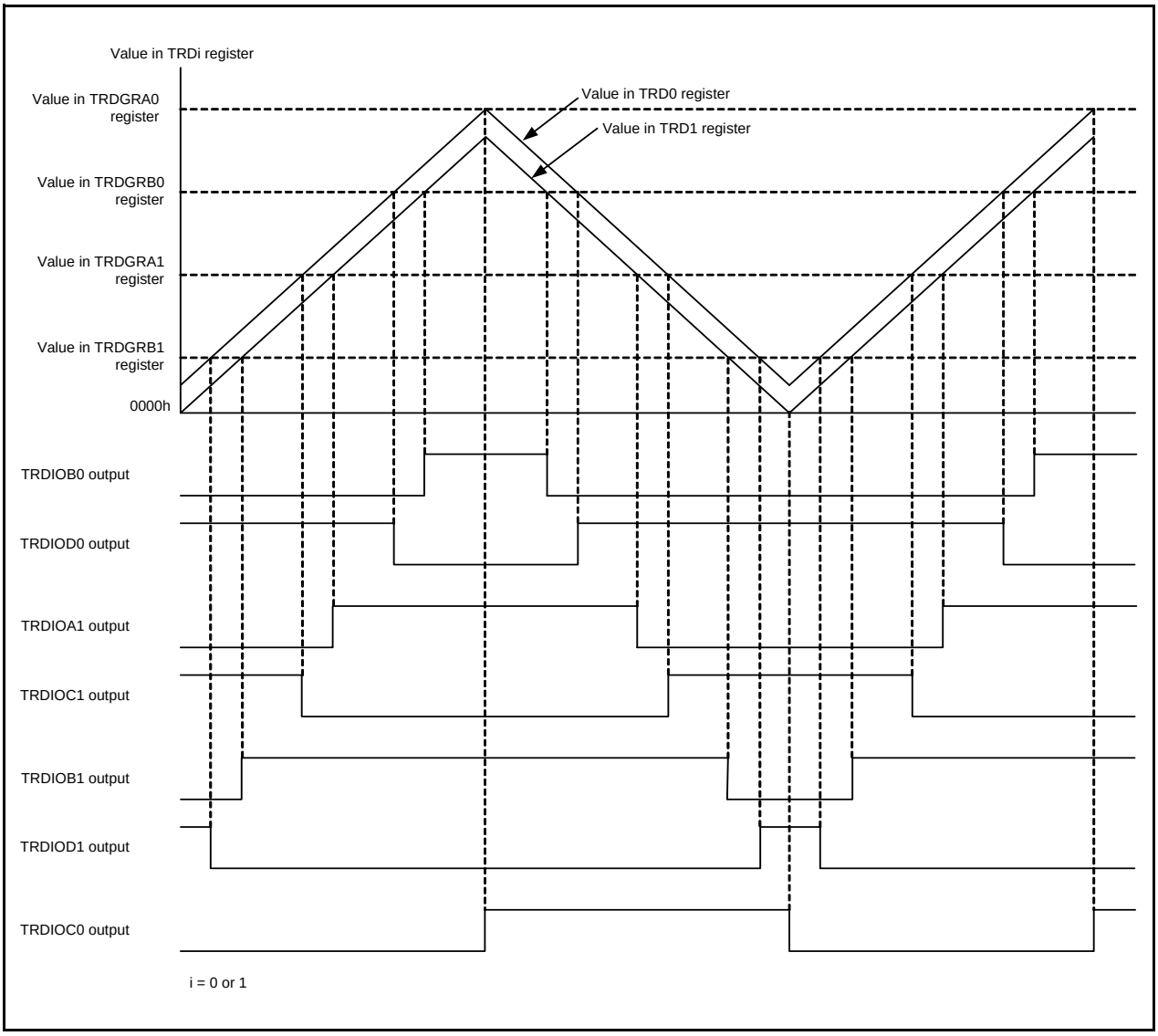


Figure 14.95 Output Model of Complementary PWM Mode

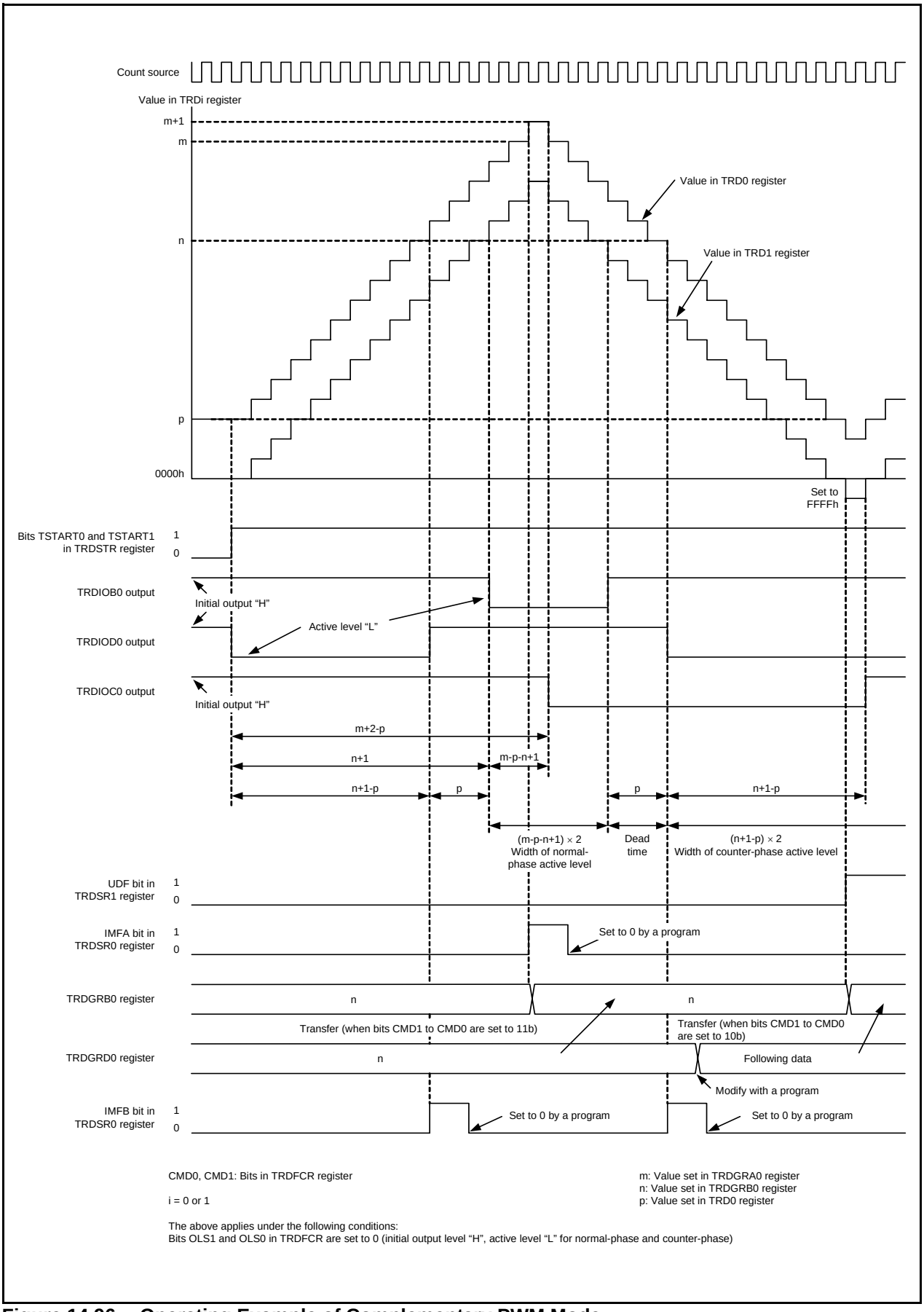


Figure 14.96 Operating Example of Complementary PWM Mode

14.3.9.1 Transfer Timing from Buffer Register

- Transfer from the TRDGRD0, TRDGRC1, or TRDGRD1 register to the TRDGRB0, TRDGRA1, or TRDGRB1 register.
  When bits CMD1 to CMD0 in the TRDFCR register are set to 10b, the content is transferred when the TRD1 register underflows.
  When bits CMD1 to CMD0 are set to 11b, the content is transferred at compare match between registers TRD0 and TRDGRA0.

14.3.9.2 A/D Trigger Generation

Compare match between registers TRD0 and TRDGRA0 and TRD1 underflow can be used as the conversion start trigger of the A/D converter. The trigger is selected by bits ADEG and ADTRG in the TRDFCR register. Also, set the ADCAP bit in the ADCON0 register to 1 (starts by timer RD).

14.3.10 PWM3 Mode

In this mode, 2 PWM waveforms are output with the same period.
Figure 14.97 shows a Block Diagram of PWM3 Mode, and Table 14.33 lists the PWM3 Mode Specifications. Figures 14.98 to 14.106 show the Registers Associated with PWM3 Mode, and Figure 14.107 shows an Operating Example of PWM3 Mode.

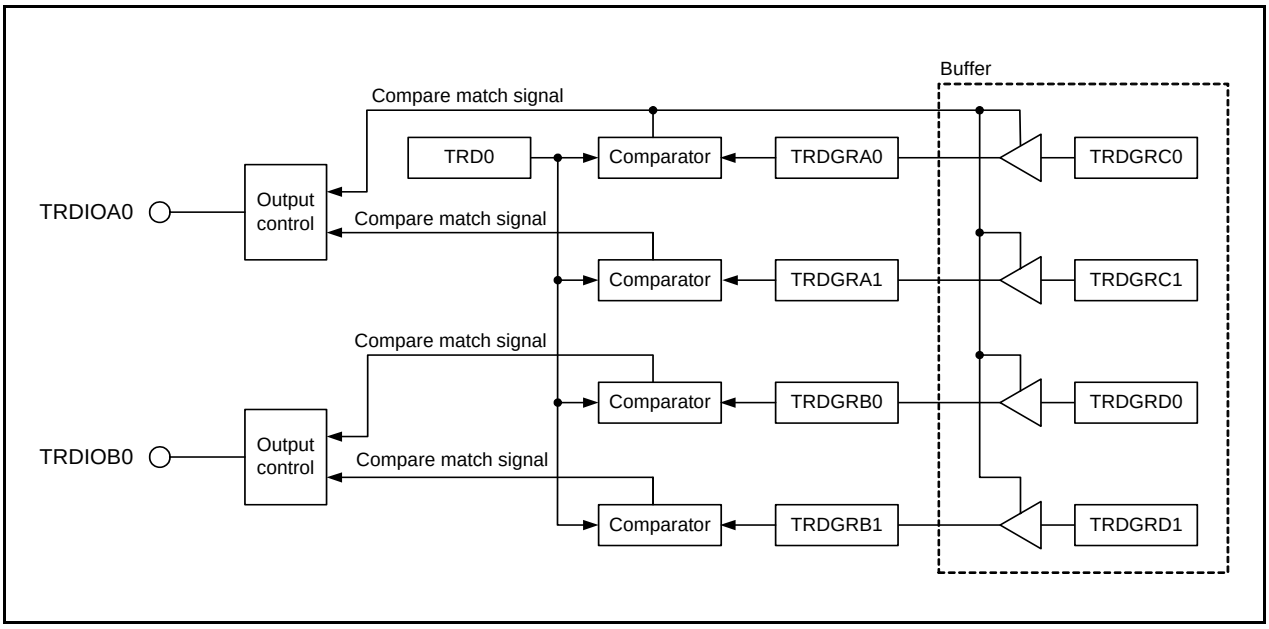
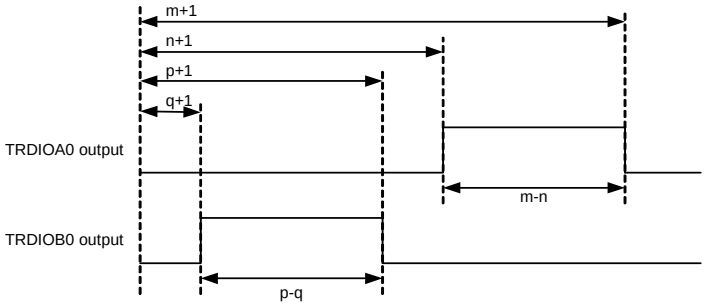


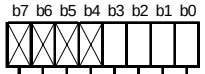
Figure 14.97 Block Diagram of PWM3 Mode

Table 14.33 PWM3 Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M
Count operations	The TRD0 register is incremented (the TRD1 is not used).
PWM waveform	PWM period: 1/fk × (m+1) Active level width of TRDIOA0 output: 1/fk × (m-n) Active level width of TRDIOB0 output: 1/fk × (p-q) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRA1 register p: Value set in the TRDGRB0 register q: Value set in the TRDGRB1 register  (When “H” is selected as the active level)
Count start condition	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the compare match with the TRDGRA0 register. The PWM output pin holds level after output change by compare match.
Interrupt request generation timing	• Compare match (The content of the TRDi register matches content of the TRDGRji register.) • The TRD0 register overflows
TRDIOA0, TRDIOB0 pin functions	PWM output
TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin functions	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRD0 register.
Write to timer	The value can be written to the TRD0 register.
Select functions	• Pulse output forced cutoff signal input (Refer to **14.3.4 Pulse Output Forced Cutoff.**) • Buffer Operation (Refer to **14.3.2 Buffer Operation.**) • Active level selectable by pin

i = 0 or 1, j = either A, B, C, or D

Timer RD Start Register(1)

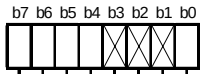


Symbol	Address	After Reset
TRDSTR	0137h	11111100b

Bit Symbol	Bit Name	Function	RW
TSTART0	TRD0 count start flag(4)	0 : Count stops(2) 1 : Count starts	RW
TSTART1	TRD1 count start flag(5)	0 : Count stops(3) 1 : Count starts	RW
CSEL0	TRD0 count operation select bit	0 : Count stops at compare match with the TRDGRA0 register 1 : Count continues at compare match with the TRDGRA0 register	RW
CSEL1	TRD1 count operation select bit [this bit is not used in PWM3 mode]	0 : Count stops at compare match with the TRDGRA1 register 1 : Count continues at compare match with the TRDGRA1 register	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **14.3.12.1 TRDSTR Register** of **Notes on Timer RD**.
2. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
3. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
4. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
5. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Timer RD Mode Register



Symbol	Address	After Reset
TRDMR	0138h	00001110b

Bit Symbol	Bit Name	Function	RW
SYNC	Timer RD synchronous bit	Set this bit to 0 (TRD0 and TRD1 operate independently) in PWM3 mode.	RW
— (b3-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
BFC0	TRDGRC0 register function select bit	0 : General register 1 : Buffer register of TRDGRA0 register	RW
BFD0	TRDGRD0 register function select bit	0 : General register 1 : Buffer register of TRDGRB0 register	RW
BFC1	TRDGRC1 register function select bit	0 : General register 1 : Buffer register of TRDGRA1 register	RW
BFD1	TRDGRD1 register function select bit	0 : General register 1 : Buffer register of TRDGRB1 register	RW

Figure 14.98 Registers TRDSTR and TRDMR in PWM3 Mode

Timer RD Function Control Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0					0	0

Symbol	Address	After Reset
TRDFCR	013Ah	10000000b

Bit Symbol	Bit Name	Function	RW
CMD0	Combination mode select bits(1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in PWM3 mode.	RW
CMD1			RW
OLS0	Normal-phase output level select bit (enabled in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
OLS1	Counter-phase output level select bit (enabled in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
ADTRG	A/D trigger enable bit (enabled in complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
ADEG	A/D trigger edge select bit (enabled in complementary PWM mode)	This bit is disabled in PWM3 mode.	RW
STCLK	External clock input select bit	Set this bit to 0 (external clock input disabled) in PWM3 mode.	RW
PWM3	PWM3 mode select bit(2)	Set this bit to 0 (PWM3 mode) in PWM3 mode.	RW

NOTES:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

Figure 14.99 TRDFCR Register in PWM3 Mode

Timer RD Output Master Enable Register 1

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	1	1		

Symbol	Address	After Reset
TRDOER1	013Bh	FFh

Bit Symbol	Bit Name	Function	RW
EA0	TRDIOA0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOA0 pin is used as a programmable I/O port.)	RW
EB0	TRDIOB0 output disable bit	0 : Enable output 1 : Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	RW
EC0	TRDIOC0 output disable bit	Set these bits to 1 (programmable I/O port) in PWM3 mode.	RW
ED0	TRDIOD0 output disable bit		RW
EA1	TRDIOA1 output disable bit		RW
EB1	TRDIOB1 output disable bit		RW
EC1	TRDIOC1 output disable bit		RW
ED1	TRDIOD1 output disable bit		RW

Timer RD Output Master Enable Register 2

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
TRDOER2	013Ch	01111111b

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PTO	$\overline{INT0}$ of pulse output forced cutoff signal input enabled bit(1)	0 : Pulse output forced cutoff input disabled 1 : Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when "L" is applied to the $\overline{INT0}$ pin.)	RW

NOTE:
1. Refer to **14.3.4 Pulse Output Forced Cutoff.**

Figure 14.100 Registers TRDOER1 to TRDOER2 in PWM3 Mode

Timer RD Output Control Register(1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRDOCR	013Dh	00h

Bit Symbol	Bit Name	Function	RW
TOA0	TRDIOA0 output level select bit(2)	0 : Active level “H”, initial output “L”, output “H” at compare match with the TRDGRA1register, output “L” at compare match with the TRDGRA0 register 1 : Active level “L”, initial output “H”, output “L” at compare match with the TRDGRA1register, output “H” at compare match with the TRDGRA0 register	RW
TOB0	TRDIOB0 output level select bit(2)	0 : Active level “H”, initial output “L”, output “H” at compare match with the TRDGRB1register, output “L” at compare match with the TRDGRB0 register 1 : Active level “L”, initial output “H”, output “L” at compare match with the TRDGRB1register, output “H” at compare match with the TRDGRB0 register	RW
TOC0	TRDIOC0 initial output level select bit	These bits are disabled in PWM3 mode.	RW
TOD0	TRDIOD0 initial output level select bit		RW
TOA1	TRDIOA1 initial output level select bit		RW
TOB1	TRDIOB1 initial output level select bit		RW
TOC1	TRDIOC1 initial output level select bit		RW
TOD1	TRDIOD1 initial output level select bit		RW

NOTES:
1. Write to the TRDOCR register when both bits TSTART0 and TSTART1 in the TRDSTR register are set to 0 (count
2. If the pin function is set for waveform output (refer to **Tables 14.12** and **14.13**), the initial output level is output when the TRDOCR register is set.

Figure 14.101 TRDOCR Register in PWM3 Mode

Timer RD Control Register 0(2)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1					

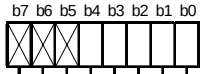
Symbol	Address	After Reset
TRDCR0	0140h	00h

Bit Symbol	Bit Name	Function	RW
TCK0	Count source select bits	b2 b1b0 0 0 0 : f1 0 0 1 : f2 0 1 0 : f4 0 1 1 : f8 1 0 0 : f32 1 0 1 : Do not set. 1 1 0 : fOCO40M 1 1 1 : Do not set.	RW
TCK1			RW
TCK2			RW
CKEG0	External clock edge select bits(1)	These bits are disabled in PWM3 mode.	RW
CKEG1			RW
CCLR0	TRD0 counter clear select bits	Set to 001b (the TRD0 register cleared at compare match with TRDGRA0 register) in PWM3 mode.	RW
CCLR1			RW
CCLR2			RW

NOTES:
1. Bits CKEG1 to CKEG0 are enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
2. The TRDCR1 register is not used in PWM3 mode.

Figure 14.102 TRDCR0 Register in PWM3 Mode

Timer RD Status Register i (i = 0 or 1)



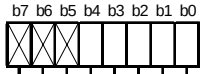
Symbol	Address	After Reset
TRDSR0	0143h	11100000b
TRDSR1	0153h	11000000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	RW
IMFB	Input capture/compare match flag B	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	RW
IMFC	Input capture/compare match flag C	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register(2).	RW
IMFD	Input capture/compare match flag D	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register(2).	RW
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] When the TRDi register overflows.	RW
UDF	Underflow flag(1)	This bit is disabled in PWM3 mode.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit (this bit remains 1 even if it is set to 1 from 0 after reading, and writing 0).
   - This bit remains unchanged if 1 is written to it.
2. Including when the BFji (j = C or D) bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

Figure 14.103 Registers TRDSR0 to TRDSR1 in PWM3 Mode

Timer RD Interrupt Enable Register i (i = 0 or 1)

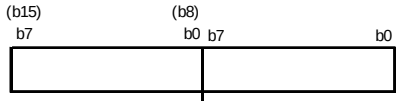


Symbol	Address	After Reset
TRDIER0	0144h	11100000b
TRDIER1	0154h	11100000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0 : Disable interrupt (IMIA) by the IMFA bit 1 : Enable interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0 : Disable interrupt (IMIB) by the IMFB bit 1 : Enable interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0 : Disable interrupt (IMIC) by the IMFC bit 1 : Enable interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0 : Disable interrupt (IMID) by the IMFD bit 1 : Enable interrupt (IMID) by the IMFD bit	RW
OVIE	Overflow /underflow interrupt enable bit	0 : Disable interrupt (OVI) by the OVF bit 1 : Enable interrupt (OVI) by the OVF bit	RW
— (b7-b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Figure 14.104 Registers TRDIER0 to TRDIER1 in PWM3 Mode

Timer RD Counter 0(1, 2)



Symbol	Address	After Reset
TRD0	0147h-0146h	0000h

Function	Setting Range	RW
Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	RW

NOTES:
1. Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.
2. The TRD1 register is not used in PWM3 mode.

Figure 14.105 TRD0 Register in PWM3 Mode

Timer RD General Registers Ai, Bi, Ci, and Di (i = 0 or 1)(1)

(b15) (b8) (b7) (b0)

Symbol	Address	After Reset
TRDGRA0	0149h-0148h	FFFFh
TRDGRB0	014Bh-014Ah	FFFFh
TRDGRC0	014Dh-014Ch	FFFFh
TRDGRD0	014Fh-014Eh	FFFFh
TRDGRA1	0159h-0158h	FFFFh
TRDGRB1	015Bh-015Ah	FFFFh
TRDGRC1	015Dh-015Ch	FFFFh
TRDGRD1	015Fh-015Eh	FFFFh

Function	RW
Refer to **Table 14.34 TRDGRji Register Functions in PWM3 Mode.**	RW

NOTE:
1. Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

Figure 14.106 Registers TRDGRAi, TRDGRBi, TRDGRCi, and TRDGRDi in PWM3 Mode

The following registers are disabled in the PWM3 mode function: TRDPMR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1.

Table 14.34 TRDGRji Register Functions in PWM3 Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period. Setting range: Value set in TRDGRA1 register or above	TRDIOA0
TRDGRA1		General register. Set the changing point (the active level timing) of PWM output. Setting range: Value set in TRDGRA0 register or below	
TRDGRB0		General register. Set the changing point (the timing that returns to initial output level) of PWM output. Setting range: Value set in TRDGRB1 register or above Value set in TRDGRA0 register or below	TRDIOB0
TRDGRB1		General register. Set the changing point (active level timing) of PWM output. Setting range: Value set in TRDGRB0 register or below	
TRDGRC0	BFC0 = 0	(These registers is not used in PWM3 mode.)	–
TRDGRC1	BFC1 = 0		
TRDGRD0	BFD0 = 0		
TRDGRD1	BFD1 = 0		
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period. (Refer to **14.3.2 Buffer Operation**.) Setting range: Value set in TRDGRC1 register or above	TRDIOA0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **14.3.2 Buffer Operation**.) Setting range: Value set in TRDGRC0 register or below	
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **14.3.2 Buffer Operation**.) Setting range: Value set in TRDGRD1 register or above, setting value or below in TRDGRC0 register.	TRDIOB0
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **14.3.2 Buffer Operation**.) Setting range: Value set in TRDGRD0 register or below	

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

Registers TRDGRC0, TRDGRC1, TRDGRD0, and TRDGRD1 are not used in PWM3 mode. To use them as buffer registers, set bits BFC0, BFC1, BFD0, and BFD1 to 0 (general register) and write a value to the TRDGRC0, TRDGRC1, TRDGRD0, or TRDGRD1 register. After this, bits BFC0, BFC1, BFD0, and BFD1 may be set to 1 (buffer register).

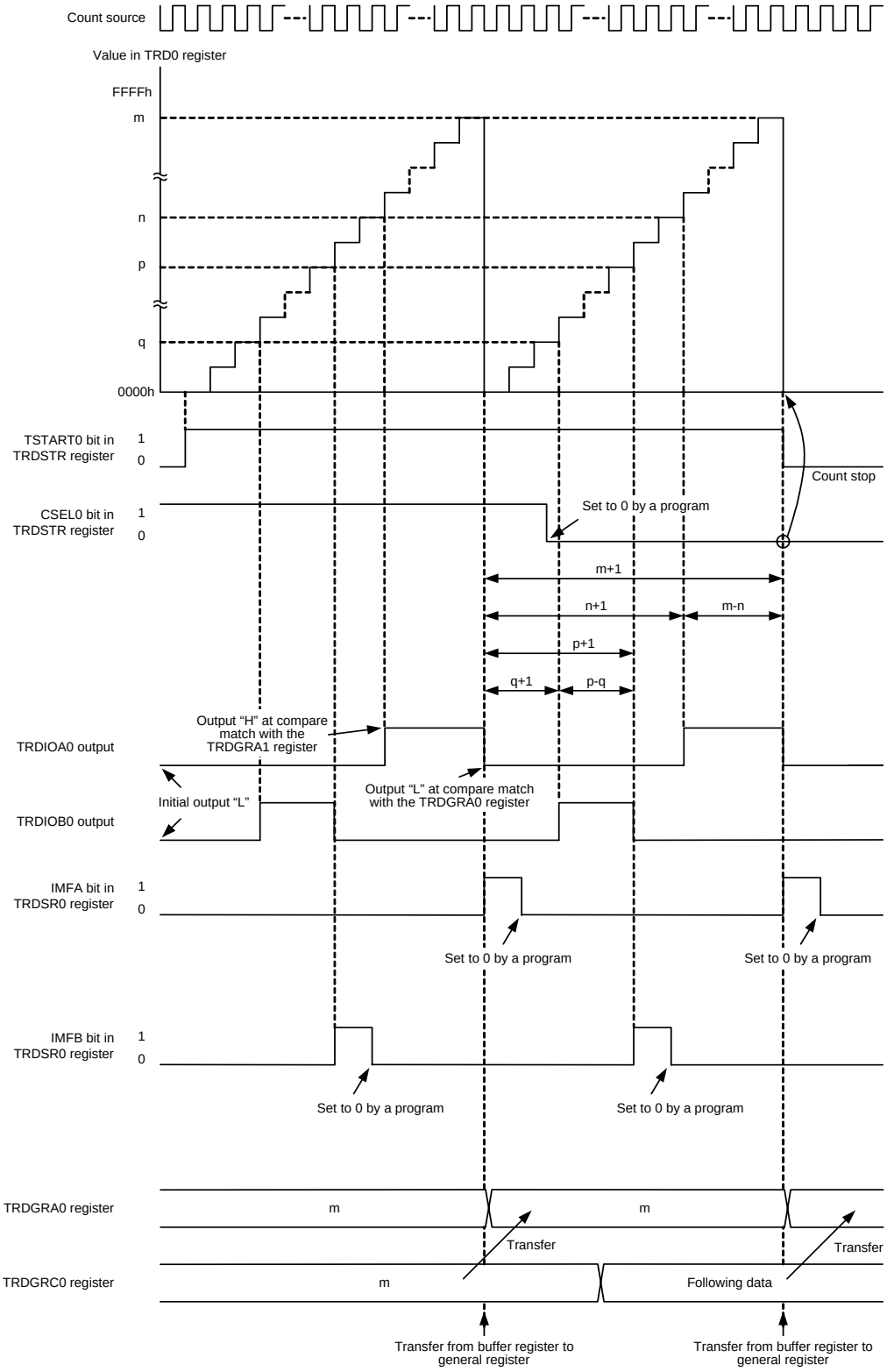


Figure 14.107 Operating Example of PWM3 Mode

14.3.11 Timer RD Interrupt

Timer RD generates the timer RD interrupt request based on 6 sources for each channel. The timer RD interrupt has 1 TRDiIC register (bits IR, and ILVL0 to ILVL2), and 1 vector for each channel.
Table 14.35 lists the Registers Associated with Timer RD Interrupt, and Figure 14.108 shows a Block Diagram of Timer RD Interrupt.

Table 14.35 Registers Associated with Timer RD Interrupt

	Timer RD Status Register	Timer RD Interrupt Enable Register	Timer RD Interrupt Control Register
Channel 0	TRDSR0	TRDIER0	TRD0IC
Channel 1	TRDSR1	TRDIER1	TRD1IC

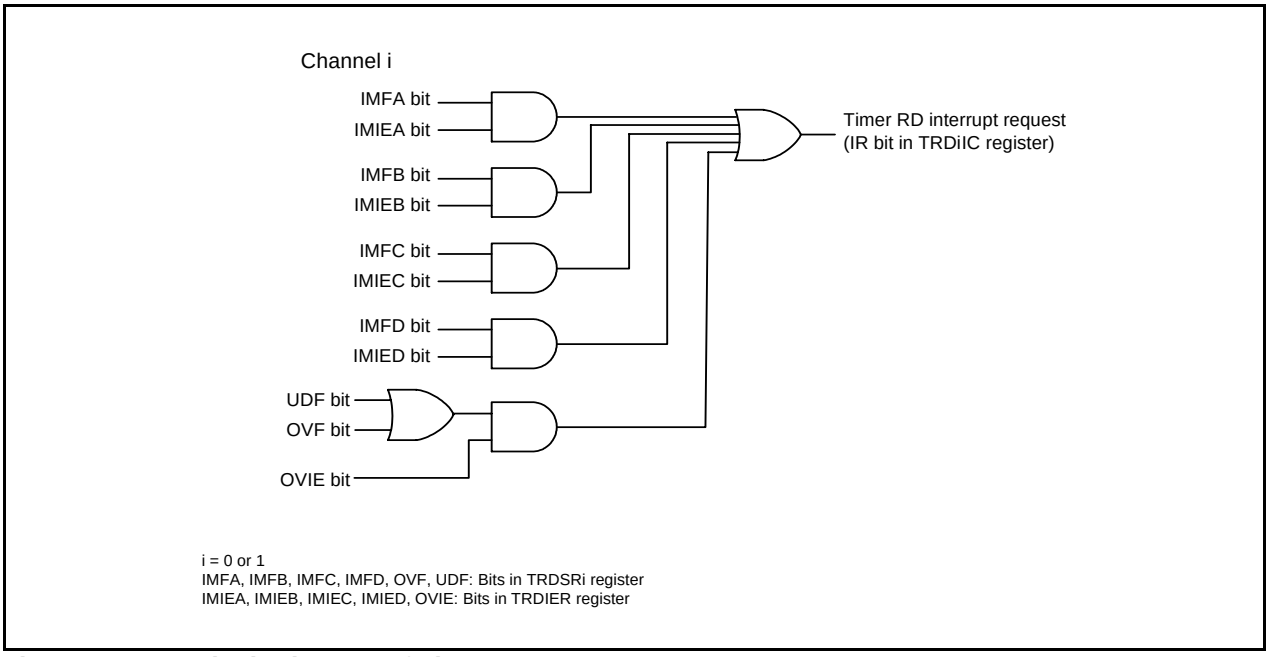


Figure 14.108 Block Diagram of Timer RD Interrupt

As with other maskable interrupts, the timer RD interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since the interrupt source (timer RD interrupt) is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the TRDSRi register corresponding to bits set to 1 in the TRDIERi register are set to 1 (enable interrupt), the IR bit in the TRDiIC register is set to 1 (interrupt requested).
- When either bits in the TRDSRi register or bits in the TRDIERi register corresponding to bits in the TRDSRi register, or both of them, are set to 0, the IR bit is set to 0 (interrupt not requested). Therefore, even though the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be maintained.
- When the conditions of other request sources are met, the IR bit remains 1.
- When multiple bits in the TRDIERi register are set to 1, which request source causes an interrupt is determined by the TRDSRi register.
- Since each bit in the TRDSRi register is not automatically set to 0 even if the interrupt is acknowledged, set each bit to 0 in the interrupt routine. For information on how to set these bits to 0, refer to the descriptions of the registers used in the different modes (**Figures 14.40, 14.55, 14.68, 14.80, 14.91, and 14.103**).

Refer to **Registers TRDSR0 to TRDSR1 in each mode (Figures 14.40, 14.55, 14.68, 14.80, 14.91, and 14.103)** for the TRDSRi register. Refer to **Registers TRDIER0 to TRDIER1 in each mode (Figures 14.41, 14.56, 14.69, 14.81, 14.92, and 14.104)** for the TRDIERi register.
Refer to **12.1.6 Interrupt Control** for information on the TRDiIC register and **12.1.5.2 Relocatable Vector Tables** for the interrupt vectors.

14.3.12 Notes on Timer RD

14.3.12.1 TRDSTR Register

- Set the TRDSTR register using the MOV instruction.

- When the CSELi (i = 0 to 1) is set to 0 (the count stops at compare match of registers TRDi and TRDGRAi), the count does not stop and the TSTARTi bit remains unchanged even if 0 (count stops) is written to the TSTARTi bit.
- Therefore, set the TSTARTi bit to 0 to change other bits without changing the TSTARTi bit when the CSELi bit is se to 0.
- To stop counting by a program, set the TSTARTi bit after setting the CSELi bit to 1. Although the CSELi bit is set to 1 and the TSTARTi bit is set to 0 at the same time (with 1 instruction), the count cannot be stopped.
- Table 14.36 lists the TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops to use the TRDIOji (j = A, B, C, or D) pin with the timer RD output.

Table 14.36 TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops

Count Stop	TRDIOji Pin Output when Count Stops
When the CSELi bit is set to 1, set the TSTARTi bit to 0 and the count stops.	Hold the output level immediately before the count stops.
When the CSELi bit is set to 0, the count stops at compare match of registers TRDi and TRDGRAi.	Hold the output level after output changes by compare match.

14.3.12.2 TRDi Register (i = 0 or 1)

- When writing the value to the TRDi register by a program while the TSTARTi bit in the TRDSTR register is set to 1 (count starts), avoid overlapping with the timing for setting the TRDi register to 0000h, and then write. If the timing for setting the TRDi register to 0000h overlaps with the timing for writing the value to the TRDi register, the value is not written and the TRDi register is set to 0000h.
  These precautions are applicable when selecting the following by bits CCLR2 to CCLR0 in the TRDCRi register.
  - 001b (Clear by the TRDi register at compare match with the TRDGRAi register.)
  - 010b (Clear by the TRDi register at compare match with the TRDGRBi register.)
  - 011b (Synchronous clear)
  - 101b (Clear by the TRDi register at compare match with the TRDGRCi register.)
  - 110b (Clear by the TRDi register at compare match with the TRDGRDi register.)

- When writing the value to the TRDi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.W   #XXXXh, TRD0     ;Writing
                    JMP.B   L1               ;JMP.B
                L1: MOV.W   TRD0,DATA        ;Reading
```

14.3.12.3 TRDSRi Register (i = 0 or 1)

When writing the value to the TRDSRi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.B   #XXh, TRDSR0     ;Writing
                    JMP.B   L1               ;JMP.B
                L1: MOV.B   TRDSR0,DATA      ;Reading
```

14.3.12.4 Count Source Switch

- Switch the count source after the count stops.

Change procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.

- When changing the count source from fOCO40M to another source and stopping fOCO40M, wait 2 cycles of f1 or more after setting the clock switch, and then stop fOCO40M.

Change procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.
(3) Wait 2 or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator stops).

14.3.12.5 Input Capture Function

- Set the pulse width of the input capture signal to 3 or more cycles of the timer RD operation clock (refer to **Table 14.11 Timer RD Operation Clocks**).
- The value in the TRDi register is transferred to the TRDGRji register 2 to 3 cycles of the timer RD operation clock after the input capture signal is applied to the TRDIOji pin (i = 0 or 1, j = either A, B, C, or D) (no digital filter).

14.3.12.6 Reset Synchronous PWM Mode

- When reset synchronous PWM mode is used for motor control, make sure OLS0 = OLS1.
- Set to reset synchronous PWM mode by the following procedure:

Change procedure

(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 01b (reset synchronous PWM mode).
(4) Set the other registers associated with timer RD again.

14.3.12.7 Complementary PWM Mode

- When complementary PWM mode is used for motor control, make sure OLS0 = OLS1.
- Change bits CMD1 to CMD0 in the TRDFCR register in the following procedure.

Change procedure: When setting to complementary PWM mode (including re-set), or changing the transfer timing from the buffer register to the general register in complementary PWM mode.

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 10b or 11b (complementary PWM mode).
(4) Set the registers associated with other timer RD again.

Change procedure: When stopping complementary PWM mode

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD to 00b (timer mode, PWM mode, and PWM3 mode).

- Do not write to TRDGRA0, TRDGRB0, TRDGRA1, or TRDGRB1 register during operation.
  When changing the PWM waveform, transfer the values written to registers TRDGRD0, TRDGRC1, and TRDGRD1 to registers TRDGRB0, TRDGRA1, and TRDGRB1 using the buffer operation.
  However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).
  The PWM period cannot be changed.

- If the value in the TRDGRA0 register is assumed to be m, the TRD0 register counts m-1, m, m+1, m, m-1, in that order, when changing from increment to decrement operation.
  When changing from m to m+1, the IMFA bit is set to 1. Also, bits CMD1 to CMD0 in the TRDFCR register are set to 11b (complementary PWM mode, buffer data transferred at compare match between registers TRD0 and TRDGRA0), the content in the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1).
  During m+1, m, and m-1 operation, the IMFA bit remains unchanged and data are not transferred to registers such as the TRDGRA0 register.

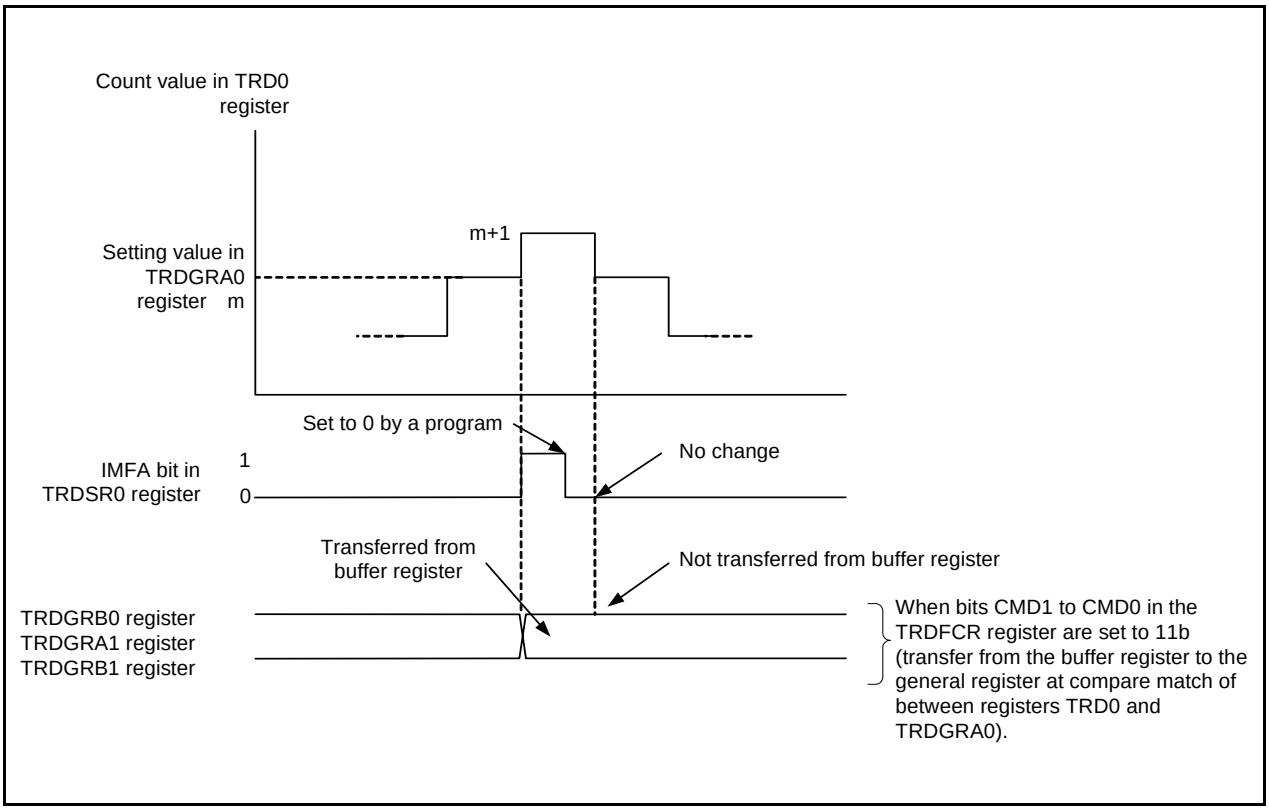


Figure 14.109 Operation at Compare Match between Registers TRD0 and TRDGRA0 in Complementary PWM Mode

- The TRD1 register counts 1, 0, FFFFh, 0, 1, in that order, when changing from decrement to increment operation.
  The UDF bit is set to 1 when changing between 1, 0, and FFFFh operation. Also, when bits CMD1 to CMD0 in the TRDFCR register are set to 10b (complementary PWM mode, buffer data transferred at underflow in the TRD1 register), the content in the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1). During FFFFh, 0, 1 operation, data are not transferred to registers such as the TRDGRB0 register. Also, at this time, the OVF bit remains unchanged.

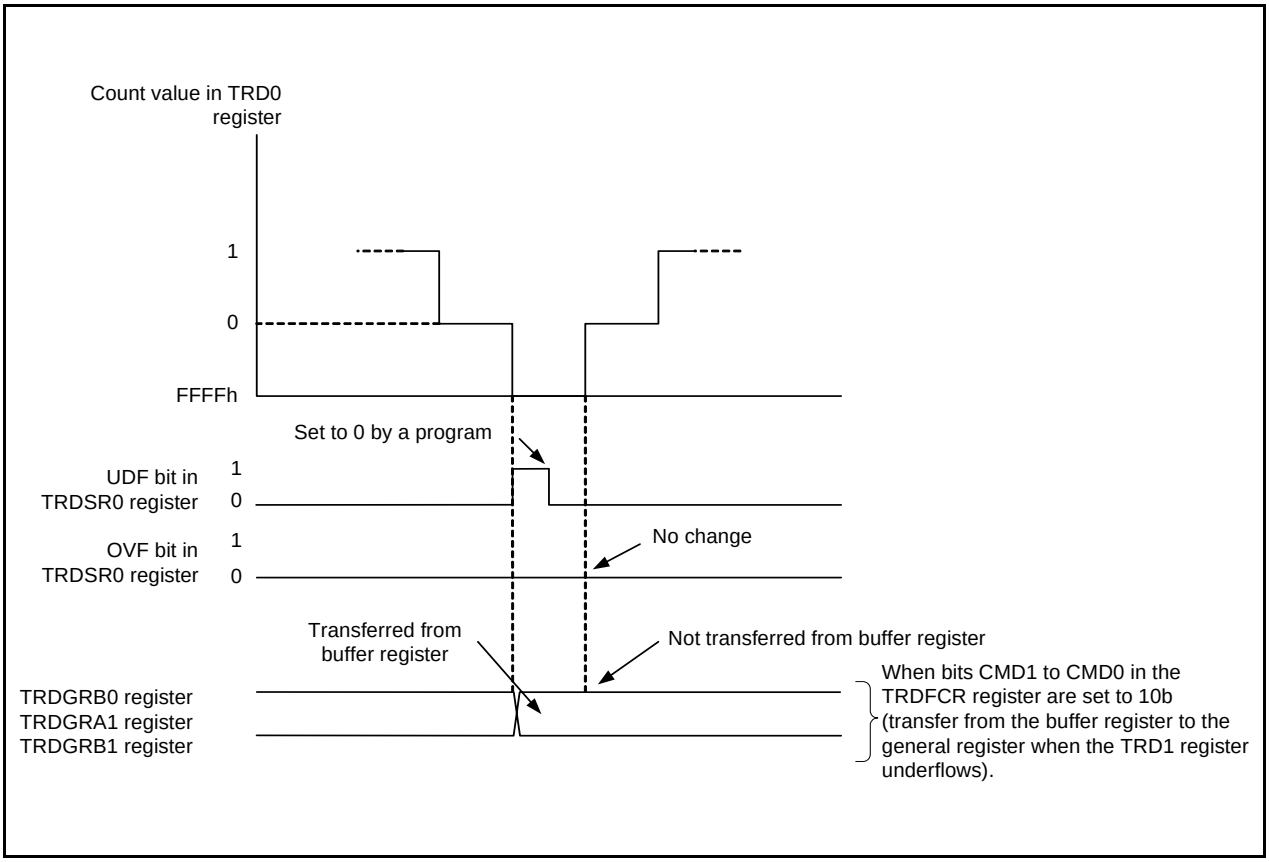
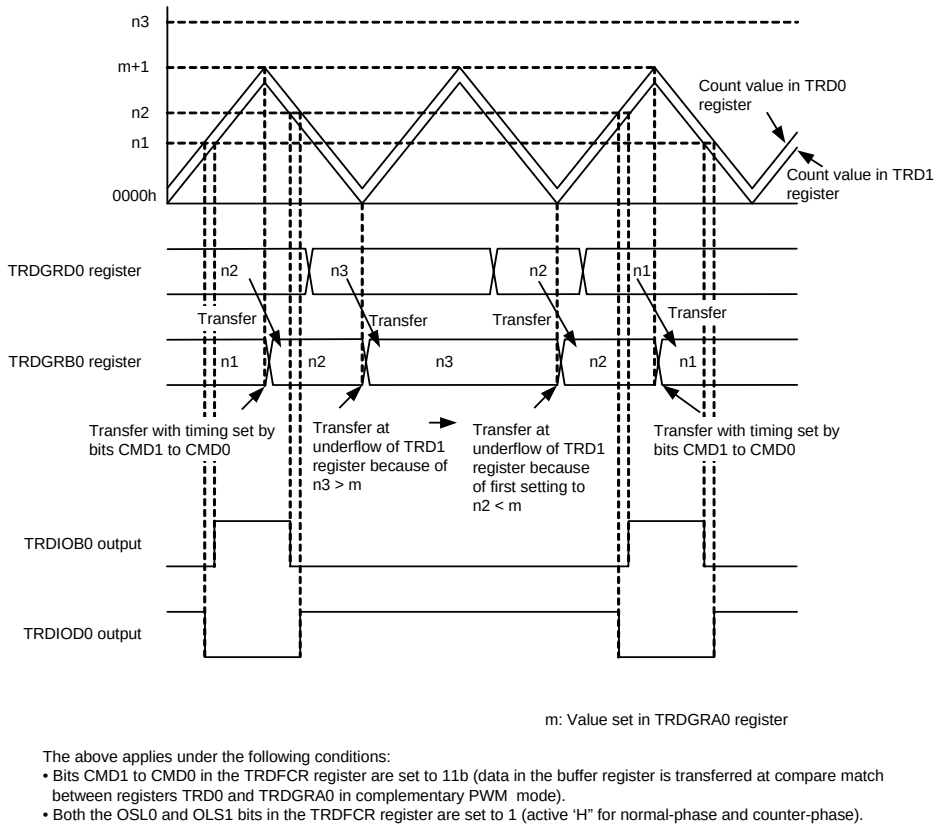


Figure 14.110 Operation when TRD1 Register Underflows in Complementary PWM Mode

- Select with bits CMD1 to CMD0 the timing of data transfer from the buffer register to the general register. However, transfer takes place with the following timing in spite of the value of bits CMD1 to CMD0 in the following cases:

  Value in buffer register ≥ value in TRDGRA0 register:
  Transfer take place at underflow of the TRD1 register.
  After this, when the buffer register is set to 0001h or above and a smaller value than the value of the TRDGRA0 register, and the TRD1 register underflows for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 to CMD0.



The above applies under the following conditions:
- Bits CMD1 to CMD0 in the TRDFCR register are set to 11b (data in the buffer register is transferred at compare match between registers TRD0 and TRDGRA0 in complementary PWM mode).
- Both the OSL0 and OLS1 bits in the TRDFCR register are set to 1 (active 'H" for normal-phase and counter-phase).

Figure 14.111 Operation when Value in Buffer Register ≥ Value in TRDGRA0 Register in Complementary PWM Mode

When the value in the buffer register is set to 0000h:
Transfer takes place at compare match between registers TRD0 and TRDGRA0.
After this, when the buffer register is set to 0001h or above and a smaller value than the value of the TRDGRA0 register, and a compare match occurs between registers TRD0 and TRDGRA0 for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 to CMD0.

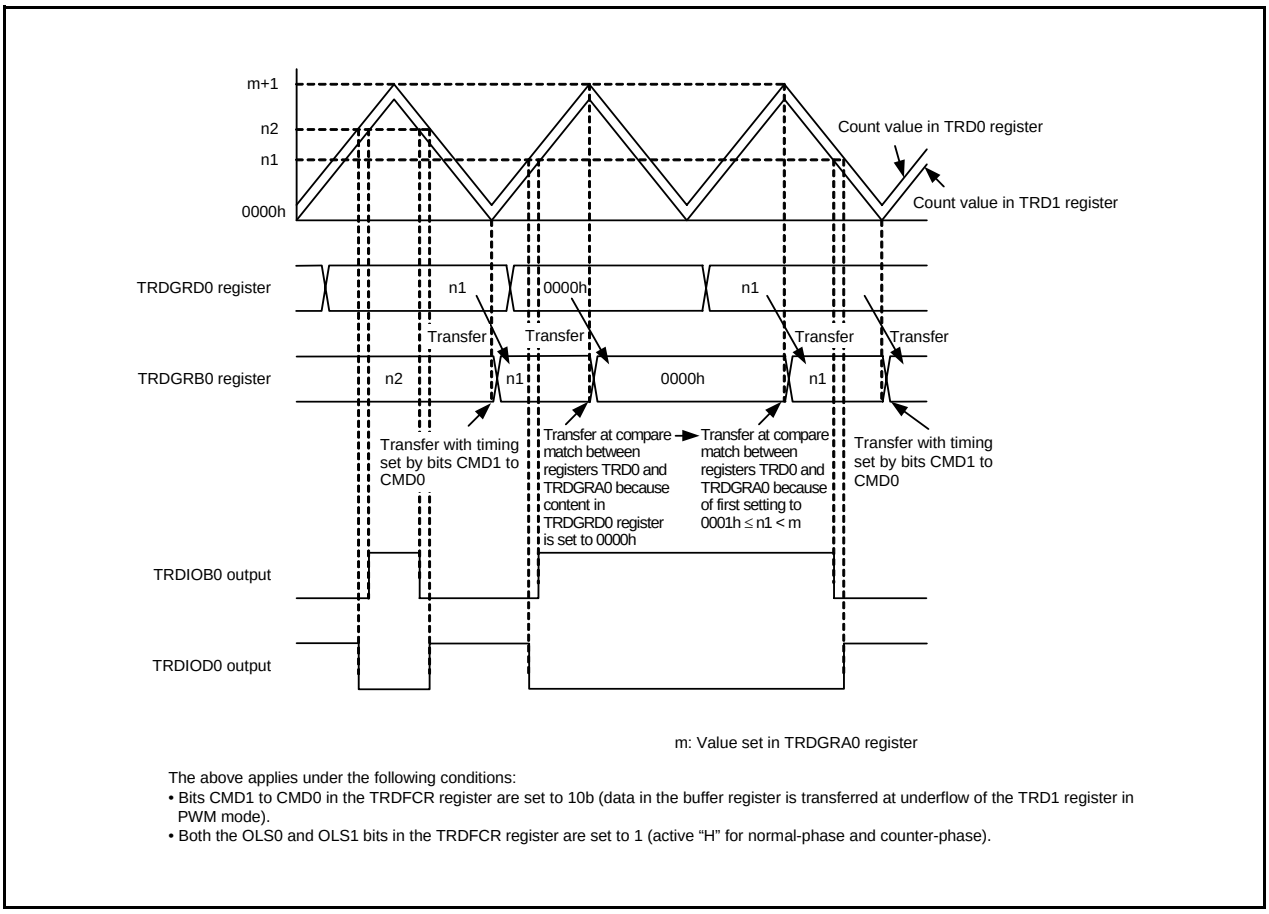


Figure 14.112 Operation when Value in Buffer Register Is Set to 0000h in Complementary PWM Mode

14.3.12.8 Count Source fOCO40M

- The count source fOCO40M can be used with supply voltage VCC = 3.0 to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in registers TRDCR0 and TRDCR to 110b (select fOCO40M as the count source).

14.4 Timer RE

Timer RE has the 4-bit counter and 8-bit counter. Timer RE has the following 2 modes:

- Real-time clock mode — Generate 1-second signal from fC4 and count seconds, minutes, hours, and days of the week.
- Output compare mode — Count a count source and detect compare matches.

The count source for timer RE is the operating clock that regulates the timing of timer operations.

14.4.1 Real-Time Clock Mode

In real-time clock mode, a 1-second signal is generated from fC4 using a divide-by-2 frequency divider, 4-bit counter, and 8-bit counter and used to count seconds, minutes, hours, and days of the week. Figure 14.113 shows a Block Diagram of Real-Time Clock Mode and Table 14.37 lists the Real-Time Clock Mode Specifications. Figures 14.114 to 14.118, and Figures 14.120 and 14.121 show the Registers Associated with Real-Time Clock Mode. Table 14.38 lists the Interrupt Sources, Figure 14.119 shows the Definition of Time Representation and Figure 14.122 shows the Operating Example in Real-Time Clock Mode.

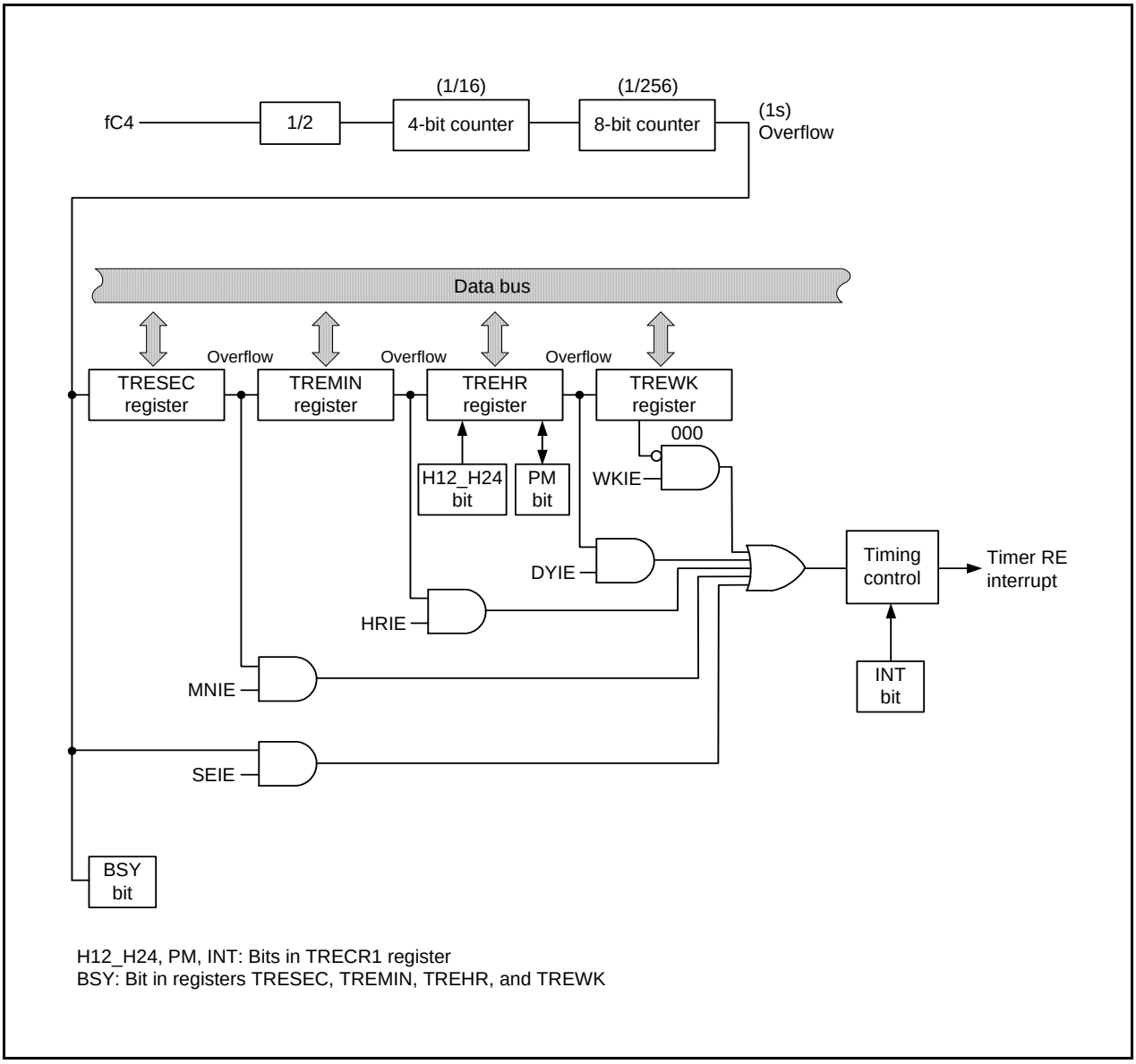
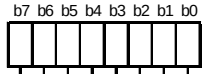


Figure 14.113 Block Diagram of Real-Time Clock Mode

Table 14.37 Real-Time Clock Mode Specifications

Item	Specification
Count source	fC4
Count operation	Increment
Count start condition	1 (count starts) is written to TSTART bit in TRECR1 register
Count stop condition	0 (count stops) is written to TSTART bit in TRECR1 register
Interrupt request generation timing	Select any one of the following: • Update second data • Update minute data • Update hour data • Update day of week data • When day of week data is set to 000b (Sunday)
TREO pin function	Programmable I/O ports or output of f2, f4, or f8
Read from timer	When reading TRESEC, TREMIN, TREHR, or TREWK register, the count value can be read. The values read from registers TRESEC, TREMIN, and TREHR are represented by the BCD code.
Write to timer	When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), the value can be written to registers TRESEC, TREMIN, TREHR, and TREWK. The values written to registers TRESEC, TREMIN, and TREHR are represented by the BCD codes.
Select function	• 12-hour mode/24-hour mode switch function

Timer RE Second Data Register

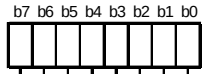


Symbol	Address	After Reset
TRESEC	0118h	00h

Bit Symbol	Bit Name	Function	Setting Range	RW
SC00	1st digit of second count bits	Count 0 to 9 every second. When the digit moves up, 1 is added to the 2nd digit of second.	0 to 9 (BCD code)	RW
SC01				RW
SC02				RW
SC03				RW
SC10	2nd digit of second count bits	When counting 0 to 5, 60 seconds are counted.	0 to 5 (BCD code)	RW
SC11				RW
SC12				RW
BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.		RO

Figure 14.114 TRESEC Register in Real-Time Clock Mode

Timer RE Minute Data Register

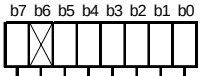


Symbol	Address	After Reset
TREMIN	0119h	00h

Bit Symbol	Bit Name	Function	Setting Range	RW
MN00	1st digit of minute count bits	Count 0 to 9 every minute. When the digit moves up, 1 is added to the 2nd digit of minute.	0 to 9 (BCD code)	RW
MN01				RW
MN02				RW
MN03				RW
MN10	2nd digit of minute count bits	When counting 0 to 5, 60 minutes are counted.	0 to 5 (BCD code)	RW
MN11				RW
MN12				RW
BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.		RO

Figure 14.115 TREMIN Register in Real-Time Clock Mode

Timer RE Hour Data Register



Symbol	Address	After Reset
TREHR	011Ah	00h

Bit Symbol	Bit Name	Function	Setting Range	RW
HR00	1st digit of hour count bits	Count 0 to 9 every hour. When the digit moves up, 1 is added to the 2nd digit of hour.	0 to 9 (BCD code)	RW
HR01				RW
HR02				RW
HR03				RW
HR10	2nd digit of hour count bits	Count 0 to 1 when the H12_H24 bit is set to 0 (12-hour mode). Count 0 to 2 when the H12_H24 bit is set to 1 (24-hour mode).	0 to 2 (BCD code)	RW
HR11				RW
— (b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—
BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.		RO

Figure 14.116 TREHR Register in Real-Time Clock Mode

Timer RE Day of Week Data Register

Symbol	Address	After Reset
TREWK	011Bh	00h

Bit Symbol	Bit Name	Function	RW
WK0	Day of week count bits	b2 b1 b0 0 0 0 : Sunday 0 0 1 : Monday 0 1 0 : Tuesday 0 1 1 : Wednesday 1 0 0 : Thursday 1 0 1 : Friday 1 1 0 : Saturday 1 1 1 : Do not set.	RW
WK1			RW
WK2			RW
— (b6-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.	RO

Figure 14.117 TREWK Register in Real-Time Clock Mode

Timer RE Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRECR1	011Ch	00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCSTF	Timer RE count status flag	0 : Count stopped 1 : Counting	RO
TOENA	TREO pin output enable bit	0 : Disable clock output 1 : Enable clock output	RW
INT	Interrupt request timing bit	Set to 1 in real-time clock mode.	RW
TRERST	Timer RE reset bit	When setting this bit to 0, after setting it to 1, the followings will occur. • Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2 are set to 00h. • Bits TCSTF, INT, PM, H12_H24, and TSTART in the TRECR1 register are set to 0. • The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.	RW
PM	A.m./p.m. bit	When the H12_H24 bit is set to 0 (12-hour mode)(1) 0 : a.m. 1 : p.m. When the H12_H24 bit is set to 1 (24-hour mode), its value is undefined.	RW
H12_H24	Operating mode select bit	0 : 12-hour mode 1 : 24-hour mode	RW
TSTART	Timer RE count start bit	0 : Count stops 1 : Count starts	RW

NOTE:
1. This bit is automatically modified while timer RE counts.

Figure 14.118 TRECR1 Register in Real-Time Clock Mode

Noon

Contents of TREHR Register	H12_H24 bit = 1 (24-hour mode)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	H12_H24 bit = 0 (12-hour mode)	0	1	2	3	4	5	6	7	8	9	10	11	0	1	2	3	4	5
Contents of PM bit		0 (a.m.)												1 (p.m.)					
Contents in TREWK register		000 (Sunday)																	

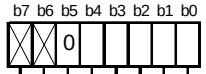
Date changes

Contents of TREHR Register	H12_H24 bit = 1 (24-hour mode)	18	19	20	21	22	23	0	1	2	3	...
	H12_H24 bit = 0 (12-hour mode)	6	7	8	9	10	11	0	1	2	3	...
Contents of PM bit		1 (p.m.)						0 (a.m.)				...
Contents in TREWK register		000 (Sunday)						001 (Monday)				...

PM bit and H12_H24 bits: Bits in TRECR1 register
The above applies to the case when count starts from a.m. 0 on Sunday.

Figure 14.119 Definition of Time Representation

Timer RE Control Register 2



Symbol	Address	After Reset
TRECR2	011Dh	00h

Bit Symbol	Bit Name	Function	RW
SEIE	Periodic interrupt triggered every second enable bit(1)	0 : Disable periodic interrupt triggered every second 1 : Enable periodic interrupt triggered every second	RW
MNIE	Periodic interrupt triggered every minute enable bit(1)	0 : Disable periodic interrupt triggered every minute 1 : Enable periodic interrupt triggered every minute	RW
HRIE	Periodic interrupt triggered every hour enable bit(1)	0 : Disable periodic interrupt triggered every hour 1 : Enable periodic interrupt triggered every hour	RW
DYIE	Periodic interrupt triggered every day enable bit(1)	0 : Disable periodic interrupt triggered every day 1 : Enable periodic interrupt triggered every day	RW
WKIE	Periodic interrupt triggered every week enable bit(1)	0 : Disable periodic interrupt triggered every week 1 : Enable periodic interrupt triggered every week	RW
COMIE	Compare match interrupt enable bit	Set to 0 in real-time clock mode.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Do not set multiple enable bits to 1 (enable interrupt).

Figure 14.120 TRECR2 Register in Real-Time Clock Mode

Table 14.38 Interrupt Sources

Factor	Interrupt Source	Interrupt Enable Bit
Periodic interrupt triggered every week	Value in TREWK register is set to 000b (Sunday) (1-week period)	WKIE
Periodic interrupt triggered every day	TREWK register is updated (1-day period)	DYIE
Periodic interrupt triggered every hour	TREHR register is updated (1-hour period)	HRIE
Periodic interrupt triggered every minute	TREMIN register is updated (1-minute period)	MNIE
Periodic interrupt triggered every second	TRESEC register is updated (1-second period)	SEIE

Timer RE Count Source Select Register

b7	b6	b5	b4	b3	b2	b1	b0
X			X	1	0	0	0

Symbol	Address	After Reset
TRECSR	011Eh	00001000b

Bit Symbol	Bit Name	Function	RW
RCS0	Count source select bits	Set to 00b in real-time clock mode.	RW
RCS1			RW
RCS2	4-bit counter select bit	Set to 0 in real-time clock mode.	RW
RCS3	Real-time clock mode select bit	Set to 1 in real-time clock mode.	RW
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
RCS5	Clock output select bits(1)	b6 b5 0 0 : f2 0 1 : f4 1 0 : f8 1 1 : Do not set.	RW
RCS6			RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Write to bits RCS5 to RCS6 when the TOENA bit in the TRECR1 register is set to 0 (disable clock output).

Figure 14.121 TRECSR Register in Real-Time Clock Mode

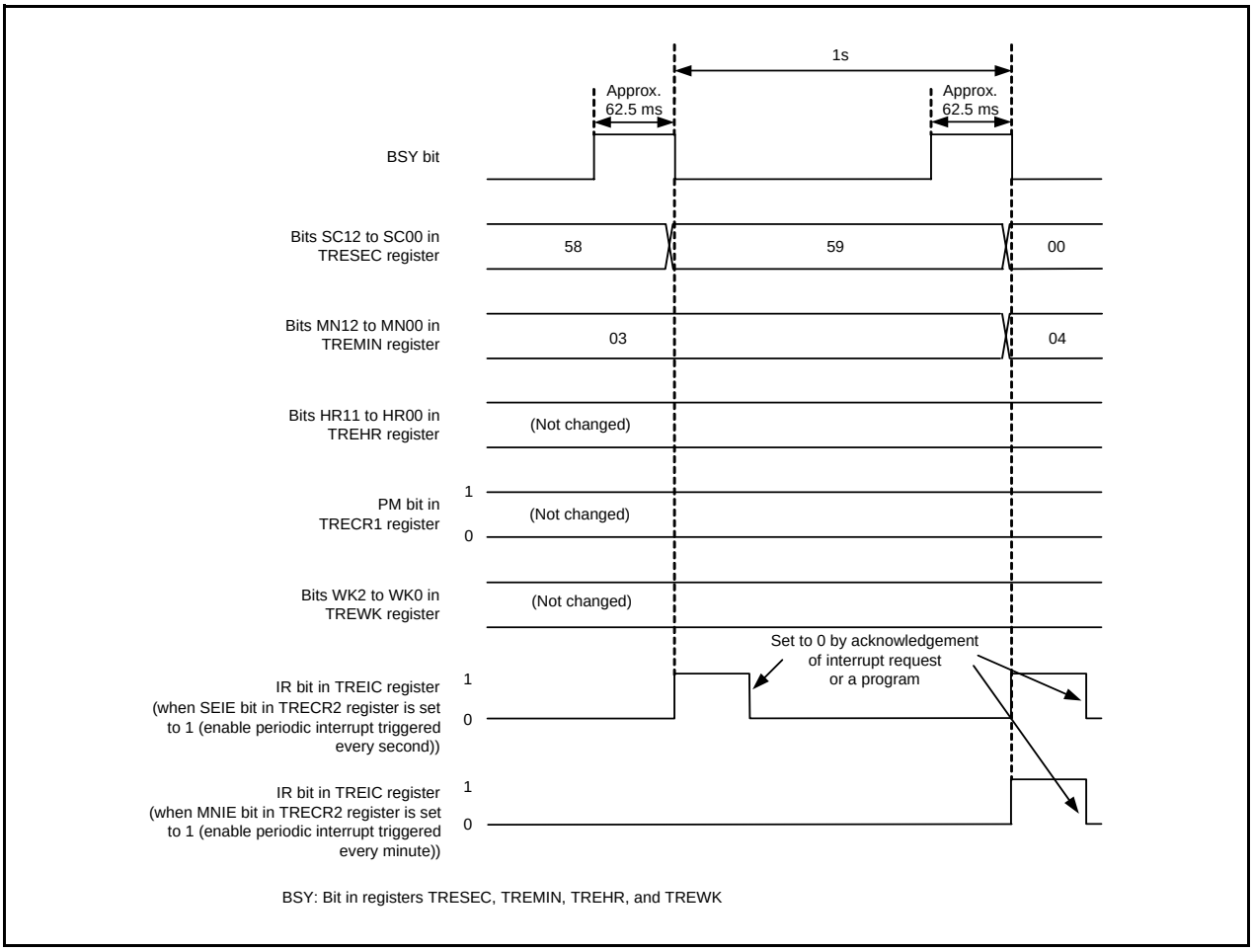


Figure 14.122 Operating Example in Real-Time Clock Mode

14.4.2 Output Compare Mode

In output compare mode, the internal count source divided by 2 is counted using the 4-bit or 8-bit counter and compare value match is detected with the 8-bit counter. Figure 14.123 shows a Block Diagram of Output Compare Mode, and Table 14.39 lists the Output Compare Mode Specifications. Figures 14.124 to 14.128 show the Registers Associated with Output Compare Mode, and Figure 14.129 shows the Operating Example in Output Compare Mode.

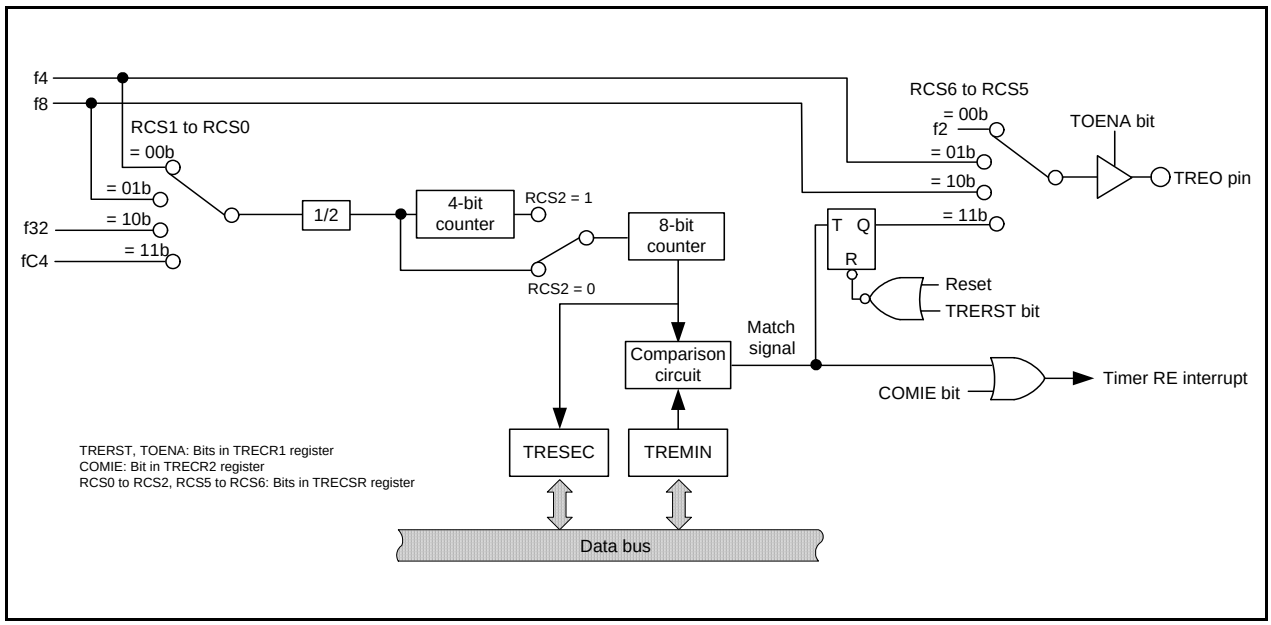


Figure 14.123 Block Diagram of Output Compare Mode

Table 14.39 Output Compare Mode Specifications

Item	Specification
Count sources	f4, f8, f32, fC4
Count operations	• Increment • When the 8-bit counter content matches with the TREMIN register content, the value returns to 00h and count continues. The count value is held while count stops.
Count period	• When RCS2 = 0 (4-bit counter is not used) 1/fi x 2 x (n+1) • When RCS2 = 1 (4-bit counter is used) 1/fi x 32 x (n+1) fi: Frequency of count source n: Setting value of TREMIN register
Count start condition	1 (count starts) is written to the TSTART bit in the TRECR1 register
Count stop condition	0 (count stops) is written to the TSTART bit in the TRECR1 register
Interrupt request generation timing	When the 8-bit counter content matches with the TREMIN register content
TREO pin function	Select any one of the following: • Programmable I/O ports • Output f2, f4, or f8 • Compare output
Read from timer	When reading the TRESEC register, the 8-bit counter value can be read. When reading the TREMIN register, the compare value can be read.
Write to timer	Writing to the TRESEC register is disabled. When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), writing to the TREMIN register is enabled.
Select functions	• Select use of 4-bit counter • Compare output function Every time the 8-bit counter value matches the TREMIN register value, TREO output polarity is reversed. The TREO pin outputs “L” after reset is deasserted and the timer RE is reset by the TRERST bit in the TRECR1 register. Output level is held by setting the TSTART bit to 0 (count stops).

Timer RE Counter Data Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRESEC	0118h	00h

Function	RW
8-bit counter data can be read. Although Timer RE stops counting, the count value is held. The TRESEC register is set to 00h at the compare match.	RO

Figure 14.124 TRESEC Register in Output Compare Mode

Timer RE Compare Data Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TREMIN	0119h	00h

Function	RW
8-bit compare data is stored.	RW

Figure 14.125 TREMIN Register in Output Compare Mode

Timer RE Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
	0	0		0			X

Symbol	Address	After Reset
TRECR1	011Ch	00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCSTF	Timer RE count status flag	0 : Count stopped 1 : Counting	RO
TOENA	TREO pin output enable bit	0 : Disable clock output 1 : Enable clock output	RW
INT	Interrupt request timing bit	Set to 0 in output compare mode.	RW
TRERST	Timer RE reset bit	When setting this bit to 0, after setting it to 1, the following will occur. • Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2 are set to 00h. • Bits TCSTF, INT, PM, H12_H24, and TSTART in the TRECR1 register are set to 0. • The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.	RW
PM	A.m./p.m. bit	Set to 0 in output compare mode.	RW
H12_H24	Operating mode select bit		RW
TSTART	Timer RE count start bit	0 : Count stops 1 : Count starts	RW

Figure 14.126 TRECR1 Register in Output Compare Mode

Timer RE Control Register 2

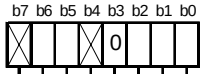
b7	b6	b5	b4	b3	b2	b1	b0
X	X		0	0	0	0	0

Symbol	Address	After Reset
TRECR2	011Dh	00h

Bit Symbol	Bit Name	Function	RW
SEIE	Periodic interrupt triggered every second enable bit	Set to 0 in output compare mode.	RW
MNIE	Periodic interrupt triggered every minute enable bit		RW
HRIE	Periodic interrupt triggered every hour enable bit		RW
DYIE	Periodic interrupt triggered every day enable bit		RW
WKIE	Periodic interrupt triggered every week enable bit		RW
COMIE	Compare match interrupt enable bit	0 : Disable compare match interrupt 1 : Enable compare match interrupt	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 14.127 TRECR2 Register in Output Compare Mode

Timer RE Count Source Select Register



Symbol	Address	After Reset
TRECSR	011Eh	00001000b

Bit Symbol	Bit Name	Function	RW
RCS0	Count source select bits	b1 b0 0 0 : f4 0 1 : f8 1 0 : f32 1 1 : fC4	RW
RCS1			RW
RCS2	4-bit counter select bit	0 : Not used 1 : Used	RW
RCS3	Real-time clock mode select bit	Set to 0 in output compare mode.	RW
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
RCS5	Clock output select bits(1)	b6 b5 0 0 : f2 0 1 : f4 1 0 : f8 1 1 : Compare output	RW
RCS6			RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Write to bits RCS5 to RCS6 when the TOENA bit in the TRECR1 register is set to 0 (disable clock output).

Figure 14.128 TRECSR Register in Output Compare Mode

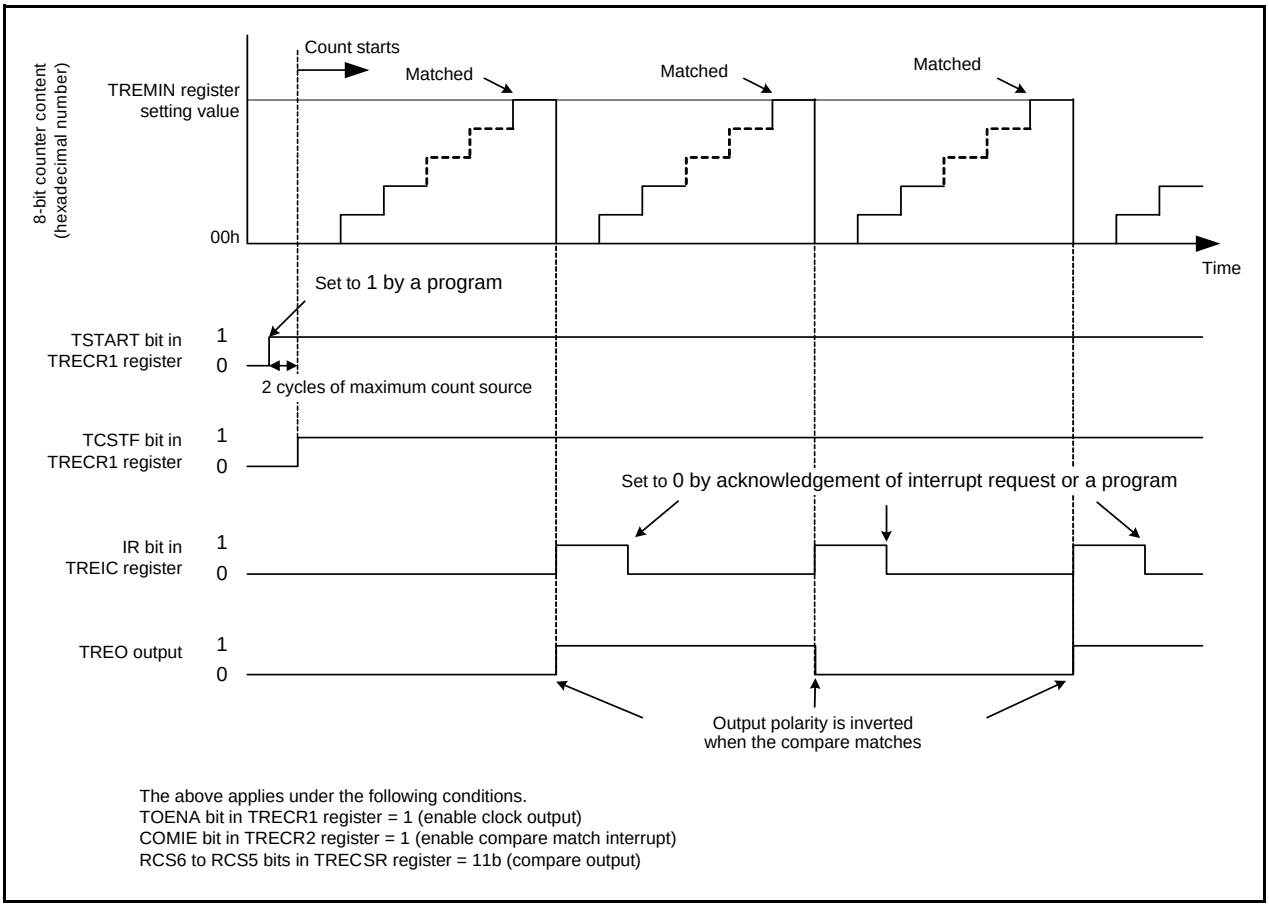


Figure 14.129 Operating Example in Output Compare Mode

14.4.3 Notes on Timer RE

14.4.3.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TRECR1 register.
Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE(1) other than the TCSTF bit.
Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

NOTE:
1. Registers associated with timer RE: TRESEC, TREMIN, TREHR, TREWK, TRECR1, TRECR2, and TRECSR.

14.4.3.2 Register Setting

Write to the following registers or bits when timer RE is stopped.
- Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2
- Bits H12_H24, PM, and INT in TRECR1 register
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.
Figure 14.130 shows a Setting Example in Real-Time Clock Mode.

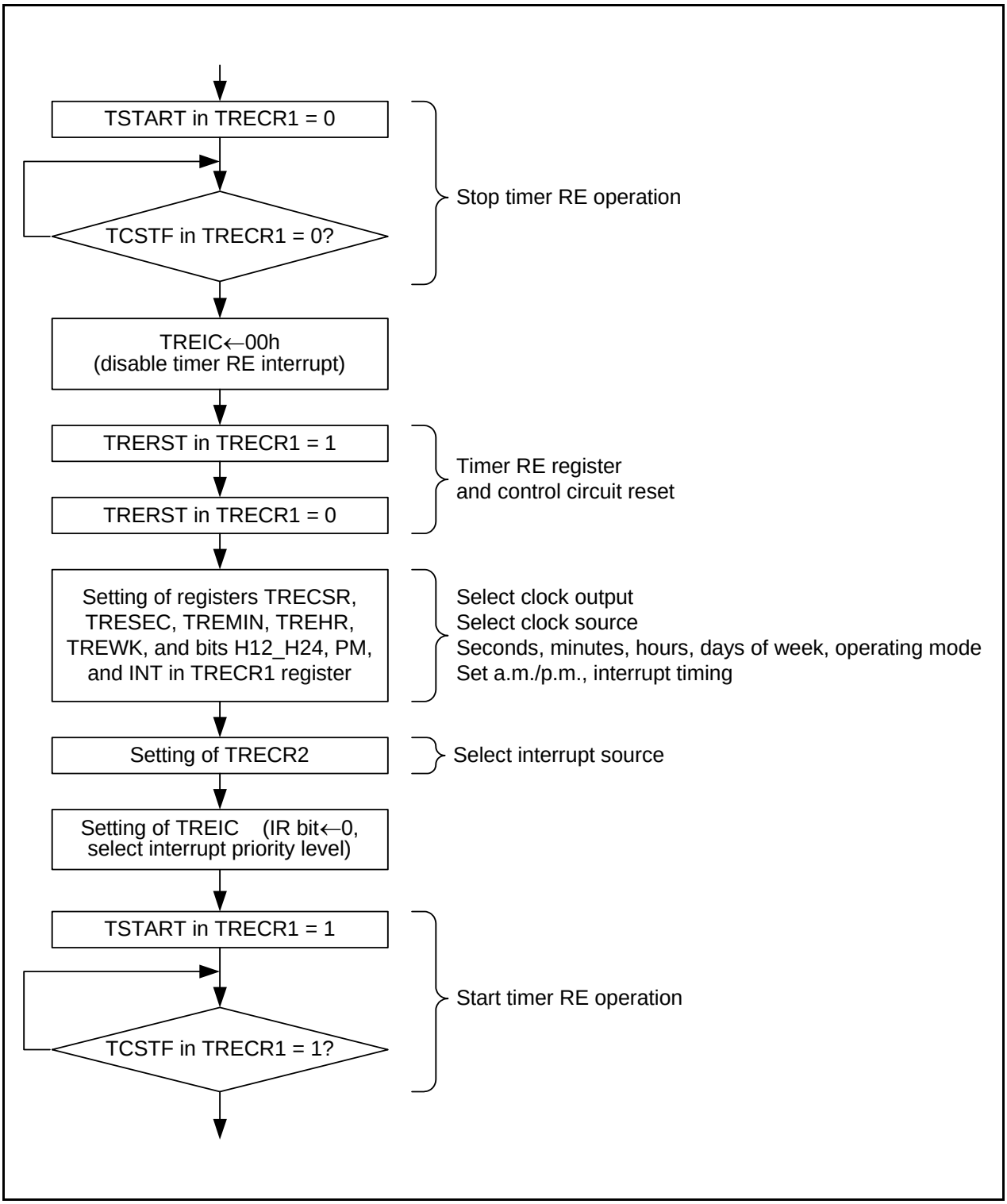


Figure 14.130 Setting Example in Real-Time Clock Mode

14.4.3.3 Time Reading Procedure of Real-Time Clock Mode

In real-time clock mode, read registers TRESEC, TREMIN, TREHR, and TREWK when time data is updated and read the PM bit in the TRECR1 register when the BSY bit is set to 0 (not while data is updated).
Also, when reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.

In order to prevent this, use the reading procedure shown below.

- Using an interrupt
  Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register in the timer RE interrupt routine.

- Monitoring with a program 1
  Monitor the IR bit in the TREIC register with a program and read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the IR bit in the TREIC register is set to 1 (timer RE interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.
(2) Monitor until the BSY bit is set to 0 after the BSY bit is set to 1 (approximately 62.5 ms while the BSY bit is set to 1).
(3) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register.
(2) Read the same register as (1) and compare the contents.
(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.

15. Serial Interface

The serial interface consists of two channels (UART0 and UART1). Each UARTi (i = 0 or 1) has an exclusive timer to generate the transfer clock and operates independently.
Figure 15.1 shows a UARTi (i = 0 or 1) Block Diagram. Figure 15.2 shows a UARTi Transmit/Receive Unit.
UARTi has two modes: clock synchronous serial I/O mode and clock asynchronous serial I/O mode (UART mode).
Figures 15.3 to 15.6 show the Registers Associated with UARTi.

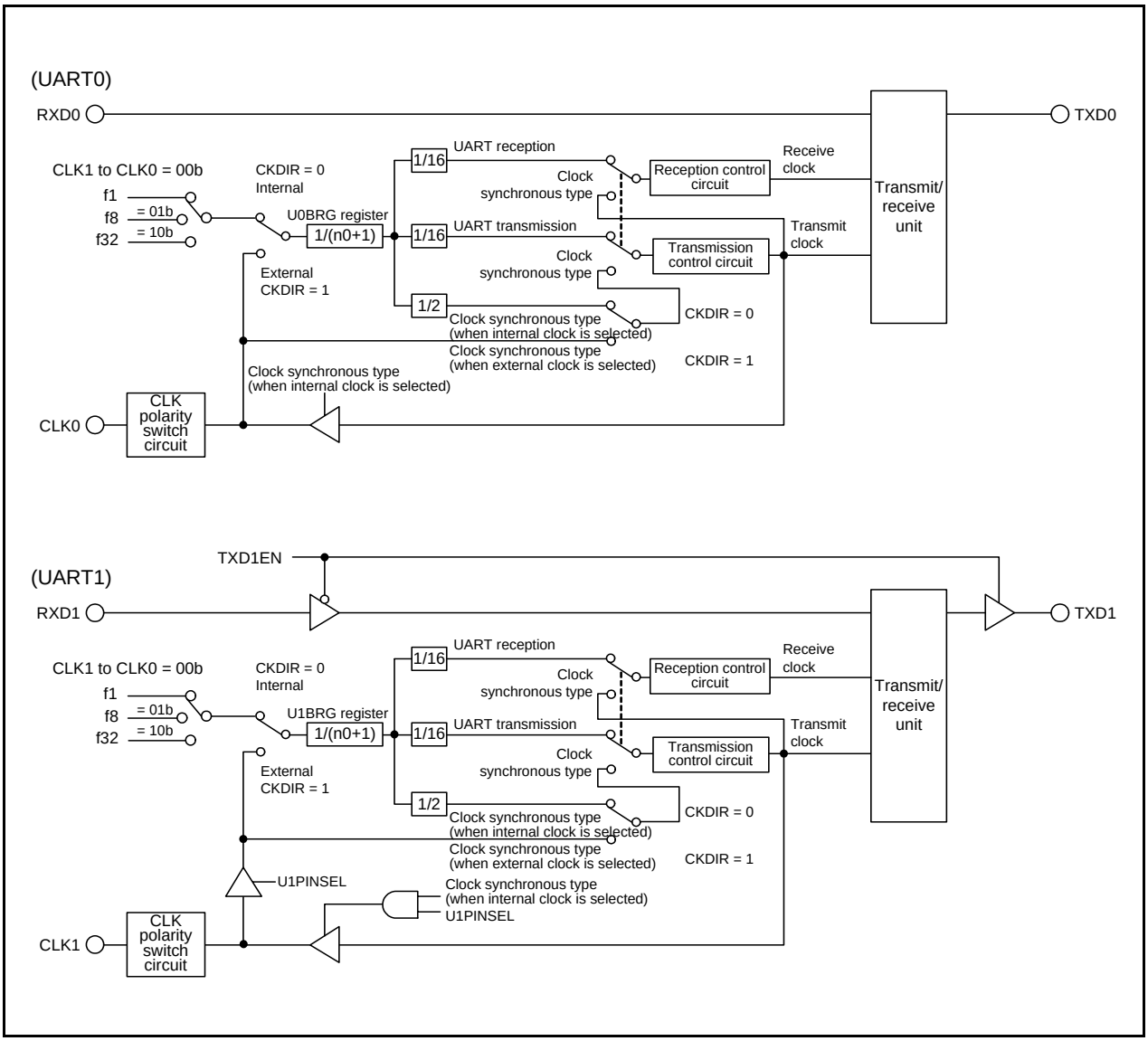


Figure 15.1 UARTi (i = 0 or 1) Block Diagram

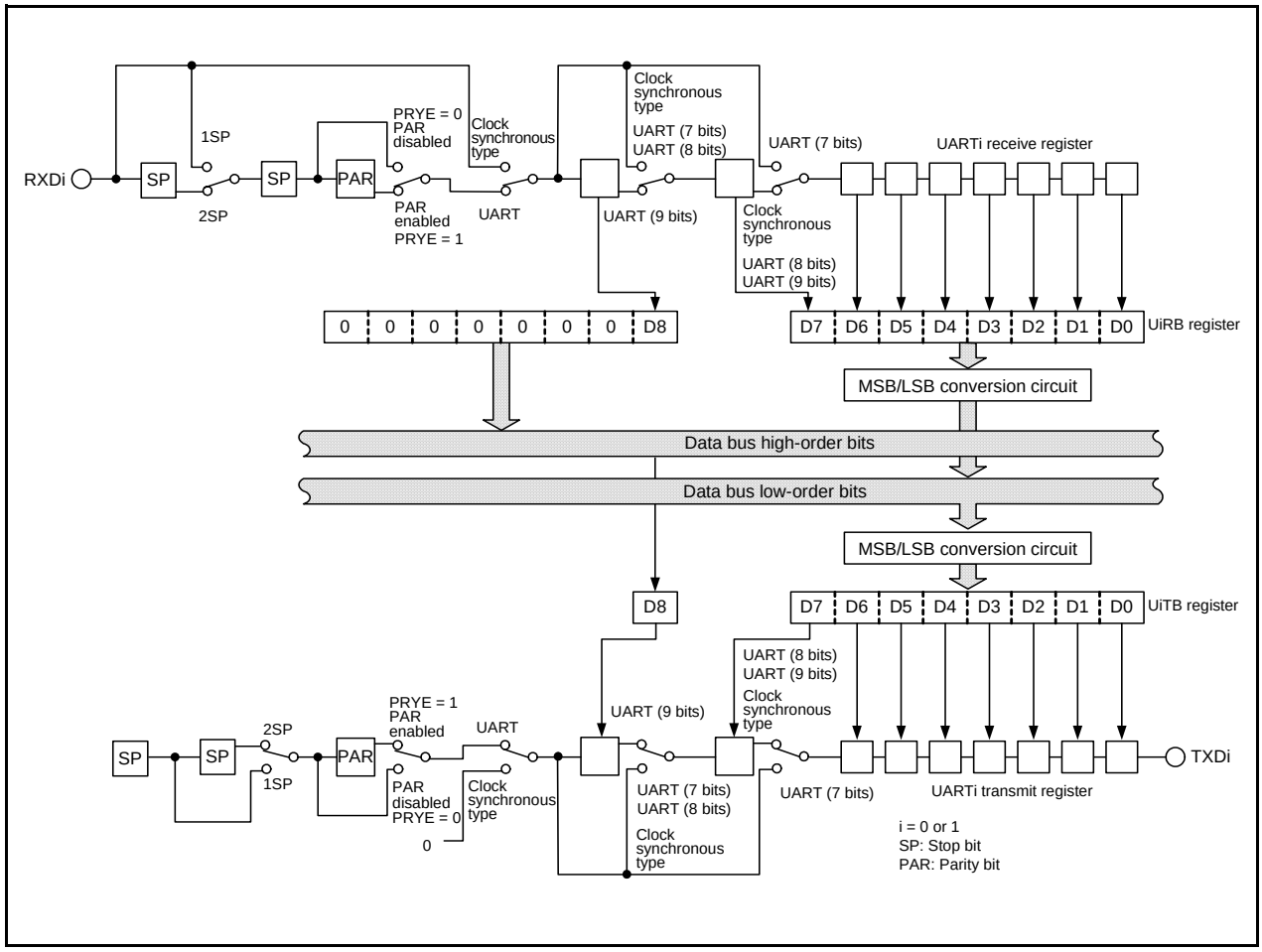
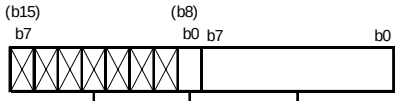


Figure 15.2 UARTi Transmit/Receive Unit

UARTi Transmit Buffer Register (i = 0 or 1)(1, 2)

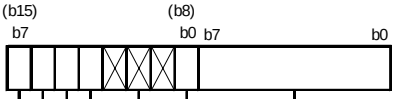


Symbol	Address	After Reset
U0TB	00A3h-00A2h	Undefined
U1TB	00ABh-00AAh	Undefined

Function		RW
— (b8-b0)	Transmit data	WO
— (b15-b9)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.	—

NOTES:
1. When the transfer data length is 9 bits, write data to high byte first, then low byte.
2. Use the MOV instruction to write to this register.

UARTi Receive Buffer Register (i = 0 or 1)(1)



Symbol	Address	After Reset
U0RB	00A7h-00A6h	Undefined
U1RB	00AFh-00AEh	Undefined

Bit Symbol	Bit Name	Function	RW
— (b7-b0)	—	Receive data (D7 to D0)	RO
— (b8)	—	Receive data (D8)	RO
— (b11-b9)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
OER	Overrun error flag(2)	0 : No overrun error 1 : Overrun error	RO
FER	Framing error flag(2)	0 : No framing error 1 : Framing error	RO
PER	Parity error flag(2)	0 : No parity error 1 : Parity error	RO
SUM	Error sum flag(2)	0 : No error 1 : Error	RO

NOTES:
1. Read out the UiRB register in 16-bit units.
2. Bits SUM, PER, FER, and OER are set to 0 (no error) when bits SMD2 to SMD0 in the UiMR register are set to 000b (serial interface disabled) or the RE bit in the UiC1 register is set to 0 (receive disabled). The SUM bit is set to 0 (no error) when bits PER, FER, and OER are set to 0 (no error). Bits PER and FER are set to 0 even when the higher byte of the UiRB register is read out.
   Also, bits PER and FER are set to 0 when reading the high-order byte of the UiRB register.

Figure 15.3 Registers U0TB to U1TB and U0RB to U1RB

UARTi Bit Rate Register (i = 0 or 1)(1, 2, 3)

b7 b0

Symbol	Address	After Reset
U0BRG	00A1h	Undefined
U1BRG	00A9h	Undefined

Function	Setting Range	RW
Assuming the set value is n, UiBRG divides the count source by n+1	00h to FFh	WO

NOTES:
1. Write to this register while the serial I/O is neither transmitting nor receiving.
2. Use the MOV instruction to write to this register.
3. After setting the CLK0 to CLK1 bits of the UiC0 register, write to the UiBRG register.

UARTi Transmit/Receive Mode Register (i = 0 or 1)

b7 b6 b5 b4 b3 b2 b1 b0

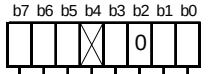
Symbol	Address	After Reset
U0MR	00A0h	00h
U1MR	00A8h	00h

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O mode select bits	b2 b1 b0 0 0 0 : Serial interface disabled 0 0 1 : Clock synchronous serial I/O mode 1 0 0 : UART mode transfer data 7 bits long 1 0 1 : UART mode transfer data 8 bits long 1 1 0 : UART mode transfer data 9 bits long Other than above : Do not set.	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock(1)	RW
STPS	Stop bit length select bit	0 : 1 stop bit 1 : 2 stop bits	RW
PRY	Odd/even parity select bit	Enable when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
— (b7)	Reserved bit	Set to 0.	RW

NOTE:
1. Set the PD1_6 bit in the PD1 register to 0 (input).

Figure 15.4 Registers U0BRG to U1BRG and U0MR to U1MR

UARTi Transmit/Receive Control Register 0 (i = 0 or 1)



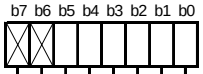
Symbol	Address	After Reset
U0C0	00A4h	00001000b
U1C0	00ACh	00001000b

Bit Symbol	Bit Name	Function	RW
CLK0	BRG count source select bits(1)	b1 b0 0 0 : Selects f1 0 1 : Selects f8 1 0 : Selects f32 1 1 : Do not set.	RW
CLK1			RW
— (b2)	Reserved bit	Set to 0.	RW
TXEPT	Transmit register empty flag	0 : Data in transmit register (during transmit) 1 : No data in transmit register (transmit completed)	RO
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
NCH	Data output select bit	0 : TXDi pin is for CMOS output 1 : TXDi pin is for N-channel open drain output	RW
CKPOL	CLK polarity select bit	0 : Transmit data is output at falling edge of transfer clock and receive data is input at rising edge 1 : Transmit data is output at rising edge of transfer clock and receive data is input at falling edge	RW
UFORM	Transfer format select bit	0 : LSB first 1 : MSB first	RW

NOTE:
1. If the BRG count source is switched, set the UiBRG register again.

Figure 15.5 Registers U0C0 to U1C0

UARTi Transmit/Receive Control Register 1 (i = 0 or 1)

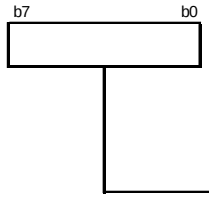


Symbol	Address	After Reset
U0C1	00A5h	00000010b
U1C1	00ADh	00000010b

Bit Symbol	Bit Name	Function	RW
TE	Transmit enable bit(1)	0 : Disables transmission 1 : Enables transmission	RW
TI	Transmit buffer empty flag	0 : Data in UiTB register 1 : No data in UiTB register	RO
RE	Receive enable bit	0 : Disables reception 1 : Enables reception	RW
RI	Receive complete flag(1)	0 : No data in UiRB register 1 : Data in UiRB register	RO
UiIRS	UARTi transmit interrupt cause select bit	0 : Transmission buffer empty (TI=1) 1 : Transmission completed (TXEPT=1)	RW
UiRRM	UARTi continuous receive mode enable bit(2)	0 : Disables continuous receive mode 1 : Enables continuous receive mode	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. The RI bit is set to 0 when the higher byte of the UiRB register is read out.
2. Set the UiRRM bit to 0 (disables continuous receive mode) in UART mode.

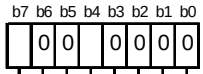
UART1 Function Select Register



Symbol	Address	After Reset
U1SR	00F5h	Undefined

Function	RW
Set to 0Fh when using UART1. As a result, UART1 can be used for clock synchronous or clock asynchronous serial I/O. Do not set values other than 0Fh. When read, its content is undefined.	WO

Port Mode Register



Symbol	Address	After Reset
PMR	00F8h	00h

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Reserved bits	Set to 0.	—
U1PINSEL	Port CLK1/TXD1/RXD1 switch bit	0 : I/O ports P6_5, P6_6, P6_7 1 : CLK1, TXD1, RXD1	RW
— (b6-b5)	Reserved bits	Set to 0.	—
IICSEL	SSU / I²C bus switch bit	0 : Selects SSU function 1 : Selects I²C bus function	RW

Figure 15.6 Registers U0C1 to U1C1, U1SR, and PMR

15.1 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 15.1 lists the Clock Synchronous Serial I/O Mode Specifications. Table 15.2 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

Table 15.1 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 bits
Transfer clocks	• CKDIR bit in UiMR register is set to 0 (internal clock): fi/(2(n+1)) fi = f1, f8, f32 n = value set in UiBRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): input from CLKi pin
Transmit start conditions	• Before transmission starts, the following requirements must be met(1) - The TE bit in the UiC1 register is set to 1 (transmission enabled) - The TI bit in the UiC1 register is set to 0 (data in the UiTB register)
Receive start conditions	• Before reception starts, the following requirements must be met(1) - The RE bit in the UiC1 register is set to 1 (reception enabled) - The TE bit in the UiC1 register is set to 1 (transmission enabled) - The TI bit in the UiC1 register is set to 0 (data in the UiTB register)
Interrupt request generation timing	• When transmitting, one of the following conditions can be selected - The UiIRS bit is set to 0 (transmit buffer empty): When transferring data from the UiTB register to UARTi transmit register (when transmission starts). - The UiIRS bit is set to 1 (transmission completes): When completing data transmission from UARTi transmit register. • When receiving When data transfer from the UARTi receive register to the UiRB register (when reception completes).
Error detection	• Overrun error(2) This error occurs if the serial interface starts receiving the next data item before reading the UiRB register and receives the 7th bit of the next data.
Select functions	• CLK polarity selection Transfer data input/output can be selected to occur synchronously with the rising or the falling edge of the transfer clock. • LSB first, MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Receive is enabled immediately by reading the UiRB register.

i = 0 or 1

NOTES:

1. If an external clock is selected, ensure that the external clock is “H” when the CKPOL bit in the UiC0 register is set to 0 (transmit data output at falling edge and receive data input at rising edge of transfer clock), and that the external clock is “L” when the CKPOL bit is set to 1 (transmit data output at rising edge and receive data input at falling edge of transfer clock).
2. If an overrun error occurs, the receive data (b0 to b8) of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 15.2 Registers Used and Settings in Clock Synchronous Serial I/O Mode(1)

Register	Bit	Function
UiTB	0 to 7	Set data transmission
UiRB	0 to 7	Data reception can be read
	OER	Overrun error flag
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to 001b
	CKDIR	Select the internal clock or external clock
UiC0	CLK1 to CLK0	Select the count source in the UiBRG register
	TXEPT	Transmit register empty flag
	NCH	Select TXDi pin output mode
	CKPOL	Select the transfer clock polarity
	UFORM	Select the LSB first or MSB first
UiC1	TE	Set this bit to 1 to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set this bit to 1 to enable reception
	RI	Reception complete flag
	UiIRS	Select the UARTi transmit interrupt source
	UiRRM	Set this bit to 1 to use continuous receive mode

i = 0 or 1

NOTE:

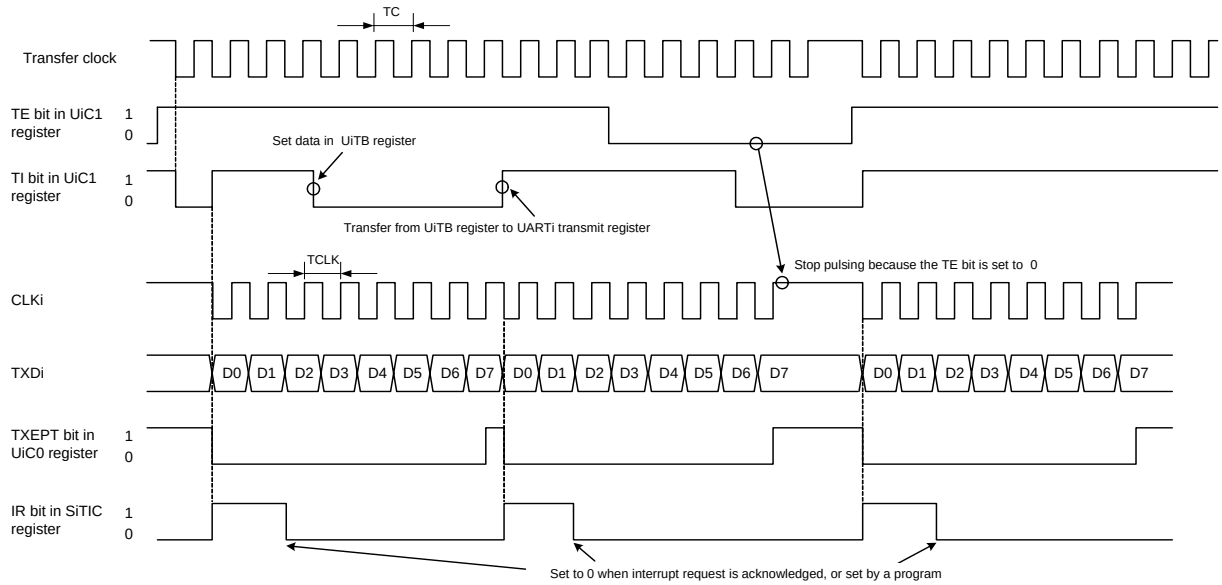
1. Set bits which are not in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 15.3 lists the I/O Pin Functions in Clock Synchronous Serial I/O Mode. The TXDi pin outputs “H” level between the operating mode selection of UARTi (i = 0 or 1) and transfer start. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in a high-impedance state.)

Table 15.3 I/O Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	Function	Selection Method
TXD0 (P1_4)	Output serial data	(Outputs dummy data when performing reception only)
RXD0 (P1_5)	Input serial data	PD1_5 bit in PD1 register = 0 (P1_5 can be used as an input port when performing transmission only)
CLK0 (P1_6)	Output transfer clock	CKDIR bit in U0MR register = 0
	Input transfer clock	CKDIR bit in U0MR register = 1 PD1_6 bit in PD1 register = 0
TXD1 (P6_6)	Output serial data	U1PINSEL bit in PMR register = 1 (Outputs dummy data when performing reception only)
RXD1 (P6_7)	Input serial data	U1PINSEL bit in PMR register = 1 PD6_7 bit in PD6 register = 0 (P6_7 can be used as an input port when performing transmission only)
CLK1 (P6_5)	Output transfer clock	U1PINSEL bit in PMR register = 1 CKDIR bit in U1MR register = 0
	Input transfer clock	U1PINSEL bit in PMR register = 1 PD6_5 bit in PD6 register = 0 CKDIR bit in U1MR register = 1

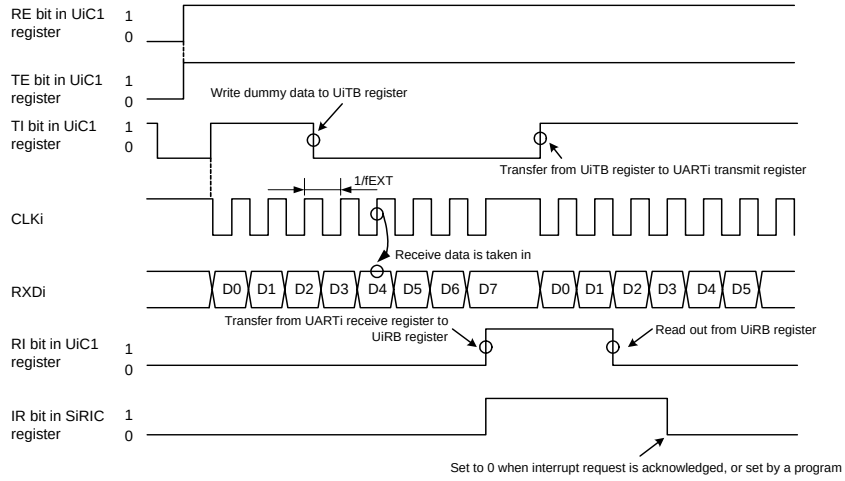
• Example of transmit timing (when internal clock is selected)



TC=TCLK=2(n+1)/fi
fi: Frequency of UiBRG count source (f1, f8, f32)
n: Setting value to UiBRG register

The above applies under the following settings:
- CKDIR bit in UiMR register = 0 (internal clock)
- CKPOL bit in UiC0 register = 0 (output transmit data at the falling edge and input receive data at the rising edge of the transfer clock)
- UiIRS bit in UiC1 register = 0 (an interrupt request is generated when the transmit buffer is empty)

• Example of receive timing (when external clock is selected)



The above applies under the following settings:
- CKDIR bit in UiMR register = 1 (external clock)
- CKPOL bit in UiC0 register = 0 (output transmit data at the falling edge and input receive data at the rising edge of the transfer clock)

The following conditions are met when “H” is applied to the CLKi pin before receiving data:
- TE bit in UiC1 register = 1 (enables transmit)
- RE bit in UiC1 register = 1 (enables receive)
- Write dummy data to the UiTB register

fEXT: Frequency of external clock

i = 0 or 1

Figure 15.7 Transmit and Receive Timing Example in Clock Synchronous Serial I/O Mode

15.1.1 Polarity Select Function

Figure 15.8 shows the Transfer Clock Polarity. Use the CKPOL bit in the UiC0 (i = 0 or 1) register to select the transfer clock polarity.

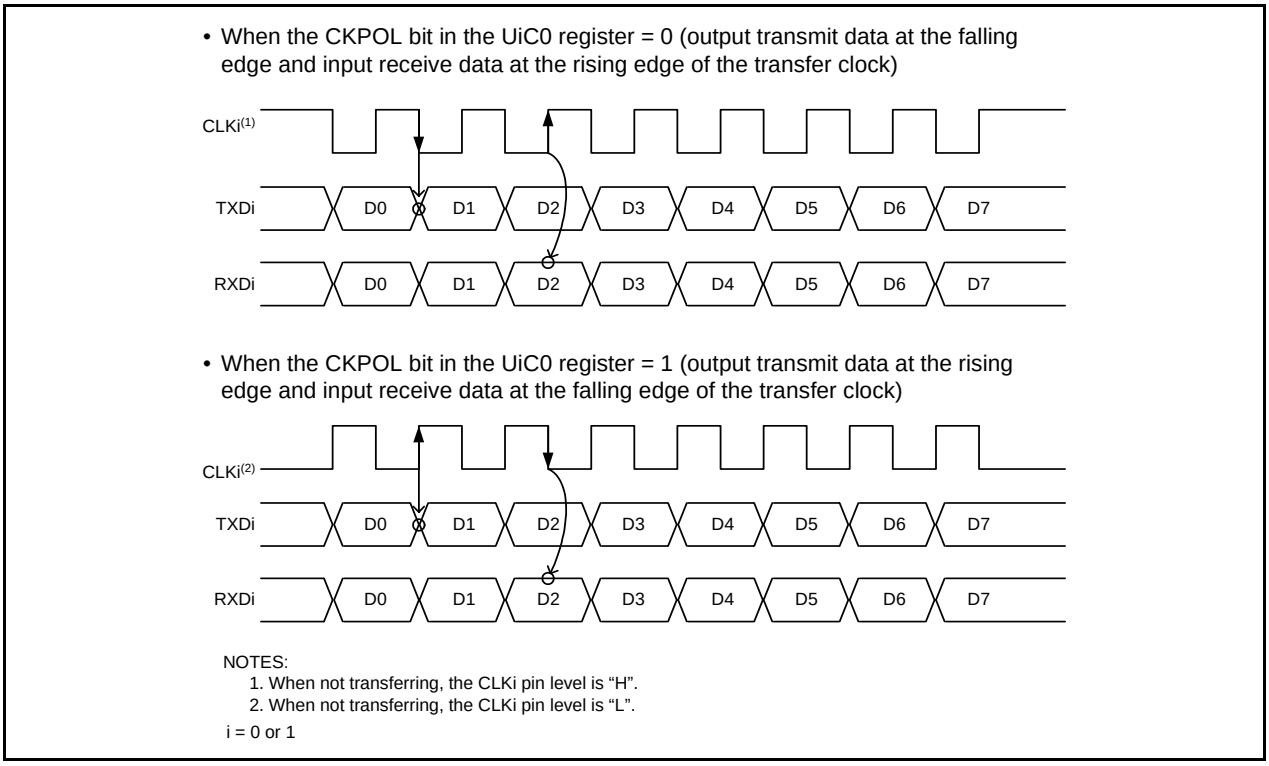


Figure 15.8 Transfer Clock Polarity

15.1.2 LSB First/MSB First Select Function

Figure 15.9 shows the Transfer Format. Use the UFORM bit in the UiC0 (i = 0 or 1) register to select the transfer format.

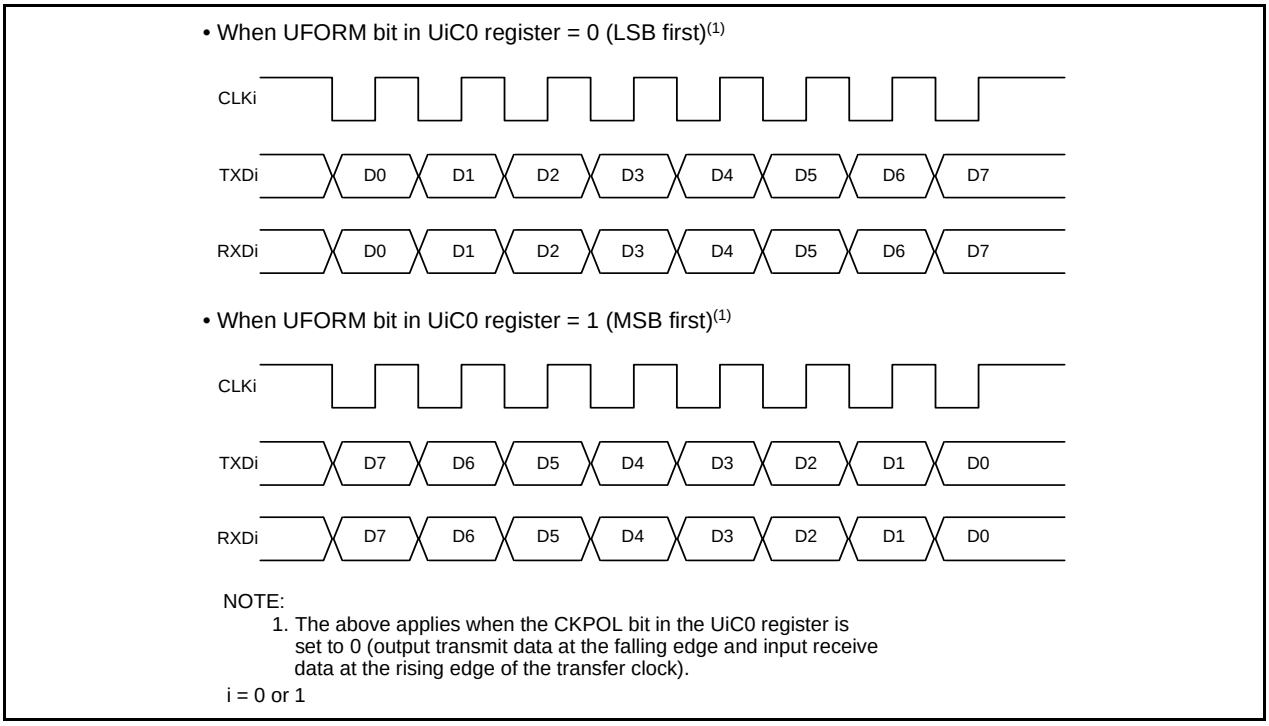


Figure 15.9 Transfer Format

15.1.3 Continuous Receive Mode

Continuous receive mode is selected by setting the UiRRM (i = 0 or 1) bit in the UiC1 register to 1 (enables continuous receive mode). In this mode, reading the UiRB register sets the TI bit in the UiC1 register to 0 (data in the UiTB register). When the UiRRM bit is set to 1, do not write dummy data to the UiTB register by a program.

15.2 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data transmission and reception after setting the desired bit rate and transfer data format. Table 15.4 lists the UART Mode Specifications. Table 15.5 lists the Registers Used and Settings for UART Mode.

Table 15.4 UART Mode Specifications

Item	Specification
Transfer data formats	• Character bit (transfer data): Selectable among 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable among odd, even, or none • Stop bit: Selectable among 1 or 2 bits
Transfer clocks	• CKDIR bit in UiMR register is set to 0 (internal clock): fj/(16(n+1)) fj = f1, f8, f32 n = value set in UiBRG register: 00h to FFh • CKDIR bit is set to 1 (external clock): fEXT/(16(n+1)) fEXT: Input from CLKi pin, n = value set in UiBRG register: 00h to FFh
Transmit start conditions	• Before transmission starts, the following are required - TE bit in UiC1 register is set to 1 (transmission enabled) - TI bit in UiC1 register is set to 0 (data in UiTB register)
Receive start conditions	• Before reception starts, the following are required - RE bit in UiC1 register is set to 1 (reception enabled) - Start bit detected
Interrupt request generation timing	• When transmitting, one of the following conditions can be selected - UiIRS bit is set to 0 (transmit buffer empty): When transferring data from the UiTB register to UARTi transmit register (when transmission starts). - UiIRS bit is set to 1 (transfer ends): When serial interfac.e completes transmitting data from the UARTi transmit register • When receiving When transferring data from the UARTi receive register to UiRB register (when reception ends).
Error detection	• Overrun error(1) This error occurs if the serial interface starts receiving the next data item before reading the UiRB register and receive the bit preceding the final stop bit of the next data item. • Framing error This error occurs when the set number of stop bits is not detected. • Parity error This error occurs when parity is enabled, and the number of 1’s in parity and character bits do not match the number of 1’s set. • Error sum flag This flag is set is set to 1 when an overrun, framing, or parity error is generated.

i = 0 or 1

NOTE:

1. If an overrun error occurs, the receive data (b0 to b8) of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 15.5 Registers Used and Settings for UART Mode

Register	Bit	Function
UiTB	0 to 8	Set transmit data(1)
UiRB	0 to 8	Receive data can be read(1, 2)
	OER,FER,PER,SUM	Error flag
UiBRG	0 to 7	Set a bit rate
UiMR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long Set to 101b when transfer data is 8 bits long Set to 110b when transfer data is 9 bits long
	CKDIR	Select the internal clock or external clock
	STPS	Select the stop bit
	PRY, PRYE	Select whether parity is included and whether odd or even
UiC0	CLK0, CLK1	Select the count source for the UiBRG register
	TXEPT	Transmit register empty flag
	NCH	Select TXDi pin output mode
	CKPOL	Set to 0
	UFORM	LSB first or MSB first can be selected when transfer data is 8 bits long. Set to 0 when transfer data is 7 or 9 bits long.
UiC1	TE	Set to 1 to enable transmit
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable receive
	RI	Receive complete flag
	UiIRS	Select the source of UARTi transmit interrupt
	UiRRM	Set to 0

i = 0 or 1

NOTES:

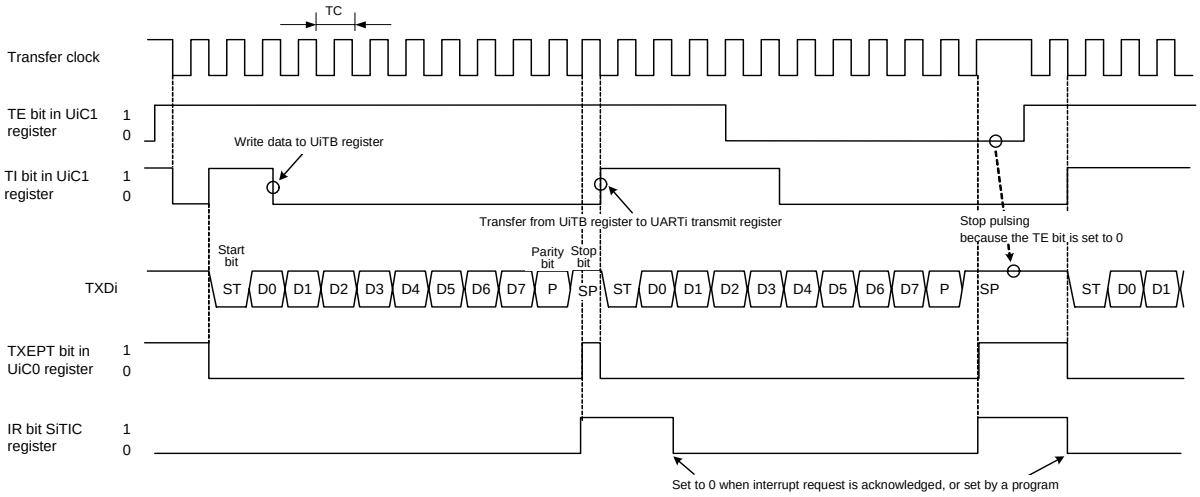
1. The bits used for transmit/receive data are as follows: Bits 0 to 6 when transfer data is 7 bits long; bits 0 to 7 when transfer data is 8 bits long; bits 0 to 8 when transfer data is 9 bits long.
2. The following bits are undefined: Bits 7 and 8 when transfer data is 7 bits long; bit 8 when transfer data is 8 bits long.

Table 15.6 lists the I/O Pin Functions in UART Mode. After the UARTi (i = 0 or 1) operating mode is selected, the TXDi pin outputs “H” level. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in a high-impedance state) until transfer starts.)

Table 15.6 I/O Pin Functions in UART Mode

Pin name	Function	Selection Method
TXD0 (P1_4)	Output serial data	(Cannot be used as a port when performing reception only)
RXD0 (P1_5)	Input serial data	PD1_5 bit in PD1 register = 0 (P1_5 can be used as an input port when performing transmission only)
CLK0 (P1_6)	Programmable I/O Port	CKDIR bit in U0MR register = 0
	Input transfer clock	CKDIR bit in U0MR register = 1 PD1_6 bit in PD1 register = 0
TXD1 (P6_6)	Output serial data	U1PINSEL bit in PMR register = 1 (Cannot be used as a port when performing reception only)
RXD1 (P6_7)	Input serial data	U1PINSEL bit in PMR register = 1 PD6_7 bit in PD6 register = 0 (P6_7 can be used as an input port when performing transmission only)
CLK1 (P6_5)	Programmable I/O Port	CKDIR bit in U1MR register = 0
	Input transfer clock	U1PINSEL bit in PMR register = 1 PD6_5 bit in PD6 register = 0 CKDIR bit in U1MR register = 1

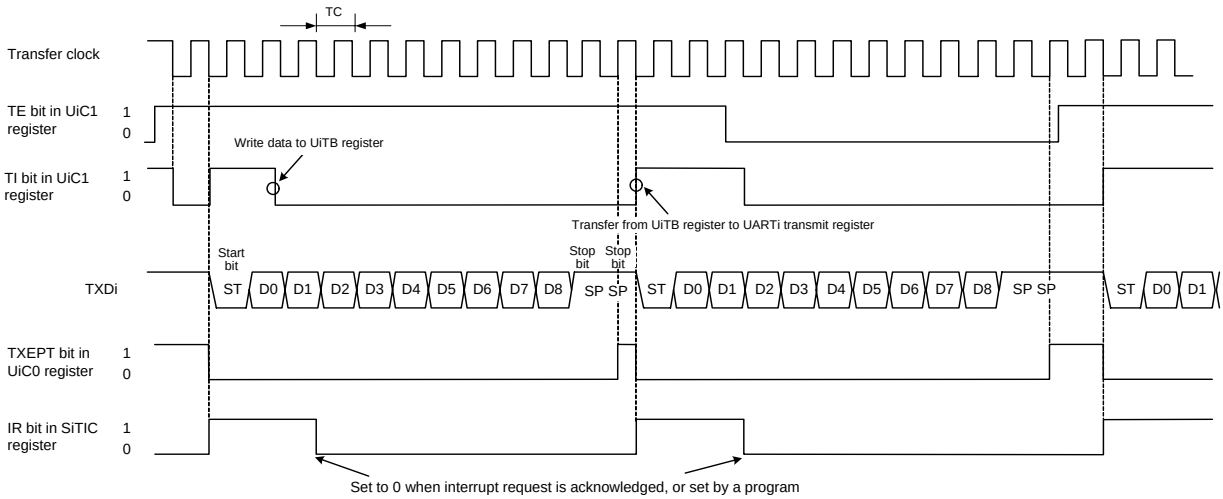
• Transmit timing when transfer data is 8 bits long (parity enabled, 1 stop bit)



The above timing diagram applies under the following conditions:
- PRYE bit in UiMR register = 1 (parity enabled)
- STPS bit in UiMR register = 0 (1 stop bit)
- UiIRS bit in UiC1 register = 1 (an interrupt request is generated when transmit completes)

TC=16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of UiBRG count source (f1, f8, f32)
fEXT: Frequency of UiBRG count source (external clock)
n: Setting value to UiBRG register
i = 0 to 1

• Transmit timing when transfer data is 9 bits long (parity disabled, 2 stop bits)



The above timing diagram applies under the following conditions:
- PRYE bit in UiMR register = 0 (parity disabled)
- STPS bit in UiMR register = 1 (2 stop bits)
- UiIRS bit in UiC1 register = 0 (an interrupt request is generated when transmit buffer is empty)

TC=16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of UiBRG count source (f1, f8, f32)
fEXT: Frequency of UiBRG count source (external clock)
n: Setting value to UiBRG register
i = 0 to 1

Figure 15.10 Transmit Timing in UART Mode

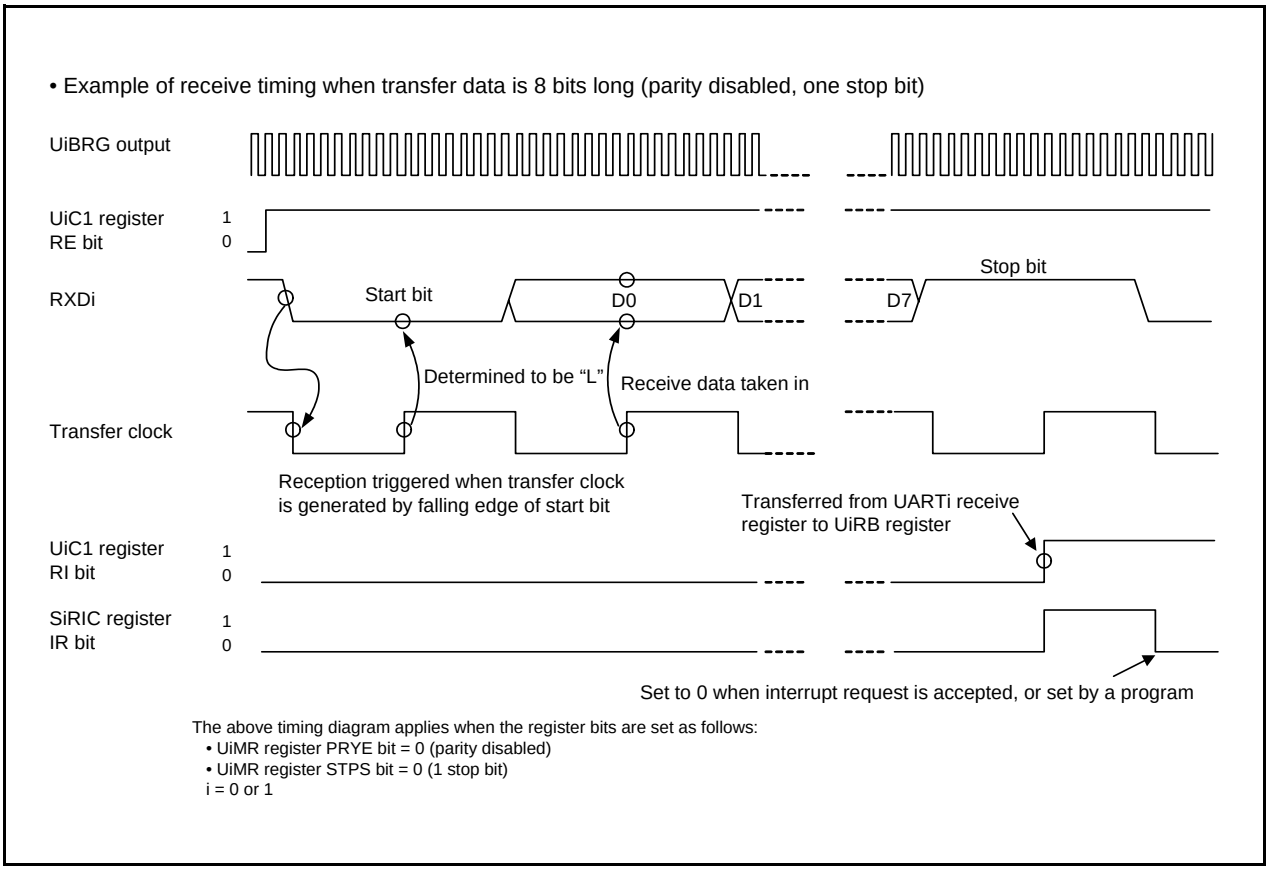


Figure 15.11 Receive Timing Example in UART Mode

15.2.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the UiBRG (i = 0 or 1) register.

UART mode

• Internal clock selected

$$\text{UiBRG register setting value} = \frac{fj}{\text{Bit Rate} \times 16} - 1$$

Fj: Count source frequency of the UiBRG register (f1, f8, or f32)

• External clock selected

$$\text{UiBRG register setting value} = \frac{fEXT}{\text{Bit Rate} \times 16} - 1$$

fEXT: Count source frequency of the UiBRG register (external clock)

i = 0 or 1

Figure 15.12 Calculation Formula of UiBRG (i = 0 or 1) Register Setting Value

Table 15.7 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	UiBRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz(1)			System Clock = 8 MHz		
		UiBRG Setting Value	Actual Time (bps)	Setting Error (%)	UiBRG Setting Value	Actual Time (bps)	Setting Error (%)	UiBRG Setting Value	Actual Time (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	-1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	-1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	-3.55
115200	f1	10 (0Ah)	113636.36	-1.36	9 (09h)	115200.00	0.00	–	–	–

i = 0 or 1

NOTE:

1. For the high-speed on-chip oscillator, the correction value in the FRA7 register should be written into the FRA1 register.
   This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-2 mode). For the precision of the high-speed on-chip oscillator, refer to **20. Electrical Characteristics**.

15.3 Notes on Serial Interface

- When reading data from the UiRB (i = 0 or 1) register either in the clock synchronous serial I/O mode or in the clock asynchronous serial I/O mode. Ensure the data is read in 16-bit units. When the high-order byte of the UiRB register is read, bits PER and FER in the UiRB register and the RI bit in the UiC1 register are set to 0. To check receive errors, read the UiRB register and then use the read data.

Example (when reading receive buffer register):

```
MOV.W    00A6H,R0    ; Read the U0RB register
```

- When writing data to the UiTB register in the clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first then the low-order byte, in 8-bit units.

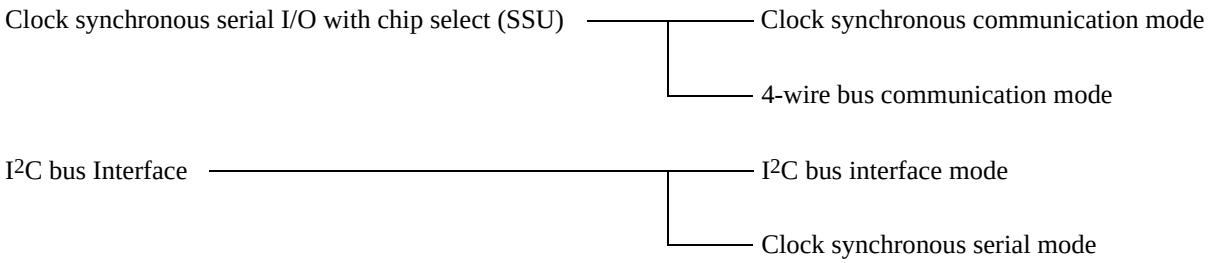
Example (when reading transmit buffer register):

```
MOV.B    #XXH,00A3H  ; Write the high-order byte of U0TB register
MOV.B    #XXH,00A2H  ; Write the low-order byte of U0TB register
```

16. Clock Synchronous Serial Interface

The clock synchronous serial interface is configured as follows.

Clock synchronous serial interface



The clock synchronous serial interface uses the registers at addresses 00B8h to 00BFh. Registers, bits, symbols, and functions vary even for the same addresses depending on the mode. Refer to the register diagrams of each function for details.
Also, the differences between clock synchronous communication mode and clock synchronous serial mode are the options of the transfer clock, clock output format, and data output format.

16.1 Mode Selection

The clock synchronous serial interface has four modes.
Table 16.1lists the Mode Selections. Refer to **16.2 Clock Synchronous Serial I/O with Chip Select (SSU)** and the sections that follow for details of each mode.

Table 16.1 Mode Selections

IICSEL Bit in PMR Register	Bit 7 in 00B8h (ICE Bit in ICCR1 Register)	Bit 0 in 00BDh (SSUMS Bit in SSMR2 Register, FS Bit in SAR Register)	Function	Mode
0	0	0	Clock synchronous serial I/O with chip select	Clock synchronous communication mode
0	0	1		4-wire bus communication mode
1	1	0	I2C bus interface	I2C bus interface mode
1	1	1		Clock synchronous serial mode

16.2 Clock Synchronous Serial I/O with Chip Select (SSU)

Clock synchronous serial I/O with chip select supports clock synchronous serial data communication.
Table 16.2 lists the Clock Synchronous Serial I/O with Chip Select Specifications, and Figure 16.1 shows a Block Diagram of Clock Synchronous Serial I/O with Chip Select. Figures 16.2 to 16.9 show Clock Synchronous Serial I/O with Chip Select Associated Registers.

Table 16.2 Clock Synchronous Serial I/O with Chip Select Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 bits Continuous transmission and reception of serial data are supported since both transmitter and receiver have buffer structures.
Operating modes	• Clock synchronous communication mode • 4-wire bus communication mode (including bidirectional communication)
Master/slave device	Selectable
I/O pins	SSCK (I/O): Clock I/O pin SSI (I/O): Data I/O pin $\overline{\text{SSO}}$ (I/O): Data I/O pin $\overline{\text{SCS}}$ (I/O): Chip-select I/O pin
Transfer clocks	• When the MSS bit in the SSCRH register is set to 0 (operates as slave device), external clock is selected (input from SSCK pin). • When the MSS bit in the SSCRH register is set to 1 (operates as master device), internal clock (selectable among f1/256, f1/128, f1/64, f1/32, f1/16, f1/8 and f1/4, output from SSCK pin) is selected. • Clock polarity and phase of SSCK can be selected.
Receive error detection	• Overrun error Overrun error occurs during reception and completes in error. While the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and when next serial data receive is completed, the ORER bit is set to 1.
Multimaster error detection	• Conflict error When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operates as master device) and when starting a serial communication, the CE bit in the SSSR register is set to 1 if “L” applies to the $\overline{\text{SCS}}$ pin input. When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operates as slave device) and the $\overline{\text{SCS}}$ pin input changes state from “L” to “H”, the CE bit in the SSSR register is set to 1.
Interrupt requests	5 interrupt requests (transmit-end, transmit-data-empty, receive-data-full, overrun error, and conflict error).(1)
Select functions	• Data transfer direction Selects MSB-first or LSB-first • SSCK clock polarity Selects “L” or “H” level when clock stops • SSCK clock phase Selects edge of data change and data download

NOTE:
1. Clock synchronous serial I/O with chip select has only one interrupt vector table.

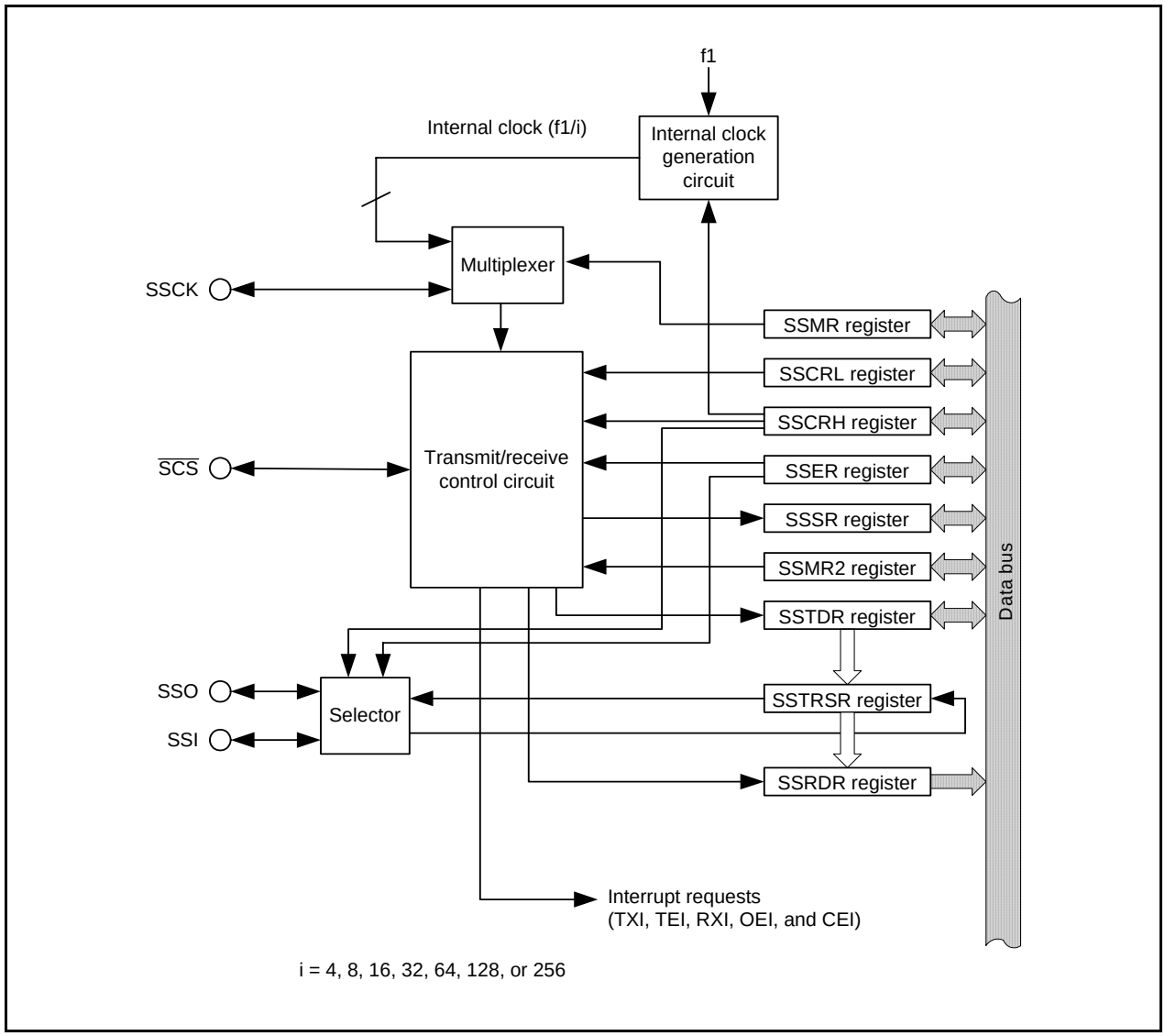
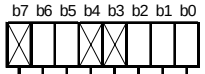


Figure 16.1 Block Diagram of Clock Synchronous Serial I/O with Chip Select

SS Control Register H



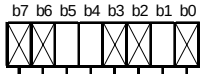
Symbol	Address	After Reset
SSCRH	00B8h	00h

Bit Symbol	Bit Name	Function	RW
CKS0	Transfer clock rate select bits(1)	b2 b1 b0 0 0 0 : f1/256 0 0 1 : f1/128 0 1 0 : f1/64 0 1 1 : f1/32 1 0 0 : f1/16 1 0 1 : f1/8 1 1 0 : f1/4 1 1 1 : Do not set.	RW
CKS1			RW
CKS2			RW
— (b4-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
MSS	Master/slave device select bit(2)	0 : Operates as slave device 1 : Operates as master device	RW
RSSTP	Receive single stop bit(3)	0 : Maintains receive operation after receiving 1 byte of data 1 : Completes receive operation after receiving 1 byte of data	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. The set clock is used when the internal clock is selected.
2. The SSCK pin functions as the transfer clock output pin when the MSS bit is set to 1 (operates as master device). The MSS bit is set to 0 (operates as slave device) when the CE bit in the SSSR register is set to 1 (conflict error occurs).
3. The RSSTP bit is disabled when the MSS bit is set to 0 (operates as slave device).

Figure 16.2 SSCRH Register

SS Control Register L



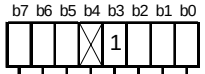
Symbol	Address	After Reset
SSCRL	00B9h	01111101b

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
SRES	Clock synchronous serial I/O with chip select control part reset bit	When this bit is set to 1, the clock synchronous serial I/O with chip select control block and SSTRSR register are reset. The values of the registers(1) in the clock synchronous serial I/O with chip select register are maintained.	RW
— (b3-b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
SOLP	SOL write protect bit(2)	The output level can be changed by the SOL bit when this bit is set to 0. The SOLP bit remains unchanged even if 1 is written to it. When read, the content is 1.	RW
SOL	Serial data output value setting bit	When read 0 : The serial data output is set to “L”. 1 : The serial data output is set to “H”. When written(2,3) 0 : The data output is “L” after the serial data output. 1 : The data output is “H” after the serial data output.	RW
— (b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Registers SSCRH, SSCRL, SSMR, SSER, SSSR, SSMR2, SSTDR, and SSRDR.
2. The data output after serial data is output can be changed by writing to the SOL bit before or after transfer. When writing to the SOL bit, set the SOLP bit to 0 and the SOL bit to 0 or 1 simultaneously by the MOV instruction.
3. Do not write to the SOL bit during data transfer.

Figure 16.3 SSCRL Register

SS Mode Register



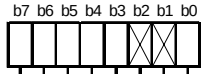
Symbol	Address	After Reset
SSMR	00BAh	00011000b

Bit Symbol	Bit Name	Function	RW
BC0	Bits counter 2 to 0	b2 b1 b0 0 0 0 : 8 bits left 0 0 1 : 1 bit left 0 1 0 : 2 bits left 0 1 1 : 3 bits left 1 0 0 : 4 bits left 1 0 1 : 5 bits left 1 1 0 : 6 bits left 1 1 1 : 7 bits left	RO
BC1			RO
BC2			RO
— (b3)	Reserved bit	Set to 1. When read, the content is 1.	RW
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
CPHS	SSCK clock phase select bit(1)	0 : Change data at odd edge (Download data at even edge) 1 : Change data at even edge (Download data at odd edge)	RW
CPOS	SSCK clock polarity select bit(1)	0 : “H” when clock stops 1 : “L” when clock stops	RW
MLS	MSB first/LSB first select bit	0 : Transfers data MSB first 1 : Transfers data LSB first	RW

NOTE:
1. Refer to **16.2.1.1 Association between Transfer Clock Polarity, Phase, and Data** for the settings of the CPHS and CPOS bits.

Figure 16.4 SSMR Register

SS Enable Register

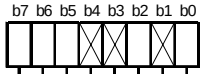


Symbol	Address	After Reset
SSER	00BBh	00h

Bit Symbol	Bit Name	Function	RW
CEIE	Conflict error interrupt enable bit	0 : Disables conflict error interrupt request 1 : Enables conflict error interrupt request	RW
— (b2-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
RE	Receive enable bit	0 : Disables receive 1 : Enables receive	RW
TE	Transmit enable bit	0 : Disables transmit 1 : Enables transmit	RW
RIE	Receive interrupt enable bit	0 : Disables receive data full and overrun error interrupt request 1 : Enables receive data full and overrun error interrupt request	RW
TEIE	Transmit end interrupt enable bit	0 : Disables transmit end interrupt request 1 : Enables transmit end interrupt request	RW
TIE	Transmit interrupt enable bit	0 : Disables transmit data empty interrupt request 1 : Enables transmit data empty interrupt request	RW

Figure 16.5 SSER Register

SS Status Register(7)



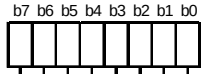
Symbol	Address	After Reset
SSSR	00BCh	00h

Bit Symbol	Bit Name	Function	RW
CE	Conflict error flag(1)	0 : No conflict errors generated 1 : Conflict errors generated(2)	RW
— (b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
ORER	Overrun error flag(1)	0 : No overrun errors generated 1 : Overrun errors generated(3)	RW
— (b4-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
RDRF	Receive data register full (1,4)	0 : No data in SSRDR register 1 : Data in SSRDR register	RW
TEND	Transmit end(1, 5)	0 : The TDRE bit is set to 0 when transmitting the last bit of transmit data 1 : The TDRE bit is set to 1 when transmitting the last bit of transmit data	RW
TDRE	Transmit data empty(1, 5, 6)	0 : Data is not transferred from registers SSTDR to SSTRSR 1 : Data is transferred from registers SSTDR to SSTRSR	RW

NOTES:
1. Writing 1 to CE, ORER, RDRF, TEND, or TDRE bits invalid. To set any of these bits to 0, first read 1 then write 0.
2. When the serial communication is started while the SSUMS bit in the SSMR2 register is set to 1 (four-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operates as master device), the CE bit is set to 1 if "L" is applied to the $\overline{SCS}$ pin input. Refer to **16.2.7 $\overline{SCS}$ Pin Control and Arbitration** for more information.
   When the SSUMS bit in the SSMR2 register is set to 1 (four-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operates as slave device) and the $\overline{SCS}$ pin input changes the level from "L" to "H" during transfer, the CE bit is set to 1.
3. Indicates when overrun errors occur and receive completes by error reception. If the next serial data receive operation is completed while the RDRF bit is set to 1 (data in the SSRDR register), the ORER bit is set to 1. After the ORER bit is set to 1 (overrun error), transmit and receive operations are disabled while the bit remains 1.
4. The RDRF bit is set to 0 when reading out the data from the SSRDR register.
5. Bits TEND and TDRE are set to 0 when writing data to the SSTDR register.
6. The TDRE bit is set to 1 when the TE bit in the SSER register is set to 1 (transmit enabled).
7. When accessing the SSSR register continuously, insert one or more NOP instructions between the instructions to access it.

Figure 16.6 SSSR Register

SS Mode Register 2



Symbol	Address	After Reset
SSMR2	00BDh	00h

Bit Symbol	Bit Name	Function	RW
SSUMS	Clock synchronous serial I/O with chip select mode select bit(1)	0 : Clock synchronous communication mode 1 : Four-wire bus communication mode	RW
CSOS	$\overline{SCS}$ pin open drain output select bit	0 : CMOS output 1 : N-channel open drain output	RW
SOOS	Serial data pin open output drain select bit(1)	0 : CMOS output(5) 1 : N-channel open drain output	RW
SCKOS	SSCK pin open drain output select bit	0 : CMOS output 1 : N-channel open drain output	RW
CSS0	$\overline{SCS}$ pin select bits(2)	b5 b4 0 0 : Functions as port 0 1 : Functions as $\overline{SCS}$ input pin 1 0 : Functions as $\overline{SCS}$ output pin(3) 1 1 : Functions as $\overline{SCS}$ output pin(3)	RW
CSS1			RW
SCKS	SSCK pin select bit	0 : Functions as port 1 : Functions as serial clock pin	RW
BIDE	Bidirectional mode enable bit(1, 4)	0 : Standard mode (communication using 2 pins of data input and data output) 1 : Bidirectional mode (communication using 1 pin of data input and data output)	RW

NOTES:
1. Refer to **16.2.2.1 Association between Data I/O Pins and SS Shift Register** for information on combinations of data I/O pins.
2. The $\overline{SCS}$ pin functions as a port, regardless of the values of bits CSS0 and CSS1 when the SSUMS bit is set to 0 (clock synchronous communication mode).
3. This bit functions as the SCS input pin before starting transfer.
4. The BIDE bit is disabled when the SSUMS bit is set to 0 (clock synchronous communication mode).
5. The SSI pin and SSO pin corresponding port direction bits are set to 0 (input mode) when the SOOS bit is set to 0 (CMOS output).

Figure 16.7 SSMR2 Register

SS Transmit Data Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
SSTDR	00BEh	FFh

Function	RW
Store the transmit data. The stored transmit data is transferred to the SSTRSR register and transmission is started when it is detected that the SSTRSR register is empty. When the next transmit data is written to the SSTDR register during the data transmission from the SSTRSR register, the data can be transmitted continuously. When the MLS bit in the SSMR register is set to 1 (transfer data with LSB-first), the data in which MSB and LSB are reversed is read, after writing to the SSTDR register.	RW

SS Receive Data Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
SSRDR	00BFh	FFh

Function	RW
Store the receive data.(1) The receive data is transferred to the SSRDR register and the receive operation is completed when 1 byte of data has been received by the SSTRSR register. At this time, the next receive operation is possible. Continuous reception is possible using registers SSTRSR and SSRDR.	RO

NOTE:
1. The SSRDR register retains the data received before an overrun error occurs (ORER bit in the SSSR register set to 1 (overrun error)). When an overrun error occurs, the receive data may contain errors and therefore should be discarded.

Figure 16.8 Registers SSTDR and SSRDR

Port Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
	0	0		0	0	0	0

Symbol	Address	After Reset
PMR	00F8h	00h

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Reserved bits	Set to 0.	—
U1PINSEL	Port CLK1/TXD1/RXD1 switch bit	0 : I/O ports P6_5, P6_6, P6_7 1 : CLK1, TXD1, RXD1	RW
— (b6-b5)	Reserved bits	Set to 0.	—
IICSEL	SSU / I^2C bus switch bit	0 : Selects SSU function 1 : Selects I^2C bus function	RW

Figure 16.9 PMR Register

16.2.1 Transfer Clock

The transfer clock can be selected from among seven internal clocks (f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, and f1/4) and an external clock.

When using clock synchronous serial I/O with chip select, set the SCKS bit in the SSMR2 register to 1 and select the SSCK pin as the serial clock pin.

When the MSS bit in the SSCRH register is set to 1 (operates as master device), an internal clock can be selected and the SSCK pin functions as output. When transfer is started, the SSCK pin outputs clocks of the transfer rate selected by bits CKS0 to CKS2 in the SSCRH register.

When the MSS bit in the SSCRH register is set to 0 (operates as slave device), an external clock can be selected and the SSCK pin functions as input.

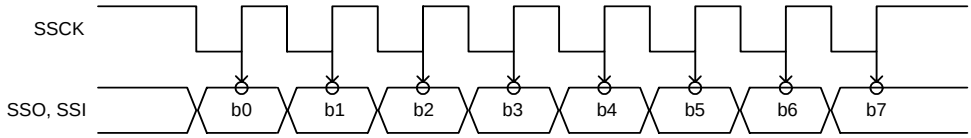
16.2.1.1 Association between Transfer Clock Polarity, Phase, and Data

The association between the transfer clock polarity, phase and data changes according to the combination of the SSUMS bit in the SSMR2 register and bits CPHS and CPOS in the SSMR register.

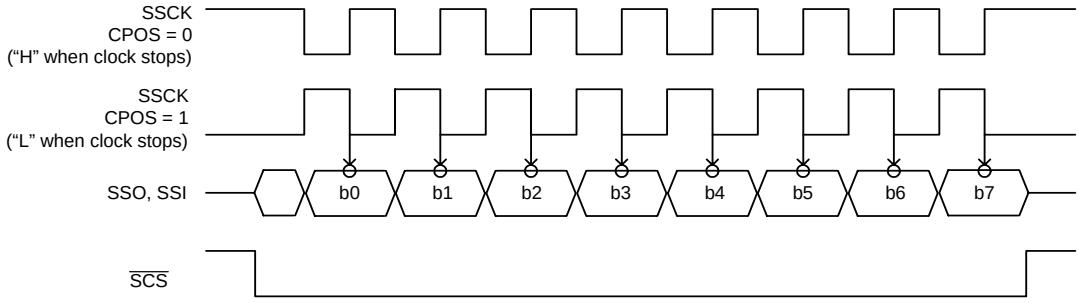
Figure 16.10 shows the Association between Transfer Clock Polarity, Phase, and Transfer Data.

Also, the MSB-first transfer or LSB-first transfer can be selected by setting the MLS bit in the SSMR register. When the MLS bit is set to 1, transfer is started from the LSB and proceeds to the MSB. When the MLS bit is set to 0, transfer is started from the MSB and proceeds to the LSB.

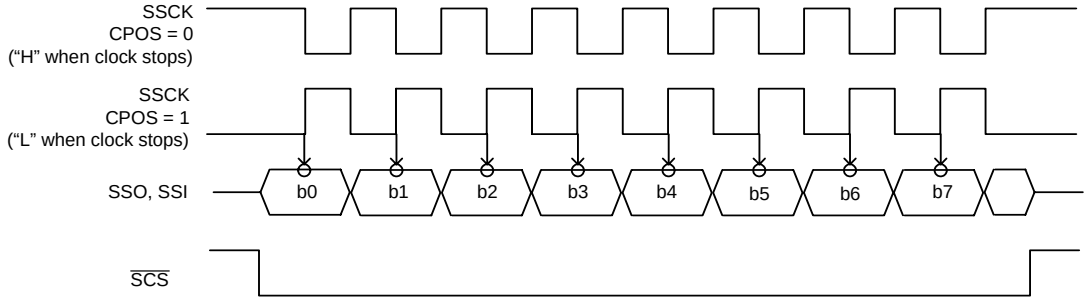
• SSUMS = 0 (clock synchronous communication mode), CPHS bit = 0 (data change at odd edge), and CPOS bit = 0 (“H” when clock stops)



• SSUMS = 1 (4-wire bus communication mode) and CPHS = 0 (data change at odd edge)



• SSUMS = 1 (4-wire bus communication mode) and CPHS = 1 (data download at odd edge)



CPHS and CPOS: Bits in SSMR register, SSUMS: Bits in SSMR2 register

Figure 16.10 Association between Transfer Clock Polarity, Phase, and Transfer Data

16.2.2 SS Shift Register (SSTRSR)

The SSTRSR register is a shift register for transmitting and receiving serial data.
When transmit data is transferred from the SSTDR register to the SSTRSR register and the MLS bit in the SSMR register is set to 0 (MSB-first), the bit 0 in the SSTDR register is transferred to bit 0 in the SSTRSR register. When the MLS bit is set to 1 (LSB-first), bit 7 in the SSTDR register is transferred to bit 0 in the SSTRSR register.

16.2.2.1 Association between Data I/O Pins and SS Shift Register

The connection between the data I/O pins and SSTRSR register (SS shift register) changes according to a combination of the MSS bit in the SSCRH register and the SSUMS bit in the SSMR2 register. The connection also changes according to the BIDE bit in the SSMR2 register.
Figure 16.11 shows the Association between Data I/O Pins and SSTRSR Register.

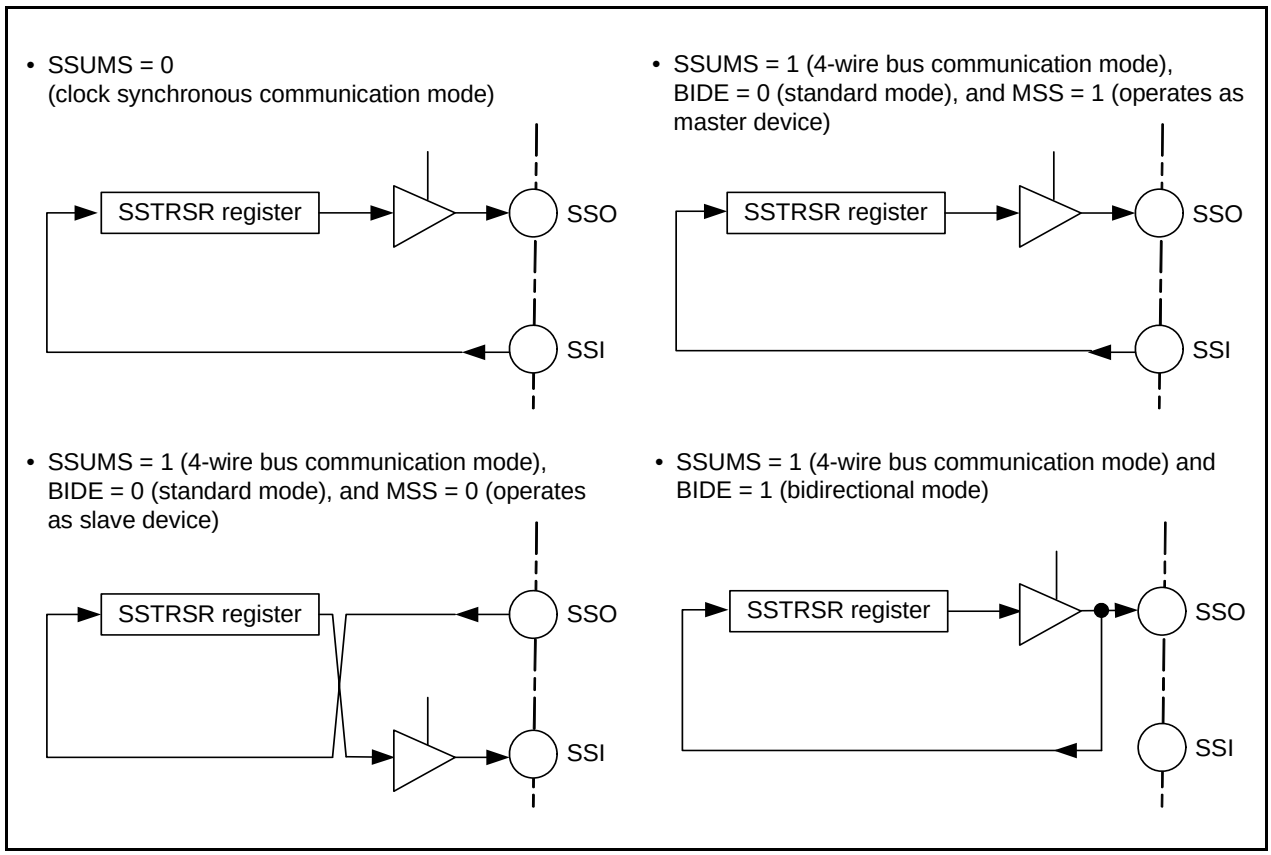


Figure 16.11 Association between Data I/O Pins and SSTRSR Register

16.2.3 Interrupt Requests

Clock synchronous serial I/O with chip select has five interrupt requests: transmit data empty, transmit end, receive data full, overrun error, and conflict error. Since these interrupt requests are assigned to the clock synchronous serial I/O with chip select interrupt vector table, determining interrupt sources by flags is required. Table 16.3 shows the Clock Synchronous Serial I/O with Chip Select Interrupt Requests.

Table 16.3 Clock Synchronous Serial I/O with Chip Select Interrupt Requests

Interrupt Request	Abbreviation	Generation Condition
Transmit data empty	TXI	TIE = 1, TDRE = 1
Transmit end	TEI	TEIE = 1, TEND = 1
Receive data full	RXI	RIE = 1, RDRF = 1
Overrun error	OEI	RIE = 1, ORER = 1
Conflict error	CEI	CEIE = 1, CE = 1

CEIE, RIE, TEIE and TIE: Bits in SSER register
ORER, RDRF, TEND and TDRE: Bits in SSSR register

If the generation conditions in Table 16.3 are met, a clock synchronous serial I/O with chip select interrupt request is generated. Set each interrupt source to 0 by a clock synchronous serial I/O with chip select interrupt routine.

However, the TDRE and TEND bits are automatically set to 0 by writing transmit data to the SSTDR register and the RDRF bit is automatically set to 0 by reading the SSRDR register. In particular, the TDRE bit is set to 1 (data transmitted from registers SSTDR to SSTRSR) at the same time transmit data is written to the SSTDR register. Setting the TDRE bit to 0 (data not transmitted from registers SSTDR to SSTRSR) can cause an additional byte of data to be transmitted.

16.2.4 Communication Modes and Pin Functions

Clock synchronous serial I/O with chip select switches the functions of the I/O pins in each communication mode according to the setting of the MSS bit in the SSCRH register and bits RE and TE in the SSER register. Table 16.4 shows the Association between Communication Modes and I/O Pins.

Table 16.4 Association between Communication Modes and I/O Pins

Communication Mode	Bit Setting					Pin State		
	SSUMS	BIDE	MSS	TE	RE	SSI	SSO	SSCK
Clock synchronous communication mode	0	Disabled	0	0	1	Input	–(1)	Input
				1	0	–(1)	Output	Input
					1	Input	Output	Input
			1	0	1	Input	–(1)	Output
				1	0	–(1)	Output	Output
					1	Input	Output	Output
4-wire bus communication mode	1	0	0	0	1	–(1)	Input	Input
				1	0	Output	–(1)	Input
					1	Output	Input	Input
			1	0	1	Input	–(1)	Output
				1	0	–(1)	Output	Output
					1	Input	Output	Output
4-wire bus (bidirectional) communication mode(2)	1	1	0	0	1	–(1)	Input	Input
				1	0	–(1)	Output	Input
			1	0	1	–(1)	Input	Output
				1	0	–(1)	Output	Output

NOTES:
1. This pin can be used as a programmable I/O port.
2. Do not set both bits TE and RE to 1 in 4-wire bus (bidirectional) communication mode.

SSUMS and BIDE: Bits in SSMR2 register
MSS: Bit in SSCRH register
TE and RE: Bits in SSER register

16.2.5 Clock Synchronous Communication Mode

16.2.5.1 Initialization in Clock Synchronous Communication Mode

Figure 16.12 shows Initialization in Clock Synchronous Communication Mode. To initialize, set the TE bit in the SSER register to 0 (transmit disabled) and the RE bit to 0 (receive disabled) before data transmission or reception.

Set the TE bit to 0 and the RE bit to 0 before changing the communication mode or format.

Setting the RE bit to 0 does not change the contents of flags RDRF and ORER or the contents of the SSRDR register.

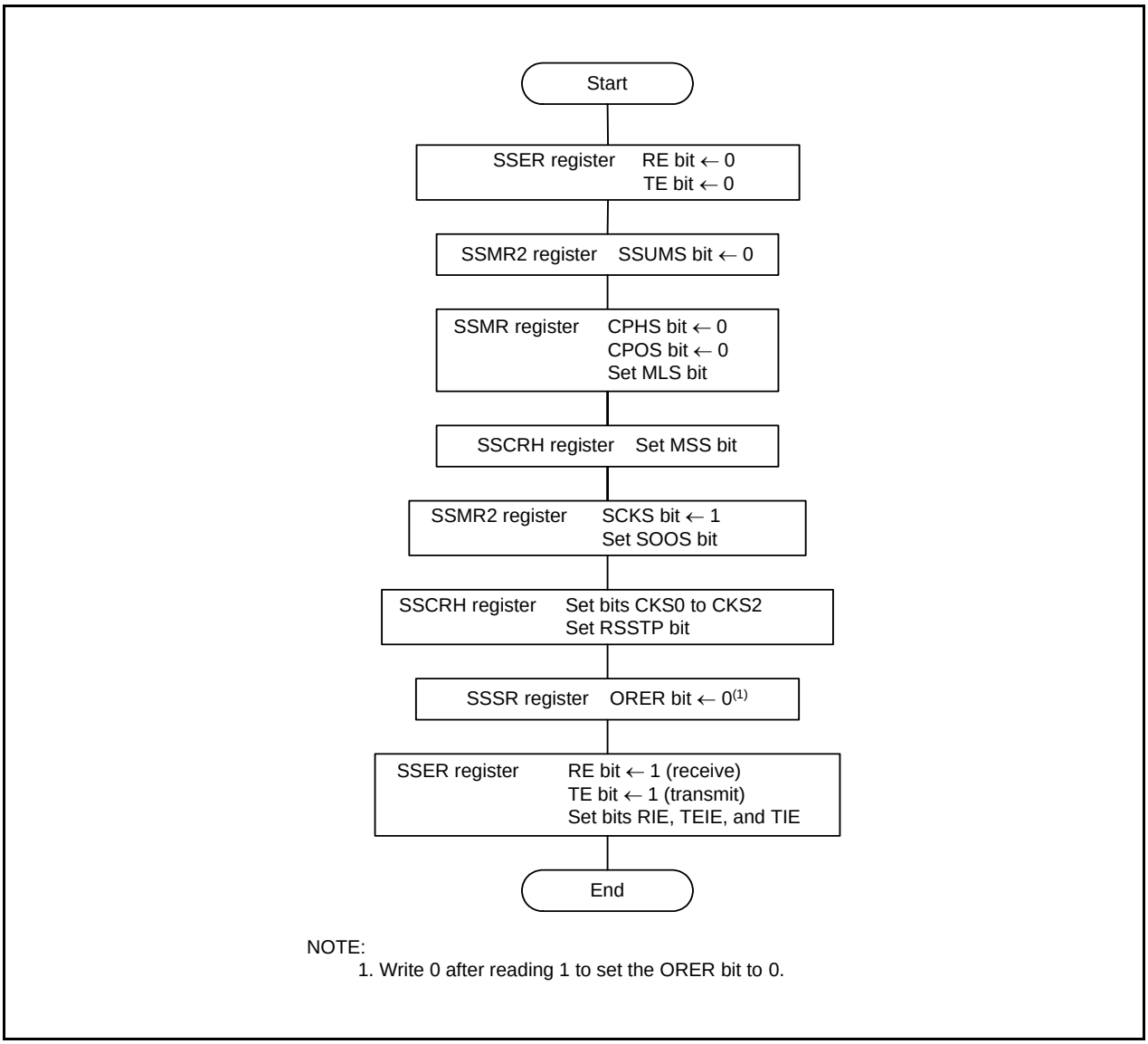


Figure 16.12 Initialization in Clock Synchronous Communication Mode

16.2.5.2 Data Transmission

Figure 16.13 shows an Example of Clock Synchronous Serial I/O with Chip Select Operation for Data Transmission (Clock Synchronous Communication Mode). During data transmission, the clock synchronous serial I/O with chip select operates as described below.

When clock synchronous serial I/O with chip select is set as a master device, it outputs a synchronous clock and data. When clock synchronous serial I/O with chip select is set as a slave device, it outputs data synchronized with the input clock.

When the TE bit is set to 1 (transmit enabled) before writing the transmit data to the SSTDR register, the TDRE bit is automatically set to 0 (data not transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR.

After the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1, the TXI interrupt request is generated. When one frame of data is transferred while the TDRE bit is set to 0, data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while the TDRE bit is set to 1, the TEND bit in the SSSR register is set to 1 (the TDRE bit is set to 1 when the last bit of the transmit data is transmitted) and the state is retained. The TEI interrupt request is generated when the TEIE bit in the SSER register is set to 1 (transmit-end interrupt request enabled). The SSCK pin is fixed “H” after transmit-end.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

Figure 16.14 shows a Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode).

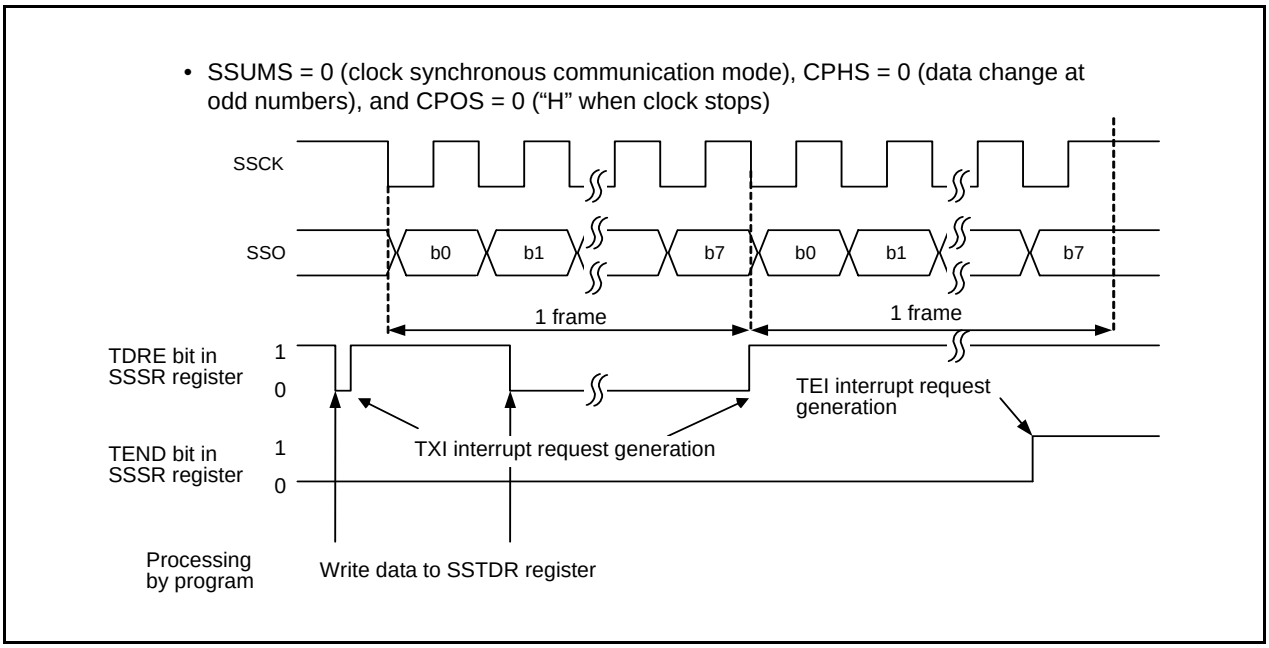
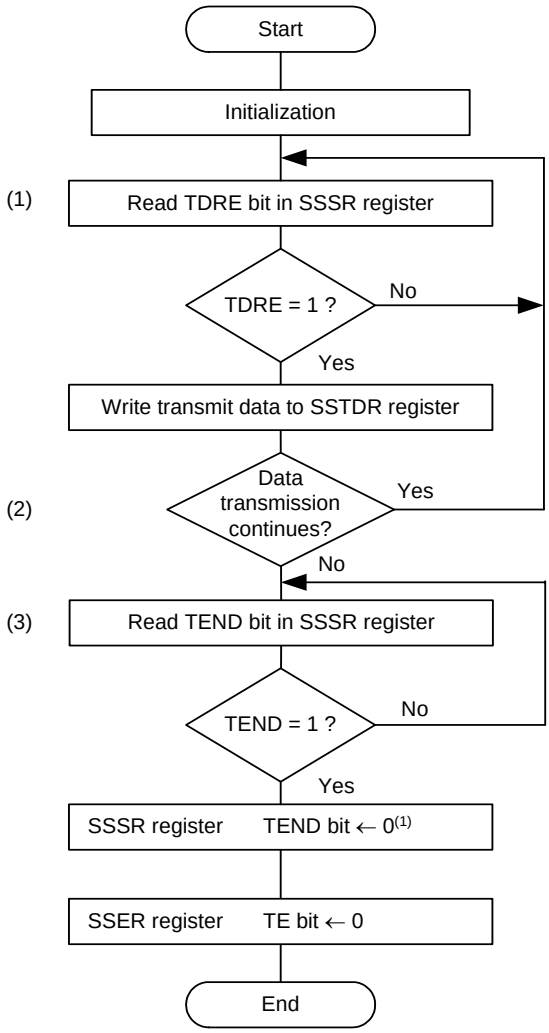


Figure 16.13 Example of Clock Synchronous Serial I/O with Chip Select Operation for Data Transmission (Clock Synchronous Communication Mode)



(1) After reading the SSSR register and confirming that the TDRE bit is set to 1, write the transmit data to the SSTDR register. When the transmit data is written to the SSTDR register, the TDRE bit is automatically set to 0.

(2) Determine whether data transmission continues.

(3) When data transmission is completed, the TEND bit is set to 1. Set the TEND bit to 0 and the TE bit to 0 and complete transmit mode.

NOTE:
1. Write 0 after reading 1 to set the TEND bit to 0.

Figure 16.14 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)

16.2.5.3 Data Reception

Figure 16.15 shows an Example of Clock Synchronous Serial I/O with Chip Select Operation for Data Reception (Clock Synchronous Communication Mode).

During data reception, clock synchronous serial I/O with chip select operates as described below. When the clock synchronous serial I/O with chip select is set as the master device, it outputs a synchronous clock and inputs data. When clock synchronous serial I/O with chip select is set as a slave device, it inputs data synchronized with the input clock.

When clock synchronous serial I/O with chip select is set as a master device, it outputs a receive clock and starts receiving by performing dummy read of the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled), the RXI interrupt request is generated. If the SSDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (after receiving 1 byte of data, the receive operation is completed). Clock synchronous serial I/O with chip select outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (receive disabled) and the RSSTP bit to 0 (receive operation is continued after receiving the 1 byte of data) and read the receive data. If the SSRDR register is read while the RE bit is set to 1 (receive enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, receive cannot be performed. Confirm that the ORER bit is set to 0 before restarting receive.

Figure 16.16 shows a Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode).

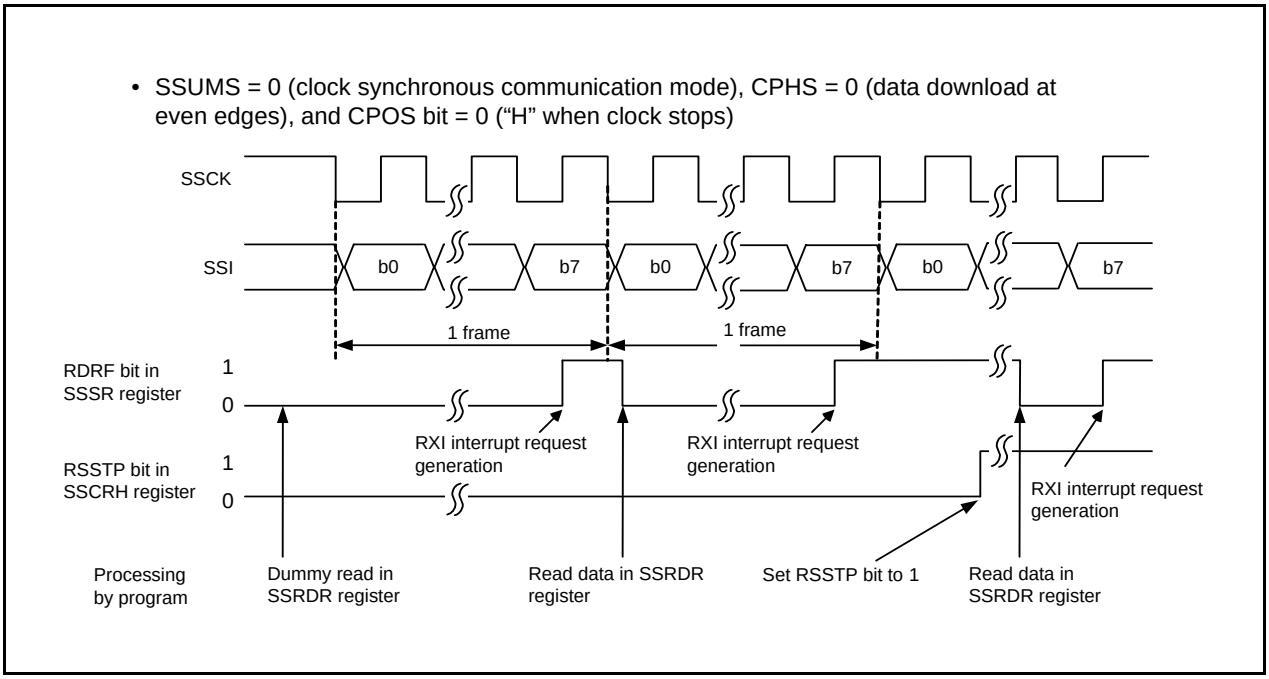


Figure 16.15 Example of Clock Synchronous Serial I/O with Chip Select Operation for Data Reception (Clock Synchronous Communication Mode)

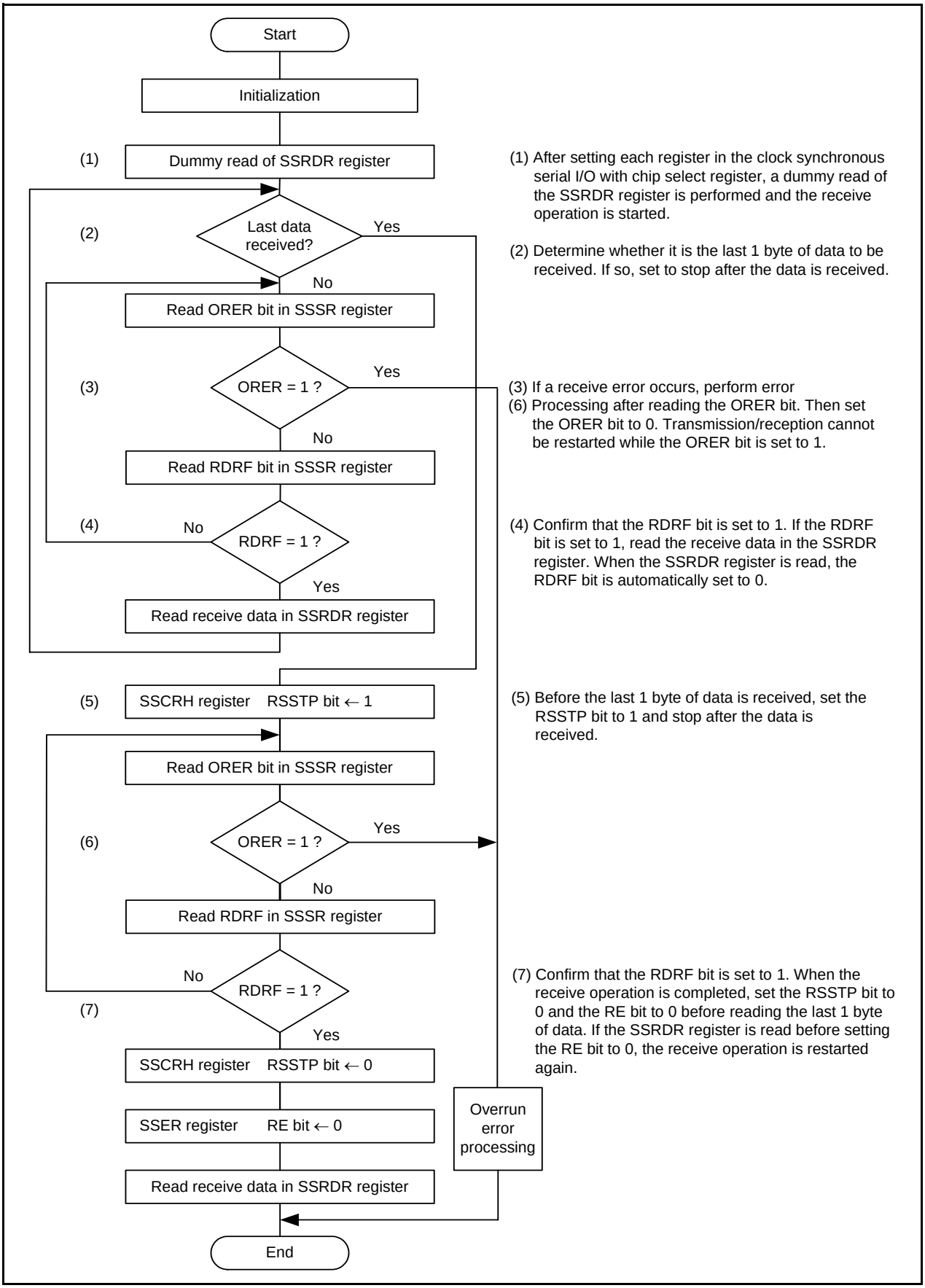


Figure 16.16 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)

16.2.5.4 Data Transmission/Reception

Data transmission/reception is an operation combining data transmission and reception which were described earlier. Transmission/reception is started by writing data to the SSTDR register.

When the 8th clock rises or the ORER bit is set to 1 (overrun error) while the TDRE bit is set to 1 (data is transferred from registers SSTDR to SSTRSR), the transmit/receive operation is stopped.

When switching from transmit mode (TE = 1) or receive mode (RE = 1) to transmit/receive mode (Te = RE = 1), set the TE bit to 0 and RE bit to 0 before switching. After confirming that the TEND bit is set to 0 (the TDRE bit is set to 0 when the last bit of the transmit data is transmitted), the RDRF bit is set to 0 (no data in the SSRDR register), and the ORER bit is set to 0 (no overrun error), set bits TE and RE to 1.

Figure 16.17 shows a Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode).

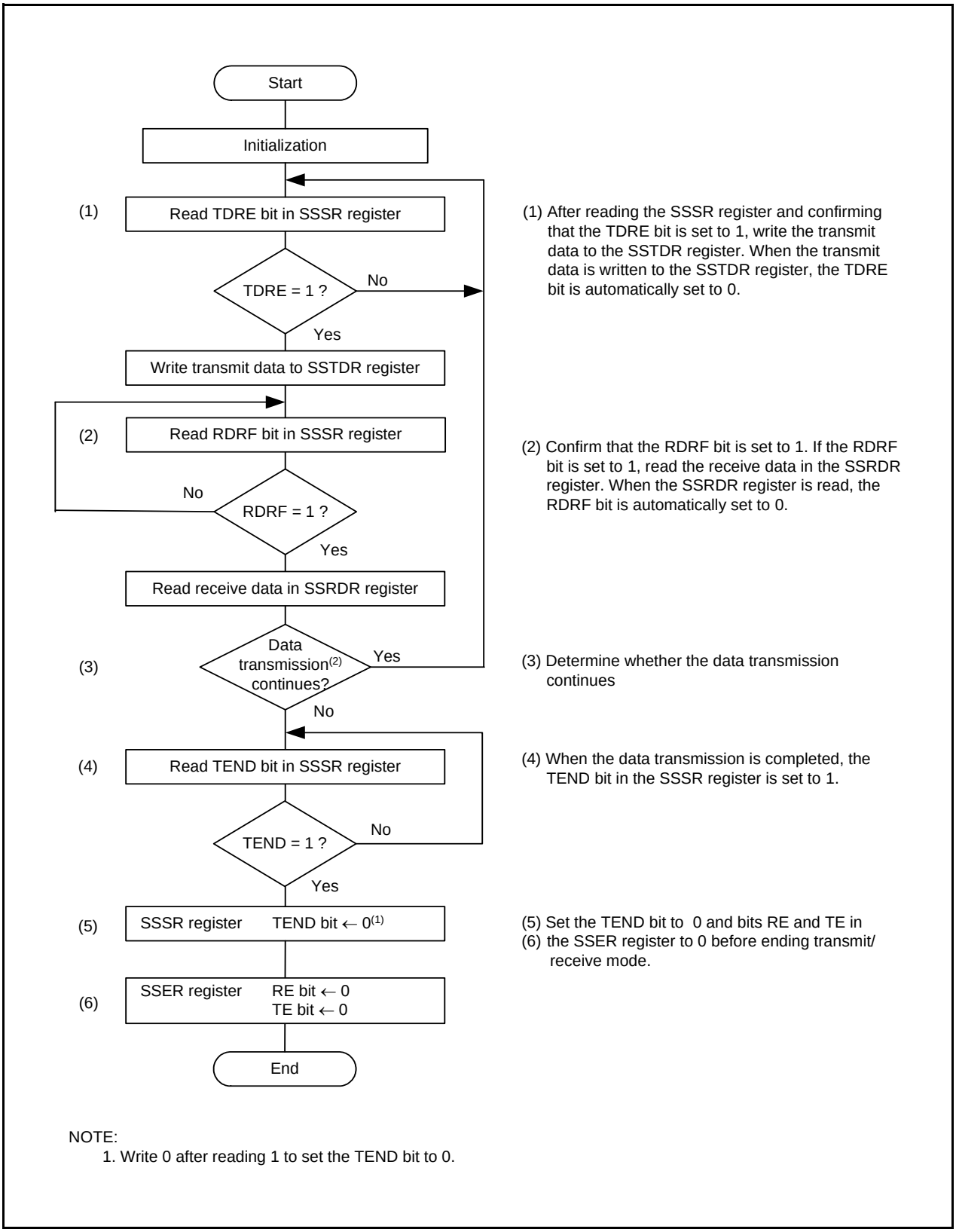


Figure 16.17 Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode)

16.2.6 Operation in 4-Wire Bus Communication Mode

In 4-wire bus communication mode, a 4-wire bus consisting of a clock line, a data input line, a data output line, and a chip select line is used for communication. This mode includes bidirectional mode in which the data input line and data output line function as a single pin.

The data input line and output line change according to the settings of the MSS bit in the SSCRH register and the BIDE bit in the SSMR2 register. For details, refer to **16.2.2.1 Association between Data I/O Pins and SS Shift Register**. In this mode, clock polarity, phase, and data settings are performed by bits CPOS and CPHS in the SSMR register. For details, refer to **16.2.1.1 Association between Transfer Clock Polarity, Phase, and Data**.

When this MCU is set as the master device, the chip select line controls output. When clock synchronous serial I/O with chip select is set as a slave device, the chip select line controls input. When it is set as the master device, the chip select line controls output of the $\overline{SCS}$ pin or controls output of a general port according to the setting of the CSS1 bit in the SSMR2 register. When the MCU is set as a slave device, the chip select line sets the $\overline{SCS}$ pin as an input pin by setting bits CSS1 and CSS0 in the SSMR2 register to 01b.

In 4-wire bus communication mode, the MLS bit in the SSMR register is set to 0 and communication is performed MSB-first.

16.2.6.1 Initialization in 4-Wire Bus Communication Mode

Figure 16.18 shows Initialization in 4-Wire Bus Communication Mode. Before the data transit/receive operation, set the TE bit in the SSER register to 0 (transmit disabled), the RE bit in the SSER register to 0 (receive disabled), and initialize the clock synchronous serial I/O with chip select.

To change the communication mode or format, set the TE bit to 0 and the RE bit to 0 before making the change. Setting the RE bit to 0 does not change the settings of flags RDRF and ORER or the contents of the SSRDR register.

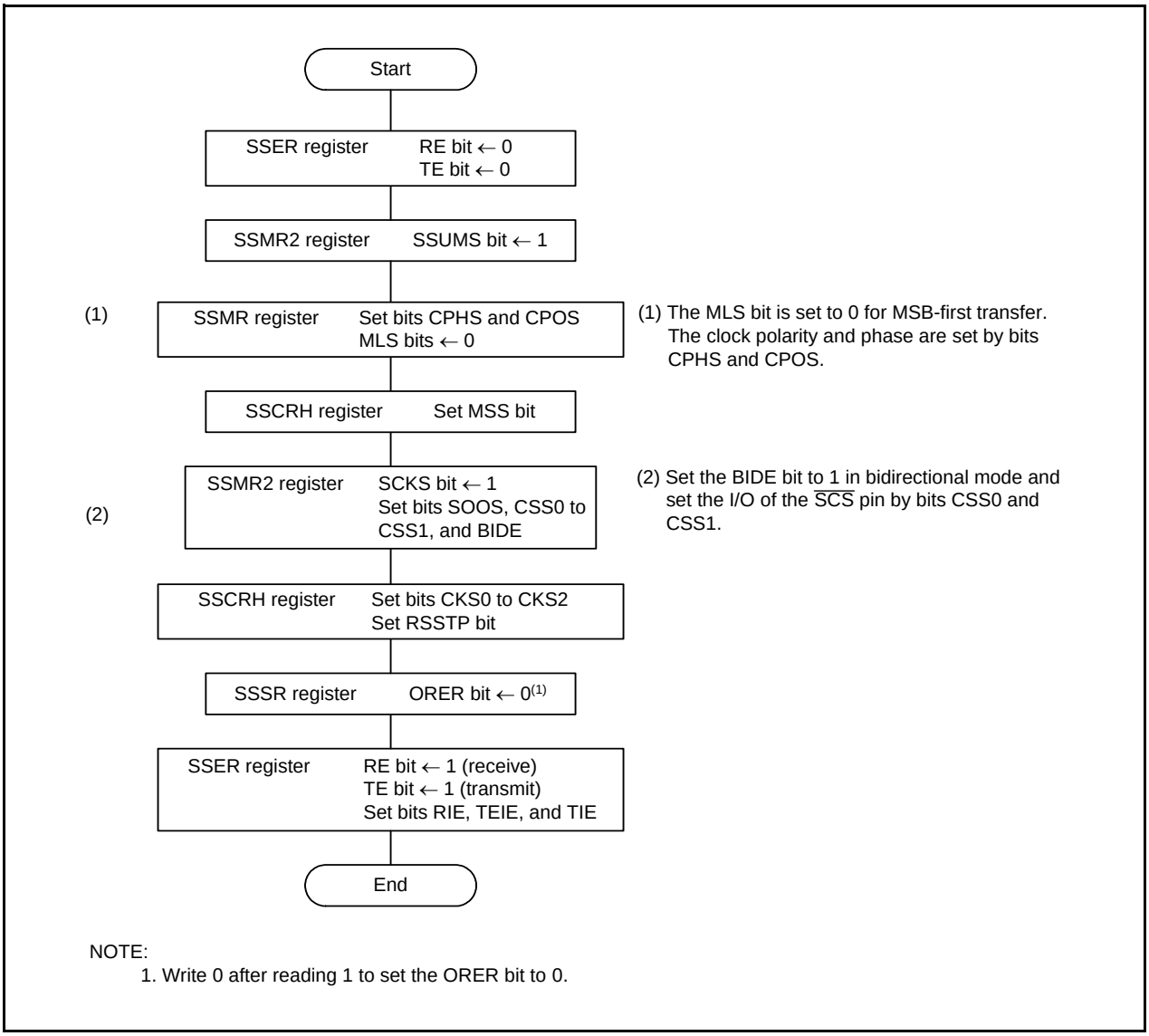


Figure 16.18 Initialization in 4-Wire Bus Communication Mode

16.2.6.2 Data Transmission

Figure 16.19 shows an Example of Clock Synchronous Serial I/O with Chip Select Operation during Data Transmission (4-Wire Bus Communication Mode). During the data transmit operation, clock synchronous serial I/O with chip select operates as described below.

When the MCU is set as the master device, it outputs a synchronous clock and data. When the MCU is set as a slave device, it outputs data in synchronization with the input clock while the $\overline{SCS}$ pin is “L”.

When the transmit data is written to the SSTDR register after setting the TE bit to 1 (transmit enabled), the TDRE bit is automatically set to 0 (data has not been transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR. After the TDRE bit is set to 1 (data is transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1, a TXI interrupt request is generated.

After 1 frame of data is transferred while the TDRE bit is set to 0, the data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while TDRE is set to 1, TEND in the SSSR register is set to 1 (when the last bit of the transmit data is transmitted, the TDRE bit is set to 1) and the state is retained. If the TEIE bit in the SSER register is set to 1 (transmit-end interrupt requests enabled), a TEI interrupt request is generated. The SSCK pin remains “H” after transmit-end and the $\overline{SCS}$ pin is held “H”. When transmitting continuously while the $\overline{SCS}$ pin is held “L”, write the next transmit data to the SSTDR register before transmitting the 8th bit.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

In contrast to the clock synchronous communication mode, the SSO pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in high-impedance state when operating as a master device and the SSI pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in “H” input state when operating as a slave device.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 16.14 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)**).

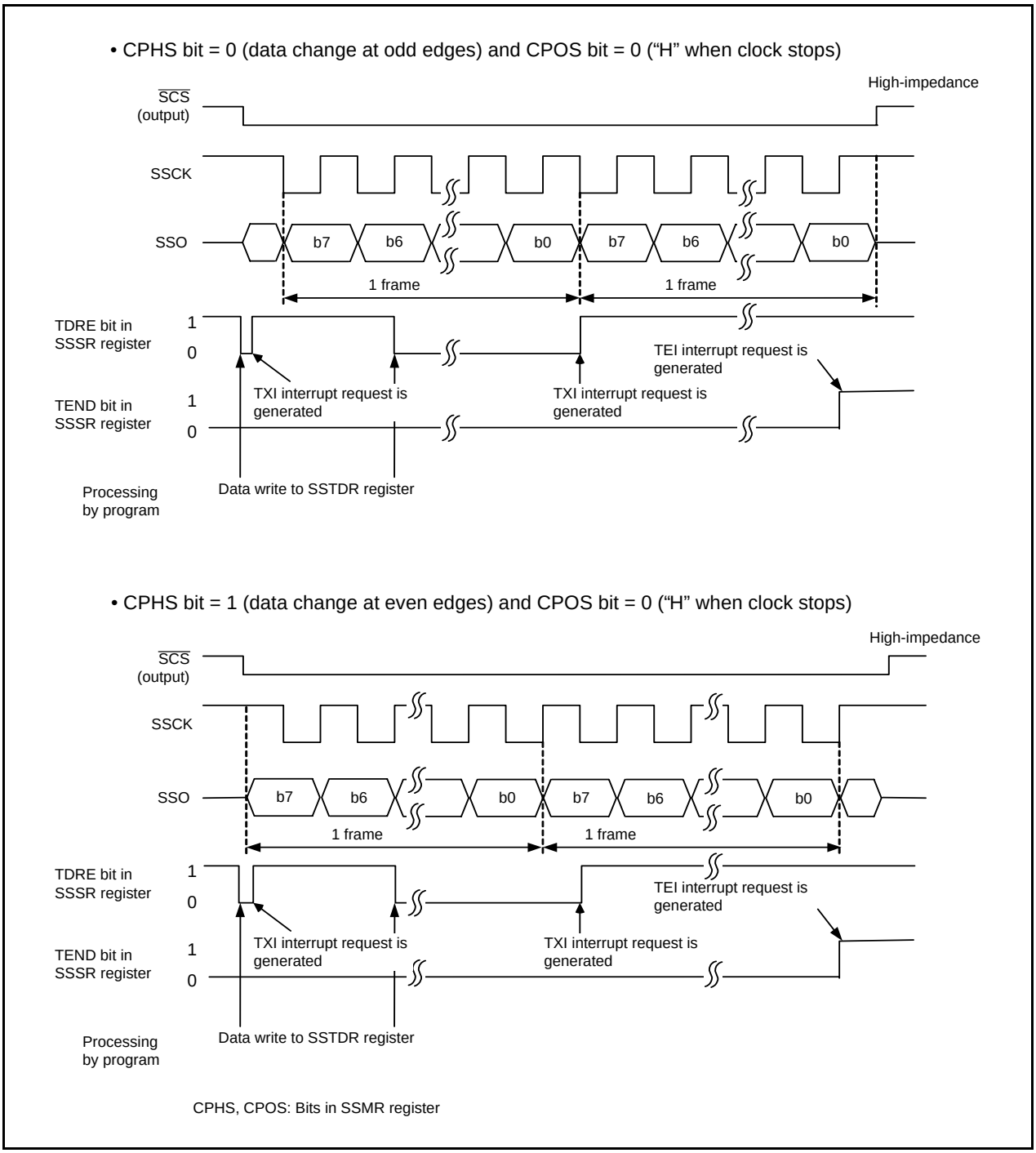


Figure 16.19 Example of Clock Synchronous Serial I/O with Chip Select Operation during Data Transmission (4-Wire Bus Communication Mode)

16.2.6.3 Data Reception

Figure 16.20 shows an Example of Clock Synchronous Serial I/O with Chip Select Operation during Data Reception (4-Wire Bus Communication Mode). During data reception, clock synchronous serial I/O with chip select operates as described below.

When the MCU is set as the master device, it outputs a synchronous clock and inputs data. When the MCU is set as a slave device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin receives “L” input. When the MCU is set as the master device, it outputs a receive clock and starts receiving by performing a dummy read of the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled), an RXI interrupt request is generated. When the SSRDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (after receiving 1-byte data, the receive operation is completed). Clock synchronous serial I/O with chip select outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (receive disabled) and the RSSTP bit to 0 (receive operation is continued after receiving 1-byte data) and read the receive data. When the SSRDR register is read while the RE bit is set to 1 (receive enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, reception cannot be performed. Confirm that the ORER bit is set to 0 before restarting reception.

The timing with which bits RDRF and ORER are set to 1 varies depending on the setting of the CPHS bit in the SSMR register. Figure 16.20 shows when bits RDRF and ORER are set to 1.

When the CPHS bit is set to 1 (data download at the odd edges), bits RDRF and ORER are set to 1 at some point during the frame.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 16.16 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)**).

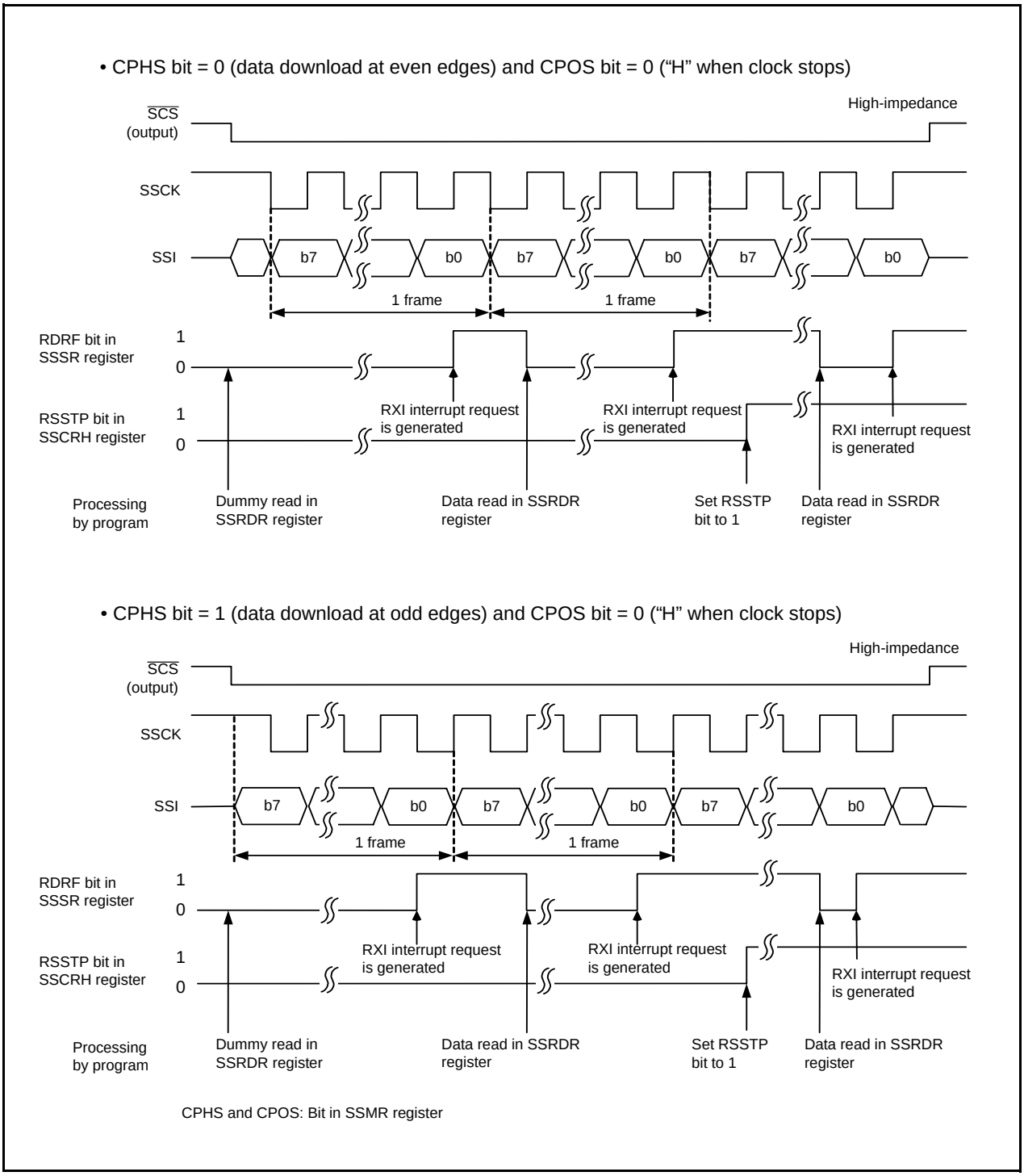


Figure 16.20 Example of Clock Synchronous Serial I/O with Chip Select Operation during Data Reception (4-Wire Bus Communication Mode)

16.2.7 $\overline{\text{SCS}}$ Pin Control and Arbitration

When setting the SSUMS bit in the SSMR2 register to 1 (4-wire bus communication mode) and the CSS1 bit in the SSMR2 register to 1 (functions as $\overline{\text{SCS}}$ output pin), set the MSS bit in the SSCRH register to 1 (operates as the master device) and check the arbitration of the $\overline{\text{SCS}}$ pin before starting serial transfer. If clock synchronous serial I/O with chip select detects that the synchronized internal $\overline{\text{SCS}}$ signal is held "L" in this period, the CE bit in the SSSR register is set to 1 (conflict error) and the MSS bit is automatically set to 0 (operates as a slave device).
Figure 16.21 shows the Arbitration Check Timing.

Future transmit operations are not performed while the CE bit is set to 1. Set the CE bit to 0 (no conflict error) before starting transmission.

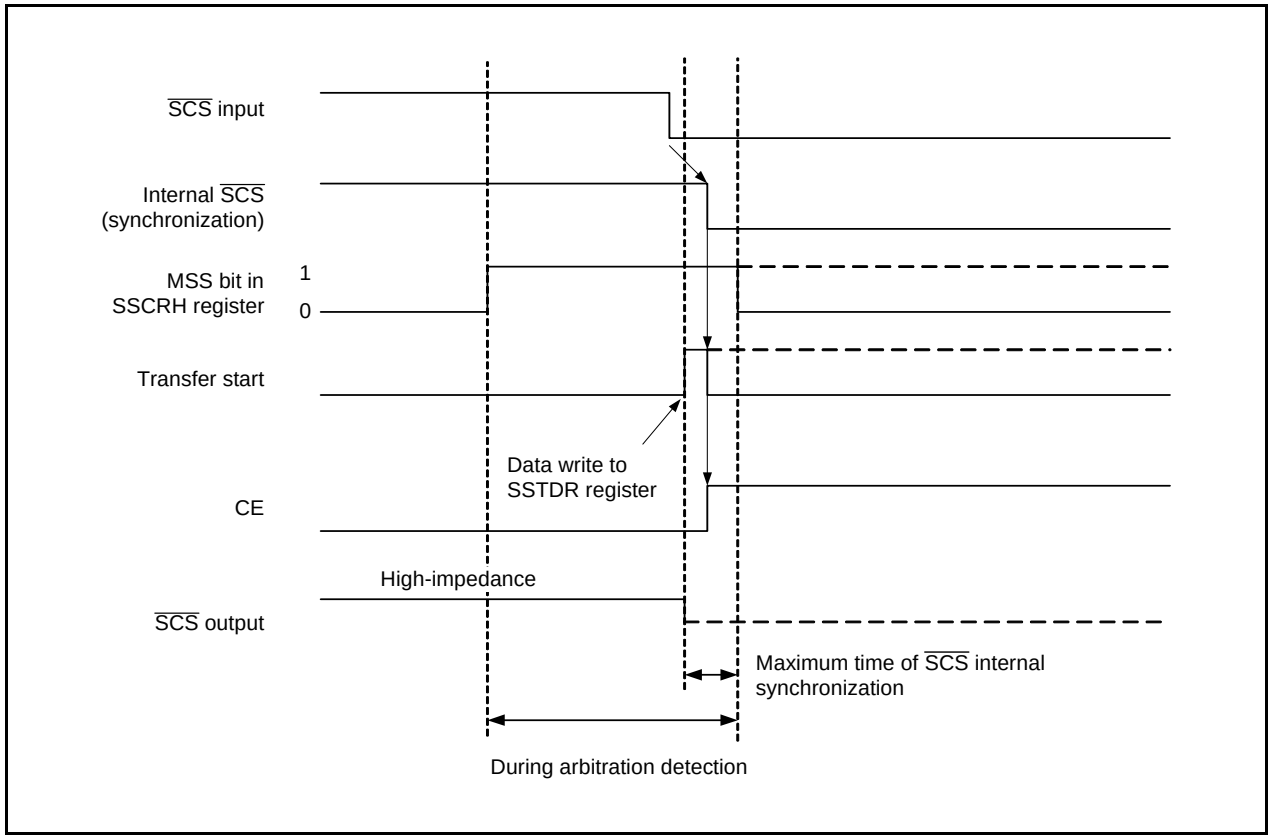


Figure 16.21 Arbitration Check Timing

16.2.8 Notes on Clock Synchronous Serial I/O with Chip Select

Set the IICSEL bit in the PMR register to 0 (select clock synchronous serial I/O with chip select function) to use the clock synchronous serial I/O with chip select function.

16.3 I²C bus Interface

The I²C bus interface is the circuit that performs serial communication based on the data transfer format of the Philips I²C bus.

Table 16.5 lists the I²C bus Interface Specifications, Figure 16.22 shows a Block Diagram of I²C bus interface, and Figure 16.23 shows the External Circuit Connection Example of Pins SCL and SDA. Figures 16.24 to 16.31 show the registers associated with the I²C bus interface.

* I²C bus is a trademark of Koninklijke Philips Electronics N. V.

Table 16.5 I²C bus Interface Specifications

Item	Specification
Communication formats	• I²C bus format - Selectable as master/slave device - Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent) - Start/stop conditions are automatically generated in master mode - Automatic loading of acknowledge bit during transmission - Bit synchronization/wait function (In master mode, the state of the SCL signal is monitored per bit and the timing is synchronized automatically. If the transfer is not possible yet, the SCL signal goes “L” and the interface stands by.) - Support for direct drive of pins SCL and SDA (N-channel open drain output) • Clock synchronous serial format - Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent)
I/O pins	SCL (I/O): Serial clock I/O pin SDA (I/O): Serial data I/O pin
Transfer clocks	• When the MST bit in the ICCR1 register is set to 0 The external clock (input from the SCL pin) • When the MST bit in the ICCR1 register is set to 1 The internal clock selected by bits CKS0 to CKS3 in the ICCR1 register (output from the SCL pin)
Receive error detection	• Overrun error detection (clock synchronous serial format) Indicates an overrun error during reception. When the last bit of the next data item is received while the RDRF bit in the ICSR register is set to 1 (data in the ICDRR register), the AL bit is set to 1.
Interrupt sources	• I²C bus format ..... 6 sources(1) Transmit data empty (including when slave address matches), transmit ends, receive data full (including when slave address matches), arbitration lost, NACK detection, and stop condition detection. • Clock synchronous serial format ..... 4 sources(1) Transmit data empty, transmit ends, receive data full and overrun error
Select functions	• I²C bus format - Selectable output level for acknowledge signal during reception • Clock synchronous serial format - MSB-first or LSB-first selectable as data transfer direction

NOTE:

1. All sources use one interrupt vector for I²C bus interface.

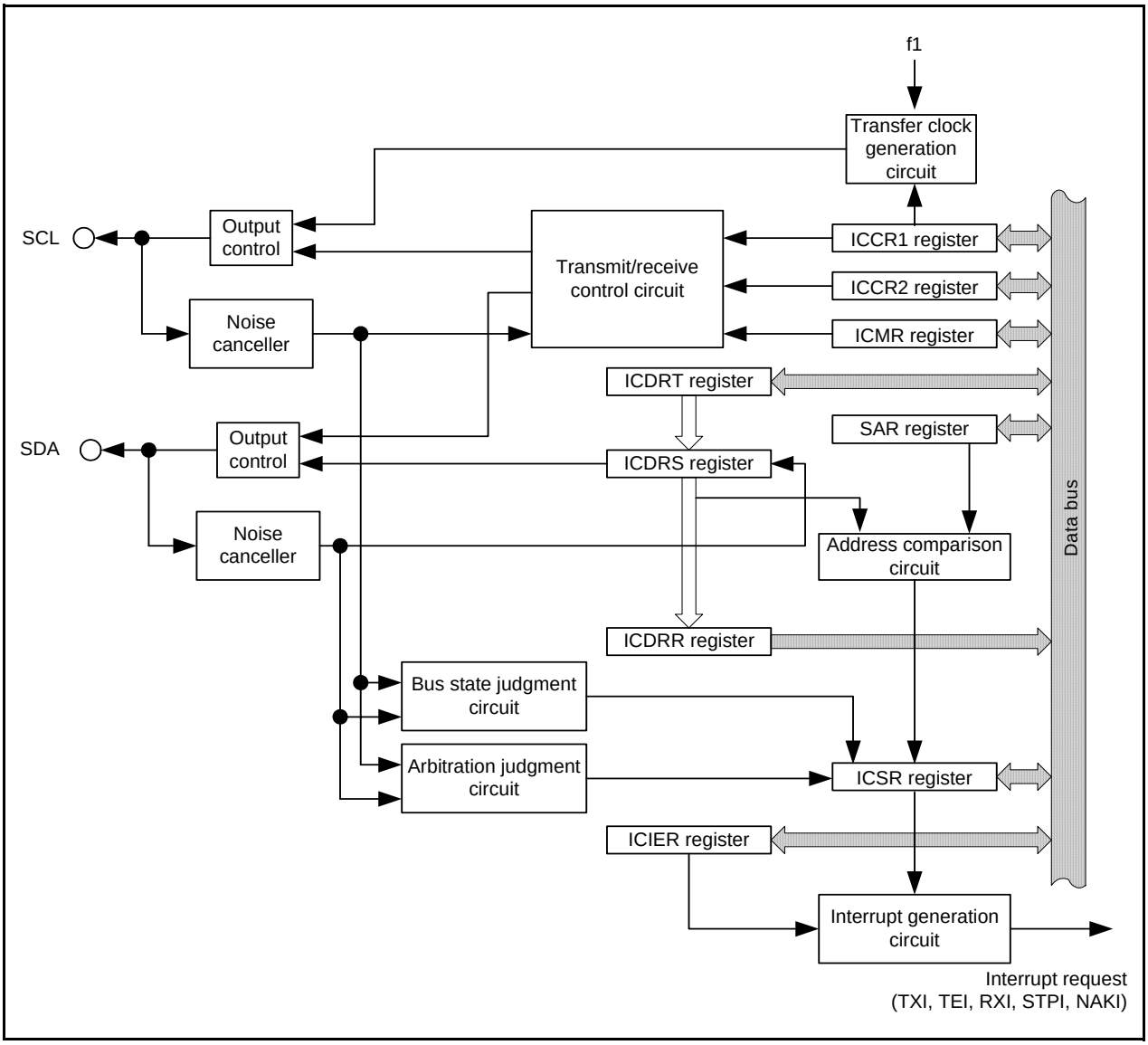


Figure 16.22 Block Diagram of I²C bus interface

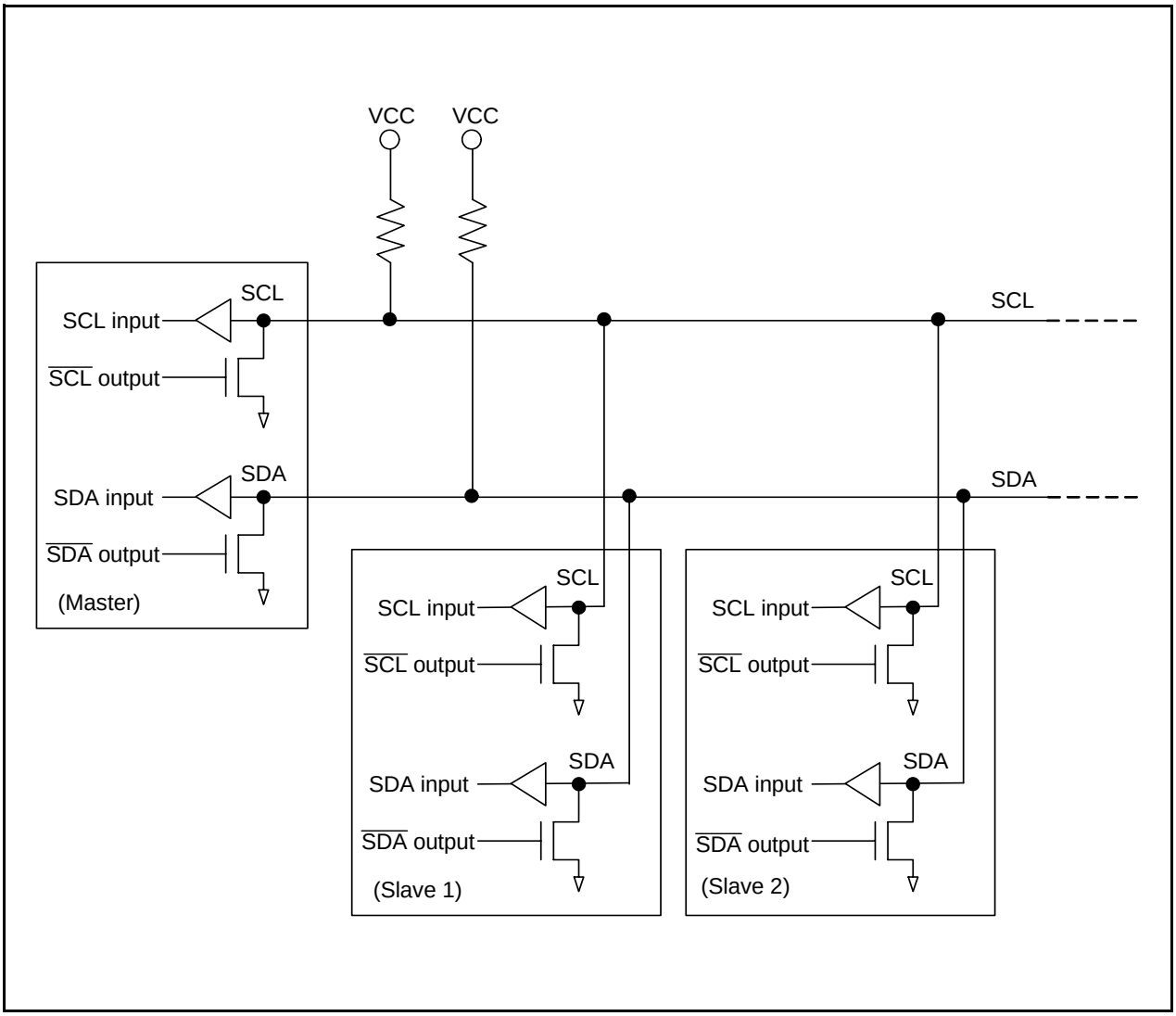
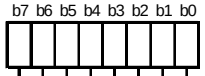


Figure 16.23 External Circuit Connection Example of Pins SCL and SDA

IIC bus Control Register 1



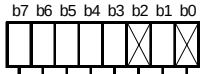
Symbol: ICCR1 | Address: 00B8h | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
CKS0	Transmit clock select bits 3 to 0(1)	b3 b2 b1 b0 0 0 0 0 : f1/28 0 0 0 1 : f1/40 0 0 1 0 : f1/48 0 0 1 1 : f1/64 0 1 0 0 : f1/80 0 1 0 1 : f1/100 0 1 1 0 : f1/112 0 1 1 1 : f1/128 1 0 0 0 : f1/56 1 0 0 1 : f1/80 1 0 1 0 : f1/96 1 0 1 1 : f1/128 1 1 0 0 : f1/160 1 1 0 1 : f1/200 1 1 1 0 : f1/224 1 1 1 1 : f1/256	RW
CKS1			RW
CKS2			RW
CKS3			RW
TRS	Transfer/receive select bit (2, 3, 6)	b5 b4 0 0 : Slave Receive Mode(4) 0 1 : Slave Transmit Mode 1 0 : Master Receive Mode 1 1 : Master Transmit Mode	RW
MST	Master/slave select bit(5, 6)		RW
RCVD	Receive disable bit	After reading the ICDRR register while the TRS bit is set to 0 0 : Maintains the next receive operation 1 : Disables the next receive operation	RW
ICE	IIC bus interface enable bit	0 : This module is halted (Pins SCL and SDA are set to port function) 1 : This module is enabled for transfer operations (Pins SCL and SDA are bus drive state)	RW

NOTES:
1. Set according to the necessary transfer rate in master mode. Refer to **Table 16.6 Transfer Rate Examples** for the transfer rate. This bit is used for maintaining of the setup time in transmit mode of slave mode. The time is 10Tcyc when the CKS3 bit is set to 0 and 20Tcyc when the CKS3 bit is set to 1. (1Tcyc = 1/f1(s))
2. Rewrite the TRS bit between transfer frames.
3. When the first 7 bit after the start condition in slave receive mode match with the slave address set in the SAR register and the 8th bit is set to 1, the TRS bit is set to 1.
4. In master mode with the I^2C bus format, when arbitration is lost, bits MST and TRS are set to 0 and the IIC enters slave receive mode.
5. When an overrun error occurs in master receive mode of the clock synchronous serial format, the MST bit is set to 0 and the IIC enters slave receive mode.
6. In multimaster operation use the MOV instruction to set bits TRS and MST.

Figure 16.24 ICCR1 Register

IIC bus Control Register 2



Symbol	Address	After Reset
ICCR2	00B9h	01111101b

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
IICRST	IIC control part reset bit	When hang-up occurs due to communication failure during I²C bus interface operation, write 1, to reset the control block of the I²C bus interface without setting ports or initializing registers.	RW
— (b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
SCLO	SCL monitor flag	0 : SCL pin is set to “L” 1 : SCL pin is set to “H”	RO
SDAOP	SDAO write protect bit	When rewrite to SDAO bit, write 0 simultaneously.(1) When read, the content is 1.	RW
SDAO	SDA output value control bit	When read 0 : SDA pin output is held “L” 1 : SDA pin output is held “H” When written(1,2) 0 : SDA pin output is changed to “L” 1 : SDA pin output is changed to high-impedance (“H” output via external pull-up resistor)	RW
SCP	Start/stop condition generation disable bit	When writing to the to BBSY bit, write 0 simultaneously.(3) When read, the content is 1. Writing 1 is invalid.	RW
BBSY	Bus busy bit(4)	When read 0 : Bus is in released state (SDA signal changes from “L” to “H” while SCL signal is in “H” state) 1 : Bus is in occupied state (SDA signal changes from “H” to “L” while SCL signal is in “H” state) When written(3) 0 : Generates stop condition 1 : Generates start condition	RW

NOTES:
1. When writing to the SDAO bit, write 0 to the SDAOP bit using the MOV instruction simultaneously.
2. Do not write during a transfer operation.
3. This bit is enabled in master mode. When writing to the BBSY bit, write 0 to the SCP bit using the MOV instruction simultaneously. Execute the same way when the start condition is regenerating.
4. This bit is disabled when the clock synchronous serial format is used.

Figure 16.25 ICCR2 Register

IIC bus Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
		0	X				

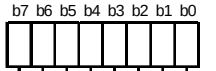
Symbol	Address	After Reset
ICMR	00BAh	00011000b

Bit Symbol	Bit Name	Function	RW
BC0	Bits counter 2 to 0	I²C bus format (remaining transfer bit count when read out and data bit count of next transfer when written).(1,2) b2 b1 b0 0 0 0 : 9 bits(3) 0 0 1 : 2 bits 0 1 0 : 3 bits 0 1 1 : 4 bits 1 0 0 : 5 bits 1 0 1 : 6 bits 1 1 0 : 7 bits 1 1 1 : 8 bits	RW
BC1		Clock synchronous serial format (when read, the remaining transfer bit count and when written 000b). b2 b1 b0 0 0 0 : 8 bits 0 0 1 : 1 bit 0 1 0 : 2 bits 0 1 1 : 3 bits 1 0 0 : 4 bits 1 0 1 : 5 bits 1 1 0 : 6 bits 1 1 1 : 7 bits	RW
BC2			RW
BCWP	BC write protect bit	When rewriting bits BC0 to BC2, write 0 simultaneously.(2,4) When read, the content is 1.	RW
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
— (b5)	Reserved bit	Set to 0.	RW
WAIT	Wait insertion bit(5)	0 : No wait (Transfer data and acknowledge bit consecutively) 1 : Wait (After the clock falls for the final data bit, “L” period is extended for two transfer clocks cycles)	RW
MLS	MSB-first/LSB-first select bit	0 : Data transfer with MSB-first(6) 1 : Data transfer with LSB-first	RW

NOTES:
1. Rewrite between transfer frames. When writing values other than 000b, write when the SCL signal is “L”.
2. When writing to bits BC0 to BC2, write 0 to the BCWP bit using the MOV instruction.
3. After data including the acknowledge bit is transferred, these bits are automatically set to 000b. When the start condition is detected, these bits are automatically set to 000b.
4. Do not rewrite when the clock synchronous serial format is used.
5. The setting value is enabled in master mode of the I²C bus format. It is disabled in slave mode of the I²C bus format or when the clock synchronous serial format is used.
6. Set to 0 when the I²C bus format is used.

Figure 16.26 ICMR Register

IIC bus Interrupt Enable Register



Symbol	Address	After Reset
ICIER	00BBh	00h

Bit Symbol	Bit Name	Function	RW
ACKBT	Transmit acknowledge select bit	0 : 0 is transmitted as acknowledge bit in receive mode. 1 : 1 is transmitted as acknowledge bit in receive mode.	RW
ACKBR	Receive acknowledge bit	0 : Acknowledge bit received from receive device in transmit mode is set to 0. 1 : Acknowledge bit received from receive device in transmit mode is set to 1.	RO
ACKE	Acknowledge bit judgment select bit	0 : Value of receive acknowledge bit is ignored and continuous transfer is performed. 1 : When receive acknowledge bit is set to 1, continuous transfer is halted.	RW
STIE	Stop condition detection interrupt enable bit	0 : Disables stop condition detection interrupt request 1 : Enables stop condition detection interrupt request(2)	RW
NAKIE	NACK receive interrupt enable bit	0 : Disables NACK receive interrupt request and arbitration lost/overrun error interrupt request 1 : Enables NACK receive interrupt request and arbitration lost/overrun error interrupt request(1)	RW
RIE	Receive interrupt enable bit	0 : Disables receive data full and overrun error interrupt request 1 : Enables receive data full and overrun error interrupt request(1)	RW
TEIE	Transmit end interrupt enable bit	0 : Disables transmit end interrupt request 1 : Enables transmit end interrupt request	RW
TIE	Transmit interrupt enable bit	0 : Disables transmit data empty interrupt request 1 : Enables transmit data empty interrupt request	RW

NOTES:
1. An overrun error interrupt request is generated when the clock synchronous format is used.
2. Set the STIE bit to 1 (enable stop condition detection interrupt request) when the STOP bit in the ICSR register is set to 0.

Figure 16.27 ICIER Register

IIC bus Status Register(7)

b7 b6 b5 b4 b3 b2 b1 b0

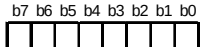
Symbol	Address	After Reset
ICSR	00BCh	0000X000b

Bit Symbol	Bit Name	Function	RW
ADZ	General call address recognition flag(1,2)	When the general call address is detected, this flag is set to 1.	RW
AAS	Slave address recognition flag(1)	This flag is set to 1 when the first frame following start condition matches bits SVA0 to SVA6 in the SAR register in slave receive mode. (Detect the slave address and generate call address)	RW
AL	Arbitration lost flag/overrun error flag(1)	When the I²C bus format is used, this flag indicates that arbitration has been lost in master mode. In the following cases, this flag is set to 1(3). • When the internal SDA signal and SDA pin level do not match at the rise of the SCL signal in master transmit mode • When the start condition is detected and the SDA pin is held "H" in master transmit/receive mode This flag indicates an overrun error when the clock synchronous format is used. In the following case, this flag is set to 1. • When the last bit of the next data item is received while the RDRF bit is set to 1	RW
STOP	Stop condition detection flag(1)	When the stop condition is detected after the frame is transferred, this flag is set to 1.	RW
NACKF	No acknowledge detection flag(1,4)	When no acknowledge is detected from the receive device after transmission, this flag is set to 1.	RW
RDRF	Receive data register full(1,5)	When receive data is transferred from in registers ICDRS to ICDRR , this flag is set to 1.	RW
TEND	Transmit end(1,6)	When the 9th clock cycle of the SCL signal in the I²C bus format occurs while the TDRE bit is set to 1, this flag is set to 1. This flag is set to 1 when the final bit of the transmit frame is transmitted in the clock synchronous format.	RW
TDRE	Transmit data empty(1,6)	In the following cases, this flag is set to 1. • Data is transferred from registers ICDRT to ICDRS and the ICDRT register is empty • When setting the TRS bit in the ICCR1 register to 1 (transmit mode) • When generating the start condition (including retransmit) • When changing from slave receive mode to slave transmit mode	RW

NOTES:
1. Each bit is set to 0 by reading 1 before writing 0.
2. This flag is enabled in slave receive mode of the I²C bus format.
3. When two or more master devices attempt to occupy the bus at nearly the same time, if the I²C bus Interface monitors the SDA pin and the data which the I²C bus Interface transmits is different, the AL flag is set to 1 and the bus is occupied by another master.
4. The NACKF bit is enabled when the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted).
5. The RDRF bit is set to 0 when reading data from the ICDRR register.
6. Bits TEND and TDRE are set to 0 when writing data to the ICDRT register.
7. When accessing the ICSR register continuously, insert one or more NOP instructions between the instructions to access it.

Figure 16.28 ICSR Register

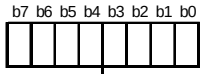
Slave Address Register



Symbol	Address	After Reset
SAR	00BDh	00h

Bit Symbol	Bit Name	Function	RW
FS	Format select bit	0 : I²C bus format 1 : Clock synchronous serial format	RW
SVA0	Slave address 6 to 0	Set an address different from that of the other slave devices which are connected to the I²C bus. When the 7 high-order bits of the first frame transmitted after the starting condition match bits SVA0 to SVA6 in slave mode of the I²C bus format, the MCU operates as a slave device.	RW
SVA1			RW
SVA2			RW
SVA3			RW
SVA4			RW
SVA5			RW
SVA6			RW

IIC bus Transmit Data Register



Symbol	Address	After Reset
ICDRT	00BEh	FFh

Function	RW
Store transmit data When it is detected that the ICDRS register is empty, the stored transmit data item is transferred to the ICDRS register and data transmission starts. When the next transmit data item is written to the ICDRT register during transmission of the data in the ICDRS register, continuous transmit is enabled. When the MLS bit in the ICMR register is set to 1 (data transferred LSB-first) and after the data is written to the ICDRT register, the MSB-LSB inverted data is read.	RW

Figure 16.29 Registers SAR and ICDRT

IIC bus Receive Data Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
ICDRR	00BFh	FFh

Function	RW
Store receive data When the ICDRS register receives 1 byte of data, the receive data is transferred to the ICDRR register and the next receive operation is enabled.	RO

IIC bus Shift Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol
ICDRS

Function	RW
This register is used to transmit and receive data. The transmit data is transferred from registers ICRDT to the ICDRS and data is transmitted from the SDA pin when transmitting. After 1 byte of data received, data is transferred from registers ICDRS to ICDRR while receiving.	—

Figure 16.30 Registers ICDRR and ICDRS

Port Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
	0	0		0	0	0	0

Symbol	Address	After Reset
PMR	00F8h	00h

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Reserved bits	Set to 0.	—
U1PINSEL	Port CLK1/TXD1/RXD1 switch bit	0 : I/O ports P6_5, P6_6, P6_7 1 : CLK1, TXD1, RXD1	RW
— (b6-b5)	Reserved bits	Set to 0.	—
IICSEL	SSU / I²C bus switch bit	0 : Selects SSU function 1 : Selects I²C bus function	RW

Figure 16.31 PMR Register

16.3.1 Transfer Clock

When the MST bit in the ICCR1 register is set to 0, the transfer clock is the external clock input from the SCL pin. When the MST bit in the ICCR1 register is set to 1, the transfer clock is the internal clock selected by bits CKS0 to CKS3 in the ICCR1 register and the transfer clock is output from the SCL pin.
Table 16.6 lists the Transfer Rate Examples.

Table 16.6 Transfer Rate Examples

ICCR1 Register				Transfer Clock	Transfer Rate				
CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	0	0	0	f1/28	179 kHz	286 kHz	357 kHz	571 kHz	714 kHz
			1	f1/40	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
		1	0	f1/48	104 kHz	167 kHz	208 kHz	333 kHz	417 kHz
			1	f1/64	78.1 kHz	125 kHz	156 kHz	250 kHz	313 kHz
	1	0	0	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
			1	f1/100	50.0 kHz	80.0 kHz	100 kHz	160 kHz	200 kHz
		1	0	f1/112	44.6 kHz	71.4 kHz	89.3 kHz	143 kHz	179 kHz
			1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
1	0	0	0	f1/56	89.3 kHz	143 kHz	179 kHz	286 kHz	357 kHz
			1	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
		1	0	f1/96	52.1 kHz	83.3 kHz	104 kHz	167 kHz	208 kHz
			1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
	1	0	0	f1/160	31.3 kHz	50.0 kHz	62.5 kHz	100 kHz	125 kHz
			1	f1/200	25.0 kHz	40.0 kHz	50.0 kHz	80.0 kHz	100 kHz
		1	0	f1/224	22.3 kHz	35.7 kHz	44.6 kHz	71.4 kHz	89.3 kHz
			1	f1/256	19.5 kHz	31.3 kHz	39.1 kHz	62.5 kHz	78.1 kHz

16.3.2 Interrupt Requests

The I2C bus interface has six interrupt requests when the I2C bus format is used and four interrupt requests when the clock synchronous serial format is used.

Table 16.7 lists the Interrupt Requests of I2C bus Interface.

Since these interrupt requests are allocated at the I2C bus interface interrupt vector table, determining the source bit by bit is necessary.

Table 16.7 Interrupt Requests of I2C bus Interface

Interrupt Request		Generation Condition	Format	
			I2C bus	Clock Synchronous Serial
Transmit data empty	TXI	TIE = 1 and TDRE = 1	Enabled	Enabled
Transmit ends	TEI	TEIE = 1 and TEND = 1	Enabled	Enabled
Receive data full	RXI	RIE = 1 and RDRF = 1	Enabled	Enabled
Stop condition detection	STPI	STIE = 1 and STOP = 1	Enabled	Disabled
NACK detection	NAKI	NAKIE = 1 and AL = 1 (or	Enabled	Disabled
Arbitration lost/overrun error		NAKIE = 1 and NACKF = 1)	Enabled	Enabled

STIE, NAKIE, RIE, TEIE, TIE: Bits in ICIER register

AL, STOP, NACKF, RDRF, TEND, TDRE: Bits in ICSR register

When the generation conditions listed in Table 16.7 are met, an I2C bus interface interrupt request is generated. Set the interrupt generation conditions to 0 by the I2C bus interface interrupt routine. However, bits TDRE and TEND are automatically set to 0 by writing transmit data to the ICDRT register and the RDRF bit is automatically set to 0 by reading the ICDRR register. When writing transmit data to the ICDRT register, the TDRE bit is set to 0. When data is transferred from registers ICDRT to ICDRS, the TDRE bit is set to 1 and by further setting the TDRE bit to 0, 1 additional byte may be transmitted.

Set the STIE bit to 1 (enable stop condition detection interrupt request) when the STOP bit is set to 0.

16.3.3 I²C bus Interface Mode

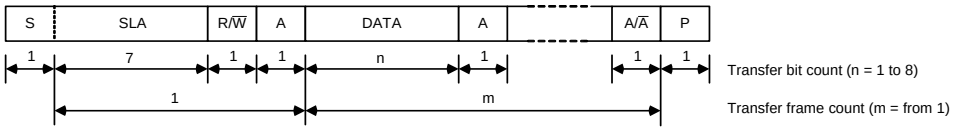
16.3.3.1 I²C bus Format

Setting the FS bit in the SAR register to 0 enables communication in I²C bus format.

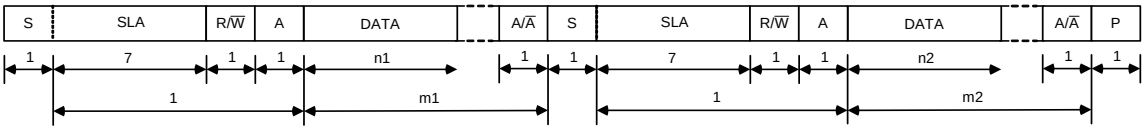
Figure 16.32 shows the I²C bus Format and Bus Timing. The 1st frame following the start condition consists of 8 bits.

(1) I²C bus format

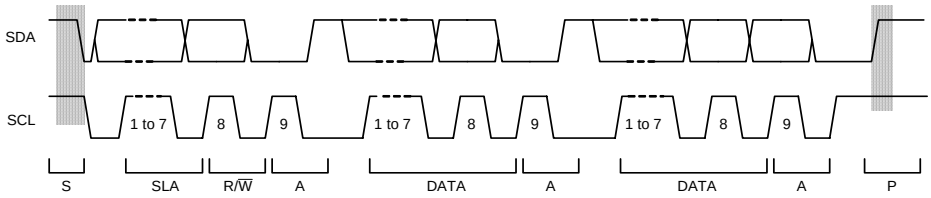
(a) I²C bus format (FS = 0)



(b) I²C bus format (when start condition is retransmitted, FS = 0)



(2) I²C bus timing



Explanation of symbols
S : Start condition
The master device changes the SDA signal from “H” to “L” while the SCL signal is held “H”.
SLA : Slave address
R/W : Indicates the direction of data transmit/receive
Data is transmitted from the slave device to the master device when R/W value is 1 and from the master device to the slave device when R/W value is 0.
A : Acknowledge
The receive device sets the SDA signal to “L”.
DATA : Transmit / receive data
P : Stop condition
The master device changes the SDA signal from “L” to “H” while the SCL signal is held “H”.

Figure 16.32 I²C bus Format and Bus Timing

16.3.3.2 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal.

Figures 16.33 and 16.34 show the Operating Timing in Master Transmit Mode (I^2C bus Interface Mode).

The transmit procedure and operation in master transmit mode are as follows.

(1) Set the STOP bit in the ICSR register to 0 to reset it. Then set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then set bits WAIT and MLS in the ICMR register and set bits CKS0 to CKS3 in the ICCR1 register (initial setting).

(2) Read the BBSY bit in the ICCR2 register to confirm that the bus is free. Set bits TRS and MST in the ICCR1 register to master transmit mode. The start condition is generated by writing 1 to the BBSY bit and 0 to the SCP bit by the MOV instruction.

(3) After confirming that the TDRE bit in the ICSR register is set to 1 (data is transferred from registers ICDRT to ICDRS), write transmit data to the ICDRT register (data in which a slave address and R/$\overline{W}$ are indicated in the 1st byte). At this time, the TDRE bit is automatically set to 0, data is transferred from registers ICDRT to ICDRS, and the TDRE bit is set to 1 again.

(4) When transmission of 1 byte of data is completed while the TDRE bit is set to 1, the TEND bit in the ICSR register is set to 1 at the rise of the 9th transmit clock pulse. Read the ACKBR bit in the ICIER register, and confirm that the slave is selected. Write the 2nd byte of data to the ICDRT register. Since the slave device is not acknowledged when the ACKBR bit is set to 1, generate the stop condition. The stop condition is generated by the writing 0 to the BBSY bit and 0 to the SCP bit by the MOV instruction. The SCL signal is held “L” until data is available and the stop condition is generated.

(5) Write the transmit data after the 2nd byte to the ICDRT register every time the TDRE bit is set to 1.

(6) When writing the number of bytes to be transmitted to the ICDRT register, wait until the TEND bit is set to 1 while the TDRE bit is set to 1. Or wait for NACK (the NACKF bit in the ICSR register is set to 1) from the receive device while the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted). Then generate the stop condition before setting bits TEND and NACKF to 0.

(7) When the STOP bit in the ICSR register is set to 1, return to slave receive mode.

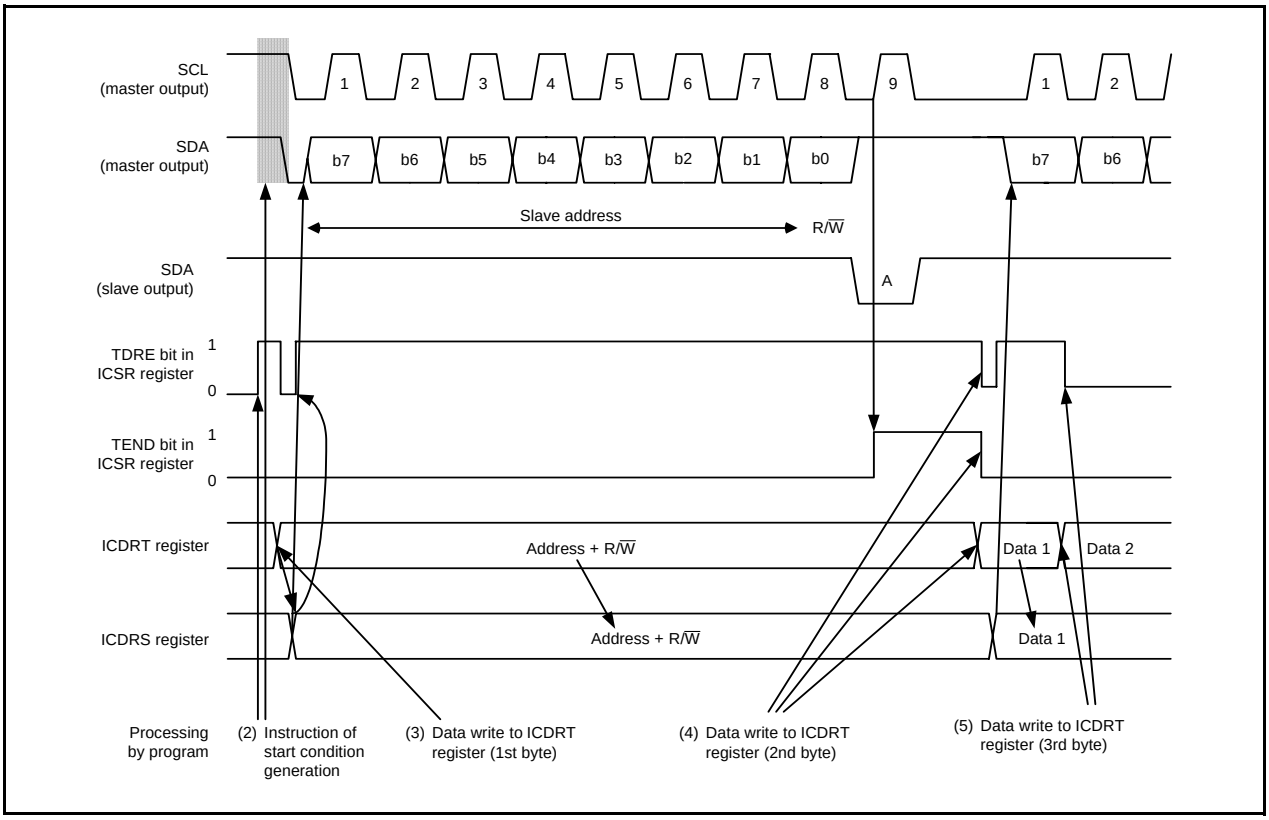


Figure 16.33 Operating Timing in Master Transmit Mode (I²C bus Interface Mode) (1)

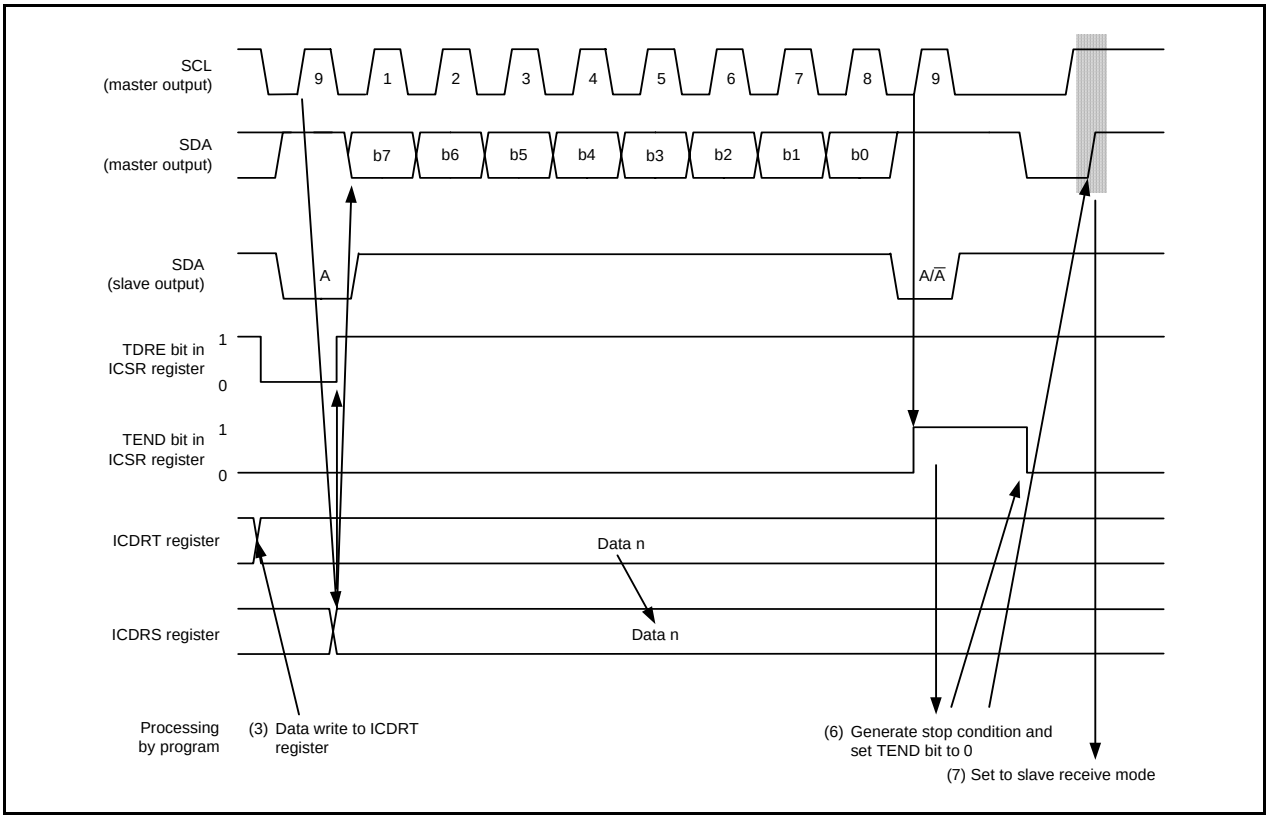


Figure 16.34 Operating Timing in Master Transmit Mode (I²C bus Interface Mode) (2)

16.3.3.3 Master Receive Operation

In master receive mode, the master device outputs the receive clock, receives data from the slave device, and returns an acknowledge signal.

Figures 16.35 and 16.36 show the Operating Timing in Master Receive Mode (I^2C bus Interface Mode).

The receive procedure and operation in master receive mode are shown below.

(1) After setting the TEND bit in the ICSR register to 0, switch from master transmit mode to master receive mode by setting the TRS bit in the ICCR1 register to 0. Also, set the TDRE bit in the ICSR register to 0.

(2) When performing the dummy read of the ICDRR register and starting the receive operation, the receive clock is output in synchronization with the internal clock and data is received. The master device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle of the receive clock.

(3) The 1-frame data receive is completed and the RDRF bit in the ICSR register is set to 1 at the rise of the 9th clock cycle. At this time, when reading the ICDRR register, the received data can be read and the RDRF bit is set to 0 simultaneously.

(4) Continuous receive operation is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls after the ICDRR register is read by another process while the RDRF bit is set to 1, the SCL signal is fixed “L” until the ICDRR register is read.

(5) If the next frame is the last receive frame and the RCVD bit in the ICCR1 register is set to 1 (disables the next receive operation) before reading the ICDRR register, stop condition generation is enabled after the next receive operation.

(6) When the RDRF bit is set to 1 at the rise of the 9th clock cycle of the receive clock, generate the stop condition.

(7) When the STOP bit in the ICSR register is set to 1, read the ICDRR register and set the RCVD bit to 0 (maintain the following receive operation).

(8) Return to slave receive mode.

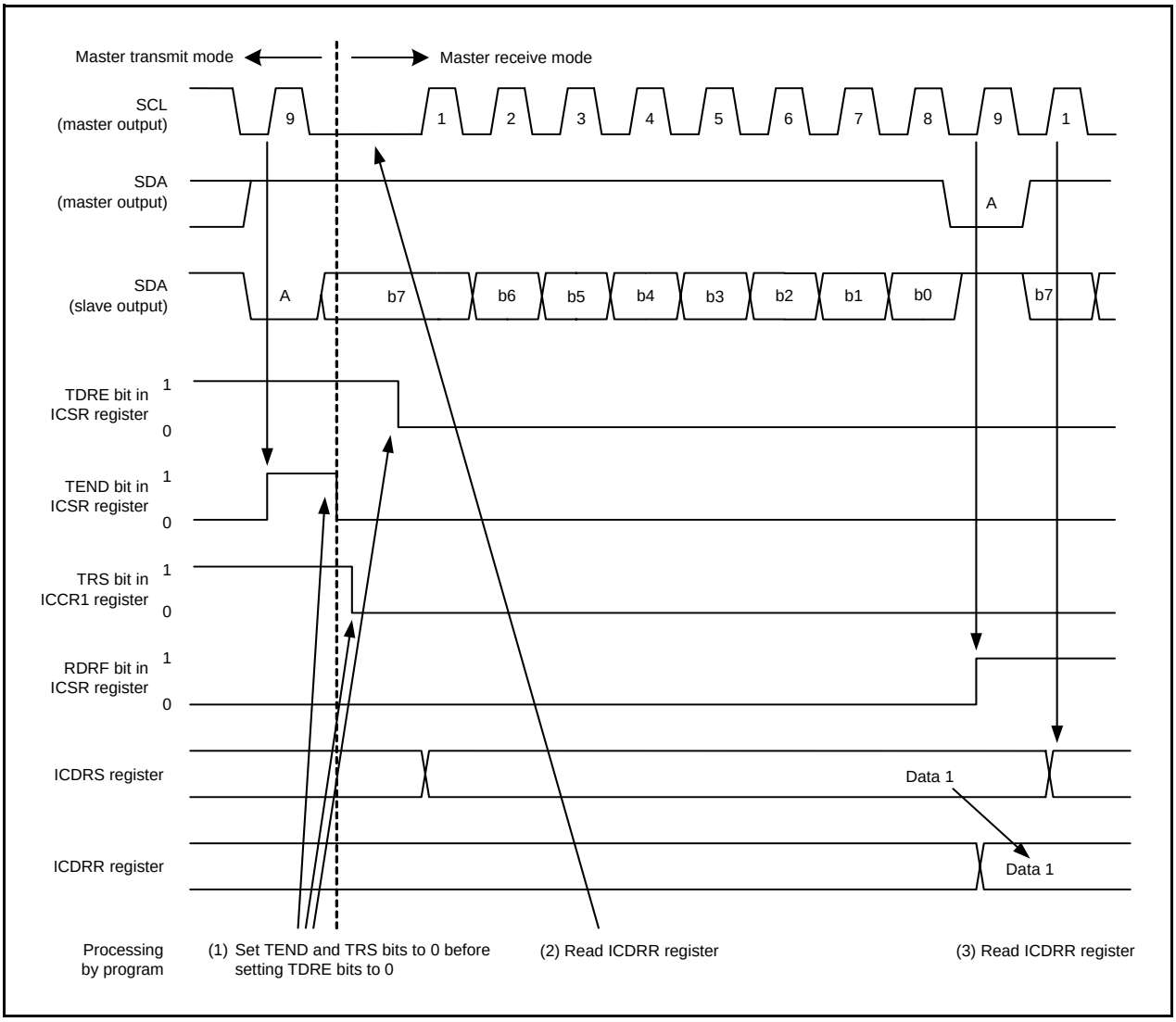


Figure 16.35 Operating Timing in Master Receive Mode (I^2C bus Interface Mode) (1)

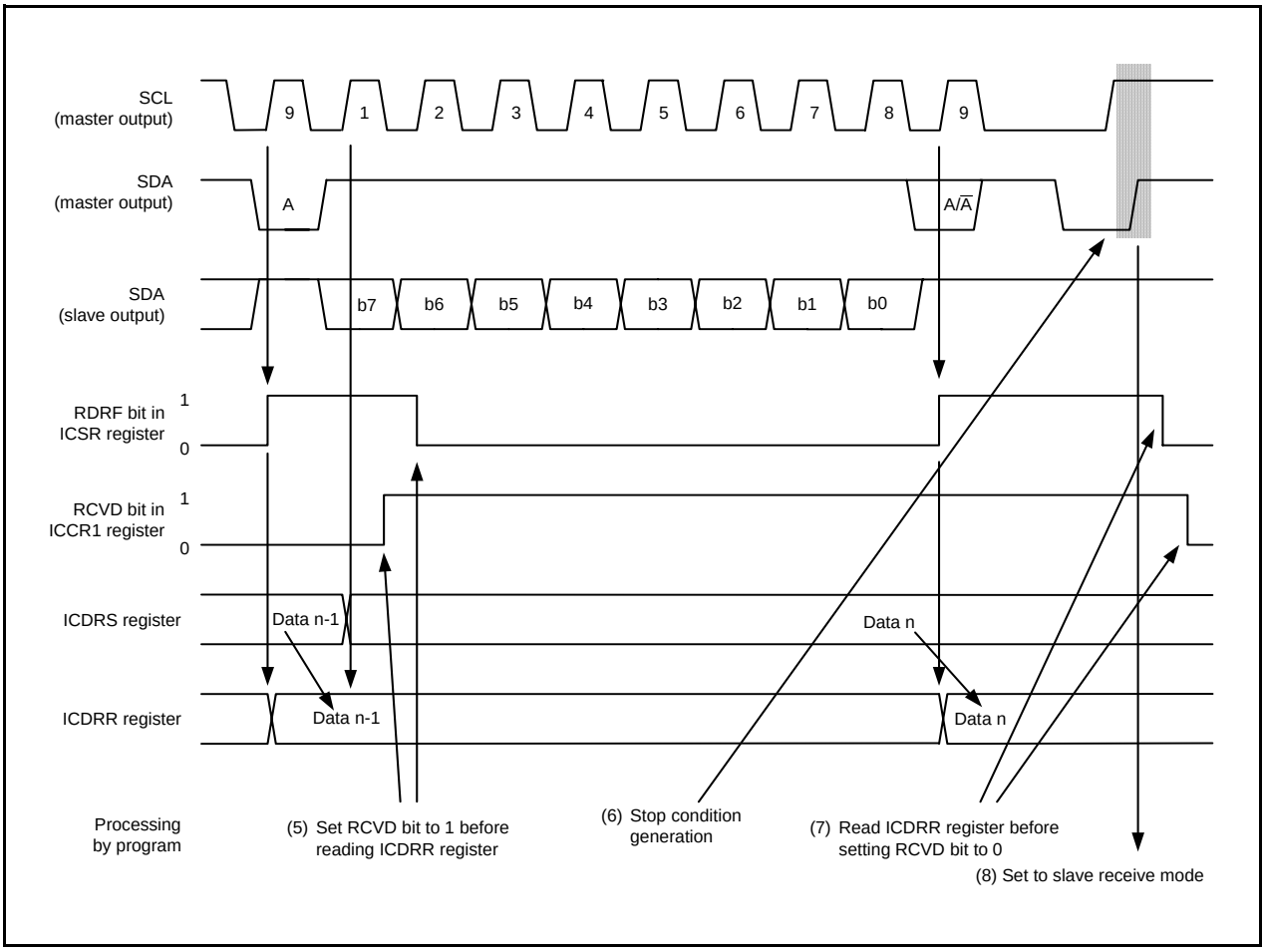


Figure 16.36 Operating Timing in Master Receive Mode (I^2C bus Interface Mode) (2)

16.3.3.4 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data while the master device outputs the receive clock and returns an acknowledge signal.

Figures 16.37 and 16.38 show the Operating Timing in Slave Transmit Mode (I^2C bus Interface Mode).

The transmit procedure and operation in slave transmit mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the 1st frame after detecting the start condition, the slave device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rise of the 9th clock cycle. At this time, if the 8th bit of data (R/$\overline{W}$) is 1, bits TRS and TDRE in the ICSR register are set to 1, and the mode is switched to slave transmit mode automatically. Continuous transmission is enabled by writing transmit data to the ICDRT register every time the TDRE bit is set to 1.

(3) When the TDRE bit in the ICDRT register is set to 1 after writing the last transmit data to the ICDRT register, wait until the TEND bit in the ICSR register is set to 1 while the TDRE bit is set to 1. When the TEND bit is set to 1, set the TEND bit to 0.

(4) The SCL signal is released by setting the TRS bit to 0 and performing a dummy read of the ICDRR register to end the process.

(5) Set the TDRE bit to 0.

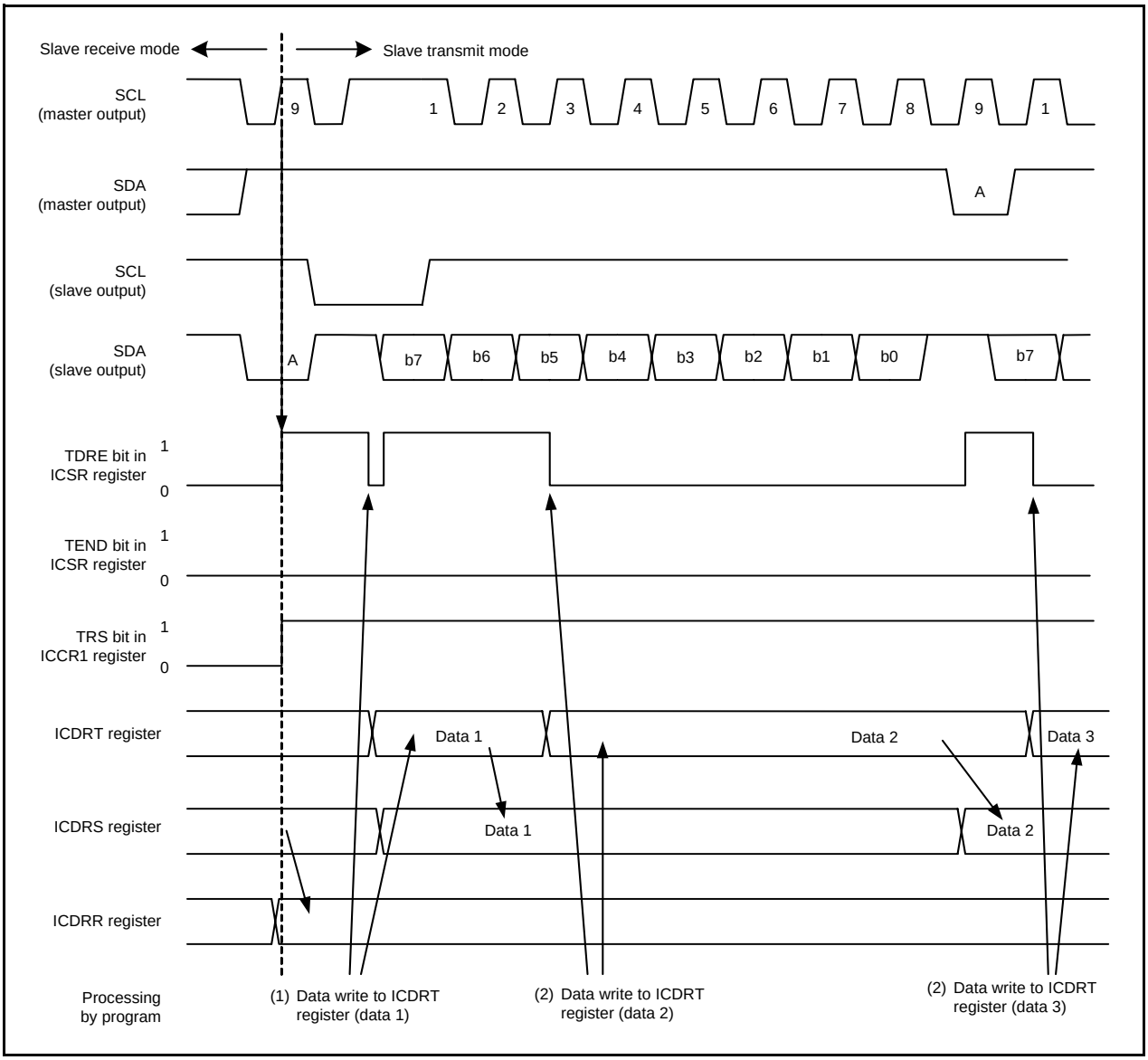


Figure 16.37 Operating Timing in Slave Transmit Mode (I^2C bus Interface Mode) (1)

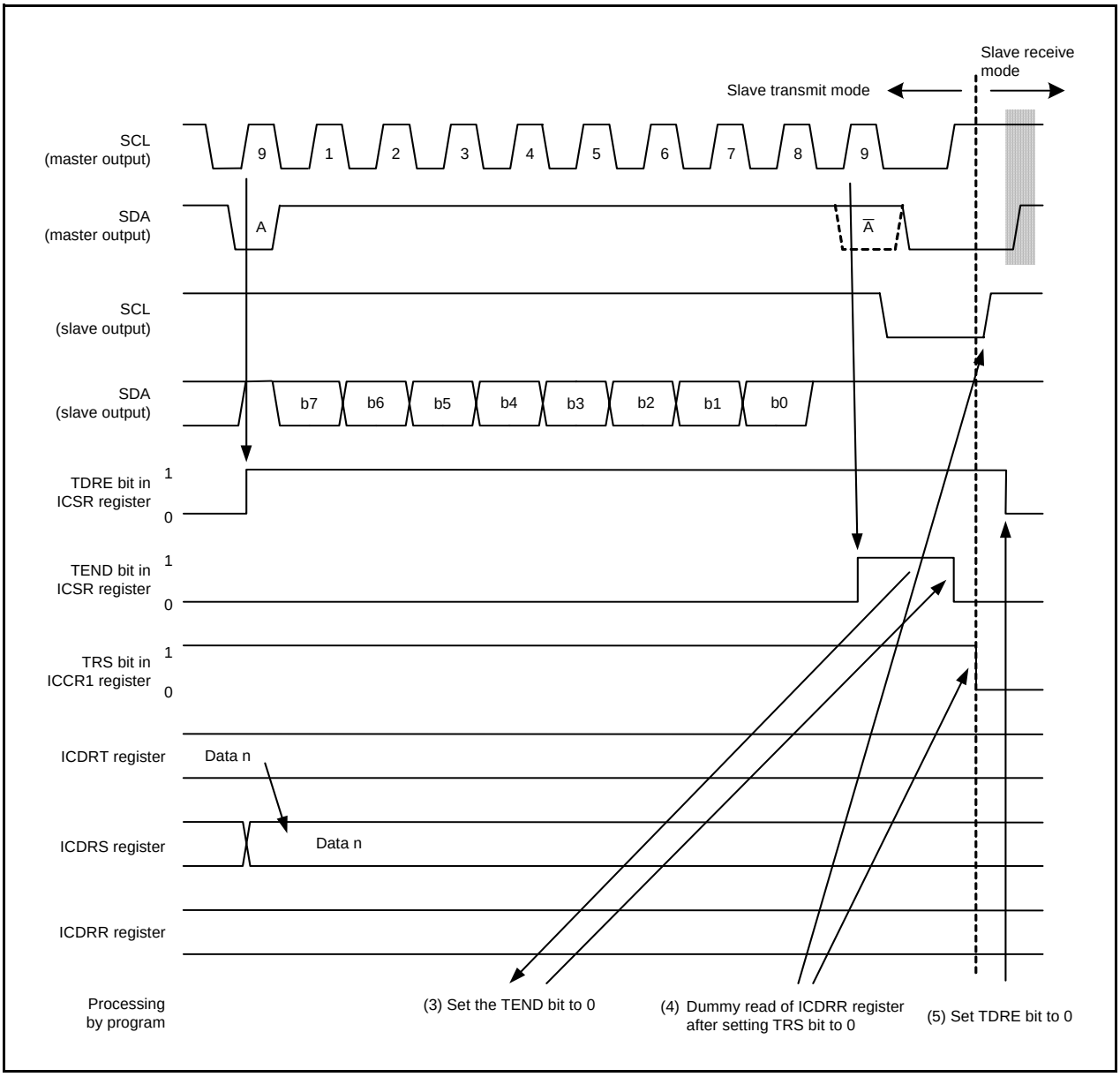


Figure 16.38 Operating Timing in Slave Transmit Mode (I^2C bus Interface Mode) (2)

16.3.3.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal.

Figures 16.39 and 16.40 show the Operating Timing in Slave Receive Mode (I^2C bus Interface Mode).

The receive procedure and operation in slave receive mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the 1st frame after detecting the start condition, the slave device outputs the level set in the ACKBT bit in the ICIER register to the SDA pin at the rise of the 9th clock cycle. Since the RDRF bit in the ICSR register is set to 1 simultaneously, perform the dummy read (the read data is unnecessary because it indicates the slave address and R/$\overline{W}$).

(3) Read the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is set to 1, the SCL signal is fixed “L” until the ICDRR register is read. The setting change of the acknowledge signal returned to the master device before reading the ICDRR register takes affect from the following transfer frame.

(4) Reading the last byte is performed by reading the ICDRR register in like manner.

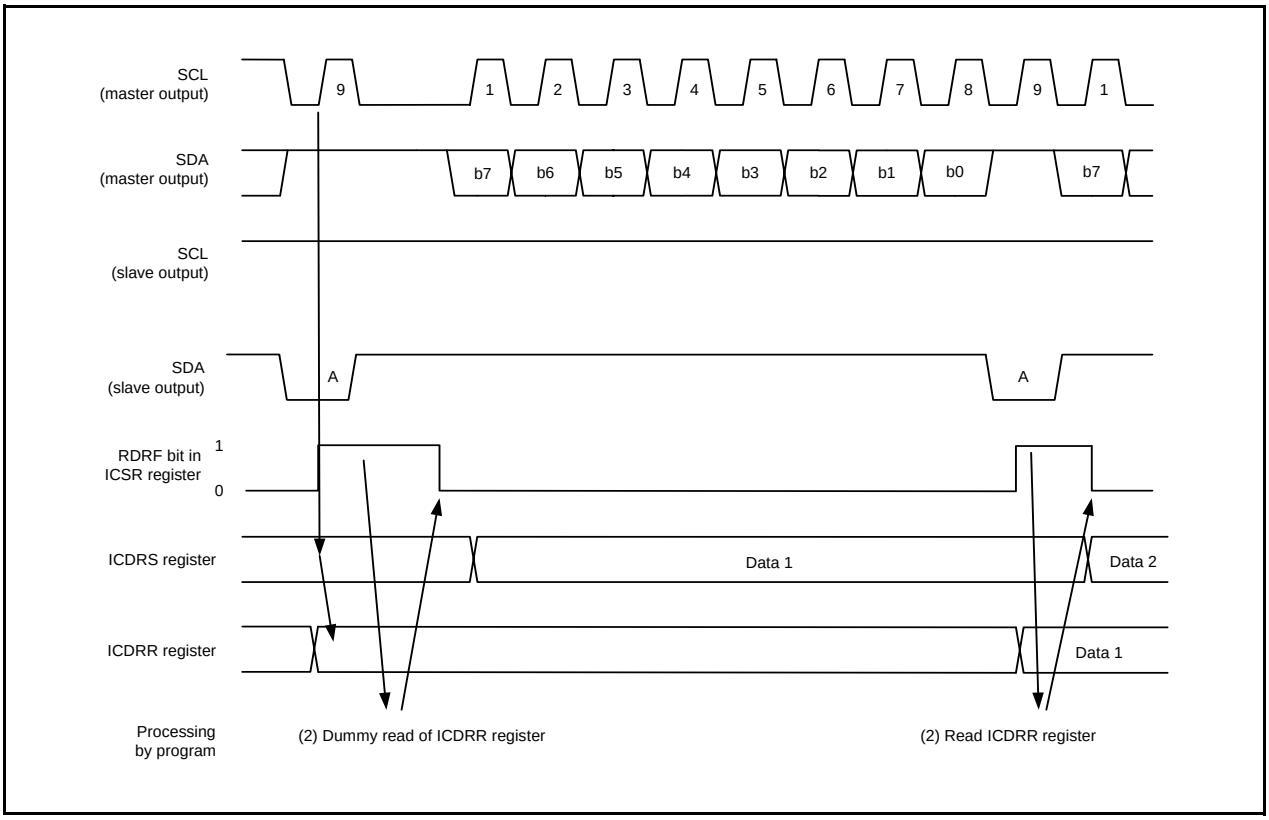


Figure 16.39 Operating Timing in Slave Receive Mode (I^2C bus Interface Mode) (1)

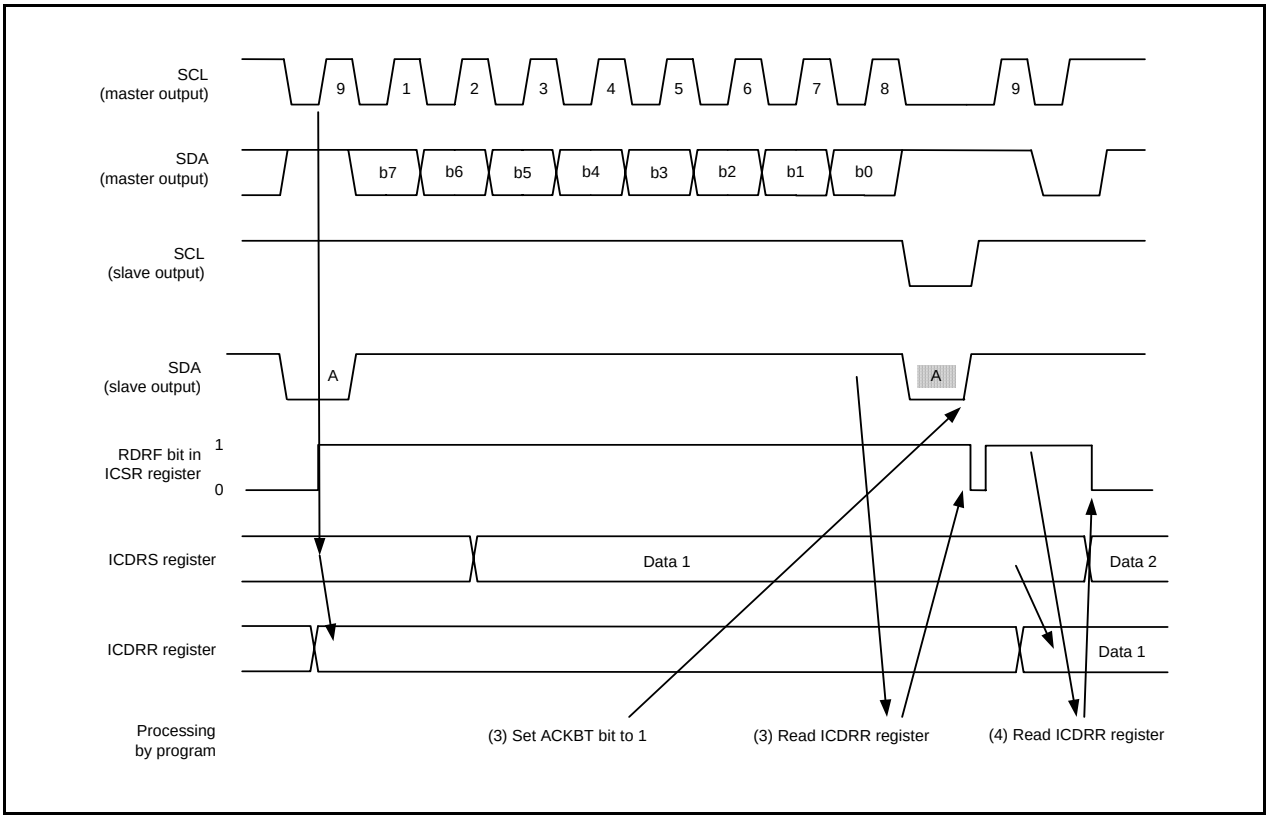


Figure 16.40 Operating Timing in Slave Receive Mode (I^2C bus Interface Mode) (2)

16.3.4 Clock Synchronous Serial Mode

16.3.4.1 Clock Synchronous Serial Format

Set the FS bit in the SAR register to 1 to use the clock synchronous serial format for communication. Figure 16.41 shows the Transfer Format of Clock Synchronous Serial Format.

When the MST bit in the ICCR1 register is set to 1, the transfer clock is output from the SCL pin, and when the MST bit is set to 0, the external clock is input.

The transfer data is output between successive falling edges of the SCL clock, and data is determined at the rising edge of the SCL clock. MSB-first or LSB-first can be selected as the order of the data transfer by setting the MLS bit in the ICMR register. The SDA output level can be changed by the SDAO bit in the ICCR2 register during transfer standby.

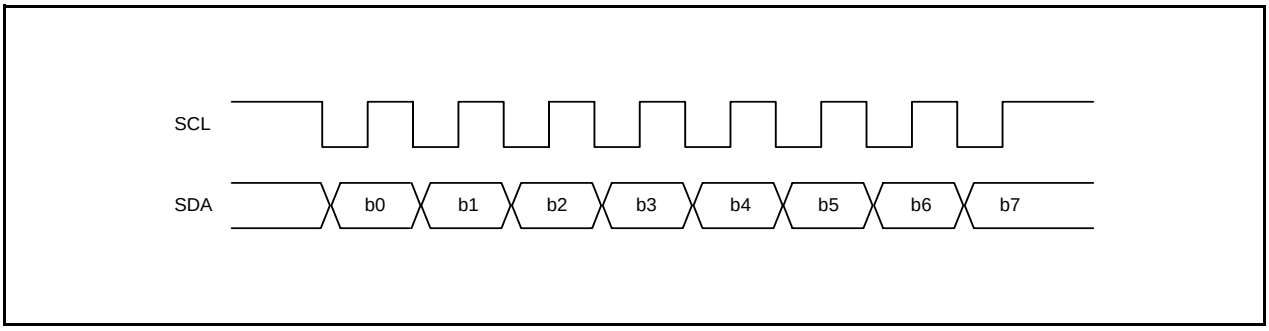


Figure 16.41 Transfer Format of Clock Synchronous Serial Format

16.3.4.2 Transmit Operation

In transmit mode, transmit data is output from the SDA pin in synchronization with the falling edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 16.42 shows the Operating Timing in Transmit Mode (Clock Synchronous Serial Mode).

The transmit procedure and operation in transmit mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Set bits CKS0 to CKS3 in the ICCR1 register and set the MST bit (initial setting).
(2) The TDRE bit in the ICSR register is set to 1 by selecting transmit mode after setting the TRS bit in the ICCR1 register to 1.
(3) Data is transferred from registers ICDRT to ICDRS and the TDRE bit is automatically set to 1 by writing transmit data to the ICDRT register after confirming that the TDRE bit is set to 1. Continuous transmission is enabled by writing data to the ICDRT register every time the TDRE bit is set to 1. When switching from transmit to receive mode, set the TRS bit to 0 while the TDRE bit is set to 1.

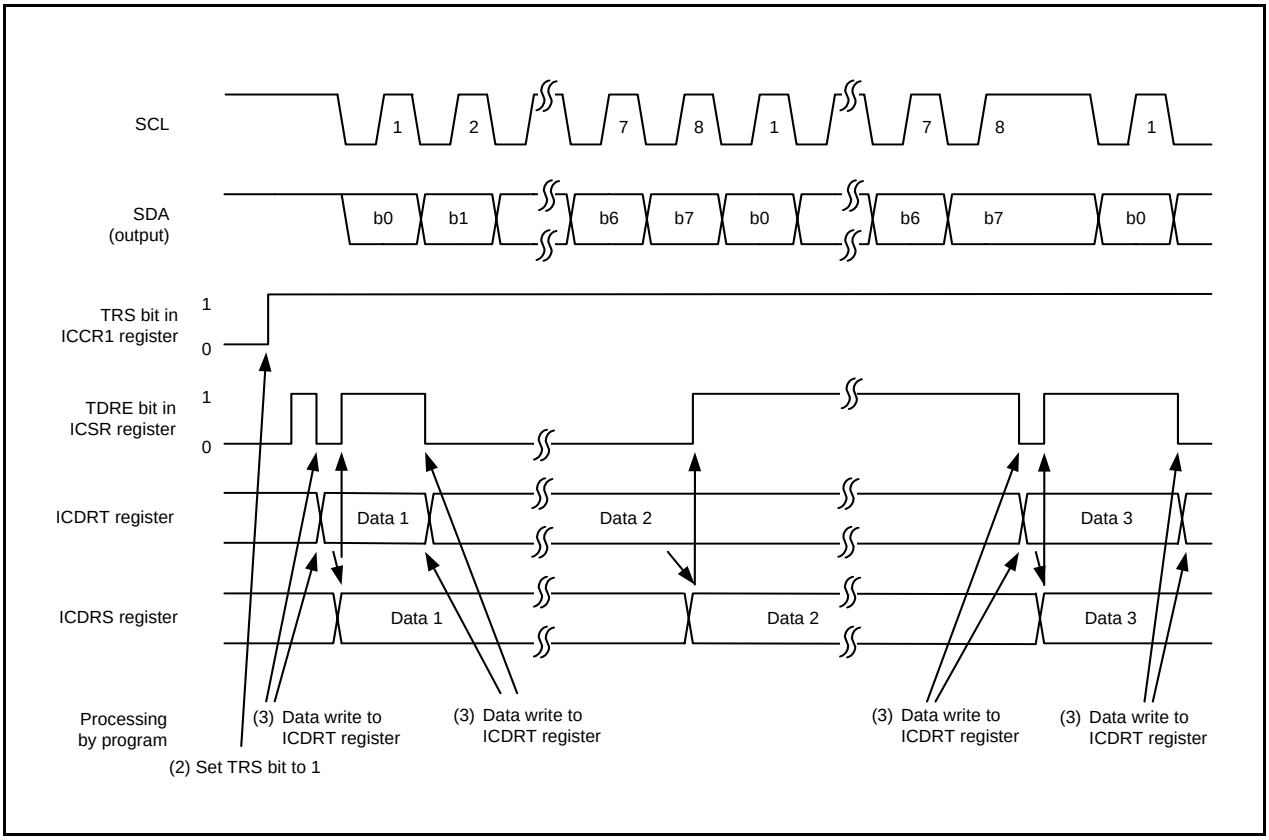


Figure 16.42 Operating Timing in Transmit Mode (Clock Synchronous Serial Mode)

16.3.4.3 Receive Operation

In receive mode, data is latched at the rising edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 16.43 shows the Operating Timing in Receive Mode (Clock Synchronous Serial Mode).

The receive procedure and operation in receive mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Set bits CKS0 to CKS3 in the ICCR1 register and set the MST bit (initial setting).
(2) The output of the receive clock starts when the MST bit is set to 1 while the transfer clock is being output.
(3) Data is transferred from registers ICDRS to ICDRR and the RDRF bit in the ICSR register is set to 1, when the receive operation is completed. Since the next byte of data is enabled when the MST bit is set to 1, the clock is output continuously. Continuous reception is enabled by reading the ICDRR register every time the RDRF bit is set to 1. An overrun is detected at the rise of the 8th clock cycle while the RDRF bit is set to 1, and the AL bit in the ICSR register is set to 1. At this time, the last receive data is retained in the ICDRR register.
(4) When the MST bit is set to 1, set the RCVD bit in the ICCR1 register to 1 (disables the next receive operation) and read the ICDRR register. The SCL signal is fixed “H” after reception of the following byte of data is completed.

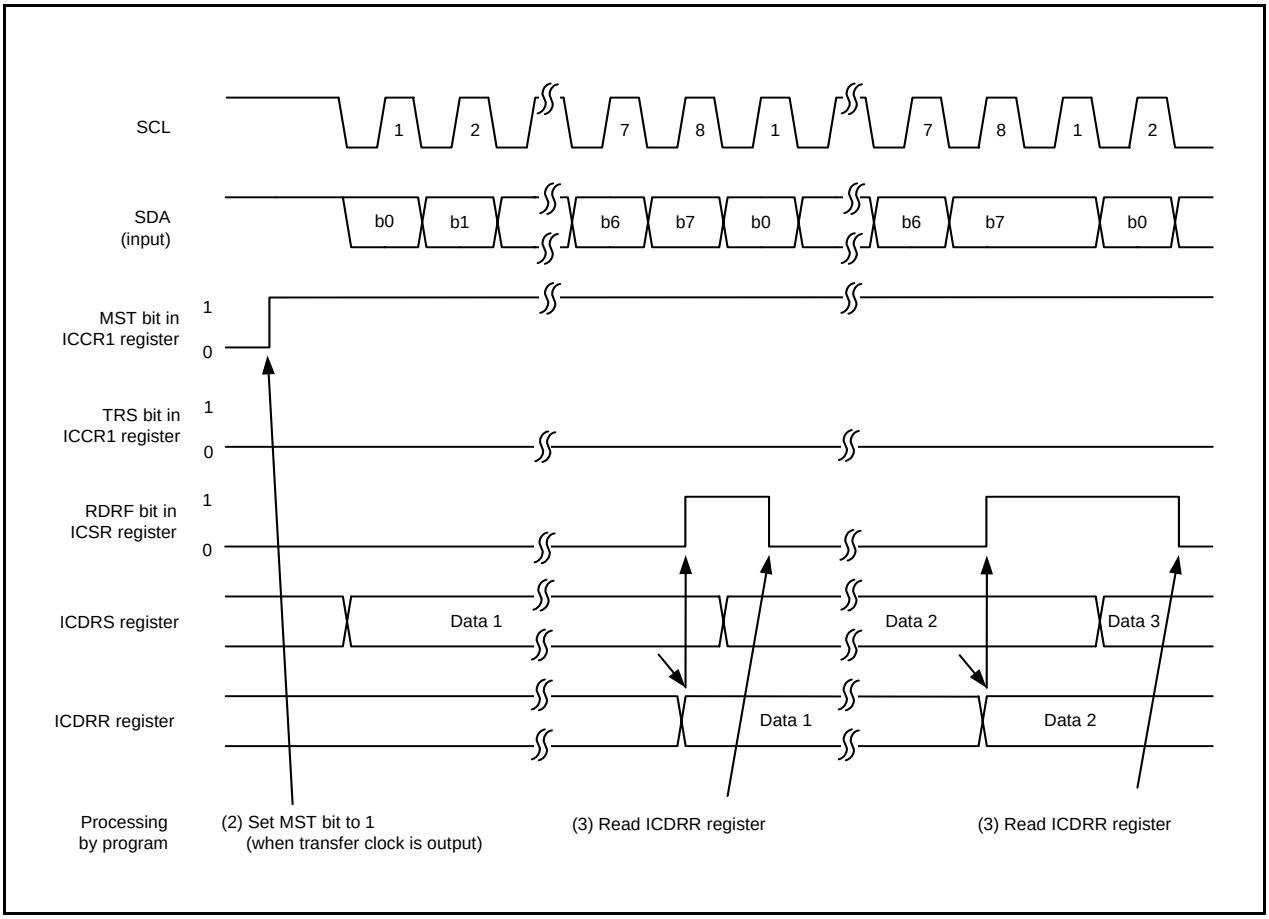


Figure 16.43 Operating Timing in Receive Mode (Clock Synchronous Serial Mode)

16.3.5 Noise Canceller

The states of pins SCL and SDA are routed through the noise canceller before being latched internally. Figure 16.44 shows a Block Diagram of Noise Canceller.

The noise canceller consists of two cascaded latch and match detector circuits. When the SCL pin input signal (or SDA pin input signal) is sampled on f1 and two latch outputs match, the level is passed forward to the next circuit. When they do not match, the former value is retained.

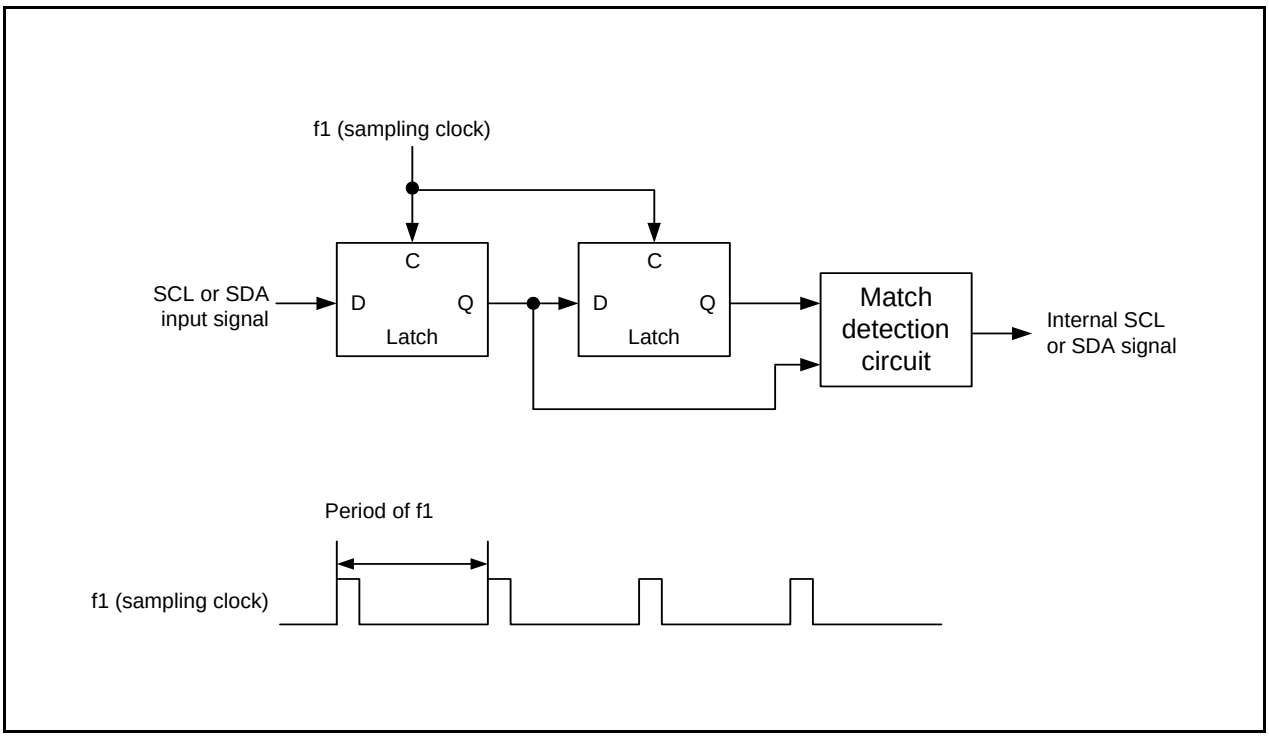


Figure 16.44 Block Diagram of Noise Canceller

16.3.6 Bit Synchronization Circuit

When setting the I^2C bus interface to master mode, the high-level period may become shorter in the following two cases:

- If the SCL signal is driven L level by a slave device
- If the rise speed of the SCL signal is reduced by a load (load capacity or pull-up resistor) on the SCL line.

Therefore, the SCL signal is monitored and communication is synchronized bit by bit.
Figure 16.45 shows the Timing of Bit Synchronization Circuit, and Table 16.8 lists the Time between Changing SCL Signal from “L” Output to High-Impedance and Monitoring of SCL Signal.

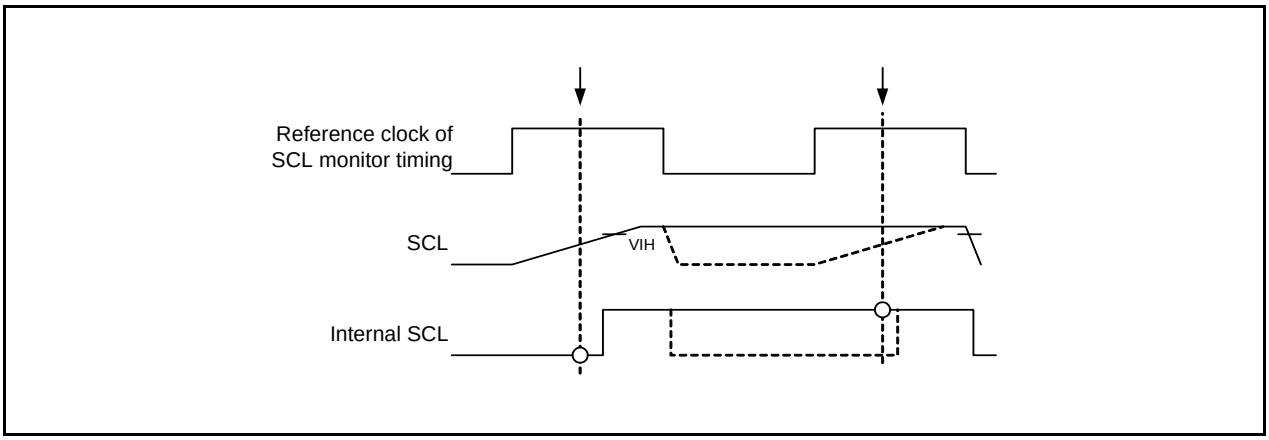


Figure 16.45 Timing of Bit Synchronization Circuit

Table 16.8 Time between Changing SCL Signal from “L” Output to High-Impedance and Monitoring of SCL Signal

ICCR1 Register		Time for Monitoring SCL
CKS3	CKS2	
0	0	7.5Tcyc
	1	19.5Tcyc
1	0	17.5Tcyc
	1	41.5Tcyc

1Tcyc = 1/f1(s)

16.3.7 Examples of Register Setting

Figures 16.46 to 16.49 show Examples of Register Setting When Using I²C bus interface.

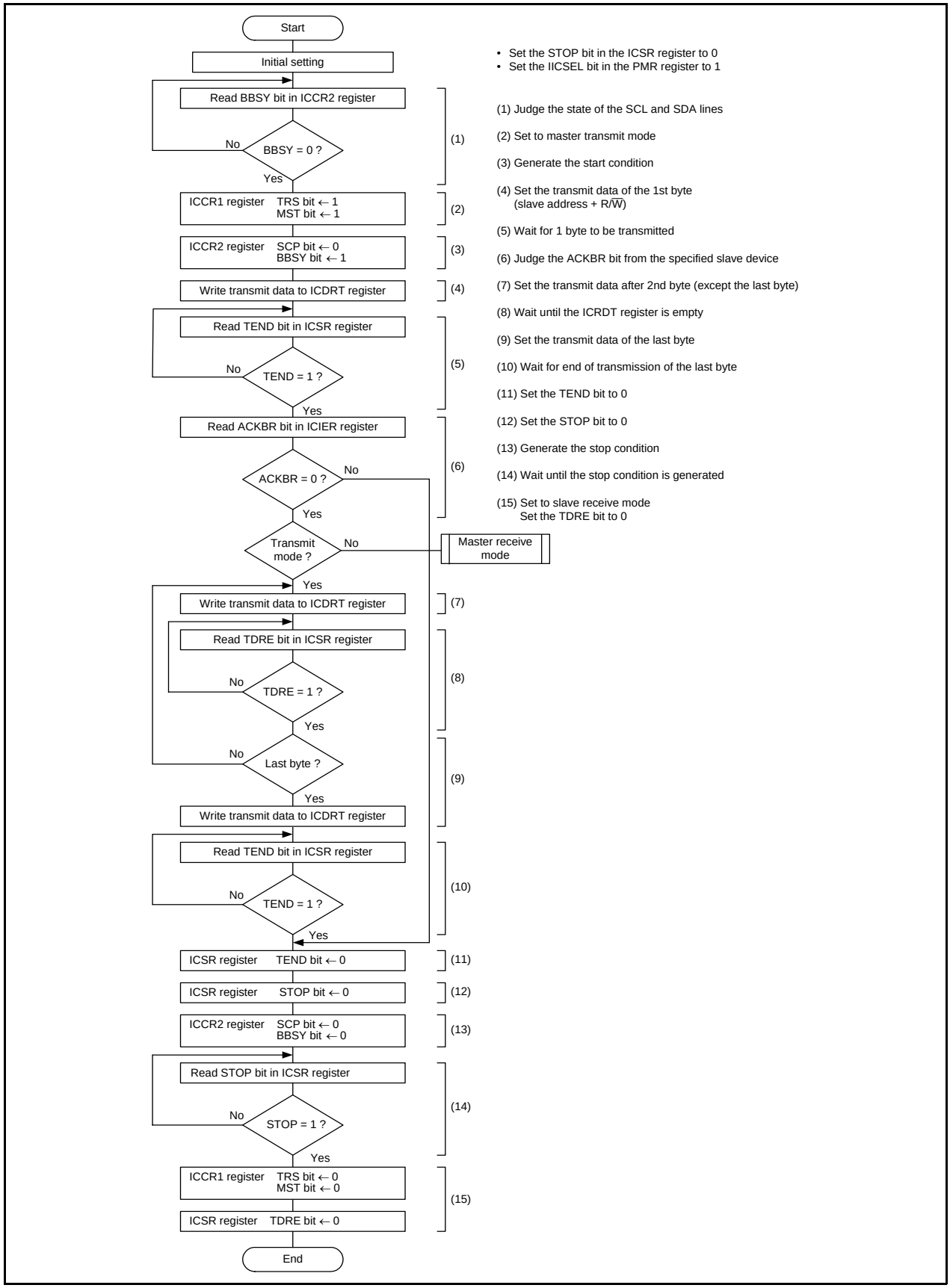
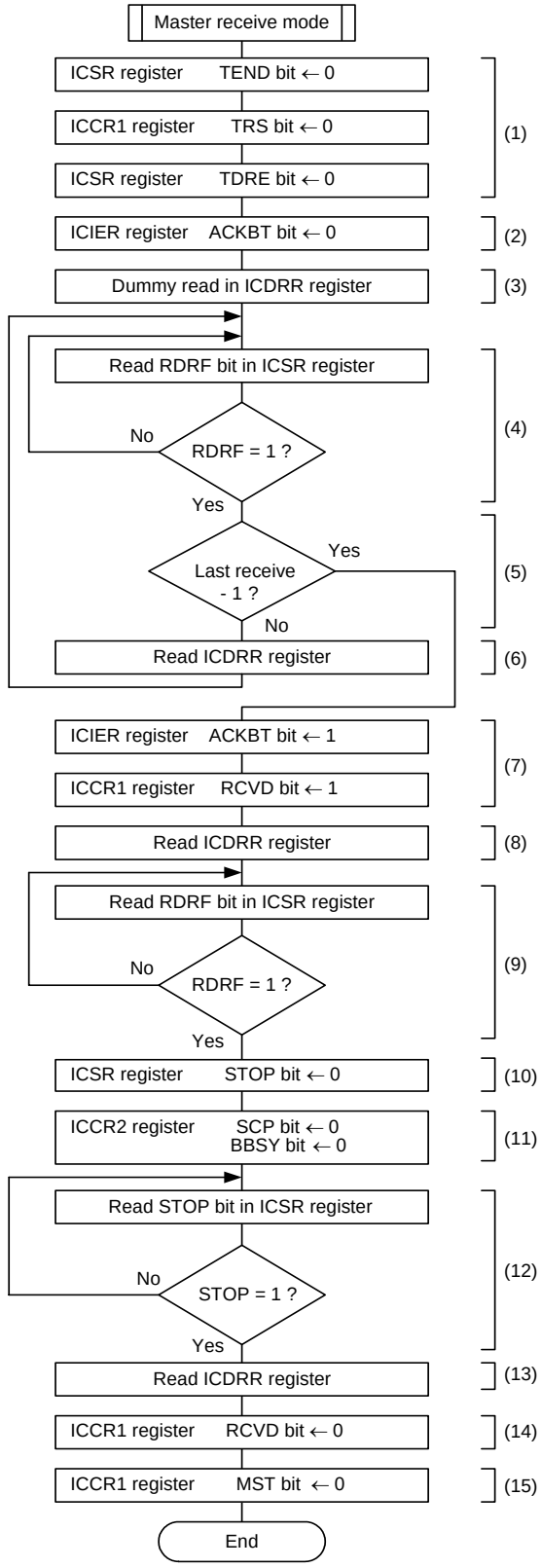


Figure 16.46 Example of Register Setting in Master Transmit Mode (I²C bus Interface Mode)



(1) Set the TEND bit to 0 and set to master receive mode. Set the TDRE bit to 0(1,2)

(2) Set the ACKBT bit to the transmit device(1)

(3) Dummy read the ICDRR register(1)

(4) Wait for 1 byte to be received

(5) Judge (last receive - 1)

(6) Read the receive data

(7) Set the ACKBT bit of the last byte and set to disable continuous receive operation (RCVD = 1)(2)

(8) Read the receive data of (last byte - 1)

(9) Wait until the last byte is received

(10) Set the STOP bit to 0

(11) Generate the stop condition

(12) Wait until the stop condition is generated

(13) Read the receive data of the last byte

(14) Set the RCVD bit to 0

(15) Set to slave receive mode

NOTES:
1. Do not generate the interrupt while processing steps (1) to (3).
2. When receiving 1 byte, skip steps (2) to (6) after (1) and jump to process of step (7). Processing step (8) is dummy read of the ICDRR register.

Figure 16.47 Example of Register Setting in Master Receive Mode (I^2C bus Interface Mode)

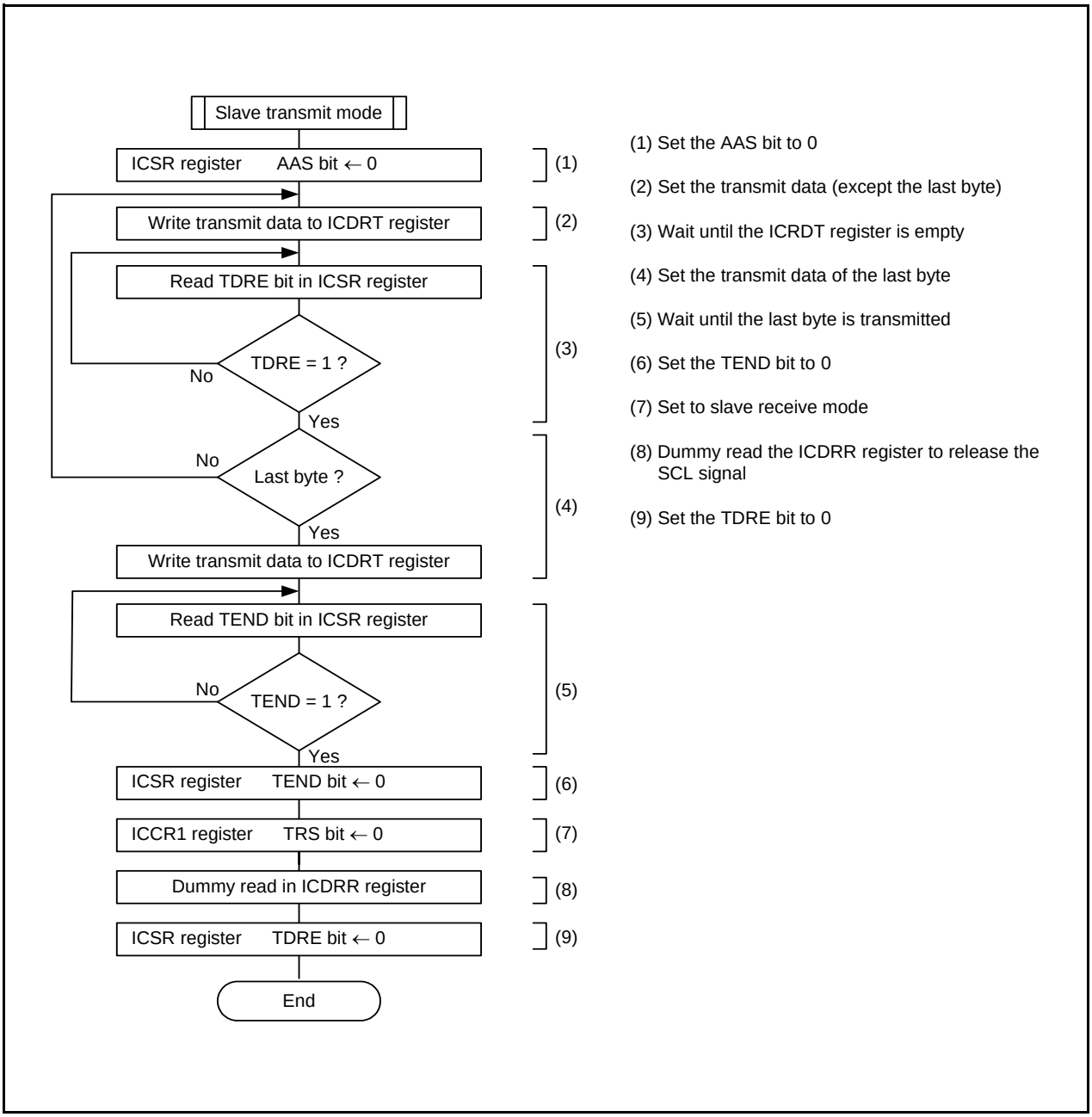


Figure 16.48 Example of Register Setting in Slave Transmit Mode (I^2C bus Interface Mode)

NOTE:
1. When receiving 1 byte, skip steps (2) to (6) after (1) and jump to processing step (7). Processing step (8) is dummy read of the ICDRR register.

Figure 16.49 Example of Register Setting in Slave Receive Mode (I^2C bus Interface Mode)

16.3.8 Notes on I²C bus Interface

Set the IICSEL bit in the PMR register to 1 (select I²C bus interface function) to use the I²C bus interface.

16.3.8.1 Multimaster Operation

The following actions must be performed to use the I²C bus interface in multimaster operation.

- Transfer rate
  Set the transfer rate by 1/1.8 or faster than the fastest rate of the other masters. For example, if the fastest transfer rate of the other masters is set to 400 kbps, the I²C-bus transfer rate in this MCU should be set to 223 kbps (= 400/1.18) or more.

- Bits MST and TRS in the ICCR1 register setting

(a) Use the MOV instruction to set bits MST and TRS.
(b) When arbitration is lost, confirm the contents of bits MST and TRS. If the contents are other than the MST bit set to 0 and the TRS bit set to 0 (slave receive mode), set the MST bit to 0 and the TRS bit to 0 again.

16.3.8.2 Master Receive Mode

Either of the following actions must be performed to use the I²C bus interface in master receive mode.

(a) In master receive mode while the RDRF bit in the ICSR register is set to 1, read the ICDRR register before the rising edge of the 8th clock.
(b) In master receive mode, set the RCVD bit in the ICCR1 register to 1 (disables the next receive operation) to perform 1-byte communications.

17. Hardware LIN

The hardware LIN performs LIN communication in cooperation with timer RA and UART0.

17.1 Features

The hardware LIN has the features listed below.
Figure 17.1 shows a Block Diagram of Hardware LIN.

Master mode
- Generates Synch Break
- Detects bus collision

Slave mode
- Detects Synch Break
- Measures Synch Field
- Controls Synch Break and Synch Field signal inputs to UART0
- Detects bus collision

NOTE:
1. The WakeUp function is detected by INT1.

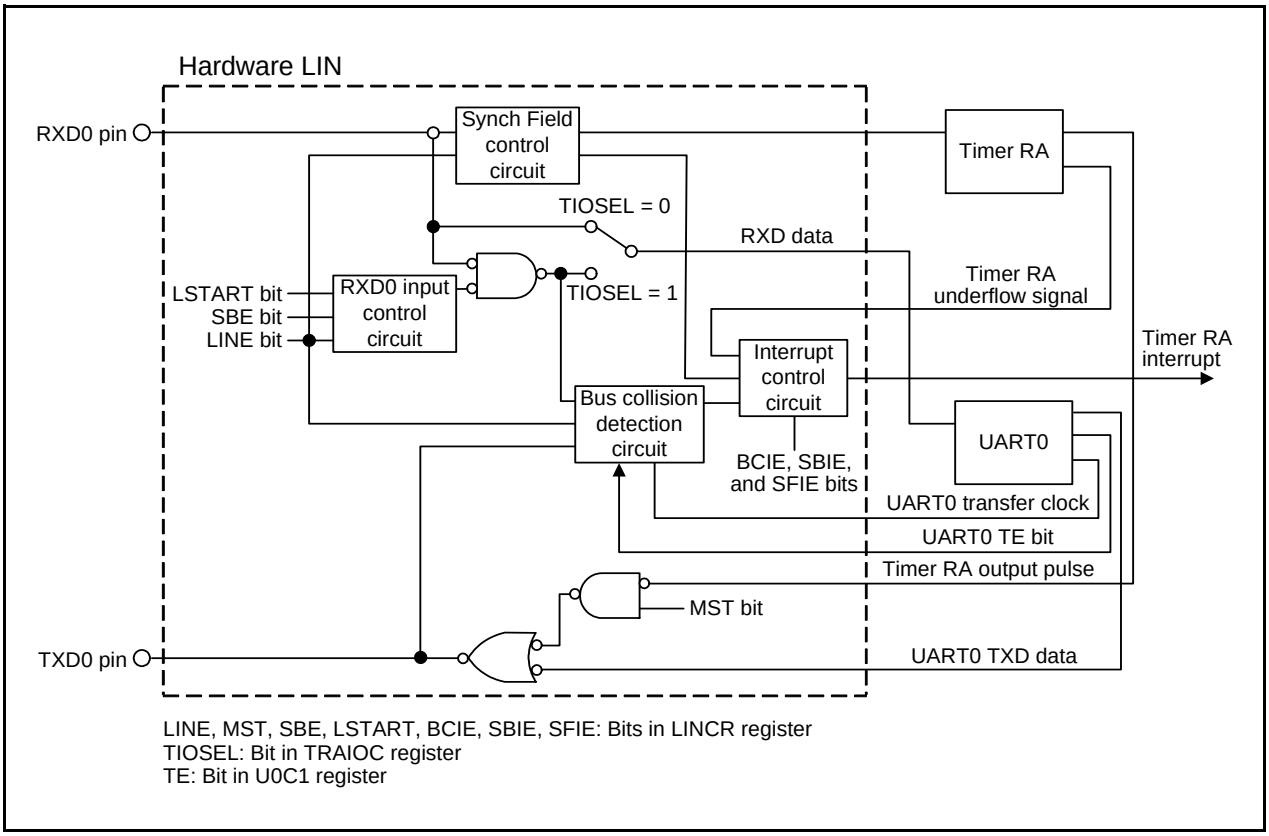


Figure 17.1 Block Diagram of Hardware LIN

17.2 Input/Output Pins

The pin configuration of the hardware LIN is listed in Table 17.1.

Table 17.1 Pin Configuration

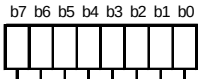
Name	Abbreviation	Input/Output	Function
Receive data input	RXD0	Input	Receive data input pin of the hardware LIN
Transmit data output	TXD0	Output	Transmit data output pin of the hardware LIN

17.3 Register Configuration

The hardware LIN contains the registers listed below.
These registers are detailed in Figures 17.2 and 17.3.

- LIN Control Register (LINCR)
- LIN Status Register (LINST)

LIN Control Register



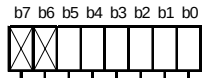
Symbol	Address	After Reset
LINCR	0106h	00h

Bit Symbol	Bit Name	Function	RW
SFIE	Synch Field measurement-completed interrupt enable bit	0 : Disables Synch Field measurement-completed interrupt 1 : Enables Synch Field measurement-completed interrupt	RW
SBIE	Synch Break detection interrupt enable bit	0 : Disables Synch Break detection interrupt 1 : Enables Synch Break detection interrupt	RW
BCIE	Bus collision detection interrupt enable bit	0 : Disables bus collision detection interrupt 1 : Enables bus collision detection interrupt	RW
RXDSF	RXD0 input status flag	0 : RXD0 input enabled 1 : RXD0 input disabled	RO
LSTART	Synch Break detection start bit(1)	When this bit is set to 1, timer RA input is enabled and RXD0 input is disabled. When read, the content is 0.	RW
SBE	RXD0 input unmasking timing select bit (effective only in slave mode)	0 : Unmasked after Synch Break is detected 1 : Unmasked after Synch Field measurement is completed	RW
MST	LIN operation mode setting bit(2)	0 : Slave mode (Synch Break detection circuit actuated) 1 : Master mode (timer RA output OR'ed with TXD0)	RW
LINE	LIN operation start bit	0 : Causes LIN to stop 1 : Causes LIN to start operating(3)	RW

NOTES:
1. After setting the LSTART bit, confirm that the RXDSF flag is set to 1 before Synch Break input starts.
2. Before changing LIN operation modes, temporarily stop the LIN operation (LINE bit = 0).
3. Inputs to timer RA and UART0 are prohibited immediately after this bit is set to 1. (Refer to **Figure 17.5 Example of Header Field Transmission Flowchart (1)** and **Figure 17.9 Example of Header Field Reception Flowchart (2)**.)

Figure 17.2 LINCR Register

LIN Status Register



Symbol	Address	After Reset
LINST	0107h	00h

Bit Symbol	Bit Name	Function	RW
SFDCT	Synch Field measurement-completed flag	1 shows Synch Field measurement completed.	RO
SBDCT	Synch Break detection flag	1 shows Synch Break detected or Synch Break generation completed.	RO
BCDCT	Bus collision detection flag	1 shows Bus collision detected	RO
B0CLR	SFDCT bit clear bit	When this bit is set to 1, the SFDCT bit is set to 0. When read, the content is 0.	RW
B1CLR	SBDCT bit clear bit	When this bit is set to 1, the SBDCT bit is set to 0. When read, the content is 0.	RW
B2CLR	BCDCT bit clear bit	When this bit is set to 1, the BCDCT bit is set to 0. When read, the content is 0.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 17.3 LINST Register

17.4 Functional Description

17.4.1 Master Mode

Figure 17.4 shows typical operation of the hardware LIN when transmitting a header field in master mode. Figures 17.5 and 17.6 show a flowchart of the procedure for transmitting a header field.
When transmitting a header field, the hardware LIN operates as described below.

(1) When the TSTART bit in the TRACR register for timer RA is set by writing 1 in software, the hardware LIN outputs “L” level from the TXD0 pin for the period that is set in registers TRAPRE and TRA for timer RA.
(2) When timer RA underflows upon reaching the terminal count, the hardware LIN reverses the output of the TXD0 pin and sets the SBDCT flag in the LINST register to 1. Furthermore, if the SBIE bit in the LINCR register is set to 1, it generates a timer RA interrupt.
(3) The hardware LIN transmits 55h via UART0.
(4) The hardware LIN transmits an ID field via UART0 after it finishes sending 55h.
(5) The hardware LIN performs communication for a response field after it finishes sending the ID field.

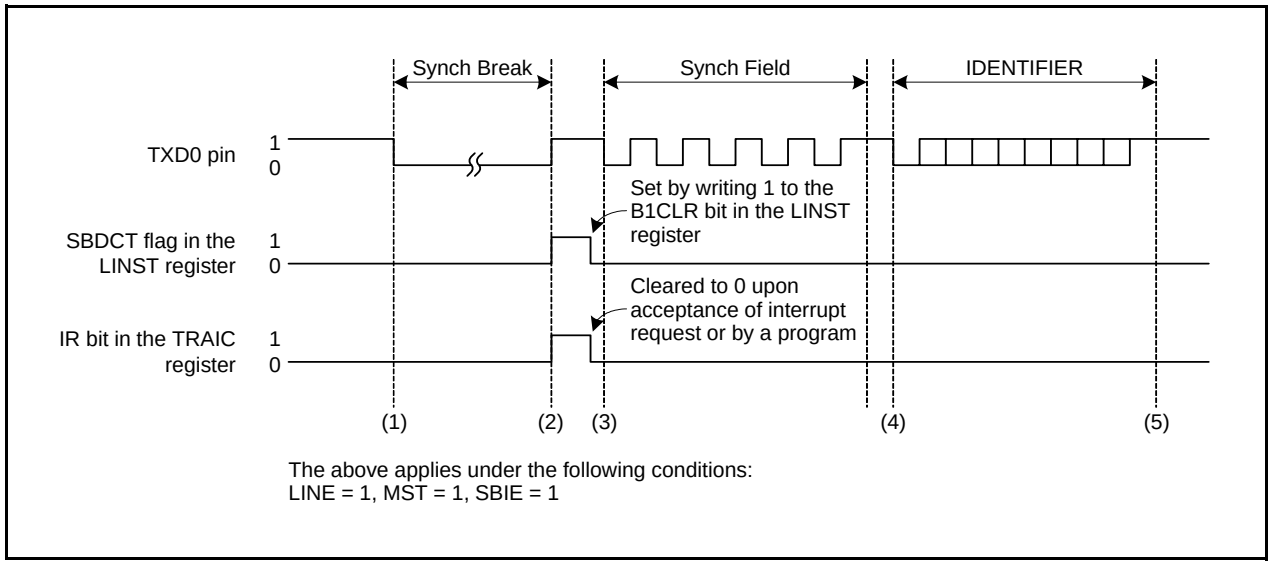


Figure 17.4 Typical Operation when Sending a Header Field

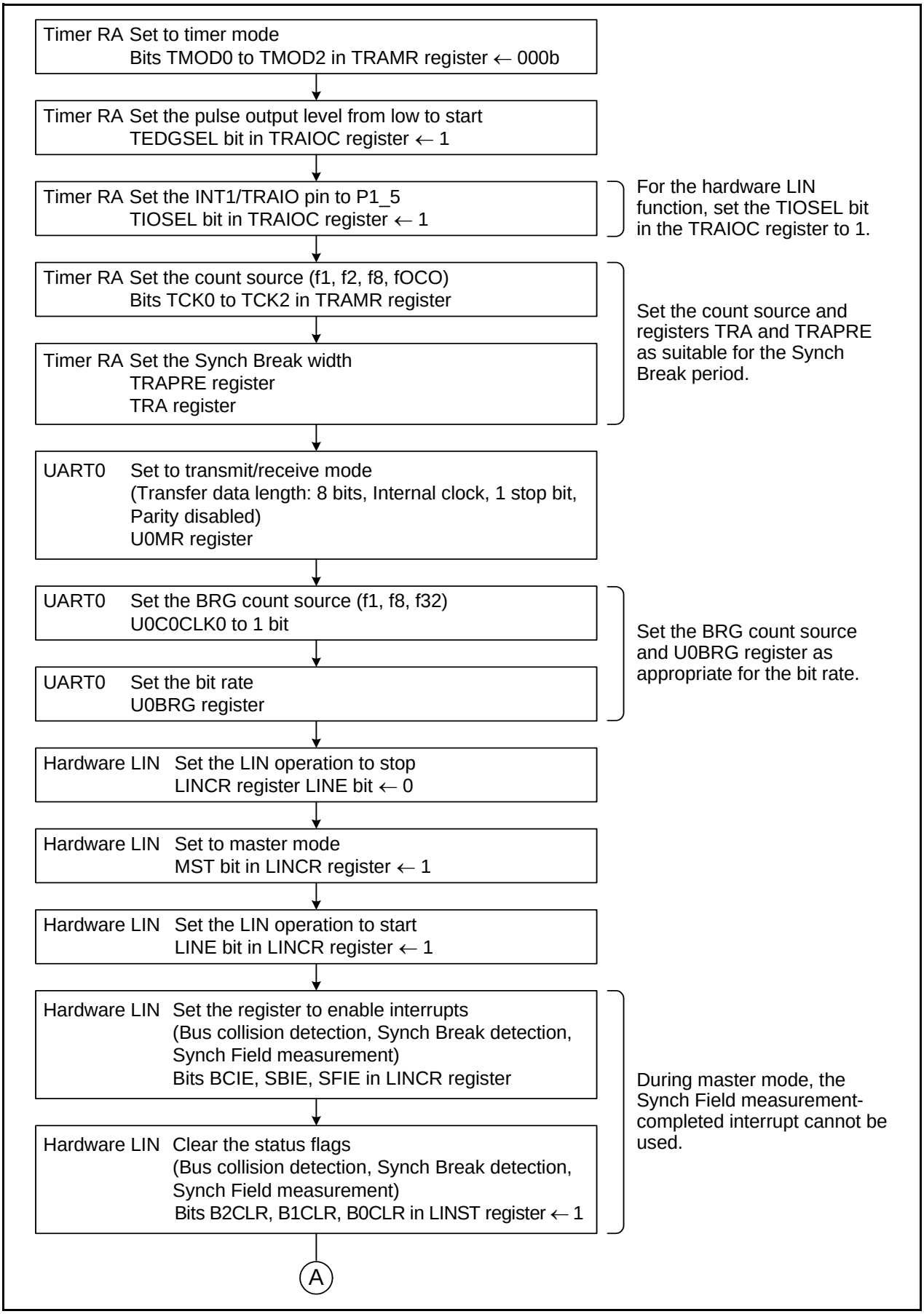


Figure 17.5 Example of Header Field Transmission Flowchart (1)

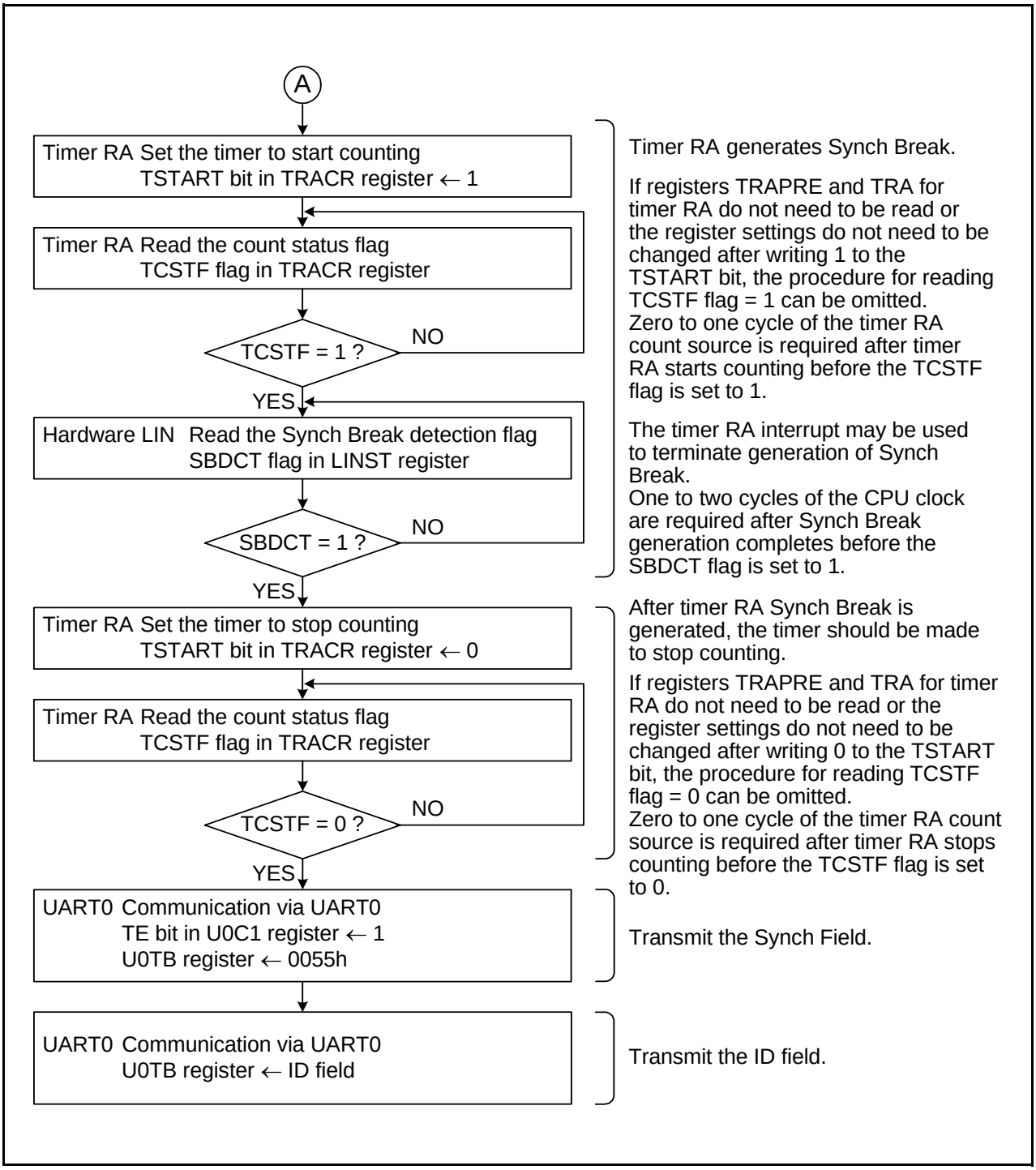


Figure 17.6 Example of Header Field Transmission Flowchart (2)

17.4.2 Slave Mode

Figure 17.7 shows typical operation of the hardware LIN when receiving a header field in slave mode. Figure 17.8 through Figure 17.10 show a flowchart for the procedure for receiving a header field.
When receiving a header field, the hardware LIN operates as described below.

(1) Synch Break detection is enabled by writing 1 to the LSTART bit in the LINCR register of the hardware LIN.
(2) When "L" level is input for a duration equal to or greater than the period set in timer RA, the hardware LIN detects it as Synch Break. At this time, the SBDCT flag in the LINST register is set to 1. Furthermore, if the SBIE bit in the LINCR register is set to 1, the hardware LIN generates a timer RA interrupt. Then it goes to Synch Field measurement.
(3) The hardware LIN receives a Synch Field (55h). At this time, it measures the period of the start bit and bits 0 to 6 by using timer RA. In this case, it is possible to select whether to input the Synch Field signal to RXD0 of UART0 by setting the SBE bit in the LINCR register accordingly.
(4) The hardware LIN sets the SFDCT flag in the LINST register to 1 when it finishes measuring the Synch Field. Furthermore, if the SFIE bit in the LINCR register is set to 1, it generates a timer RA interrupt.
(5) After it finishes measuring the Synch Field, calculate a transfer rate from the count value of timer RA and set to UART0 and registers TRAPRE and TRA of timer RA again.
(6) The hardware LIN performs communication for a response field after it finishes receiving the ID field.

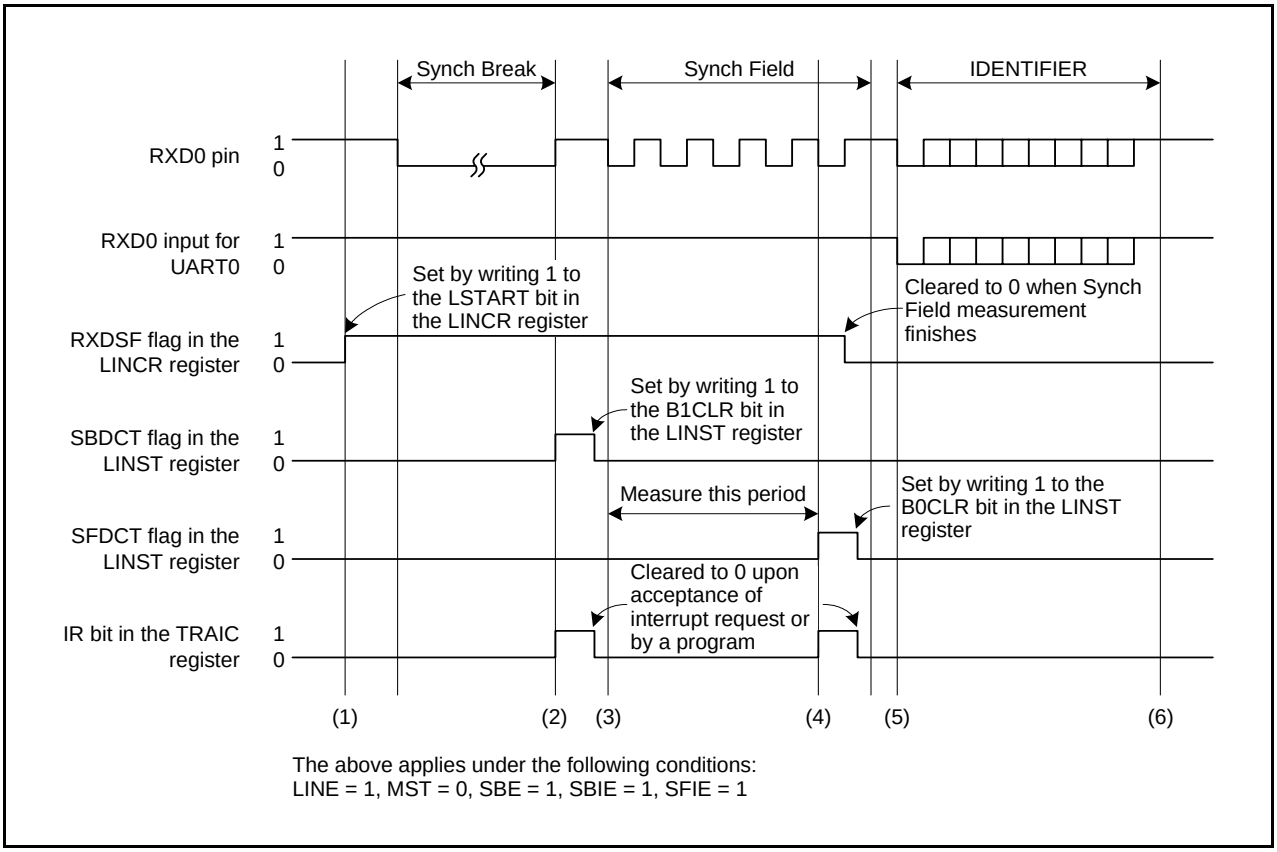


Figure 17.7 Typical Operation when Receiving a Header Field

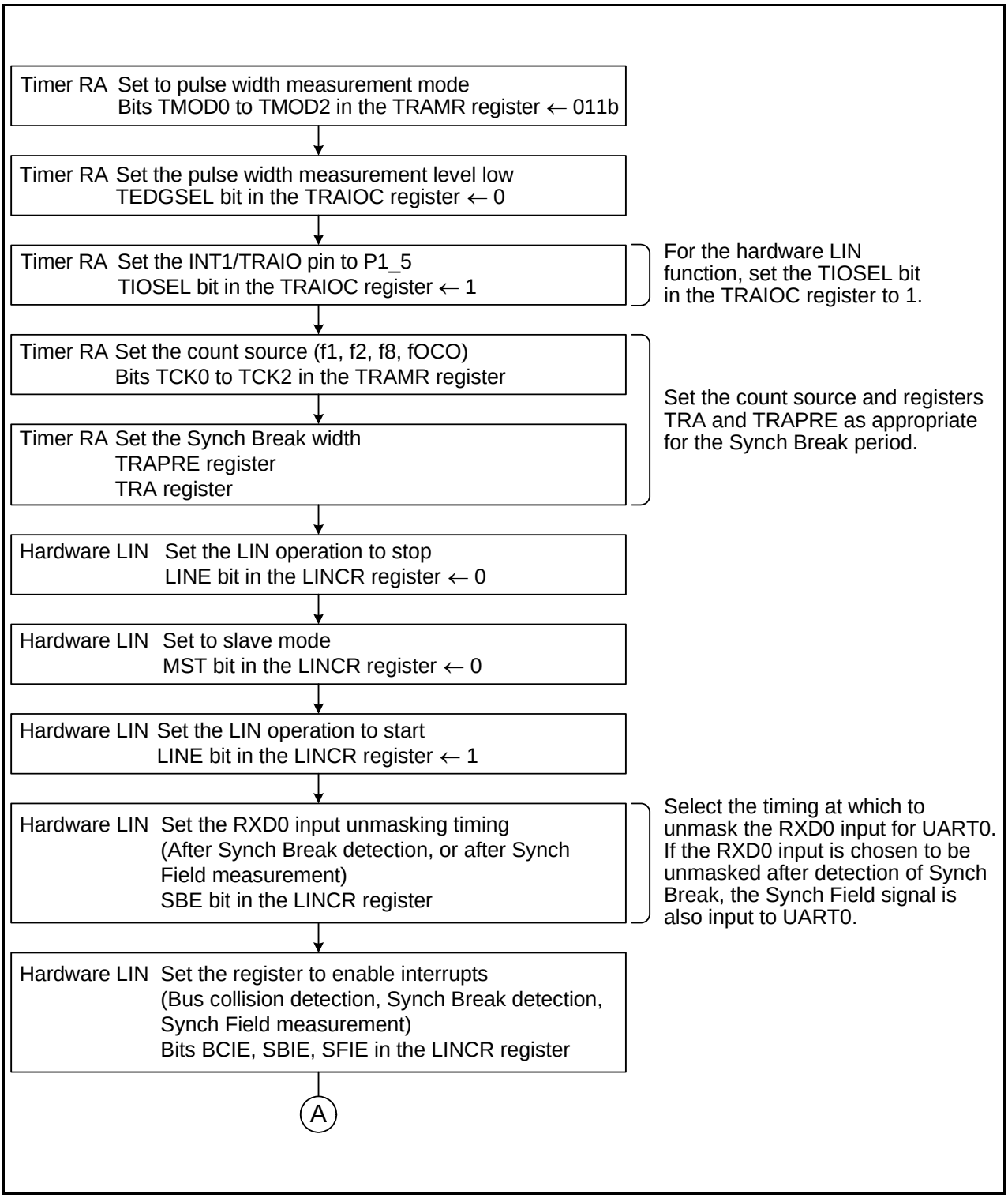


Figure 17.8 Example of Header Field Reception Flowchart (1)

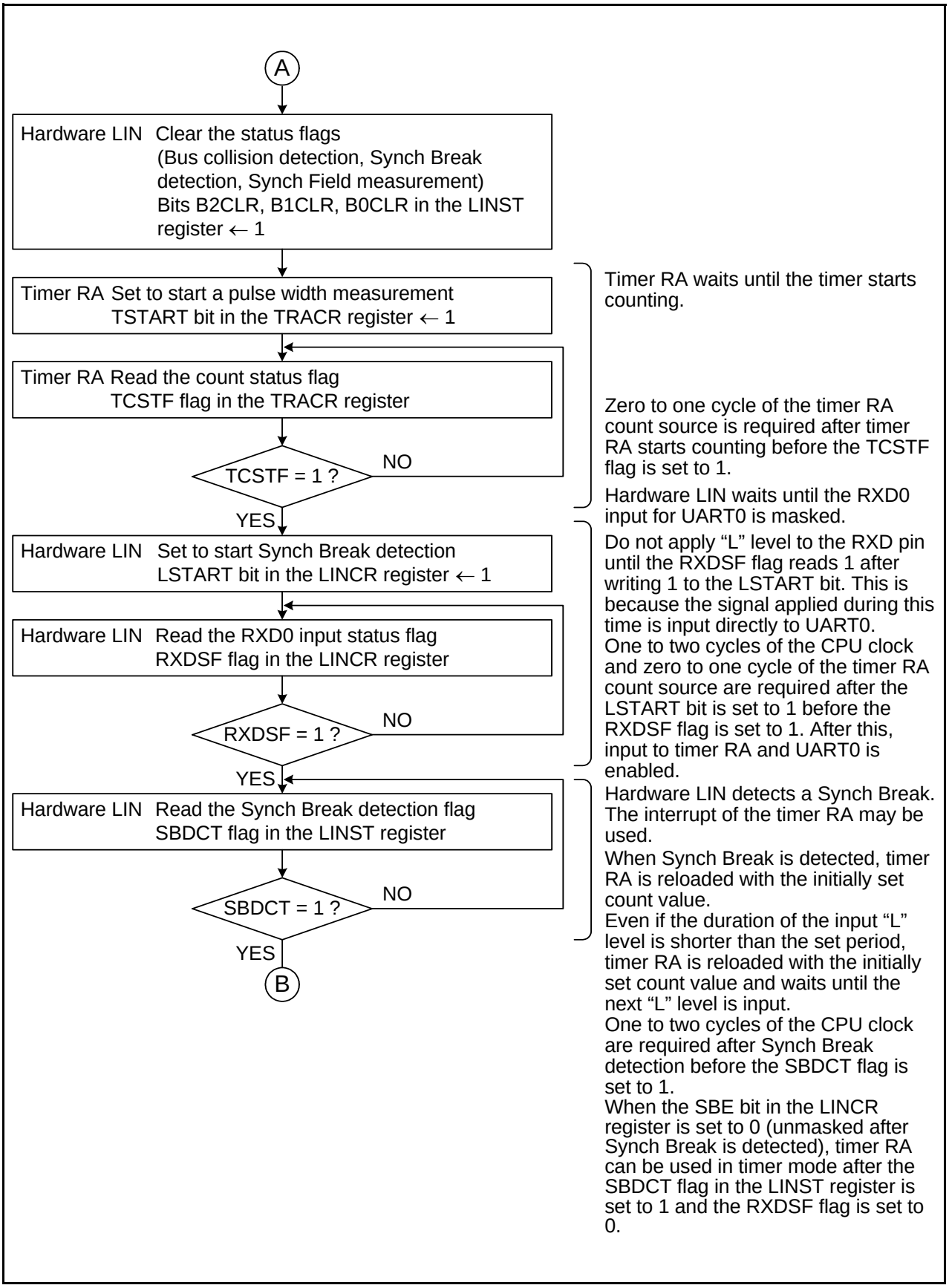


Figure 17.9 Example of Header Field Reception Flowchart (2)

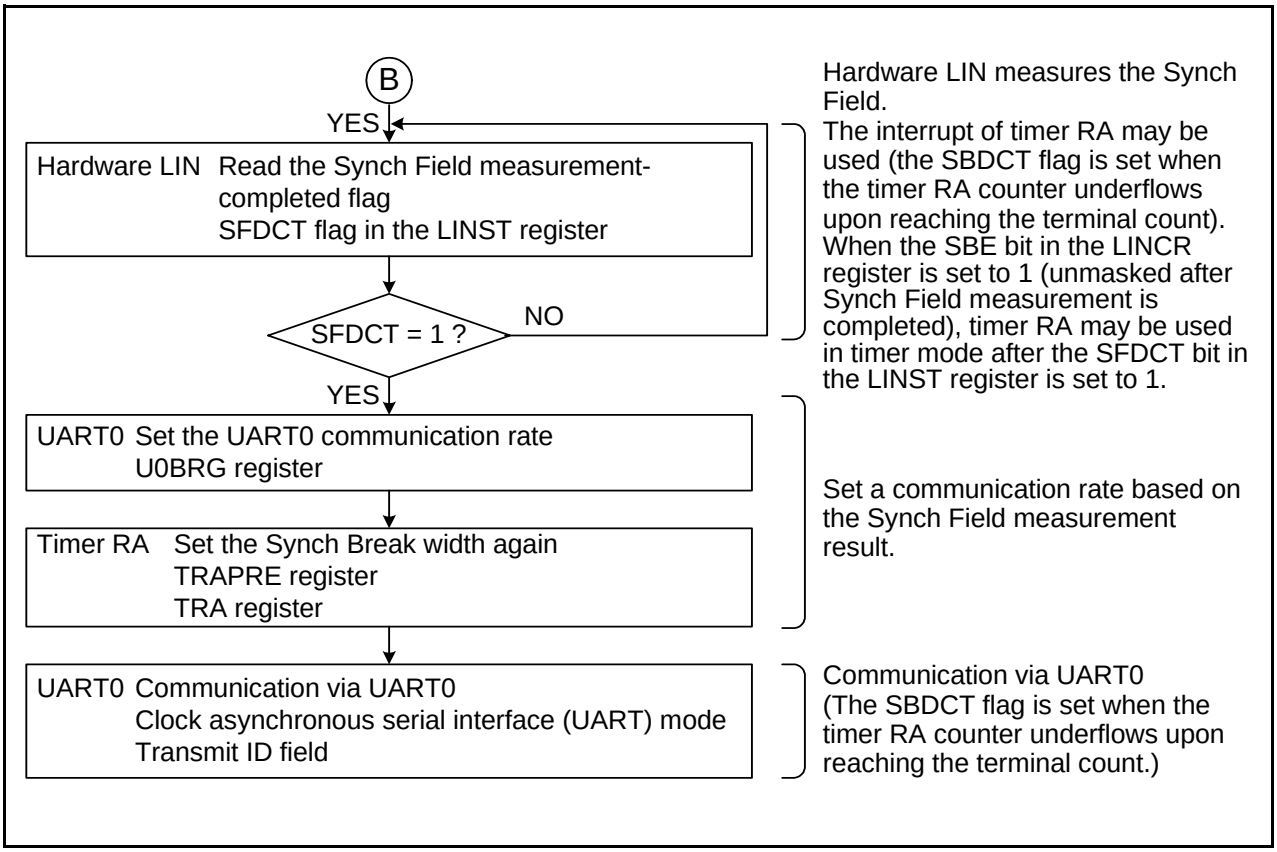


Figure 17.10 Example of Header Field Reception Flowchart (3)

17.4.3 Bus Collision Detection Function

The bus collision detection function can be used when UART0 is enabled for transmission (TE bit in the U0C1 register = 1).
Figure 17.11 shows the Typical Operation when a Bus Collision is Detected.

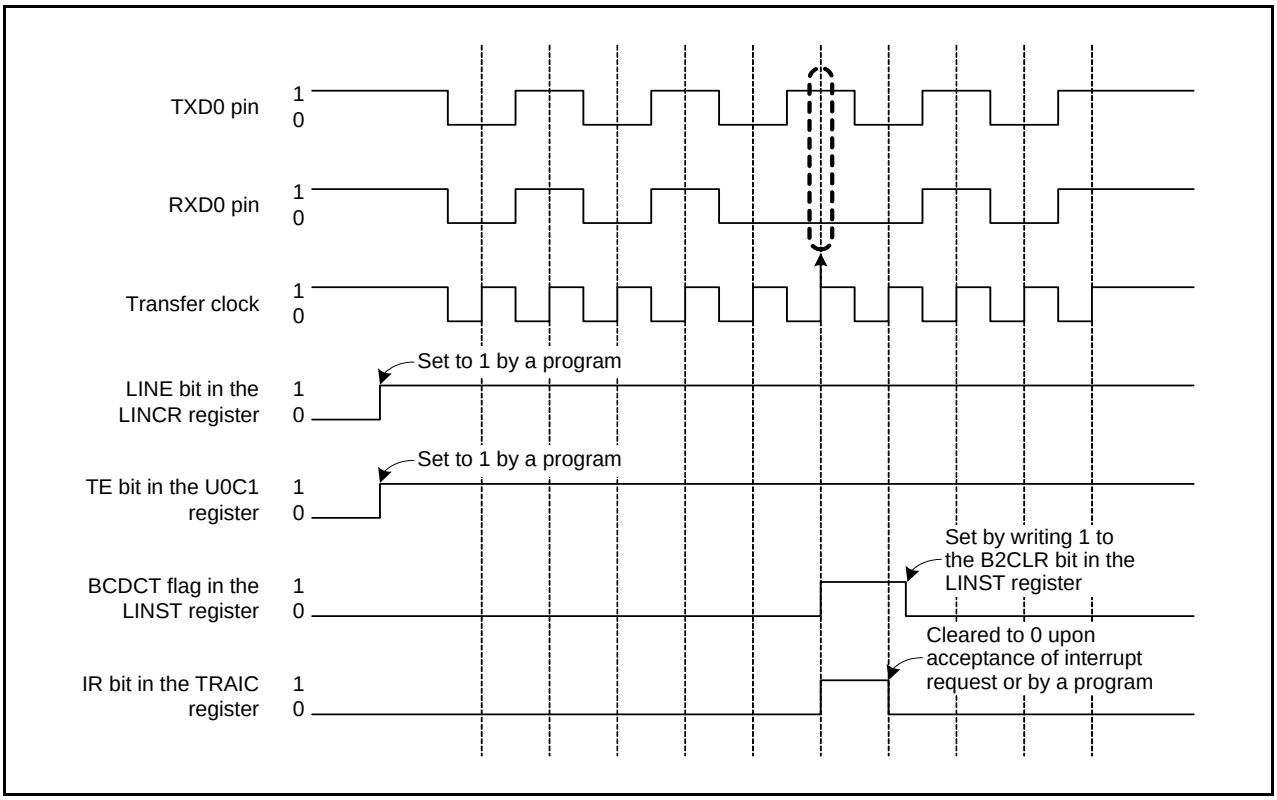


Figure 17.11 Typical Operation when a Bus Collision is Detected

17.4.4 Hardware LIN End Processing

Figure 17.12 shows an Example of Hardware LIN Communication Completion Flowchart.
Use the following timing for hardware LIN end processing:

- If the hardware bus collision detection function is used
  Perform hardware LIN end processing after checksum transmission completes.
- If the bus collision detection function is not used
  Perform hardware LIN end processing after header field transmission and reception complete.

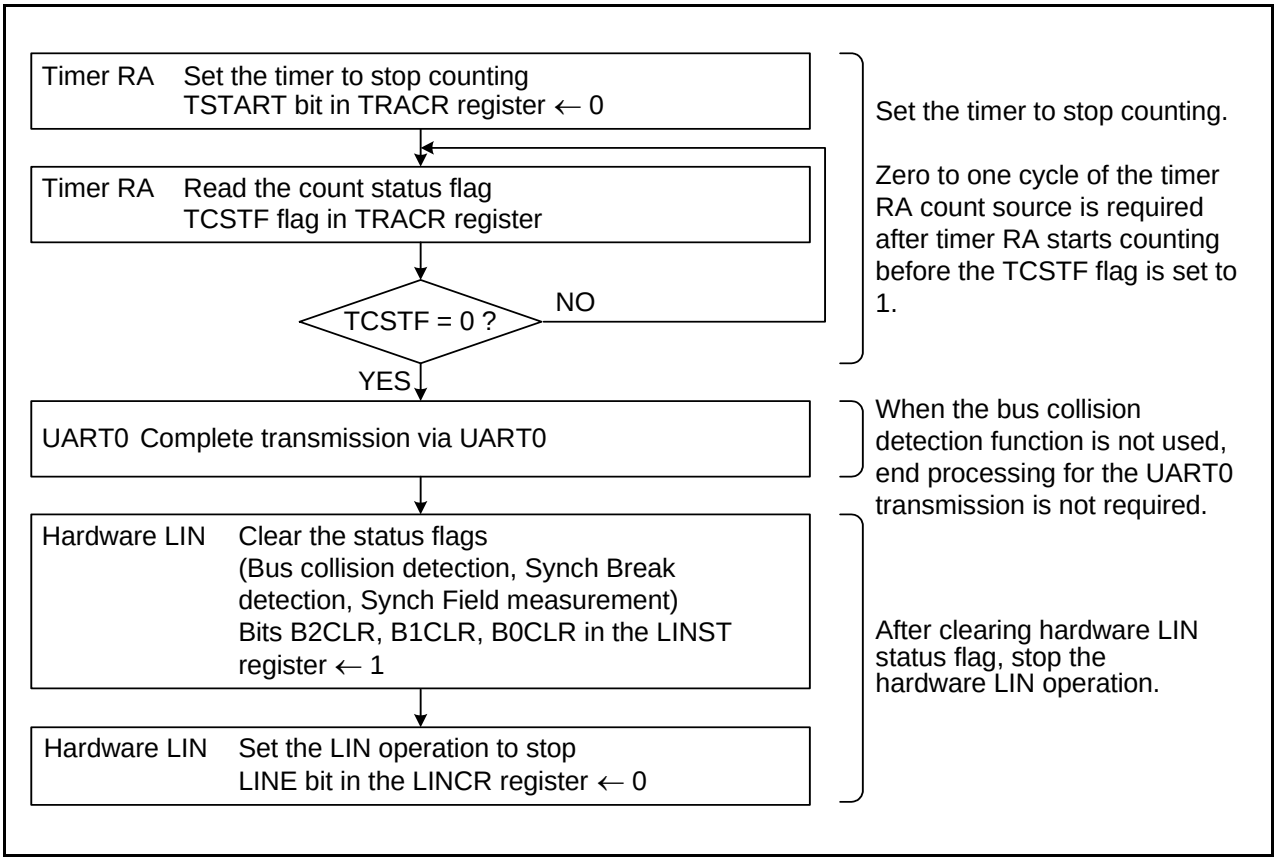


Figure 17.12 Example of Hardware LIN Communication Completion Flowchart

17.5 Interrupt Requests

There are four interrupt requests that are generated by the hardware LIN: Synch Break detection, Synch Break generation completed, Synch Field measurement, and bus collision detection. These interrupts are shared with timer RA.
Table 17.2 lists the Interrupt Requests of Hardware LIN.

Table 17.2 Interrupt Requests of Hardware LIN

Interrupt Request	Status Flag	Cause of Interrupt
Synch Break detection	SBDCT	Generated when timer RA has underflowed after measuring the “L” level duration of RXD0 input, or when a “L” level is input for a duration longer than the Synch Break period during communication.
Synch Break generation completed		Generated when “L” level output to TXD0 for the duration set by timer RA completes.
Synch Field measurement	SFDCT	Generated when measurement for 6 bits of the Synch Field by timer RA is completed.
Bus collision detection	BCDCT	Generated when the RXD0 input and TXD0 output values differed at data latch timing while UART0 is enabled for transmission.

17.6 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

18. A/D Converter

The A/D converter consists of one 10-bit successive approximation A/D converter circuit with a capacitive coupling amplifier. The analog input shares pins P0_0 to P0_7, and P1_0 to P1_3. Therefore, when using these pins, ensure that the corresponding port direction bits are set to 0 (input mode).
When not using the A/D converter, set the VCUT bit in the ADCON1 register to 0 (Vref unconnected) so that no current will flow from the VREF pin into the resistor ladder. This helps to reduce the power consumption of the chip.
The result of A/D conversion is stored in the AD register.
Table 18.1 lists the Performance of A/D converter. Figure 18.1 shows a Block Diagram of A/D Converter.
Figures 18.2 and 18.3 show the A/D converter-related registers.

Table 18.1 Performance of A/D converter

Item	Performance
A/D conversion method	Successive approximation (with capacitive coupling amplifier)
Analog input voltage(1)	0 V to AVCC
Operating clock ϕAD(2)	4.2 V ≤ AVCC ≤ 5.5 V f1, f2, f4, fOCO-F 2.2 V ≤ AVCC < 4.2 V f2, f4, fOCO-F
Resolution	8 bits or 10 bits selectable
Absolute accuracy	AVCC = Vref = 5 V, ϕAD = 10 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±3 LSB AVCC = Vref = 3.3 V, ϕAD = 10 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB AVCC = Vref = 2.2 V, ϕAD = 5 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB
Operating mode	One-shot and repeat(3)
Analog input pin	12 pins (AN0 to AN11)
A/D conversion start condition	• Software trigger Set the ADST bit in the ADCON0 register to 1 (A/D conversion starts) • Capture Timer RD interrupt request is generated while the ADST bit is set to 1
Conversion rate per pin	• Without sample and hold function 8-bit resolution: 49ϕAD cycles, 10-bit resolution: 59ϕAD cycles • With sample and hold function 8-bit resolution: 28ϕAD cycles, 10-bit resolution: 33ϕAD cycles

NOTES:
1. The analog input voltage does not depend on use of a sample and hold function.
   When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.
2. When 2.7 V ≤ AVCC ≤ 5.5 V, the frequency of ϕAD must be 10 MHz or below.
   When 2.2 V ≤ AVCC < 2.7 V, the frequency of ϕAD must be 5 MHz or below.
   Without a sample and hold function, the ϕAD frequency should be 250 kHz or above.
   With a sample and hold function, the ϕAD frequency should be 1 MHz or above.
3. In repeat mode, only 8-bit mode can be used.

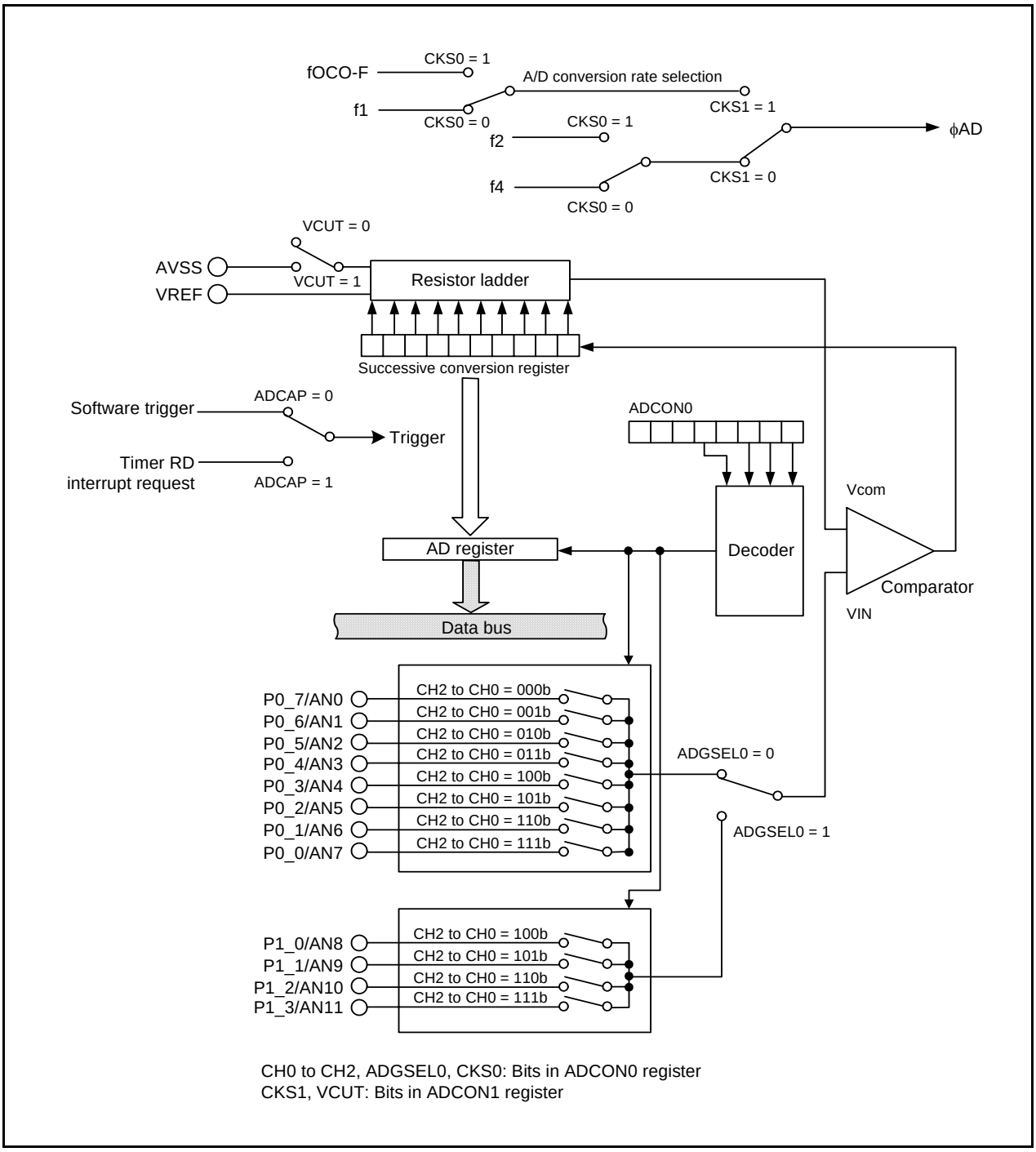
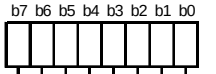


Figure 18.1 Block Diagram of A/D Converter

A/D Control Register 0(1)



Symbol	Address	After Reset
ADCON0	00D6h	00h

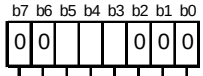
Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bits	(Note 4)	RW
CH1			RW
CH2			RW
MD	A/D operating mode select bit(2)	0 : One-shot mode 1 : Repeat mode	RW
ADGSEL0	A/D input group select bit(4)	0 : Selects port P0 group (AN0 to AN7) 1 : Selects port P1 group (AN8 to AN11)	RW
ADCAP	A/D conversion automatic start bit	0 : Starts at software trigger (ADST bit) 1 : Starts at timer RD (complementary PWM mode)	RW
ADST	A/D conversion start flag	0 : Stops A/D conversion 1 : Starts A/D conversion	RW
CKS0	Frequency select bit 0	[When CKS1 in ADCON1 register = 0] 0 : Selects f4 1 : Selects f2 [When CKS1 in ADCON1 register = 1] 0 : Selects f1(3) 1 : Selects fOCO-F	RW

NOTES:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.
2. When changing A/D operating mode, set the analog input pin again.
3. Set øAD frequency to 10 MHz or below.
4. The analog input pin can be selected according to a combination of bits CH0 to CH2 and the ADGSEL0 bit.

CH2 to CH0	ADGSEL0 = 0	ADGSEL0 = 1
000b	AN0	Do not set.
001b	AN1	
010b	AN2	
011b	AN3	
100b	AN4	AN8
101b	AN5	AN9
110b	AN6	AN10
111b	AN7	AN11

Figure 18.2 ADCON0 Register

A/D Control Register 1(1)

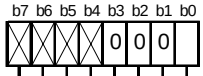


Symbol	Address	After Reset
ADCON1	00D7h	00h

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0.	RW
BITS	8/10-bit mode select bit(2)	0 : 8-bit mode 1 : 10-bit mode	RW
CKS1	Frequency select bit 1	Refer to the description of the CKS0 bit in the ADCON0 register function	RW
VCUT	Vref connect bit(3)	0 : Vref not connected 1 : Vref connected	RW
— (b6-b7)	Reserved bits	Set to 0.	RW

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.
2. Set the BITS bit to 0 (8-bit mode) in repeat mode.
3. When the VCUT bit is set to 1 (connected) from 0 (not connected), wait for 1 µs or more before starting A/D conversion.

A/D Control Register 2(1)

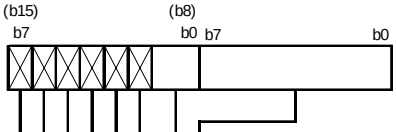


Symbol	Address	After Reset
ADCON2	00D4h	00h

Bit Symbol	Bit Name	Function	RW
SMP	A/D conversion method select bit	0 : Without sample and hold 1 : With sample and hold	RW
— (b3-b1)	Reserved bits	Set to 0.	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. If the ADCON2 register is rewritten during A/D conversion, the conversion result is undefined.

A/D Register



Symbol	Address	After Reset
AD	00C1h-00C0h	Undefined

Function		RW
When BITS bit in ADCON1 register is set to 1 (10-bit mode).	When BITS bit in ADCON1 register is set to 0 (8-bit mode).	RW
8 low-order bits in A/D conversion result	A/D conversion result	RO
2 high-order bits in A/D conversion result	When read, the content is undefined.	RO
Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 18.3 Registers ADCON1, ADCON2, and AD

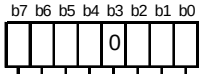
18.1 One-Shot Mode

In one-shot mode, the input voltage of one selected pin is A/D converted once.
Table 18.2 lists the One-Shot Mode Specifications. Figures 18.4 and 18.5 show Registers ADCON0 and ADCON1 in One-Shot Mode.

Table 18.2 One-Shot Mode Specifications

Item	Specification
Function	The input voltage of one pin selected by bits CH2 to CH0 and ADGSEL0 is A/D converted once
Start condition	• When the ADCAP bit is set to 0 (software trigger): Set the ADST bit to 1 (A/D conversion starts) • When the ADCAP bit is set to 1 (starts in timer RD (complementary PWM mode): A compare match between registers TRD0 and TRDGRA0 or a TRD1 underflow is generated while the ADST bit is set to 1
Stop condition	• A/D conversion completes (when the ADCAP bit is set to 0 (software trigger) ADST bit is set to 0) • Set the ADST bit to 0
Interrupt request generation timing	A/D conversion completes
Input pin	Select one of AN0 to AN11
Reading of A/D conversion result	Read AD register

A/D Control Register 0(1)



Symbol	Address	After Reset
ADCON0	00D6h	00h

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bits	(Note 4)	RW
CH1			RW
CH2			RW
MD	A/D operating mode select bit(2)	0 : One-shot mode	RW
ADGSEL0	A/D input group select bit(4)	0 : Selects port P0 group (AN0 to AN7) 1 : Selects port P1 group (AN8 to AN11)	RW
ADCAP	A/D conversion automatic start bit	0 : Starts at software trigger (ADST bit) 1 : Starts at timer RD (complementary PWM mode)	RW
ADST	A/D conversion start flag	0 : Stops A/D conversion 1 : Starts A/D conversion	RW
CKS0	Frequency select bit 0	[When CKS1 in ADCON1 register = 0] 0 : Selects f4 1 : Selects f2 [When CKS1 in ADCON1 register = 1] 0 : Selects f1(3) 1 : Selects fOCO-F	RW

NOTES:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.
2. After changing the A/D operating mode, select the analog input pin again.
3. Set øAD frequency to 10 MHz or below.
4. The analog input pin can be selected according to a combination of bits CH0 to CH2 and the ADGSEL0 bit.

CH2 to CH0	ADGSEL0 = 0	ADGSEL0 = 1
000b	AN0	Do not set.
001b	AN1	
010b	AN2	
011b	AN3	
100b	AN4	AN8
101b	AN5	AN9
110b	AN6	AN10
111b	AN7	AN11

Figure 18.4 ADCON0 Register in One-Shot Mode

A/D Control Register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1			0	0	0

Symbol	Address	After Reset
ADCON1	00D7h	00h

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0.	RW
BITS	8/10-bit mode select bit	0 : 8-bit mode 1 : 10-bit mode	RW
CKS1	Frequency select bit 1	Refer to the description of the CKS0 bit in the ADCON0 register function	RW
VCUT	Vref connect bit(2)	1 : Vref connected	RW
— (b6-b7)	Reserved bits	Set to 0.	RW

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.
2. When the VCUT bit is set to 1 (connected) from 0 (not connected), wait for 1 µs or more before starting A/D conversion.

Figure 18.5 ADCON1 Register in One-Shot Mode

18.2 Repeat Mode

In repeat mode, the input voltage of one selected pin is A/D converted repeatedly.
Table 18.3 lists the Repeat Mode Specifications. Figures 18.6 and 18.7 show Registers ADCON0 and ADCON1 in Repeat Mode.

Table 18.3 Repeat Mode Specifications

Item	Specification
Function	The Input voltage of one pin selected by bits CH2 to CH0 and ADGSEL0 is A/D converted repeatedly
Start conditions	• When the ADCAP bit is set to 0 (software trigger): Set the ADST bit to 1 (A/D conversion starts) • When the ADCAP bit is set to 1 (starts in timer RD (complementary PWM mode)): A compare match between registers TRD0 and TRDGRA0 or a TRD1 underflow is generated while the ADST bit is set to 1
Stop condition	Set the ADST bit to 0
Interrupt request generation timing	Not generated
Input pin	Select one of AN0 to AN11
Reading of result of A/D converter	Read AD register

A/D Control Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
				1			

Symbol	Address	After Reset
ADCON0	00D6h	00h

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bits	(Note 4)	RW
CH1			RW
CH2			RW
MD	A/D operating mode select bit(2)	1 : Repeat mode	RW
ADGSEL0	A/D input group select bit(4)	0 : Selects port P0 group (AN0 to AN7) 1 : Selects port P1 group (AN8 to AN11)	RW
ADCAP	A/D conversion automatic start bit	0 : Starts at software trigger (ADST bit) 1 : Starts at timer RD (complementary PWM mode)	RW
ADST	A/D conversion start flag	0 : Stops A/D conversion 1 : Starts A/D conversion	RW
CKS0	Frequency select bit 0	[When CKS1 in ADCON1 register = 0] 0 : Selects f4 1 : Selects f2 [When CKS1 in ADCON1 register = 1] 0 : Selects f1(3) 1 : Do not set.	RW

NOTES:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.
2. After changing A/D operation mode, select the analog input pin again.
3. Set øAD frequency to 10 MHz or below.
4. The analog input pin can be selected according to a combination of bits CH0 to CH2 and the ADGSEL0 bit.

CH2 to CH0	ADGSEL0 = 0	ADGSEL0 = 1
000b	AN0	Do not set.
001b	AN1	
010b	AN2	
011b	AN3	
100b	AN4	AN8
101b	AN5	AN9
110b	AN6	AN10
111b	AN7	AN11

Figure 18.6 ADCON0 Register in Repeat Mode

A/D Control Register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1		0	0	0	0

Symbol	Address	After Reset
ADCON1	00D7h	00h

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0.	RW
BITS	8/10-bit mode select bit(2)	0 : 8-bit mode	RW
CKS1	Frequency select bit 1	Refer to the description of the CKS0 bit in the ADCON0 register function	RW
VCUT	Vref connect bit(3)	1 : Vref connected	RW
— (b6-b7)	Reserved bits	Set to 0.	RW

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.
2. Set the BITS bit to 0 (8-bit mode) in repeat mode.
3. When the VCUT bit is set to 1 (connected) from 0 (not connected), wait for 1 µs or more before starting A/D conversion.

Figure 18.7 ADCON1 Register in Repeat Mode

18.3 Sample and Hold

When the SMP bit in the ADCON2 register is set to 1 (sample and hold function enabled), the A/D conversion rate per pin increases. The sample and hold function is available in all operating modes. Start A/D conversion after selecting whether the sample and hold circuit is to be used or not.
Figure 18.8 shows a Timing Diagram of A/D Conversion.

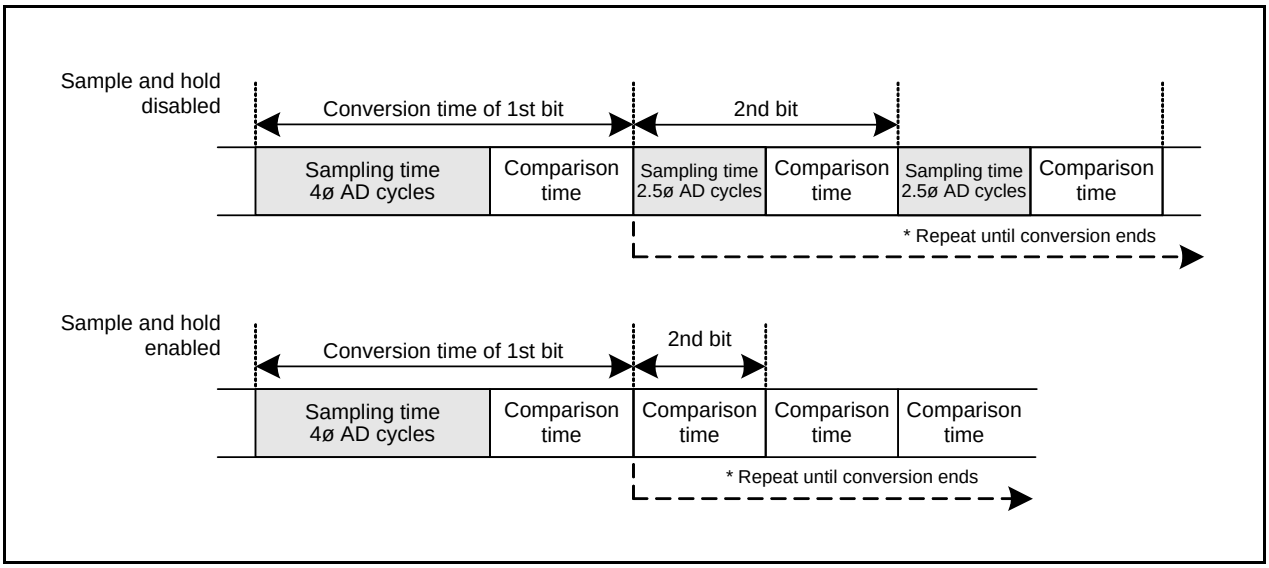
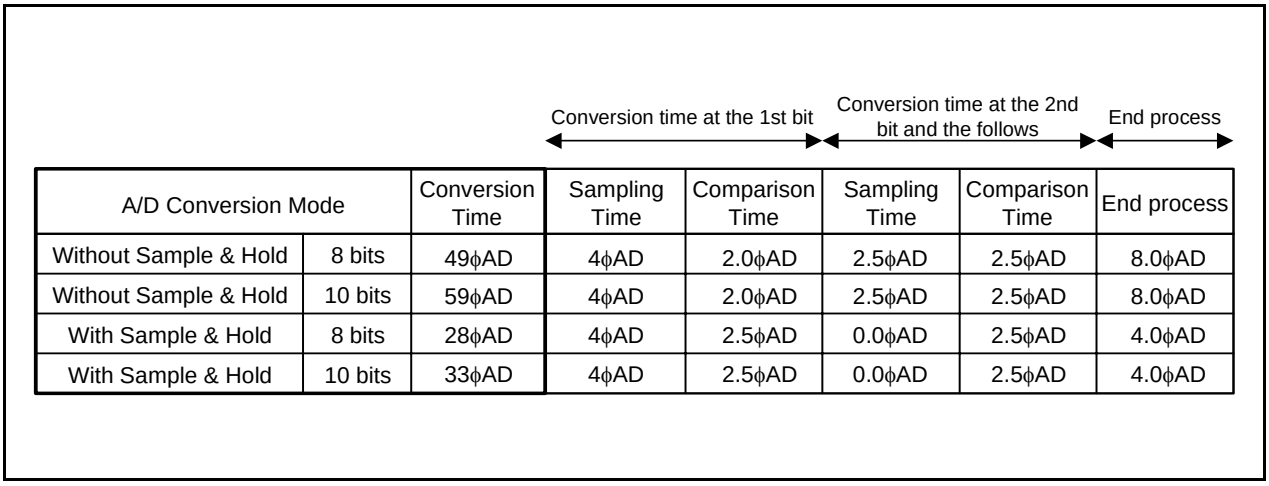


Figure 18.8 Timing Diagram of A/D Conversion

18.4 A/D Conversion Cycles

Figure 18.9 shows the A/D Conversion Cycles.

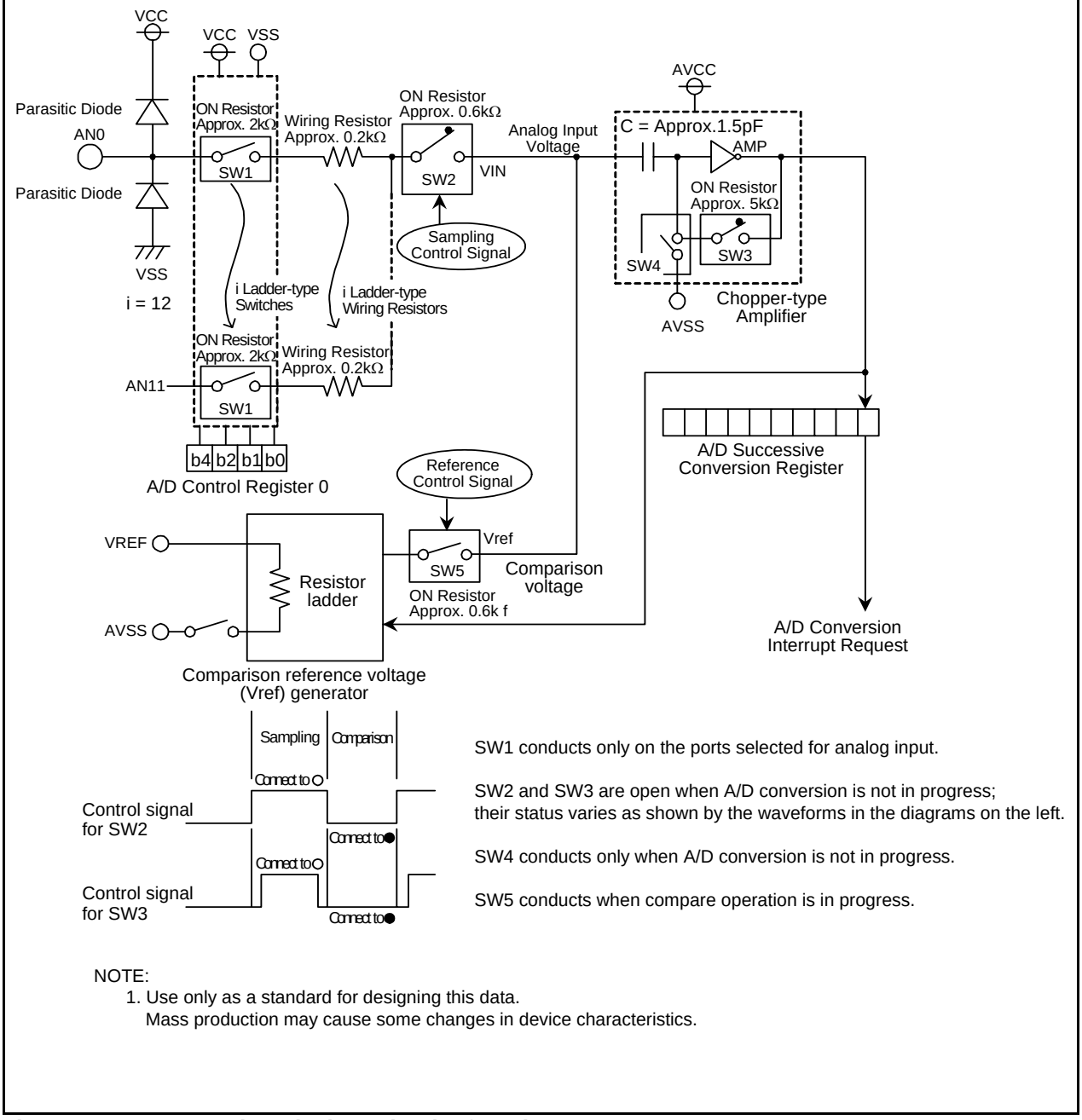


A/D Conversion Mode		Conversion Time	Sampling Time	Comparison Time	Sampling Time	Comparison Time	End process
Without Sample & Hold	8 bits	49ϕAD	4ϕAD	2.0ϕAD	2.5ϕAD	2.5ϕAD	8.0ϕAD
Without Sample & Hold	10 bits	59ϕAD	4ϕAD	2.0ϕAD	2.5ϕAD	2.5ϕAD	8.0ϕAD
With Sample & Hold	8 bits	28ϕAD	4ϕAD	2.5ϕAD	0.0ϕAD	2.5ϕAD	4.0ϕAD
With Sample & Hold	10 bits	33ϕAD	4ϕAD	2.5ϕAD	0.0ϕAD	2.5ϕAD	4.0ϕAD

Figure 18.9 A/D Conversion Cycles

18.5 Internal Equivalent Circuit of Analog Input

Figure 18.10 shows the Internal Equivalent Circuit of Analog Input.



NOTE:
1. Use only as a standard for designing this data.
   Mass production may cause some changes in device characteristics.

Figure 18.10 Internal Equivalent Circuit of Analog Input

18.6 Output Impedance of Sensor under A/D Conversion

To carry out A/D conversion properly, charging the internal capacitor C shown in Figure 18.11 has to be completed within a specified period of time. T (sampling time) as the specified time. Let output impedance of sensor equivalent circuit be R0, internal resistance of microcomputer be R, precision (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in the 10-bit mode, and 256 in the 8-bit mode).

VC is generally $VC = VIN\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$

And when t = T, $VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

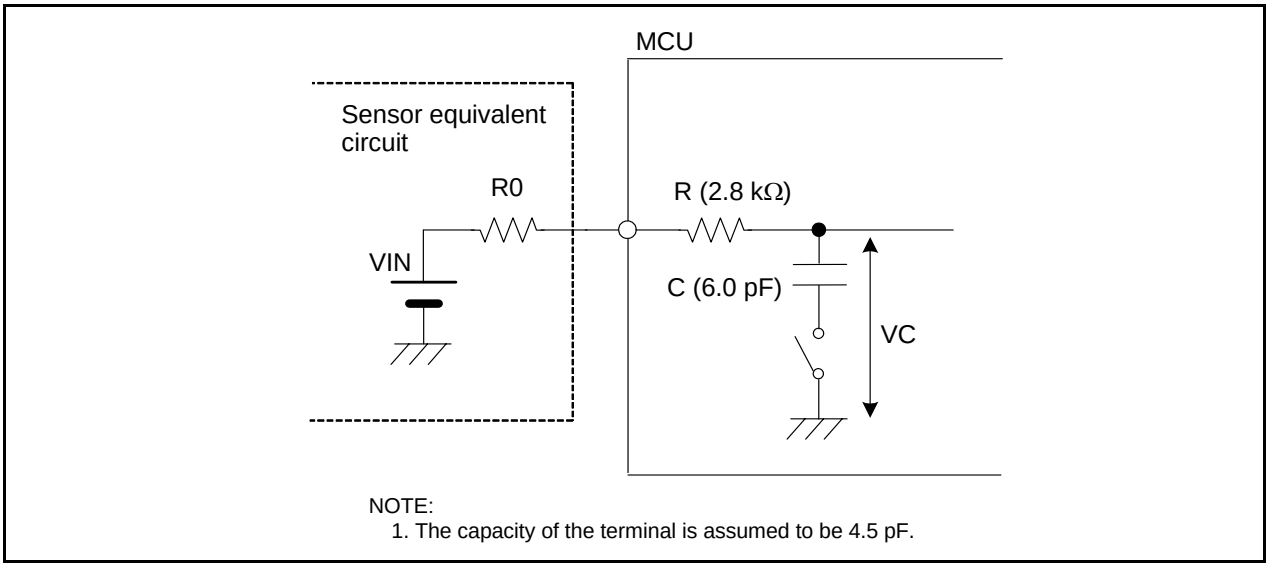
Hence, $R0 = -\frac{T}{C \bullet \ln\frac{X}{Y}} - R$

Figure 18.11 shows the Analog Input Pin and External Sensor Equivalent Circuit. When the difference between VIN and VC becomes 0.1LSB, we find impedance R0 when voltage between pins VC changes from 0 to VIN-(0.1/1024) VIN in time T. (0.1/1024) means that A/D precision drop due to insufficient capacitor charge is held to 0.1LSB at time of A/D conversion in the 10-bit mode. Actual error however is the value of absolute precision added to 0.1LSB.
When f(XIN) = 10 MHz, T = 0.25 µs in the A/D conversion mode without sample & hold. Output impedance R0 for sufficiently charging capacitor C within time T is determined as follows.

T = 0.25 µs, R = 2.8 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024. Hence,

$$R0 = -\frac{0.25 \times 10^{-6}}{6.0 \times 10^{-12} \bullet \ln\frac{0.1}{1024}} - 2.8 \times 10^{3} \approx 1.7 \times 10^{3}$$

Thus, the allowable output impedance of the sensor equivalent circuit, making the precision (error) 0.1LSB or less, is approximately 1.7 kΩ maximum.



NOTE:
1. The capacity of the terminal is assumed to be 4.5 pF.

Figure 18.11 Analog Input Pin and External Sensor Equivalent Circuit

18.7 Notes on A/D Converter

- Write to each bit (other than bit 6) in the ADCON0 register, each bit in the ADCON1 register, or the SMP bit in the ADCON2 register when A/D conversion is stopped (before a trigger occurs).
- When the VCUT bit in the ADCON1 register is changed from 0 (VREF not connected) to 1 (VREF connected), wait for at least 1 μs before starting the A/D conversion.
- After changing the A/D operating mode, select an analog input pin again.
- When using the one-shot mode, ensure that A/D conversion is completed before reading the AD register. The IR bit in the ADIC register or the ADST bit in the ADCON0 register can be used to determine whether A/D conversion is completed.
- When using the repeat mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select the fOCO-F for the ϕAD.
- If the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program and A/D conversion is forcibly terminated during an A/D conversion operation, the conversion result of the A/D converter will be undefined. If the ADST bit is set to 0 by a program, do not use the value of the AD register.
- Connect 0.1 μF capacitor between the P4_2/VREF pin and AVSS pin.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode when the CM02 bit in the CM0 register is set to 1 (peripheral function clock stops in wait mode) during A/D conversion.

19. Flash Memory

19.1 Overview

In the flash memory, rewrite operations to the flash memory can be performed in three modes: CPU rewrite, standard serial I/O, and parallel I/O.
Table 19.1 lists the Flash Memory Performance (refer to **Table 1.1 Functions and Specifications for R8C/24 Group** and **Table 1.2 Functions and Specifications for R8C/25 Group** for items not listed in **Table 19.1**).

Table 19.1 Flash Memory Performance

Item		Specification
Flash memory operating mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Division of erase block		Refer to **Figure 19.1** and **Figure 19.2**
Programming method		Byte unit
Erase method		Block erase
Programming and erasure control method(3)		Program and erase control by software command
Rewrite control method		Rewrite control for blocks 0 and 1 by FMR02 bit in FMR0 register
		Rewrite control for block 0 by FMR15 bit and Block 1 by FMR16 bit in FMR1 register
Number of commands		5 commands
Programming and erasure endurance(1)	Blocks 0 and 1 (program ROM)	R8C/24 Group: 100 times; R8C/25 Group: 1,000 times
	Blocks A and B (data flash)(2)	10,000 times
ID code check function		Standard serial I/O mode supported
ROM code protect		Parallel I/O mode supported

NOTES:
1. Definition of programming and erasure endurance
   The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1-Kbyte block, and then the block is erased, the erase count stands at one. When performing 100 or more rewrites, the actual erase count can be reduced by executing programming operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
2. Blocks A and B are implemented only in the R8C/25 group.
3. To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

Table 19.2 Flash Memory Rewrite Modes

Flash memory Rewrite mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	User ROM area is rewritten by executing software commands from the CPU. EW0 mode: Rewritable in the RAM EW1 mode: Rewritable in flash memory	User ROM area is rewritten by a dedicated serial programmer.	User ROM area is rewritten by a dedicated parallel programmer.
Areas which can be rewritten	User ROM area	User ROM area	User ROM area
Operating mode	Single chip mode	Boot mode	Parallel I/O mode
ROM Programmer	None	Serial programmer	Parallel programmer

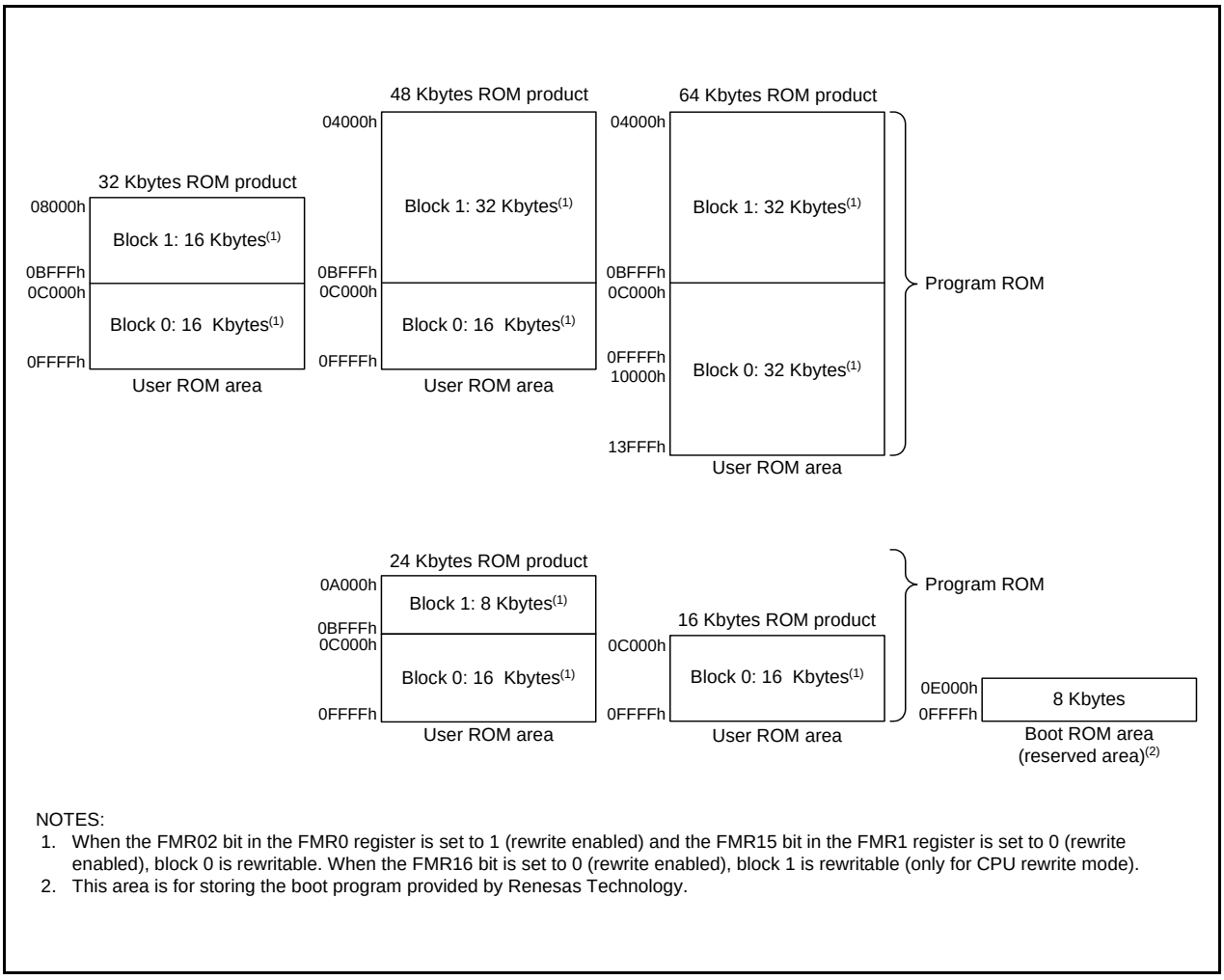
19.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area). Figure 19.1 shows the Flash Memory Block Diagram for R8C/24 Group. Figure 19.2 shows a Flash Memory Block Diagram for R8C/25 Group. The user ROM area of the R8C/25 Group contains an area (program ROM) which stores MCU operating programs and blocks A and B (data flash) each 1 Kbyte in size.

The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite mode and standard serial I/O and parallel I/O modes.

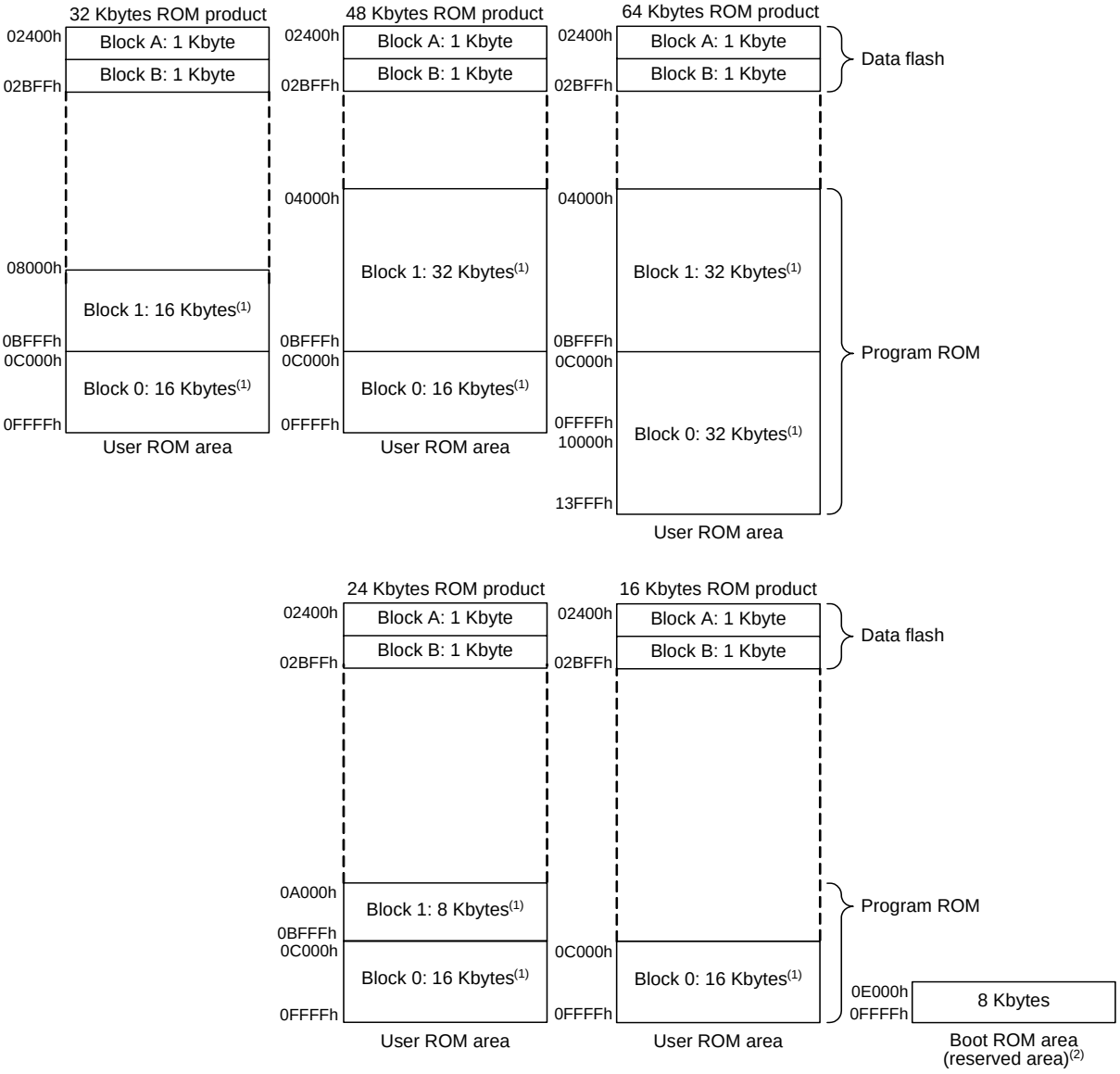
When rewriting blocks 0 and 1 in CPU rewrite mode, set the FMR02 bit in the FMR0 register to 1 (rewrite enabled). When the FMR15 bit in the FMR1 register is set to 0 (rewrite enabled), block 0 is rewritable. When the FMR16 bit is set to 0 (rewrite enabled), block 1 is rewritable.

The rewrite control program for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area and the user ROM area share the same address, but have separate memory areas.



NOTES:
1. When the FMR02 bit in the FMR0 register is set to 1 (rewrite enabled) and the FMR15 bit in the FMR1 register is set to 0 (rewrite enabled), block 0 is rewritable. When the FMR16 bit is set to 0 (rewrite enabled), block 1 is rewritable (only for CPU rewrite mode).
2. This area is for storing the boot program provided by Renesas Technology.

Figure 19.1 Flash Memory Block Diagram for R8C/24 Group



NOTES:
1. When the FMR02 bit in the FMR0 register is set to 1 (rewrite enabled) and the FMR15 bit in the FMR1 register is set to 0 (rewrite enabled), block 0 is rewritable. When the FMR16 bit is set to 0 (rewrite enabled), block 1 is rewritable (only for CPU rewrite mode).
2. This area is for storing the boot program provided by Renesas Technology.

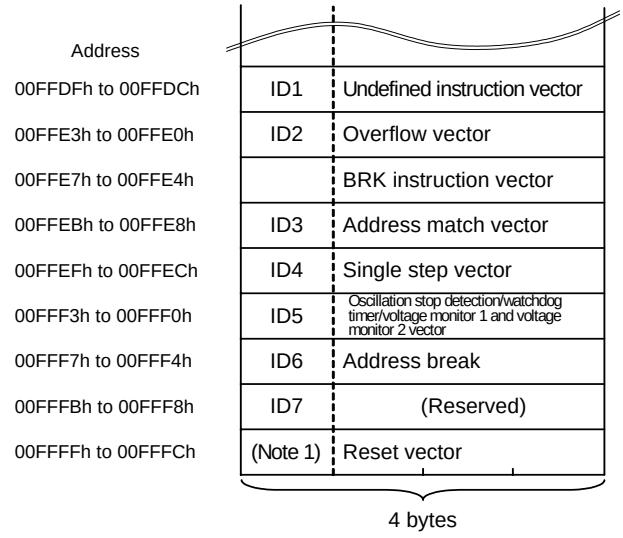
Figure 19.2 Flash Memory Block Diagram for R8C/25 Group

19.3 Functions to Prevent Rewriting of Flash Memory

Standard serial I/O mode has an ID code check function, and parallel I/O mode has a ROM code protect function to prevent the flash memory from being read or rewritten easily.

19.3.1 ID Code Check Function

This function is used in standard serial I/O mode. Unless the flash memory is blank, the ID codes sent from the programmer and the ID codes written in the flash memory are checked to see if they match. If the ID codes do not match, the commands sent from the programmer are not acknowledged. The ID codes consist of 8 bits of data each, the areas of which, beginning with the first byte, are 00FFDFh, 00FFE3h, 00FFEBh, 00FFEFh, 00FFF3h, 00FFF7h, and 00FFFBh. Write programs in which the ID codes are set at these addresses and write them to the flash memory.



NOTE:
1. The OFS register is assigned to 00FFFFh.
Refer to **Figure 19.4 OFS Register** for OFS register details.

Figure 19.3 Address for Stored ID Code

19.3.2 ROM Code Protect Function

The ROM code protect function disables reading or changing the contents of the on-chip flash memory by the OFS register in parallel I/O mode. Figure 19.4 shows the OFS Register.
The ROM code protect function is enabled by writing 0 to the ROMCP1 bit and 1 to the ROMCR bit. It disables reading or changing the contents of the on-chip flash memory.
Once ROM code protect is enabled, the content in the internal flash memory cannot be rewritten in parallel I/O mode. To disable ROM code protect, erase the block including the OFS register with CPU rewrite mode or standard serial I/O mode.

Option Function Select Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
	1		1			1	

Symbol	Address	When Shipping
OFS	0FFFFh	FFh(3)

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Starts watchdog timer automatically after reset 1 : Watchdog timer is inactive after reset	RW
— (b1)	Reserved bit	Set to 1.	RW
ROMCR	ROM code protect disabled bit	0 : ROM code protect disabled 1 : ROMCP1 enabled	RW
ROMCP1	ROM code protect bit	0 : ROM code protect enabled 1 : ROM code protect disabled	RW
— (b4)	Reserved bit	Set to 1.	RW
LVD0ON	Voltage detection 0 circuit start bit(2)	0 : Voltage monitor 0 reset enabled after hardware reset 1 : Voltage monitor 0 reset disabled after hardware reset	RW
— (b6)	Reserved bit	Set to 1.	RW
CSPROINI	Count source protect mode after reset select bit	0 : Count source protect mode enabled after reset 1 : Count source protect mode disabled after reset	RW

NOTES:
1. The OFS register is on the flash memory. Write to the OFS register with a program. After writing is completed, do not write additions to the OFS register.
2. To use the power-on reset, set the LVD0ON bit to 0 (voltage monitor 0 reset enabled after reset).
3. If the block including the OFS register is erased, FFh is set to the OFS register.

Figure 19.4 OFS Register

19.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. Execute the program and block erase commands only to blocks in the user ROM area.
The flash module has an erase-suspend function when an interrupt request is generated during an erase operation in CPU rewrite mode. It performs an interrupt process after the erase operation is halted temporarily. During erase-suspend, the user ROM area can be read by a program.
In case an interrupt request is generated during an auto-program operation in CPU rewrite mode, the flash module has a program-suspend function which performs the interrupt process after the auto-program operation is suspended. During program-suspend, the user ROM area can be read by a program.
CPU rewrite mode has an erase write 0 mode (EW0 mode) and an erase write 1 mode (EW1 mode). Table 19.3 lists the Differences between EW0 Mode and EW1 Mode.

Table 19.3 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	Single-chip mode	Single-chip mode
Areas in which a rewrite control program can be located	User ROM area	User ROM area
Areas in which a rewrite control program can be executed	Necessary to transfer to any area other than the flash memory (e.g., RAM) before executing	Executing directly in user ROM or RAM area possible
Areas which can be rewritten	User ROM area	User ROM area However, blocks which contain a rewrite control program are excluded(1)
Software command restrictions	None	• Program and block erase commands Cannot be run on any block which contains a rewrite control program • Read status register command Cannot be executed
Modes after program or erase	Read status register mode	Read array mode
Modes after read status register	Read status register mode	Do not execute this command
CPU status during auto-write and auto-erase	Operating	Hold state (I/O ports hold state before the command is executed)
Flash memory status detection	• Read bits FMR00, FMR06, and FMR07 in the FMR0 register by a program • Execute the read status register command and read bits SR7, SR5, and SR4 in the status register.	Read bits FMR00, FMR06, and FMR07 in the FMR0 register by a program
Conditions for transition to erase-suspend	Set bits FMR40 and FMR41 in the FMR4 register to 1 by a program.	The FMR40 bit in the FMR4 register is set to 1 and the interrupt request of the enabled maskable interrupt is generated
Conditions for transitions to program-suspend	Set bits FMR40 and FMR42 in the FMR4 register to 1 by a program.	The FMR40 bit in the FMR4 register is set to 1 and the interrupt request of the enabled maskable interrupt is generated
CPU clock	5 MHz or below	No restriction (on clock frequency to be used)

NOTE:
1. When the FMR02 bit in the FMR0 register is set to 1 (rewrite enabled), rewriting block 0 is enabled by setting the FMR15 bit in the FMR1 register to 0 (rewrite enabled), and rewriting block 1 is enabled by setting the FMR16 bit to 0 (rewrite enabled).

19.4.1 EW0 Mode

The MCU enters CPU rewrite mode and software commands can be acknowledged by setting the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled). In this case, since the FMR11 bit in the FMR1 register is set to 0, EW0 mode is selected.

Use software commands to control program and erase operations. The FMR0 register or the status register can be used to determine when program and erase operations complete.

During auto-erasure, set the FMR40 bit to 1 (erase-suspend enabled) and the FMR41 bit to 1 (request erase-suspend). Wait for td(SR-SUS) and ensure that the FMR46 bit is set to 1 (read enabled) before accessing the user ROM area. The auto-erase operation can be restarted by setting the FMR41 bit to 0 (erase restarts).

To enter program-suspend during the auto-program operation, set the FMR40 bit to 1 (suspend enabled) and the FMR42 bit to 1 (request program-suspend). Wait for td(SR-SUS) and ensure that the FMR46 bit is set to 1 (read enabled) before accessing the user ROM area. The auto-program operation can be restarted by setting the FMR42 bit to 0 (program restarts).

19.4.2 EW1 Mode

The MCU is switched to EW1 mode by setting the FMR11 bit to 1 (EW1 mode) after setting the FMR01 bit to 1 (CPU rewrite mode enabled).

The FMR0 register can be used to determine when program and erase operations complete. Do not execute commands that use the read status register in EW1 mode.

To enable the erase-suspend function during auto-erasure, execute the block erase command after setting the FMR40 bit to 1 (erase-suspend enabled). The interrupt to enter erase-suspend should be in interrupt enabled status. After waiting for td(SR-SUS) after the block erase command is executed, the interrupt request is acknowledged.

When an interrupt request is generated, the FMR41 bit is automatically set to 1 (requests erase-suspend) and the auto-erase operation suspends. If an auto-erase operation does not complete (FMR00 bit is 0) after an interrupt process completes, the auto-erase operation restarts by setting the FMR41 bit to 0 (erasure restarts)

To enable the program-suspend function during auto-programming, execute the program command after setting the FMR40 bit to 1 (suspend enabled). The interrupt to enter program-suspend should be in interrupt enabled status. After waiting for td(SR-SUS) after the program command is executed, an interrupt request is acknowledged.

When an interrupt request is generated, the FMR42 bit is automatically set to 1 (request program-suspend) and the auto-program operation suspends. When the auto-program operation does not complete (FMR00 bit is 0) after the interrupt process completes, the auto-program operation can be restarted by setting the FMR42 bit to 0 (programming restarts).

Figure 19.5 shows the FMR0 Register. Figure 19.6 shows the FMR1 Register. Figure 19.7 shows the FMR4 Register.

19.4.2.1 FMR00 Bit

This bit indicates the operating status of the flash memory. The bits value is 0 during programming, erasure (including suspend periods), or erase-suspend mode; otherwise, it is 1.

19.4.2.2 FMR01 Bit

The MCU is made ready to accept commands by setting the FMR01 bit to 1 (CPU rewrite mode).

19.4.2.3 FMR02 Bit

Rewriting of blocks 0 and 1 does not accept program or block erase commands if the FMR02 bit is set to 0 (rewrite disabled).
Rewriting of blocks 0 and 1 is controlled by bits FMR15 and FMR16 if the FMR02 bit is set to 1 (rewrite enabled).

19.4.2.4 FMSTP Bit

This bit is used to initialize the flash memory control circuits, and also to reduce the amount of current consumed by the flash memory. Access to the flash memory is disabled by setting the FMSTP bit to 1. Therefore, the FMSTP bit must be written to by a program transferred to the RAM.
In the following cases, set the FMSTP bit to 1:

- When flash memory access resulted in an error while erasing or programming in EW0 mode (FMR00 bit not reset to 1 (ready))
- To provide lower consumption in high-speed on-chip oscillator mode, low-speed on-chip oscillator mode (XIN clock stops), and low-speed clock mode (XIN clock stops).

Figure 19.11 shows the handling to provide lower consumption in high-speed on-chip oscillator mode, low-speed on-chip oscillator mode (XIN clock stops), and low-speed clock mode (XIN clock stops). Handle according to this flowchart. Note that when going to stop or wait mode while the CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on again after returning from stop or wait mode.

19.4.2.5 FMR06 Bit

This is a read-only bit indicating the status of an auto-program operation. The bit is set to 1 when a program error occurs; otherwise, it is set to 0. For details, refer to the description in **19.4.5 Full Status Check**.

19.4.2.6 FMR07 Bit

This is a read-only bit indicating the status of an auto-erase operation. The bit is set to 1 when an erase error occurs; otherwise, it is set to 0. Refer to **19.4.5 Full Status Check** for details.

19.4.2.7 FMR11 Bit

Setting this bit to 1 (EW1 mode) places the MCU in EW1 mode.

19.4.2.8 FMR15 Bit

When the FMR02 bit is set to 1 (rewrite enabled) and the FMR15 bit is set to 0 (rewrite enabled), block 0 accepts program and block erase commands.

19.4.2.9 FMR16 Bit

When the FMR02 bit is set to 1 (rewrite enabled) and the FMR16 bit is set to 0 (rewrite enabled), block 1 accepts program and block erase commands.

19.4.2.10 FMR40 Bit

The suspend function is enabled by setting the FMR40 bit to 1 (enable).

19.4.2.11 FMR41 Bit

In EW0 mode, the MCU enters erase-suspend mode when the FMR41 bit is set to 1 by a program. The FMR41 bit is automatically set to 1 (request erase-suspend) when an interrupt request of an enabled interrupt is generated in EW1 mode, and then the MCU enters erase-suspend mode.
Set the FMR41 bit to 0 (erase restarts) when the auto-erase operation restarts.

19.4.2.12 FMR42 Bit

In EW0 mode, the MCU enters program-suspend mode when the FMR42 bit is set to 1 by a program. The FMR42 bit is automatically set to 1 (request program-suspend) when an interrupt request of an enabled interrupt is generated in EW1 mode, and then the MCU enters program-suspend mode.
Set the FMR42 bit to 0 (program restart) when the auto-program operation restarts.

19.4.2.13 FMR43 Bit

When the auto-erase operation starts, the FMR43 bit is set to 1 (erase execution in progress). The FMR43 bit remains set to 1 (erase execution in progress) during erase-suspend operation.
When the auto-erase operation ends, the FMR43 bit is set to 0 (erase not executed).

19.4.2.14 FMR44 Bit

When the auto-program operation starts, the FMR44 bit is set to 1 (program execution in progress). The FMR44 bit remains set to 1 (program execution in progress) during program-suspend operation.
When the auto-program operation ends, the FMR44 bit is set to 0 (program not executed).

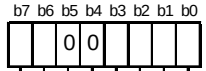
19.4.2.15 FMR46 Bit

The FMR46 bit is set to 0 (reading disabled) during auto-program or auto-erase execution and set to 1 (reading enabled) in suspend mode. Do not access the flash memory while this bit is set to 0.

19.4.2.16 FMR47 Bit

Power consumption when reading the flash memory can be reduced by setting the FMR47 bit to 1 (enabled) in low-speed clock mode (XIN clock stops) and low-speed on-chip oscillator mode (XIN clock stops).

Flash Memory Control Register 0



Symbol: FMR0 | Address: 01B7h | After Reset: 00000001b

Bit Symbol	Bit Name	Function	RW
FMR00	RY/$\overline{BY}$ status flag	0 : Busy (writing or erasing in progress) 1 : Ready	RO
FMR01	CPU rewrite mode select bit(1)	0 : CPU rewrite mode disabled 1 : CPU rewrite mode enabled	RW
FMR02	Block 0, 1 rewrite enable bit(2, 6)	0 : Disables rewrite 1 : Enables rewrite	RW
FMSTP	Flash memory stop bit(3, 5)	0 : Enables flash memory operation 1 : Stops flash memory (enters low-power consumption state and flash memory is reset)	RW
— (b5-b4)	Reserved bits	Set to 0.	RW
FMR06	Program status flag(4)	0 : Completed successfully 1 : Terminated by error	RO
FMR07	Erase status flag(4)	0 : Completed successfully 1 : Terminated by error	RO

NOTES:
1. To set this bit to 1, set it to 1 immediately after setting it first to 0. Do not generate an interrupt between setting the bit to 0 and setting it to 1. Enter read array mode and set this bit to 0.
2. Set this bit to 1 immediately after setting it first to 0 while the FMR01 bit is set to 1. Do not generate an interrupt between setting the bit to 0 and setting it to 1.
3. Set this bit by a program transferred to the RAM.
4. This bit is set to 0 by executing the clear status command.
5. This bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled). When the FMR01 bit is set to 0, writing 1 to the FMSTP bit causes the FMSTP bit to be set to 1. The flash memory does not enter low-power consumption state nor is it reset.
6. When setting the FMR01 bit to 0 (CPU rewrite mode disabled), the FMR02 bit is set to 0 (disables rewrite).

Figure 19.5 FMR0 Register

Flash Memory Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
1			0	0	0		

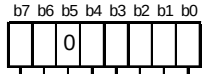
Symbol	Address	After Reset
FMR1	01B5h	1000000Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	When read, the content is undefined.	RO
FMR11	EW1 mode select bit(1, 2)	0 : EW0 mode 1 : EW1 mode	RW
— (b4-b2)	Reserved bits	Set to 0.	RW
FMR15	Block 0 rewrite disable bit(2,3)	0 : Enables rewrite 1 : Disables rewrite	RW
FMR16	Block 1 rewrite disable bit(2,3)	0 : Enables rewrite 1 : Disables rewrite	RW
— (b7)	Reserved bit	Set to 1.	RW

NOTES:
1. To set this bit to 1, set it to 1 immediately after setting it first to 0 while the FMR01 bit is set to 1 (CPU rewrite mode enable). Do not generate an interrupt between setting the bit to 0 and setting it to 1.
2. This bit is set to 0 by setting the FMR01 bit to 0 (CPU rewrite mode disabled).
3. When the FMR01 bit is set to 1 (CPU rewrite mode enabled), bits FMR15 and FMR16 can be written to.
   To set this bit to 0, set it to 0 immediately after setting it first to 1.
   To set this bit to 1, set it to 1.

Figure 19.6 FMR1 Register

Flash Memory Control Register 4



Symbol	Address	After Reset
FMR4	01B3h	01000000b

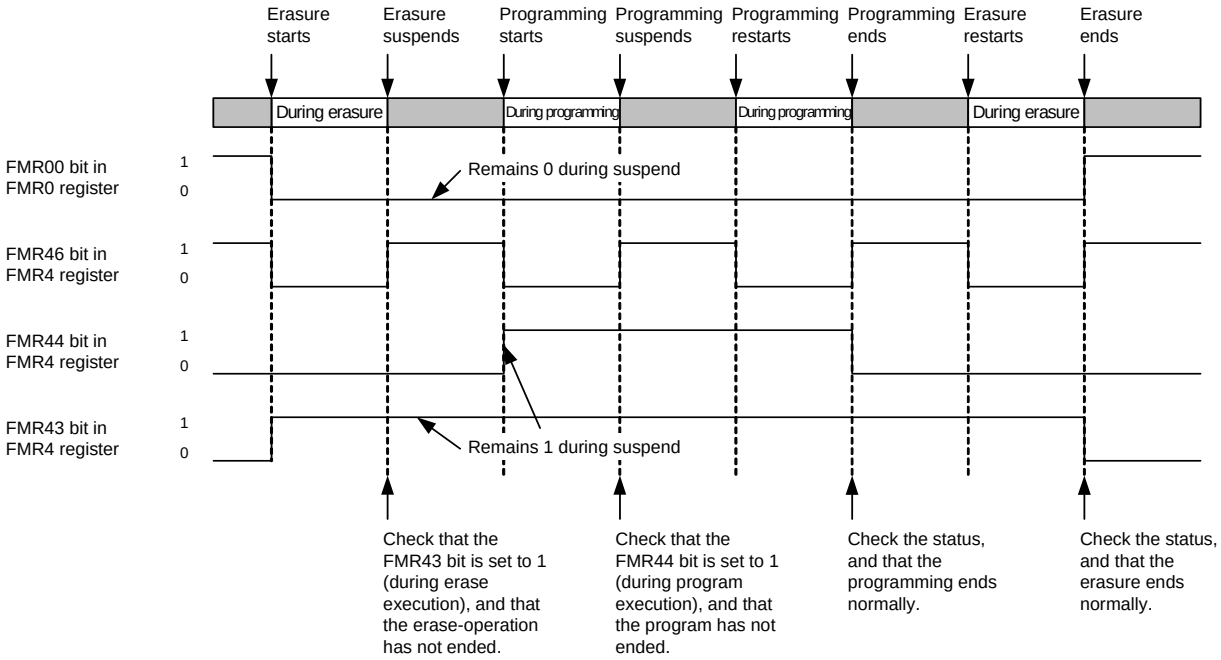
Bit Symbol	Bit Name	Function	RW
FMR40	Erase-suspend function enable bit(1)	0 : Disable 1 : Enable	RW
FMR41	Erase-suspend request bit(2)	0 : Erase restart 1 : Erase-suspend request	RW
FMR42	Program-suspend request bit(3)	0 : Program restart 1 : Program-suspend request	RW
FMR43	Erase command flag	0 : Erase not executed 1 : Erase execution in progress	RO
FMR44	Program command flag	0 : Program not executed 1 : Program execution in progress	RO
— (b5)	Reserved bit	Set to 0.	RO
FMR46	Read status flag	0 : Disables reading 1 : Enables reading	RO
FMR47	Low-power consumption read mode enable bit (1, 4, 5)	0 : Disable 1 : Enable	RW

NOTES:

1. To set this bit to 1, set it to 1 immediately after setting it first to 0. Do not generate an interrupt between setting the bit to 0 and setting it to 1.
2. This bit is enabled when the FMR40 bit is set to 1 (enable) and it can be written to during the period between issuing an erase command and completing the erase. (This bit is set to 0 during periods other than above.)
   In EW0 mode, it can be set to 0 or 1 by a program.
   In EW1 mode, it is automatically set to 1 if a maskable interrupt is generated during an erase operation while the FMR40 bit is set to 1. Do not set this bit to 1 by a program (0 can be written).
3. The FMR42 bit is enabled only when the FMR40 bit is set to 1 (enable) and programming to the FMR42 bit is enabled until auto-programming ends after a program command is generated. (This bit is set to 0 during periods other than the above.)
   In EW0 mode, 0 or 1 can be programmed to the FMR42 bit by a program.
   In EW1 mode, the FMR42 bit is automatically set to 1 by generating a maskable interrupt during auto-programming when the FMR40 bit is set to 1. 1 cannot be written to the FMR42 bit by a program.
4. In high-speed clock mode and high-speed on-chip oscillator mode, set the FMR47 bit to 0 (disabled).
5. Set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) in low-power consumption read mode.

Figure 19.7 FMR4 Register

Figure 19.8 shows the Timing of Suspend Operation.



The above figure shows an example of the use of program-suspend during programming following erase-suspend.

NOTE:
1. If program-suspend is entered during erase-suspend, always restart programming.

Figure 19.8 Timing of Suspend Operation

Figure 19.9 shows the How to Set and Exit EW0 Mode. Figure 19.10 shows the How to Set and Exit EW1 Mode.

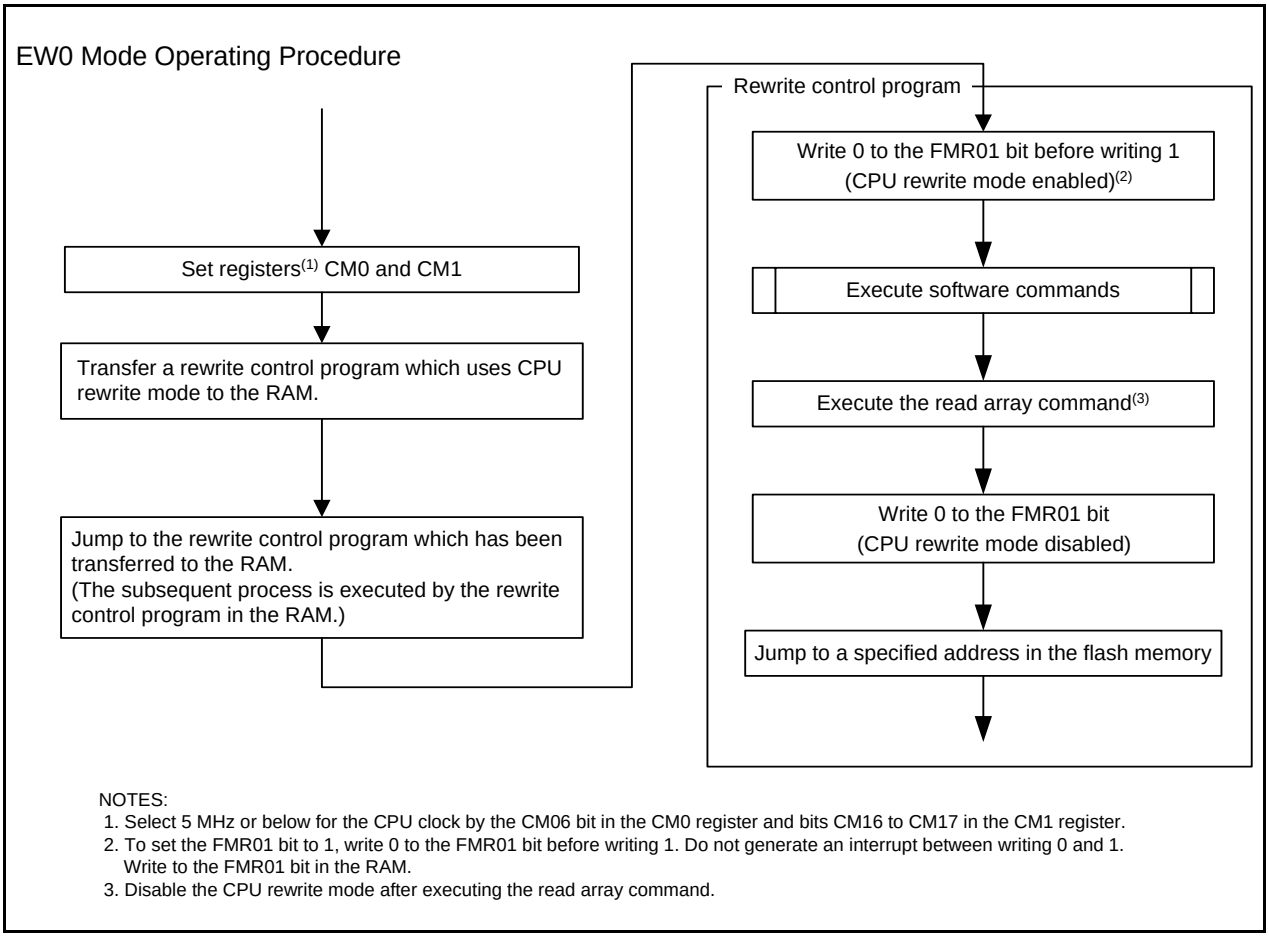


Figure 19.9 How to Set and Exit EW0 Mode

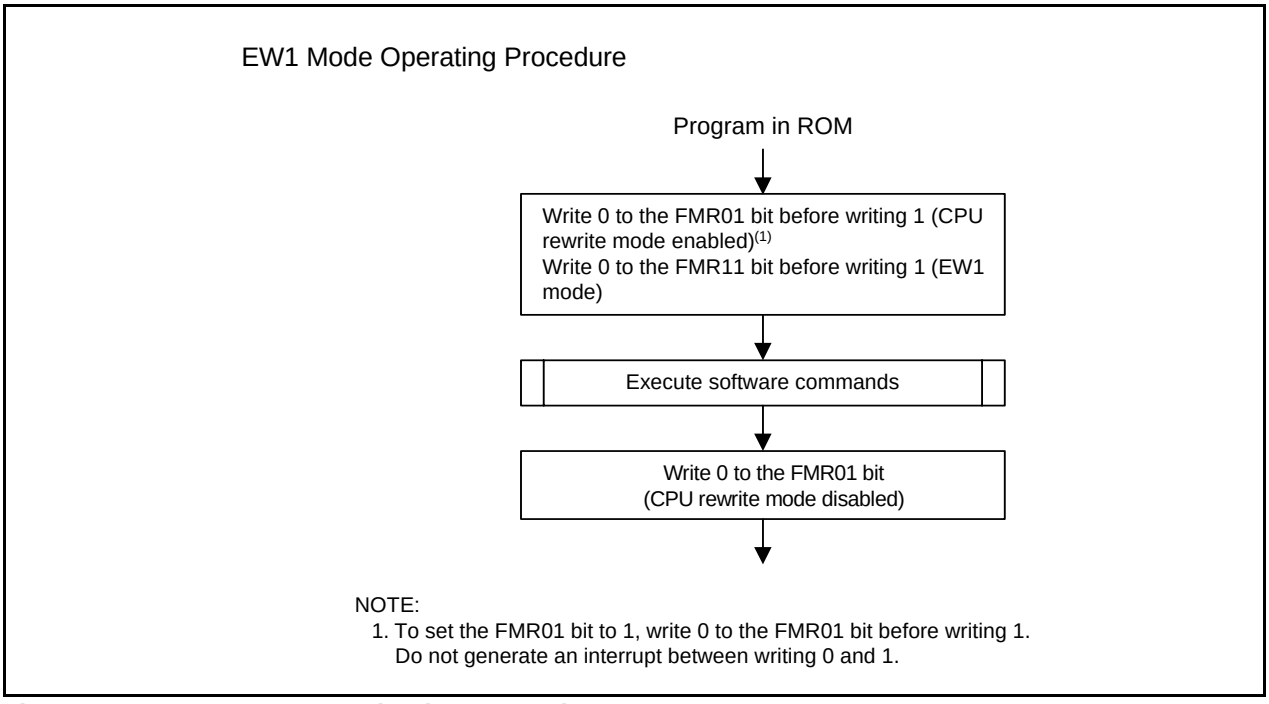


Figure 19.10 How to Set and Exit EW1 Mode

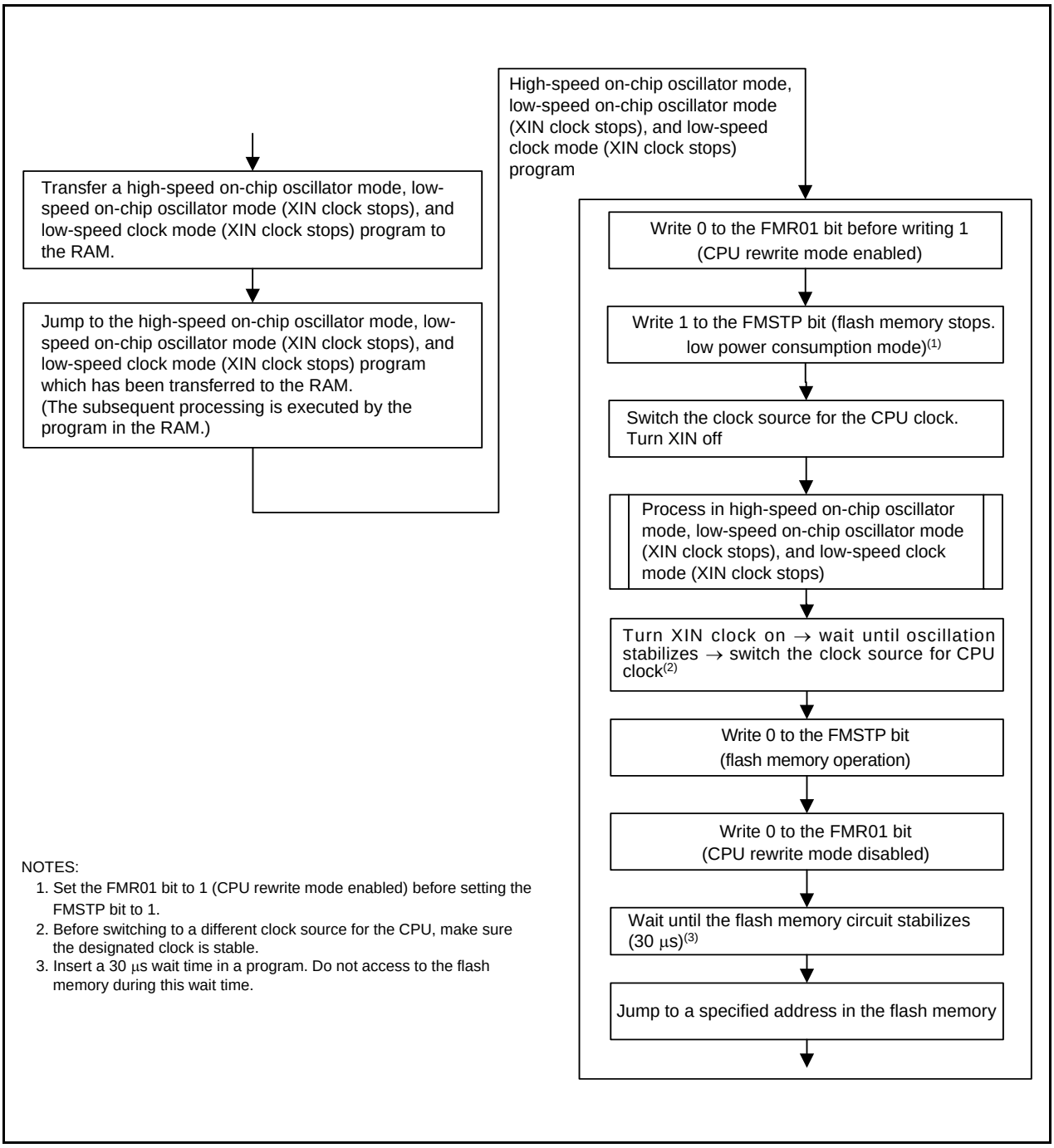


Figure 19.11 Process to Reduce Power Consumption in High-Speed On-Chip Oscillator Mode, Low-Speed On-Chip Oscillator Mode (XIN Clock Stops) and Low-Speed Clock Mode (XIN Clock Stops)

19.4.3 Software Commands

The software commands are described below. Read or write commands and data in 8-bit units.

Table 19.4 Software Commands

Command	First Bus Cycle			Second Bus Cycle		
	Mode	Address	Data (D7 to D0)	Mode	Address	Data (D7 to D0)
Read array	Write	×	FFh			
Read status register	Write	×	70h	Read	×	SRD
Clear status register	Write	×	50h			
Program	Write	WA	40h	Write	WA	WD
Block erase	Write	×	20h	Write	BA	D0h

SRD: Status register data (D7 to D0)
WA: Write address (ensure the address specified in the first bus cycle is the same address as the write address specified in the second bus cycle.)
WD: Write data (8 bits)
BA: Given block address
×: Any specified address in the user ROM area

19.4.3.1 Read Array Command

The read array command reads the flash memory.
The MCU enters read array mode when FFh is written in the first bus cycle. When the read address is entered in the following bus cycles, the content of the specified address can be read in 8-bit units.
Since the MCU remains in read array mode until another command is written, the contents of multiple addresses can be read continuously.
In addition, the MCU enters read array mode after a reset.

19.4.3.2 Read Status Register Command

The read status register command is used to read the status register.
When 70h is written in the first bus cycle, the status register can be read in the second bus cycle (refer to **19.4.4 Status Registers**). When reading the status register, specify an address in the user ROM area.
Do not execute this command in EW1 mode.
The MCU remains in read status register mode until the next read array command is written.

19.4.3.3 Clear Status Register Command

The clear status register command sets the status register to 0.
When 50h is written in the first bus cycle, bits FMR06 to FMR07 in the FMR0 register and SR4 to SR5 in the status register are set to 0.

19.4.3.4 Program Command

The program command writes data to the flash memory in 1-byte units.
By writing 40h in the first bus cycle and data in the second bus cycle to the write address, an auto-program operation (data program and verify) will start. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle.
The FMR00 bit in the FMR0 register can be used to determine whether auto-programming has completed. When suspend function disabled, the FMR00 bit is set to 0 during auto-programming and set to 1 when auto-programming completes. When suspend function enabled, the FMR44 bit is set to 1 during auto-programming and set to 0 when auto-programming completes.
The FMR06 bit in the FMR0 register can be used to determine the result of auto-programming after it has been finished (refer to **19.4.5 Full Status Check**).
Do not write additions to the already programmed addresses.
When the FMR02 bit in the FMR0 register is set to 0 (rewriting disabled), or the FMR02 bit is set to 1 (rewrite enabled) and the FMR15 bit in the FMR1 register is set to 1 (rewriting disabled), program commands targeting block 0 are not acknowledged. When the FMR16 bit is set to 1 (rewriting disabled), program commands targeting block 1 are not acknowledged.
Figure 19.12 shows the Program Command (When Suspend Function Disabled). Figure 19.13 shows the Program Command (When Suspend Function Enabled).
In EW1 mode, do not execute this command for any address which a rewrite control program is allocated.
In EW0 mode, the MCU enters read status register mode at the same time auto-programming starts and the status register can be read. The status register bit 7 (SR7) is set to 0 at the same time auto-programming starts and set back to 1 when auto-programming completes. In this case, the MCU remains in read status register mode until the next read array command is written. The status register can be read to determine the result of auto-programming after auto-programming has completed.

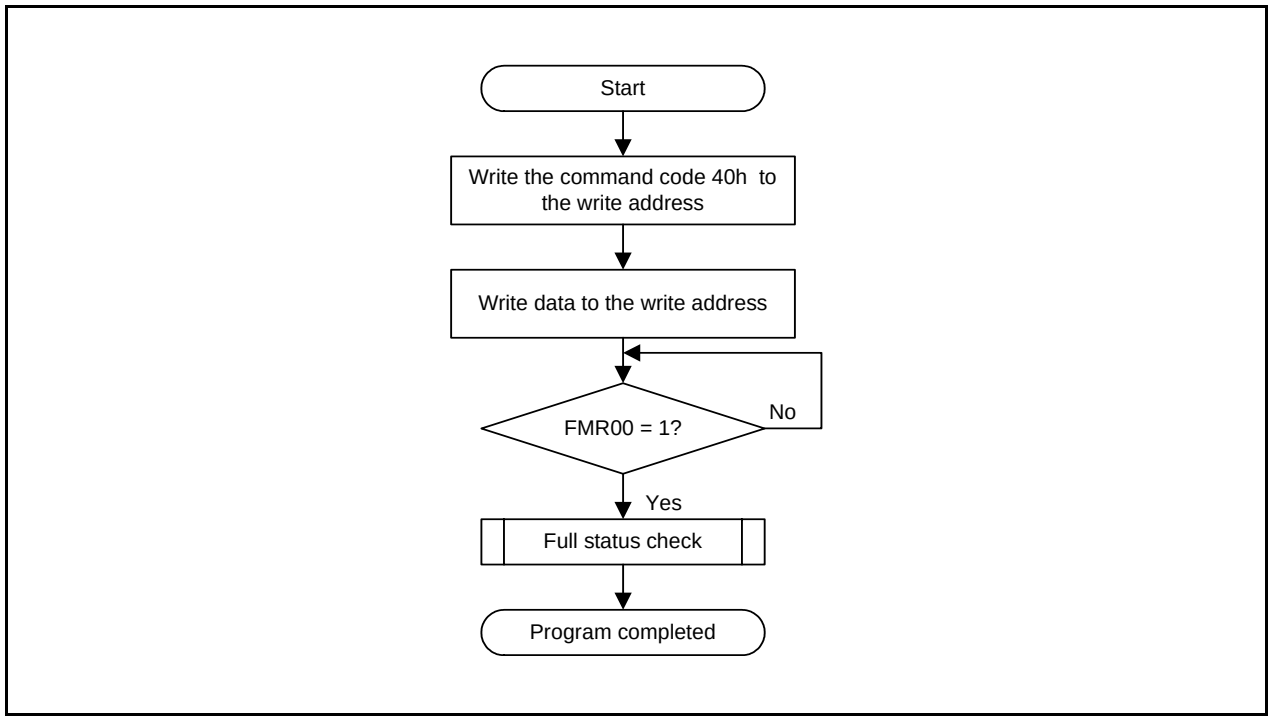
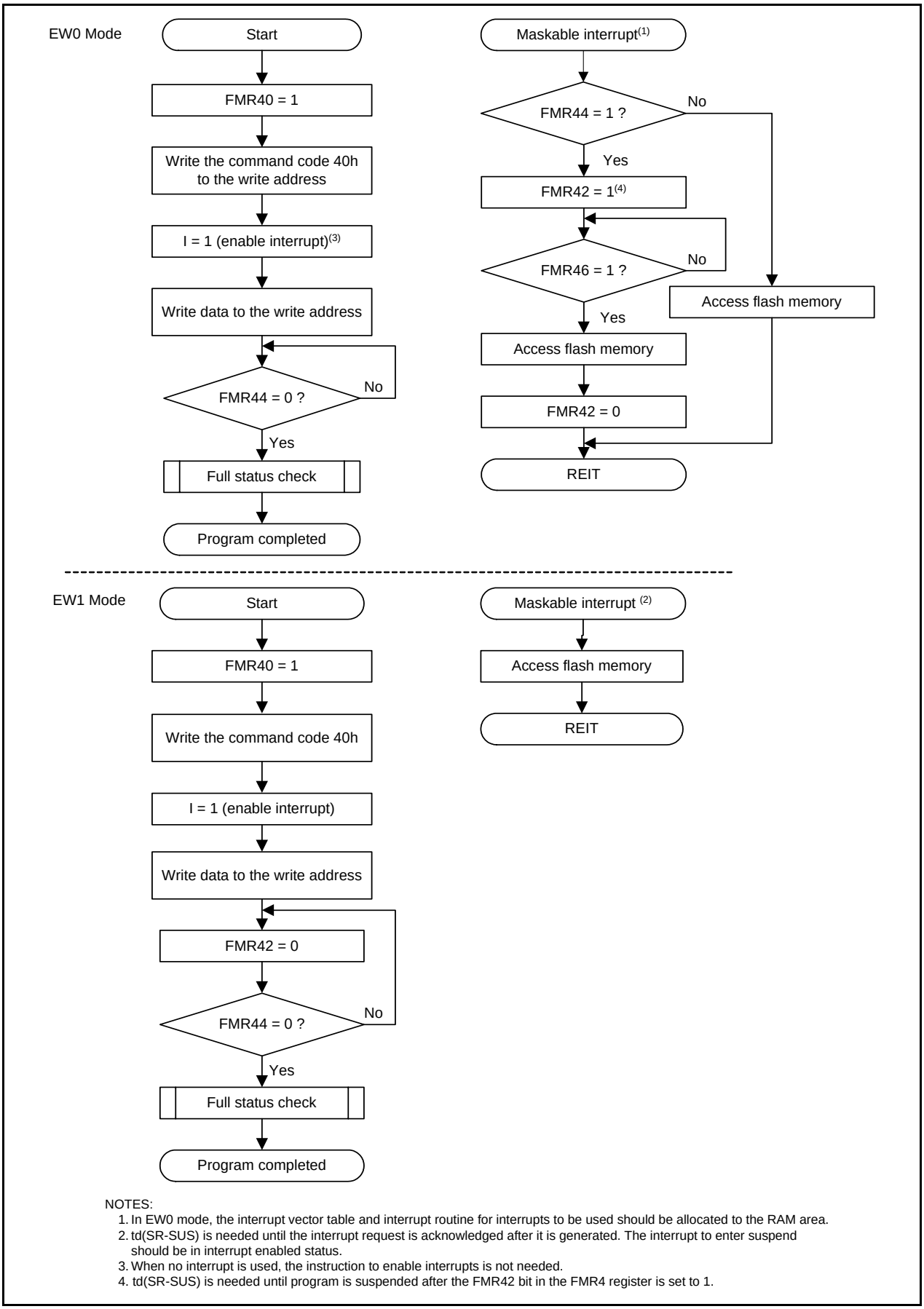


Figure 19.12 Program Command (When Suspend Function Disabled)



NOTES:
1. In EW0 mode, the interrupt vector table and interrupt routine for interrupts to be used should be allocated to the RAM area.
2. td(SR-SUS) is needed until the interrupt request is acknowledged after it is generated. The interrupt to enter suspend should be in interrupt enabled status.
3. When no interrupt is used, the instruction to enable interrupts is not needed.
4. td(SR-SUS) is needed until program is suspended after the FMR42 bit in the FMR4 register is set to 1.

Figure 19.13 Program Command (When Suspend Function Enabled)

19.4.3.5 Block Erase

When 20h is written in the first bus cycle and D0h is written to a given address of a block in the second bus cycle, an auto-erase operation (erase and verify) of the specified block starts.
The FMR00 bit in the FMR0 register can be used to determine whether auto-erasure has completed.
The FMR00 bit is set to 0 during auto-erasure and set to 1 when auto-erasure completes.
The FMR07 bit in the FMR0 register can be used to determine the result of auto-erasure after auto-erasure has completed (refer to **19.4.5 Full Status Check**).
When the FMR02 bit in the FMR0 register is set to 0 (rewriting disabled) or the FMR02 bit is set to 1 (rewriting enabled) and the FMR15 bit in the FMR1 register is set to 1 (rewriting disabled), the block erase commands targeting block 0 are not acknowledged. When the FMR16 bit is set to 1 (rewriting disabled), block erase commands targeting block 1 are not acknowledged.
Do not use the block erase command during program-suspend.
Figure 19.14 shows the Block Erase Command (When Erase-Suspend Function Disabled). Figure 19.15 shows the Block Erase Command (When Erase-Suspend Function Enabled).
In EW1 mode, do not execute this command for any address to which a rewrite control program is allocated.
In EW0 mode, the MCU enters read status register mode at the same time auto-erasure starts and the status register can be read. The status register bit 7 (SR7) is set to 0 at the same time auto-erasure starts and set back to 1 when auto-erasure completes. In this case, the MCU remains in read status register mode until the next read array command is written.

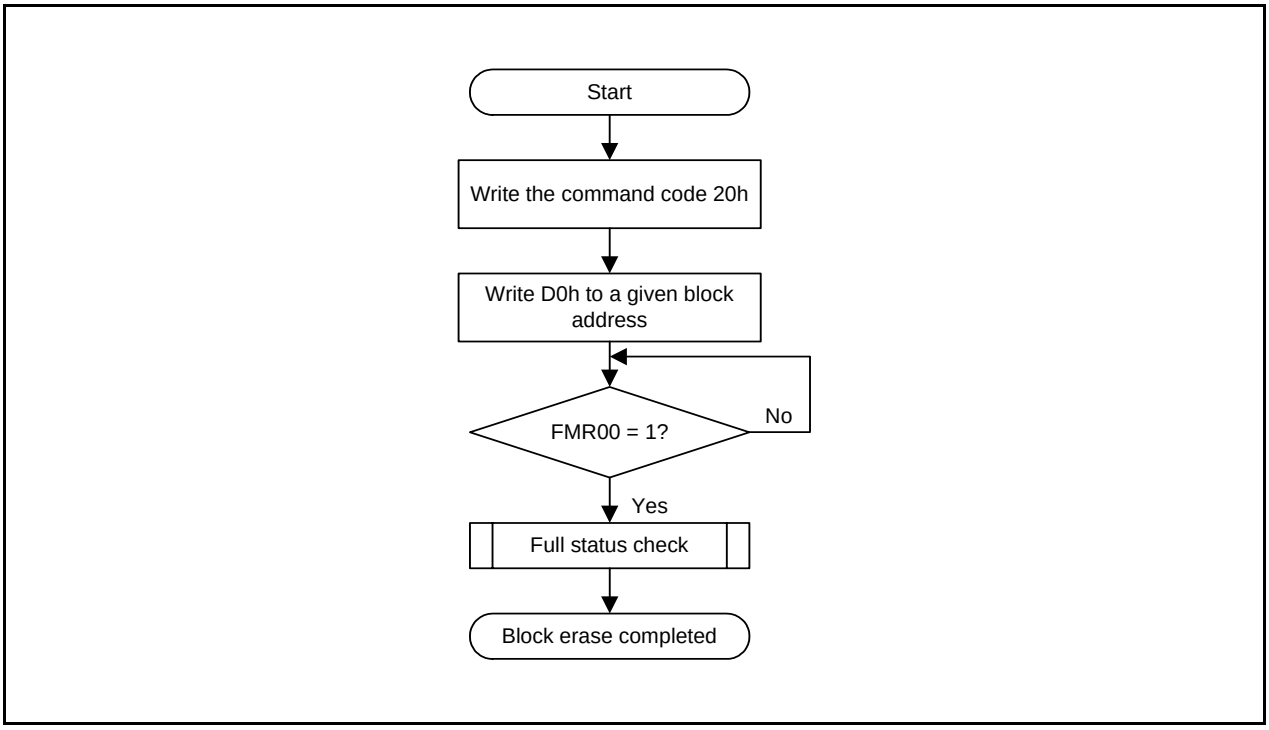
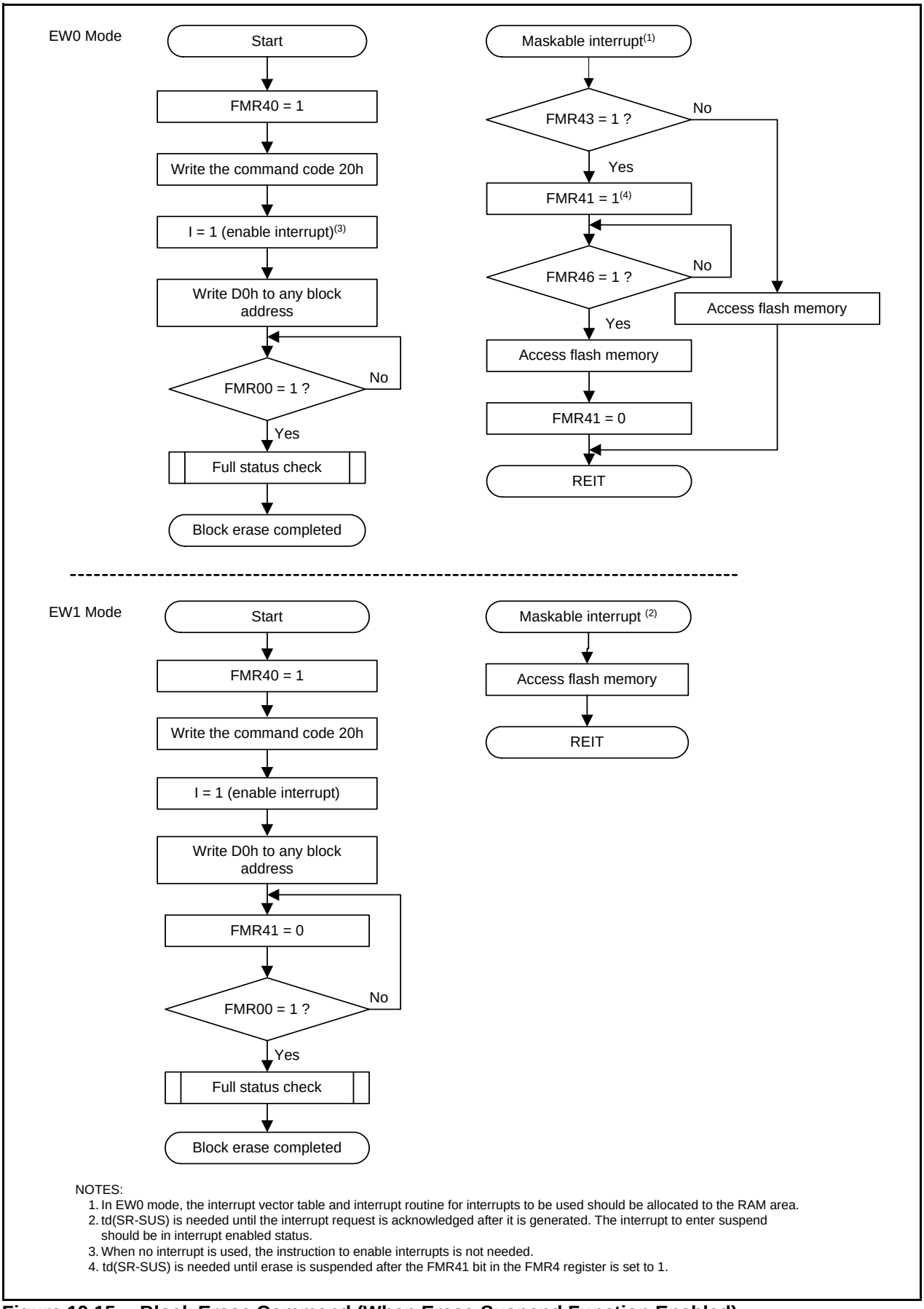


Figure 19.14 Block Erase Command (When Erase-Suspend Function Disabled)



NOTES:
1. In EW0 mode, the interrupt vector table and interrupt routine for interrupts to be used should be allocated to the RAM area.
2. td(SR-SUS) is needed until the interrupt request is acknowledged after it is generated. The interrupt to enter suspend should be in interrupt enabled status.
3. When no interrupt is used, the instruction to enable interrupts is not needed.
4. td(SR-SUS) is needed until erase is suspended after the FMR41 bit in the FMR4 register is set to 1.

Figure 19.15 Block Erase Command (When Erase-Suspend Function Enabled)

19.4.4 Status Registers

The status register indicates the operating status of the flash memory and whether an erase or program operation has completed normally or in error. Status of the status register can be read by bits FMR00, FMR06, and FMR07 in the FMR0 register.
Table 19.5 lists the Status Register Bits.
In EW0 mode, the status register can be read in the following cases:

- When a given address in the user ROM area is read after writing the read status register command
- When a given address in the user ROM area is read after executing program or block erase command but before executing the read array command.

19.4.4.1 Sequencer Status (Bits SR7 and FMR00)

The sequencer status bits indicate the operating status of the flash memory. SR7 is set to 0 (busy) during auto-programming and auto-erasure, and is set to 1 (ready) at the same time the operation completes.

19.4.4.2 Erase Status (Bits SR5 and FMR07)

Refer to **19.4.5 Full Status Check**.

19.4.4.3 Program Status (Bits SR4 and FMR06)

Refer to **19.4.5 Full Status Check**.

Table 19.5 Status Register Bits

Status Register Bit	FMR0 Register Bit	Status Name	Description		Value after Reset
			0	1	
SR0 (D0)	–	Reserved	–	–	–
SR1 (D1)	–	Reserved	–	–	–
SR2 (D2)	–	Reserved	–	–	–
SR3 (D3)	–	Reserved	–	–	–
SR4 (D4)	FMR06	Program status	Completed normally	Error	0
SR5 (D5)	FMR07	Erase status	Completed normally	Error	0
SR6 (D6)	–	Reserved	–	–	–
SR7 (D7)	FMR00	Sequencer status	Busy	Ready	1

D0 to D7: Indicate the data bus which is read when the read status register command is executed.
Bits FMR07 (SR5) to FMR06 (SR4) are set to 0 by executing the clear status register command.
When the FMR07 bit (SR5) or FMR06 bit (SR4) is set to 1, the program and block erase commands cannot be accepted.

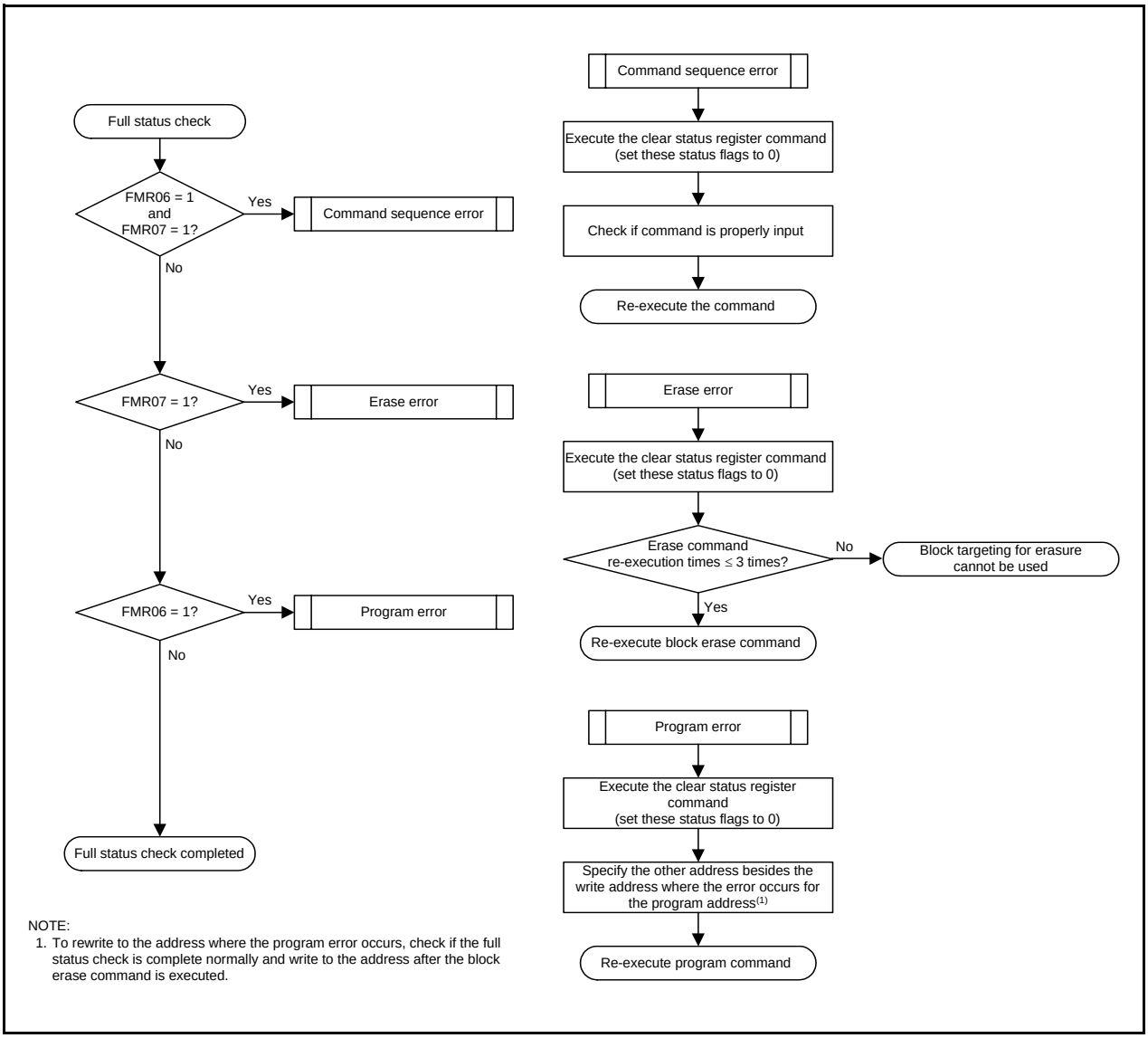
19.4.5 Full Status Check

When an error occurs, bits FMR06 to FMR07 in the FMR0 register are set to 1, indicating the occurrence of an error. Therefore, checking these status bits (full status check) can be used to determine the execution result. Table 19.6 lists the Errors and FMR0 Register Status. Figure 19.16 shows the Full Status Check and Handling Procedure for Individual Errors.

Table 19.6 Errors and FMR0 Register Status

FMR0 Register (Status Register) Status		Error	Error Occurrence Condition
FMR07(SR5)	FMR06(SR4)		
1	1	Command sequence error	• When a command is not written correctly • When invalid data other than that which can be written in the second bus cycle of the block erase command is written (i.e., other than D0h or FFh)(1) • When the program command or block erase command is executed while rewriting is disabled by the FMR02 bit in the FMR0 register, or the FMR15 or FMR16 bit in the FMR1 register. • When an address not allocated in flash memory is input during erase command input • When attempting to erase the block for which rewriting is disabled during erase command input. • When an address not allocated in flash memory is input during write command input. • When attempting to write to a block for which rewriting is disabled during write command input.
1	0	Erase error	• When the block erase command is executed but auto-erasure does not complete correctly
0	1	Program error	• When the program command is executed but not auto-programming does not complete.

NOTE:
1. The MCU enters read array mode when FFh is written in the second bus cycle of these commands. At the same time, the command code written in the first bus cycle is disabled.



NOTE:
1. To rewrite to the address where the program error occurs, check if the full status check is complete normally and write to the address after the block erase command is executed.

Figure 19.16 Full Status Check and Handling Procedure for Individual Errors

19.5 Standard Serial I/O Mode

In standard serial I/O mode, the user ROM area can be rewritten while the MCU is mounted on-board by using a serial programmer which is suitable for the MCU.
There are three types of Standard serial I/O modes:

- Standard serial I/O mode 1 .....Clock synchronous serial I/O used to connect with a serial programmer
- Standard serial I/O mode 2 .....Clock asynchronous serial I/O used to connect with a serial programmer
- Standard serial I/O mode 3 .....Special clock asynchronous serial I/O used to connect with a serial programmer

This MCU uses Standard serial I/O mode 2 and Standard serial I/O mode 3.

Refer to **Appendix 2. Connection Examples between Serial Writer and On-Chip Debugging Emulator.** Contact the manufacturer of your serial programmer for details. Refer to the user's manual of your serial programmer for instructions on how to use it.

Table 19.7 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2), Table 19.8 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3), and Figure 19.17 shows Pin Connections for Standard Serial I/O Mode 3.
After processing the pins shown in Table 19.8 and rewriting the flash memory using the programmer, apply "H" to the MODE pin and reset the hardware to run a program in the flash memory in single-chip mode.

19.5.1 ID Code Check Function

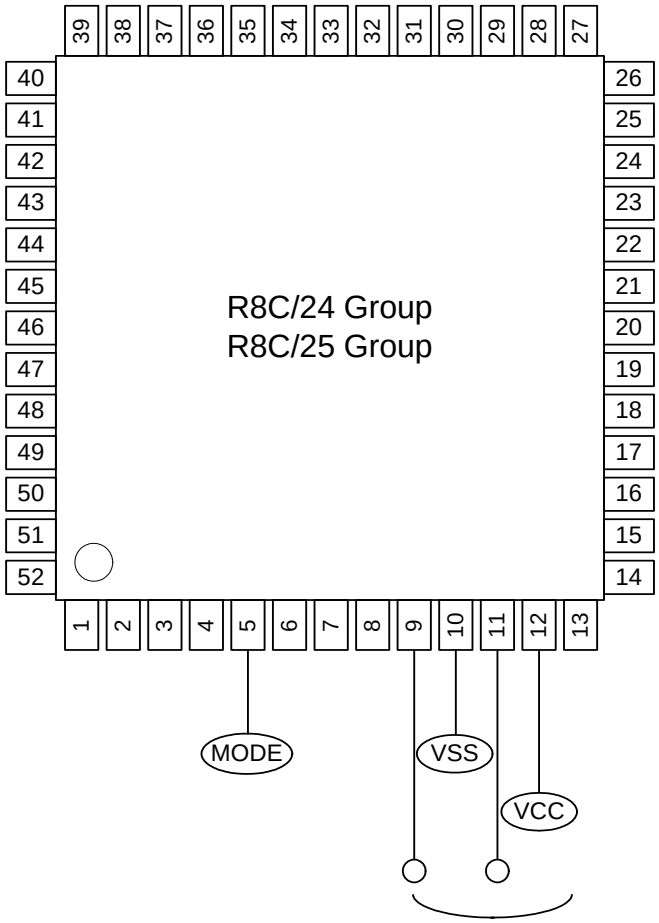
The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match (refer to **19.3 Functions to Prevent Rewriting of Flash Memory**).

Table 19.7 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Description
VCC,VSS	Power input		Apply the voltage guaranteed for programming and erasure to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
P4_6/XIN	P4_6 input/clock input	I	Connect a ceramic resonator or crystal oscillator between the XIN and XOUT pins.
P4_7/XOUT	P4_7 input/clock output	I/O	
P4_3/XCIN	P4_3 input/clock input	I	Connect crystal oscillator between pins XCIN and XCOUT.
P4_4/XCOUT	P4_4 input/clock output	I/O	
P0_0 to P0_7	Input port P0	I	Input "H" or "L" level signal or leave the pin open.
P1_0 to P1_7	Input port P1	I	Input "H" or "L" level signal or leave the pin open.
P2_0 to P2_7	Input port P2	I	Input "H" or "L" level signal or leave the pin open.
P3_0, P3_1, P3_3 to P3_5, P3_7	Input port P3	I	Input "H" or "L" level signal or leave the pin open.
P4_2/VREF, P4_5	Input port P4	I	Input "H" or "L" level signal or leave the pin open.
P6_0 to P6_5	Input port P6	I	Input "H" or "L" level signal or leave the pin open.
MODE	MODE	I	Input "L" level signal.
P6_6	TXD output	O	Serial data output pin.
P6_7	RXD input	I	Serial data input pin.

Table 19.8 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin	Name	I/O	Description
VCC,VSS	Power input		Apply the voltage guaranteed for programming and erasure to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
P4_6/XIN	P4_6 input/clock input	I	Connect a ceramic resonator or crystal oscillator between the XIN and XOUT pins when connecting external oscillator. Apply “H” and “L” or leave the pin open when using as input port.
P4_7/XOUT	P4_7 input/clock output	I/O	
P4_3/XCIN	P4_3 input/clock input	I	Connect crystal oscillator between pins XCIN and XCOUT when connecting external oscillator. Apply “H” and “L” or leave the pin open when using as a port.
P4_4/XCOUT	P4_4 input/clock output	I/O	
P0_0 to P0_7	Input port P0	I	Input “H” or “L” level signal or leave the pin open.
P1_0 to P1_7	Input port P1	I	Input “H” or “L” level signal or leave the pin open.
P2_0 to P2_7	Input port P2	I	Input “H” or “L” level signal or leave the pin open.
P3_0, P3_1, P3_3 to P3_5, P3_7	Input port P3	I	Input “H” or “L” level signal or leave the pin open.
P4_2/VREF, P4_5	Input port P4	I	Input “H” or “L” level signal or leave the pin open.
P6_0 to P6_7	Input port P6	I	Input “H” or “L” level signal or leave the pin open.
MODE	MODE	I/O	Serial data I/O pin. Connect to the flash programmer.



Mode setting

Signal	Value
MODE	Voltage from programmer
$\overline{\text{RESET}}$	VSS → VCC

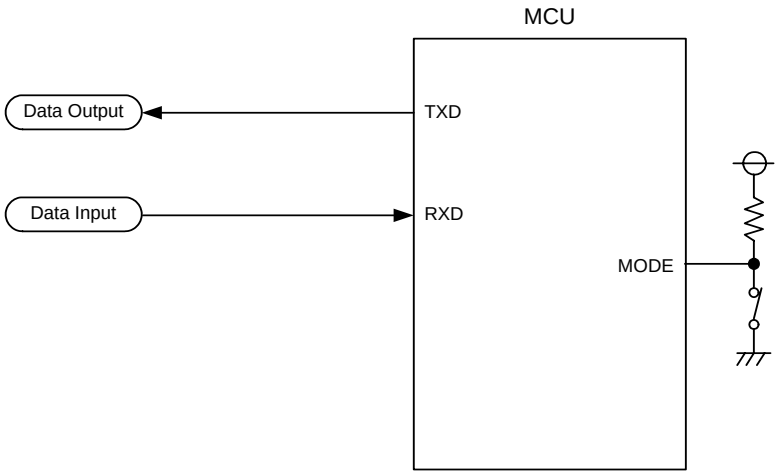
Package: PLQP0052JA-A

NOTE:
1. It is not necessary to connect an oscillating circuit when operating with the on-chip oscillator clock.

Figure 19.17 Pin Connections for Standard Serial I/O Mode 3

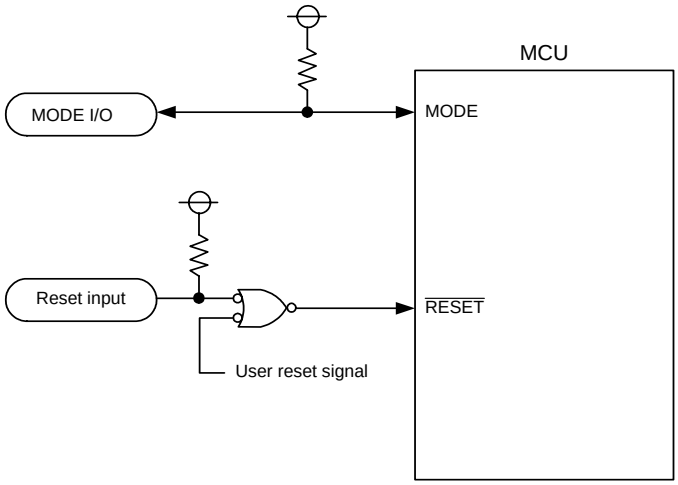
19.5.1.1 Example of Circuit Application in Standard Serial I/O Mode

Figure 19.18 shows an Example of Pin Processing in Standard Serial I/O Mode 2, and Figure 19.19 shows an Example of Pin Processing in Standard Serial I/O Mode 3. Since the controlled pins vary depending on the programmer, refer to the manual of your serial programmer for details.



NOTES:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
2. Connecting the oscillation is necessary. Set the main clock frequency 1 MHz to 20 MHz. Refer to **Appendix Figure 2.1 Connection Example with M16C Flash Starter (M3A-0806)**.

Figure 19.18 Example of Pin Processing in Standard Serial I/O Mode 2



NOTES:
1. Controlled pins and external circuits vary depending on the programmer. Refer to the programmer manual for details.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
3. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillating circuit.

Figure 19.19 Example of Pin Processing in Standard Serial I/O Mode 3

19.6 Parallel I/O Mode

Parallel I/O mode is used to input and output software commands, addresses and data necessary to control (read, program, and erase) the on-chip flash memory. Use a parallel programmer which supports this MCU. Contact the manufacturer of the parallel programmer for more information, and refer to the user's manual of the parallel programmer for details on how to use it.
ROM areas shown in Figures 19.1 and 19.2 can be rewritten in parallel I/O mode.

19.6.1 ROM Code Protect Function

The ROM code protect function disables the reading and rewriting of the flash memory. (Refer to **19.3 Functions to Prevent Rewriting of Flash Memory**.)

19.7 Notes on Flash Memory

19.7.1 CPU Rewrite Mode

19.7.1.1 Operating Speed

Before entering CPU rewrite mode (EW0 mode), select 5 MHz or below for the CPU clock using the CM06 bit in the CM0 register and bits CM16 to CM17 in the CM1 register. This does not apply to EW1 mode.

19.7.1.2 Prohibited Instructions

The following instructions cannot be used in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

19.7.1.3 Interrupts

Table 19.9 lists the EW0 Mode Interrupts, and Table 19.10 lists the EW1 Mode Interrupts.

Table 19.9 EW0 Mode Interrupts

Mode	Status	When Maskable Interrupt Request is Acknowledged	When Watchdog Timer, Oscillation Stop Detection, Voltage Monitor 1, or Voltage Monitor 2 Interrupt Request is Acknowledged
EW0	During auto-erasure	Any interrupt can be used by allocating a vector in RAM	Once an interrupt request is acknowledged, auto-programming or auto-erasure is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts after the fixed period and the flash memory restarts. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. Execute auto-erasure again and ensure it completes normally. Since the watchdog timer does not stop during the command operation, interrupt requests may be generated. Reset the watchdog timer regularly.
	Auto-programming		

NOTES:
1. Do not use the address match interrupt while a command is being executed because the vector of the address match interrupt is allocated in ROM.
2. Do not use a non-maskable interrupt while block 0 is being automatically erased because the fixed vector is allocated in block 0.

Table 19.10 EW1 Mode Interrupts

Mode	Status	When Maskable Interrupt Request is Acknowledged	When Watchdog Timer, Oscillation Stop Detection, Voltage Monitor 1, or Voltage Monitor 2 Interrupt Request is Acknowledged
EW1	During auto-erasure (erase-suspend function enabled)	Auto-erasure is suspended after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR41 bit in the FMR4 register to 0 (erase restart) after interrupt handling completes.	Once an interrupt request is acknowledged, auto-programming or auto-erasure is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts after the fixed period and the flash memory restarts. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. Execute auto-erasure again and ensure it completes normally. Since the watchdog timer does not stop during the command operation, interrupt requests may be generated. Reset the watchdog timer regularly using the erase-suspend function.
	During auto-erasure (erase-suspend function disabled)	Auto-erasure has priority and the interrupt request acknowledgement is put on standby. Interrupt handling is executed after auto-erasure completes.	
	During auto-programming (program suspend function enabled)	Auto-programming is suspended after td(SR-SUS) and interrupt handling is executed. Auto-programming can be restarted by setting the FMR42 bit in the FMR4 register to 0 (program restart) after interrupt handling completes.	
	During auto-programming (program suspend function disabled)	Auto-programming has priority and the interrupt request acknowledgement is put on standby. Interrupt handling is executed after auto-programming completes.	

NOTES:
1. Do not use the address match interrupt while a command is executing because the vector of the address match interrupt is allocated in ROM.
2. Do not use a non-maskable interrupt while block 0 is being automatically erased because the fixed vector is allocated in block 0.

19.7.1.4 How to Access

Write 0 before writing 1 when setting the FMR01, FMR02, or FMR11 bit to 1. Do not generate an interrupt between writing 0 and 1.

19.7.1.5 Rewriting User ROM Area

In EW0 Mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

19.7.1.6 Program

Do not write additions to the already programmed address.

19.7.1.7 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.

19.7.1.8 Program and Erase Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

20. Electrical Characteristics

The electrical characteristics of N version (Topr = -20 to 85°C) and D version (Topr = -40 to 85°C) are listed below.
Please contact Renesas Technology sales offices for the electrical characteristics in the Y version (Topr = -20 to 105°C).

Table 20.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC} + 0.3	V
V_O	Output voltage		-0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	T_{opr} = 25°C	500(1)	mW
T_{opr}	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

NOTE:
1. 300 mW for the PTLG0064JA-A package.

Table 20.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.2	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8 V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2 V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$		–	–	-160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$		–	–	-80	mA
$I_{OH(peak)}$	Peak output “H” current	Except P2_0 to P2_7		–	–	-10	mA
		P2_0 to P2_7		–	–	-40	mA
$I_{OH(avg)}$	Average output “H” current	Except P2_0 to P2_7		–	–	-5	mA
		P2_0 to P2_7		–	–	-20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$		–	–	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$		–	–	80	mA
$I_{OL(peak)}$	Peak output “L” current	Except P2_0 to P2_7		–	–	10	mA
		P2_0 to P2_7		–	–	40	mA
$I_{OL(avg)}$	Average output “L” current	Except P2_0 to P2_7		–	–	5	mA
		P2_0 to P2_7		–	–	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V_{CC} < 2.7 V	0	–	5	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency		2.2 V ≤ V_{CC} ≤ 5.5 V	0	–	70	kHz
–	System clock	OCD2 = 0 XIN clock selected	3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
			2.2 V ≤ V_{CC} < 2.7 V	0	–	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	–	125	–	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	10	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ V_{CC} ≤ 5.5 V	–	–	5	MHz

NOTES:
1. V_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 20.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}	–	–	10	Bit
–	Absolute accuracy	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	–	–	±3	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 3.3 V	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 3.3 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 5 MHz, V_{ref} = AV_{CC} = 2.2 V	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 5 MHz, V_{ref} = AV_{CC} = 2.2 V	–	–	±2	LSB
R_{ladder}	Resistor ladder		V_{ref} = AV_{CC}	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	3.3	–	–	µs
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage(2)			0	–	AV_{CC}	V
–	A/D operating clock frequency	Without sample and hold	V_{ref} = AV_{CC} = 2.7 to 5.5 V	0.25	–	10	MHz
		With sample and hold	V_{ref} = AV_{CC} = 2.7 to 5.5 V	1	–	10	MHz
		Without sample and hold	V_{ref} = AV_{CC} = 2.2 to 5.5 V	0.25	–	5	MHz
		With sample and hold	V_{ref} = AV_{CC} = 2.2 to 5.5 V	1	–	5	MHz

NOTES:
1. AV_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

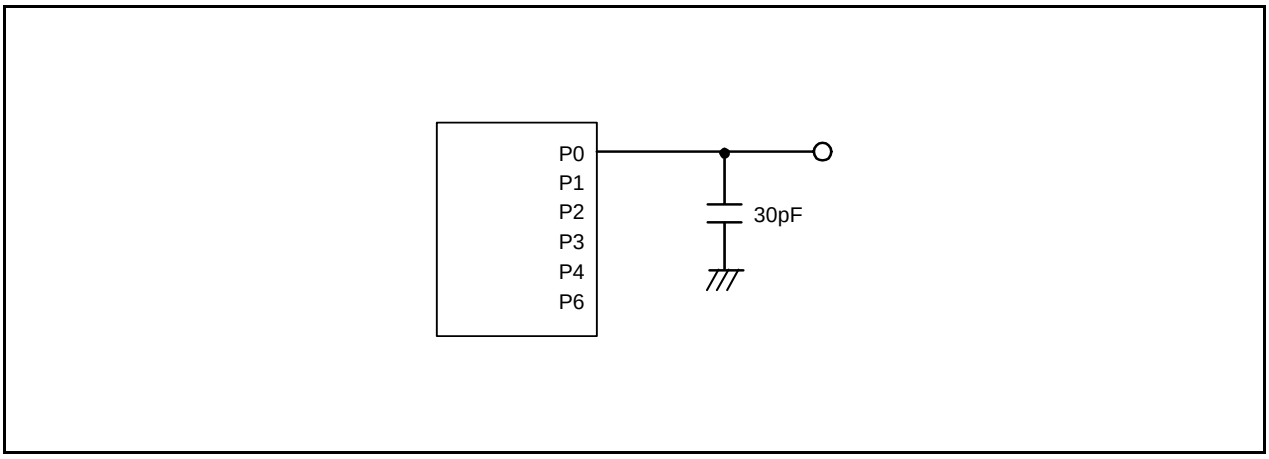


Figure 20.1 Ports P0 to P4, P6 Timing Measurement Circuit

Table 20.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/24 Group	100(3)	–	–	times
		R8C/25 Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 20.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		-20(8)	–	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. -40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

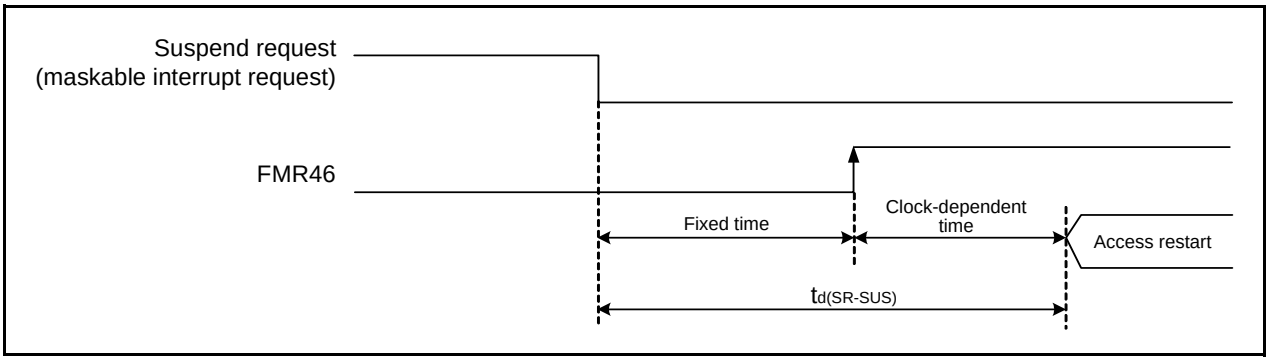


Figure 20.2 Time delay until Suspend

Table 20.6 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level		2.2	2.3	2.4	V
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	0.9	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	300	µs
Vccmin	MCU operating voltage minimum value		2.2	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 20.7 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level		2.70	2.85	3.00	V
–	Voltage monitor 1 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 20.8 Voltage Detection 2 Circuit Electrical Characteristics

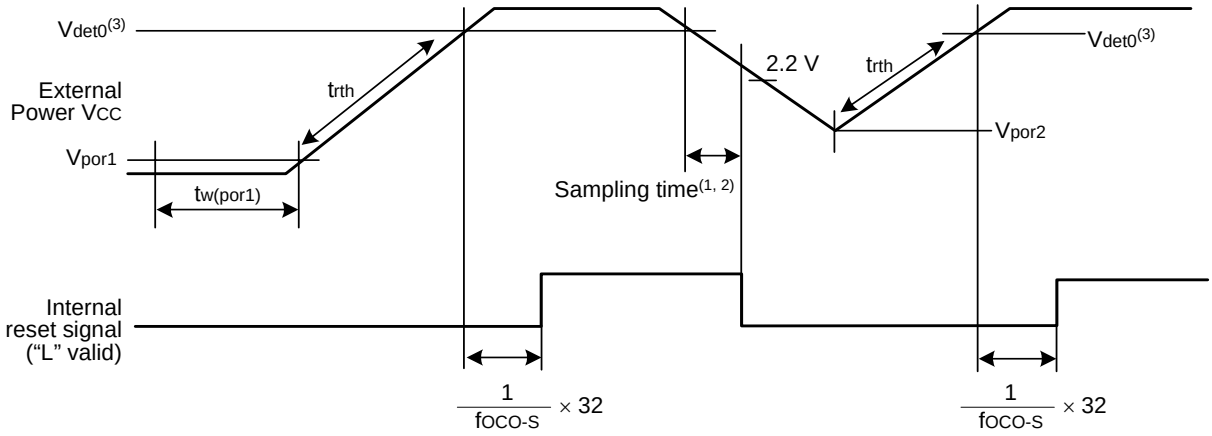
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level		3.3	3.6	3.9	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 20.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V_{det0}	V
t_{rth}	External power V_{CC} rise gradient(2)		20	–	–	mV/msec

NOTES:
1. The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if -20°C ≤ T_{opr} ≤ 85°C, maintain $t_{w(por1)}$ for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.



NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
3. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.

Figure 20.3 Power-on Reset Circuit Electrical Characteristics

Table 20.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 to 5.25 V 0°C ≤ T_{opr} ≤ 60°C(2)	39.2	40	40.8	MHz
		V_{CC} = 4.5 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C	38.8	40	40.8	MHz
		V_{CC} = 4.5 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C	38.4	40	40.8	MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38.8	40	41.2	MHz
		V_{CC} = 3.0 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	38.4	40	41.6	MHz
		V_{CC} = 2.7 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(2)	38	40	42	MHz
		V_{CC} = 2.7 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(2)	37.6	40	42.4	MHz
		V_{CC} = 2.2 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C(3)	35.2	40	44.8	MHz
		V_{CC} = 2.2 to 5.5 V -40°C ≤ T_{opr} ≤ 85°C(3)	34	40	46	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register(4)	V_{CC} = 5.0 V, T_{opr} = 25°C	–	36.864		MHz
		V_{CC} = 3.0 to 5.5 V -20°C ≤ T_{opr} ≤ 85°C	-3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	–	+0.3	–	MHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

NOTES:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. Standard values when the FRA1 register value after reset is assumed.
3. Standard values when the corrected value of the FRA6 register has been written to the FRA1 register.
4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 20.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 20.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 20.13 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			2.2 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5t_{CYC} + 100	ns
			2.2 V ≤ V_{CC} < 2.7 V	–	–	1.5t_{CYC} + 200	ns

NOTES:
1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

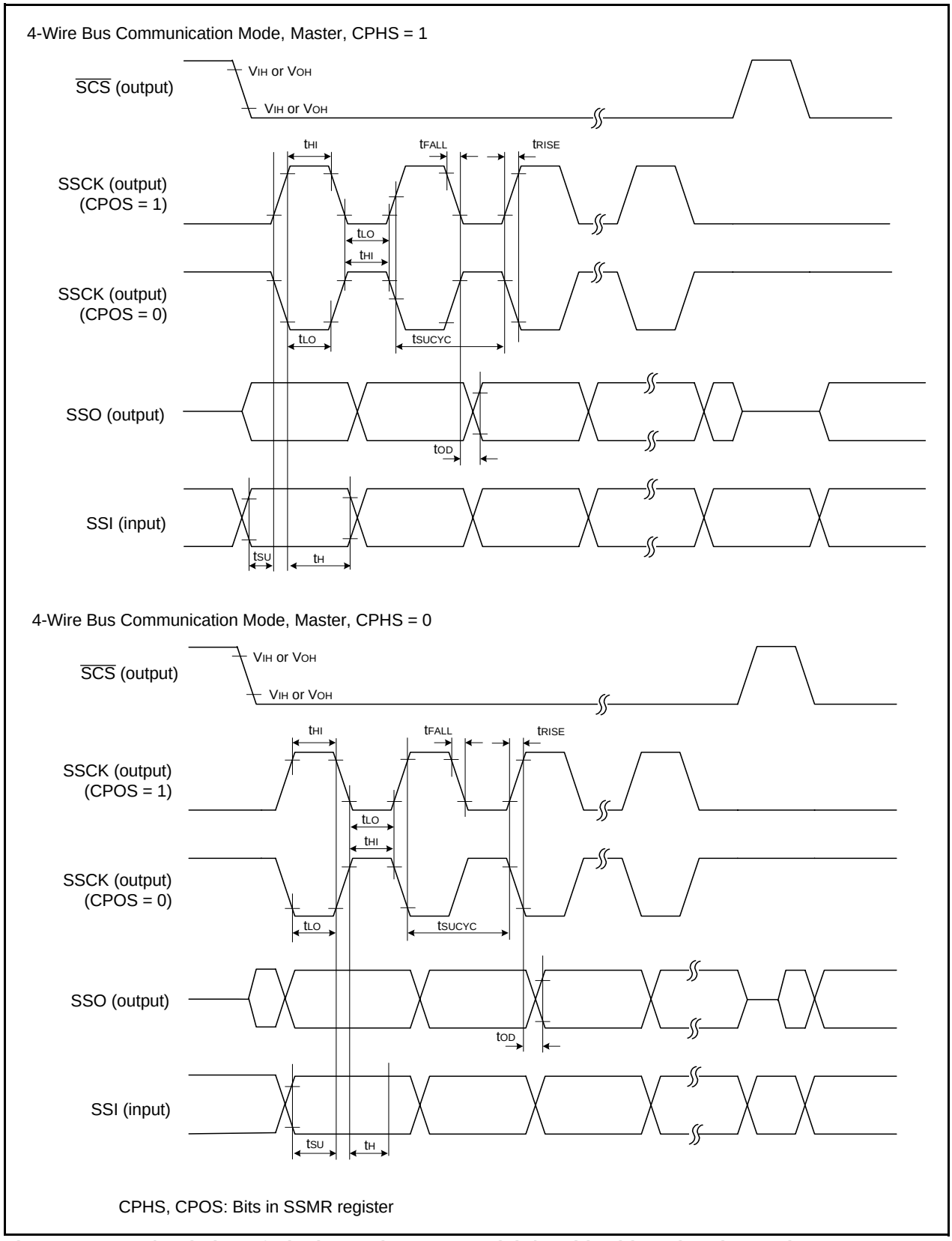


Figure 20.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

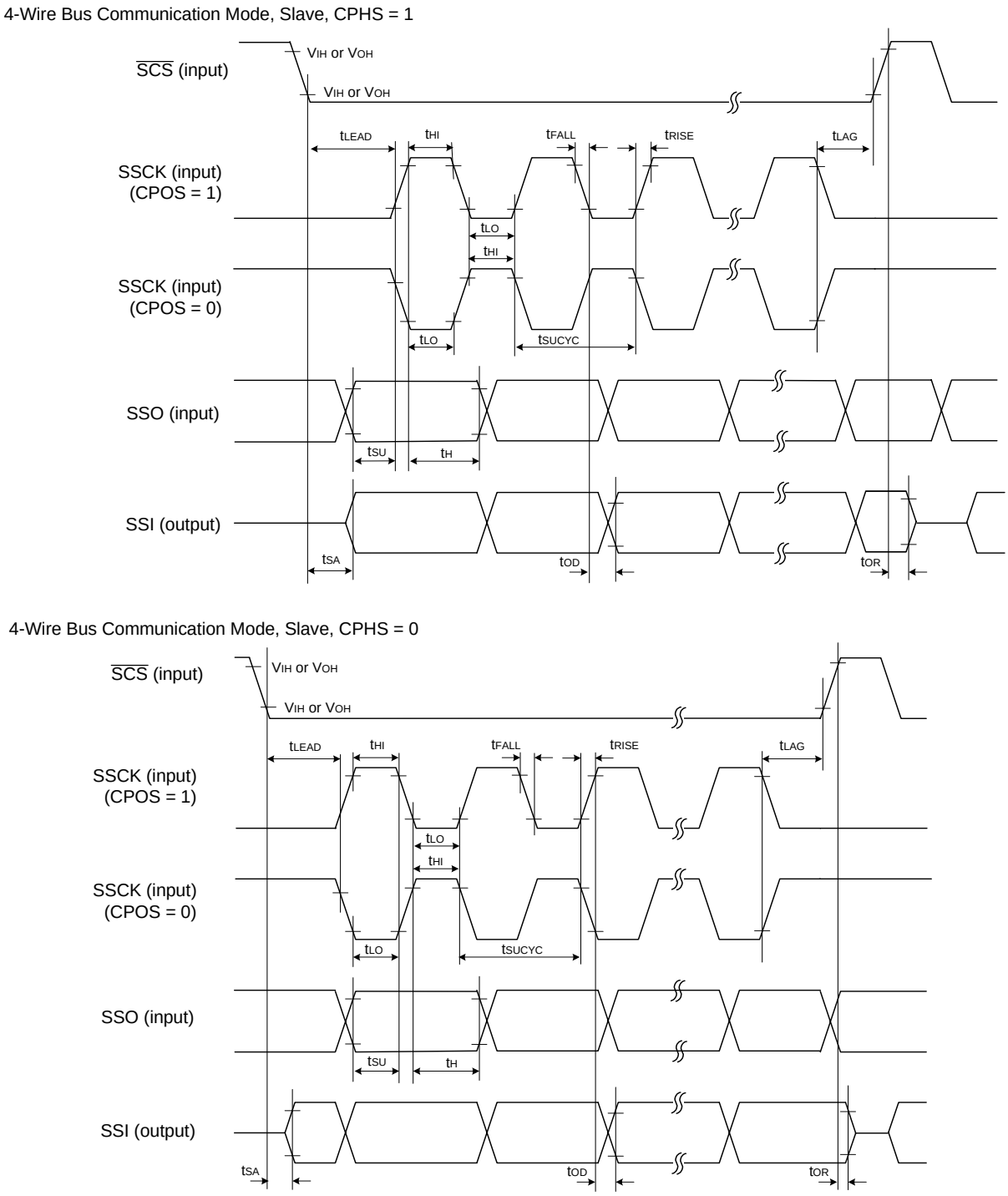


Figure 20.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

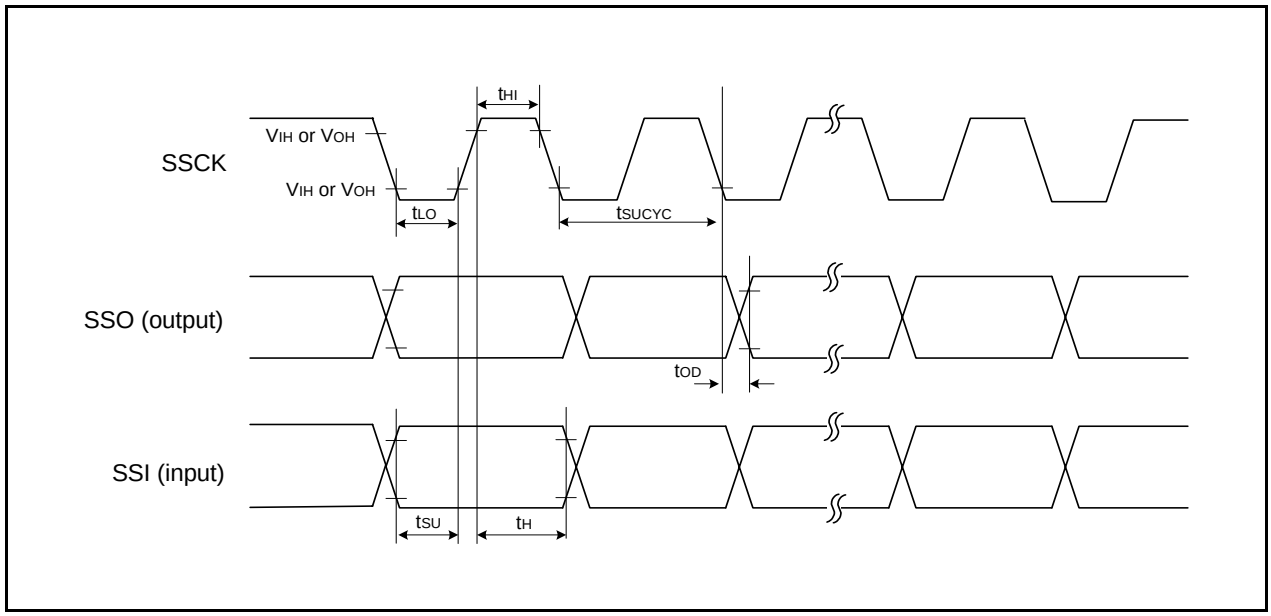


Figure 20.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 20.14 Timing Requirements of I²C bus Interface(1)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$(2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$(2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$(2)	–	–	ns
t_{sf}	SCL, SDA input fall time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$(2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$(2)	–	–	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$(2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 20$(2)	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$

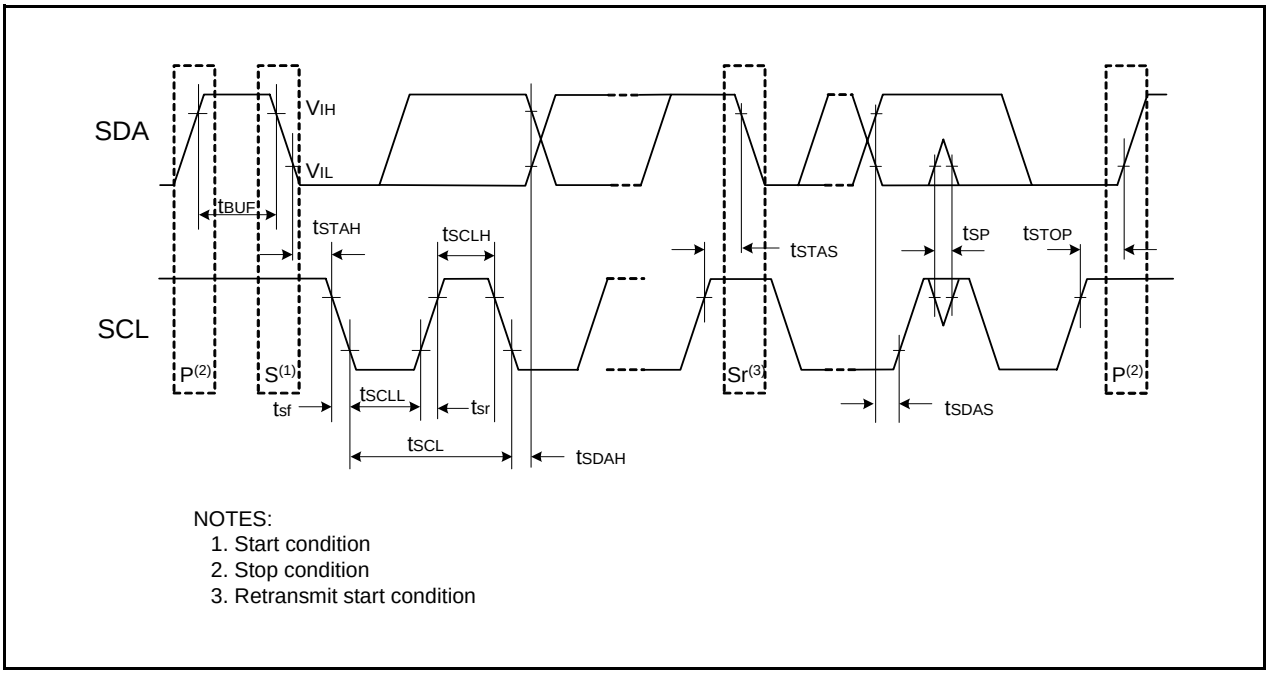


Figure 20.7 I/O Timing of I²C bus Interface

Table 20.15 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -5 mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = -200 µA		V_{CC} – 0.5	–	V_{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -5 mA	V_{CC} – 2.0	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500 µA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 µA		–	–	0.45	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 20 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 5 mA	–	–	2.0	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 µA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, Vcc = 5V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 5V		–	–	-5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, Vcc = 5V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	XIN			–	1.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 20.16 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10	17	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	130	300	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA

Table 20.17 Electrical Characteristics (3) [Vcc = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V_{SS}	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4.0	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	2.2	–	µA
		Increase during A/D converter operation	Without sample & hold	–	2.6	–	mA
			With sample & hold	–	1.6	–	mA
		Stop mode	XIN clock off, T_{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.8	3.0	µA
			XIN clock off, T_{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.2	–	µA

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 20.18 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

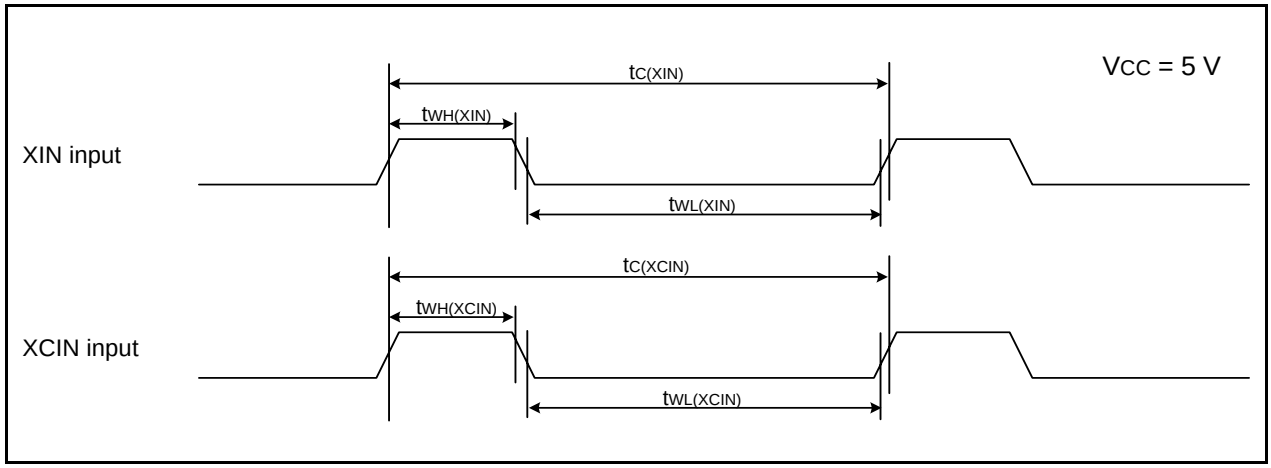


Figure 20.8 XIN Input and XCIN Input Timing Diagram when Vcc = 5 V

Table 20.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

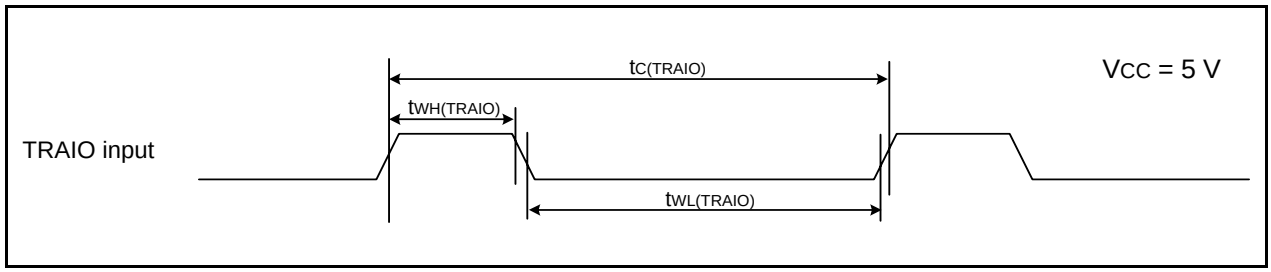


Figure 20.9 TRAIO Input Timing Diagram when Vcc = 5 V

Table 20.20 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

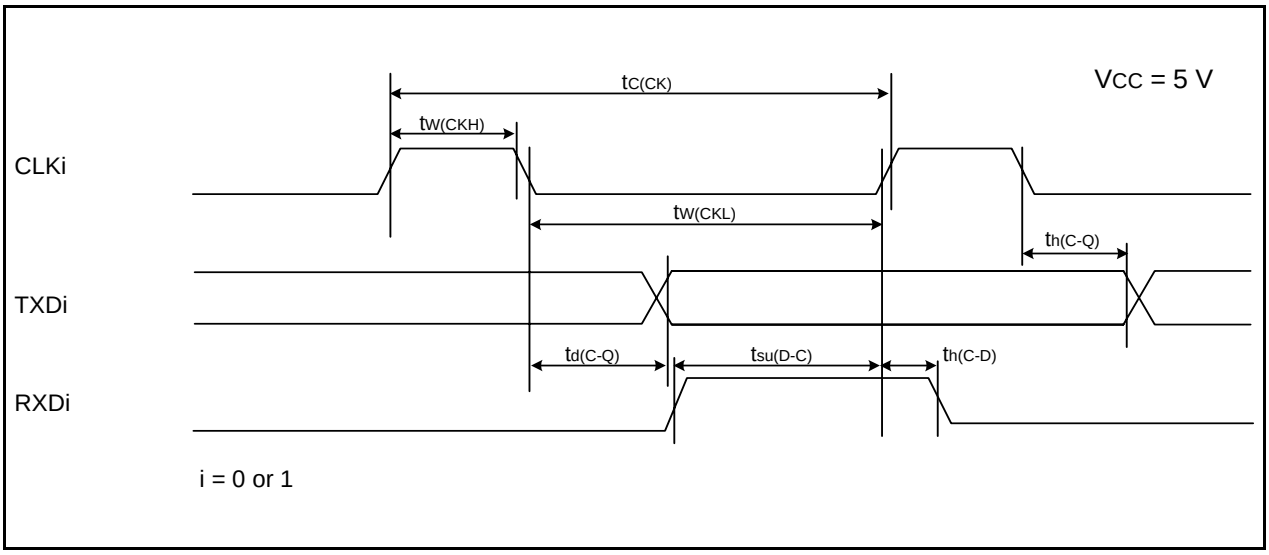


Figure 20.10 Serial Interface Timing Diagram when VCC = 5 V

Table 20.21 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

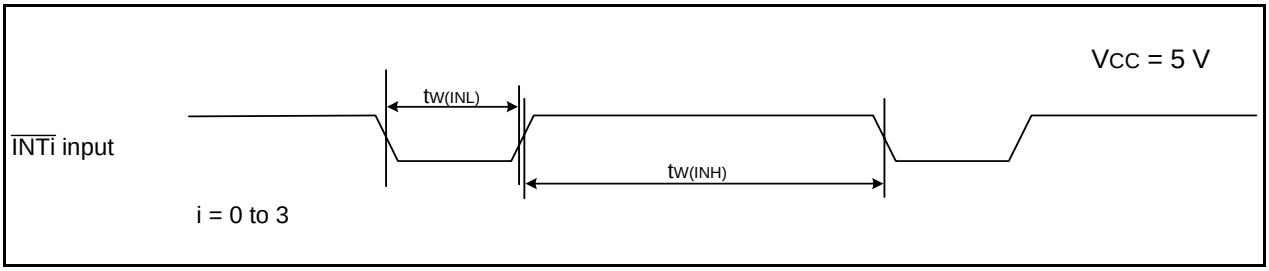


Figure 20.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V

Table 20.22 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -1 mA		Vcc - 0.5	–	Vcc	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -5 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -1 mA	Vcc - 0.5	–	Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	Vcc - 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = -50 µA	Vcc - 0.5	–	Vcc	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 1 mA		–	–	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 5 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.1	0.3	–	V
		$\overline{RESET}$			0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V, Vcc = 3V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 3V		–	–	-4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, Vcc = 3V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. Vcc =2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 20.23 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	9	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	130	300	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	70	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	55	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.8	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	2.0	–	µA
		Increase during A/D converter operation	Without sample & hold	–	0.9	–	mA
			With sample & hold	–	0.5	–	mA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA

Timing requirements
(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C) [Vcc = 3 V]

Table 20.24 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

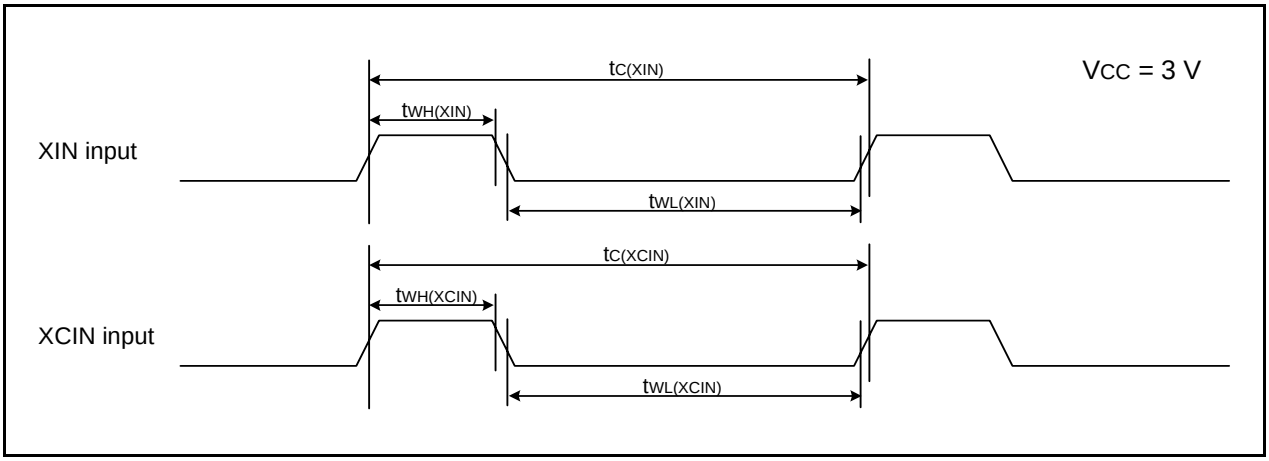


Figure 20.12 XIN Input and XCIN Input Timing Diagram when Vcc = 3 V

Table 20.25 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

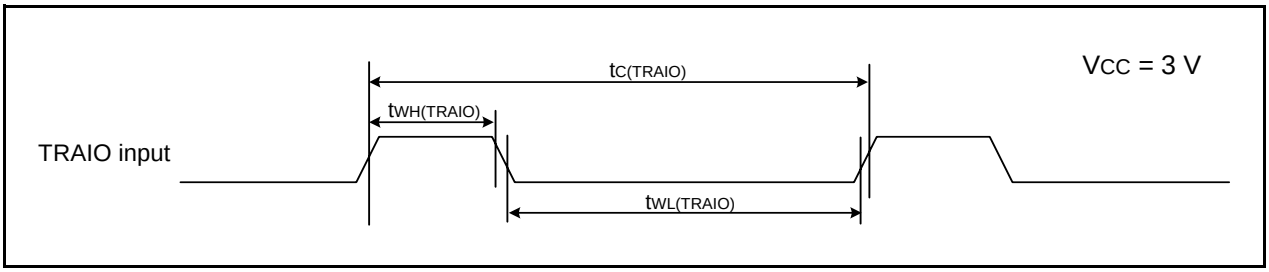


Figure 20.13 TRAIO Input Timing Diagram when Vcc = 3 V

Table 20.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

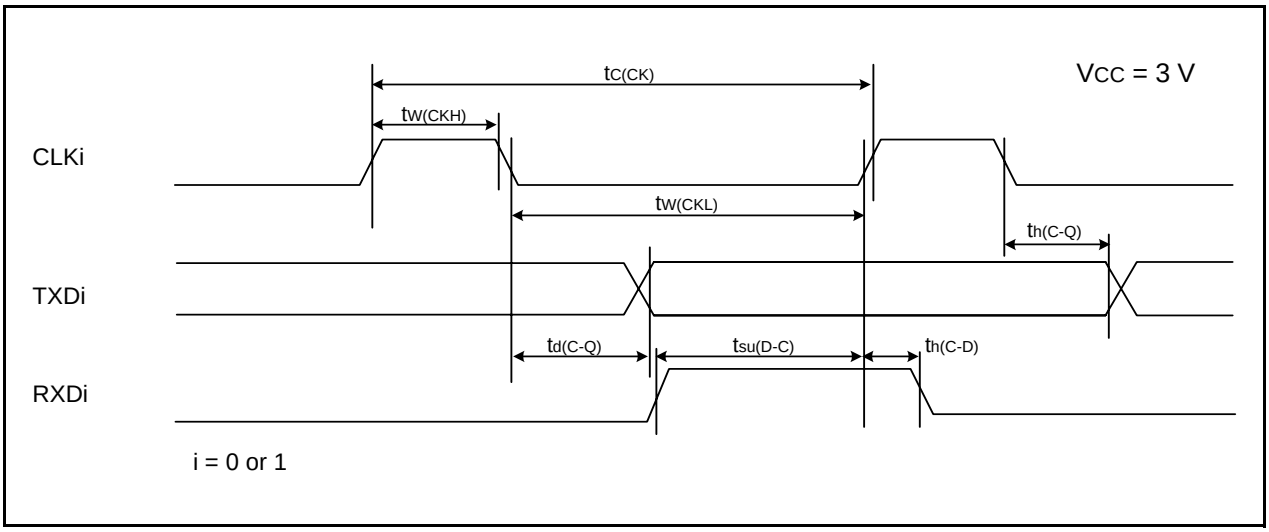


Figure 20.14 Serial Interface Timing Diagram when VCC = 3 V

Table 20.27 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

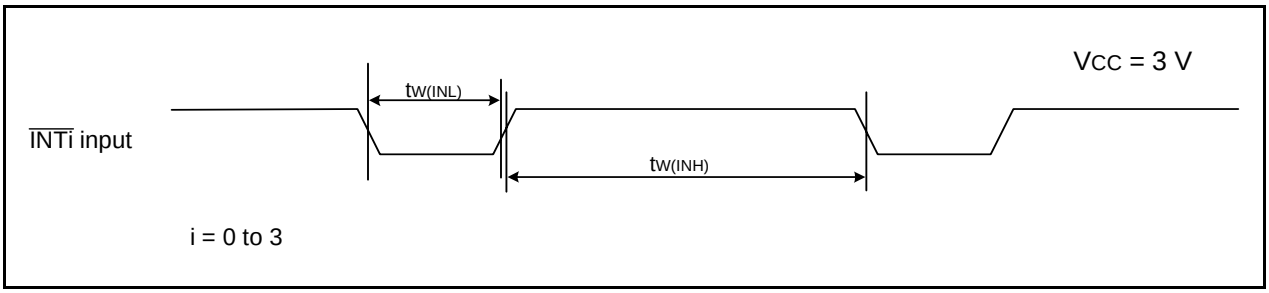


Figure 20.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 3 V

Table 20.28 Electrical Characteristics (5) [V_{CC} = 2.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = -1 mA		V_{CC} - 0.5	–	V_{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = -2 mA	V_{CC} - 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -1 mA	V_{CC} - 0.5	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	V_{CC} - 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -50 µA	V_{CC} - 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 1 mA		–	–	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 2 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, CLK1, SSI, SCL, SDA, SSO			0.05	0.3	–	V
		$\overline{RESET}$			0.05	0.15	–	V
I_{IH}	Input “H” current		VI = 2.2 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V		–	–	-4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V		100	200	600	kΩ
R_{fXIN}	Feedback resistance	XIN			–	5	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	35	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. V_{CC} = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Table 20.29 Electrical Characteristics (6) [Vcc = 2.2 V]
(Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	100	230	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	100	230	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	25	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	22	60	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	20	55	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.0	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	1.8	–	µA
		Increase during A/D converter operation	Without sample & hold	–	0.4	–	mA
			With sample & hold	–	0.3	–	mA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.7	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.1	–	µA

Timing requirements
(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C) [Vcc = 2.2 V]

Table 20.30 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

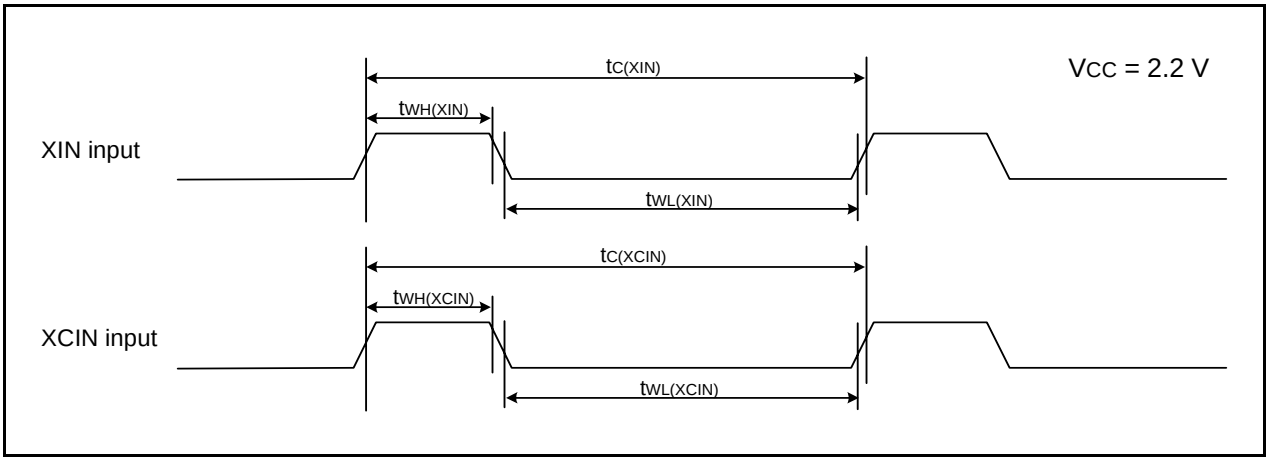


Figure 20.16 XIN Input and XCIN Input Timing Diagram when Vcc = 2.2 V

Table 20.31 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

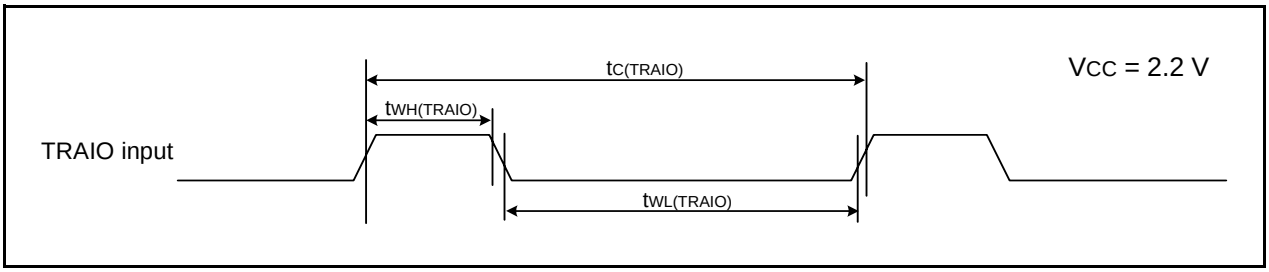


Figure 20.17 TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 20.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

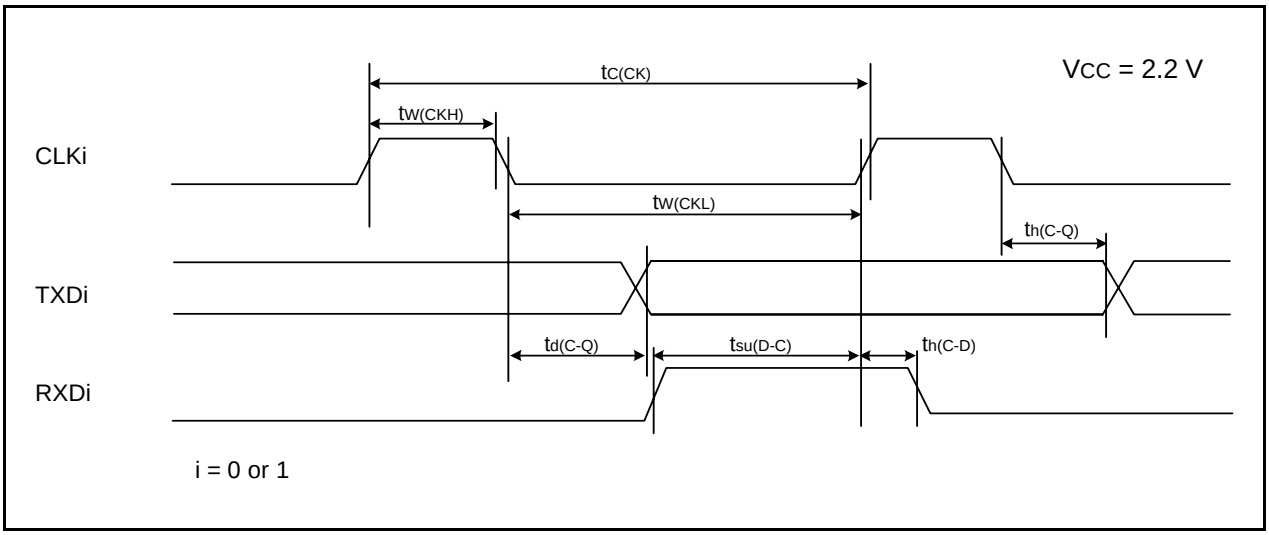


Figure 20.18 Serial Interface Timing Diagram when VCC = 2.2 V

Table 20.33 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	1000(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	1000(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

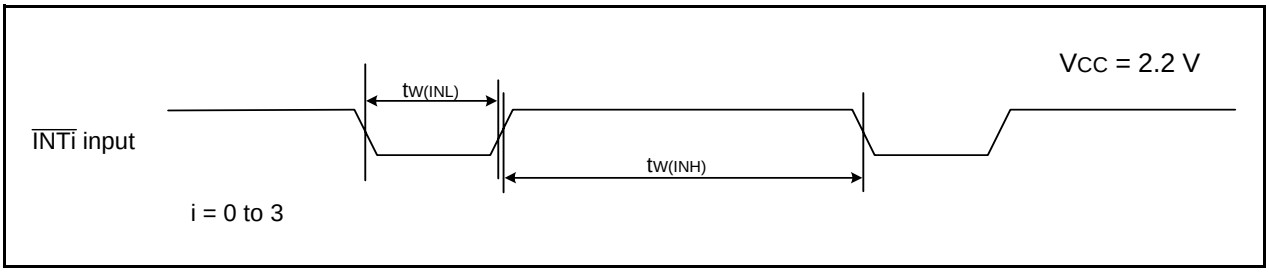


Figure 20.19 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 2.2 V

21. Usage Notes

21.1 Notes on Clock Generation Circuit

21.1.1 Stop Mode

When entering stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least 4 NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

• Program example to enter stop mode

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        BSET    0,PRCR          ; Protect disabled
        FSET    I               ; Enable interrupt
        BSET    0,CM1           ; Stop mode
        JMP.B   LABEL_001
LABEL_001 :
        NOP
        NOP
        NOP
        NOP
```

21.1.2 Wait Mode

When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the WAIT instruction and the program stops. Insert at least 4 NOP instructions after the WAIT instruction.

• Program example to execute the WAIT instruction

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        FSET    I               ; Enable interrupt
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

21.1.3 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is 2 MHz or below, set bits OCD1 to OCD0 to 00b.

21.1.4 Oscillation Circuit Constants

Ask the manufacturer of the oscillator to specify the best oscillation circuit constants for your system.
To use this MCU with supply voltage below VCC = 2.7 V, it is recommended to set the CM11 bit in the CM1 register to 1 (on-chip feedback resistor disabled), the CM15 bit to 1 (high drive capacity), and connect the feedback resistor to the chip externally.

21.2 Notes on Interrupts

21.2.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the acknowledged interrupt IR bit is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

21.2.2 SP Setting

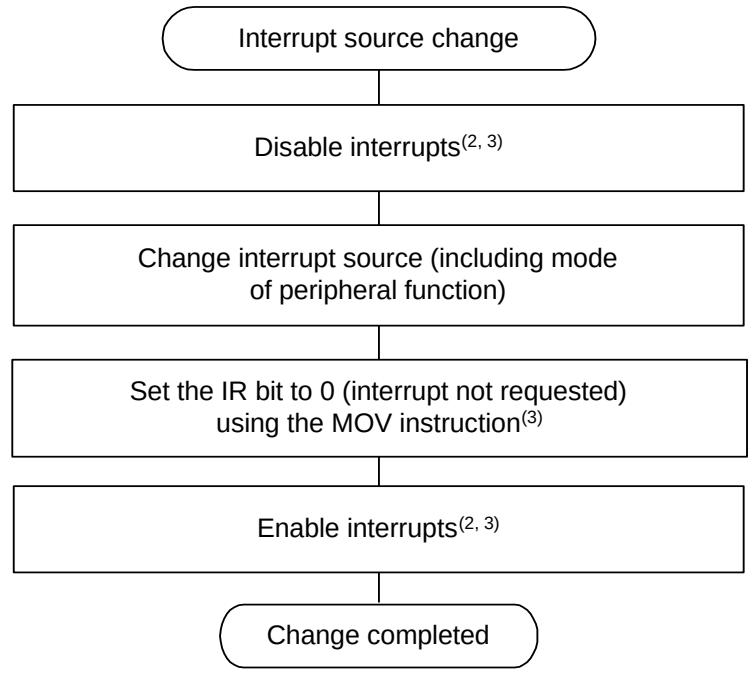
Set any value in the SP before an interrupt is acknowledged. The SP is set to 0000h after reset. Therefore, if an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

21.2.3 External Interrupt and Key Input Interrupt

Either “L” level or an “H” level of width shown in the Electrical Characteristics is necessary for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, regardless of the CPU clock.
For details, refer to **Table 20.21** (VCC = 5V), **Table 20.27** (VCC = 3V), **Table 20.33** (VCC = 2.2V) **External Interrupt $\overline{\text{INTi}}$ (i = 0 to 3) Input**.

21.2.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. When using an interrupt, set the IR bit to 0 (no interrupt requested) after changing the interrupt source. In addition, changes of interrupt sources include all factors that change the interrupt sources assigned to individual software interrupt numbers, polarities, and timing. Therefore, if a mode change of a peripheral function involves interrupt sources, edge polarities, and timing, set the IR bit to 0 (no interrupt requested) after the change. Refer to the individual peripheral function for its related interrupts.
Figure 21.1 shows an Example of Procedure for Changing Interrupt Sources.



IR bit: The interrupt control register bit of an interrupt whose source is changed.

NOTES:
1. Execute the above settings individually. Do not execute two or more settings at once (by one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled. If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 of the interrupt whose source is changed.
3. Refer to **12.6.5 Changing Interrupt Control Register Contents** for the instructions to be used and usage notes.

Figure 21.1 Example of Procedure for Changing Interrupt Sources

21.2.5 Changing Interrupt Control Register Contents

(a) The contents of an interrupt control register can only be changed while no interrupt requests corresponding to that register are generated. If interrupt requests may be generated, disable interrupts before changing the interrupt control register contents.

(b) When changing the contents of an interrupt control register after disabling interrupts, be careful to choose appropriate instructions.
Changing any bit other than IR bit
If an interrupt request corresponding to a register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt request may be ignored. If this causes a problem, use the following instructions to change the register: AND, OR, BCLR, BSET
Changing IR bit
If the IR bit is set to 0 (interrupt not requested), it may not be set to 0 depending on the instruction used. Therefore, use the MOV instruction to set the IR bit to 0.

(c) When disabling interrupts using the I flag, set the I flag as shown in the sample programs below. Refer to (b) regarding changing the contents of interrupt control registers by the sample programs.

Sample programs 1 to 3 are for preventing the I flag from being set to 1 (interrupts enabled) before the interrupt control register is changed for reasons of the internal bus or the instruction queue buffer.

Example 1: Use NOP instructions to prevent I flag from being set to 1 before interrupt control register is changed

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use dummy read to delay FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use POPC instruction to change I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

21.3 Notes on Timers

21.3.1 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after The TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

21.3.2 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (count stops) or setting the TOSSP bit in the TRBOCR register to 1 (one-shot stops), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB(1) other than the TCSTF bit.
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.

21.3.2.1 Timer mode

The following workaround should be performed in timer mode.
To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

21.3.2.2 Programmable waveform generation mode

The following three workarounds should be performed in programmable waveform generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) To change registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), synchronize the TRBO output cycle using a timer RB interrupt, etc. This operation should be preformed only once in the same output cycle. Also, make sure that writing to the TRBPR register does not occur during period A shown in Figures 21.2 and 21.3.

The following shows the detailed workaround examples.

- Workaround example (a):
  As shown in Figure 21.2, write to registers TRBSC and TRBPR in the timer RB interrupt routine. These write operations must be completed by the beginning of period A.

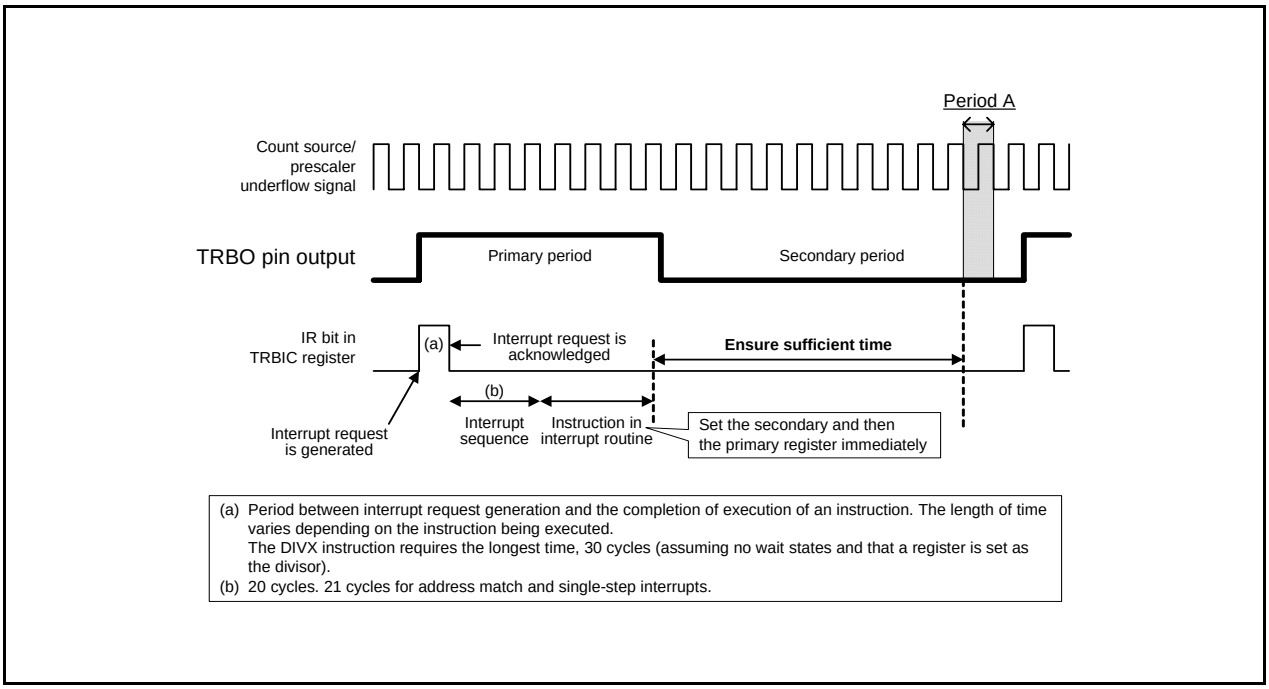


Figure 21.2 Workaround Example (a) When Timer RB interrupt is Used

• Workaround example (b):
As shown in Figure 21.3 detect the start of the primary period by the TRBO pin output level and write to registers TRBSC and TRBPR. These write operations must be completed by the beginning of period A.
If the port register's bit value is read after the port direction register's bit corresponding to the TRBO pin is set to 0 (input mode), the read value indicates the TRBO pin output value.

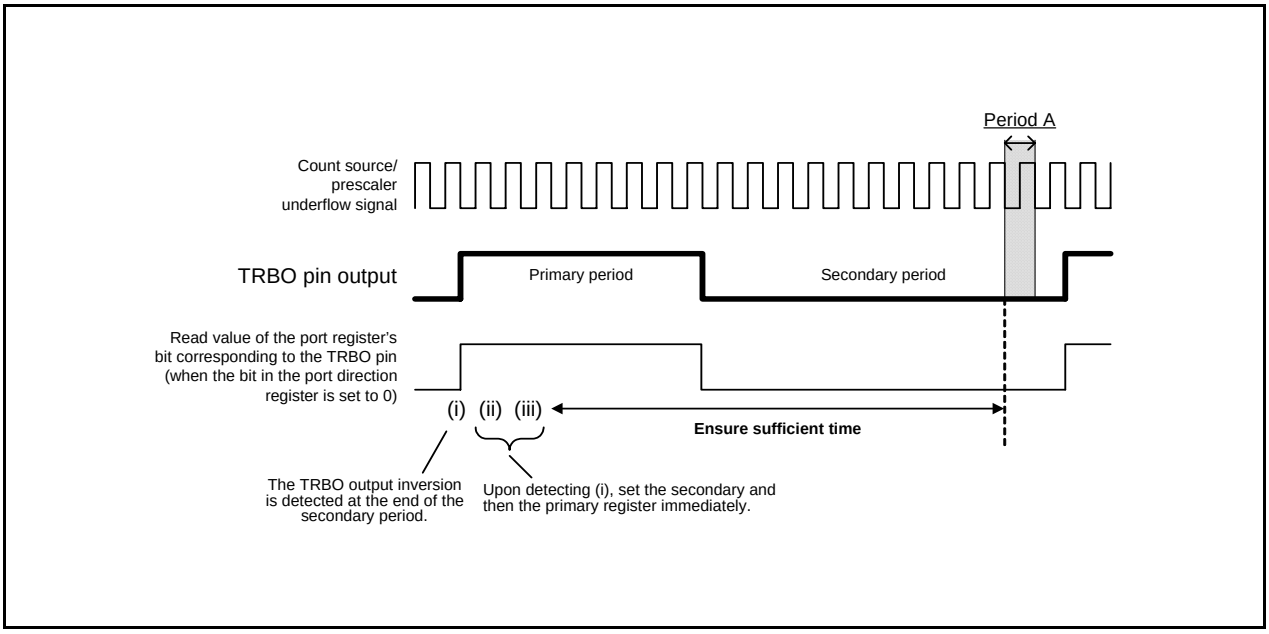


Figure 21.3 Workaround Example (b) When TRBO Pin Output Value is Read

(3) To stop the timer counting in the primary period, use the TSTOP bit in the TRBCR register. In this case, registers TRBPRE and TRBPR are initialized and their values are set to the values after reset.

21.3.2.3 Programmable one-shot generation mode

The following two workarounds should be performed in programmable one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

• When the TRBPRE register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.

• When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

21.3.2.4 Programmable wait one-shot generation mode

The following three workarounds should be performed in programmable wait one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

(3) Set registers TRBSC and TRBPR using the following procedure.

(a) To use "$\overline{\text{INT0}}$ pin one-shot trigger enabled" as the count start condition
Set the TRBSC register and then the TRBPR register. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before trigger input from the $\overline{\text{INT0}}$ pin.

(b) To use "writing 1 to TOSST bit" as the start condition
Set the TRBSC register, the TRBPR register, and then TOSST bit. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before writing to the TOSST bit.

21.3.3 Notes on Timer RD

21.3.3.1 TRDSTR Register

- Set the TRDSTR register using the MOV instruction.

- When the CSELi (i = 0 to 1) is set to 0 (the count stops at compare match of registers TRDi and TRDGRAi), the count does not stop and the TSTARTi bit remains unchanged even if 0 (count stops) is written to the TSTARTi bit.
- Therefore, set the TSTARTi bit to 0 to change other bits without changing the TSTARTi bit when the CSELi bit is se to 0.
- To stop counting by a program, set the TSTARTi bit after setting the CSELi bit to 1. Although the CSELi bit is set to 1 and the TSTARTi bit is set to 0 at the same time (with 1 instruction), the count cannot be stopped.
- Table 21.1 lists the TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops to use the TRDIOji (j = A, B, C, or D) pin with the timer RD output.

Table 21.1 TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops

Count Stop	TRDIOji Pin Output when Count Stops
When the CSELi bit is set to 1, set the TSTARTi bit to 0 and the count stops.	Hold the output level immediately before the count stops.
When the CSELi bit is set to 0, the count stops at compare match of registers TRDi and TRDGRAi.	Hold the output level after output changes by compare match.

21.3.3.2 TRDi Register (i = 0 or 1)

- When writing the value to the TRDi register by a program while the TSTARTi bit in the TRDSTR register is set to 1 (count starts), avoid overlapping with the timing for setting the TRDi register to 0000h, and then write. If the timing for setting the TRDi register to 0000h overlaps with the timing for writing the value to the TRDi register, the value is not written and the TRDi register is set to 0000h.
  These precautions are applicable when selecting the following by bits CCLR2 to CCLR0 in the TRDCRi register.
  - 001b (Clear by the TRDi register at compare match with the TRDGRAi register.)
  - 010b (Clear by the TRDi register at compare match with the TRDGRBi register.)
  - 011b (Synchronous clear)
  - 101b (Clear by the TRDi register at compare match with the TRDGRCi register.)
  - 110b (Clear by the TRDi register at compare match with the TRDGRDi register.)

- When writing the value to the TRDi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.W   #XXXXh, TRD0     ;Writing
                    JMP.B   L1               ;JMP.B
                L1: MOV.W   TRD0,DATA        ;Reading
```

21.3.3.3 TRDSRi Register (i = 0 or 1)

When writing the value to the TRDSRi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.B   #XXh, TRDSR0     ;Writing
                    JMP.B   L1               ;JMP.B
                L1: MOV.B   TRDSR0,DATA      ;Reading
```

21.3.3.4 Count Source Switch

- Switch the count source after the count stops.

Change procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.

- When changing the count source from fOCO40M to another source and stopping fOCO40M, wait 2 cycles of f1 or more after setting the clock switch, and then stop fOCO40M.

Change procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.
(3) Wait 2 or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator stops).

21.3.3.5 Input Capture Function

- Set the pulse width of the input capture signal to 3 or more cycles of the timer RD operation clock (refer to **Table 14.11 Timer RD Operation Clocks**).
- The value in the TRDi register is transferred to the TRDGRji register 2 to 3 cycles of the timer RD operation clock after the input capture signal is applied to the TRDIOji pin (i = 0 or 1, j = either A, B, C, or D) (no digital filter).

21.3.3.6 Reset Synchronous PWM Mode

- When reset synchronous PWM mode is used for motor control, make sure OLS0 = OLS1.
- Set to reset synchronous PWM mode by the following procedure:

Change procedure

(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 01b (reset synchronous PWM mode).
(4) Set the other registers associated with timer RD again.

21.3.3.7 Complementary PWM Mode

- When complementary PWM mode is used for motor control, make sure OLS0 = OLS1.
- Change bits CMD1 to CMD0 in the TRDFCR register in the following procedure.

Change procedure: When setting to complementary PWM mode (including re-set), or changing the transfer timing from the buffer register to the general register in complementary PWM mode.

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 10b or 11b (complementary PWM mode).
(4) Set the registers associated with other timer RD again.

Change procedure: When stopping complementary PWM mode

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD to 00b (timer mode, PWM mode, and PWM3 mode).

- Do not write to TRDGRA0, TRDGRB0, TRDGRA1, or TRDGRB1 register during operation.
  When changing the PWM waveform, transfer the values written to registers TRDGRD0, TRDGRC1, and TRDGRD1 to registers TRDGRB0, TRDGRA1, and TRDGRB1 using the buffer operation.
  However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).
  The PWM period cannot be changed.

- If the value in the TRDGRA0 register is assumed to be m, the TRD0 register counts m-1, m, m+1, m, m-1, in that order, when changing from increment to decrement operation.

  When changing from m to m+1, the IMFA bit is set to 1. Also, bits CMD1 to CMD0 in the TRDFCR register are set to 11b (complementary PWM mode, buffer data transferred at compare match between registers TRD0 and TRDGRA0), the content in the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1).

  During m+1, m, and m-1 operation, the IMFA bit remains unchanged and data are not transferred to registers such as the TRDGRA0 register.

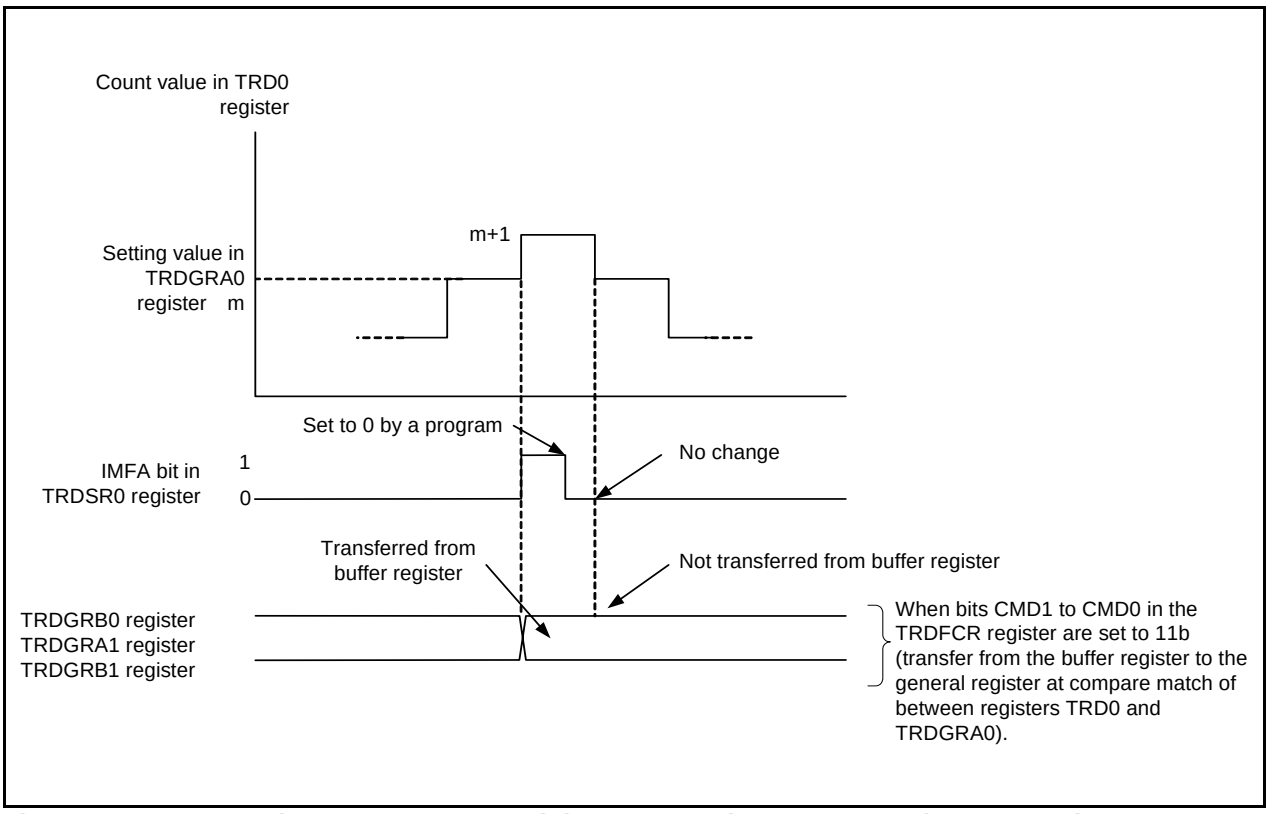


Figure 21.4 Operation at Compare Match between Registers TRD0 and TRDGRA0 in Complementary PWM Mode

- The TRD1 register counts 1, 0, FFFFh, 0, 1, in that order, when changing from decrement to increment operation.

  The UDF bit is set to 1 when changing between 1, 0, and FFFFh operation. Also, when bits CMD1 to CMD0 in the TRDFCR register are set to 10b (complementary PWM mode, buffer data transferred at underflow in the TRD1 register), the content in the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1). During FFFFh, 0, 1 operation, data are not transferred to registers such as the TRDGRB0 register. Also, at this time, the OVF bit remains unchanged.

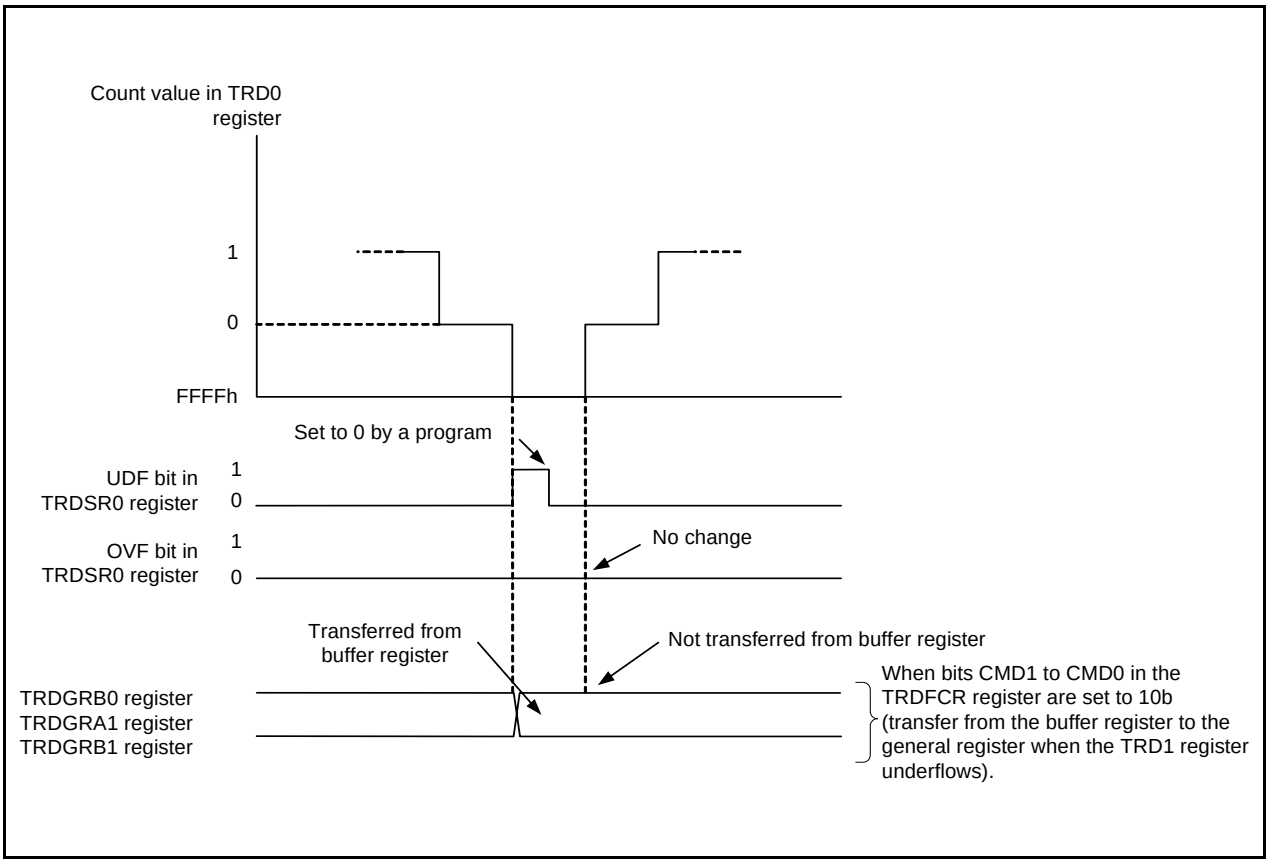
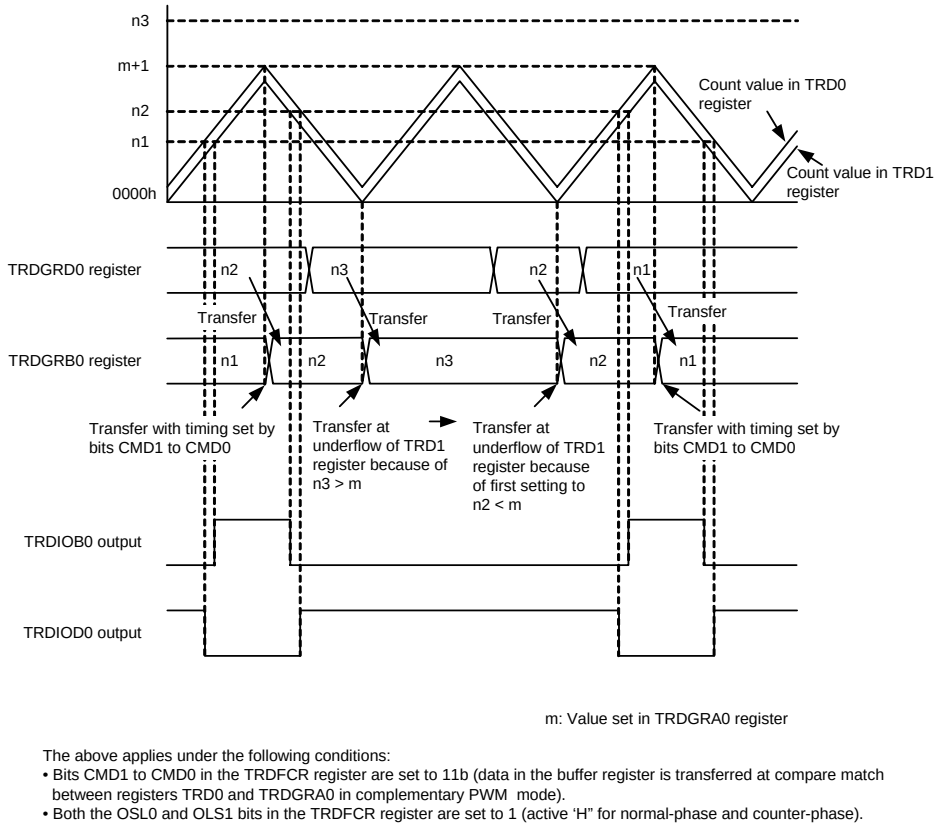


Figure 21.5 Operation when TRD1 Register Underflows in Complementary PWM Mode

- Select with bits CMD1 to CMD0 the timing of data transfer from the buffer register to the general register. However, transfer takes place with the following timing in spite of the value of bits CMD1 to CMD0 in the following cases:

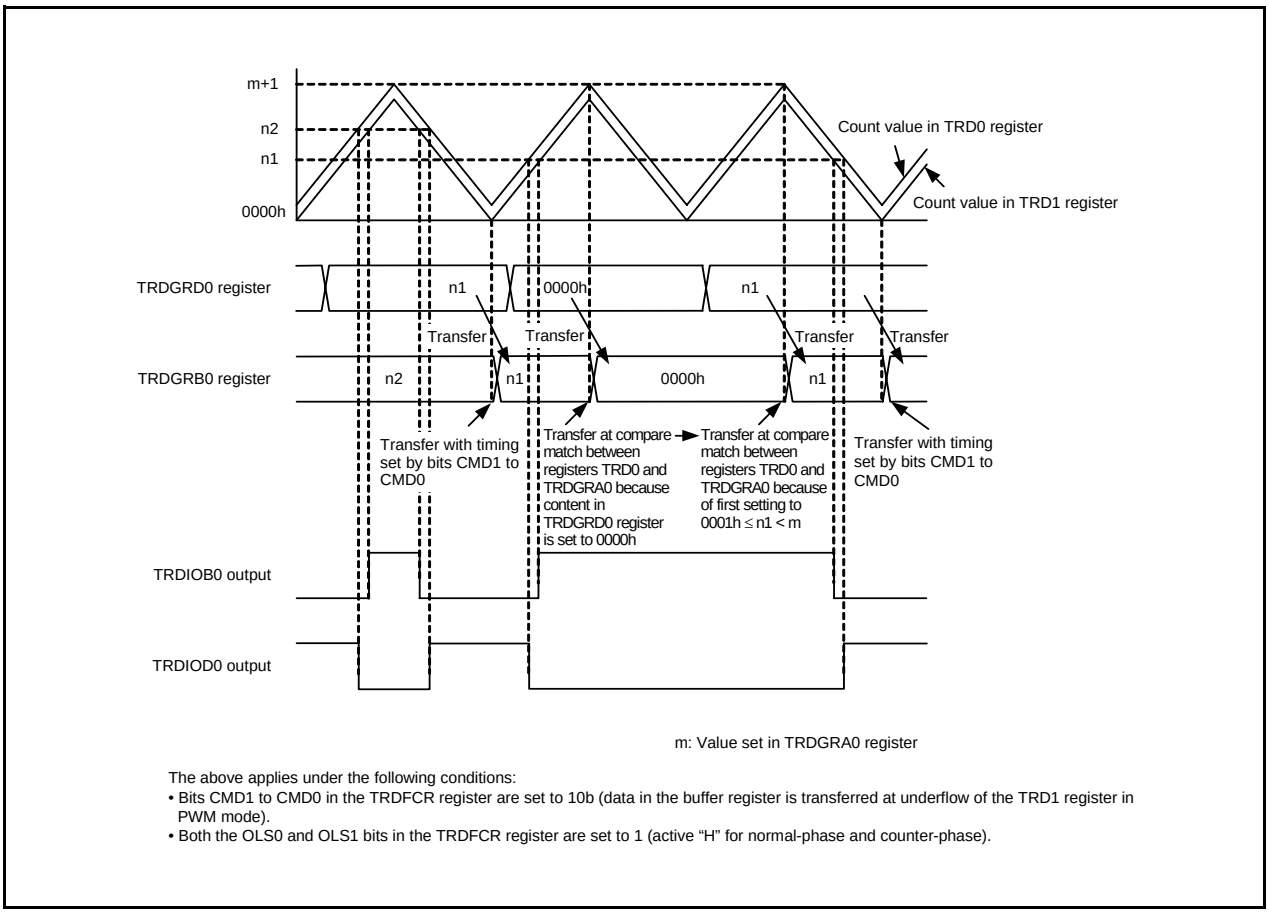
  Value in buffer register ≥ value in TRDGRA0 register:
  Transfer take place at underflow of the TRD1 register.
  After this, when the buffer register is set to 0001h or above and a smaller value than the value of the TRDGRA0 register, and the TRD1 register underflows for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 to CMD0.



The above applies under the following conditions:
- Bits CMD1 to CMD0 in the TRDFCR register are set to 11b (data in the buffer register is transferred at compare match between registers TRD0 and TRDGRA0 in complementary PWM mode).
- Both the OSL0 and OLS1 bits in the TRDFCR register are set to 1 (active 'H" for normal-phase and counter-phase).

Figure 21.6 Operation when Value in Buffer Register ≥ Value in TRDGRA0 Register in Complementary PWM Mode

When the value in the buffer register is set to 0000h:
Transfer takes place at compare match between registers TRD0 and TRDGRA0.
After this, when the buffer register is set to 0001h or above and a smaller value than the value of the TRDGRA0 register, and a compare match occurs between registers TRD0 and TRDGRA0 for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 to CMD0.



The above applies under the following conditions:
- Bits CMD1 to CMD0 in the TRDFCR register are set to 10b (data in the buffer register is transferred at underflow of the TRD1 register in PWM mode).
- Both the OLS0 and OLS1 bits in the TRDFCR register are set to 1 (active “H” for normal-phase and counter-phase).

Figure 21.7 Operation when Value in Buffer Register Is Set to 0000h in Complementary PWM Mode

21.3.3.8 Count Source fOCO40M

- The count source fOCO40M can be used with supply voltage VCC = 3.0 to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in registers TRDCR0 and TRDCR to 110b (select fOCO40M as the count source).

21.3.4 Notes on Timer RE

21.3.4.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TRECR1 register.
Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE(1) other than the TCSTF bit.
Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

NOTE:
1. Registers associated with timer RE: TRESEC, TREMIN, TREHR, TREWK, TRECR1, TRECR2, and TRECSR.

21.3.4.2 Register Setting

Write to the following registers or bits when timer RE is stopped.

- Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2
- Bits H12_H24, PM, and INT in TRECR1 register
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.
Figure 21.8 shows a Setting Example in Real-Time Clock Mode.

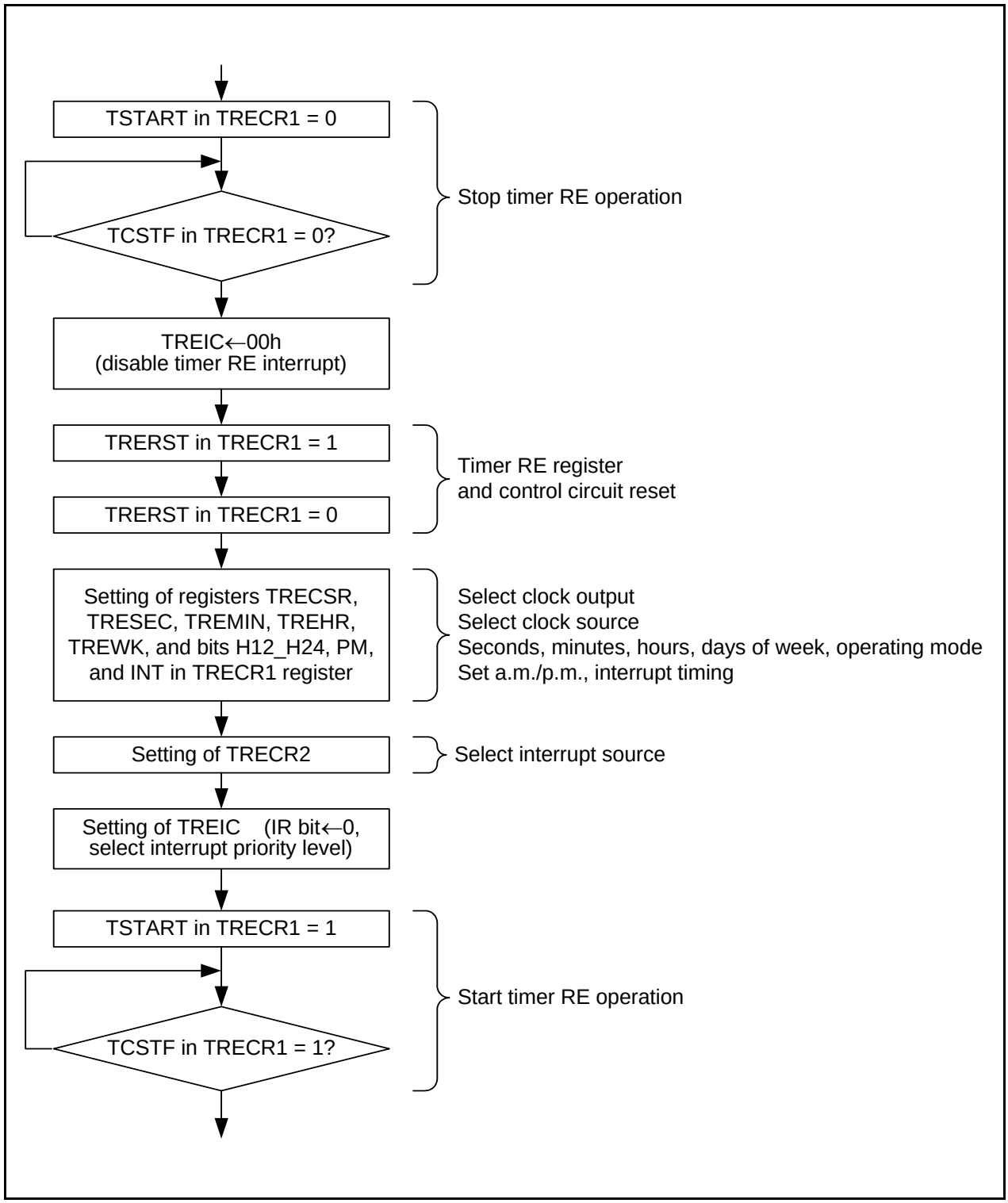


Figure 21.8 Setting Example in Real-Time Clock Mode

21.3.4.3 Time Reading Procedure of Real-Time Clock Mode

In real-time clock mode, read registers TRESEC, TREMIN, TREHR, and TREWK when time data is updated and read the PM bit in the TRECR1 register when the BSY bit is set to 0 (not while data is updated).
Also, when reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.

In order to prevent this, use the reading procedure shown below.

- Using an interrupt
  Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register in the timer RE interrupt routine.

- Monitoring with a program 1
  Monitor the IR bit in the TREIC register with a program and read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the IR bit in the TREIC register is set to 1 (timer RE interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.
(2) Monitor until the BSY bit is set to 0 after the BSY bit is set to 1 (approximately 62.5 ms while the BSY bit is set to 1).
(3) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register.
(2) Read the same register as (1) and compare the contents.
(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.

21.4 Notes on Serial Interface

- When reading data from the UiRB (i = 0 or 1) register either in the clock synchronous serial I/O mode or in the clock asynchronous serial I/O mode. Ensure the data is read in 16-bit units. When the high-order byte of the UiRB register is read, bits PER and FER in the UiRB register and the RI bit in the UiC1 register are set to 0. To check receive errors, read the UiRB register and then use the read data.

Example (when reading receive buffer register):

```
MOV.W    00A6H,R0    ; Read the U0RB register
```

- When writing data to the UiTB register in the clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first then the low-order byte, in 8-bit units.

Example (when reading transmit buffer register):

```
MOV.B    #XXH,00A3H  ; Write the high-order byte of U0TB register
MOV.B    #XXH,00A2H  ; Write the low-order byte of U0TB register
```

21.5 Notes on Clock Synchronous Serial Interface

21.5.1 Notes on Clock Synchronous Serial I/O with Chip Select

Set the IICSEL bit in the PMR register to 0 (select clock synchronous serial I/O with chip select function) to use the clock synchronous serial I/O with chip select function.

21.5.2 Notes on I^2C bus Interface

Set the IICSEL bit in the PMR register to 1 (select I^2C bus interface function) to use the I^2C bus interface.

21.5.2.1 Multimaster Operation

The following actions must be performed to use the I^2C bus interface in multimaster operation.

- Transfer rate
  Set the transfer rate by 1/1.8 or faster than the fastest rate of the other masters. For example, if the fastest transfer rate of the other masters is set to 400 kbps, the I^2C-bus transfer rate in this MCU should be set to 223 kbps (= 400/1.18) or more.

- Bits MST and TRS in the ICCR1 register setting

(a) Use the MOV instruction to set bits MST and TRS.
(b) When arbitration is lost, confirm the contents of bits MST and TRS. If the contents are other than the MST bit set to 0 and the TRS bit set to 0 (slave receive mode), set the MST bit to 0 and the TRS bit to 0 again.

21.5.2.2 Master Receive Mode

Either of the following actions must be performed to use the I^2C bus interface in master receive mode.

(a) In master receive mode while the RDRF bit in the ICSR register is set to 1, read the ICDRR register before the rising edge of the 8th clock.
(b) In master receive mode, set the RCVD bit in the ICCR1 register to 1 (disables the next receive operation) to perform 1-byte communications.

21.6 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

21.7 Notes on A/D Converter

- Write to each bit (other than bit 6) in the ADCON0 register, each bit in the ADCON1 register, or the SMP bit in the ADCON2 register when A/D conversion is stopped (before a trigger occurs).
- When the VCUT bit in the ADCON1 register is changed from 0 (VREF not connected) to 1 (VREF connected), wait for at least 1 µs before starting the A/D conversion.
- After changing the A/D operating mode, select an analog input pin again.
- When using the one-shot mode, ensure that A/D conversion is completed before reading the AD register. The IR bit in the ADIC register or the ADST bit in the ADCON0 register can be used to determine whether A/D conversion is completed.
- When using the repeat mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select the fOCO-F for the ϕAD.
- If the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program and A/D conversion is forcibly terminated during an A/D conversion operation, the conversion result of the A/D converter will be undefined. If the ADST bit is set to 0 by a program, do not use the value of the AD register.
- Connect 0.1 µF capacitor between the P4_2/VREF pin and AVSS pin.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode when the CM02 bit in the CM0 register is set to 1 (peripheral function clock stops in wait mode) during A/D conversion.

21.8 Notes on Flash Memory

21.8.1 CPU Rewrite Mode

21.8.1.1 Operating Speed

Before entering CPU rewrite mode (EW0 mode), select 5 MHz or below for the CPU clock using the CM06 bit in the CM0 register and bits CM16 to CM17 in the CM1 register. This does not apply to EW1 mode.

21.8.1.2 Prohibited Instructions

The following instructions cannot be used in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

21.8.1.3 Interrupts

Table 21.2 lists the EW0 Mode Interrupts, and Table 21.3 lists the EW1 Mode Interrupts.

Table 21.2 EW0 Mode Interrupts

Mode	Status	When Maskable Interrupt Request is Acknowledged	When Watchdog Timer, Oscillation Stop Detection, Voltage Monitor 1, or Voltage Monitor 2 Interrupt Request is Acknowledged
EW0	During auto-erasure	Any interrupt can be used by allocating a vector in RAM	Once an interrupt request is acknowledged, auto-programming or auto-erasure is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts after the fixed period and the flash memory restarts. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. Execute auto-erasure again and ensure it completes normally. Since the watchdog timer does not stop during the command operation, interrupt requests may be generated. Reset the watchdog timer regularly.
	Auto-programming		

NOTES:
1. Do not use the address match interrupt while a command is being executed because the vector of the address match interrupt is allocated in ROM.
2. Do not use a non-maskable interrupt while block 0 is being automatically erased because the fixed vector is allocated in block 0.

Table 21.3 EW1 Mode Interrupts

Mode	Status	When Maskable Interrupt Request is Acknowledged	When Watchdog Timer, Oscillation Stop Detection, Voltage Monitor 1, or Voltage Monitor 2 Interrupt Request is Acknowledged
EW1	During auto-erasure (erase-suspend function enabled)	Auto-erasure is suspended after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR41 bit in the FMR4 register to 0 (erase restart) after interrupt handling completes.	Once an interrupt request is acknowledged, auto-programming or auto-erasure is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts after the fixed period and the flash memory restarts. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. Execute auto-erasure again and ensure it completes normally. Since the watchdog timer does not stop during the command operation, interrupt requests may be generated. Reset the watchdog timer regularly using the erase-suspend function.
	During auto-erasure (erase-suspend function disabled)	Auto-erasure has priority and the interrupt request acknowledgement is put on standby. Interrupt handling is executed after auto-erasure completes.	
	During auto-programming (program suspend function enabled)	Auto-programming is suspended after td(SR-SUS) and interrupt handling is executed. Auto-programming can be restarted by setting the FMR42 bit in the FMR4 register to 0 (program restart) after interrupt handling completes.	
	During auto-programming (program suspend function disabled)	Auto-programming has priority and the interrupt request acknowledgement is put on standby. Interrupt handling is executed after auto-programming completes.	

NOTES:
1. Do not use the address match interrupt while a command is executing because the vector of the address match interrupt is allocated in ROM.
2. Do not use a non-maskable interrupt while block 0 is being automatically erased because the fixed vector is allocated in block 0.

21.8.1.4 How to Access

Write 0 before writing 1 when setting the FMR01, FMR02, or FMR11 bit to 1. Do not generate an interrupt between writing 0 and 1.

21.8.1.5 Rewriting User ROM Area

In EW0 Mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

21.8.1.6 Program

Do not write additions to the already programmed address.

21.8.1.7 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.

21.8.1.8 Program and Erase Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

21.9 Notes on Noise

21.9.1 Inserting a Bypass Capacitor between VCC and VSS Pins as a Countermeasure against Noise and Latch-up

Connect a bypass capacitor (at least 0.1 μF) using the shortest and thickest write possible.

21.9.2 Countermeasures against Noise Error of Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU's internal noise control circuitry. In such cases the contents of the port related registers may be changed.
As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may be created between the reset routine and interrupt routines.

22. Notes on On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R8C/24 Group and R8C/25 Group take note of the following.

(1) Do not access the related UART1 registers.
(2) Some of the user flash memory and RAM areas are used by the on-ship debugger. These areas cannot be accessed by the user.
Refer to the on-chip debugger manual for which areas are used.
(3) Do not set the address match interrupt (registers AIER, RMAD0, and RMAD1 and fixed vector tables) in a user system.
(4) Do not use the BRK instruction in a user system.
(5) Debugging is available under the condition of supply voltage VCC = 2.7 to 5.5 V. Debugging with the on-chip debugger under less than 2.7 V is not allowed.

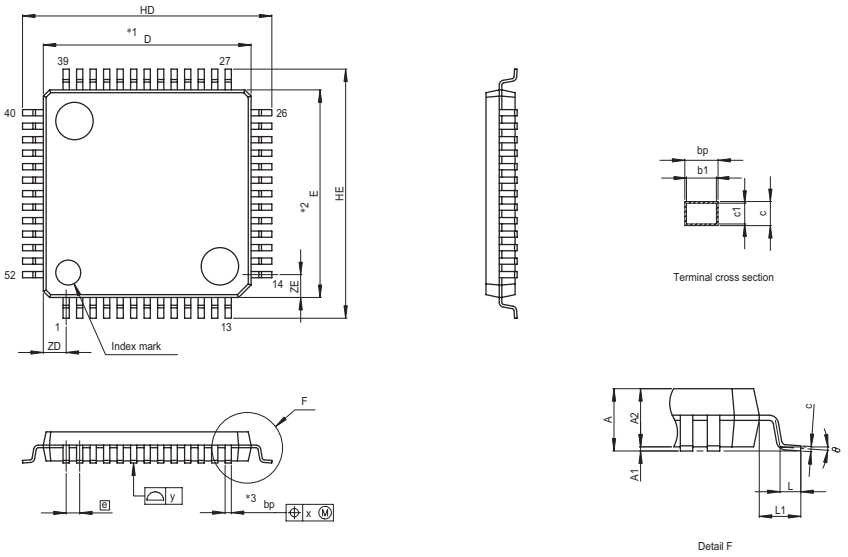
Connecting and using the on-chip debugger has some special restrictions. Refer to the on-chip debugger manual for details.

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3g

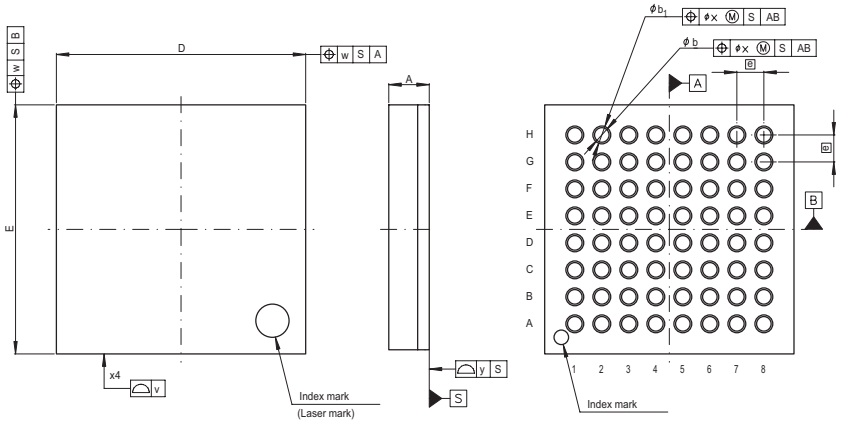
Under development



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.1	—
Z_E	—	1.1	—
L	0.35	0.5	0.65
L_1	—	1.0	—

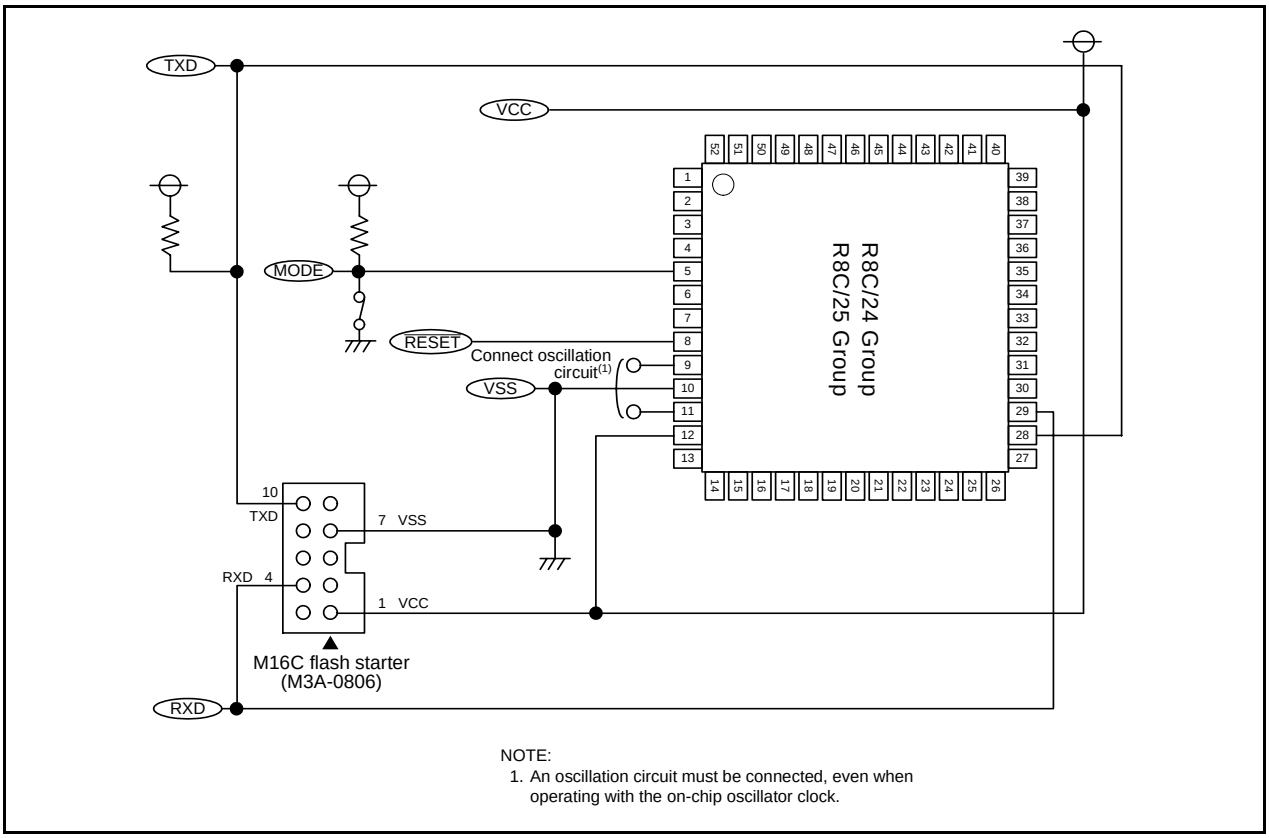
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA64-6x6-0.65	PTLG0064JA-A	64F0G	0.07g



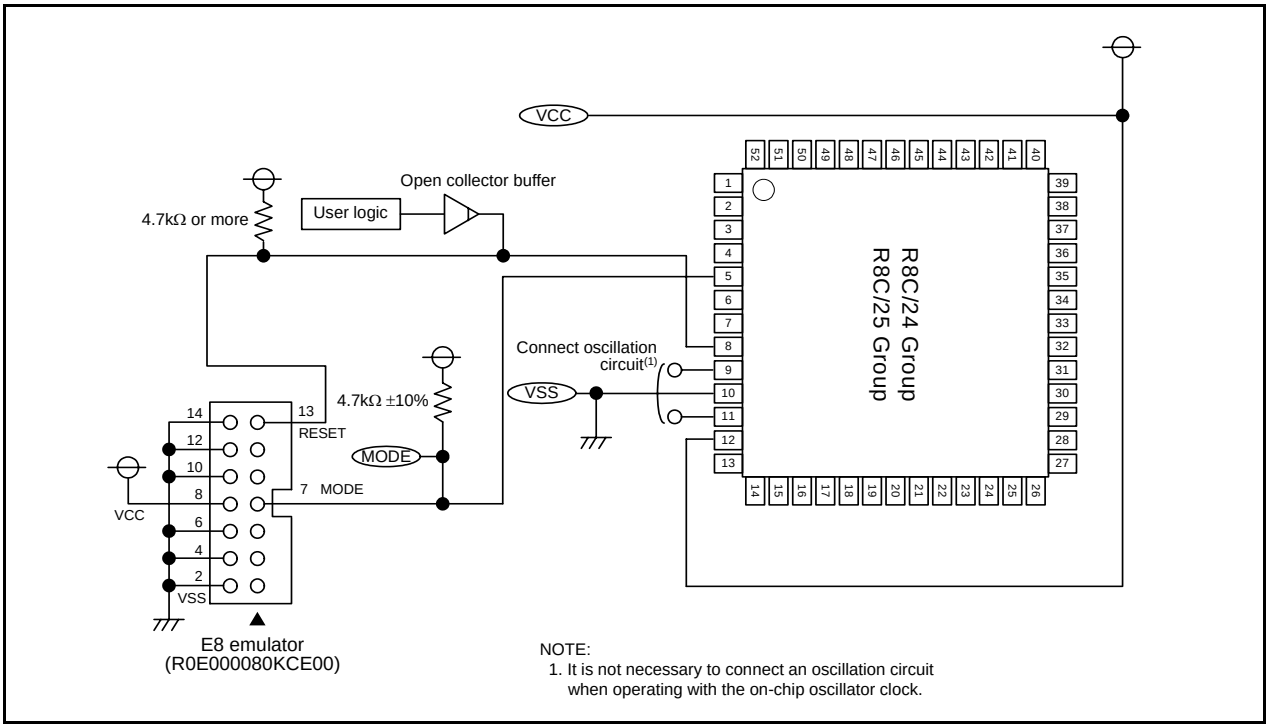
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.0	—
E	—	6.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10

Appendix 2. Connection Examples between Serial Writer and On-Chip Debugging Emulator

Appendix Figure 2.1 shows a Connection Example with M16C Flash Starter (M3A-0806), and Appendix Figure 2.2 shows a Connection Example with E8 Emulator (R0E000080KCE00).



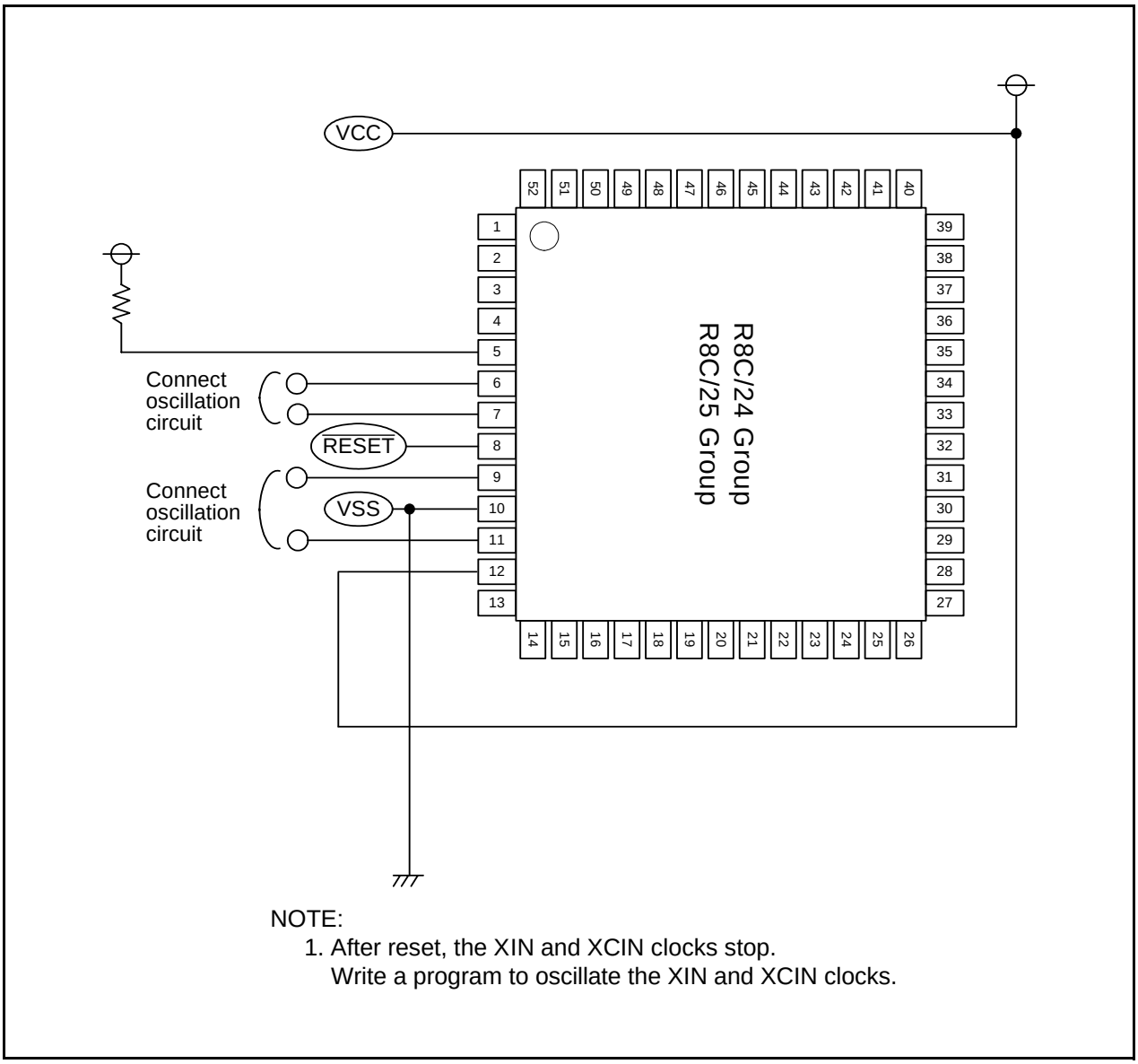
Appendix Figure 2.1 Connection Example with M16C Flash Starter (M3A-0806)



Appendix Figure 2.2 Connection Example with E8 Emulator (R0E000080KCE00)

Appendix 3. Example of Oscillation Evaluation Circuit

Appendix Figure 3.1 shows an Example of Oscillation Evaluation Circuit.



NOTE:
1. After reset, the XIN and XCIN clocks stop.
   Write a program to oscillate the XIN and XCIN clocks.

Appendix Figure 3.1 Example of Oscillation Evaluation Circuit

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Rev.	Date	Description	
		Page	Summary
0.10	Jul 27, 2005	–	First Edition issued
0.20	Jan 16, 2006	all pages	• “Preliminary” deleted • Symbol name “TRDMDR” → “TRDMR”, “SSUAIC” → “SSUIC”, “IIC2AIC” → “IICIC”, and “TSTOP0, TSTOP1” → “CSEL0, CSEL1” revised • Pin name “TCLK” → “TRDCLK” revised • Bit name “TPSC0 to TPSC2” → “TCK0 to TCK2”, “TRD0 count stop bit” → “TRD0 count operation select bit”, and “TRD1 count stop bit” → “TRD1 count operation select bit” revised
		2	Table 1.1 Functions and Specifications for R8C/24 Group revised
		3	Table 1.2 Functions and Specifications for R8C/25 Group revised
		4	Figure 1.1 Block Diagram; “Peripheral Functions” added, “System Clock Generation” → “System Clock Generator” revised
		5	Table 1.3 Product Information for R8C/24 Group revised
		6	Table 1.4 Product Information of R8C/25 Group revised
		7	Figure 1.4 Pin Assignment (Top View); “VSS” → “VSS/AVSS” and “VCC” → “VCC/AVCC” revised
		8	Table 1.5 Pin Functions; “Analog power supply input” added, “Reference voltage input” revised
		9	Table 1.6 Pin Name Information by Pin Number “VSS” → “VSS/AVSS” and “VCC” → “VCC/AVCC” revised
		10	Figure 2.1 CPU Registers; “Reserved Area” → “Reserved Bit” revised
		12	2.8.10 Reserved Area; “Reserved Area” → “Reserved bit” revised
		13	Figure 3.1 Memory Map of R8C/24 Group; “Program area” → “program ROM” revised
		14	3.2 R8C/25 Group, Figure 3.2 Memory Map of R8C/25 Group; “Data area” → “data flash”, “Program area” → “program ROM” revised
		15	Table 4.1 SFR Information(1); 0012h: “X0h” → “00h” 0016h: “X0h” → “00h” 0024h: “TBD” → “When shipping” NOTES 3 and 4 revised
		24	Figure 5.4 OFS Register; NOTE1 revised and NOTE3 added
		25	5.1.1 When Power Supply is Stable (2) revised 5.1.2 Power On (4) revised
		26	Figure 5.5 Example of Hardware Reset Circuit and Operation and Figure 5.6 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation revised

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Rev.	Date	Description	
		Page	Summary
0.20	Jan 16, 2006	27	5.2 Power-On Reset Function “When a capacitor is ... or more.” added Figure 5.7 Example of Power-On Reset Circuit and Operation revised
		28	5.4 Voltage Monitor 1 Reset; “When ... VCC pin drops the Vdet1 ...” → “When ... VCC pin reaches to the Vdet1 ...” revised
		30 to 67	“6. Programmable I/O Ports” → “6. Voltage Detection Circuit” and “7. Voltage Detection Circuit” → “7. Programmable I/O Ports” revised
		33	Figure 6.5 Registers VCA1 and VCA2; VCA2 register revised
		34	Figure 6.6 VW0C Register revised
		46	Figure 7.2 Configuration of Programmable I/O Ports (2) revised
		47	Figure 7.3 Configuration of Programmable I/O Ports (3) revised
		49	Figure 7.5 Configuration of Programmable I/O Ports (5) revised
		50	Figure 7.6 Configuration of Programmable I/O Ports (6) revised
		51	Figure 7.7 Configuration of Programmable I/O Ports (7) revised
		56 to 66	7.4 Port setting added; Table 7.4 Port P0_0/AN7 to Table 7.47 Port P6_7/$\overline{\text{INT3}}$/RXD1 added
		67	Table 7.48 Unassigned Pin Handling revised
		69	9. Bus revised; “However, only following SFRs are ... accessed at a time.” added Table 9.2 Bus Cycles by Access Space of the R8C/25 Group added, Table 9.3 Access Unit and Bus Operations; “SFR” → “SFR, data flash”, “ROM/RAM” → “ROM (program ROM), RAM” revised
		71	Figure 10.1 Clock Generation Circuit revised
		72	Figure 10.2 CM0 Register revised
		73	Figure 10.3 CM1 Register revised
		75	Figure 10.5 Registers FRA0 and FRA1; FRA0 register revised
		77	Figure 10.8 VCA2 Register added
		78	Figure 10.9 Examples of XIN Clock Connection Circuit revised
		79	10.2.2 High-Speed On-Chip Oscillator Clock; “To use the high-speed on-chip ... or more).” added
		80	10.3 XCIN Clock “To input an external clock ... pin open.” added
		81	10.4.2 CPU Clock “Use the XCIN clock while ... stabilizes.” added 10.4.3 Peripheral Function Clock (f1, f2, f4, f8, f32, fC4, and fC32); “Use fC4 and fC32 while the XCIN clock oscillation stabilizes.” added 10.4.5 fOCO40M; “fOCO40M can be ... supply voltage VCC = 3.0 to 5.5 V.” added 10.4.8 fOCO128 added
		82	Table 10.2 Settings and Modes of Clock Associated Bits revised

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		Page	Summary
0.20	Jan 16, 2006	83	10.5.1.2 Low-Speed Clock Mode; "In this mode, stopping the XIN clock ... the VCA20 bit." added 10.5.1.4 Low-Speed On-Chip Oscillator Mode; "In this mode, stopping the XIN clock ... the VCA20 bit." added
		84	Figure 10.11 Handling Procedure of Internal Power Low Consumption Enabled by VCA20 bit added
		88	Figure 10.12 State Transition in Power Control Mode revised
		89	10.6.1 How to Use Oscillation Stop Detection Function; "• This function cannot be... is 2 MHz or below. ..." → "• This function cannot be... is below 2 MHz. ..." revised
		92	10.7.1 Stop Mode and 10.7.2 Wait Mode → 10.7.1 Stop Mode and Wait Mode revised 10.7.3 Oscillation Stop Detection Function; "Since ... is 2 MHz or below, ..." → "Since ... is below 2 MHz. ..." revised "To use this MCU with supply voltage ... to the chip externally." added 10.7.4 fOCO40M added
		107	Figure 12.11 Interrupt Priority Level Judgement Circuit; NOTE2 deleted
		114	Figure 12.18 Registers AIER and RMAD0 to RMAD1; AIER and RMAD0 to RMAD1 register revised
		119	12.6.7 Entering Wait Mode after Oscillation Stop Detection Interrupt is Detected added
		121	Figure 13.2 Registers OFS and WDC; OFS register NOTE1 revised and NOTE3 added, and WDC register NOTE1 deleted
		126	Table 14.1 Functional Comparison of Timers; Input Pin: Timer RD "TRDCLK" added
		127	Figure 14.1 Block Diagram of Timer RA revised
		135	Table 14.3 Pulse Output Mode Specifications revised
		142	Table 14.6 Pulse Period Measurement Mode Specifications revised
		144	Figure 14.11 Operating Example of Pulse Period Measurement Mode revised
		146	Figure 14.12 Block Diagram of Timer RB revised
		147	Figure 14.13 Registers TRBCR and TRBOCR; TRBOCR register revised
		149	Figure 14.15 Registers TRBPRE, TRBSC, and TRBPR; TRBPR register revised
		158	Figure 14.20 TRBIOC Register in Programmable One-Shot Generation Mode Figure 14.23 Registers TRBIOC and TRBMR in Programmable One-Shot Generation Mode; TRBIOC register NOTE2 revised
		162	Figure 14.25 Registers TRBIOC and TRBMR in Programmable Wait One-Shot Generation Mode; TRBIOC register NOTE2 revised
		165	-Output compare function; "(Pin output can be changed at detection)" added

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0.20	Jan 16, 2006	166 to 168	Tables 14.12 Pin Functions TRDIOA0/TRDCLK(P2_0) Tables 14.13 Pin Functions TRDIOB0(P2_1) Tables 14.14 Pin Functions TRDIOC0(P2_2) Tables 14.15 Pin Functions TRDIOD0(P2_3) Tables 14.16 Pin Functions TRDIOA1(P2_4) Tables 14.17 Pin Functions TRDIOB1(P2_5) Tables 14.18 Pin Functions TRDIOC1(P2_6) Tables 14.19 Pin Functions TRDIOD1(P2_7) Tables 14.20 Pin Functions INT0(P4_5) added
		170	14.3.1 Mode Selection deleted
		170	Table 14.21 Count Source Selection revised 14.3.1 Count Sources; “TRDCRi register to ...” → “TRDCRi register (i = 0 or 1) to ...” revised
		171	Figure14.29 Buffer Operation in Input Capture Function revised
		172	Figure14.30 Buffer Operation in Output Capture Function revised 14.3.2 Buffer Operation; “input capture and ...” → “timer mode (input capture and ...” “the IOC2 to IOC0 bits in ...” → “the IOC2 bit in ...” “the IOA2 to IOA0 bits in ...” → “the IOA2 bit in ...” “the IOD2 to IOD0 bits in ...” → “the IOD2 bit in ...” “the IOB2 to IOC0 bits in ...” → “the IOB2 bit in ...” revised “Bits IMFC and IMFD in the TRDSRi...input capture function.” added
		173	14.3.3 Synchronous Operation; “For the synchronous operation, ... register = 110b).” deleted
		174	14.3.4 Pulse Output Forced Cutoff; “P2D” → “PD2”, “P4D” → “PD4”, and “P4_5” → “PD4_5”, revised “According to the selection ... details of interrupts.” added
		176	14.3.5 Input Capture Function; “The TRDGRA0 register can also ... trigger input.” added Figure 14.33 Block Diagram of Input Capture Function revised
		177	Table 14.23 Specifications of Input Capture Function revised
		178	Figure 14.34 Registers TRDSTR and TRDMR in Input Capture Function revised
		179	Figure 14.35 TRDPMR Register in Input Capture Function revised
		180	Figure 14.36 TRDFCR Register in Input Capture Function revised
		183	Figure 14.39 Registers TRDIORA0 to TRDIORA1 in Input Capture Function revised
		184	Figure 14.40 Registers TRDIORC0 to TRDIORC1 in Input Capture Function revised
		185	Figure 14.41 Registers TRDSR0 to TRDSR1 in Input Capture Function revised
		187	Table 14.25 Input Pin Function in Input Capture Function deleted
		189	14.3.5.1 Digital Filter; “TRDDF register ...” → “TRDDFi register ...” revised

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0.20	Jan 16, 2006	192	Figure 14.48 Registers TRDSTR and TRDMR in Output Compare Function revised
		193	Figure 14.49 TRDPMR Register in Output Compare Function revised
		194	Figure 14.50 TRDFCR Register in Output Compare Function revised
		195	Figure 14.51 Registers TRDOER1 to TRDOER2 in Output Compare Function; TRDOER2 register: NOTE1 added
		198	Figure 14.54 Registers TRDIORA0 to TRDIORA1 in Output Compare Function revised
		199	Figure 14.55 Registers TRDIORC0 to TRDIORC1 in Output Compare Function revised
		200	Figure 14.56 Registers TRDSR0 to TRDSR1 in Output Compare Function revised
		209	Figure 14.64 Registers TRDSTR and TRDMR in PWM Mode revised
		210	Figure 14.65 TRDPMR Register in PWM Mode revised
		211	Figure 14.66 TRDFCR Register in PWM Mode revised
		212	Figure 14.67 Registers TRDOER1 to TRDOER2 in PWM Mode; TRDOER2 register: NOTE1 added
		214	Figure 14.69 Registers TRDSR0 to TRDSR1 in PWM Mode revised
		222	Figure 14.77 Registers TRDSTR to TRDMR in Reset Synchronous PWM Mode revised
		223	Figure 14.78 TRDFCR Register in Reset Synchronous PWM Mode revised
		224	Figure 14.79 Registers TRDOER1 to TRDOER2 in Reset Synchronous PWM Mode; TRDOER2 register: NOTE1 added
		226	Figure 14.81 Registers TRDSR0 to TRDSR1 in Reset Synchronous PWM Mode revised
		232	Figure 14.87 TRDSTR Register in Complementary PWM Mode revised
		233	Figure 14.88 TRDMR Register in Complementary PWM Mode revised
		234	Figure 14.89 TRDFCR Register in Complementary PWM Mode revised
		235	Figure 14.90 Registers TRDOER1 to TRDOER2 in Complementary PWM Mode; TRDOER2 register: NOTE1 added
		237	Figure 14.92 Registers TRDSR0 to TRDSR1 in Complementary PWM Mode revised
		244	Figure 14.98 Block Diagram of PWM3 Mode revised
		245	Table 14.33 Specifications of PWM3 Mode revised
		246	Figure 14.99 TRDSTR Register in PWM3 Mode revised
		247	Figure 14.100 TRDMR Register in PWM3 Mode revised
		248	Figure 14.101 TRDFCR Register in PWM3 Mode revised

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0.20	Jan 16, 2006	249	Figure 14.102 Registers TRDOER1 to TRDOER2 in PWM3 Mode; TRDOER2 register: NOTE1 added
		251	Figure 14.104 TRDCR0 Register in PWM3 Mode NOTE1 deleted
		252	Figure 14.105 TRDSR0 Register in PWM3 Mode revised
		253	Figure 14.106 TRDIER0 Register in PWM3 Mode revised
		255	Table 14.34 TRDGRji Register Functions in PWM3 Mode revised
		256	Figure 14.109 Operating Example of PWM3 Mode revised
		259	14.3.12.1 TRDSTR Register (i = 0 or 1) added
		260	14.3.12.4 “Count Clock Source Switch” → “Count Source Switch” revised
		264	14.3.12.9 Count Source fOCO40M added
		275	Table 14.39 Output Compare Mode Specifications revised
		281	Figure 14.132 Setting Example in Real-Time Clock Mode revised
		285	Figure 15.3 Registers U0TB to U1TB and U0RB to U1RB revised
		286	Figure 15.4 Registers U0BRG to U1BRG and U0MR to U1MR; U0BRG to U1BRG register revised
		287	Figure 15.5 Registers U0C0 to U1C0 NOTE1 added
		295	Table 15.5 Registers Used and Settings for UART Mode; UiBRG: “–” → “0 to 7” revised
		300	Table 16.1 Mode Selections revised
		358	Figure 16.46 Example of Register Setting in Master Transmit Mode (Clock Synchronous Serial Mode); “• Set the IICSEL bit in the PMR register to 1” added
		377	Table 18.1 Performance of A/D converter revised
		378	Figure 18.1 Block Diagram of A/D Converter; “VSS” → “AVSS” and “Vref” → “Vcom” revised
		387 to 389	18.4 A/D Conversion Cycles to 18.6 Inflow Current Bypass Circuit added
		390	18.7 Notes on A/D Converter “• Connect 0.1μF capacitor ... VSS pin.” → “• Connect 0.1μF capacitor ... AVSS pin.” revised
		391	Table 19.1 Flash Memory Version Performance; • Program and Erase Endurance:(Program area) → (Program ROM), (Data area) → (Data flash) revised • NOTE3 added
		392	19.2 Memory Map; “The user ROM ... area ... Block A and B.” → “The user ROM ... area (program ROM) ... Block A and B (data flash).” revised Figure 19.1 Flash Memory Block Diagram for R8C/24 Group revised
		393	Figure 19.2 Flash Memory Block Diagram for R8C/25 Group revised
		395	Figure 19.4 OFS Register; NOTE1 revised and NOTE3 added
		398	19.4.2.4 FMSTP Bit revised

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0.20	Jan 16, 2006	399	19.4.2.16 FMR47 Bit revised
		402	Figure 19.7 FMR4 Register NOTE4 revised
		405	Figure 19.11 Process to Reduce Power Consumption in High-Speed On-Chip Oscillator Mode, Low-Speed On-Chip Oscillator Mode (XIN Clock Stops) and Low-Speed Clock Mode (XIN Clock Stops) revised
		408	19.4.3.5 Block Erase; "The block erase command cannot be ... program-suspend." added
		409	Figure 19.14 Block Erase Command (When Using Erase-Suspend Function) revised
		412	Figure 19.15 Full Status Check and Handling Procedure for Individual Errors revised
		414	Figure 19.16 Pin Connections for Standard Serial I/O Mode revised
		419	19.7.1.9 Program and Erase Voltage for Flash Memory added
		420	Table 20.1 Absolute Maximum Ratings; "VCC" →"VCC/AVCC" revised Table 20.2 Recommended Operating Conditions revised
		421	Table 20.3 A/D Converter Characteristics revised
		422	Table 20.4 Flash Memory (Program ROM) Electrical Characteristics revised
		423	Table 20.5 Flash Memory (Data flash Block A, Block B) Electrical revised
		424	Table 20.6 Voltage Detection 0 Circuit Electrical Characteristics revised Table 20.7 Voltage Detection 1 Circuit Electrical Characteristics revised Table 20.8 Voltage Detection 2 Circuit Electrical Characteristics revised
		425	Table 20.9 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 0 Reset) NOTE2 revised
		426	Table 20.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 20.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 20.13 Power Supply Circuit Timing Characteristics revised
		427	Table 20.14 Timing Requirements of Clock Synchronous Serial I/O with Chip Select revised
		431	Table 20.15 Timing Requirements of I^2C bus Interface NOTE1 revised
		432	Table 20.16 Electrical Characteristics (1) [VCC = 5 V] revised
		433	Table 20.17 Electrical Characteristics (2) [VCC = 5 V] revised
		434	Table 20.18 XIN Input, XCIN Input revised
		435	Table 20.20 Serial Interface revised
		436	Table 20.22 Electrical Characteristics (3) [VCC = 3 V] revised
		437	Table 20.23 Electrical Characteristics (4) [Vcc = 3 V] revised
		438	Table 20.24 XIN Input, XCIN Input revised
		439	Table 20.26 Serial Interface revised
		440	Table 20.28 Electrical Characteristics (5) [VCC = 2.2 V] revised

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0.20	Jan 16, 2006	441	Table 20.29 Electrical Characteristics (6) [Vcc = 2.2 V] revised
		442	Table 20.30 XIN Input, XCIN Input revised Table 20.31 TRAIO Input, INT1 Input revised
		443	Table 20.32 Serial Interface revised Table 20.33 External Interrupt INTi (i = 0, 2, 3) Input
		444	21.1.1 Stop Mode and 21.1.2 Wait Mode → 21.1.1 Stop Mode and Wait Mode revised 21.1.3 Oscillation Stop Detection Function; "Since ... is 2 MHz or below, ..." → "Since ... is below 2 MHz. ..." revised "To use this MCU with supply voltage ... to the chip externally." added 21.1.4 fOCO40M added
		447	21.2.7 Entering Wait Mode after Oscillation Stop Detection Interrupt is Detected added
		462	21.7 Notes on A/D Converter "• Connect 0.1μF capacitor ... VSS pin." → "• Connect 0.1μF capacitor ... AVSS pin." revised
		465	21.8.1.9 Program and Erase Voltage for Flash Memory added
		467	22. Notes for On-Chip Debugger; (1) and (6) added, "(2) Do not use addresses ... addresses." deleted
		468	Appendix 1. Package Dimensions; "TBD" → "PLQP0052JA-A (52P6A-A)" added
		469	Appendix Figure 2.1 Connection Example with M16C Flash Starter (M3A-0806) revised Appendix Figure 2.2 Connection Example with E8 Emulator (R0E000080KCE00) revised
		470	Appendix Figure 3.1 Example of Oscillation Evaluation Circuit revised
1.00	May 31, 2006	all pages	"Under development" deleted
		3	Table 1.2 Functions and Specifications for R8C/25 Group revised
		4	Figure 1.1 Block Diagram; "System clock generator" → "System clock generation circuit" revised
		5 to 6	Table 1.3 Product Information for R8C/24 Group and Table 1.4 Product Information for R8C/25 Group; A part of (D) mark is deleted.
		9	Table 1.6 Pin Name Information by Pin Number NOTE1 added
		15	Table 4.1 SFR Information(1); 001Ch: "00h" → "00h, 10000000b" revised 0029h: High-Speed On-Chip Oscillator Control Register 4 FRA4 When shipping added 002Bh: High-Speed On-Chip Oscillator Control Register 6 FRA6 When shipping added NOTE6 added
		19	Table 4.5 SFR Information(5); 0118h: Timer RE Second Data Register / Counter Data Register, 0119h: Timer RE Minute Data Register / Compare Data Register register name revised

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1.00	May 31, 2006	20	Table 4.6 SFR Information(6); 0143h: “11000000b” → “11100000b” revised
		24	Figure 5.4 OFS Register NOTE2 revised
		25	5.1.1 When Power Supply is Stable (2) revised 5.1.2 Power On (4) revised
		26	Figure 5.5 Example of Hardware Reset Circuit and Operation and Figure 5.6 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation revised
		27	Figure 5.7 Example of Power-On Reset Circuit and Operation revised
		28	5.3 Voltage Monitor 0 Reset revised
		33	Figure 6.5 Registers VCA1 and VCA2; VCA2 register NOTE6 revised
		45 to 51	Figures 7.1 to .7.7 Configuration of Programmable I/O Ports NOTE1 added
		53	Figure 7.9 PDi (i = 0 to 4 and 6) Registers NOTE3 added
		54	Figure 7.11 Registers PUR0 and PUR1; After Reset revised
		62	Table 7.31 Port P3_4/SDA/$\overline{\text{SCS}}$ revised
		70	Table 10.1 Specifications of Clock Generation Circuit revised
		71	Figure 10.1 Clock Generation Circuit revised
		72	Figure 10.2 CM0 Register; NOTE6 deleted and NOTE9 revised
		74	Figure 10.4 OCD Register revised
		75	Figure 10.5 Registers FRA0 and FRA1; FRA0 register NOTE2 revised
		76	Figure 10.6 Registers FRA2, FRA4, and FRA6; FRA2 register NOTE2 deleted, registers FRA4 and FRA6 added
		77	Figure 10.8 VCA2 Register NOTE6 revised
		78	Figure 10.9 Examples of XIN Clock Connection Circuit NOTE1 revised
		79	10.2.2 High-Speed On-Chip Oscillator Clock revised
		81	10.4.3 Peripheral Function Clock (f1, f2, f4, f8, and f32) revised
		82	10.4.9 fC4 and fC32 added
		83	Table 10.2 Settings and Modes of Clock Associated Bits revised
		84	10.5.1.2 Low-Speed Clock Mode revised
		85	10.5.2.2 Entering Wait Mode and 10.5.2.3 Pin Status in Wait Mode revised
		86	10.5.2.4 Exiting Wait Mode; “When using a peripheral ...instruction is executed.” page changed Table 10.3 Interrupts to Exit Wait Mode and Usage Conditions revised
		87	10.5.2.4 Exiting Wait Mode; “When exiting by a peripheral ... CPU clock supply is started.” → “When exiting by a peripheral ... CM07 bit in the CM0 register.” revised Figure 10.11 Time between Wait Mode and Interrupt Routine Execution added
		88	10.5.2.5 Reducing the Internal Power Consumption added Figure 10.12 Handling Procedure of Internal Power Low Consumption Enabled by VCA20 bit revised

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1.00	May 31, 2006	89	Table 10.4 Interrupts to Exit Stop Mode and Usage Conditions revised
		90	Figure 10.13 Time between Stop Mode and Interrupt Routine Execution added
		92	10.6.1 How to Use Oscillation Stop Detection Function revised
		93	Figure 10.15 Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock revised
		94	Figure 10.16 Example of Determining Interrupt Source for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt revised
		95	10.7.1 Stop Mode and Wait Mode revised and 10.7.4 fOCO40M deleted
		97	Figure 12.1 Interrupts revised
		107	Table 12.5 IPL Value When Software or Special Interrupt Is Acknowledged revised
		109	Figure 12.10 Priority Levels of Hardware Interrupts revised
		122	12.6.7 Entering Wait Mode after Oscillation Stop Detection Interrupt is Detected deleted
		123	Figure 13.1 Block Diagram of Watchdog Timer revised
		124	Figure 13.2 Registers OFS and WDC; OFS Register NOTE2 revised
		128	14. Timers; “The count source for each timer ... and reloading.” deleted
		130	14.1 Timer RA; “The count source for timer RA ... and reloading.” added Figure 14.1 Block Diagram of Timer RA revised
		131	Figure 14.2 Registers TRACR and TRAIOC revised
		132	Figure 14.3 Registers TRAMR, TRAPRE, and TRA revised
		133	Table 14.2 Timer Mode Specifications revised Figure 14.4 TRAIOC Register in Timer Mode revised (Figure 14.4 TRACR Register in Timer Mode deleted, Figure 14.5 Registers TRAIOC and TRAMR in Timer Mode TRAMR register deleted)
		134	14.1.1.1 Timer Write Control during Count added Figure 14.5 Operating Example of Timer RA when Count Value is Rewritten during Count added
		135	Table 14.3 Pulse Output Mode Specifications revised
		136	Figure 14.6 TRAIOC Register in Pulse Output Mode revised (Figure 14.6 Registers TRACR and TRAIOC in Pulse Output Mode TRACR register deleted, Figure 14.7 TRAMR Register in Pulse Output Mode deleted)
		137	Table 14.4 Event Counter Mode Specifications revised
		138	Figure 14.7 TRAIOC Register in Event Counter Mode revised (Figure 14.8 Registers TRACR and TRAIOC in Event Counter Mode TRACR register deleted, Figure 14.9 TRAMR Register in Event Counter Mode deleted)
		139	Table 14.5 Pulse Width Measurement Mode Specifications revised

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1.00	May 31, 2006	140	Figure 14.8 TRAIOC Register in Pulse Width Measurement Mode revised (Figure 14.10 Registers TRACR and TRAIOC in Pulse Width Measurement Mode TRACR register deleted, Figure 14.11 TRAMR Register in Pulse Width Measurement Mode deleted)
		141	Figure 14.9 Operating Example of Pulse Width Measurement Mode revised
		142	Table 14.6 Pulse Period Measurement Mode Specifications revised
		143	Figure 14.10 TRAIOC Register in Pulse Period Measurement Mode revised (Figure 14.13 Registers TRACR and TRAIOC in Pulse Period Measurement Mode TRACR register deleted, Figure 14.14 TRAMR Register in Pulse Period Measurement Mode deleted)
		144	Figure 14.11 Operating Example of Pulse Period Measurement Mode revised
		146	14.2 Timer RB; “The count source for timer RB ... and reloading.” added • Timer mode: ... (peripheral function clock ... added Figure 14.12 Block Diagram of Timer RB revised
		147	Figure 14.13 Registers TRBCR and TRBOCR revised
		148	Figure 14.14 Registers TRBIOC and TRBMR revised
		149	Figure 14.15 Registers TRBPRE, TRBSC, and TRBPR revised
		150	Table 14.7 Timer Mode Specifications revised Figure 14.16 TRBIOC Register in Timer Mode revised (Figure 14.20 Registers TRBIOC and TRBMR in Timer Mode TRBMR register deleted)
		151	14.2.1.1 Timer Write Control during Count added
		152	Figure 14.17 Operating Example of Timer RB when Count Value is Rewritten during Count added
		153	Table 14.8 Programmable Waveform Generation Mode Specifications revised
		154	Figure 14.18 TRBIOC Register in Programmable Waveform Generation Mode revised (Figure 14.20 Registers TRBIOC and TRBMR in Timer Mode TRBMR register deleted) Figure 14.19 Operating Example of Timer RB in Programmable Waveform Generation Mode revised
		155	Table 14.9 Programmable One-Shot Generation Mode Specifications revised
		156	Figure 14.20 TRBIOC Register in Programmable One-Shot Generation Mode revised (Figure 14.23 Registers TRBIOC and TRBMR in Programmable One-Shot Generation Mode TRBMR register deleted)
		157	Figure 14.21 Operating Example of Programmable One-Shot Generation Mode revised
		158	14.2.3.1 Selecting One-shot Trigger added
		159	Table 14.10 Programmable Wait One-Shot Generation Mode Specifications revised

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1.00	May 31, 2006	161	Figure 14.22 TRBIOC Register in Programmable Wait One-Shot Generation Mode (Figure 14.25 Registers TRBIOC and TRBMR in Programmable Wait One-Shot Generation Mode TRBMR register deleted)
		162	Figure 14.23 Operating Example of Programmable Wait One-Shot Generation Mode revised
		163	14.2.5 Notes on Timer RB; "• ... Timer RB starts counting at the first ... 1 (during count)." deleted "• When the TSTOP bit in the TRBCR register ... immediately stops. • If the TOSST bit or the TOSSP bit ... also be set to 0 or 1." added
		165	Table 14.12 Pin Functions TRDIOA0/TRDCLK(P2_0) revised
		167	Table 14.20 Pin Functions $\overline{\text{INT0}}$(P4_5) revised
		179	Figure 14.33 TRDFCR Register in Input Capture Function NOTE2 revised
		193	Figure 14.47 TRDFCR Register in Output Compare Function NOTE2 revised
		210	Figure 14.63 TRDFCR Register in PWM Mode NOTE2 revised
		220	Table 14.29 Reset Synchronous PWM Mode Specifications revised
		222	Figure 14.75 TRDFCR Register in Reset Synchronous PWM Mode NOTES 1 and 3 revised
		225	Figure 14.78 Registers TRDSR0 to TRDSR1 in Reset Synchronous PWM Mode revised
		227	Table 14.30 TRDGRji Register Functions in Reset Synchronous PWM Mode revised
		233	Figure 14.86 TRDFCR Register in Complementary PWM Mode NOTES 1 and 4 revised
		239	14.3.9 Complementary PWM Mode; "Since a value cannot be written to ... BFC1, and BFD1." added
		244	Table 14.33 Specifications of PWM3 Mode revised
		247	Figure 14.98 TRDFCR Register in PWM3 Mode NOTE2 revised
		254	Table 14.34 TRDGRji Register Functions in PWM3 Mode revised, 14.3.10 PWM3 Mode; "Registers TRDGRC0, ... and BFD1." added
		258	14.3.12.1 TRDSTR Register (i = 0 or 1); "• Table 14.36 lists the TRDIOji (j = A, B, C, ... timer RD output." added
		259	14.3.12.6 Reset Synchronous PWM Mode; Change procedure (2) revised 14.3.12.7 Complementary PWM Mode; •Change bits CMD1 to CMD0 in the TRDFCR register in the ... ; Change procedure: When setting to complementary ... (2) , Change procedure: When stopping complementary ... (1) and (2) revised •Do not write to ... ; "However, set to the TRDGRD0, ... BFD1." added
		263	14.3.12.8 PWM3 Mode deleted
		264	14.4 Timer RE; "The count source for timer RE ... operations." added
		265	Figure 14.112 Block Diagram of Real-Time Clock Mode revised

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1.00	May 31, 2006	287	Figure 15.6 Registers U0C1 to U1C1, U1SR, and PMR; U0C1 to U1C1 register NOTE2 added
		288	Table 15.1 Clock Synchronous Serial I/O Mode Specifications revised
		289	15.1 Clock Synchronous Serial I/O Mode; "Table 15.3 ... The TXD0 pin ..." → "Table 15.3 ... The TXDi pin ..." revised
		294	15.2 Clock Asynchronous Serial I/O (UART) Mode; "Table 15.6 ... The TXD0 pin ..." → "Table 15.6 ... The TXDi pin ..." revised
		296	Figure 15.11 Receive Timing Example in UART Mode; "RI bit" → "IR bit" revised
		300	Table 16.2 Clock Synchronous Serial I/O with Chip Select Specifications; "ϕ" → "f1" revised and NOTE2 deleted
		304	Figure 16.4 SSMR Register
		307	Figure 16.7 SSMR2 Register revised
		308	Figure 16.8 Registers SSTDR and SSRDR; SSTDR registers NOTE1 deleted
		309	16.2.1 Transfer Clock; "ϕ" → "f1" revised
		314	16.2.5.2 Data Transmission; "When setting the MCU is set as a slave device, ... enabled." deleted
		316	Figure 16.14 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode) NOTE2 deleted
		319	16.2.5.4 Data Transmission/Reception; "When the MCU is set as the slave device, ... enabled." deleted
		320	Figure 16.17 Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode) NOTE2 deleted
		322	Figure 16.18 Initialization in 4-Wire Bus Communication Mode revised
		323	16.2.6.2 Data Transmission; "When the MCU is set as a slave device, ... enabled." deleted
		358	Figure 16.47 Example of Register Setting in Master Receive Mode (I^2C bus Interface Mode) revised
		362 to 375	17. Hardware LIN; "Sync Break" → "Synch Break" and "Sync Field" → "Synch Field" revised
		362	Figure 17.1 Block Diagram of Hardware LIN revised
		364	Figure 17.2 LINCR Register revised
		365	Figure 17.3 LINST Register revised
		366	Figure 17.4 Typical Operation when Sending a Header Field "RAIC" → "TRAIC" revised
		367	Figure 17.5 Example of Header Field Transmission Flowchart (1) revised
		368	Figure 17.6 Example of Header Field Transmission Flowchart (2) revised
		369	17.4.2 Slave Mode (5) revised Figure 17.7 Typical Operation when Receiving a Header Field revised
		370	Figure 17.8 Example of Header Field Reception Flowchart (1) revised
		371	Figure 17.9 Example of Header Field Reception Flowchart (2) revised

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1.00	May 31, 2006	372	Figure 17.10 Example of Header Field Reception Flowchart (3) revised
		373	Figure 17.11 Typical Operation when a Bus Collision is Detected; "RAIC" → "TRAIC" revised
		374	17.5 Interrupt Requests; "There are four ... Sync Break generation completed, ... , and bus collision detection." → "There are three ... , and bus collision detection." revised Table 17.2 Interrupt Requests of Hardware LIN revised
		376	Table 18.1 Performance of A/D converter revised
		380	Table 18.2 One-Shot Mode Specifications revised
		384	Figure 18.6 ADCON0 Register in Repeat Mode revised
		386	18.3 Sample and Hold; "... to 28 ϕAD cycles for 8-bit resolution or 33 ϕAD resolution" and "When performing A/D conversion, charge the sampling time." deleted
		387	Figure 18.10 Internal Equivalent Circuit of Analog Input revised
		388	18.6 Inflow Current Bypass Circuit deleted 18.6 Output Impedance of Sensor under A/D Conversion added
		389	18.7 Notes on A/D Converter revised
		394	Figure 19.4 OFS Register NOTE2 revised
		395	Table 19.3 Differences between EW0 Mode and EW1 Mode revised
		397	19.4.2.1 FMR00 Bit "... (including suspend periods) ..." added
		399	Figure 19.5 FMR0 Register NOTE6 added
		401	Figure 19.7 FMR4 Register; NOTES 2, 3 and 4 revised and NOTE5 added
		402	Figure 19.8 Timing of Suspend Operation revised
		405	19.4.3.1 Read Array Command "The MCU also enters read array mode after a reset." added 19.4.3.2 Read Status Register Command "The MCU remains in read status mode ... command is written." added
		406	19.4.3.4 Program Command; "When suspend function disabled, ...", "When suspend function enabled, the FMR44 bit ... when auto-programming completes." added Figure 19.12 Program Command (When Suspend Function Disabled) title revised
		407	Figure 19.13 Program Command (When Suspend Function Enabled) added
		408	19.4.3.5 Block Erase revised Figure 19.14 Block Erase Command (When Erase-Suspend Function Disabled) title revised
		409	Figure 19.15 Block Erase Command (When Erase-Suspend Function Enabled) revised
		410	Table 19.5 Status Register Bits revised
		413	19.5 Standard Serial I/O Mode revised Table 19.7 Pin Functions (Flash Memory Standard Serial I/O Mode 2) added
		414	Table 19.8 Pin Functions (Flash Memory Standard Serial I/O Mode 3) revised

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1.00	May 31, 2006	415	Figure 19.17 Pin Connections for Standard Serial I/O Mode 3 title revised
		416	Figure 19.18 Pin Processing in Standard Serial I/O Mode 2 added, Figure 19.19 Pin Processing in Standard Serial I/O Mode 3 title revised
		420	19.7.1.7 Reset Flash Memory deleted
		421	Table 20.2 Recommended Operating Conditions revised
		422	Figure 20.1 Ports P0 to P4, P6 Timing Measurement Circuit; title revised
		423	Table 20.4 Flash Memory (Program ROM) Electrical Characteristics revised
		424	Table 20.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics revised
		425	Figure 20.2 Time delay until Suspend title revised
		426	Table 20.9 Voltage Monitor 0 Reset Electrical Characteristics → Table 20.9 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics revised Table 20.10 Power-on Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 0 Reset) deleted Figure 20.3 Power-on Reset Circuit Electrical Characteristics revised
		427	Table 20.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics revised Table 20.11 Low-speed On-Chip Oscillator Circuit Electrical Characteristics revised
		434	Table 20.16 Electrical Characteristics (2) [Vcc = 5 V] revised
		438	Table 20.22 Electrical Characteristics (4) [Vcc = 3 V] revised
		442	Table 20.28 Electrical Characteristics (6) [Vcc = 2.2 V] revised
		445	21.1.1 Stop Mode and Wait Mode revised and 21.1.4 fOCO40M deleted
		448	21.2.7 Entering Wait Mode after Oscillation Stop Detection Interrupt is Detected deleted
		450	21.3.2 Notes on Timer RB; "• ... Timer RB starts counting at the first ... 1 (during count)." deleted "• When the TSTOP bit in the TRBCR register ... immediately stops. • If the TOSST bit or the TOSSP bit ... also be set to 0 or 1." added
		451	21.3.3.1 TRDSTR Register (i = 0 or 1) revised
		452	21.3.3.6 Reset Synchronous PWM Mode; Change procedure (2) revised 21.3.3.7 Complementary PWM Mode; •Change bits CMD1 to CMD0 in the TRDFCR register in the ...; Change procedure: When setting to complementary ... (2) , Change procedure: When stopping complementary ... (1) and (2) revised •Do not write to ...; "However, set to the TRDGRD0, ... BFD1." added
		456	21.3.3.8 PWM3 Mode deleted
		462	21.6 Notes on Hardware LIN; "Sync Break" → "Synch Break" revised
		463	21.7 Notes on A/D Converter revised
		466	21.8.1.7 Reset Flash Memory deleted

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		Page	Summary
1.00	May 31, 2006	468	22. Notes on On-Chip Debugger; (2) revised
		469	Appendix 1. Package Dimensions "The latest package ... Renesas Technology website." added
2.00	Nov 01, 2006	all pages	"PTLG0064JA-A (64F0G)" package added Y version added Factory programming product added
		1	1. Overview; "... or a 64-pin molded-plastic FLGA." added
		2, 3	Table 1.1 Functions and Specifications for R8C/24 Group, Table 1.2 Functions and Specifications for R8C/25 Group; Package: "64-pin molded-plastic FLGA" added
		9	Figure 1.4 PLQP0052JA-A Package Pin Assignments (Top View); NOTE3 revised
		10	Figure 1.5 PTLG0064JA-A Package Pin Assignments added
		18	Table 4.1 revised
		36	Figure 6.5 NOTE6 revised
		61	Table 7.17 revised
		62	Table 7.19 revised
		66	Table 7.33, Table 7.35 revised
		67	Table 7.36 revised
		78	Figure 10.5 NOTE2 added
		80	Figure 10.8 NOTE6 revised
		81	Figure 10.9 revised
		82	10.2.2 "Adjust the FRA1 register so that .... 40 MHz or less." added
		90	Figure 10.11 revised
		91	Figure 10.12 revised
		93	Figure 10.13 revised
		98	10.7.1 revised, 10.7.2 added
		123	12.6.3 "and Table 20.18 (VCC = 5V), ... TRAIO Input, INT1 Input." deleted
		127	Figure 13.2; Watchdog Timer Control Register: After Reset "When read, the content is undefined." added
		140	Table 14.4; TRAO pin function: Specification "or pulse output" added
		198	Figure 14.49 NOTE2 added
		215	Figure 14.65 Timer RD Output Control Register NOTE2 added
		220	Figure 14.71 revised
		252	Figure 14.100 NOTE2 added
		262	14.3.12.7 "Do not use the TRDGRC0 register in complementary PWM mode." deleted
		291	Table 15.1 NOTE2 revised
		296	Table 15.4 NOTE1 revised

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2.00	Nov 01, 2006	298	Figure 15.10 revised
		306	Figure 16.3 NOTE2 revised
		337	Figure 16.26 NOTE3 revised
		344 to 349	Figure 16.32, Figure 16.33, Figure 16.34, Figure 16.35, Figure 16.36 revised
		370	Figure 17.5 revised
		374	Figure 17.9 revised
		375	Figure 17.10 revised
		377	17.4.4 added
		378	Table 17.2 Cause of Interrupt “8” → “6”
		384	Table 18.2; Stop condition: Specification “when the ADCAP .... (software trigger)” added, Input pin: Specification “AN8” → “AN0”
		395	Figure 19.1 revised
		396	Figure 19.2 revised
		411	Figure 19.13 NOTE3 added
		413	Figure 19.15 NOTE3 added
		416	Figure 19.16 revised
		425	Table 20.1 Absolute Maximum Ratings; NOTE1 added
		432	Table 20.10; “V_{CC} = 4.5 V to 5.5 V -20°C ≤ Topr ≤ 85°C”, “V_{CC} = 4.5 V to 5.5 V -40°C ≤ Topr ≤ 85°C” added Oscillation stability time: Condition “V_{CC} = 5.0 V, Topr = 25°C” deleted Table 5.11; Oscillation stability time: Condition “V_{CC} = 5.0 V, Topr = 25°C” deleted
		438	Table 20.15; I_{IH}, I_{IL}, R_{PULLUP} Condition: “Vcc = 5V” added
		439	Table 20.16; Condition: High-speed on-chip oscillator mode revised
		440	Table 20.17 added
		441	Figure 20.8 revised
		443	Table 20.22; I_{IH}, I_{IL}, R_{PULLUP} Condition: “Vcc = 3V” added
		444	Table 20.23; Condition “Increase during A/D converter operation” added
		445	Figure 20.12 revised
		448	Table 20.29; Condition “Increase during A/D converter operation” added
		449	Figure 20.16 revised
		475	Package Dimensions; “PTLG0064JA-A (64F0G)” added
3.00	Feb 29, 2008	–	“RENESAS TECHNICAL UPDATE” reflected: TN-16C-A164A/E, TN-16C-A165A/E, TN-16C-A166A/E, TN-16C-A167A/E
		2, 3	Table 1.1, Table 1.2 Clock; “Real-time clock (timer RE)” added
		5, 7	Table 1.3, Table 1.4 revised
		6, 8	Figure 1.2, Figure 1.3; ROM number “XXX” added
		16, 17	Figure 3.1, Figure 3.2; “Expanded area” deleted

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3.00	Feb 29, 2008	18	Table 4.1; “002Ch” added, “003Bh” “003Ch” “003Dh” deleted
		27	Figure 5.3 revised
		27, 128, 401	Figure 5.4, Figure 13.2, Figure 19.4; “OFS Register” revised
		28	5.1.1, 5.1.2; “Wait for 1/fOCO-S × 20.” → “Wait for 10 μs or more.”
		29	Figure 5.5, Figure 5.6 revised
		30	5.2, Figure 5.7 revised
		36	Figure 6.5 NOTE6 revised
		61, 62	Table 7.17, Table 7.19 revised
		65	Table 7.29, Table 7.30 revised
		70	Table 7.48 revised
		73	10. “(with oscillation stop detection function)” deleted
		74	Figure 10.1 revised
		75	Figure 10.2 NOTE4 revised
		78	Figure 10.5 NOTE2 revised
		79	Figure 10.6 “FRA7 Register” added
		80	Figure 10.8 NOTE6 revised
		81	Figure 10.9 added
		83	10.2.2 revised
		88	10.5.1.2, 10.5.1.4 revised
		90	Table 10.3 revised
		92	10.5.2.5, Figure 10.13 revised
		94	Figure 10.14 revised
		96	10.6.1 revised
		99	10.7.1, 10.7.2 revised
		103	12.1.3.1 revised
		105	Table 12.2 “Reference” revised
		115	12.2.1 revised
		120	Table 12.6 revised, NOTE2 added
		124	12.6.4 deleted
		125	Figure 12.20 NOTE2 revised
		133	Table 14.1 “• fC32” deleted
		134	Figure 14.1 “TSTART” → “TCSTF”
		138	Figure 14.5 “... to 0 (During count).” → “... to 1 (During count).”
		149	14.1.6 revised, “• When the TRAPRE ...” “• When the TRA ...” added
		150	14.2 “The reload register ...” deleted Figure 14.12 revised
		153	Table 14.15 revised
		156	Figure 14.17 “... to 0 (During count).” → “... to 1 (During count).”

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		Page	Summary
3.00	Feb 29, 2008	159	Table 14.9 NOTE2 added "...0 (one-shot stops)." → "...1 (one-shot stops)." "TRBP pin function" → "TRBO pin function"
		160	Figure 14.20 "... When write, ..." → "... If necessary, ..."
		164	Table 14.10 NOTE2 added
		167 to 170	14.2.5 revised 14.2.5.1, 14.2.5.2, 14.2.5.3, 14.2.5.4 added
		197, 214	Table 14.25, Table 14.27; "at the same time as the TRDi register ... 0000h" deleted
		198, 215	Figure 14.47, Figure 14.63; "TRDSTR register" revised
		201	Figure 14.50 "TRDOER1 register" revised
		206	Figure 14.55 revised
		209	Figure 14.59 "of counter clear" deleted
		212	Figure 14.61 revised
		214	Table 14.27 revised
		220	Figure 14.68 revised
		227, 251	Table 14.29, Table 14.33; "at the same time as the TRD0 register ... 0000h" deleted
		228	Figure 14.76 revised
		232	Figure 14.80 revised
		238	Figure 14.86 revised
		239	Figure 14.87 revised
		243	Figure 14.91 revised
		252	Figure 14.98 "TRDSTR register" revised
		257	Figure 14.103 revised
		261	Figure 14.107 revised
		264	14.3.12.1, Table 14.36; "after the count is cleared" deleted
		277	Figure 14.121 "00" → "00b"
		286	Figure 14.130 revised
		291	Figure 15.4 "UARTi Transmit/Receive Mode Register" NOTE2 deleted
		293	Figure 15.6 "(b7-b4)" → "(b7-b6)"
		300	Table 15.5 NOTE2 added
		303	Table 15.7 revised
		304	15.3 revised
		308	Figure 16.2 NOTE4 deleted
		309	Figure 16.3 revised, NOTE4 deleted
		310	Figure 16.4 NOTE2 deleted
		311	Figure 16.5 NOTE1 deleted
		312	Figure 16.6 NOTE2, NOTE7 revised
		313	Figure 16.7 NOTE5 revised

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3.00	Feb 29, 2008	314	Figure 16.8; SSTDR register: NOTE1 deleted, SSRDR register: NOTE2 deleted
		328	Figure 16.18 revised
		334	16.2.8.1 deleted
		338	Figure 16.24 NOTE6 revised
		339	Figure 16.25 NOTE5 deleted
		340	Figure 16.26 NOTE7 deleted
		341	Figure 16.27 NOTE3 revised
		342	Figure 16.28 NOTE7 revised
		343, 344	Figure 16.29, Figure 16.30; NOTE1 deleted
		367	16.3.8.1 revised, 16.3.8.2 added
		368	Figure 17.1 revised
		373	Figure 17.5 “... in LINST register → 0” → “... in LINST register → 1”
		374	Figure 17.6 revised
		375	Figure 17.7 revised
		377	Figure 17.9 revised
		379	Figure 17.11 “SCDCT” → “BCDCT”
		380	Figure 17.12 revised
		385, 388, 391	Figure 18.2, Figure 18.4, Figure 18.6; NOTE4 revised
		394	Figure 18.10 revised
		396	18.7 revised
		397	Table 19.2 revised
		402	Table 19.3 revised
		403	19.4.1, 19.4.2; “(SR-ES)” → “(SR-SUS)”
		404	19.4.2.4 “located outside ... memory.” → “transferred to the RAM.”
		405	19.4.2.15 revised
		406	Figure 19.5 NOTE3, NOTE5 revised
		408	Figure 19.7 NOTE5 revised
		410	Figure 19.9 revised
		411	Figure 19.11 revised
		413	19.4.3.4 revised
		414	Figure 19.13 revised
		416	Figure 19.15 revised
		418	Table 19.6 “FRM00 Register” → “FRM0 Register”
		420	Table 19.7 revised
		429	Table 20.2 NOTE2 revised
		435	Table 20.10 revised, NOTE4 added
		454	21.1.1, 21.1.2 revised

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		Page	Summary
3.00	Feb 29, 2008	455	21.2.4 deleted
		456	Figure 21.1 NOTE2 revised
		458	21.3.1 revised, “• When the TRAPRE ...” “• When the TRA ...” added
		459 to 462	21.3.2 revised 21.3.2.1, 21.3.2.2, 21.3.2.3, 21.3.2.4 added
		463	21.3.1.1, Table 21.1; “after the count is cleared” deleted
		470	Figure 21.8 revised
		472	21.4 revised
		473	2.5.1.1 deleted, 2.5.2.1 revised, 2.5.2.2 added
		475	21.7 revised
		482	Appendix Figure 2.1, Appendix Figure 2.2 revised
		483	Appendix Figure 3.1 revised

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