

## **1. Overview**

### **1.1 Features**

The M16C Family offers a robust platform of 32-/16-bit CISC microcomputers (MCUs) featuring high ROM code efficiency, extensive EMI/EMS noise immunity, ultra-low power consumption, high-speed processing in actual applications, and numerous and varied integrated peripherals. Extensive device scalability from low- to high-end, featuring a single architecture as well as compatible pin assignments and peripheral functions, provides support for a vast range of application fields.

The R32C/100 Series is a high-end microcontroller series in the M16C Family. With a 4-Gbyte memory space, it achieves maximum code efficiency and high-speed processing with 32-bit CISC architecture, multiplier, multiply-accumulate unit, and floating point unit. The selection from the broadest choice of on-chip peripheral devices — UART, CRC, DMAC, A/D converter, timers, I<sup>2</sup>C, and WDT enables to minimize external components.

The R32C/100 Series, in particular, provides the R32C/161 Group, a product specific to vehicle network. This product, provided as 80-pin plastic molded LQFP package, configures two channels of CAN, one channel of LIN, and standard peripherals.

#### **1.1.1 Applications**

Automotive, audio, communication equipment, industrial equipment etc.

### 1.1.2 Performance Overview

Table 1.1 and Table 1.2 show the performance overview of the R32C/161 Group.

**Table 1.1 R32C/161 Group Performance (1/2)**

| Unit             | Function                | Performance                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------------|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CPU              | Central processing unit | R32C/100 Series CPU Core <ul style="list-style-type: none"> <li>• Basic instructions: 108</li> <li>• Minimum instruction execution time: 20.83 ns (<math>f(\text{CPU}) = 48 \text{ MHz}</math>)</li> <li>• Multiplier: 32-bit <math>\times</math> 32-bit <math>\rightarrow</math> 64-bit</li> <li>• Multiply-accumulate unit: 32-bit <math>\times</math> 32-bit + 64-bit <math>\rightarrow</math> 64-bit</li> <li>• IEEE-754 floating point standard: Single precision</li> <li>• 32-bit barrel shifter</li> <li>• Operating mode: Single-chip mode</li> </ul> |
| Memory           |                         | Flash memory: 128/256 Kbytes<br>RAM: 12/20 Kbytes<br>Data flash: 4 Kbytes $\times$ 2 blocks<br>E <sup>2</sup> dataFlash: none <sup>(1)</sup> /4 Kbytes<br>Refer to Table 1.3 for details                                                                                                                                                                                                                                                                                                                                                                       |
| Voltage Detector | Low voltage detector    | Optional <sup>(2)</sup><br>Low voltage detection interrupt                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Clock            | Clock generator         | <ul style="list-style-type: none"> <li>• 4 circuits (main clock, sub clock, PLL, on-chip oscillator)</li> <li>• Oscillation stop detector: Main clock oscillator stop/re-oscillation detection</li> <li>• Frequency divide circuit: Divide-by-2 to divide-by-24 selectable</li> <li>• Low power modes: Wait mode, stop mode</li> </ul>                                                                                                                                                                                                                         |
| Interrupts       |                         | Interrupt vectors: 261<br>External interrupt inputs: $\overline{\text{NMI}}$ , $\overline{\text{INT}} \times 6$<br>Interrupt priority levels: 7 levels                                                                                                                                                                                                                                                                                                                                                                                                         |
| Watchdog Timer   |                         | 15 bits $\times$ 1 (selectable input frequency from prescaler output)<br>Automatic timer start function is available                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| DMA              | DMAC                    | 4 channels <ul style="list-style-type: none"> <li>• Cycle-steal transfer mode</li> <li>• Request sources: 44</li> <li>• 2 transfer modes: Single transfer, repeat transfer</li> </ul>                                                                                                                                                                                                                                                                                                                                                                          |
|                  | DMAC II                 | <ul style="list-style-type: none"> <li>• Can be activated by any peripheral interrupt source</li> <li>• 3 transfer functions: Immediate data transfer, calculation transfer, chained transfer</li> </ul>                                                                                                                                                                                                                                                                                                                                                       |
| I/O Ports        | Programmable I/O ports  | <ul style="list-style-type: none"> <li>• 2 input-only ports</li> <li>• 64 CMOS inputs/outputs</li> <li>• A pull-up resistor is selectable for every 4 input ports</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                   |

Notes:

1. Please contact a Renesas sales office to use the non-E<sup>2</sup>dataFlash version.
2. Please contact a Renesas sales office to use the optional feature.

**Table 1.2 R32C/161 Group Performance (2/2)**

| Unit                               | Function                        | Performance                                                                                                                                                                                                                   |
|------------------------------------|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timer                              | Timer A                         | 16-bit timer × 5<br>Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode<br>Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3                           |
|                                    | Timer B                         | 16-bit timer × 6<br>Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode                                                                                                            |
|                                    | Three-phase motor control timer | Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used)<br>8-bit programmable dead time timer                                                                                                                    |
| Serial Interface                   | UART0 to UART4                  | Asynchronous/synchronous serial interface × 5 channels<br>• I <sup>2</sup> C-bus (UART0 to UART2)<br>• Special mode 2 (UART0 to UART2)                                                                                        |
| A/D Converter                      |                                 | 10-bit resolution × 23 channels<br>Sample and hold functionality integrated<br>Self Test/Open-Circuit Detection Assist                                                                                                        |
| CRC Calculator                     |                                 | CRC-CCITT ( $X^{16} + X^{12} + X^5 + 1$ )                                                                                                                                                                                     |
| X-Y Converter                      |                                 | 16 bits × 16 bits                                                                                                                                                                                                             |
| Intelligent I/O                    |                                 | Time measurement (input capture): 16 bits × 8<br>Digital debounce circuit contained<br>Waveform generation (output compare): 16 bits × 8<br>Phase shift waveform output mode contained                                        |
| Serial Bus Interface (SBI)         |                                 | 1 channel<br>• Synchronous serial communication mode<br>• 4-wire serial bus mode<br>Programmable character length: 8 to 16 bits                                                                                               |
| LIN Module                         |                                 | 1 channel                                                                                                                                                                                                                     |
| CAN Module                         |                                 | 2 channels<br>CAN functionality compliant with ISO11898-1<br>32 mailboxes                                                                                                                                                     |
| Flash Memory                       |                                 | Programming and erasure supply voltage: VCC = 3.0 to 5.5 V<br>Minimum endurance: 1,000 program/erase cycles<br>Security protection: ROM code protect, ID code protect<br>Debugging: On-chip debug, on-board flash programming |
| E <sup>2</sup> dataFlash           |                                 | Minimum endurance: 100,000 program/erase cycles                                                                                                                                                                               |
| Operating Frequency/Supply Voltage |                                 | 48 MHz/VCC = 3.0 to 5.5 V                                                                                                                                                                                                     |
| Operating Temperature              |                                 | -40°C to 85°C (version J)<br>-40°C to 105°C (version L) <sup>(1)</sup><br>-40°C to 125°C (version K)                                                                                                                          |
| Current Consumption                |                                 | 31 mA (VCC = 5.0 V, f(CPU) = 48 MHz)<br>8 μA (VCC = 3.3 V, f(XCIN) = 32.768 kHz, wait mode)                                                                                                                                   |
| Package                            |                                 | 80-pin plastic molded LQFP (PLQP0080KB-A)                                                                                                                                                                                     |

Note:

1. Please contact a Renesas sales office to use the version L products.

## 1.2 Product Information

Table 1.3 lists the product information and Figure 1.1 shows the details of the part number.

**Table 1.3 R32C/161 Group Product List**

**As of December, 2009**

| Part Number     | Package Code <sup>(1)</sup> | ROM Capacity <sup>(2)</sup> | RAM Capacity | E <sup>2</sup> dataFlash | Remarks                  |
|-----------------|-----------------------------|-----------------------------|--------------|--------------------------|--------------------------|
| R5F64610JFP     | PLQP0080KB-A                | 128 Kbytes<br>+ 8 Kbytes    | 12 Kbytes    | 4 Kbytes                 | Version J                |
| R5F64610LFP (D) |                             |                             |              |                          | Version L <sup>(3)</sup> |
| R5F64610KFP (D) |                             |                             |              |                          | Version K                |
| R5F6461EJFP (D) |                             |                             |              | NA <sup>(3)</sup>        | Version J                |
| R5F6461ELFP (D) |                             |                             |              |                          | Version L <sup>(3)</sup> |
| R5F6461EKFP (D) |                             |                             |              |                          | Version K                |
| R5F64611JFP (D) |                             | 256 Kbytes<br>+ 8 Kbytes    | 20 Kbytes    | 4 Kbytes                 | Version J                |
| R5F64611LFP (D) |                             |                             |              |                          | Version L <sup>(3)</sup> |
| R5F64611KFP (D) |                             |                             |              |                          | Version K                |
| R5F6461FJFP (D) |                             |                             |              | NA <sup>(3)</sup>        | Version J                |
| R5F6461FLFP (D) |                             |                             |              |                          | Version L <sup>(3)</sup> |
| R5F6461FKFP (D) |                             |                             |              |                          | Version K                |

(D): Under development

Notes:

1. The old package code is as follows: PLQP0080KB-A: 80P6Q-A
2. Data flash memory provides an additional 8 Kbytes of ROM capacity.
3. Please contact a Renesas sales office to use the non-E<sup>2</sup>dataFlash version or the version L products.

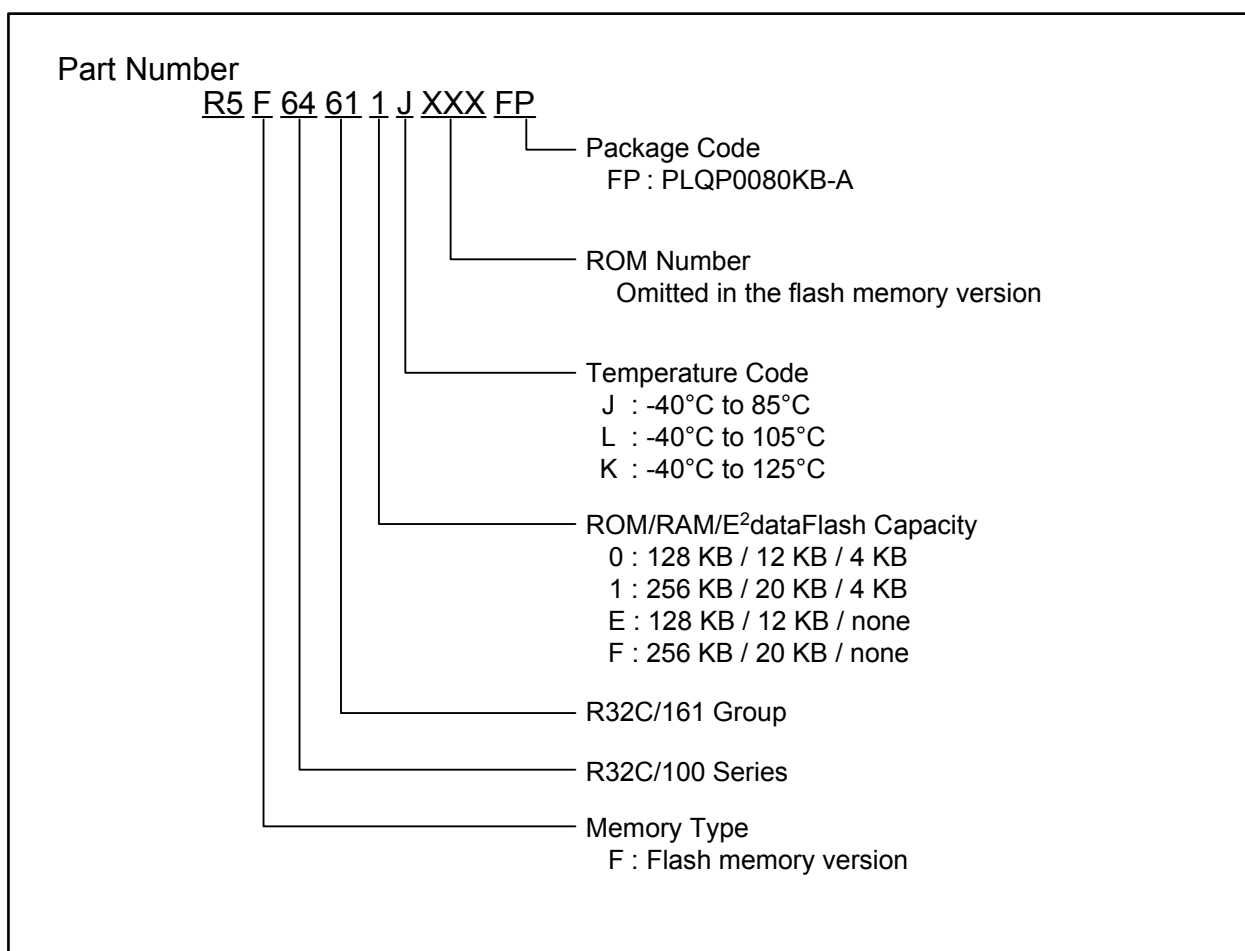


Figure 1.1 Part Numbering

### 1.3 Block Diagram

Figure 1.2 shows a block diagram of the R32C/161 Group.

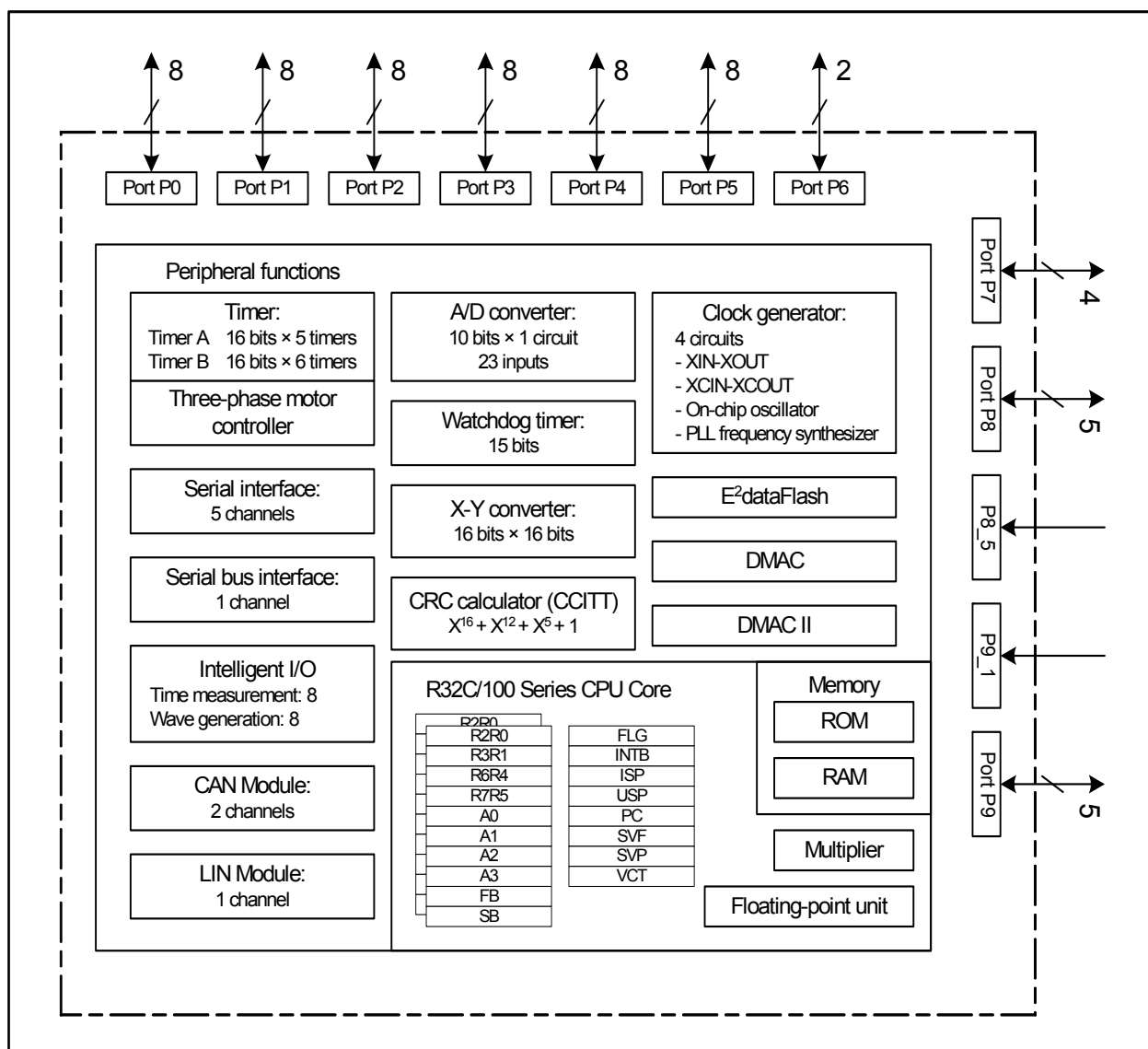
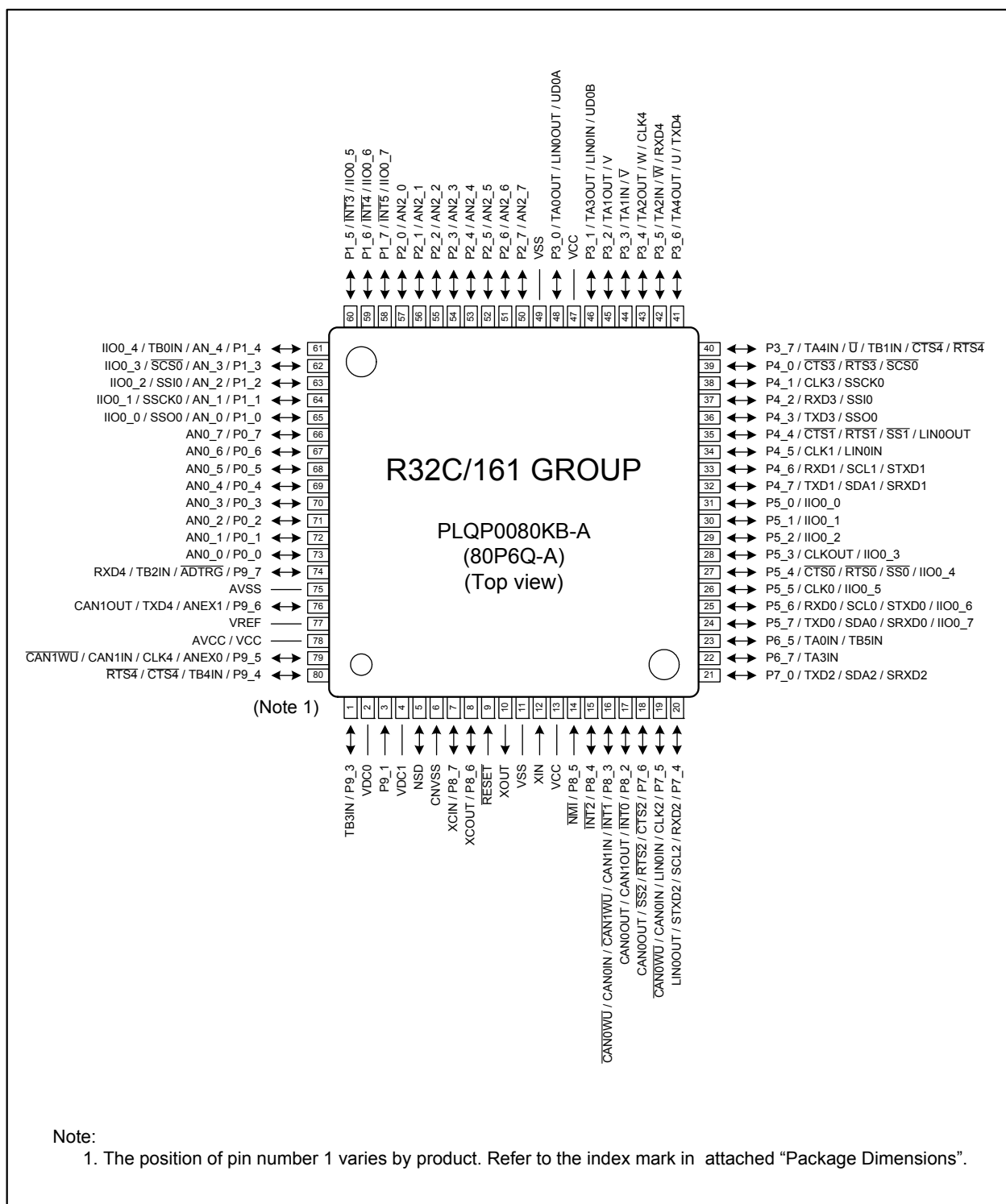


Figure 1.2 R32C/161 Group Block Diagram

## 1.4 Pin Assignment

Figure 1.3 shows the pin assignment (top view) and Table 1.4 and Table 1.5 show the pin characteristics.



**Figure 1.3 Pin Assignment (top view)**

**Table 1.4 Pin Characteristics (1/2)**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin       | UART / SBI Pin  | Intelligent I/O Pin | LIN / CAN Module Pin            | Analog Pin |
|---------|-------------|------|---------------|-----------------|-----------------|---------------------|---------------------------------|------------|
| 1       |             | P9_3 |               | TB3IN           |                 |                     |                                 |            |
| 2       | VDC0        |      |               |                 |                 |                     |                                 |            |
| 3       |             | P9_1 |               |                 |                 |                     |                                 |            |
| 4       | VDC1        |      |               |                 |                 |                     |                                 |            |
| 5       | NSD         |      |               |                 |                 |                     |                                 |            |
| 6       | CNVSS       |      |               |                 |                 |                     |                                 |            |
| 7       | XCIN        | P8_7 |               |                 |                 |                     |                                 |            |
| 8       | XCOU        | P8_6 |               |                 |                 |                     |                                 |            |
| 9       | RESET       |      |               |                 |                 |                     |                                 |            |
| 10      | XOUT        |      |               |                 |                 |                     |                                 |            |
| 11      | VSS         |      |               |                 |                 |                     |                                 |            |
| 12      | XIN         |      |               |                 |                 |                     |                                 |            |
| 13      | VCC         |      |               |                 |                 |                     |                                 |            |
| 14      |             | P8_5 | NMI           |                 |                 |                     |                                 |            |
| 15      |             | P8_4 | INT2          |                 |                 |                     |                                 |            |
| 16      |             | P8_3 | INT1          |                 |                 |                     | CAN0IN/CAN0WU/<br>CAN1IN/CAN1WU |            |
| 17      |             | P8_2 | INT0          |                 |                 |                     | CAN0OUT/<br>CAN1OUT             |            |
| 18      |             | P7_6 |               |                 | CTS2/RTS2/SS2   |                     | CAN0OUT                         |            |
| 19      |             | P7_5 |               |                 | CLK2            |                     | LIN0IN/CAN0IN/<br>CAN0WU        |            |
| 20      |             | P7_4 |               |                 | RXD2/SCL2/STXD2 |                     | LIN0OUT                         |            |
| 21      |             | P7_0 |               |                 | TXD2/SDA2/SRXD2 |                     |                                 |            |
| 22      |             | P6_7 |               | TA3IN           |                 |                     |                                 |            |
| 23      |             | P6_5 |               | TA0IN/<br>TB5IN |                 |                     |                                 |            |
| 24      |             | P5_7 |               |                 | TXD0/SDA0/SRXD0 | IIO0_7              |                                 |            |
| 25      |             | P5_6 |               |                 | RXD0/SCL0/STXD0 | IIO0_6              |                                 |            |
| 26      |             | P5_5 |               |                 | CLK0            | IIO0_5              |                                 |            |
| 27      |             | P5_4 |               |                 | CTS0/RTS0/SS0   | IIO0_4              |                                 |            |
| 28      | CLKOUT      | P5_3 |               |                 |                 | IIO0_3              |                                 |            |
| 29      |             | P5_2 |               |                 |                 | IIO0_2              |                                 |            |
| 30      |             | P5_1 |               |                 |                 | IIO0_1              |                                 |            |
| 31      |             | P5_0 |               |                 |                 | IIO0_0              |                                 |            |
| 32      |             | P4_7 |               |                 | TXD1/SDA1/SRXD1 |                     |                                 |            |
| 33      |             | P4_6 |               |                 | RXD1/SCL1/STXD1 |                     |                                 |            |
| 34      |             | P4_5 |               |                 | CLK1            |                     | LIN0IN                          |            |
| 35      |             | P4_4 |               |                 | CTS1/RTS1/SS1   |                     | LIN0OUT                         |            |
| 36      |             | P4_3 |               |                 | TXD3/SS00       |                     |                                 |            |
| 37      |             | P4_2 |               |                 | RXD3/SSI0       |                     |                                 |            |
| 38      |             | P4_1 |               |                 | CLK3/SSCK0      |                     |                                 |            |
| 39      |             | P4_0 |               |                 | CTS3/RTS3/SCS0  |                     |                                 |            |

**Table 1.5 Pin Characteristics (2/2)**

| Pin No. | Control Pin  | Port | Interrupt Pin | Timer Pin         | UART / SBI Pin | Intelligent I/O Pin | LIN / CAN Module Pin | Analog Pin |
|---------|--------------|------|---------------|-------------------|----------------|---------------------|----------------------|------------|
| 40      |              | P3_7 |               | TA4IN/U/<br>TB1IN | CTS4/RTS4      |                     |                      |            |
| 41      |              | P3_6 |               | TA4OUT/U          | TXD4           |                     |                      |            |
| 42      |              | P3_5 |               | TA2IN/W           | RXD4           |                     |                      |            |
| 43      |              | P3_4 |               | TA2OUT/W          | CLK4           |                     |                      |            |
| 44      |              | P3_3 |               | TA1IN/V           |                |                     |                      |            |
| 45      |              | P3_2 |               | TA1OUT/V          |                |                     |                      |            |
| 46      |              | P3_1 |               | TA3OUT            |                | UD0B                | LIN0IN               |            |
| 47      | VCC          |      |               |                   |                |                     |                      |            |
| 48      |              | P3_0 |               | TA0OUT            |                | UD0A                | LIN0OUT              |            |
| 49      | VSS          |      |               |                   |                |                     |                      |            |
| 50      |              | P2_7 |               |                   |                |                     |                      | AN2_7      |
| 51      |              | P2_6 |               |                   |                |                     |                      | AN2_6      |
| 52      |              | P2_5 |               |                   |                |                     |                      | AN2_5      |
| 53      |              | P2_4 |               |                   |                |                     |                      | AN2_4      |
| 54      |              | P2_3 |               |                   |                |                     |                      | AN2_3      |
| 55      |              | P2_2 |               |                   |                |                     |                      | AN2_2      |
| 56      |              | P2_1 |               |                   |                |                     |                      | AN2_1      |
| 57      |              | P2_0 |               |                   |                |                     |                      | AN2_0      |
| 58      |              | P1_7 | INT5          |                   |                | IIO0_7              |                      |            |
| 59      |              | P1_6 | INT4          |                   |                | IIO0_6              |                      |            |
| 60      |              | P1_5 | INT3          |                   |                | IIO0_5              |                      |            |
| 61      |              | P1_4 |               | TB0IN             |                | IIO0_4              |                      | AN_4       |
| 62      |              | P1_3 |               |                   | SCS0           | IIO0_3              |                      | AN_3       |
| 63      |              | P1_2 |               |                   | SSI0           | IIO0_2              |                      | AN_2       |
| 64      |              | P1_1 |               |                   | SSCK0          | IIO0_1              |                      | AN_1       |
| 65      |              | P1_0 |               |                   | SSO0           | IIO0_0              |                      | AN_0       |
| 66      |              | P0_7 |               |                   |                |                     |                      | AN0_7      |
| 67      |              | P0_6 |               |                   |                |                     |                      | AN0_6      |
| 68      |              | P0_5 |               |                   |                |                     |                      | AN0_5      |
| 69      |              | P0_4 |               |                   |                |                     |                      | AN0_4      |
| 70      |              | P0_3 |               |                   |                |                     |                      | AN0_3      |
| 71      |              | P0_2 |               |                   |                |                     |                      | AN0_2      |
| 72      |              | P0_1 |               |                   |                |                     |                      | AN0_1      |
| 73      |              | P0_0 |               |                   |                |                     |                      | AN0_0      |
| 74      |              | P9_7 |               | TB2IN             | RXD4           |                     |                      | ADTRG      |
| 75      | AVSS         |      |               |                   |                |                     |                      |            |
| 76      |              | P9_6 |               |                   | TXD4           |                     | CAN1OUT              | ANEX1      |
| 77      | VREF         |      |               |                   |                |                     |                      |            |
| 78      | AVCC/<br>VCC |      |               |                   |                |                     |                      |            |
| 79      |              | P9_5 |               |                   | CLK4           |                     | CAN1IN/CAN1WU        | ANEX0      |
| 80      |              | P9_4 |               | TB4IN             | CTS4/RTS4      |                     |                      |            |

## 1.5 Pin Definitions and Functions

Table 1.6 and Table 1.7 shows the pin definitions and functions.

**Table 1.6 Pin Definitions and Functions (1/2)**

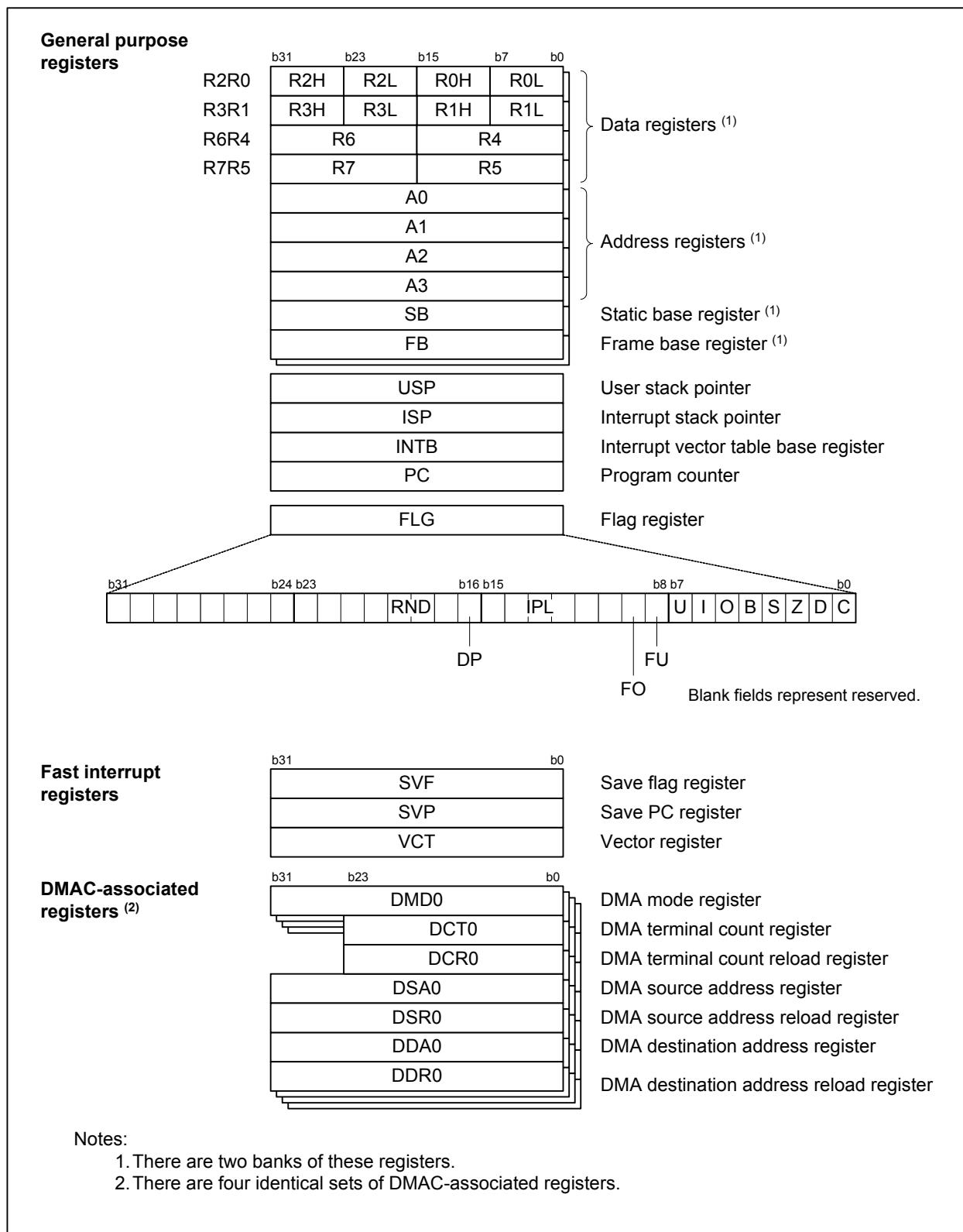
| Function                                 | Symbol                                                                                                                                                                         | I/O | Description                                                                                                                                                                                                                                                     |
|------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Power supply                             | VCC, VSS                                                                                                                                                                       | I   | Applicable as follows: VCC = 3.0 to 5.5 V, VSS = 0 V                                                                                                                                                                                                            |
| Connecting pins for decoupling capacitor | VDC0, VDC1                                                                                                                                                                     | —   | A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1                                                                                                                                                                           |
| Analog power supply                      | AVCC, AVSS                                                                                                                                                                     | I   | Power supply for the A/D converter. AVSS should be connected to VSS                                                                                                                                                                                             |
| Reset input                              | $\overline{\text{RESET}}$                                                                                                                                                      | I   | The MCU is reset when this pin is driven low                                                                                                                                                                                                                    |
| CNVSS                                    | CNVSS                                                                                                                                                                          | I   | This pin should be connected to VSS via a resistor                                                                                                                                                                                                              |
| Debug port                               | NSD                                                                                                                                                                            | I/O | This pin is to communicate with a debugger. It should be connected to VCC via a resistor of 1 to 4.7 k $\Omega$                                                                                                                                                 |
| Main clock input                         | XIN                                                                                                                                                                            | I   | Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open                                                           |
| Main clock output                        | XOUT                                                                                                                                                                           | O   |                                                                                                                                                                                                                                                                 |
| Sub clock input                          | XCIN                                                                                                                                                                           | I   | Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOUT. An external clock should be input at the XCIN while leaving the XCOUT open                                                                     |
| Sub clock output                         | XCOUT                                                                                                                                                                          | O   |                                                                                                                                                                                                                                                                 |
| Clock output                             | CLKOUT                                                                                                                                                                         | O   | Output of the clock with the same frequency as fC, f8, or f32                                                                                                                                                                                                   |
| External interrupt input                 | INT0 to INT5                                                                                                                                                                   | I   | Input for external interrupts                                                                                                                                                                                                                                   |
| NMI input                                | P8_5/ $\overline{\text{NMI}}$                                                                                                                                                  | I   | Input for NMI                                                                                                                                                                                                                                                   |
| I/O ports                                | P0_0 to P0_7<br>P1_0 to P1_7<br>P2_0 to P2_7<br>P3_0 to P3_7<br>P4_0 to P4_7<br>P5_0 to P5_7<br>P6_5, P6_7<br>P7_0, P7_4 to P7_6<br>P8_2 to P8_4<br>P8_6, P8_7<br>P9_3 to P9_7 | I/O | I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register.<br>Pull-up resistors are selected for following 4-pin units, but are enabled only for the input pins: Pi_0 to Pi_3 and Pi_4 to Pi_7 (i = 0 to 9) |
| Input port                               | P9_1                                                                                                                                                                           | I   | Input port in CMOS. Pull-up resistors are selectable for P9_1 and P9_3                                                                                                                                                                                          |

**Table 1.7 Pin Definitions and Functions (2/2)**

| Function                               | Symbol                                           | I/O | Description                                                                                        |
|----------------------------------------|--------------------------------------------------|-----|----------------------------------------------------------------------------------------------------|
| Timer A                                | TA0OUT to TA4OUT                                 | I/O | Timers A0 to A4 input/output                                                                       |
|                                        | TA0IN to TA4IN                                   | I   | Timers A0 to A4 input                                                                              |
| Timer B                                | TB0IN to TB5IN                                   | I   | Timers B0 to B5 input                                                                              |
| Three-phase motor control timer output | U, $\bar{U}$ , V, $\bar{V}$ , W, $\bar{W}$       | O   | Three-phase motor control timer output                                                             |
| Serial interface                       | CTS0 to CTS4                                     | I   | Handshake input                                                                                    |
|                                        | RTS0 to RTS4                                     | O   | Handshake output                                                                                   |
|                                        | CLK0 to CLK4                                     | I/O | Transmit/receive clock input/output                                                                |
|                                        | RXD0 to RXD4                                     | I   | Serial data input                                                                                  |
|                                        | TXD0 to TXD4                                     | O   | Serial data output                                                                                 |
| I <sup>2</sup> C bus (simplified)      | SDA0 to SDA2                                     | I/O | Serial data input/output                                                                           |
|                                        | SCL0 to SCL2                                     | I/O | Transmit/receive clock input/output                                                                |
| Serial interface special functions     | STXD0 to STXD2                                   | O   | Serial data output in slave mode                                                                   |
|                                        | SRXD0 to SRXD2                                   | I   | Serial data input in slave mode                                                                    |
|                                        | $\overline{SS0}$ to $\overline{SS2}$             | I   | Input to control serial interface special functions                                                |
| A/D converter                          | AN_0 to AN_4<br>AN0_0 to AN0_7<br>AN2_0 to AN2_7 | I   | Analog input for the A/D converter                                                                 |
|                                        | ADTRG                                            | I   | External trigger input for the A/D converter                                                       |
|                                        | ANEX0                                            | I/O | Expanded analog input for the A/D converter and output in external op-amp connection mode          |
|                                        | ANEX1                                            | I   | Expanded analog input for the A/D converter                                                        |
| Reference voltage input                | VREF                                             | I   | Reference voltage input for the A/D converter and D/A converter                                    |
| Intelligent I/O                        | IIO0_0 to IIO0_7                                 | I/O | Input/output for the Intelligent I/O group 0. Either input capture or output compare is selectable |
|                                        | UD0A, UD0B                                       | I   | Input for the two-phase encoder                                                                    |
| Serial bus interface                   | SSO0                                             | I/O | Serial data output. Functions as serial data input/output in 4-wire serial bus mode                |
|                                        | SSI0                                             | I/O | Serial data input. Functions as serial data input/output in 4-wire serial bus mode                 |
|                                        | SSCK0                                            | I/O | Transmit/receive clock input/output                                                                |
|                                        | $\overline{SCS0}$                                | I/O | Input/output to control the synchronous serial interface                                           |
| LIN module                             | LIN0OUT                                          | O   | Transmit data output for the LIN communications                                                    |
|                                        | LIN0IN                                           | I   | Receive data input for the LIN communications                                                      |
| CAN module                             | CAN0IN, CAN1IN                                   | I   | Receive data input for the CAN communications                                                      |
|                                        | CAN0OUT, CAN1OUT                                 | O   | Transmit data output for the CAN communications                                                    |
|                                        | CAN0WU, CAN1WU                                   | I   | Input for the CAN wake-up interrupt                                                                |

## 2. Central Processing Unit (CPU)

The CPU contains registers as shown below. There are two register banks each consisting of registers R2R0, R3R1, R6R4, R7R5, A0 to A3, SB, and FB.



**Figure 2.1 CPU Registers**

## 2.1 General Purpose Registers

### 2.1.1 Data Registers (R2R0, R3R1, R6R4, and R7R5)

These 32-bit registers are primarily used for transfers and arithmetic/logic operations.

Each of the registers can be divided into upper and lower 16-bit registers, e.g. R2R0 can be divided into R2 and R0, R3R0 can be divided into R3 and R1, etc.

Moreover, data registers R2R0 and R3R1 can be divided into four 8-bit data registers: upper (R2H and R3H), mid-upper (R2L and R3L), mid-lower (R0H and R1H), and lower (R0L and R1L).

### 2.1.2 Address Registers (A0, A1, A2, and A3)

These 32-bit registers have functions similar to data registers. They are also used for address register indirect addressing and address register relative addressing.

### 2.1.3 Static Base Register (SB)

This 32-bit register is used for SB relative addressing.

### 2.1.4 Frame Base Register (FB)

This 32-bit register is used for FB relative addressing.

### 2.1.5 Program Counter (PC)

This 32-bit counter indicates the address of the instruction to be executed next.

### 2.1.6 Interrupt Vector Table Base Register (INTB)

This 32-bit register indicates the start address of a relocatable vector table.

### 2.1.7 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Two types of 32-bit stack pointers (SPs) are provided: user stack pointer (USP) and interrupt stack pointer (ISP).

Use the stack pointer select flag (U flag) to select either the user stack pointer (USP) or the interrupt stack pointer (ISP). The U flag is bit 7 in the flag register (FLG). Refer to 2.1.8 "Flag Register (FLG)" for details.

To minimize the overhead of interrupt sequence due to less memory access, set the user stack pointer (USP) or the interrupt stack pointer (ISP) to a multiple of 4.

### 2.1.8 Flag Register (FLG)

This 32-bit register indicates the CPU status.

#### 2.1.8.1 Carry Flag (C flag)

This flag becomes 1 when any of the carry, borrow, shifted-out bit, etc. is generated in the arithmetic logic unit (ALU).

#### 2.1.8.2 Debug Flag (D flag)

This flag is only for debugging. Only set this bit to 0.

#### 2.1.8.3 Zero Flag (Z flag)

This flag becomes 1 when the result of an operation is 0; otherwise it is 0.

#### 2.1.8.4 Sign Flag (S flag)

This flag becomes 1 when the result of an operation is a negative value; otherwise it is 0.

**2.1.8.5 Register Bank Select Flag (B flag)**

This flag selects a register bank. It indicates 0 when the register bank 0 is selected, and 1 when the register bank 1 is selected.

**2.1.8.6 Overflow Flag (O flag)**

This flag becomes 1 if an overflow occurs in an operation; otherwise it is 0.

**2.1.8.7 Interrupt Enable Flag (I flag)**

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

**2.1.8.8 Stack Pointer Select Flag (U flag)**

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.

It becomes 0 when a hardware interrupts is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

**2.1.8.9 Floating-point Underflow Flag (FU flag)**

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand has invalid numbers (subnormal numbers).

**2.1.8.10 Floating-point Overflow Flag (FO flag)**

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand has invalid numbers (subnormal numbers).

**2.1.8.11 Processor Interrupt Priority Level (IPL)**

The processor interrupt priority level (IPL), consisting of three bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is acceptable when the interrupt request level is higher than the selected IPL.

When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

**2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)**

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to take. It is used in the MULX instruction.

**2.1.8.13 Floating-point Rounding Mode (RND)**

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

**2.1.8.14 Reserved**

Only set this bit to 0. The read value is undefined.

## 2.2 Fast Interrupt Registers

The following three registers are provided to minimize the overhead of interrupt sequence.

### 2.2.1 Save Flag Register (SVF)

This 32-bit register is used to save the flag register when a fast interrupt is generated.

### 2.2.2 Save PC Register (SVP)

This 32-bit register is used to save the program counter when a fast interrupt is generated.

### 2.2.3 Vector Register (VCT)

This 32-bit register is used to indicate a jump address when a fast interrupt is generated.

## 2.3 DMAC-associated Registers

There are seven types of DMAC-associated registers.

### 2.3.1 DMA Mode Registers (DMD0, DMD1, DMD2, and DMD3)

These 32-bit registers are used to set DMA transfer mode, bit rate etc.

### 2.3.2 DMA Terminal Count Registers (DCT0, DCT1, DCT2, and DCT3)

These 24-bit registers are used to set DMA transfer counting.

### 2.3.3 DMA Terminal Count Reload Registers (DCR0, DCR1, DCR2, and DCR3)

These 24-bit registers are used to set the reloaded values for DMA terminal count registers.

### 2.3.4 DMA Source Address Registers (DSA0, DSA1, DSA2, and DSA3)

These 32-bit registers are used to set DMA source addresses.

### 2.3.5 DMA Source Address Reload Registers (DSR0, DSR1, DSR2, and DSR3)

These 32-bit registers are used to set the reloaded value for DMA source address register.

### 2.3.6 DMA Destination Address Registers (DDA0, DDA1, DDA2, and DDA3)

These 32-bit registers are used to set DMA destination address.

### 2.3.7 DMA Destination Address Reload Registers (DDR0, DDR1, DDR2, and DDR3)

These 32-bit registers are used to set reloaded values for DMA destination address registers.

### 3. Memory

Figure 3.1 shows the memory map of the R32C/161 Group.

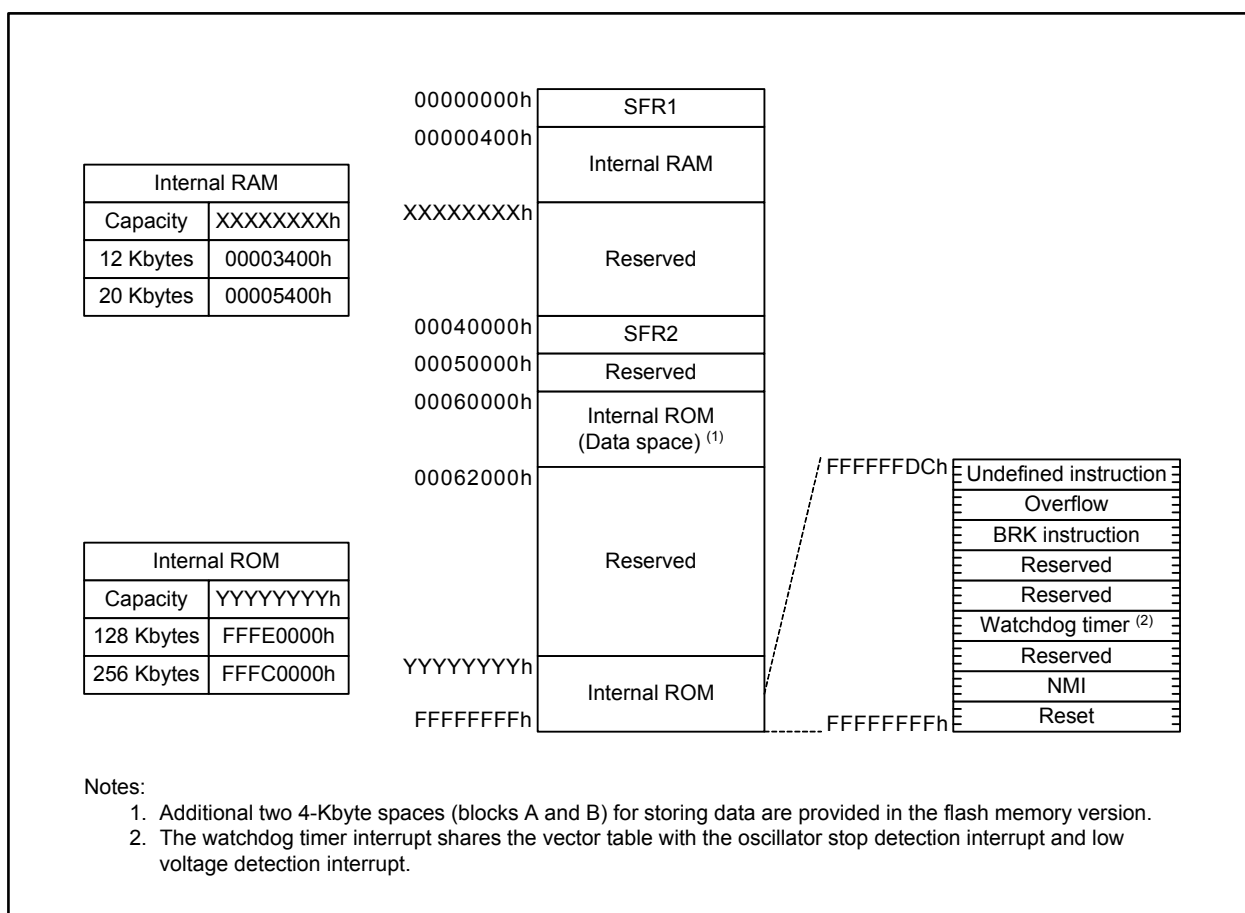
The R32C/161 Group provides a 4-Gbyte address space from 00000000h to FFFFFFFFh.

The internal ROM is mapped to the end of the memory map with the ending address fixed at FFFFFFFFh. Therefore, the 256-Kbyte internal ROM is mapped from FFFC0000h to FFFFFFFFh.

The fixed interrupt vector table which contains each start address of interrupt handlers is mapped from FFFFFFFDCh to FFFFFFFFh.

The internal RAM is mapped to the beginning of the memory map with the starting address fixed at 00000400h. Therefore, the 20-Kbyte internal RAM is mapped from 00000400h to 000053FFh. Besides being used for data storage, the internal RAM functions as a stack(s) for subroutines and/or interrupt handlers.

Special Function Registers (SFRs), which are control registers for peripheral functions, are mapped from 00000000h to 00003FFh, and from 00040000h to 0004FFFFh. Unoccupied SFR locations are reserved. No access is allowed.



**Figure 3.1 Memory Map**

## 4. Special Function Registers (SFRs)

SFRs are memory-mapped peripheral registers that control the operation of peripherals. Table 4.1 SFR List (1) to Table 4.53 SFR List (53) list the SFR details.

**Table 4.1 SFR List (1)**

| Address               | Register                                  | Symbol | Reset Value |
|-----------------------|-------------------------------------------|--------|-------------|
| 000000h               |                                           |        |             |
| 000001h               |                                           |        |             |
| 000002h               |                                           |        |             |
| 000003h               |                                           |        |             |
| 000004h               | Clock Control Register                    | CCR    | 0001 1000b  |
| 000005h               |                                           |        |             |
| 000006h               | Flash Memory Control Register             | FMCR   | 0000 0001b  |
| 000007h               | Protect Release Register                  | PRR    | 00h         |
| 000008h               |                                           |        |             |
| 000009h               |                                           |        |             |
| 00000Ah               |                                           |        |             |
| 00000Bh               |                                           |        |             |
| 00000Ch               |                                           |        |             |
| 00000Dh               |                                           |        |             |
| 00000Eh               |                                           |        |             |
| 00000Fh               |                                           |        |             |
| 000010h               |                                           |        |             |
| 000011h               |                                           |        |             |
| 000012h               |                                           |        |             |
| 000013h               |                                           |        |             |
| 000014h               |                                           |        |             |
| 000015h               |                                           |        |             |
| 000016h               |                                           |        |             |
| 000017h               |                                           |        |             |
| 000018h               |                                           |        |             |
| 000019h               |                                           |        |             |
| 00001Ah               |                                           |        |             |
| 00001Bh               |                                           |        |             |
| 00001Ch               | Flash Memory Rewrite Bus Control Register | FEBC   | 0000h       |
| 00001Dh               |                                           |        |             |
| 00001Eh               | Peripheral Bus Control Register           | PBC    | 0504h       |
| 00001Fh               |                                           |        |             |
| 000020h to<br>00005Fh |                                           |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.2 SFR List (2)**

| Address | Register                                                                  | Symbol  | Reset Value |
|---------|---------------------------------------------------------------------------|---------|-------------|
| 000060h |                                                                           |         |             |
| 000061h | Timer B5 Interrupt Control Register                                       | TB5IC   | XXXX X000b  |
| 000062h |                                                                           |         |             |
| 000063h | UART2 Receive/ACK Interrupt Control Register                              | S2RIC   | XXXX X000b  |
| 000064h |                                                                           |         |             |
| 000065h |                                                                           |         |             |
| 000066h |                                                                           |         |             |
| 000067h |                                                                           |         |             |
| 000068h | DMA0 Transfer Complete Interrupt Control Register                         | DM0IC   | XXXX X000b  |
| 000069h | UART0 Start Condition/Stop Condition Detection Interrupt Control Register | BCN0IC  | XXXX X000b  |
| 00006Ah | DMA2 Transfer Complete Interrupt Control Register                         | DM2IC   | XXXX X000b  |
| 00006Bh | A/D Converter 0 Convert Completion Interrupt Control Register             | AD0IC   | XXXX X000b  |
| 00006Ch | Timer A0 Interrupt Control Register                                       | TA0IC   | XXXX X000b  |
| 00006Dh | Intelligent I/O Interrupt Control Register 0                              | IIO0IC  | XXXX X000b  |
| 00006Eh | Timer A2 Interrupt Control Register                                       | TA2IC   | XXXX X000b  |
| 00006Fh | Intelligent I/O Interrupt Control Register 2                              | IIO2IC  | XXXX X000b  |
| 000070h | Timer A4 Interrupt Control Register                                       | TA4IC   | XXXX X000b  |
| 000071h | Intelligent I/O Interrupt Control Register 4                              | IIO4IC  | XXXX X000b  |
| 000072h | UART0 Receive/ACK Interrupt Control Register                              | S0RIC   | XXXX X000b  |
| 000073h | Intelligent I/O Interrupt Control Register 6                              | IIO6IC  | XXXX X000b  |
| 000074h | UART1 Receive/ACK Interrupt Control Register                              | S1RIC   | XXXX X000b  |
| 000075h | Intelligent I/O Interrupt Control Register 8                              | IIO8IC  | XXXX X000b  |
| 000076h | Timer B1 Interrupt Control Register                                       | TB1IC   | XXXX X000b  |
| 000077h | Intelligent I/O Interrupt Control Register 10                             | IIO10IC | XXXX X000b  |
| 000078h | Timer B3 Interrupt Control Register                                       | TB3IC   | XXXX X000b  |
| 000079h |                                                                           |         |             |
| 00007Ah | INT5 Interrupt Control Register                                           | INT5IC  | XX00 X000b  |
| 00007Bh | CAN0 Wake-up Interrupt Control Register                                   | C0WIC   | XXXX X000b  |
| 00007Ch | INT3 Interrupt Control Register                                           | INT3IC  | XX00 X000b  |
| 00007Dh |                                                                           |         |             |
| 00007Eh | INT1 Interrupt Control Register                                           | INT1IC  | XX00 X000b  |
| 00007Fh | LIN Low Detection Interrupt Control Register                              | LLDIC   | XXXX X000b  |
| 000080h |                                                                           |         |             |
| 000081h | UART2 Transmit/NACK Interrupt Control Register                            | S2TIC   | XXXX X000b  |
| 000082h |                                                                           |         |             |
| 000083h |                                                                           |         |             |
| 000084h |                                                                           |         |             |
| 000085h |                                                                           |         |             |
| 000086h |                                                                           |         |             |
| 000087h | UART2 Start Condition/Stop Condition Detection Interrupt Control Register | BCN2IC  | XXXX X000b  |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.3 SFR List (3)**

| Address | Register                                                                  | Symbol  | Reset Value |
|---------|---------------------------------------------------------------------------|---------|-------------|
| 000088h | DMA1 Transfer Complete Interrupt Control Register                         | DM1IC   | XXXX X000b  |
| 000089h | UART1 Start Condition/Stop Condition Detection Interrupt Control Register | BCN1IC  | XXXX X000b  |
| 00008Ah | DMA3 Transfer Complete Interrupt Control Register                         | DM3IC   | XXXX X000b  |
| 00008Bh |                                                                           |         |             |
| 00008Ch | Timer A1 Interrupt Control Register                                       | TA1IC   | XXXX X000b  |
| 00008Dh | Intelligent I/O Interrupt Control Register 1                              | IIO1IC  | XXXX X000b  |
| 00008Eh | Timer A3 Interrupt Control Register                                       | TA3IC   | XXXX X000b  |
| 00008Fh | Intelligent I/O Interrupt Control Register 3                              | IIO3IC  | XXXX X000b  |
| 000090h | UART0 Transmit/NACK Interrupt Control Register                            | S0TIC   | XXXX X000b  |
| 000091h | Intelligent I/O Interrupt Control Register 5                              | IIO5IC  | XXXX X000b  |
| 000092h | UART1 Transmit/NACK Interrupt Control Register                            | S1TIC   | XXXX X000b  |
| 000093h | Intelligent I/O Interrupt Control Register 7                              | IIO7IC  | XXXX X000b  |
| 000094h | Timer B0 Interrupt Control Register                                       | TB0IC   | XXXX X000b  |
| 000095h | Intelligent I/O Interrupt Control Register 9                              | IIO9IC  | XXXX X000b  |
| 000096h | Timer B2 Interrupt Control Register                                       | TB2IC   | XXXX X000b  |
| 000097h | Intelligent I/O Interrupt Control Register 11                             | IIO11IC | XXXX X000b  |
| 000098h | Timer B4 Interrupt Control Register                                       | TB4IC   | XXXX X000b  |
| 000099h |                                                                           |         |             |
| 00009Ah | INT4 Interrupt Control Register                                           | INT4IC  | XX00 X000b  |
| 00009Bh | CAN1 Wake-up Interrupt Control Register                                   | C1WIC   | XXXX X000b  |
| 00009Ch | INT2 Interrupt Control Register                                           | INT2IC  | XX00 X000b  |
| 00009Dh |                                                                           |         |             |
| 00009Eh | INT0 Interrupt Control Register                                           | INT0IC  | XX00 X000b  |
| 00009Fh |                                                                           |         |             |
| 0000A0h | Intelligent I/O Interrupt Request Register 0                              | IIO0IR  | 0000 00X1b  |
| 0000A1h | Intelligent I/O Interrupt Request Register 1                              | IIO1IR  | 0000 00X1b  |
| 0000A2h | Intelligent I/O Interrupt Request Register 2                              | IIO2IR  | 0000 0001b  |
| 0000A3h | Intelligent I/O Interrupt Request Register 3                              | IIO3IR  | 0000 00X1b  |
| 0000A4h | Intelligent I/O Interrupt Request Register 4                              | IIO4IR  | 0000 00X1b  |
| 0000A5h | Intelligent I/O Interrupt Request Register 5                              | IIO5IR  | 0000 00X1b  |
| 0000A6h | Intelligent I/O Interrupt Request Register 6                              | IIO6IR  | 0000 00X1b  |
| 0000A7h | Intelligent I/O Interrupt Request Register 7                              | IIO7IR  | 000X 00X1b  |
| 0000A8h | Intelligent I/O Interrupt Request Register 8                              | IIO8IR  | 0000 0001b  |
| 0000A9h | Intelligent I/O Interrupt Request Register 9                              | IIO9IR  | 0000 0001b  |
| 0000AAh | Intelligent I/O Interrupt Request Register 10                             | IIO10IR | 0000 0001b  |
| 0000ABh | Intelligent I/O Interrupt Request Register 11                             | IIO11IR | 0000 00X1b  |
| 0000ACh |                                                                           |         |             |
| 0000ADh |                                                                           |         |             |
| 0000AEh |                                                                           |         |             |
| 0000AFh |                                                                           |         |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.4 SFR List (4)**

| Address | Register                                          | Symbol  | Reset Value |
|---------|---------------------------------------------------|---------|-------------|
| 0000B0h | Intelligent I/O Interrupt Enable Register 0       | IIO0IE  | 00h         |
| 0000B1h | Intelligent I/O Interrupt Enable Register 1       | IIO1IE  | 00h         |
| 0000B2h | Intelligent I/O Interrupt Enable Register 2       | IIO2IE  | 00h         |
| 0000B3h | Intelligent I/O Interrupt Enable Register 3       | IIO3IE  | 00h         |
| 0000B4h | Intelligent I/O Interrupt Enable Register 4       | IIO4IE  | 00h         |
| 0000B5h | Intelligent I/O Interrupt Enable Register 5       | IIO5IE  | 00h         |
| 0000B6h | Intelligent I/O Interrupt Enable Register 6       | IIO6IE  | 00h         |
| 0000B7h | Intelligent I/O Interrupt Enable Register 7       | IIO7IE  | 00h         |
| 0000B8h | Intelligent I/O Interrupt Enable Register 8       | IIO8IE  | 00h         |
| 0000B9h | Intelligent I/O Interrupt Enable Register 9       | IIO9IE  | 00h         |
| 0000BAh | Intelligent I/O Interrupt Enable Register 10      | IIO10IE | 00h         |
| 0000BBh | Intelligent I/O Interrupt Enable Register 11      | IIO11IE | 00h         |
| 0000BCh |                                                   |         |             |
| 0000BDh |                                                   |         |             |
| 0000BEh |                                                   |         |             |
| 0000BFh |                                                   |         |             |
| 0000C0h | Serial Bus Interface 0 Interrupt Control Register | SS0IC   | XXXX X000b  |
| 0000C1h | CAN0 Transmit Interrupt Control Register          | C0TIC   | XXXX X000b  |
| 0000C2h |                                                   |         |             |
| 0000C3h | CAN0 Error Interrupt Control Register             | C0EIC   | XXXX X000b  |
| 0000C4h |                                                   |         |             |
| 0000C5h | CAN1 Receive Interrupt Control Register           | C1RIC   | XXXX X000b  |
| 0000C6h |                                                   |         |             |
| 0000C7h |                                                   |         |             |
| 0000C8h |                                                   |         |             |
| 0000C9h |                                                   |         |             |
| 0000CAh |                                                   |         |             |
| 0000CBh |                                                   |         |             |
| 0000CCh |                                                   |         |             |
| 0000CDh |                                                   |         |             |
| 0000CEh |                                                   |         |             |
| 0000CFh |                                                   |         |             |
| 0000D0h | CAN0 Transmit FIFO Interrupt Control Register     | C0FTIC  | XXXX X000b  |
| 0000D1h |                                                   |         |             |
| 0000D2h | CAN1 Transmit FIFO Interrupt Control Register     | C1FTIC  | XXXX X000b  |
| 0000D3h |                                                   |         |             |
| 0000D4h |                                                   |         |             |
| 0000D5h | LIN0 Interrupt Control Register                   | L0IC    | XXXX X000b  |
| 0000D6h |                                                   |         |             |
| 0000D7h |                                                   |         |             |
| 0000D8h | E2dataFlash Interrupt Control Register            | E2FIC   | XXXX X000b  |
| 0000D9h |                                                   |         |             |
| 0000DAh |                                                   |         |             |
| 0000DBh |                                                   |         |             |
| 0000DCh |                                                   |         |             |
| 0000DDh | UART3 Transmit Interrupt Control Register         | S3TIC   | XXXX X000b  |
| 0000DEh |                                                   |         |             |
| 0000DFh | UART4 Transmit Interrupt Control Register         | S4TIC   | XXXX X000b  |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.5 SFR List (5)**

| Address | Register                                     | Symbol | Reset Value |
|---------|----------------------------------------------|--------|-------------|
| 0000E0h |                                              |        |             |
| 0000E1h | CAN0 Receive Interrupt Control Register      | C0RIC  | XXXX X000b  |
| 0000E2h |                                              |        |             |
| 0000E3h | CAN1 Transmit Interrupt Control Register     | C1TIC  | XXXX X000b  |
| 0000E4h |                                              |        |             |
| 0000E5h | CAN1 Error Interrupt Control Register        | C1EIC  | XXXX X000b  |
| 0000E6h |                                              |        |             |
| 0000E7h |                                              |        |             |
| 0000E8h |                                              |        |             |
| 0000E9h |                                              |        |             |
| 0000EAh |                                              |        |             |
| 0000EBh |                                              |        |             |
| 0000ECh |                                              |        |             |
| 0000EDh |                                              |        |             |
| 0000EEh |                                              |        |             |
| 0000EFh |                                              |        |             |
| 0000F0h | CAN0 Receive FIFO Interrupt Control Register | C0FRIC | XXXX X000b  |
| 0000F1h |                                              |        |             |
| 0000F2h | CAN1 Receive FIFO Interrupt Control Register | C1FRIC | XXXX X000b  |
| 0000F3h |                                              |        |             |
| 0000F4h |                                              |        |             |
| 0000F5h |                                              |        |             |
| 0000F6h |                                              |        |             |
| 0000F7h |                                              |        |             |
| 0000F8h |                                              |        |             |
| 0000F9h |                                              |        |             |
| 0000FAh |                                              |        |             |
| 0000FBh |                                              |        |             |
| 0000FCh |                                              |        |             |
| 0000FDh | UART3 Receive Interrupt Control Register     | S3RIC  | XXXX X000b  |
| 0000FEh |                                              |        |             |
| 0000FFh | UART4 Receive Interrupt Control Register     | S4RIC  | XXXX X000b  |
| 000100h |                                              |        |             |
| 000101h |                                              |        |             |
| 000102h |                                              |        |             |
| 000103h |                                              |        |             |
| 000104h |                                              |        |             |
| 000105h |                                              |        |             |
| 000106h |                                              |        |             |
| 000107h |                                              |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.6 SFR List (6)**

| Address            | Register                                                | Symbol      | Reset Value |
|--------------------|---------------------------------------------------------|-------------|-------------|
| 000108h to 00016Fh |                                                         |             |             |
| 000170h            |                                                         |             |             |
| 000171h            |                                                         |             |             |
| 000172h            |                                                         |             |             |
| 000173h            |                                                         |             |             |
| 000174h            |                                                         |             |             |
| 000175h            |                                                         |             |             |
| 000176h            |                                                         |             |             |
| 000177h            |                                                         |             |             |
| 000178h            |                                                         |             |             |
| 000179h            |                                                         |             |             |
| 00017Ah            |                                                         |             |             |
| 00017Bh            |                                                         |             |             |
| 00017Ch            |                                                         |             |             |
| 00017Dh            |                                                         |             |             |
| 00017Eh            |                                                         |             |             |
| 00017Fh            |                                                         |             |             |
| 000180h            | Group 0 Time Measurement/Waveform Generation Register 0 | G0TM0/G0PO0 | XXXXh       |
| 000181h            |                                                         |             |             |
| 000182h            | Group 0 Time Measurement/Waveform Generation Register 1 | G0TM1/G0PO1 | XXXXh       |
| 000183h            |                                                         |             |             |
| 000184h            | Group 0 Time Measurement/Waveform Generation Register 2 | G0TM2/G0PO2 | XXXXh       |
| 000185h            |                                                         |             |             |
| 000186h            | Group 0 Time Measurement/Waveform Generation Register 3 | G0TM3/G0PO3 | XXXXh       |
| 000187h            |                                                         |             |             |
| 000188h            | Group 0 Time Measurement/Waveform Generation Register 4 | G0TM4/G0PO4 | XXXXh       |
| 000189h            |                                                         |             |             |
| 00018Ah            | Group 0 Time Measurement/Waveform Generation Register 5 | G0TM5/G0PO5 | XXXXh       |
| 00018Bh            |                                                         |             |             |
| 00018Ch            | Group 0 Time Measurement/Waveform Generation Register 6 | G0TM6/G0PO6 | XXXXh       |
| 00018Dh            |                                                         |             |             |
| 00018Eh            | Group 0 Time Measurement/Waveform Generation Register 7 | G0TM7/G0PO7 | XXXXh       |
| 00018Fh            |                                                         |             |             |
| 000190h            | Group 0 Waveform Generation Control Register 0          | G0POCR0     | 0000 X000b  |
| 000191h            | Group 0 Waveform Generation Control Register 1          | G0POCR1     | 0X00 X000b  |
| 000192h            | Group 0 Waveform Generation Control Register 2          | G0POCR2     | 0X00 X000b  |
| 000193h            | Group 0 Waveform Generation Control Register 3          | G0POCR3     | 0X00 X000b  |
| 000194h            | Group 0 Waveform Generation Control Register 4          | G0POCR4     | 0X00 X000b  |
| 000195h            | Group 0 Waveform Generation Control Register 5          | G0POCR5     | 0X00 X000b  |
| 000196h            | Group 0 Waveform Generation Control Register 6          | G0POCR6     | 0X00 X000b  |
| 000197h            | Group 0 Waveform Generation Control Register 7          | G0POCR7     | 0X00 X000b  |
| 000198h            | Group 0 Time Measurement Control Register 0             | G0TMCR0     | 00h         |
| 000199h            | Group 0 Time Measurement Control Register 1             | G0TMCR1     | 00h         |
| 00019Ah            | Group 0 Time Measurement Control Register 2             | G0TMCR2     | 00h         |
| 00019Bh            | Group 0 Time Measurement Control Register 3             | G0TMCR3     | 00h         |
| 00019Ch            | Group 0 Time Measurement Control Register 4             | G0TMCR4     | 00h         |
| 00019Dh            | Group 0 Time Measurement Control Register 5             | G0TMCR5     | 00h         |
| 00019Eh            | Group 0 Time Measurement Control Register 6             | G0TMCR6     | 00h         |
| 00019Fh            | Group 0 Time Measurement Control Register 7             | G0TMCR7     | 00h         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.7 SFR List (7)**

| Address | Register                                       | Symbol | Reset Value |
|---------|------------------------------------------------|--------|-------------|
| 0001A0h | Group 0 Base Timer Register                    | G0BT   | XXXXh       |
| 0001A1h |                                                |        |             |
| 0001A2h | Group 0 Base Timer Control Register 0          | G0BCR0 | 00h         |
| 0001A3h | Group 0 Base Timer Control Register 1          | G0BCR1 | 0000 0000b  |
| 0001A4h | Group 0 Timer Measurement Prescaler Register 6 | G0TPR6 | 00h         |
| 0001A5h | Group 0 Timer Measurement Prescaler Register 7 | G0TPR7 | 00h         |
| 0001A6h | Group 0 Function Enable Register               | G0FE   | 00h         |
| 0001A7h | Group 0 Function Select Register               | G0FS   | 00h         |
| 0001A8h |                                                |        |             |
| 0001A9h |                                                |        |             |
| 0001AAh |                                                |        |             |
| 0001ABh |                                                |        |             |
| 0001ACh |                                                |        |             |
| 0001ADh |                                                |        |             |
| 0001AEh |                                                |        |             |
| 0001AFh |                                                |        |             |
| 0001B0h |                                                |        |             |
| 0001B1h |                                                |        |             |
| 0001B2h |                                                |        |             |
| 0001B3h |                                                |        |             |
| 0001B4h |                                                |        |             |
| 0001B5h |                                                |        |             |
| 0001B6h |                                                |        |             |
| 0001B7h |                                                |        |             |
| 0001B8h |                                                |        |             |
| 0001B9h |                                                |        |             |
| 0001BAh |                                                |        |             |
| 0001BBh |                                                |        |             |
| 0001BCh |                                                |        |             |
| 0001BDh |                                                |        |             |
| 0001BEh |                                                |        |             |
| 0001BFh |                                                |        |             |
| 0001C0h |                                                |        |             |
| 0001C1h |                                                |        |             |
| 0001C2h |                                                |        |             |
| 0001C3h |                                                |        |             |
| 0001C4h |                                                |        |             |
| 0001C5h |                                                |        |             |
| 0001C6h |                                                |        |             |
| 0001C7h |                                                |        |             |
| 0001C8h |                                                |        |             |
| 0001C9h |                                                |        |             |
| 0001CAh |                                                |        |             |
| 0001CBh |                                                |        |             |
| 0001CCh |                                                |        |             |
| 0001CDh |                                                |        |             |
| 0001CEh |                                                |        |             |
| 0001CFh |                                                |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.8 SFR List (8)**

| Address | Register                                         | Symbol | Reset Value |
|---------|--------------------------------------------------|--------|-------------|
| 0001D0h |                                                  |        |             |
| 0001D1h |                                                  |        |             |
| 0001D2h |                                                  |        |             |
| 0001D3h |                                                  |        |             |
| 0001D4h |                                                  |        |             |
| 0001D5h |                                                  |        |             |
| 0001D6h |                                                  |        |             |
| 0001D7h |                                                  |        |             |
| 0001D8h |                                                  |        |             |
| 0001D9h |                                                  |        |             |
| 0001DAh |                                                  |        |             |
| 0001DBh |                                                  |        |             |
| 0001DCh |                                                  |        |             |
| 0001DDh |                                                  |        |             |
| 0001DEh |                                                  |        |             |
| 0001DFh |                                                  |        |             |
| 0001E0h | UART3 Transmit/Receive Mode Register             | U3MR   | 00h         |
| 0001E1h | UART3 Bit Rate Register                          | U3BRG  | XXh         |
| 0001E2h | UART3 Transmit Buffer Register                   | U3TB   | XXXXh       |
| 0001E3h |                                                  |        |             |
| 0001E4h | UART3 Transmit/Receive Control Register 0        | U3C0   | 00X0 1000b  |
| 0001E5h | UART3 Transmit/Receive Control Register 1        | U3C1   | XXXX 0010b  |
| 0001E6h | UART3 Receive Buffer Register                    | U3RB   | XXXXh       |
| 0001E7h |                                                  |        |             |
| 0001E8h | UART4 Transmit/Receive Mode Register             | U4MR   | 00h         |
| 0001E9h | UART4 Bit Rate Register                          | U4BRG  | XXh         |
| 0001EAh | UART4 Transmit Buffer Register                   | U4TB   | XXXXh       |
| 0001EBh |                                                  |        |             |
| 0001ECh | UART4 Transmit/Receive Control Register 0        | U4C0   | 00X0 1000b  |
| 0001EDh | UART4 Transmit/Receive Control Register 1        | U4C1   | XXXX 0010b  |
| 0001EEh | UART4 Receive Buffer Register                    | U4RB   | XXXXh       |
| 0001EFh |                                                  |        |             |
| 0001F0h | UART3, UART4 Transmit/Receive Control Register 2 | U34CON | X000 0000b  |
| 0001F1h |                                                  |        |             |
| 0001F2h |                                                  |        |             |
| 0001F3h |                                                  |        |             |
| 0001F4h |                                                  |        |             |
| 0001F5h |                                                  |        |             |
| 0001F6h |                                                  |        |             |
| 0001F7h |                                                  |        |             |
| 0001F8h |                                                  |        |             |
| 0001F9h |                                                  |        |             |
| 0001FAh |                                                  |        |             |
| 0001FBh |                                                  |        |             |
| 0001FCh |                                                  |        |             |
| 0001FDh |                                                  |        |             |
| 0001FEh |                                                  |        |             |
| 0001FFh |                                                  |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.9 SFR List (9)**

| Address | Register                                                                | Symbol  | Reset Value |
|---------|-------------------------------------------------------------------------|---------|-------------|
| 000200h | Group0 Phase Shift Waveform Output Mode Clock Division Setting Register | G0SDR   | 00h         |
| 000201h | Group0 Phase Shift Waveform Output Mode Control Register                | G0PSCR  | 00h         |
| 000202h |                                                                         |         |             |
| 000203h |                                                                         |         |             |
| 000204h |                                                                         |         |             |
| 000205h |                                                                         |         |             |
| 000206h |                                                                         |         |             |
| 000207h |                                                                         |         |             |
| 000208h | Timer B Event Clock Select Register                                     | TBECKS  | 0000 0000b  |
| 000209h |                                                                         |         |             |
| 00020Ah |                                                                         |         |             |
| 00020Bh |                                                                         |         |             |
| 00020Ch |                                                                         |         |             |
| 00020Dh |                                                                         |         |             |
| 00020Eh |                                                                         |         |             |
| 00020Fh |                                                                         |         |             |
| 000210h | IIO0_7 Digital Debounce Register                                        | IC07DDR | FFh         |
| 000211h |                                                                         |         |             |
| 000212h |                                                                         |         |             |
| 000213h |                                                                         |         |             |
| 000214h |                                                                         |         |             |
| 000215h |                                                                         |         |             |
| 000216h |                                                                         |         |             |
| 000217h |                                                                         |         |             |
| 000218h |                                                                         |         |             |
| 000219h |                                                                         |         |             |
| 00021Ah |                                                                         |         |             |
| 00021Bh |                                                                         |         |             |
| 00021Ch |                                                                         |         |             |
| 00021Dh |                                                                         |         |             |
| 00021Eh |                                                                         |         |             |
| 00021Fh |                                                                         |         |             |
| 000220h | Timer A1 Mirror Register                                                | TA1M    | XXXXh       |
| 000221h |                                                                         |         |             |
| 000222h | Timer A1-1 Mirror Register                                              | TA11M   | XXXXh       |
| 000223h |                                                                         |         |             |
| 000224h | Timer A2 Mirror Register                                                | TA2M    | XXXXh       |
| 000225h |                                                                         |         |             |
| 000226h | Timer A2-1 Mirror Register                                              | TA21M   | XXXXh       |
| 000227h |                                                                         |         |             |
| 000228h | Timer A4 Mirror Register                                                | TA4M    | XXXXh       |
| 000229h |                                                                         |         |             |
| 00022Ah | Timer A4-1 Mirror Register                                              | TA41M   | XXXXh       |
| 00022Bh |                                                                         |         |             |
| 00022Ch |                                                                         |         |             |
| 00022Dh |                                                                         |         |             |
| 00022Eh |                                                                         |         |             |
| 00022Fh |                                                                         |         |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.10 SFR List (10)**

| Address            | Register                                  | Symbol    | Reset Value |
|--------------------|-------------------------------------------|-----------|-------------|
| 000230h to 0002BFh |                                           |           |             |
| 0002C0h<br>0002C1h | X0 Register/Y0 Register                   | X0R/Y0R   | XXXXh       |
| 0002C2h<br>0002C3h | X1 Register/Y1 Register                   | X1R/Y1R   | XXXXh       |
| 0002C4h<br>0002C5h | X2 Register/Y2 Register                   | X2R/Y2R   | XXXXh       |
| 0002C6h<br>0002C7h | X3 Register/Y3 Register                   | X3R/Y3R   | XXXXh       |
| 0002C8h<br>0002C9h | X4 Register/Y4 Register                   | X4R/Y4R   | XXXXh       |
| 0002CAh<br>0002CBh | X5 Register/Y5 Register                   | X5R/Y5R   | XXXXh       |
| 0002CCh<br>0002CDh | X6 Register/Y6 Register                   | X6R/Y6R   | XXXXh       |
| 0002CEh<br>0002CFh | X7 Register/Y7 Register                   | X7R/Y7R   | XXXXh       |
| 0002D0h<br>0002D1h | X8 Register/Y8 Register                   | X8R/Y8R   | XXXXh       |
| 0002D2h<br>0002D3h | X9 Register/Y9 Register                   | X9R/Y9R   | XXXXh       |
| 0002D4h<br>0002D5h | X10 Register/Y10 Register                 | X10R/Y10R | XXXXh       |
| 0002D6h<br>0002D7h | X11 Register/Y11 Register                 | X11R/Y11R | XXXXh       |
| 0002D8h<br>0002D9h | X12 Register/Y12 Register                 | X12R/Y12R | XXXXh       |
| 0002DAh<br>0002DBh | X13 Register/Y13 Register                 | X13R/Y13R | XXXXh       |
| 0002DCh<br>0002DDh | X14 Register/Y14 Register                 | X14R/Y14R | XXXXh       |
| 0002DEh<br>0002DFh | X15 Register/Y15 Register                 | X15R/Y15R | XXXXh       |
| 0002E0h            | XY Control Register                       | XYC       | XXXX XX00b  |
| 0002E1h            |                                           |           |             |
| 0002E2h            |                                           |           |             |
| 0002E3h            |                                           |           |             |
| 0002E4h            | UART1 Special Mode Register 4             | U1SMR4    | 00h         |
| 0002E5h            | UART1 Special Mode Register 3             | U1SMR3    | 00h         |
| 0002E6h            | UART1 Special Mode Register 2             | U1SMR2    | 00h         |
| 0002E7h            | UART1 Special Mode Register               | U1SMR     | 00h         |
| 0002E8h            | UART1 Transmit/Receive Mode Register      | U1MR      | 00h         |
| 0002E9h            | UART1 Bit Rate Register                   | U1BRG     | XXh         |
| 0002EAh<br>0002EBh | UART1 Transmit Buffer Register            | U1TB      | XXXXh       |
| 0002ECh            | UART1 Transmit/Receive Control Register 0 | U1C0      | 0000 1000b  |
| 0002EDh            | UART1 Transmit/Receive Control Register 1 | U1C1      | 0000 0010b  |
| 0002EEh<br>0002EFh | UART1 Receive Buffer Register             | U1RB      | XXXXh       |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.11 SFR List (11)**

| Address | Register                                            | Symbol | Reset Value |
|---------|-----------------------------------------------------|--------|-------------|
| 0002F0h |                                                     |        |             |
| 0002F1h |                                                     |        |             |
| 0002F2h |                                                     |        |             |
| 0002F3h |                                                     |        |             |
| 0002F4h |                                                     |        |             |
| 0002F5h |                                                     |        |             |
| 0002F6h |                                                     |        |             |
| 0002F7h |                                                     |        |             |
| 0002F8h |                                                     |        |             |
| 0002F9h |                                                     |        |             |
| 0002FAh |                                                     |        |             |
| 0002FBh |                                                     |        |             |
| 0002FCh |                                                     |        |             |
| 0002FDh |                                                     |        |             |
| 0002FEh |                                                     |        |             |
| 0002FFh |                                                     |        |             |
| 000300h | Count Start Register for Timers B3, B4 and B5       | TBSR   | 000X XXXXb  |
| 000301h |                                                     |        |             |
| 000302h | Timer A1-1 Register                                 | TA11   | XXXXh       |
| 000303h |                                                     |        |             |
| 000304h | Timer A2-1 Register                                 | TA21   | XXXXh       |
| 000305h |                                                     |        |             |
| 000306h | Timer A4-1 Register                                 | TA41   | XXXXh       |
| 000307h |                                                     |        |             |
| 000308h | Three-phase PWM Control Register 0                  | INVC0  | 00h         |
| 000309h | Three-phase PWM Control Register 1                  | INVC1  | 00h         |
| 00030Ah | Three-phase Output Buffer Register 0                | IDB0   | XX11 1111b  |
| 00030Bh | Three-phase Output Buffer Register 1                | IDB1   | XX11 1111b  |
| 00030Ch | Dead Time Timer                                     | DTT    | XXh         |
| 00030Dh | Timer B2 Interrupt Generating Frequency Set Counter | ICTB2  | XXh         |
| 00030Eh |                                                     |        |             |
| 00030Fh |                                                     |        |             |
| 000310h | Timer B3 Register                                   | TB3    | XXXXh       |
| 000311h |                                                     |        |             |
| 000312h | Timer B4 Register                                   | TB4    | XXXXh       |
| 000313h |                                                     |        |             |
| 000314h | Timer B5 Register                                   | TB5    | XXXXh       |
| 000315h |                                                     |        |             |
| 000316h |                                                     |        |             |
| 000317h |                                                     |        |             |
| 000318h |                                                     |        |             |
| 000319h |                                                     |        |             |
| 00031Ah |                                                     |        |             |
| 00031Bh | Timer B3 Mode Register                              | TB3MR  | 00XX 0000b  |
| 00031Ch | Timer B4 Mode Register                              | TB4MR  | 00XX 0000b  |
| 00031Dh | Timer B5 Mode Register                              | TB5MR  | 00XX 0000b  |
| 00031Eh |                                                     |        |             |
| 00031Fh |                                                     |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.12 SFR List (12)**

| Address | Register                                     | Symbol | Reset Value |
|---------|----------------------------------------------|--------|-------------|
| 000320h |                                              |        |             |
| 000321h |                                              |        |             |
| 000322h |                                              |        |             |
| 000323h |                                              |        |             |
| 000324h |                                              |        |             |
| 000325h |                                              |        |             |
| 000326h |                                              |        |             |
| 000327h |                                              |        |             |
| 000328h |                                              |        |             |
| 000329h |                                              |        |             |
| 00032Ah |                                              |        |             |
| 00032Bh |                                              |        |             |
| 00032Ch |                                              |        |             |
| 00032Dh |                                              |        |             |
| 00032Eh |                                              |        |             |
| 00032Fh |                                              |        |             |
| 000330h |                                              |        |             |
| 000331h |                                              |        |             |
| 000332h |                                              |        |             |
| 000333h |                                              |        |             |
| 000334h | UART2 Special Mode Register 4                | U2SMR4 | 00h         |
| 000335h | UART2 Special Mode Register 3                | U2SMR3 | 00h         |
| 000336h | UART2 Special Mode Register 2                | U2SMR2 | 00h         |
| 000337h | UART2 Special Mode Register                  | U2SMR  | 00h         |
| 000338h | UART2 Transmission/Receive Mode Register     | U2MR   | 00h         |
| 000339h | UART2 Bit Rate Register                      | U2BRG  | XXh         |
| 00033Ah | UART2 Transmit Buffer Register               | U2TB   | XXXXh       |
| 00033Bh |                                              |        |             |
| 00033Ch | UART2 Transmit/Receive Control Register 0    | U2C0   | 0000 1000b  |
| 00033Dh | UART2 Transmit/Receive Control Register 1    | U2C1   | 0000 0010b  |
| 00033Eh | UART2 Receive Buffer Register                | U2RB   | XXXXh       |
| 00033Fh |                                              |        |             |
| 000340h | Count Start Register                         | TABSR  | 00h         |
| 000341h | Clock Prescaler Reset Register               | CPSRF  | 0XXX XXXXb  |
| 000342h | One-shot Start Register                      | ONSF   | 00h         |
| 000343h | Trigger Select Register                      | TRGSR  | 00h         |
| 000344h | Increment/Decrement Counting Select Register | UDF    | 0000 0000b  |
| 000345h |                                              |        |             |
| 000346h | Timer A0 Register                            | TA0    | XXXXh       |
| 000347h |                                              |        |             |
| 000348h | Timer A1 Register                            | TA1    | XXXXh       |
| 000349h |                                              |        |             |
| 00034Ah | Timer A2 Register                            | TA2    | XXXXh       |
| 00034Bh |                                              |        |             |
| 00034Ch | Timer A3 Register                            | TA3    | XXXXh       |
| 00034Dh |                                              |        |             |
| 00034Eh | Timer A4 Register                            | TA4    | XXXXh       |
| 00034Fh |                                              |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.13 SFR List (13)**

| Address | Register                                  | Symbol | Reset Value |
|---------|-------------------------------------------|--------|-------------|
| 000350h | Timer B0 Register                         | TB0    | XXXXh       |
| 000351h |                                           |        |             |
| 000352h | Timer B1 Register                         | TB1    | XXXXh       |
| 000353h |                                           |        |             |
| 000354h | Timer B2 Register                         | TB2    | XXXXh       |
| 000355h |                                           |        |             |
| 000356h | Timer A0 Mode Register                    | TA0MR  | 0000 0000b  |
| 000357h | Timer A1 Mode Register                    | TA1MR  | 0000 0000b  |
| 000358h | Timer A2 Mode Register                    | TA2MR  | 0000 0000b  |
| 000359h | Timer A3 Mode Register                    | TA3MR  | 0000 0000b  |
| 00035Ah | Timer A4 Mode Register                    | TA4MR  | 0000 0000b  |
| 00035Bh | Timer B0 Mode Register                    | TB0MR  | 00XX 0000b  |
| 00035Ch | Timer B1 Mode Register                    | TB1MR  | 00XX 0000b  |
| 00035Dh | Timer B2 Mode Register                    | TB2MR  | 00XX 0000b  |
| 00035Eh | Timer B2 Special Mode Register            | TB2SC  | XXXX XXX0b  |
| 00035Fh | Count Source Prescaler Register           | TCSPR  | 0000 0000b  |
| 000360h |                                           |        |             |
| 000361h |                                           |        |             |
| 000362h |                                           |        |             |
| 000363h |                                           |        |             |
| 000364h | UART0 Special Mode Register 4             | U0SMR4 | 00h         |
| 000365h | UART0 Special Mode Register 3             | U0SMR3 | 00h         |
| 000366h | UART0 Special Mode Register 2             | U0SMR2 | 00h         |
| 000367h | UART0 Special Mode Register               | U0SMR  | 00h         |
| 000368h | UART0 Transmit/Receive Mode Register      | U0MR   | 00h         |
| 000369h | UART0 Bit Rate Register                   | U0BRG  | XXh         |
| 00036Ah | UART0 Transmit Buffer Register            | U0TB   | XXXXh       |
| 00036Bh |                                           |        |             |
| 00036Ch | UART0 Transmit/Receive Control Register 0 | U0C0   | 0000 1000b  |
| 00036Dh | UART0 Transmit/Receive Control Register 1 | U0C1   | 0000 0010b  |
| 00036Eh | UART0 Receive Buffer Register             | U0RB   | XXXXh       |
| 00036Fh |                                           |        |             |
| 000370h |                                           |        |             |
| 000371h |                                           |        |             |
| 000372h |                                           |        |             |
| 000373h |                                           |        |             |
| 000374h |                                           |        |             |
| 000375h |                                           |        |             |
| 000376h |                                           |        |             |
| 000377h |                                           |        |             |
| 000378h |                                           |        |             |
| 000379h |                                           |        |             |
| 00037Ah |                                           |        |             |
| 00037Bh |                                           |        |             |
| 00037Ch | CRC Data Register                         | CRCD   | XXXXh       |
| 00037Dh |                                           |        |             |
| 00037Eh | CRC Input Register                        | CRCIN  | XXh         |
| 00037Fh |                                           |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.14 SFR List (14)**

| Address | Register                | Symbol  | Reset Value |
|---------|-------------------------|---------|-------------|
| 000380h | A/D0 Register 0         | AD00    | 00XXh       |
| 000381h |                         |         |             |
| 000382h | A/D0 Register 1         | AD01    | 00XXh       |
| 000383h |                         |         |             |
| 000384h | A/D0 Register 2         | AD02    | 00XXh       |
| 000385h |                         |         |             |
| 000386h | A/D0 Register 3         | AD03    | 00XXh       |
| 000387h |                         |         |             |
| 000388h | A/D0 Register 4         | AD04    | 00XXh       |
| 000389h |                         |         |             |
| 00038Ah | A/D0 Register 5         | AD05    | 00XXh       |
| 00038Bh |                         |         |             |
| 00038Ch | A/D0 Register 6         | AD06    | 00XXh       |
| 00038Dh |                         |         |             |
| 00038Eh | A/D0 Register 7         | AD07    | 00XXh       |
| 00038Fh |                         |         |             |
| 000390h |                         |         |             |
| 000391h |                         |         |             |
| 000392h |                         |         |             |
| 000393h | A/D0 Control Register 5 | AD0CON5 | 00h         |
| 000394h | A/D0 Control Register 2 | AD0CON2 | X00X X000b  |
| 000395h | A/D0 Control Register 3 | AD0CON3 | XXXX X000b  |
| 000396h | A/D0 Control Register 0 | AD0CON0 | 00h         |
| 000397h | A/D0 Control Register 1 | AD0CON1 | 00h         |
| 000398h |                         |         |             |
| 000399h |                         |         |             |
| 00039Ah |                         |         |             |
| 00039Bh |                         |         |             |
| 00039Ch |                         |         |             |
| 00039Dh |                         |         |             |
| 00039Eh |                         |         |             |
| 00039Fh |                         |         |             |
| 0003A0h |                         |         |             |
| 0003A1h |                         |         |             |
| 0003A2h |                         |         |             |
| 0003A3h |                         |         |             |
| 0003A4h |                         |         |             |
| 0003A5h |                         |         |             |
| 0003A6h |                         |         |             |
| 0003A7h |                         |         |             |
| 0003A8h |                         |         |             |
| 0003A9h |                         |         |             |
| 0003AAh |                         |         |             |
| 0003ABh |                         |         |             |
| 0003ACh |                         |         |             |
| 0003ADh |                         |         |             |
| 0003AEh |                         |         |             |
| 0003AFh |                         |         |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.15 SFR List (15)**

| Address | Register                   | Symbol | Reset Value |
|---------|----------------------------|--------|-------------|
| 0003B0h |                            |        |             |
| 0003B1h |                            |        |             |
| 0003B2h |                            |        |             |
| 0003B3h |                            |        |             |
| 0003B4h |                            |        |             |
| 0003B5h |                            |        |             |
| 0003B6h |                            |        |             |
| 0003B7h |                            |        |             |
| 0003B8h |                            |        |             |
| 0003B9h |                            |        |             |
| 0003BAh |                            |        |             |
| 0003BBh |                            |        |             |
| 0003BCh |                            |        |             |
| 0003BDh |                            |        |             |
| 0003BEh |                            |        |             |
| 0003BFh |                            |        |             |
| 0003C0h | Port P0 Register           | P0     | XXh         |
| 0003C1h | Port P1 Register           | P1     | XXh         |
| 0003C2h | Port P0 Direction Register | PD0    | 0000 0000b  |
| 0003C3h | Port P1 Direction Register | PD1    | 0000 0000b  |
| 0003C4h | Port P2 Register           | P2     | XXh         |
| 0003C5h | Port P3 Register           | P3     | XXh         |
| 0003C6h | Port P2 Direction Register | PD2    | 0000 0000b  |
| 0003C7h | Port P3 Direction Register | PD3    | 0000 0000b  |
| 0003C8h | Port P4 Register           | P4     | XXh         |
| 0003C9h | Port P5 Register           | P5     | XXh         |
| 0003CAh | Port P4 Direction Register | PD4    | 0000 0000b  |
| 0003CBh | Port P5 Direction Register | PD5    | 0000 0000b  |
| 0003CCh | Port P6 Register           | P6     | XXh         |
| 0003CDh | Port P7 Register           | P7     | XXh         |
| 0003CEh | Port P6 Direction Register | PD6    | 0000 0000b  |
| 0003CFh | Port P7 Direction Register | PD7    | 0000 0000b  |
| 0003D0h | Port P8 Register           | P8     | XXh         |
| 0003D1h | Port P9 Register           | P9     | XXh         |
| 0003D2h | Port P8 Direction Register | PD8    | 00X0 0000b  |
| 0003D3h | Port P9 Direction Register | PD9    | 0000 0000b  |
| 0003D4h |                            |        |             |
| 0003D5h |                            |        |             |
| 0003D6h |                            |        |             |
| 0003D7h |                            |        |             |
| 0003D8h |                            |        |             |
| 0003D9h |                            |        |             |
| 0003DAh |                            |        |             |
| 0003DBh |                            |        |             |
| 0003DCh |                            |        |             |
| 0003DDh |                            |        |             |
| 0003DEh |                            |        |             |
| 0003DFh |                            |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.16 SFR List (16)**

| Address | Register                   | Symbol | Reset Value |
|---------|----------------------------|--------|-------------|
| 0003E0h |                            |        |             |
| 0003E1h |                            |        |             |
| 0003E2h |                            |        |             |
| 0003E3h |                            |        |             |
| 0003E4h |                            |        |             |
| 0003E5h |                            |        |             |
| 0003E6h |                            |        |             |
| 0003E7h |                            |        |             |
| 0003E8h |                            |        |             |
| 0003E9h |                            |        |             |
| 0003EAh |                            |        |             |
| 0003EBh |                            |        |             |
| 0003ECh |                            |        |             |
| 0003EDh |                            |        |             |
| 0003EEh |                            |        |             |
| 0003EFh |                            |        |             |
| 0003F0h | Pull-up Control Register 0 | PUR0   | 0000 0000b  |
| 0003F1h | Pull-up Control Register 1 | PUR1   | XXXX 0000b  |
| 0003F2h | Pull-up Control Register 2 | PUR2   | 0000 0000b  |
| 0003F3h |                            |        |             |
| 0003F4h |                            |        |             |
| 0003F5h |                            |        |             |
| 0003F6h |                            |        |             |
| 0003F7h |                            |        |             |
| 0003F8h |                            |        |             |
| 0003F9h |                            |        |             |
| 0003FAh |                            |        |             |
| 0003FBh |                            |        |             |
| 0003FCh |                            |        |             |
| 0003FDh |                            |        |             |
| 0003FEh |                            |        |             |
| 0003FFh | Port Control Register      | PCR    | XXXX XXX0b  |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.17 SFR List (17)**

| Address | Register                                    | Symbol | Reset Value    |
|---------|---------------------------------------------|--------|----------------|
| 040000h | Flash Memory Control Register 0             | FMR0   | 0X01 XX00b     |
| 040001h | Flash Memory Status Register 0              | FMSR0  | 1000 0000b     |
| 040002h |                                             |        |                |
| 040003h |                                             |        |                |
| 040004h |                                             |        |                |
| 040005h |                                             |        |                |
| 040006h |                                             |        |                |
| 040007h |                                             |        |                |
| 040008h | Flash Register Protection Unlock Register 0 | FPR0   | 00h            |
| 040009h | Flash Memory Control Register 1             | FMR1   | 0000 0010b     |
| 04000Ah | Block Protect Bit Monitor Register 0        | FBPM0  | X?X? ???b (1)  |
| 04000Bh | Block Protect Bit Monitor Register 1        | FBPM1  | XXX? ?XXXb (1) |
| 04000Ch |                                             |        |                |
| 04000Dh |                                             |        |                |
| 04000Eh |                                             |        |                |
| 04000Fh |                                             |        |                |
| 040010h |                                             |        |                |
| 040011h |                                             |        |                |
| 040012h |                                             |        |                |
| 040013h |                                             |        |                |
| 040014h |                                             |        |                |
| 040015h |                                             |        |                |
| 040016h |                                             |        |                |
| 040017h |                                             |        |                |
| 040018h |                                             |        |                |
| 040019h |                                             |        |                |
| 04001Ah |                                             |        |                |
| 04001Bh |                                             |        |                |
| 04001Ch |                                             |        |                |
| 04001Dh |                                             |        |                |
| 04001Eh |                                             |        |                |
| 04001Fh |                                             |        |                |
| 040020h | PLL Control Register 0                      | PLC0   | 0000 0001b     |
| 040021h | PLL Control Register 1                      | PLC1   | 0001 1111b     |
| 040022h |                                             |        |                |
| 040023h |                                             |        |                |
| 040024h | PLL Status Register                         | PLS    | 1XXX XX00b     |
| 040025h |                                             |        |                |
| 040026h |                                             |        |                |
| 040027h |                                             |        |                |
| 040028h |                                             |        |                |
| 040029h |                                             |        |                |
| 04002Ah |                                             |        |                |
| 04002Bh |                                             |        |                |
| 04002Ch |                                             |        |                |
| 04002Dh |                                             |        |                |
| 04002Eh |                                             |        |                |
| 04002Fh |                                             |        |                |

X: Undefined

Blanks are reserved. No access is allowed.

Note:

1. The status of protect bit of each block in flash memory is reflected.

**Table 4.18 SFR List (18)**

| Address            | Register                                 | Symbol | Reset Value |
|--------------------|------------------------------------------|--------|-------------|
| 040030h to 04003Fh |                                          |        |             |
| 040040h            |                                          |        |             |
| 040041h            |                                          |        |             |
| 040042h            |                                          |        |             |
| 040043h            |                                          |        |             |
| 040044h            | Processor Mode Register 0                | PM0    | 1000 0000b  |
| 040045h            |                                          |        |             |
| 040046h            | System Clock Control Register 0          | CM0    | 0000 1000b  |
| 040047h            | System Clock Control Register 1          | CM1    | 0010 0000b  |
| 040048h            | Processor Mode Register 3                | PM3    | 00h         |
| 040049h            |                                          |        |             |
| 04004Ah            | Protect Register                         | PRCR   | XXXX X000b  |
| 04004Bh            |                                          |        |             |
| 04004Ch            | Protect Register 3                       | PRCR3  | 0000 0000b  |
| 04004Dh            | Oscillator Stop Detection Register       | CM2    | 00h         |
| 04004Eh            |                                          |        |             |
| 04004Fh            |                                          |        |             |
| 040050h            |                                          |        |             |
| 040051h            |                                          |        |             |
| 040052h            |                                          |        |             |
| 040053h            | Processor Mode Register 2                | PM2    | 00h         |
| 040054h            |                                          |        |             |
| 040055h            |                                          |        |             |
| 040056h            |                                          |        |             |
| 040057h            |                                          |        |             |
| 040058h            |                                          |        |             |
| 040059h            |                                          |        |             |
| 04005Ah            | Low Speed Mode Clock Control Register    | CM3    | XXXX XX00b  |
| 04005Bh            |                                          |        |             |
| 04005Ch            |                                          |        |             |
| 04005Dh            |                                          |        |             |
| 04005Eh            |                                          |        |             |
| 04005Fh            |                                          |        |             |
| 040060h            | Voltage Regulator Control Register       | VRCR   | 0000 0000b  |
| 040061h            |                                          |        |             |
| 040062h            | Low Voltage Detector Control Register    | LVDC   | 0000 XX00b  |
| 040063h            |                                          |        |             |
| 040064h            | Detection Voltage Configuration Register | DVCR   | 0000 XXXXb  |
| 040065h            |                                          |        |             |
| 040066h            |                                          |        |             |
| 040067h            |                                          |        |             |
| 040068h to 040093h |                                          |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.19 SFR List (19)**

| Address | Register                                   | Symbol | Reset Value |
|---------|--------------------------------------------|--------|-------------|
| 040094h |                                            |        |             |
| 040095h |                                            |        |             |
| 040096h |                                            |        |             |
| 040097h | Three-phase Output Buffer Control Register | IOBC   | 0XXX XX0Xb  |
| 040098h | Input Function Select Register 0           | IFS0   | X000 X000b  |
| 040099h | Input Function Select Register 1           | IFS1   | XXXX X0X0b  |
| 04009Ah | Input Function Select Register 2           | IFS2   | 0000 0000b  |
| 04009Bh |                                            |        |             |
| 04009Ch |                                            |        |             |
| 04009Dh | Input Function Select Register 5           | IFS5   | XXX0 X0X0b  |
| 04009Eh | Input Function Select Register 6           | IFS6   | XXXX 0000b  |
| 04009Fh |                                            |        |             |
| 0400A0h | Port P0_0 Function Select Register         | P0_0S  | 0XXX X000b  |
| 0400A1h | Port P1_0 Function Select Register         | P1_0S  | 0XXX X000b  |
| 0400A2h | Port P0_1 Function Select Register         | P0_1S  | 0XXX X000b  |
| 0400A3h | Port P1_1 Function Select Register         | P1_1S  | 0XXX X000b  |
| 0400A4h | Port P0_2 Function Select Register         | P0_2S  | 0XXX X000b  |
| 0400A5h | Port P1_2 Function Select Register         | P1_2S  | 0XXX X000b  |
| 0400A6h | Port P0_3 Function Select Register         | P0_3S  | 0XXX X000b  |
| 0400A7h | Port P1_3 Function Select Register         | P1_3S  | 0XXX X000b  |
| 0400A8h | Port P0_4 Function Select Register         | P0_4S  | 0XXX X000b  |
| 0400A9h | Port P1_4 Function Select Register         | P1_4S  | 0XXX X000b  |
| 0400AAh | Port P0_5 Function Select Register         | P0_5S  | 0XXX X000b  |
| 0400ABh | Port P1_5 Function Select Register         | P1_5S  | XXXX X000b  |
| 0400ACh | Port P0_6 Function Select Register         | P0_6S  | 0XXX X000b  |
| 0400ADh | Port P1_6 Function Select Register         | P1_6S  | XXXX X000b  |
| 0400AEh | Port P0_7 Function Select Register         | P0_7S  | 0XXX X000b  |
| 0400AFh | Port P1_7 Function Select Register         | P1_7S  | XXXX X000b  |
| 0400B0h | Port P2_0 Function Select Register         | P2_0S  | 0XXX X000b  |
| 0400B1h | Port P3_0 Function Select Register         | P3_0S  | XXXX X000b  |
| 0400B2h | Port P2_1 Function Select Register         | P2_1S  | 0XXX X000b  |
| 0400B3h | Port P3_1 Function Select Register         | P3_1S  | XXXX X000b  |
| 0400B4h | Port P2_2 Function Select Register         | P2_2S  | 0XXX X000b  |
| 0400B5h | Port P3_2 Function Select Register         | P3_2S  | XXXX X000b  |
| 0400B6h | Port P2_3 Function Select Register         | P2_3S  | 0XXX X000b  |
| 0400B7h | Port P3_3 Function Select Register         | P3_3S  | XXXX X000b  |
| 0400B8h | Port P2_4 Function Select Register         | P2_4S  | 0XXX X000b  |
| 0400B9h | Port P3_4 Function Select Register         | P3_4S  | XXXX X000b  |
| 0400BAh | Port P2_5 Function Select Register         | P2_5S  | 0XXX X000b  |
| 0400BBh | Port P3_5 Function Select Register         | P3_5S  | XXXX X000b  |
| 0400BCh | Port P2_6 Function Select Register         | P2_6S  | 0XXX X000b  |
| 0400BDh | Port P3_6 Function Select Register         | P3_6S  | XXXX X000b  |
| 0400BEh | Port P2_7 Function Select Register         | P2_7S  | 0XXX X000b  |
| 0400BFh | Port P3_7 Function Select Register         | P3_7S  | XXXX X000b  |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.20 SFR List (20)**

| Address | Register                           | Symbol | Reset Value |
|---------|------------------------------------|--------|-------------|
| 0400C0h | Port P4_0 Function Select Register | P4_0S  | XXXX X000b  |
| 0400C1h | Port P5_0 Function Select Register | P5_0S  | XXXX X000b  |
| 0400C2h | Port P4_1 Function Select Register | P4_1S  | XXXX X000b  |
| 0400C3h | Port P5_1 Function Select Register | P5_1S  | XXXX X000b  |
| 0400C4h | Port P4_2 Function Select Register | P4_2S  | XXXX X000b  |
| 0400C5h | Port P5_2 Function Select Register | P5_2S  | XXXX X000b  |
| 0400C6h | Port P4_3 Function Select Register | P4_3S  | XXXX X000b  |
| 0400C7h | Port P5_3 Function Select Register | P5_3S  | XXXX X000b  |
| 0400C8h | Port P4_4 Function Select Register | P4_4S  | XXXX X000b  |
| 0400C9h | Port P5_4 Function Select Register | P5_4S  | XXXX X000b  |
| 0400CAh | Port P4_5 Function Select Register | P4_5S  | XXXX X000b  |
| 0400CBh | Port P5_5 Function Select Register | P5_5S  | XXXX X000b  |
| 0400CCh | Port P4_6 Function Select Register | P4_6S  | XXXX X000b  |
| 0400CDh | Port P5_6 Function Select Register | P5_6S  | XXXX X000b  |
| 0400CEh | Port P4_7 Function Select Register | P4_7S  | XXXX X000b  |
| 0400CFh | Port P5_7 Function Select Register | P5_7S  | XXXX X000b  |
| 0400D0h |                                    |        |             |
| 0400D1h | Port P7_0 Function Select Register | P7_0S  | XXXX X000b  |
| 0400D2h |                                    |        |             |
| 0400D3h |                                    |        |             |
| 0400D4h |                                    |        |             |
| 0400D5h |                                    |        |             |
| 0400D6h |                                    |        |             |
| 0400D7h |                                    |        |             |
| 0400D8h |                                    |        |             |
| 0400D9h | Port P7_4 Function Select Register | P7_4S  | XXXX X000b  |
| 0400DAh | Port P6_5 Function Select Register | P6_5S  | XXXX X000b  |
| 0400DBh | Port P7_5 Function Select Register | P7_5S  | XXXX X000b  |
| 0400DCh |                                    |        |             |
| 0400DDh | Port P7_6 Function Select Register | P7_6S  | XXXX X000b  |
| 0400DEh | Port P6_7 Function Select Register | P6_7S  | XXXX X000b  |
| 0400DFh |                                    |        |             |
| 0400E0h |                                    |        |             |
| 0400E1h |                                    |        |             |
| 0400E2h |                                    |        |             |
| 0400E3h |                                    |        |             |
| 0400E4h | Port P8_2 Function Select Register | P8_2S  | XXXX X000b  |
| 0400E5h |                                    |        |             |
| 0400E6h | Port P8_3 Function Select Register | P8_3S  | XXXX X000b  |
| 0400E7h | Port P9_3 Function Select Register | P9_3S  | 0XXX X000b  |
| 0400E8h | Port P8_4 Function Select Register | P8_4S  | XXXX X000b  |
| 0400E9h | Port P9_4 Function Select Register | P9_4S  | 0XXX X000b  |
| 0400EAh |                                    |        |             |
| 0400EBh | Port P9_5 Function Select Register | P9_5S  | 0XXX X000b  |
| 0400ECh | Port P8_6 Function Select Register | P8_6S  | XXXX X000b  |
| 0400EDh | Port P9_6 Function Select Register | P9_6S  | 0XXX X000b  |
| 0400EEh | Port P8_7 Function Select Register | P8_7S  | XXXX X000b  |
| 0400EFh | Port P9_7 Function Select Register | P9_7S  | XXXX X000b  |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.21 SFR List (21)**

| Address            | Register                              | Symbol | Reset Value |
|--------------------|---------------------------------------|--------|-------------|
| 0400F0h to 04403Fh |                                       |        |             |
| 044040h            |                                       |        |             |
| 044041h            |                                       |        |             |
| 044042h            |                                       |        |             |
| 044043h            |                                       |        |             |
| 044044h            |                                       |        |             |
| 044045h            |                                       |        |             |
| 044046h            |                                       |        |             |
| 044047h            |                                       |        |             |
| 044048h            |                                       |        |             |
| 044049h            |                                       |        |             |
| 04404Ah            |                                       |        |             |
| 04404Bh            |                                       |        |             |
| 04404Ch            | Protect Register 4                    | PRCR4  | 0000 0000b  |
| 04404Dh            | Watchdog Timer Clock Control Register | WDK    | 0000 0000b  |
| 04404Eh            | Watchdog Timer Start Register         | WDTS   | XXXX XXXXb  |
| 04404Fh            | Watchdog Timer Control Register       | WDC    | 000X XXXXb  |
| 044050h            |                                       |        |             |
| 044051h            |                                       |        |             |
| 044052h            |                                       |        |             |
| 044053h            |                                       |        |             |
| 044054h            |                                       |        |             |
| 044055h            |                                       |        |             |
| 044056h            |                                       |        |             |
| 044057h            |                                       |        |             |
| 044058h            |                                       |        |             |
| 044059h            |                                       |        |             |
| 04405Ah            |                                       |        |             |
| 04405Bh            |                                       |        |             |
| 04405Ch            |                                       |        |             |
| 04405Dh            |                                       |        |             |
| 04405Eh            |                                       |        |             |
| 04405Fh            | Protect Register 2                    | PRCR2  | 0XXX XXXXb  |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.22 SFR List (22)**

| Address | Register                                          | Symbol | Reset Value |
|---------|---------------------------------------------------|--------|-------------|
| 044060h |                                                   |        |             |
| 044061h |                                                   |        |             |
| 044062h |                                                   |        |             |
| 044063h |                                                   |        |             |
| 044064h |                                                   |        |             |
| 044065h |                                                   |        |             |
| 044066h |                                                   |        |             |
| 044067h |                                                   |        |             |
| 044068h |                                                   |        |             |
| 044069h |                                                   |        |             |
| 04406Ah |                                                   |        |             |
| 04406Bh |                                                   |        |             |
| 04406Ch |                                                   |        |             |
| 04406Dh |                                                   |        |             |
| 04406Eh |                                                   |        |             |
| 04406Fh | External Interrupt Source Select Register 0       | IFSR0  | 0000 0000b  |
| 044070h | DMA0 Request Source Select Register 2             | DM0SL2 | XX00 0000b  |
| 044071h | DMA1 Request Source Select Register 2             | DM1SL2 | XX00 0000b  |
| 044072h | DMA2 Request Source Select Register 2             | DM2SL2 | XX00 0000b  |
| 044073h | DMA3 Request Source Select Register 2             | DM3SL2 | XX00 0000b  |
| 044074h |                                                   |        |             |
| 044075h |                                                   |        |             |
| 044076h |                                                   |        |             |
| 044077h |                                                   |        |             |
| 044078h | DMA0 Request Source Select Register               | DM0SL  | XXX0 0000b  |
| 044079h | DMA1 Request Source Select Register               | DM1SL  | XXX0 0000b  |
| 04407Ah | DMA2 Request Source Select Register               | DM2SL  | XXX0 0000b  |
| 04407Bh | DMA3 Request Source Select Register               | DM3SL  | XXX0 0000b  |
| 04407Ch |                                                   |        |             |
| 04407Dh | Wake-up IPL Setting Register 2                    | RIPL2  | XX0X 0000b  |
| 04407Eh |                                                   |        |             |
| 04407Fh | Wake-up IPL Setting Register 1                    | RIPL1  | XX0X 0000b  |
| 044080h | External Interrupt Input Filter Select Register 0 | INTF0  | 0000 0000b  |
| 044081h |                                                   |        |             |
| 044082h | External Interrupt Input Filter Select Register 1 | INTF1  | 0000 0000b  |
| 044083h |                                                   |        |             |
| 044084h |                                                   |        |             |
| 044085h |                                                   |        |             |
| 044086h |                                                   |        |             |
| 044087h |                                                   |        |             |
| 044088h |                                                   |        |             |
| 044089h |                                                   |        |             |
| 04408Ah |                                                   |        |             |
| 04408Bh |                                                   |        |             |
| 04408Ch |                                                   |        |             |
| 04408Dh |                                                   |        |             |
| 04408Eh |                                                   |        |             |
| 04408Fh |                                                   |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.23 SFR List (23)**

| Address            | Register                                                             | Symbol | Reset Value |
|--------------------|----------------------------------------------------------------------|--------|-------------|
| 044090h to 044DFFh |                                                                      |        |             |
| 044E00h            | LIN Channel Window Select/Input Signal Low Detection Status Register | LCW    | 0000 0000b  |
| 044E01h            | LIN Baud Rate Generator Control Register                             | LBRG   | 0000 0000b  |
| 044E02h            | LIN Baud Rate Prescaler 0                                            | LBRP0  | 00h         |
| 044E03h            | LIN Baud Rate Prescaler 1                                            | LBRP1  | 00h         |
| 044E04h            | LIN Mode Register 0                                                  | LMD0   | 0000 0000b  |
| 044E05h            | LIN Mode Register 1                                                  | LMD1   | 00h         |
| 044E06h            | LIN Wake-up Setting Register                                         | LWUP   | 00h         |
| 044E07h            |                                                                      |        |             |
| 044E08h            | LIN Break Field Setting Register                                     | LBRK   | 0000 0000b  |
| 044E09h            | LIN Space Setting Register                                           | LSPC   | 0000 0000b  |
| 044E0Ah            | LIN Response Field Setting Register                                  | LRFC   | 0000 0000b  |
| 044E0Bh            | LIN ID Buffer Register                                               | LIDB   | 00h         |
| 044E0Ch            | LIN Status Control Register                                          | LSC    | 0000 0000b  |
| 044E0Dh            | LIN Transmission Control Register                                    | LTC    | 0000 0000b  |
| 044E0Eh            | LIN Status Register                                                  | LST    | 0000 0000b  |
| 044E0Fh            | LIN Error Status Register                                            | LEST   | 0000 0000b  |
| 044E10h            | LIN Data 1 Buffer Register                                           | LDB1   | 00h         |
| 044E11h            | LIN Data 2 Buffer Register                                           | LDB2   | 00h         |
| 044E12h            | LIN Data 3 Buffer Register                                           | LDB3   | 00h         |
| 044E13h            | LIN Data 4 Buffer Register                                           | LDB4   | 00h         |
| 044E14h            | LIN Data 5 Buffer Register                                           | LDB5   | 00h         |
| 044E15h            | LIN Data 6 Buffer Register                                           | LDB6   | 00h         |
| 044E16h            | LIN Data 7 Buffer Register                                           | LDB7   | 00h         |
| 044E17h            | LIN Data 8 Buffer Register                                           | LDB8   | 00h         |
| 044E18h            |                                                                      |        |             |
| 044E19h            |                                                                      |        |             |
| 044E1Ah            |                                                                      |        |             |
| 044E1Bh            |                                                                      |        |             |
| 044E1Ch            |                                                                      |        |             |
| 044E1Dh            |                                                                      |        |             |
| 044E1Eh            |                                                                      |        |             |
| 044E1Fh            |                                                                      |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.24 SFR List (24)**

| Address            | Register                       | Symbol     | Reset Value |
|--------------------|--------------------------------|------------|-------------|
| 044E20h to 044EFFh |                                |            |             |
| 044F00h            |                                |            |             |
| 044F01h            |                                |            |             |
| 044F02h            |                                |            |             |
| 044F03h            |                                |            |             |
| 044F04h            |                                |            |             |
| 044F05h            |                                |            |             |
| 044F06h            | SS0 Receive Data Register      | SS0RDR     | FFh         |
| 044F07h            | SS0 Receive Data Register (H)  | SS0RDR (H) | FFh         |
| 044F08h            | SS0 Control Register H         | SS0CRH     | 00h         |
| 044F09h            | SS0 Control Register L         | SS0CRL     | 0111 1101b  |
| 044F0Ah            | SS0 Mode Register              | SS0MR      | 0001 0000b  |
| 044F0Bh            | SS0 Enable Register            | SS0ER      | 00h         |
| 044F0Ch            | SS0 Status Register            | SS0SR      | 00h         |
| 044F0Dh            | SS0 Mode Register 2            | SS0MR2     | 00h         |
| 044F0Eh            | SS0 Transmit Data Register     | SS0TDR     | FFh         |
| 044F0Fh            | SS0 Transmit Data Register (H) | SS0TDR (H) | FFh         |
| 044F10h            |                                |            |             |
| 044F11h            |                                |            |             |
| 044F12h            |                                |            |             |
| 044F13h            |                                |            |             |
| 044F14h            |                                |            |             |
| 044F15h            |                                |            |             |
| 044F16h            |                                |            |             |
| 044F17h            |                                |            |             |
| 044F18h            |                                |            |             |
| 044F19h            |                                |            |             |
| 044F1Ah            |                                |            |             |
| 044F1Bh            |                                |            |             |
| 044F1Ch            |                                |            |             |
| 044F1Dh            |                                |            |             |
| 044F1Eh            |                                |            |             |
| 044F1Fh            |                                |            |             |
| 044F20h            |                                |            |             |
| 044F21h            |                                |            |             |
| 044F22h            |                                |            |             |
| 044F23h            |                                |            |             |
| 044F24h            |                                |            |             |
| 044F25h            |                                |            |             |
| 044F26h            |                                |            |             |
| 044F27h            |                                |            |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.25 SFR List (25)**

| Address                                                                                                                          | Register                                      | Symbol | Reset Value |
|----------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|--------|-------------|
| 044F28h to<br>044FDFh                                                                                                            |                                               |        |             |
| 044FE0h<br>044FE1h<br>044FE2h<br>044FE3h<br>044FE4h<br>044FE5h<br>044FE6h<br>044FE7h                                             | E <sup>2</sup> dataFlash Address Register     | E2FA   | XXXX 0000h  |
| 044FE8h<br>044FE9h<br>044FEAh<br>044FEBh                                                                                         | E <sup>2</sup> dataFlash Instruction Register | E2FI   | XX00h       |
| 044FEC<br>044FEDh<br>044FEEh<br>044FEFh                                                                                          | E <sup>2</sup> dataFlash Data Register        | E2FD   | XXXXh       |
| 044FF0h<br>044FF1h                                                                                                               | E <sup>2</sup> dataFlash Mode Register        | E2FM   | 0000 0000b  |
| 044FF2h<br>044FF3h                                                                                                               | E <sup>2</sup> dataFlash Control Register     | E2FC   | XXXX XXX0b  |
| 044FF4h<br>044FF5h<br>044FF6h<br>044FF7h<br>044FF8h<br>044FF9h<br>044FFAh<br>044FFBh<br>044FFCh<br>044FFDh<br>044FFEh<br>044FFFh | E <sup>2</sup> dataFlash Status Register 1    | E2FS1  | XXXX XXX0b  |
| 045000h                                                                                                                          |                                               |        |             |
| 045001h<br>045002h<br>045003h<br>045004h<br>045005h<br>045006h<br>045007h                                                        | E <sup>2</sup> dataFlash Status Register 0    | E2FS0  | XXXX XXXXb  |
| 045008h to<br>045FFFh                                                                                                            |                                               |        |             |
| 046000h to<br>0467FFh                                                                                                            |                                               |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.26 SFR List (26)**

| Address            | Register                           | Symbol | Reset Value             |
|--------------------|------------------------------------|--------|-------------------------|
| 046800h to 0477FFh |                                    |        |                         |
| 047800h            | CAN1 Mailbox 0: Message Identifier | C1MB0  | XXXX XXXXh              |
| 047801h            |                                    |        |                         |
| 047802h            |                                    |        |                         |
| 047803h            |                                    |        |                         |
| 047804h            |                                    |        |                         |
| 047805h            | CAN1 Mailbox 0: Data Length        |        | XXh                     |
| 047806h            | CAN1 Mailbox 0: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047807h            |                                    |        |                         |
| 047808h            |                                    |        |                         |
| 047809h            |                                    |        |                         |
| 04780Ah            |                                    |        |                         |
| 04780Bh            |                                    |        |                         |
| 04780Ch            |                                    |        |                         |
| 04780Dh            |                                    |        |                         |
| 04780Eh            | CAN1 Mailbox 0: Time Stamp         |        | XXXXh                   |
| 04780Fh            |                                    |        |                         |
| 047810h            | CAN1 Mailbox 1: Message Identifier | C1MB1  | XXXX XXXXh              |
| 047811h            |                                    |        |                         |
| 047812h            |                                    |        |                         |
| 047813h            |                                    |        |                         |
| 047814h            |                                    |        |                         |
| 047815h            | CAN1 Mailbox 1: Data Length        |        | XXh                     |
| 047816h            | CAN1 Mailbox 1: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047817h            |                                    |        |                         |
| 047818h            |                                    |        |                         |
| 047819h            |                                    |        |                         |
| 04781Ah            |                                    |        |                         |
| 04781Bh            |                                    |        |                         |
| 04781Ch            |                                    |        |                         |
| 04781Dh            |                                    |        |                         |
| 04781Eh            | CAN1 Mailbox 1: Time Stamp         |        | XXXXh                   |
| 04781Fh            |                                    |        |                         |
| 047820h            | CAN1 Mailbox 2: Message Identifier | C1MB2  | XXXX XXXXh              |
| 047821h            |                                    |        |                         |
| 047822h            |                                    |        |                         |
| 047823h            |                                    |        |                         |
| 047824h            |                                    |        |                         |
| 047825h            | CAN1 Mailbox 2: Data Length        |        | XXh                     |
| 047826h            | CAN1 Mailbox 2: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047827h            |                                    |        |                         |
| 047828h            |                                    |        |                         |
| 047829h            |                                    |        |                         |
| 04782Ah            |                                    |        |                         |
| 04782Bh            |                                    |        |                         |
| 04782Ch            |                                    |        |                         |
| 04782Dh            |                                    |        |                         |
| 04782Eh            | CAN1 Mailbox 2: Time Stamp         |        | XXXXh                   |
| 04782Fh            |                                    |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.27 SFR List (27)**

| Address | Register                           | Symbol | Reset Value             |
|---------|------------------------------------|--------|-------------------------|
| 047830h | CAN1 Mailbox 3: Message Identifier | C1MB3  | XXXX XXXXh              |
| 047831h |                                    |        |                         |
| 047832h |                                    |        |                         |
| 047833h |                                    |        |                         |
| 047834h |                                    |        |                         |
| 047835h | CAN1 Mailbox 3: Data Length        |        | XXh                     |
| 047836h | CAN1 Mailbox 3: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047837h |                                    |        |                         |
| 047838h |                                    |        |                         |
| 047839h |                                    |        |                         |
| 04783Ah |                                    |        |                         |
| 04783Bh |                                    |        |                         |
| 04783Ch |                                    |        |                         |
| 04783Dh |                                    |        |                         |
| 04783Eh | CAN1 Mailbox 3: Time Stamp         |        | XXXXh                   |
| 04783Fh |                                    |        |                         |
| 047840h | CAN1 Mailbox 4: Message Identifier | C1MB4  | XXXX XXXXh              |
| 047841h |                                    |        |                         |
| 047842h |                                    |        |                         |
| 047843h |                                    |        |                         |
| 047844h |                                    |        |                         |
| 047845h | CAN1 Mailbox 4: Data Length        |        | XXh                     |
| 047846h | CAN1 Mailbox 4: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047847h |                                    |        |                         |
| 047848h |                                    |        |                         |
| 047849h |                                    |        |                         |
| 04784Ah |                                    |        |                         |
| 04784Bh |                                    |        |                         |
| 04784Ch |                                    |        |                         |
| 04784Dh |                                    |        |                         |
| 04784Eh | CAN1 Mailbox 4: Time Stamp         |        | XXXXh                   |
| 04784Fh |                                    |        |                         |
| 047850h | CAN1 Mailbox 5: Message Identifier | C1MB5  | XXXX XXXXh              |
| 047851h |                                    |        |                         |
| 047852h |                                    |        |                         |
| 047853h |                                    |        |                         |
| 047854h |                                    |        |                         |
| 047855h | CAN1 Mailbox 5: Data Length        |        | XXh                     |
| 047856h | CAN1 Mailbox 5: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047857h |                                    |        |                         |
| 047858h |                                    |        |                         |
| 047859h |                                    |        |                         |
| 04785Ah |                                    |        |                         |
| 04785Bh |                                    |        |                         |
| 04785Ch |                                    |        |                         |
| 04785Dh |                                    |        |                         |
| 04785Eh | CAN1 Mailbox 5: Time Stamp         |        | XXXXh                   |
| 04785Fh |                                    |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.28 SFR List (28)**

| Address | Register                           | Symbol | Reset Value             |
|---------|------------------------------------|--------|-------------------------|
| 047860h | CAN1 Mailbox 6: Message Identifier | C1MB6  | XXXX XXXXh              |
| 047861h |                                    |        |                         |
| 047862h |                                    |        |                         |
| 047863h |                                    |        |                         |
| 047864h |                                    |        |                         |
| 047865h | CAN1 Mailbox 6: Data Length        |        | XXh                     |
| 047866h | CAN1 Mailbox 6: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047867h |                                    |        |                         |
| 047868h |                                    |        |                         |
| 047869h |                                    |        |                         |
| 04786Ah |                                    |        |                         |
| 04786Bh |                                    |        |                         |
| 04786Ch |                                    |        |                         |
| 04786Dh |                                    |        |                         |
| 04786Eh | CAN1 Mailbox 6: Time Stamp         |        | XXXXh                   |
| 04786Fh |                                    |        |                         |
| 047870h | CAN1 Mailbox 7: Message Identifier | C1MB7  | XXXX XXXXh              |
| 047871h |                                    |        |                         |
| 047872h |                                    |        |                         |
| 047873h |                                    |        |                         |
| 047874h |                                    |        |                         |
| 047875h | CAN1 Mailbox 7: Data Length        |        | XXh                     |
| 047876h | CAN1 Mailbox 7: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047877h |                                    |        |                         |
| 047878h |                                    |        |                         |
| 047879h |                                    |        |                         |
| 04787Ah |                                    |        |                         |
| 04787Bh |                                    |        |                         |
| 04787Ch |                                    |        |                         |
| 04787Dh |                                    |        |                         |
| 04787Eh | CAN1 Mailbox 7: Time Stamp         |        | XXXXh                   |
| 04787Fh |                                    |        |                         |
| 047880h | CAN1 Mailbox 8: Message Identifier | C1MB8  | XXXX XXXXh              |
| 047881h |                                    |        |                         |
| 047882h |                                    |        |                         |
| 047883h |                                    |        |                         |
| 047884h |                                    |        |                         |
| 047885h | CAN1 Mailbox 8: Data Length        |        | XXh                     |
| 047886h | CAN1 Mailbox 8: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047887h |                                    |        |                         |
| 047888h |                                    |        |                         |
| 047889h |                                    |        |                         |
| 04788Ah |                                    |        |                         |
| 04788Bh |                                    |        |                         |
| 04788Ch |                                    |        |                         |
| 04788Dh |                                    |        |                         |
| 04788Eh | CAN1 Mailbox 8: Time Stamp         |        | XXXXh                   |
| 04788Fh |                                    |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.29 SFR List (29)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 047890h | CAN1 Mailbox 9: Message Identifier  | C1MB9  | XXXX XXXXh              |
| 047891h |                                     |        |                         |
| 047892h |                                     |        |                         |
| 047893h |                                     |        |                         |
| 047894h |                                     |        |                         |
| 047895h | CAN1 Mailbox 9: Data Length         |        | XXh                     |
| 047896h | CAN1 Mailbox 9: Data Field          |        | XXXX XXXX<br>XXXX XXXXh |
| 047897h |                                     |        |                         |
| 047898h |                                     |        |                         |
| 047899h |                                     |        |                         |
| 04789Ah |                                     |        |                         |
| 04789Bh |                                     |        |                         |
| 04789Ch |                                     |        |                         |
| 04789Dh |                                     |        |                         |
| 04789Eh | CAN1 Mailbox 9: Time Stamp          |        | XXXXh                   |
| 04789Fh |                                     |        |                         |
| 0478A0h | CAN1 Mailbox 10: Message Identifier | C1MB10 | XXXX XXXXh              |
| 0478A1h |                                     |        |                         |
| 0478A2h |                                     |        |                         |
| 0478A3h |                                     |        |                         |
| 0478A4h |                                     |        |                         |
| 0478A5h | CAN1 Mailbox 10: Data Length        |        | XXh                     |
| 0478A6h | CAN1 Mailbox 10: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0478A7h |                                     |        |                         |
| 0478A8h |                                     |        |                         |
| 0478A9h |                                     |        |                         |
| 0478AAh |                                     |        |                         |
| 0478ABh |                                     |        |                         |
| 0478ACh |                                     |        |                         |
| 0478ADh |                                     |        |                         |
| 0478AEh | CAN1 Mailbox 10: Time Stamp         |        | XXXXh                   |
| 0478AFh |                                     |        |                         |
| 0478B0h | CAN1 Mailbox 11: Message Identifier | C1MB11 | XXXX XXXXh              |
| 0478B1h |                                     |        |                         |
| 0478B2h |                                     |        |                         |
| 0478B3h |                                     |        |                         |
| 0478B4h |                                     |        |                         |
| 0478B5h | CAN1 Mailbox 11: Data Length        |        | XXh                     |
| 0478B6h | CAN1 Mailbox 11: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0478B7h |                                     |        |                         |
| 0478B8h |                                     |        |                         |
| 0478B9h |                                     |        |                         |
| 0478BAh |                                     |        |                         |
| 0478BBh |                                     |        |                         |
| 0478BCh |                                     |        |                         |
| 0478BDh |                                     |        |                         |
| 0478BEh | CAN1 Mailbox 11: Time Stamp         |        | XXXXh                   |
| 0478BFh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.30 SFR List (30)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 0478C0h | CAN1 Mailbox 12: Message Identifier | C1MB12 | XXXX XXXXh              |
| 0478C1h |                                     |        |                         |
| 0478C2h |                                     |        |                         |
| 0478C3h |                                     |        |                         |
| 0478C4h |                                     |        |                         |
| 0478C5h | CAN1 Mailbox 12: Data Length        |        | XXh                     |
| 0478C6h | CAN1 Mailbox 12: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0478C7h |                                     |        |                         |
| 0478C8h |                                     |        |                         |
| 0478C9h |                                     |        |                         |
| 0478CAh |                                     |        |                         |
| 0478CBh |                                     |        |                         |
| 0478CCh |                                     |        |                         |
| 0478CDh |                                     |        |                         |
| 0478CEh | CAN1 Mailbox 12: Time Stamp         |        | XXXXh                   |
| 0478CFh |                                     |        |                         |
| 0478D0h | CAN1 Mailbox 13: Message Identifier | C1MB13 | XXXX XXXXh              |
| 0478D1h |                                     |        |                         |
| 0478D2h |                                     |        |                         |
| 0478D3h |                                     |        |                         |
| 0478D4h |                                     |        |                         |
| 0478D5h | CAN1 Mailbox 13: Data Length        |        | XXh                     |
| 0478D6h | CAN1 Mailbox 13: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0478D7h |                                     |        |                         |
| 0478D8h |                                     |        |                         |
| 0478D9h |                                     |        |                         |
| 0478DAh |                                     |        |                         |
| 0478DBh |                                     |        |                         |
| 0478DCh |                                     |        |                         |
| 0478DDh |                                     |        |                         |
| 0478DEh | CAN1 Mailbox 13: Time Stamp         |        | XXXXh                   |
| 0478DFh |                                     |        |                         |
| 0478E0h | CAN1 Mailbox 14: Message Identifier | C1MB14 | XXXX XXXXh              |
| 0478E1h |                                     |        |                         |
| 0478E2h |                                     |        |                         |
| 0478E3h |                                     |        |                         |
| 0478E4h |                                     |        |                         |
| 0478E5h | CAN1 Mailbox 14: Data Length        |        | XXh                     |
| 0478E6h | CAN1 Mailbox 14: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0478E7h |                                     |        |                         |
| 0478E8h |                                     |        |                         |
| 0478E9h |                                     |        |                         |
| 0478EAh |                                     |        |                         |
| 0478EBh |                                     |        |                         |
| 0478ECh |                                     |        |                         |
| 0478EDh |                                     |        |                         |
| 0478EEh | CAN1 Mailbox 14: Time Stamp         |        | XXXXh                   |
| 0478EFh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.31 SFR List (31)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 0478F0h | CAN1 Mailbox 15: Message Identifier | C1MB15 | XXXX XXXXh              |
| 0478F1h |                                     |        |                         |
| 0478F2h |                                     |        |                         |
| 0478F3h |                                     |        |                         |
| 0478F4h |                                     |        |                         |
| 0478F5h | CAN1 Mailbox 15: Data Length        |        | XXh                     |
| 0478F6h | CAN1 Mailbox 15: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0478F7h |                                     |        |                         |
| 0478F8h |                                     |        |                         |
| 0478F9h |                                     |        |                         |
| 0478FAh |                                     |        |                         |
| 0478FBh |                                     |        |                         |
| 0478FCh |                                     |        |                         |
| 0478FDh |                                     |        |                         |
| 0478FEh | CAN1 Mailbox 15: Time Stamp         |        | XXXXh                   |
| 0478FFh |                                     |        |                         |
| 047900h | CAN1 Mailbox 16: Message Identifier | C1MB16 | XXXX XXXXh              |
| 047901h |                                     |        |                         |
| 047902h |                                     |        |                         |
| 047903h |                                     |        |                         |
| 047904h |                                     |        |                         |
| 047905h | CAN1 Mailbox 16: Data Length        |        | XXh                     |
| 047906h | CAN1 Mailbox 16: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047907h |                                     |        |                         |
| 047908h |                                     |        |                         |
| 047909h |                                     |        |                         |
| 04790Ah |                                     |        |                         |
| 04790Bh |                                     |        |                         |
| 04790Ch |                                     |        |                         |
| 04790Dh |                                     |        |                         |
| 04790Eh | CAN1 Mailbox 16: Time Stamp         |        | XXXXh                   |
| 04790Fh |                                     |        |                         |
| 047910h | CAN1 Mailbox 17: Message Identifier | C1MB17 | XXXX XXXXh              |
| 047911h |                                     |        |                         |
| 047912h |                                     |        |                         |
| 047913h |                                     |        |                         |
| 047914h |                                     |        |                         |
| 047915h | CAN1 Mailbox 17: Data Length        |        | XXh                     |
| 047916h | CAN1 Mailbox 17: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047917h |                                     |        |                         |
| 047918h |                                     |        |                         |
| 047919h |                                     |        |                         |
| 04791Ah |                                     |        |                         |
| 04791Bh |                                     |        |                         |
| 04791Ch |                                     |        |                         |
| 04791Dh |                                     |        |                         |
| 04791Eh | CAN1 Mailbox 17: Time Stamp         |        | XXXXh                   |
| 04791Fh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.32 SFR List (32)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 047920h | CAN1 Mailbox 18: Message Identifier | C1MB18 | XXXX XXXXh              |
| 047921h |                                     |        |                         |
| 047922h |                                     |        |                         |
| 047923h |                                     |        |                         |
| 047924h |                                     |        |                         |
| 047925h | CAN1 Mailbox 18: Data Length        |        | XXh                     |
| 047926h | CAN1 Mailbox 18: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047927h |                                     |        |                         |
| 047928h |                                     |        |                         |
| 047929h |                                     |        |                         |
| 04792Ah |                                     |        |                         |
| 04792Bh |                                     |        |                         |
| 04792Ch |                                     |        |                         |
| 04792Dh |                                     |        |                         |
| 04792Eh | CAN1 Mailbox18: Time Stamp          |        | XXXXh                   |
| 04792Fh |                                     |        |                         |
| 047930h | CAN1 Mailbox 19: Message Identifier | C1MB19 | XXXX XXXXh              |
| 047931h |                                     |        |                         |
| 047932h |                                     |        |                         |
| 047933h |                                     |        |                         |
| 047934h |                                     |        |                         |
| 047935h | CAN1 Mailbox 19: Data Length        |        | XXh                     |
| 047936h | CAN1 Mailbox 19: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047937h |                                     |        |                         |
| 047938h |                                     |        |                         |
| 047939h |                                     |        |                         |
| 04793Ah |                                     |        |                         |
| 04793Bh |                                     |        |                         |
| 04793Ch |                                     |        |                         |
| 04793Dh |                                     |        |                         |
| 04793Eh | CAN1 Mailbox 19: Time Stamp         |        | XXXXh                   |
| 04793Fh |                                     |        |                         |
| 047940h | CAN1 Mailbox 20: Message Identifier | C1MB20 | XXXX XXXXh              |
| 047941h |                                     |        |                         |
| 047942h |                                     |        |                         |
| 047943h |                                     |        |                         |
| 047944h |                                     |        |                         |
| 047945h | CAN1 Mailbox 20: Data Length        |        | XXh                     |
| 047946h | CAN1 Mailbox 20: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047947h |                                     |        |                         |
| 047948h |                                     |        |                         |
| 047949h |                                     |        |                         |
| 04794Ah |                                     |        |                         |
| 04794Bh |                                     |        |                         |
| 04794Ch |                                     |        |                         |
| 04794Dh |                                     |        |                         |
| 04794Eh | CAN1 Mailbox 20: Time Stamp         |        | XXXXh                   |
| 04794Fh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.33 SFR List (33)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 047950h | CAN1 Mailbox 21: Message Identifier | C1MB21 | XXXX XXXXh              |
| 047951h |                                     |        |                         |
| 047952h |                                     |        |                         |
| 047953h |                                     |        |                         |
| 047954h |                                     |        |                         |
| 047955h | CAN1 Mailbox 21: Data Length        |        | XXh                     |
| 047956h | CAN1 Mailbox 21: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047957h |                                     |        |                         |
| 047958h |                                     |        |                         |
| 047959h |                                     |        |                         |
| 04795Ah |                                     |        |                         |
| 04795Bh |                                     |        |                         |
| 04795Ch |                                     |        |                         |
| 04795Dh |                                     |        |                         |
| 04795Eh | CAN1 Mailbox 21: Time Stamp         | C1MB22 | XXXXh                   |
| 04795Fh |                                     |        |                         |
| 047960h | CAN1 Mailbox 22: Identifier         |        | XXXX XXXXh              |
| 047961h |                                     |        |                         |
| 047962h |                                     |        |                         |
| 047963h |                                     |        |                         |
| 047964h |                                     |        |                         |
| 047965h | CAN1 Mailbox 22: Data Length        |        | XXh                     |
| 047966h | CAN1 Mailbox 22: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047967h |                                     |        |                         |
| 047968h |                                     |        |                         |
| 047969h |                                     |        |                         |
| 04796Ah |                                     |        |                         |
| 04796Bh |                                     |        |                         |
| 04796Ch |                                     |        |                         |
| 04796Dh |                                     |        |                         |
| 04796Eh | CAN1 Mailbox 22: Time Stamp         | C1MB23 | XXXXh                   |
| 04796Fh |                                     |        |                         |
| 047970h | CAN1 Mailbox 23: Message Identifier |        | XXXX XXXXh              |
| 047971h |                                     |        |                         |
| 047972h |                                     |        |                         |
| 047973h |                                     |        |                         |
| 047974h |                                     |        |                         |
| 047975h | CAN1 Mailbox 23: Data Length        |        | XXh                     |
| 047976h | CAN1 Mailbox 23: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047977h |                                     |        |                         |
| 047978h |                                     |        |                         |
| 047979h |                                     |        |                         |
| 04797Ah |                                     |        |                         |
| 04797Bh |                                     |        |                         |
| 04797Ch |                                     |        |                         |
| 04797Dh |                                     |        |                         |
| 04797Eh | CAN1 Mailbox 23: Time Stamp         |        | XXXXh                   |
| 04797Fh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.34 SFR List (34)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 047980h | CAN1 Mailbox 24: Message Identifier | C1MB24 | XXXX XXXXh              |
| 047981h |                                     |        |                         |
| 047982h |                                     |        |                         |
| 047983h |                                     |        |                         |
| 047984h |                                     |        |                         |
| 047985h | CAN1 Mailbox 24: Data Length        |        | XXh                     |
| 047986h | CAN1 Mailbox 24: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047987h |                                     |        |                         |
| 047988h |                                     |        |                         |
| 047989h |                                     |        |                         |
| 04798Ah |                                     |        |                         |
| 04798Bh |                                     |        |                         |
| 04798Ch |                                     |        |                         |
| 04798Dh |                                     |        |                         |
| 04798Eh | CAN1 Mailbox 24: Time Stamp         |        | XXXXh                   |
| 04798Fh |                                     |        |                         |
| 047990h | CAN1 Mailbox 25: Message Identifier | C1MB25 | XXXX XXXXh              |
| 047991h |                                     |        |                         |
| 047992h |                                     |        |                         |
| 047993h |                                     |        |                         |
| 047994h |                                     |        |                         |
| 047995h | CAN1 Mailbox 25: Data Length        |        | XXh                     |
| 047996h | CAN1 Mailbox 25: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047997h |                                     |        |                         |
| 047998h |                                     |        |                         |
| 047999h |                                     |        |                         |
| 04799Ah |                                     |        |                         |
| 04799Bh |                                     |        |                         |
| 04799Ch |                                     |        |                         |
| 04799Dh |                                     |        |                         |
| 04799Eh | CAN1 Mailbox 25: Time Stamp         |        | XXXXh                   |
| 04799Fh |                                     |        |                         |
| 0479A0h | CAN1 Mailbox 26: Message Identifier | C1MB26 | XXXX XXXXh              |
| 0479A1h |                                     |        |                         |
| 0479A2h |                                     |        |                         |
| 0479A3h |                                     |        |                         |
| 0479A4h |                                     |        |                         |
| 0479A5h | CAN1 Mailbox 26: Data Length        |        | XXh                     |
| 0479A6h | CAN1 Mailbox 26: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0479A7h |                                     |        |                         |
| 0479A8h |                                     |        |                         |
| 0479A9h |                                     |        |                         |
| 0479AAh |                                     |        |                         |
| 0479ABh |                                     |        |                         |
| 0479ACh |                                     |        |                         |
| 0479ADh |                                     |        |                         |
| 0479AEh | CAN1 Mailbox 26: Time Stamp         |        | XXXXh                   |
| 0479AFh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.35 SFR List (35)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 0479B0h | CAN1 Mailbox 27: Message Identifier | C1MB27 | XXXX XXXXh              |
| 0479B1h |                                     |        |                         |
| 0479B2h |                                     |        |                         |
| 0479B3h |                                     |        |                         |
| 0479B4h |                                     |        |                         |
| 0479B5h | CAN1 Mailbox 27: Data Length        |        | XXh                     |
| 0479B6h | CAN1 Mailbox 27: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0479B7h |                                     |        |                         |
| 0479B8h |                                     |        |                         |
| 0479B9h |                                     |        |                         |
| 0479BAh |                                     |        |                         |
| 0479BBh |                                     |        |                         |
| 0479BCh |                                     |        |                         |
| 0479BDh |                                     |        |                         |
| 0479BEh | CAN1 Mailbox 27: Time Stamp         |        | XXXXh                   |
| 0479BFh |                                     |        |                         |
| 0479C0h | CAN1 Mailbox 28: Message Identifier | C1MB28 | XXXX XXXXh              |
| 0479C1h |                                     |        |                         |
| 0479C2h |                                     |        |                         |
| 0479C3h |                                     |        |                         |
| 0479C4h |                                     |        |                         |
| 0479C5h | CAN1 Mailbox 28: Data Length        |        | XXh                     |
| 0479C6h | CAN1 Mailbox 28: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0479C7h |                                     |        |                         |
| 0479C8h |                                     |        |                         |
| 0479C9h |                                     |        |                         |
| 0479CAh |                                     |        |                         |
| 0479CBh |                                     |        |                         |
| 0479CCh |                                     |        |                         |
| 0479CDh |                                     |        |                         |
| 0479CEh | CAN1 Mailbox 28: Time Stamp         |        | XXXXh                   |
| 0479CFh |                                     |        |                         |
| 0479D0h | CAN1 Mailbox 29: Message Identifier | C1MB29 | XXXX XXXXh              |
| 0479D1h |                                     |        |                         |
| 0479D2h |                                     |        |                         |
| 0479D3h |                                     |        |                         |
| 0479D4h |                                     |        |                         |
| 0479D5h | CAN1 Mailbox 29: Data Length        |        | XXh                     |
| 0479D6h | CAN1 Mailbox 29: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0479D7h |                                     |        |                         |
| 0479D8h |                                     |        |                         |
| 0479D9h |                                     |        |                         |
| 0479DAh |                                     |        |                         |
| 0479DBh |                                     |        |                         |
| 0479DCh |                                     |        |                         |
| 0479DDh |                                     |        |                         |
| 0479DEh | CAN1 Mailbox 29: Time Stamp         |        | XXXXh                   |
| 0479DFh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.36 SFR List (36)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 0479E0h | CAN1 Mailbox 30: Message Identifier | C1MB30 | XXXX XXXXh              |
| 0479E1h |                                     |        |                         |
| 0479E2h |                                     |        |                         |
| 0479E3h |                                     |        |                         |
| 0479E4h |                                     |        |                         |
| 0479E5h | CAN1 Mailbox 30: Data Length        |        | XXh                     |
| 0479E6h | CAN1 Mailbox 30: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0479E7h |                                     |        |                         |
| 0479E8h |                                     |        |                         |
| 0479E9h |                                     |        |                         |
| 0479EAh |                                     |        |                         |
| 0479EBh |                                     |        |                         |
| 0479ECh |                                     |        |                         |
| 0479EDh |                                     |        |                         |
| 0479EEh | CAN1 Mailbox 30: Time Stamp         |        | XXXXh                   |
| 0479EFh |                                     |        |                         |
| 0479F0h | CAN1 Mailbox 31: Message Identifier | C1MB31 | XXXX XXXXh              |
| 0479F1h |                                     |        |                         |
| 0479F2h |                                     |        |                         |
| 0479F3h |                                     |        |                         |
| 0479F4h |                                     |        |                         |
| 0479F5h | CAN1 Mailbox 31: Data Length        |        | XXh                     |
| 0479F6h | CAN1 Mailbox 31: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 0479F7h |                                     |        |                         |
| 0479F8h |                                     |        |                         |
| 0479F9h |                                     |        |                         |
| 0479FAh |                                     |        |                         |
| 0479FBh |                                     |        |                         |
| 0479FCh |                                     |        |                         |
| 0479FDh |                                     |        |                         |
| 0479FEh | CAN1 Mailbox 31: Time Stamp         |        | XXXXh                   |
| 0479FFh |                                     |        |                         |
| 047A00h | CAN1 Acceptance Mask Register 0     | C1MKR0 | XXXX XXXXh              |
| 047A01h |                                     |        |                         |
| 047A02h |                                     |        |                         |
| 047A03h |                                     |        |                         |
| 047A04h | CAN1 Acceptance Mask Register 1     | C1MKR1 | XXXX XXXXh              |
| 047A05h |                                     |        |                         |
| 047A06h |                                     |        |                         |
| 047A07h |                                     |        |                         |
| 047A08h | CAN1 Acceptance Mask Register 2     | C1MKR2 | XXXX XXXXh              |
| 047A09h |                                     |        |                         |
| 047A0Ah |                                     |        |                         |
| 047A0Bh |                                     |        |                         |
| 047A0Ch | CAN1 Acceptance Mask Register 3     | C1MKR3 | XXXX XXXXh              |
| 047A0Dh |                                     |        |                         |
| 047A0Eh |                                     |        |                         |
| 047A0Fh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.37 SFR List (37)**

| Address               | Register                                 | Symbol   | Reset Value |
|-----------------------|------------------------------------------|----------|-------------|
| 047A10h               | CAN1 Acceptance Mask Register 4          | C1MKR4   | XXXX XXXXh  |
| 047A11h               |                                          |          |             |
| 047A12h               |                                          |          |             |
| 047A13h               |                                          |          |             |
| 047A14h               | CAN1 Acceptance Mask Register 5          | C1MKR5   | XXXX XXXXh  |
| 047A15h               |                                          |          |             |
| 047A16h               |                                          |          |             |
| 047A17h               |                                          |          |             |
| 047A18h               | CAN1 Acceptance Mask Register 6          | C1MKR6   | XXXX XXXXh  |
| 047A19h               |                                          |          |             |
| 047A1Ah               |                                          |          |             |
| 047A1Bh               |                                          |          |             |
| 047A1Ch               | CAN1 Acceptance Mask Register 7          | C1MKR7   | XXXX XXXXh  |
| 047A1Dh               |                                          |          |             |
| 047A1Eh               |                                          |          |             |
| 047A1Fh               |                                          |          |             |
| 047A20h               | CAN1 FIFO Received ID Compare Register 0 | C1FIDCR0 | XXXX XXXXh  |
| 047A21h               |                                          |          |             |
| 047A22h               |                                          |          |             |
| 047A23h               |                                          |          |             |
| 047A24h               | CAN1 FIFO Received ID Compare Register 1 | C1FIDCR1 | XXXX XXXXh  |
| 047A25h               |                                          |          |             |
| 047A26h               |                                          |          |             |
| 047A27h               |                                          |          |             |
| 047A28h               | CAN1 Mask Invalid Register               | C1MKIVLR | XXXX XXXXh  |
| 047A29h               |                                          |          |             |
| 047A2Ah               |                                          |          |             |
| 047A2Bh               |                                          |          |             |
| 047A2Ch               | CAN1 Mailbox Interrupt Enable Register   | C1MIER   | XXXX XXXXh  |
| 047A2Dh               |                                          |          |             |
| 047A2Eh               |                                          |          |             |
| 047A2Fh               |                                          |          |             |
| 047A30h               |                                          |          |             |
| 047A31h               |                                          |          |             |
| 047A32h               |                                          |          |             |
| 047A33h               |                                          |          |             |
| 047A34h               |                                          |          |             |
| 047A35h               |                                          |          |             |
| 047A36h               |                                          |          |             |
| 047A37h               |                                          |          |             |
| 047A38h               |                                          |          |             |
| 047A39h               |                                          |          |             |
| 047A3Ah               |                                          |          |             |
| 047A3Bh               |                                          |          |             |
| 047A3Ch               |                                          |          |             |
| 047A3Dh               |                                          |          |             |
| 047A3Eh               |                                          |          |             |
| 047A3Fh               |                                          |          |             |
| 047A40h to<br>047B1Fh |                                          |          |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.38 SFR List (38)**

| Address | Register                         | Symbol   | Reset Value |
|---------|----------------------------------|----------|-------------|
| 047B20h | CAN1 Message Control Register 0  | C1MCTL0  | 00h         |
| 047B21h | CAN1 Message Control Register 1  | C1MCTL1  | 00h         |
| 047B22h | CAN1 Message Control Register 2  | C1MCTL2  | 00h         |
| 047B23h | CAN1 Message Control Register 3  | C1MCTL3  | 00h         |
| 047B24h | CAN1 Message Control Register 4  | C1MCTL4  | 00h         |
| 047B25h | CAN1 Message Control Register 5  | C1MCTL5  | 00h         |
| 047B26h | CAN1 Message Control Register 6  | C1MCTL6  | 00h         |
| 047B27h | CAN1 Message Control Register 7  | C1MCTL7  | 00h         |
| 047B28h | CAN1 Message Control Register 8  | C1MCTL8  | 00h         |
| 047B29h | CAN1 Message Control Register 9  | C1MCTL9  | 00h         |
| 047B2Ah | CAN1 Message Control Register 10 | C1MCTL10 | 00h         |
| 047B2Bh | CAN1 Message Control Register 11 | C1MCTL11 | 00h         |
| 047B2Ch | CAN1 Message Control Register 12 | C1MCTL12 | 00h         |
| 047B2Dh | CAN1 Message Control Register 13 | C1MCTL13 | 00h         |
| 047B2Eh | CAN1 Message Control Register 14 | C1MCTL14 | 00h         |
| 047B2Fh | CAN1 Message Control Register 15 | C1MCTL15 | 00h         |
| 047B30h | CAN1 Message Control Register 16 | C1MCTL16 | 00h         |
| 047B31h | CAN1 Message Control Register 17 | C1MCTL17 | 00h         |
| 047B32h | CAN1 Message Control Register 18 | C1MCTL18 | 00h         |
| 047B33h | CAN1 Message Control Register 19 | C1MCTL19 | 00h         |
| 047B34h | CAN1 Message Control Register 20 | C1MCTL20 | 00h         |
| 047B35h | CAN1 Message Control Register 21 | C1MCTL21 | 00h         |
| 047B36h | CAN1 Message Control Register 22 | C1MCTL22 | 00h         |
| 047B37h | CAN1 Message Control Register 23 | C1MCTL23 | 00h         |
| 047B38h | CAN1 Message Control Register 24 | C1MCTL24 | 00h         |
| 047B39h | CAN1 Message Control Register 25 | C1MCTL25 | 00h         |
| 047B3Ah | CAN1 Message Control Register 26 | C1MCTL26 | 00h         |
| 047B3Bh | CAN1 Message Control Register 27 | C1MCTL27 | 00h         |
| 047B3Ch | CAN1 Message Control Register 28 | C1MCTL28 | 00h         |
| 047B3Dh | CAN1 Message Control Register 29 | C1MCTL29 | 00h         |
| 047B3Eh | CAN1 Message Control Register 30 | C1MCTL30 | 00h         |
| 047B3Fh | CAN1 Message Control Register 31 | C1MCTL31 | 00h         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.39 SFR List (39)**

| Address            | Register                                    | Symbol  | Reset Value |
|--------------------|---------------------------------------------|---------|-------------|
| 047B40h            | CAN1 Control Register                       | C1CTLR  | 0000 0101b  |
| 047B41h            |                                             |         | 0000 0000b  |
| 047B42h            | CAN1 Status Register                        | C1STR   | 0000 0101b  |
| 047B43h            |                                             |         | 0000 0000b  |
| 047B44h            | CAN1 Bit Configuration Register             | C1BCR   | 00 0000h    |
| 047B45h            |                                             |         |             |
| 047B46h            |                                             |         |             |
| 047B47h            | CAN1 Clock Select Register                  | C1CLKR  | 000X 0000b  |
| 047B48h            | CAN1 Receive FIFO Control Register          | C1RFCR  | 1000 0000b  |
| 047B49h            | CAN1 Receive FIFO Pointer Control Register  | C1RFPCR | XXh         |
| 047B4Ah            | CAN1 Transmit FIFO Control Register         | C1TFCR  | 1000 0000b  |
| 047B4Bh            | CAN1 Transmit FIFO Pointer Control Register | C1TFPCR | XXh         |
| 047B4Ch            | CAN1 Error Interrupt Enable Register        | C1EIER  | 00h         |
| 047B4Dh            | CAN1 Error Interrupt Factor Judge Register  | C1EIFR  | 00h         |
| 047B4Eh            | CAN1 Reception Error Count Register         | C1RECR  | 00h         |
| 047B4Fh            | CAN1 Transmission Error Count Register      | C1TECR  | 00h         |
| 047B50h            | CAN1 Error Code Store Register              | C1ECSR  | 00h         |
| 047B51h            | CAN1 Channel Search Support Register        | C1CSSR  | XXh         |
| 047B52h            | CAN1 Mailbox Search Status Register         | C1MSSR  | 1000 0000b  |
| 047B53h            | CAN1 Mailbox Search Mode Register           | C1MSMR  | XXXX XX00b  |
| 047B54h            | CAN1 Time Stamp Register                    | C1TSR   | 0000h       |
| 047B55h            |                                             |         |             |
| 047B56h            | CAN1 Acceptance Filter Support Register     | C1AFSR  | XXXXh       |
| 047B57h            |                                             |         |             |
| 047B58h            | CAN1 Test Control Register                  | C1TCR   | 00h         |
| 047B59h            |                                             |         |             |
| 047B5Ah            |                                             |         |             |
| 047B5Bh            |                                             |         |             |
| 047B5Ch            |                                             |         |             |
| 047B5Dh            |                                             |         |             |
| 047B5Eh            |                                             |         |             |
| 047B5Fh            |                                             |         |             |
| 047B60h to 047BFFh |                                             |         |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.40 SFR List (40)**

| Address | Register                           | Symbol | Reset Value             |
|---------|------------------------------------|--------|-------------------------|
| 047C00h | CAN0 Mailbox 0: Message Identifier | C0MB0  | XXXX XXXXh              |
| 047C01h |                                    |        |                         |
| 047C02h |                                    |        |                         |
| 047C03h |                                    |        |                         |
| 047C04h |                                    |        |                         |
| 047C05h | CAN0 Mailbox 0: Data Length        |        | XXh                     |
| 047C06h | CAN0 Mailbox 0: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047C07h |                                    |        |                         |
| 047C08h |                                    |        |                         |
| 047C09h |                                    |        |                         |
| 047C0Ah |                                    |        |                         |
| 047C0Bh |                                    |        |                         |
| 047C0Ch |                                    |        |                         |
| 047C0Dh |                                    |        |                         |
| 047C0Eh | CAN0 Mailbox 0: Time Stamp         |        | XXXXh                   |
| 047C0Fh |                                    |        |                         |
| 047C10h | CAN0 Mailbox 1: Message Identifier | C0MB1  | XXXX XXXXh              |
| 047C11h |                                    |        |                         |
| 047C12h |                                    |        |                         |
| 047C13h |                                    |        |                         |
| 047C14h |                                    |        |                         |
| 047C15h | CAN0 Mailbox 1: Data Length        |        | XXh                     |
| 047C16h | CAN0 Mailbox 1: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047C17h |                                    |        |                         |
| 047C18h |                                    |        |                         |
| 047C19h |                                    |        |                         |
| 047C1Ah |                                    |        |                         |
| 047C1Bh |                                    |        |                         |
| 047C1Ch |                                    |        |                         |
| 047C1Dh |                                    |        |                         |
| 047C1Eh | CAN0 Mailbox 1: Time Stamp         |        | XXXXh                   |
| 047C1Fh |                                    |        |                         |
| 047C20h | CAN0 Mailbox 2: Message Identifier | C0MB2  | XXXX XXXXh              |
| 047C21h |                                    |        |                         |
| 047C22h |                                    |        |                         |
| 047C23h |                                    |        |                         |
| 047C24h |                                    |        |                         |
| 047C25h | CAN0 Mailbox 2: Data Length        |        | XXh                     |
| 047C26h | CAN0 Mailbox 2: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047C27h |                                    |        |                         |
| 047C28h |                                    |        |                         |
| 047C29h |                                    |        |                         |
| 047C2Ah |                                    |        |                         |
| 047C2Bh |                                    |        |                         |
| 047C2Ch |                                    |        |                         |
| 047C2Dh |                                    |        |                         |
| 047C2Eh | CAN0 Mailbox 2: Time Stamp         |        | XXXXh                   |
| 047C2Fh |                                    |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.41 SFR List (41)**

| Address | Register                           | Symbol | Reset Value             |
|---------|------------------------------------|--------|-------------------------|
| 047C30h | CAN0 Mailbox 3: Message Identifier | C0MB3  | XXXX XXXXh              |
| 047C31h |                                    |        |                         |
| 047C32h |                                    |        |                         |
| 047C33h |                                    |        |                         |
| 047C34h |                                    |        |                         |
| 047C35h | CAN0 Mailbox 3: Data Length        |        | XXh                     |
| 047C36h | CAN0 Mailbox 3: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047C37h |                                    |        |                         |
| 047C38h |                                    |        |                         |
| 047C39h |                                    |        |                         |
| 047C3Ah |                                    |        |                         |
| 047C3Bh |                                    |        |                         |
| 047C3Ch |                                    |        |                         |
| 047C3Dh |                                    |        |                         |
| 047C3Eh | CAN0 Mailbox 3: Time Stamp         |        | XXXXh                   |
| 047C3Fh |                                    |        |                         |
| 047C40h | CAN0 Mailbox 4: Message Identifier | C0MB4  | XXXX XXXXh              |
| 047C41h |                                    |        |                         |
| 047C42h |                                    |        |                         |
| 047C43h |                                    |        |                         |
| 047C44h |                                    |        |                         |
| 047C45h | CAN0 Mailbox 4: Data Length        |        | XXh                     |
| 047C46h | CAN0 Mailbox 4: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047C47h |                                    |        |                         |
| 047C48h |                                    |        |                         |
| 047C49h |                                    |        |                         |
| 047C4Ah |                                    |        |                         |
| 047C4Bh |                                    |        |                         |
| 047C4Ch |                                    |        |                         |
| 047C4Dh |                                    |        |                         |
| 047C4Eh | CAN0 Mailbox 4: Time Stamp         |        | XXXXh                   |
| 047C4Fh |                                    |        |                         |
| 047C50h | CAN0 Mailbox 5: Message Identifier | C0MB5  | XXXX XXXXh              |
| 047C51h |                                    |        |                         |
| 047C52h |                                    |        |                         |
| 047C53h |                                    |        |                         |
| 047C54h |                                    |        |                         |
| 047C55h | CAN0 Mailbox 5: Data Length        |        | XXh                     |
| 047C56h | CAN0 Mailbox 5: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047C57h |                                    |        |                         |
| 047C58h |                                    |        |                         |
| 047C59h |                                    |        |                         |
| 047C5Ah |                                    |        |                         |
| 047C5Bh |                                    |        |                         |
| 047C5Ch |                                    |        |                         |
| 047C5Dh |                                    |        |                         |
| 047C5Eh | CAN0 Mailbox 5: Time Stamp         |        | XXXXh                   |
| 047C5Fh |                                    |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.42 SFR List (42)**

| Address | Register                           | Symbol | Reset Value             |
|---------|------------------------------------|--------|-------------------------|
| 047C60h | CAN0 Mailbox 6: Message Identifier | C0MB6  | XXXX XXXXh              |
| 047C61h |                                    |        |                         |
| 047C62h |                                    |        |                         |
| 047C63h |                                    |        |                         |
| 047C64h |                                    |        |                         |
| 047C65h | CAN0 Mailbox 6: Data Length        |        | XXh                     |
| 047C66h | CAN0 Mailbox 6: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047C67h |                                    |        |                         |
| 047C68h |                                    |        |                         |
| 047C69h |                                    |        |                         |
| 047C6Ah |                                    |        |                         |
| 047C6Bh |                                    |        |                         |
| 047C6Ch |                                    |        |                         |
| 047C6Dh |                                    |        |                         |
| 047C6Eh | CAN0 Mailbox 6: Time Stamp         |        | XXXXh                   |
| 047C6Fh |                                    |        |                         |
| 047C70h | CAN0 Mailbox 7: Message Identifier | C0MB7  | XXXX XXXXh              |
| 047C71h |                                    |        |                         |
| 047C72h |                                    |        |                         |
| 047C73h |                                    |        |                         |
| 047C74h |                                    |        |                         |
| 047C75h | CAN0 Mailbox 7: Data Length        |        | XXh                     |
| 047C76h | CAN0 Mailbox 7: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047C77h |                                    |        |                         |
| 047C78h |                                    |        |                         |
| 047C79h |                                    |        |                         |
| 047C7Ah |                                    |        |                         |
| 047C7Bh |                                    |        |                         |
| 047C7Ch |                                    |        |                         |
| 047C7Dh |                                    |        |                         |
| 047C7Eh | CAN0 Mailbox 7: Time Stamp         |        | XXXXh                   |
| 047C7Fh |                                    |        |                         |
| 047C80h | CAN0 Mailbox 8: Message Identifier | C0MB8  | XXXX XXXXh              |
| 047C81h |                                    |        |                         |
| 047C82h |                                    |        |                         |
| 047C83h |                                    |        |                         |
| 047C84h |                                    |        |                         |
| 047C85h | CAN0 Mailbox 8: Data Length        |        | XXh                     |
| 047C86h | CAN0 Mailbox 8: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047C87h |                                    |        |                         |
| 047C88h |                                    |        |                         |
| 047C89h |                                    |        |                         |
| 047C8Ah |                                    |        |                         |
| 047C8Bh |                                    |        |                         |
| 047C8Ch |                                    |        |                         |
| 047C8Dh |                                    |        |                         |
| 047C8Eh | CAN0 Mailbox 8: Time Stamp         |        | XXXXh                   |
| 047C8Fh |                                    |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.43 SFR List (43)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 047C90h | CAN0 Mailbox 9: Message Identifier  | C0MB9  | XXXX XXXXh              |
| 047C91h |                                     |        |                         |
| 047C92h |                                     |        |                         |
| 047C93h |                                     |        |                         |
| 047C94h |                                     |        |                         |
| 047C95h | CAN0 Mailbox 9: Data Length         |        | XXh                     |
| 047C96h | CAN0 Mailbox 9: Data Field          |        | XXXX XXXX<br>XXXX XXXXh |
| 047C97h |                                     |        |                         |
| 047C98h |                                     |        |                         |
| 047C99h |                                     |        |                         |
| 047C9Ah |                                     |        |                         |
| 047C9Bh |                                     |        |                         |
| 047C9Ch |                                     |        |                         |
| 047C9Dh |                                     |        |                         |
| 047C9Eh | CAN0 Mailbox 9: Time Stamp          |        | XXXXh                   |
| 047C9Fh |                                     |        |                         |
| 047CA0h | CAN0 Mailbox 10: Message Identifier | C0MB10 | XXXX XXXXh              |
| 047CA1h |                                     |        |                         |
| 047CA2h |                                     |        |                         |
| 047CA3h |                                     |        |                         |
| 047CA4h |                                     |        |                         |
| 047CA5h | CAN0 Mailbox 10: Data Length        |        | XXh                     |
| 047CA6h | CAN0 Mailbox 10: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047CA7h |                                     |        |                         |
| 047CA8h |                                     |        |                         |
| 047CA9h |                                     |        |                         |
| 047CAAh |                                     |        |                         |
| 047CABh |                                     |        |                         |
| 047CACH |                                     |        |                         |
| 047CADh |                                     |        |                         |
| 047CAEh | CAN0 Mailbox 10: Time Stamp         |        | XXXXh                   |
| 047CAFh |                                     |        |                         |
| 047CB0h | CAN0 Mailbox 11: Message Identifier | C0MB11 | XXXX XXXXh              |
| 047CB1h |                                     |        |                         |
| 047CB2h |                                     |        |                         |
| 047CB3h |                                     |        |                         |
| 047CB4h |                                     |        |                         |
| 047CB5h | CAN0 Mailbox 11: Data Length        |        | XXh                     |
| 047CB6h | CAN0 Mailbox 11: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047CB7h |                                     |        |                         |
| 047CB8h |                                     |        |                         |
| 047CB9h |                                     |        |                         |
| 047CBAh |                                     |        |                         |
| 047CBBh |                                     |        |                         |
| 047CBCh |                                     |        |                         |
| 047CBDh |                                     |        |                         |
| 047CBEh | CAN0 Mailbox 11: Time Stamp         |        | XXXXh                   |
| 047CBFh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.44 SFR List (44)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 047CC0h | CAN0 Mailbox 12: Message Identifier | C0MB12 | XXXX XXXXh              |
| 047CC1h |                                     |        |                         |
| 047CC2h |                                     |        |                         |
| 047CC3h |                                     |        |                         |
| 047CC4h |                                     |        |                         |
| 047CC5h | CAN0 Mailbox 12: Data Length        |        | XXh                     |
| 047CC6h | CAN0 Mailbox 12: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047CC7h |                                     |        |                         |
| 047CC8h |                                     |        |                         |
| 047CC9h |                                     |        |                         |
| 047CCAh |                                     |        |                         |
| 047CCBh |                                     |        |                         |
| 047CCCh |                                     |        |                         |
| 047CCDh |                                     |        |                         |
| 047CCEh | CAN0 Mailbox 12: Time Stamp         |        | XXXXh                   |
| 047CCFh |                                     |        |                         |
| 047CD0h | CAN0 Mailbox 13: Message Identifier | C0MB13 | XXXX XXXXh              |
| 047CD1h |                                     |        |                         |
| 047CD2h |                                     |        |                         |
| 047CD3h |                                     |        |                         |
| 047CD4h |                                     |        |                         |
| 047CD5h | CAN0 Mailbox 13: Data Length        |        | XXh                     |
| 047CD6h | CAN0 Mailbox 13: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047CD7h |                                     |        |                         |
| 047CD8h |                                     |        |                         |
| 047CD9h |                                     |        |                         |
| 047CDAh |                                     |        |                         |
| 047CDBh |                                     |        |                         |
| 047CDCh |                                     |        |                         |
| 047CDDh |                                     |        |                         |
| 047CDEh | CAN0 Mailbox 13: Time Stamp         |        | XXXXh                   |
| 047CDFh |                                     |        |                         |
| 047CE0h | CAN0 Mailbox 14: Message Identifier | C0MB14 | XXXX XXXXh              |
| 047CE1h |                                     |        |                         |
| 047CE2h |                                     |        |                         |
| 047CE3h |                                     |        |                         |
| 047CE4h |                                     |        |                         |
| 047CE5h | CAN0 Mailbox 14: Data Length        |        | XXh                     |
| 047CE6h | CAN0 Mailbox 14: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047CE7h |                                     |        |                         |
| 047CE8h |                                     |        |                         |
| 047CE9h |                                     |        |                         |
| 047CEAh |                                     |        |                         |
| 047CEBh |                                     |        |                         |
| 047CECh |                                     |        |                         |
| 047CEDh |                                     |        |                         |
| 047CEEh | CAN0 Mailbox 14: Time Stamp         |        | XXXXh                   |
| 047CEFh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.45 SFR List (45)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 047CF0h | CAN0 Mailbox 15: Message Identifier | C0MB15 | XXXX XXXXh              |
| 047CF1h |                                     |        |                         |
| 047CF2h |                                     |        |                         |
| 047CF3h |                                     |        |                         |
| 047CF4h |                                     |        |                         |
| 047CF5h | CAN0 Mailbox 15: Data Length        |        | XXh                     |
| 047CF6h | CAN0 Mailbox 15: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047CF7h |                                     |        |                         |
| 047CF8h |                                     |        |                         |
| 047CF9h |                                     |        |                         |
| 047CFAh |                                     |        |                         |
| 047CFBh |                                     |        |                         |
| 047CFCh |                                     |        |                         |
| 047CFDh |                                     |        |                         |
| 047CFEh | CAN0 Mailbox 15: Time Stamp         |        | XXXXh                   |
| 047CFFh |                                     |        |                         |
| 047D00h | CAN0 Mailbox 16: Message Identifier | C0MB16 | XXXX XXXXh              |
| 047D01h |                                     |        |                         |
| 047D02h |                                     |        |                         |
| 047D03h |                                     |        |                         |
| 047D04h |                                     |        |                         |
| 047D05h | CAN0 Mailbox 16: Data Length        |        | XXh                     |
| 047D06h | CAN0 Mailbox 16: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047D07h |                                     |        |                         |
| 047D08h |                                     |        |                         |
| 047D09h |                                     |        |                         |
| 047D0Ah |                                     |        |                         |
| 047D0Bh |                                     |        |                         |
| 047D0Ch |                                     |        |                         |
| 047D0Dh |                                     |        |                         |
| 047D0Eh | CAN0 Mailbox 16: Time Stamp         |        | XXXXh                   |
| 047D0Fh |                                     |        |                         |
| 047D10h | CAN0 Mailbox 17: Message Identifier | C0MB17 | XXXX XXXXh              |
| 047D11h |                                     |        |                         |
| 047D12h |                                     |        |                         |
| 047D13h |                                     |        |                         |
| 047D14h |                                     |        |                         |
| 047D15h | CAN0 Mailbox 17: Data Length        |        | XXh                     |
| 047D16h | CAN0 Mailbox 17: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047D17h |                                     |        |                         |
| 047D18h |                                     |        |                         |
| 047D19h |                                     |        |                         |
| 047D1Ah |                                     |        |                         |
| 047D1Bh |                                     |        |                         |
| 047D1Ch |                                     |        |                         |
| 047D1Dh |                                     |        |                         |
| 047D1Eh | CAN0 Mailbox 17: Time Stamp         |        | XXXXh                   |
| 047D1Fh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.46 SFR List (46)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 047D20h | CAN0 Mailbox 18: Message Identifier | C0MB18 | XXXX XXXXh              |
| 047D21h |                                     |        |                         |
| 047D22h |                                     |        |                         |
| 047D23h |                                     |        |                         |
| 047D24h |                                     |        |                         |
| 047D25h | CAN0 Mailbox 18: Data Length        |        | XXh                     |
| 047D26h | CAN0 Mailbox 18: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047D27h |                                     |        |                         |
| 047D28h |                                     |        |                         |
| 047D29h |                                     |        |                         |
| 047D2Ah |                                     |        |                         |
| 047D2Bh |                                     |        |                         |
| 047D2Ch |                                     |        |                         |
| 047D2Dh |                                     |        |                         |
| 047D2Eh | CAN0 Mailbox 18: Time Stamp         |        | XXXXh                   |
| 047D2Fh |                                     |        |                         |
| 047D30h | CAN0 Mailbox 19: Message Identifier | C0MB19 | XXXX XXXXh              |
| 047D31h |                                     |        |                         |
| 047D32h |                                     |        |                         |
| 047D33h |                                     |        |                         |
| 047D34h |                                     |        |                         |
| 047D35h | CAN0 Mailbox 19: Data Length        |        | XXh                     |
| 047D36h | CAN0 Mailbox 19: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047D37h |                                     |        |                         |
| 047D38h |                                     |        |                         |
| 047D39h |                                     |        |                         |
| 047D3Ah |                                     |        |                         |
| 047D3Bh |                                     |        |                         |
| 047D3Ch |                                     |        |                         |
| 047D3Dh |                                     |        |                         |
| 047D3Eh | CAN0 Mailbox 19: Time Stamp         |        | XXXXh                   |
| 047D3Fh |                                     |        |                         |
| 047D40h | CAN0 Mailbox 20: Message Identifier | C0MB20 | XXXX XXXXh              |
| 047D41h |                                     |        |                         |
| 047D42h |                                     |        |                         |
| 047D43h |                                     |        |                         |
| 047D44h |                                     |        |                         |
| 047D45h | CAN0 Mailbox 20: Data Length        |        | XXh                     |
| 047D46h | CAN0 Mailbox 20: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047D47h |                                     |        |                         |
| 047D48h |                                     |        |                         |
| 047D49h |                                     |        |                         |
| 047D4Ah |                                     |        |                         |
| 047D4Bh |                                     |        |                         |
| 047D4Ch |                                     |        |                         |
| 047D4Dh |                                     |        |                         |
| 047D4Eh | CAN0 Mailbox 20: Time Stamp         |        | XXXXh                   |
| 047D4Fh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.47 SFR List (47)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 047D50h | CAN0 Mailbox 21: Message Identifier | C0MB21 | XXXX XXXXh              |
| 047D51h |                                     |        |                         |
| 047D52h |                                     |        |                         |
| 047D53h |                                     |        |                         |
| 047D54h |                                     |        |                         |
| 047D55h | CAN0 Mailbox 21: Data Length        |        | XXh                     |
| 047D56h | CAN0 Mailbox 21: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047D57h |                                     |        |                         |
| 047D58h |                                     |        |                         |
| 047D59h |                                     |        |                         |
| 047D5Ah |                                     |        |                         |
| 047D5Bh |                                     |        |                         |
| 047D5Ch |                                     |        |                         |
| 047D5Dh |                                     |        |                         |
| 047D5Eh | CAN0 Mailbox 21: Time Stamp         |        | XXXXh                   |
| 047D5Fh |                                     |        |                         |
| 047D60h | CAN0 Mailbox 22: Message Identifier | C0MB22 | XXXX XXXXh              |
| 047D61h |                                     |        |                         |
| 047D62h |                                     |        |                         |
| 047D63h |                                     |        |                         |
| 047D64h |                                     |        |                         |
| 047D65h | CAN0 Mailbox 22: Data Length        |        | XXh                     |
| 047D66h | CAN0 Mailbox 22: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047D67h |                                     |        |                         |
| 047D68h |                                     |        |                         |
| 047D69h |                                     |        |                         |
| 047D6Ah |                                     |        |                         |
| 047D6Bh |                                     |        |                         |
| 047D6Ch |                                     |        |                         |
| 047D6Dh |                                     |        |                         |
| 047D6Eh | CAN0 Mailbox 22: Time Stamp         |        | XXXXh                   |
| 047D6Fh |                                     |        |                         |
| 047D70h | CAN0 Mailbox 23: Message Identifier | C0MB23 | XXXX XXXXh              |
| 047D71h |                                     |        |                         |
| 047D72h |                                     |        |                         |
| 047D73h |                                     |        |                         |
| 047D74h |                                     |        |                         |
| 047D75h | CAN0 Mailbox 23: Data Length        |        | XXh                     |
| 047D76h | CAN0 Mailbox 23: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047D77h |                                     |        |                         |
| 047D78h |                                     |        |                         |
| 047D79h |                                     |        |                         |
| 047D7Ah |                                     |        |                         |
| 047D7Bh |                                     |        |                         |
| 047D7Ch |                                     |        |                         |
| 047D7Dh |                                     |        |                         |
| 047D7Eh | CAN0 Mailbox 23: Time Stamp         |        | XXXXh                   |
| 047D7Fh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.48 SFR List (48)**

| Address | Register                            | Symbol | Reset Value |
|---------|-------------------------------------|--------|-------------|
| 047D80h | CAN0 Mailbox 24: Message Identifier | C0MB24 | XXXX XXXXh  |
| 047D81h |                                     |        |             |
| 047D82h |                                     |        |             |
| 047D83h |                                     |        |             |
| 047D84h |                                     |        |             |
| 047D85h | CAN0 Mailbox 24: Data Length        |        | XXh         |
| 047D86h | CAN0 Mailbox 24: Data Field         |        | XXXX XXXX   |
| 047D87h |                                     |        | XXXX XXXXh  |
| 047D88h |                                     |        |             |
| 047D89h |                                     |        |             |
| 047D8Ah |                                     |        |             |
| 047D8Bh |                                     |        |             |
| 047D8Ch |                                     |        |             |
| 047D8Dh |                                     |        |             |
| 047D8Eh | CAN0 Mailbox 24: Time Stamp         |        | XXXXh       |
| 047D8Fh |                                     |        |             |
| 047D90h | CAN0 Mailbox 25: Message Identifier | C0MB25 | XXXX XXXXh  |
| 047D91h |                                     |        |             |
| 047D92h |                                     |        |             |
| 047D93h |                                     |        |             |
| 047D94h |                                     |        |             |
| 047D95h | CAN0 Mailbox 25: Data Length        |        | XXh         |
| 047D96h | CAN0 Mailbox 25: Data Field         |        | XXXX XXXX   |
| 047D97h |                                     |        | XXXX XXXXh  |
| 047D98h |                                     |        |             |
| 047D99h |                                     |        |             |
| 047D9Ah |                                     |        |             |
| 047D9Bh |                                     |        |             |
| 047D9Ch |                                     |        |             |
| 047D9Dh |                                     |        |             |
| 047D9Eh | CAN0 Mailbox 25: Time Stamp         |        | XXXXh       |
| 047D9Fh |                                     |        |             |
| 047DA0h | CAN0 Mailbox 26: Message Identifier | C0MB26 | XXXX XXXXh  |
| 047DA1h |                                     |        |             |
| 047DA2h |                                     |        |             |
| 047DA3h |                                     |        |             |
| 047DA4h |                                     |        |             |
| 047DA5h | CAN0 Mailbox 26: Data Length        |        | XXh         |
| 047DA6h | CAN0 Mailbox 26: Data Field         |        | XXXX XXXX   |
| 047DA7h |                                     |        | XXXX XXXXh  |
| 047DA8h |                                     |        |             |
| 047DA9h |                                     |        |             |
| 047DAAh |                                     |        |             |
| 047DABh |                                     |        |             |
| 047DACH |                                     |        |             |
| 047DADh |                                     |        |             |
| 047DAEh | CAN0 Mailbox 26: Time Stamp         |        | XXXXh       |
| 047DAFh |                                     |        |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.49 SFR List (49)**

| Address  | Register                            | Symbol | Reset Value             |
|----------|-------------------------------------|--------|-------------------------|
| 047DB0h  | CAN0 Mailbox 27: Message Identifier | C0MB27 | XXXX XXXXh              |
| 047DB1h  |                                     |        |                         |
| 047DB2h  |                                     |        |                         |
| 047DB3h  |                                     |        |                         |
| 047DB4h  |                                     |        |                         |
| 047DB5h  | CAN0 Mailbox 27: Data Length        |        | XXh                     |
| 047DB6h  | CAN0 Mailbox 27: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047DB7h  |                                     |        |                         |
| 047DB8h  |                                     |        |                         |
| 047DB9h  |                                     |        |                         |
| 047DBAh  |                                     |        |                         |
| 047DBBh  |                                     |        |                         |
| 047DBCh  |                                     |        |                         |
| 047DBDh  |                                     |        |                         |
| 047DBEh  | CAN0 Mailbox 27: Time Stamp         |        | XXXXh                   |
| 047DBFh  |                                     |        |                         |
| 047DC0h  | CAN0 Mailbox 28: Message Identifier | C0MB28 | XXXX XXXXh              |
| 047DC1h  |                                     |        |                         |
| 047DC2h  |                                     |        |                         |
| 047DC3h  |                                     |        |                         |
| 047DC4h  |                                     |        |                         |
| 047DC5h  | CAN0 Mailbox 28: Data Length        |        | XXh                     |
| 047DC6h  | CAN0 Mailbox 28: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047DC7h  |                                     |        |                         |
| 047DC8h  |                                     |        |                         |
| 047DC9h  |                                     |        |                         |
| 047DCAh  |                                     |        |                         |
| 047DCBh  |                                     |        |                         |
| 047DCCCh |                                     |        |                         |
| 047DCDh  |                                     |        |                         |
| 047DCEh  | CAN0 Mailbox 28: Time Stamp         |        | XXXXh                   |
| 047DCFh  |                                     |        |                         |
| 047DD0h  | CAN0 Mailbox 29: Message Identifier | C0MB29 | XXXX XXXXh              |
| 047DD1h  |                                     |        |                         |
| 047DD2h  |                                     |        |                         |
| 047DD3h  |                                     |        |                         |
| 047DD4h  |                                     |        |                         |
| 047DD5h  | CAN0 Mailbox 29: Data Length        |        | XXh                     |
| 047DD6h  | CAN0 Mailbox 29: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047DD7h  |                                     |        |                         |
| 047DD8h  |                                     |        |                         |
| 047DD9h  |                                     |        |                         |
| 047DDAh  |                                     |        |                         |
| 047DDBh  |                                     |        |                         |
| 047DDCh  |                                     |        |                         |
| 047DDDh  |                                     |        |                         |
| 047DDEh  | CAN0 Mailbox 29: Time Stamp         |        | XXXXh                   |
| 047DDFh  |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.50 SFR List (50)**

| Address | Register                            | Symbol | Reset Value             |
|---------|-------------------------------------|--------|-------------------------|
| 047DE0h | CAN0 Mailbox 30: Message Identifier | C0MB30 | XXXX XXXXh              |
| 047DE1h |                                     |        |                         |
| 047DE2h |                                     |        |                         |
| 047DE3h |                                     |        |                         |
| 047DE4h |                                     |        |                         |
| 047DE5h | CAN0 Mailbox 30: Data Length        |        | XXh                     |
| 047DE6h | CAN0 Mailbox 30: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047DE7h |                                     |        |                         |
| 047DE8h |                                     |        |                         |
| 047DE9h |                                     |        |                         |
| 047DEAh |                                     |        |                         |
| 047DEBh |                                     |        |                         |
| 047DECh |                                     |        |                         |
| 047DEDh |                                     |        |                         |
| 047DEEh | CAN0 Mailbox 30: Time Stamp         |        | XXXXh                   |
| 047DEFh |                                     |        |                         |
| 047DF0h | CAN0 Mailbox 31: Message Identifier | C0MB31 | XXXX XXXXh              |
| 047DF1h |                                     |        |                         |
| 047DF2h |                                     |        |                         |
| 047DF3h |                                     |        |                         |
| 047DF4h |                                     |        |                         |
| 047DF5h | CAN0 Mailbox 31: Data Length        |        | XXh                     |
| 047DF6h | CAN0 Mailbox 31: Data Field         |        | XXXX XXXX<br>XXXX XXXXh |
| 047DF7h |                                     |        |                         |
| 047DF8h |                                     |        |                         |
| 047DF9h |                                     |        |                         |
| 047DFAh |                                     |        |                         |
| 047DFBh |                                     |        |                         |
| 047DFCh |                                     |        |                         |
| 047DFDh |                                     |        |                         |
| 047DFEh | CAN0 Mailbox 31: Time Stamp         |        | XXXXh                   |
| 047DFFh |                                     |        |                         |
| 047E00h | CAN0 Acceptance Mask Register 0     | C0MKR0 | XXXX XXXXh              |
| 047E01h |                                     |        |                         |
| 047E02h |                                     |        |                         |
| 047E03h |                                     |        |                         |
| 047E04h | CAN0 Acceptance Mask Register 1     | C0MKR1 | XXXX XXXXh              |
| 047E05h |                                     |        |                         |
| 047E06h |                                     |        |                         |
| 047E07h |                                     |        |                         |
| 047E08h | CAN0 Acceptance Mask Register 2     | C0MKR2 | XXXX XXXXh              |
| 047E09h |                                     |        |                         |
| 047E0Ah |                                     |        |                         |
| 047E0Bh |                                     |        |                         |
| 047E0Ch | CAN0 Acceptance Mask Register 3     | C0MKR3 | XXXX XXXXh              |
| 047E0Dh |                                     |        |                         |
| 047E0Eh |                                     |        |                         |
| 047E0Fh |                                     |        |                         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.51 SFR List (51)**

| Address               | Register                                | Symbol   | Reset Value |
|-----------------------|-----------------------------------------|----------|-------------|
| 047E10h               | CAN0 Acceptance Mask Register 4         | C0MKR4   | XXXX XXXXh  |
| 047E11h               |                                         |          |             |
| 047E12h               |                                         |          |             |
| 047E13h               |                                         |          |             |
| 047E14h               | CAN0 Acceptance Mask Register 5         | C0MKR5   | XXXX XXXXh  |
| 047E15h               |                                         |          |             |
| 047E16h               |                                         |          |             |
| 047E17h               |                                         |          |             |
| 047E18h               | CAN0 Acceptance Mask Register 6         | C0MKR6   | XXXX XXXXh  |
| 047E19h               |                                         |          |             |
| 047E1Ah               |                                         |          |             |
| 047E1Bh               |                                         |          |             |
| 047E1Ch               | CAN0 Acceptance Mask Register 7         | C0MKR7   | XXXX XXXXh  |
| 047E1Dh               |                                         |          |             |
| 047E1Eh               |                                         |          |             |
| 047E1Fh               |                                         |          |             |
| 047E20h               | CAN0 FIFO Receive ID Compare Register 0 | C0FIDCR0 | XXXX XXXXh  |
| 047E21h               |                                         |          |             |
| 047E22h               |                                         |          |             |
| 047E23h               |                                         |          |             |
| 047E24h               | CAN0 FIFO Receive ID Compare Register 1 | C0FIDCR1 | XXXX XXXXh  |
| 047E25h               |                                         |          |             |
| 047E26h               |                                         |          |             |
| 047E27h               |                                         |          |             |
| 047E28h               | CAN0 Mask Invalid Register              | C0MKIVLR | XXXX XXXXh  |
| 047E29h               |                                         |          |             |
| 047E2Ah               |                                         |          |             |
| 047E2Bh               |                                         |          |             |
| 047E2Ch               | CAN0 Mailbox Interrupt Enable Register  | C0MIER   | XXXX XXXXh  |
| 047E2Dh               |                                         |          |             |
| 047E2Eh               |                                         |          |             |
| 047E2Fh               |                                         |          |             |
| 047E30h               |                                         |          |             |
| 047E31h               |                                         |          |             |
| 047E32h               |                                         |          |             |
| 047E33h               |                                         |          |             |
| 047E34h               |                                         |          |             |
| 047E35h               |                                         |          |             |
| 047E36h               |                                         |          |             |
| 047E37h               |                                         |          |             |
| 047E38h               |                                         |          |             |
| 047E39h               |                                         |          |             |
| 047E3Ah               |                                         |          |             |
| 047E3Bh               |                                         |          |             |
| 047E3Ch               |                                         |          |             |
| 047E3Dh               |                                         |          |             |
| 047E3Eh               |                                         |          |             |
| 047E3Fh               |                                         |          |             |
| 047E40h to<br>047F1Fh |                                         |          |             |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.52 SFR List (52)**

| Address | Register                         | Symbol   | Reset Value |
|---------|----------------------------------|----------|-------------|
| 047F20h | CAN0 Message Control Register 0  | C0MCTL0  | 00h         |
| 047F21h | CAN0 Message Control Register 1  | C0MCTL1  | 00h         |
| 047F22h | CAN0 Message Control Register 2  | C0MCTL2  | 00h         |
| 047F23h | CAN0 Message Control Register 3  | C0MCTL3  | 00h         |
| 047F24h | CAN0 Message Control Register 4  | C0MCTL4  | 00h         |
| 047F25h | CAN0 Message Control Register 5  | C0MCTL5  | 00h         |
| 047F26h | CAN0 Message Control Register 6  | C0MCTL6  | 00h         |
| 047F27h | CAN0 Message Control Register 7  | C0MCTL7  | 00h         |
| 047F28h | CAN0 Message Control Register 8  | C0MCTL8  | 00h         |
| 047F29h | CAN0 Message Control Register 9  | C0MCTL9  | 00h         |
| 047F2Ah | CAN0 Message Control Register 10 | C0MCTL10 | 00h         |
| 047F2Bh | CAN0 Message Control Register 11 | C0MCTL11 | 00h         |
| 047F2Ch | CAN0 Message Control Register 12 | C0MCTL12 | 00h         |
| 047F2Dh | CAN0 Message Control Register 13 | C0MCTL13 | 00h         |
| 047F2Eh | CAN0 Message Control Register 14 | C0MCTL14 | 00h         |
| 047F2Fh | CAN0 Message Control Register 15 | C0MCTL15 | 00h         |
| 047F30h | CAN0 Message Control Register 16 | C0MCTL16 | 00h         |
| 047F31h | CAN0 Message Control Register 17 | C0MCTL17 | 00h         |
| 047F32h | CAN0 Message Control Register 18 | C0MCTL18 | 00h         |
| 047F33h | CAN0 Message Control Register 19 | C0MCTL19 | 00h         |
| 047F34h | CAN0 Message Control Register 20 | C0MCTL20 | 00h         |
| 047F35h | CAN0 Message Control Register 21 | C0MCTL21 | 00h         |
| 047F36h | CAN0 Message Control Register 22 | C0MCTL22 | 00h         |
| 047F37h | CAN0 Message Control Register 23 | C0MCTL23 | 00h         |
| 047F38h | CAN0 Message Control Register 24 | C0MCTL24 | 00h         |
| 047F39h | CAN0 Message Control Register 25 | C0MCTL25 | 00h         |
| 047F3Ah | CAN0 Message Control Register 26 | C0MCTL26 | 00h         |
| 047F3Bh | CAN0 Message Control Register 27 | C0MCTL27 | 00h         |
| 047F3Ch | CAN0 Message Control Register 28 | C0MCTL28 | 00h         |
| 047F3Dh | CAN0 Message Control Register 29 | C0MCTL29 | 00h         |
| 047F3Eh | CAN0 Message Control Register 30 | C0MCTL30 | 00h         |
| 047F3Fh | CAN0 Message Control Register 31 | C0MCTL31 | 00h         |

X: Undefined

Blanks are reserved. No access is allowed.

**Table 4.53 SFR List (53)**

| Address               | Register                                    | Symbol  | Reset Value |
|-----------------------|---------------------------------------------|---------|-------------|
| 047F40h               | CAN0 Control Register                       | C0CTLR  | 0000 0101b  |
| 047F41h               |                                             |         | 0000 0000b  |
| 047F42h               | CAN0 Status Register                        | C0STR   | 0000 0101b  |
| 047F43h               |                                             |         | 0000 0000b  |
| 047F44h               | CAN0 Bit Configuration Register             | C0BCR   | 00 0000h    |
| 047F45h               |                                             |         |             |
| 047F46h               |                                             |         |             |
| 047F47h               | CAN0 Clock Select Register                  | C0CLKR  | 000X 0000b  |
| 047F48h               | CAN0 Receive FIFO Control Register          | C0RFCR  | 1000 0000b  |
| 047F49h               | CAN0 Receive FIFO Pointer Control Register  | C0RFPCR | XXh         |
| 047F4Ah               | CAN0 Transmit FIFO Control Register         | C0TFCR  | 1000 0000b  |
| 047F4Bh               | CAN0 Transmit FIFO Pointer Control Register | C0TFPCR | XXh         |
| 047F4Ch               | CAN0 Error Interrupt Enable Register        | C0EIER  | 00h         |
| 047F4Dh               | CAN0 Error Interrupt Factor Judge Register  | C0EIFR  | 00h         |
| 047F4Eh               | CAN0 Reception Error Count Register         | C0RECR  | 00h         |
| 047F4Fh               | CAN0 Transmission Error Count Register      | C0TECR  | 00h         |
| 047F50h               | CAN0 Error Code Store Register              | C0ECSR  | 00h         |
| 047F51h               | CAN0 Channel Search Support Register        | C0CSSR  | XXh         |
| 047F52h               | CAN0 Mailbox Search Status Register         | C0MSSR  | 1000 0000b  |
| 047F53h               | CAN0 Mailbox Search Mode Register           | C0MSMR  | XXXX XX00b  |
| 047F54h               | CAN0 Time Stamp Register                    | C0TSR   | 0000h       |
| 047F55h               |                                             |         |             |
| 047F56h               | CAN0 Acceptance Filter Support Register     | C0AFSR  | XXXXh       |
| 047F57h               |                                             |         |             |
| 047F58h               | CAN0 Test Control Register                  | C0TCR   | 00h         |
| 047F59h               |                                             |         |             |
| 047F5Ah               |                                             |         |             |
| 047F5Bh               |                                             |         |             |
| 047F5Ch               |                                             |         |             |
| 047F5Dh               |                                             |         |             |
| 047F5Eh               |                                             |         |             |
| 047F5Fh               |                                             |         |             |
| 047F60h to<br>047FFFh |                                             |         |             |
| 048000h to<br>04FFFFh |                                             |         |             |

X: Undefined

Blanks are reserved. No access is allowed.

## 5. Electrical Characteristics

**Table 5.1 Absolute Maximum Ratings (1)**

| Symbol    | Characteristic              |                                                                                                                                                                                                                       | Condition                | Value                  | Unit             |
|-----------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|------------------------|------------------|
| $V_{CC}$  | Supply voltage              |                                                                                                                                                                                                                       | $V_{CC} = AV_{CC}$       | -0.3 to 6.0            | V                |
| $AV_{CC}$ | Analog supply voltage       |                                                                                                                                                                                                                       | $V_{CC} = AV_{CC}$       | -0.3 to 6.0            | V                |
| $V_I$     | Input voltage               | XIN, $\overline{RESET}$ , CNVSS, NSD, $V_{REF}$ ,<br>P0_0 to P0_7, P1_0 to P1_7,<br>P2_0 to P2_7, P3_0 to P3_7,<br>P4_0 to P4_7, P5_0 to P5_7, P6_5,<br>P6_7, P7_0, P7_4 to P7_6,<br>P8_2 to P8_7, P9_1, P9_3 to P9_7 |                          | -0.3 to $V_{CC} + 0.3$ | V                |
| $V_O$     | Output voltage              | XOUT, P0_0 to P0_7, P1_0 to P1_7,<br>P2_0 to P2_7, P3_0 to P3_7,<br>P4_0 to P4_7, P5_0 to P5_7, P6_5,<br>P6_7, P7_0, P7_4 to P7_6,<br>P8_2 to P8_4, P8_6, P8_7,<br>P9_3 to P9_7                                       |                          | -0.3 to $V_{CC} + 0.3$ | V                |
| $P_d$     | Power consumption           |                                                                                                                                                                                                                       | $T_a = 25^\circ\text{C}$ | 500                    | mW               |
| —         | Operating temperature range |                                                                                                                                                                                                                       |                          | -40 to 125             | $^\circ\text{C}$ |
| $T_{stg}$ | Storage temperature range   |                                                                                                                                                                                                                       |                          | -65 to 150             | $^\circ\text{C}$ |

Note:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 5.2 Operating Conditions (1/6) (1)**

| Symbol       | Characteristic                            |                                                                                                                                                          | Value               |          |                     | Unit |
|--------------|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|----------|---------------------|------|
|              |                                           |                                                                                                                                                          | Min.                | Typ.     | Max.                |      |
| $V_{CC}$     | Digital supply voltage                    |                                                                                                                                                          | 3.0                 | 5.0      | 5.5                 | V    |
| $AV_{CC}$    | Analog supply voltage                     |                                                                                                                                                          |                     | $V_{CC}$ |                     | V    |
| $V_{REF}$    | Reference voltage                         |                                                                                                                                                          | 3.0                 |          | $V_{CC}$            | V    |
| $V_{SS}$     | Digital ground voltage                    |                                                                                                                                                          |                     | 0        |                     | V    |
| $AV_{SS}$    | Analog ground voltage                     |                                                                                                                                                          |                     | 0        |                     | V    |
| $dV_{CC}/dt$ | $V_{CC}$ ramp up rate ( $V_{CC} < 2.0$ V) |                                                                                                                                                          | 0.05                |          |                     | V/ms |
| $V_{IH}$     | High level input voltage                  | XIN, RESET, CNVSS, NSD                                                                                                                                   | $0.8 \times V_{CC}$ |          | $V_{CC}$            | V    |
|              |                                           | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_7 (2), P9_1, P9_3 to P9_7 | $0.7 \times V_{CC}$ |          | $V_{CC}$            | V    |
| $V_{IL}$     | Low level input voltage                   | XIN, RESET, CNVSS, NSD                                                                                                                                   | 0                   |          | $0.2 \times V_{CC}$ | V    |
|              |                                           | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_7 (2), P9_1, P9_3 to P9_7 | 0                   |          | $0.3 \times V_{CC}$ | V    |
| $T_{opr}$    | Operating temperature range               | Version J                                                                                                                                                | -40                 |          | 85                  | °C   |
|              |                                           | Version L                                                                                                                                                | -40                 |          | 105                 | °C   |
|              |                                           | Version K                                                                                                                                                | -40                 |          | 125                 | °C   |

**Notes:**

1. The device is operationally guaranteed under these operating conditions.
2.  $V_{IH}$  and  $V_{IL}$  for P8\_7 are specified for P8\_7 as a programmable port. These values are not applicable to P8\_7 as XCIN.

**Table 5.3 Operating Conditions (2/6)**  
**( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted) <sup>(1)</sup>**

| Symbol    | Characteristic                               |                          | Value <sup>(2)</sup> |      |      | Unit    |
|-----------|----------------------------------------------|--------------------------|----------------------|------|------|---------|
|           |                                              |                          | Min.                 | Typ. | Max. |         |
| $C_{VDC}$ | Decoupling capacitance for voltage regulator | Inter-pin voltage: 1.5 V | 2.4                  |      | 10.0 | $\mu F$ |

Notes:

1. The device is operationally guaranteed under these operating conditions.
2. This value should be satisfied with due consideration of every condition as follows: operating temperature, DC bias, aging, etc.

**Table 5.4 Operating Conditions (3/6)**  
**( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted) <sup>(1)</sup>**

| Symbol         | Characteristic                                   |                                                                                                                                                            | Value |      |       | Unit |
|----------------|--------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|------|
|                |                                                  |                                                                                                                                                            | Min.  | Typ. | Max.  |      |
| $I_{OH(peak)}$ | High level peak output current <sup>(2)</sup>    | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_3 to P9_7 |       |      | -10.0 | mA   |
| $I_{OH(avg)}$  | High level average output current <sup>(3)</sup> | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_3 to P9_7 |       |      | -5.0  | mA   |
| $I_{OL(peak)}$ | Low level peak output current <sup>(2)</sup>     | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_3 to P9_7 |       |      | 10.0  | mA   |
| $I_{OL(avg)}$  | Low level average output current <sup>(3)</sup>  | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_3 to P9_7 |       |      | 5.0   | mA   |

Notes:

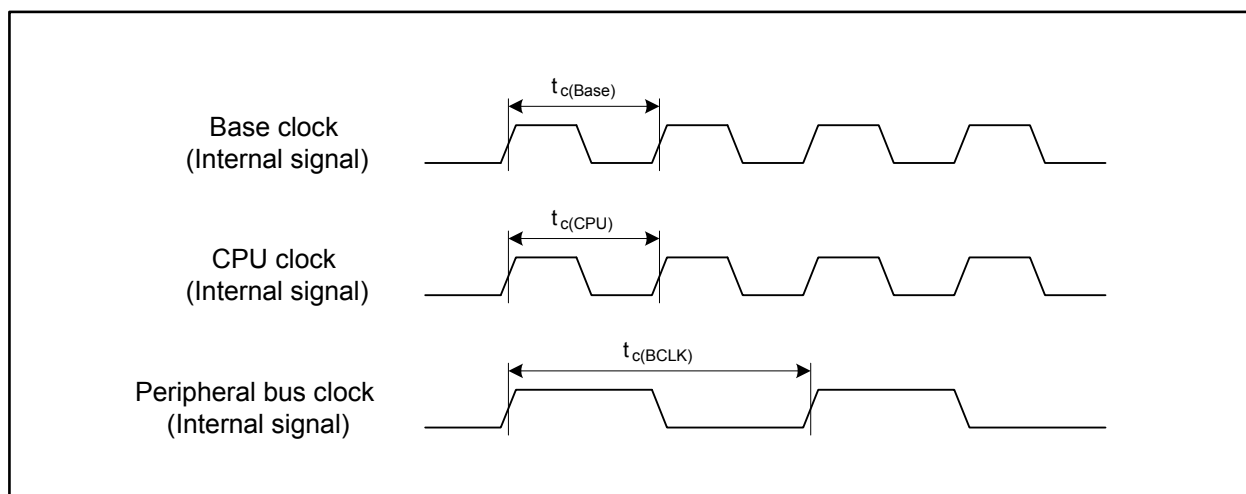
- The device is operationally guaranteed under these operating conditions.
- The following conditions should be satisfied:
  - The sum of  $I_{OL(peak)}$  of ports P0, P1, P2, P8\_6, P8\_7, and P9 is 80 mA or less.
  - The sum of  $I_{OL(peak)}$  of ports P3, P4, P5, P6, P7, and P8\_2 to P8\_4 is 80 mA or less.
  - The sum of  $I_{OH(peak)}$  of ports P1 and P2 is -40 mA or less.
  - The sum of  $I_{OH(peak)}$  of ports P0, P9\_6, and P9\_7 is -40 mA or less.
  - The sum of  $I_{OH(peak)}$  of ports P3, P4, P5, and P6 is -40 mA or less.
  - The sum of  $I_{OH(peak)}$  of ports P7, P8, and P9\_3 to P9\_5 is -40 mA or less.
- Average value within 100 ms.

**Table 5.5 Operating Conditions (4/6)**  
**( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted) <sup>(1)</sup>**

| Symbol        | Characteristic                           | Value |        |      | Unit |
|---------------|------------------------------------------|-------|--------|------|------|
|               |                                          | Min.  | Typ.   | Max. |      |
| $f_{(XIN)}$   | Main clock oscillator frequency          | 4     |        | 8    | MHz  |
| $f_{(XRef)}$  | Reference clock frequency                | 2     |        | 4    | MHz  |
| $f_{(PLL)}$   | PLL clock oscillator frequency           | 96    |        | 144  | MHz  |
| $f_{(Base)}$  | Base clock frequency                     |       |        | 48   | MHz  |
| $t_{c(Base)}$ | Base clock cycle time                    | 20.83 |        |      | ns   |
| $f_{(CPU)}$   | CPU operating frequency                  |       |        | 48   | MHz  |
| $t_{c(CPU)}$  | CPU clock cycle time                     | 20.83 |        |      | ns   |
| $f_{(BCLK)}$  | Peripheral bus clock operating frequency |       |        | 24   | MHz  |
| $t_{c(BCLK)}$ | Peripheral bus clock cycle time          | 41.67 |        |      | ns   |
| $f_{(PER)}$   | Peripheral clock source frequency        |       |        | 24   | MHz  |
| $f_{(XCIN)}$  | Sub clock oscillator frequency           |       | 32.768 | 50   | kHz  |

Note:

1. The device is operationally guaranteed under these operating conditions.



**Figure 5.1 Clock Cycle Time**

**Table 5.6 Operating Conditions (5/6)****( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted) (1, 2)**

| Symbol           | Characteristic               |                                                                                                                                                | Measurement Condition | Value |      |      | Unit |
|------------------|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-------|------|------|------|
|                  |                              |                                                                                                                                                |                       | Min.  | Typ. | Max. |      |
| $I_{IC(H)}$      | High input injection current | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_5, P9_3 to P9_7 | $V_I > V_{CC}$        |       |      | 2    | mA   |
| $I_{IC(L)}$      | Low input injection current  | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_5, P9_3 to P9_7 | $V_I < V_{SS}$        |       |      | -2   | mA   |
| $\Sigma I_{IC} $ | Total injection current      |                                                                                                                                                |                       |       |      | 20   | mA   |

Notes:

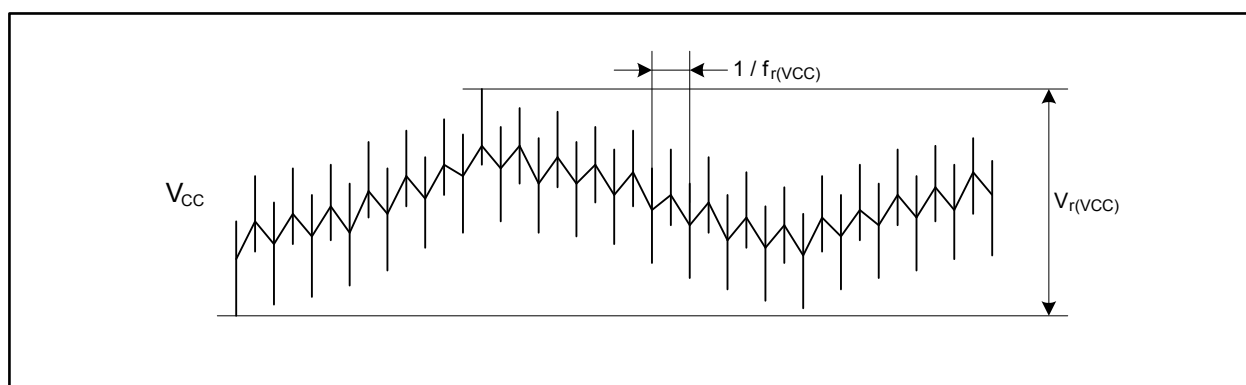
1. The device is operationally guaranteed under these operating conditions.
2. These conditions are applicable when each port is designated as input.

**Table 5.7 Operating Conditions (6/6)**  
**( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted) <sup>(1)</sup>**

| Symbol           | Characteristic             | Value            |      |           | Unit |
|------------------|----------------------------|------------------|------|-----------|------|
|                  |                            | Min.             | Typ. | Max.      |      |
| $V_{r(VCC)}$     | Allowable ripple voltage   | $V_{CC} = 5.0$ V |      | 0.5       | Vp-p |
|                  |                            | $V_{CC} = 3.0$ V |      | 0.3       | Vp-p |
| $dV_{r(VCC)}/dt$ | Ripple voltage gradient    | $V_{CC} = 5.0$ V |      | $\pm 0.3$ | V/ms |
|                  |                            | $V_{CC} = 3.0$ V |      | $\pm 0.3$ | V/ms |
| $f_{r(VCC)}$     | Allowable ripple frequency |                  |      | 10        | kHz  |

Note:

1. The device is operationally guaranteed under these operating conditions.



**Figure 5.2 Ripple Waveform**

**Table 5.8 Flash Memory Electrical Characteristics**  
**( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted)**

| Symbol | Characteristic                                        |                                 | Value |      |      | Unit    |
|--------|-------------------------------------------------------|---------------------------------|-------|------|------|---------|
|        |                                                       |                                 | Min.  | Typ. | Max. |         |
| —      | Programming and erasure endurance of flash memory (1) | Program area                    | 1000  |      |      | times   |
|        |                                                       | Data area                       | 10000 |      |      | times   |
| —      | 4-word program time                                   | Program area                    |       | 150  | 900  | $\mu$ s |
|        |                                                       | Data area                       |       | 300  | 1700 | $\mu$ s |
| —      | Lock bit-program time                                 | Program area                    |       | 70   | 500  | $\mu$ s |
|        |                                                       | Data area                       |       | 140  | 1000 | $\mu$ s |
| —      | Block erasure time                                    | 4 Kbyte block                   |       | 0.12 | 3.0  | s       |
|        |                                                       | 32 Kbyte block                  |       | 0.17 | 3.0  | s       |
|        |                                                       | 64 Kbyte block                  |       | 0.20 | 3.0  | s       |
| —      | Data retention (2)                                    | $T_a = 55^\circ\text{C}$ (3, 4) | 20    |      |      | years   |

Notes:

1. Program/erase definition

This value represents the number of erasures per block.

If the flash memory is programmed/erased n times, each block can be erased n times.

i.e. If 4-word write is performed in 512 different addresses in the block A of 4 Kbyte and then the block is erased, it is considered the programming/erasure is performed just once.

However a write in the same address more than once for one erasure is disabled. (overwrite disabled).

2. The data retention time includes the periods when the supply voltage is not applied and no clock is provided.

3. This data retention includes 3000 hours in  $T_a = 125^\circ\text{C}$  and 7000 hours in  $T_a = 85^\circ\text{C}$ .

4. Please contact a Renesas sales office regarding data retention time other than the above.

**Table 5.9 E<sup>2</sup>dataFlash Electrical Characteristics**  
**( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted)**

| Symbol   | Characteristic                                                   |                                              | Value  |      |      | Unit  |
|----------|------------------------------------------------------------------|----------------------------------------------|--------|------|------|-------|
|          |                                                                  |                                              | Min.   | Typ. | Max. |       |
| —        | Programming and erasure endurance of flash memory <sup>(1)</sup> |                                              | 100000 |      |      | times |
| —        | Word program time                                                |                                              |        | 100  | 2000 | μs    |
| —        | Block erasure time                                               | 32 byte block                                |        | 15   | 200  | ms    |
| $t_{PS}$ | Flash memory circuit start-up stabilization time                 |                                              |        | 35   | 50   | μs    |
| —        | Data retention <sup>(2)</sup>                                    | $T_a = 55^{\circ}\text{C}$ <sup>(3, 4)</sup> | 20     |      |      | years |

Notes:

1. Program/erase definition

This value represents the number of erasure per block.

If the flash memory is programmed/erased n times, each block can be erased n times.

i.e. If a word write is performed in different 16 addresses in a block and then the block is erased, it is considered the programming/erasure is performed just once. However a write in the same address more than once for one erasure is disabled. (overwrite disabled).

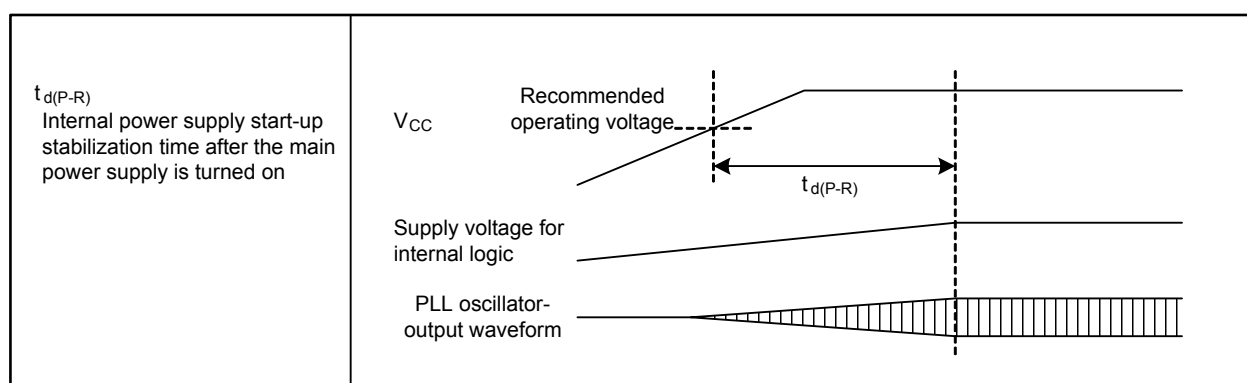
2. The data retention time includes the periods when the supply voltage is not applied and no clock is provided.

3. This data retention includes 3000 hours in  $T_a = 125^{\circ}\text{C}$  and 7000 hours in  $T_a = 85^{\circ}\text{C}$ .

4. Please contact a Renesas sales office regarding data retention time other than the above.

**Table 5.10 Power Supply Circuit Timing Characteristics**  
**( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted)**

| Symbol       | Characteristic                                                                             | Measurement condition | Value |      |      | Unit |
|--------------|--------------------------------------------------------------------------------------------|-----------------------|-------|------|------|------|
|              |                                                                                            |                       | Min.  | Typ. | Max. |      |
| $t_{d(P-R)}$ | Internal power supply start-up stabilization time after the main power supply is turned on |                       |       |      | 2    | ms   |



**Figure 5.3 Power Supply Circuit Timing**

**Table 5.11 Electrical Characteristics of Voltage Regulator for Internal Logic**  
**( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted)**

| Symbol     | Characteristics | Measurement condition | Value |      |      | Unit |
|------------|-----------------|-----------------------|-------|------|------|------|
|            |                 |                       | Min.  | Typ. | Max. |      |
| $V_{VDC1}$ | Output voltage  |                       |       | 1.5  |      | V    |

**Table 5.12 Electrical Characteristics of Low Voltage Detector**  
**( $V_{CC} = 4.2$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted)**

| Symbol                    | Characteristics                              | Measurement condition                          | Value |      |           | Unit    |
|---------------------------|----------------------------------------------|------------------------------------------------|-------|------|-----------|---------|
|                           |                                              |                                                | Min.  | Typ. | Max.      |         |
| $\Delta V_{det}$          | Detected voltage error                       |                                                |       |      | $\pm 0.2$ | V       |
| $V_{det(R)} - V_{det(F)}$ | Hysteresis width                             |                                                | 0     |      |           | V       |
| —                         | Self-consuming current                       | $V_{CC} = 5.0$ V, low voltage detector enabled |       | 4    |           | $\mu A$ |
| $t_{d(E-A)}$              | Operation start time of low voltage detector |                                                |       |      | 150       | $\mu s$ |

**Table 5.13 Electrical Characteristics of Oscillator**  
**( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted)**

| Symbol            | Characteristics                      | Measurement condition | Value |      |      | Unit |
|-------------------|--------------------------------------|-----------------------|-------|------|------|------|
|                   |                                      |                       | Min.  | Typ. | Max. |      |
| $f_{SO(PLL)}$     | PLL clock self-oscillation frequency |                       | 35    | 50   | 80   | MHz  |
| $t_{LOCK(PLL)}$   | PLL lock time (1, 2)                 | $f_{(XRef)} = 4$ MHz  |       |      | 1    | ms   |
| $t_{jitter(p-p)}$ | PLL jitter period (p-p)              |                       |       |      | 2.0  | ns   |
| $f_{(OCO)}$       | On-chip oscillator frequency         |                       | 94    | 125  | 156  | kHz  |

Notes:

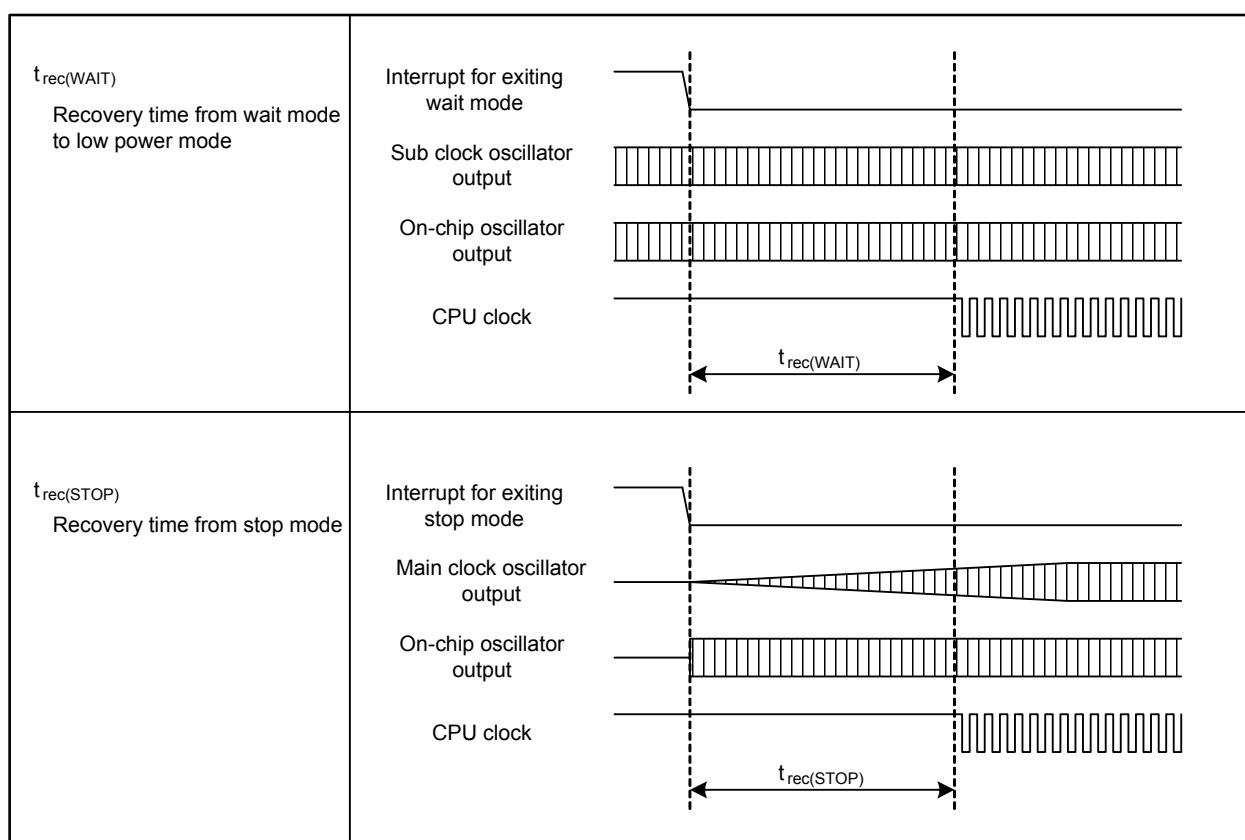
1. This value is applicable only when the main clock oscillation is stable.
2. This value is the time until the PLF1 bit in the PLS register becomes 1.

**Table 5.14 Electrical Characteristics of Clock Circuitry**  
**( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted)**

| Symbol          | Characteristics                                | Measurement condition | Value |      |      | Unit    |
|-----------------|------------------------------------------------|-----------------------|-------|------|------|---------|
|                 |                                                |                       | Min.  | Typ. | Max. |         |
| $t_{rec(WAIT)}$ | Recovery time from wait mode to low power mode |                       |       |      | 225  | $\mu s$ |
| $t_{rec(STOP)}$ | Recovery time from stop mode (1)               |                       |       |      | 225  | $\mu s$ |

Note:

1. This recovery time does not include the period until the main clock oscillator is stabilized. The CPU starts operating before the oscillator is stabilized.

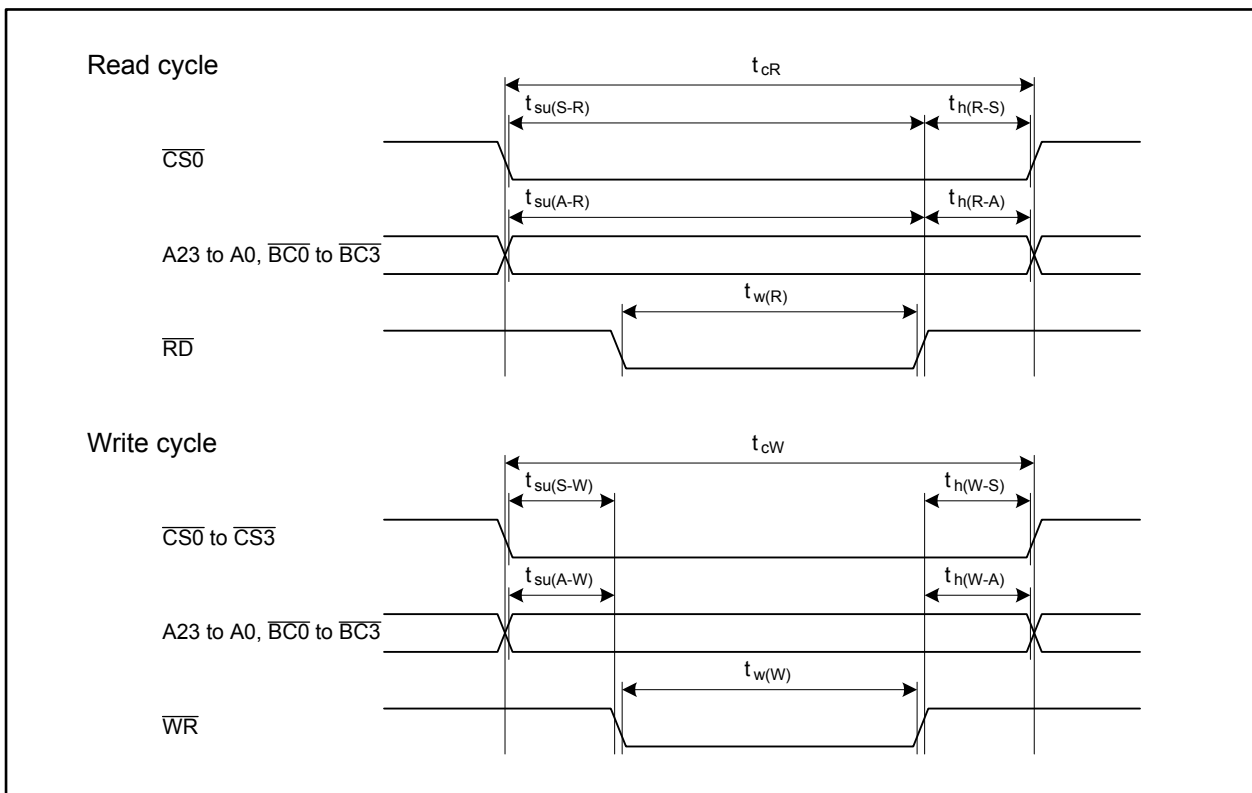


**Figure 5.4 Clock Circuit Timing**

Timing Requirements ( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.15 Flash Memory CPU Rewrite Mode Timing**

| Symbol        | Characteristics                   | Value |      | Unit |
|---------------|-----------------------------------|-------|------|------|
|               |                                   | Min.  | Max. |      |
| $t_{cR}$      | Read cycle time                   | 200   |      | ns   |
| $t_{su(S-R)}$ | Chip-select setup time for read   | 200   |      | ns   |
| $t_{h(R-S)}$  | Chip-select hold time after read  | 0     |      | ns   |
| $t_{su(A-R)}$ | Address setup time for read       | 200   |      | ns   |
| $t_{h(R-A)}$  | Address hold time after read      | 0     |      | ns   |
| $t_{w(R)}$    | Read pulse width                  | 100   |      | ns   |
| $t_{cW}$      | Write cycle time                  | 200   |      | ns   |
| $t_{su(S-W)}$ | Chip-select setup time for write  | 0     |      | ns   |
| $t_{h(W-S)}$  | Chip-select hold time after write | 30    |      | ns   |
| $t_{su(A-W)}$ | Address setup time for write      | 0     |      | ns   |
| $t_{h(W-A)}$  | Address hold time after write     | 30    |      | ns   |
| $t_{w(W)}$    | Write pulse width                 | 50    |      | ns   |



**Figure 5.5 Flash Memory CPU Rewrite Mode Timing**

$$V_{CC} = 5\text{ V}$$

**Table 5.16 Electrical Characteristics (1/3)**

( $V_{CC} = 4.2$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = T_{opr}$ , and  $f_{(CPU)} = 48\text{ MHz}$ , unless otherwise noted)

| Symbol   | Characteristic            |                                                                                                                                                            | Measurement condition              | Value          |      |          | Unit |
|----------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|----------------|------|----------|------|
|          |                           |                                                                                                                                                            |                                    | Min.           | Typ. | Max.     |      |
| $V_{OH}$ | High level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_3 to P9_7 | $I_{OH} = -5\text{ mA}$            | $V_{CC} - 2.0$ |      | $V_{CC}$ | V    |
|          |                           | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_3 to P9_7 | $I_{OH} = -200\text{ }\mu\text{A}$ | $V_{CC} - 0.3$ |      | $V_{CC}$ | V    |
| $V_{OL}$ | Low level output voltage  | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_3 to P9_7 | $I_{OL} = 5\text{ mA}$             |                |      | 2.0      | V    |
|          |                           | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_3 to P9_7 | $I_{OL} = 200\text{ }\mu\text{A}$  |                |      | 0.45     | V    |

$$V_{CC} = 5 \text{ V}$$

**Table 5.17 Electrical Characteristics (2/3) ( $V_{CC} = 4.2$  to  $5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_a = T_{opr}$ , and  $f_{CPU} = 48 \text{ MHz}$ , unless otherwise noted)**

| Symbol            | Characteristic           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Measurement condition | Value |      |      | Unit             |
|-------------------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-------|------|------|------------------|
|                   |                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                       | Min.  | Typ. | Max. |                  |
| $V_{T+} - V_{T-}$ | Hysteresis               | NMI, $\overline{\text{INT0}}$ to $\overline{\text{INT5}}$ , TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, $\overline{\text{CTS0}}$ to $\overline{\text{CTS4}}$ , CLK0 to CLK4, RXD0 to RXD4, SCL0 to SCL2, SDA0 to SDA2, $\overline{\text{SS0}}$ to $\overline{\text{SS2}}$ , SRXD0 to SRXD2, $\overline{\text{ADTRG}}$ , IIO0_0 to IIO0_7, UD0A, UD0B, $\overline{\text{SCS0}}$ , SSCK0, SSI0, SSO0, LININ, CAN0IN, CAN1IN, $\overline{\text{CAN0WU}}$ , $\overline{\text{CAN1WU}}$ |                       | 0.2   |      | 1.0  | V                |
|                   |                          | $\overline{\text{RESET}}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                       | 0.2   |      | 1.8  | V                |
| $I_{IH}$          | High level input current | XIN, $\overline{\text{RESET}}$ , CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_7, P9_1, P9_3 to P9_7                                                                                                                                                                                                                                                                                        | $V_I = 5 \text{ V}$   |       |      | 1.0  | $\mu\text{A}$    |
| $I_{IL}$          | Low level input current  | XIN, $\overline{\text{RESET}}$ , CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_7, P9_1, P9_3 to P9_7                                                                                                                                                                                                                                                                                        | $V_I = 0 \text{ V}$   |       |      | -1.0 | $\mu\text{A}$    |
| $R_{PULLUP}$      | Pull-up resistor         | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_1, P9_3 to P9_7                                                                                                                                                                                                                                                                                                                         | $V_I = 0 \text{ V}$   | 30    | 50   | 170  | $\text{k}\Omega$ |
| $R_{fXIN}$        | Feedback resistor        | XIN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                       |       | 1.5  |      | $\text{M}\Omega$ |
| $R_{fXCIN}$       | Feedback resistor        | XCIN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                       |       | 15   |      | $\text{M}\Omega$ |

$$V_{CC} = 5 \text{ V}$$

**Table 5.18 Electrical Characteristics (3/3)****( $V_{CC} = 4.2$  to  $5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)**

| Symbol   | Characteristic       | Measurement condition                                                                                                                                                       | Value |      |      | Unit          |
|----------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|------|---------------|
|          |                      |                                                                                                                                                                             | Min.  | Typ. | Max. |               |
| $I_{CC}$ | Power supply current | In single-chip mode, output pins are left open and others are connected to $V_{SS}$                                                                                         |       | 31   | 48   | mA            |
|          |                      | XIN-XOUT<br>Drive power: low                                                                                                                                                |       | 7    |      | mA            |
|          |                      | XCIN-XCOUT<br>Drive power: low                                                                                                                                              |       | 1.2  |      | mA            |
|          |                      | $f_{(CPU)} = f_{(BCLK)} = 32.768 \text{ kHz}$ ,<br>Active: XCIN,<br>Stopped: XIN, PLL, OCO,<br>Main regulator: shutdown                                                     |       | 220  |      | $\mu\text{A}$ |
|          |                      | $f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4 \text{ kHz}$ ,<br>Active: OCO,<br>Stopped: XIN, PLL, XCIN,<br>Main regulator: shutdown                                                |       | 230  |      | $\mu\text{A}$ |
|          |                      | $f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256 \text{ MHz}$ ,<br>$f_{(XIN)} = 8 \text{ MHz}$ ,<br>Active: XIN,<br>Stopped: PLL, XCIN, OCO,<br>$T_a = 25^\circ\text{C}$ , Wait mode |       | 960  | 1600 | $\mu\text{A}$ |
|          |                      | $f_{(CPU)} = f_{(BCLK)} = 32.768 \text{ kHz}$ ,<br>Active: XCIN,<br>Stopped: XIN, PLL, OCO,<br>Main regulator: shutdown,<br>$T_a = 25^\circ\text{C}$ , Wait mode            |       | 8    | 140  | $\mu\text{A}$ |
|          |                      | $f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4 \text{ kHz}$ ,<br>Active: OCO,<br>Stopped: XIN, PLL, XCIN,<br>Main regulator: shutdown,<br>$T_a = 25^\circ\text{C}$ , Wait mode       |       | 10   | 150  | $\mu\text{A}$ |
|          |                      | Stopped: all clocks,<br>Main regulator: shutdown,<br>$T_a = 25^\circ\text{C}$                                                                                               |       | 5    | 70   | $\mu\text{A}$ |
|          |                      | Stopped: all clocks,<br>Main regulator: shutdown,<br>$T_a = 85^\circ\text{C}$                                                                                               |       |      | 400  | $\mu\text{A}$ |
|          |                      | Stopped: all clocks,<br>Main regulator: shutdown,<br>$T_a = 105^\circ\text{C}$                                                                                              |       |      | 1200 | $\mu\text{A}$ |
|          |                      | Stopped: all clocks,<br>Main regulator: shutdown,<br>$T_a = 125^\circ\text{C}$                                                                                              |       |      | 2000 | $\mu\text{A}$ |

$$V_{CC} = 5 \text{ V}$$

**Table 5.19 A/D Conversion Characteristics** ( $V_{CC} = AV_{CC} = V_{REF} = 4.2 \text{ to } 5.5 \text{ V}$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_a = T_{opr}$ , and  $f_{(BCLK)} = 24 \text{ MHz}$ , unless otherwise noted)

| Symbol              | Characteristic                                   | Measurement condition                                                                                   | Value |      |                  | Unit          |
|---------------------|--------------------------------------------------|---------------------------------------------------------------------------------------------------------|-------|------|------------------|---------------|
|                     |                                                  |                                                                                                         | Min.  | Typ. | Max.             |               |
| —                   | Resolution                                       | $V_{REF} = V_{CC}$                                                                                      |       |      | 10               | Bits          |
| —                   | Absolute error                                   | $V_{REF} = V_{CC} = 5 \text{ V}$<br>AN_0 to AN_4,<br>AN0_0 to AN0_7,<br>AN2_0 to AN2_7,<br>ANEX0, ANEX1 |       |      | $\pm 3$          | LSB           |
|                     |                                                  | External op-amp<br>connection mode                                                                      |       |      | $\pm 7$          | LSB           |
| INL                 | Integral non-linearity<br>error                  | $V_{REF} = V_{CC} = 5 \text{ V}$<br>AN_0 to AN_4,<br>AN0_0 to AN0_7,<br>AN2_0 to AN2_7,<br>ANEX0, ANEX1 |       |      | $\pm 3$          | LSB           |
|                     |                                                  | External op-amp<br>connection mode                                                                      |       |      | $\pm 7$          | LSB           |
| DNL                 | Differential non-linearity<br>error              |                                                                                                         |       |      | $\pm 1$          | LSB           |
| —                   | Offset error                                     |                                                                                                         |       |      | $\pm 3$          | LSB           |
| —                   | Gain error                                       |                                                                                                         |       |      | $\pm 3$          | LSB           |
| R <sub>LADDER</sub> | Resistor ladder                                  | $V_{REF} = V_{CC}$                                                                                      | 4     |      | 20               | k $\Omega$    |
| t <sub>CONV</sub>   | Conversion time<br>(10 bits)                     | $\phi_{AD} = 16 \text{ MHz}$ , with sample and hold<br>function                                         | 2.06  |      |                  | $\mu\text{s}$ |
|                     |                                                  | $\phi_{AD} = 16 \text{ MHz}$ , without sample and hold<br>function                                      | 3.69  |      |                  | $\mu\text{s}$ |
| t <sub>CONV</sub>   | Conversion time<br>(8 bits)                      | $\phi_{AD} = 16 \text{ MHz}$ , with sample and hold<br>function                                         | 1.75  |      |                  | $\mu\text{s}$ |
|                     |                                                  | $\phi_{AD} = 16 \text{ MHz}$ , without sample and hold<br>function                                      | 3.06  |      |                  | $\mu\text{s}$ |
| t <sub>SAMP</sub>   | Sampling time                                    | $\phi_{AD} = 16 \text{ MHz}$                                                                            | 0.188 |      |                  | $\mu\text{s}$ |
| V <sub>IA</sub>     | Analog input voltage                             |                                                                                                         | 0     |      | V <sub>REF</sub> | V             |
| $\phi_{AD}$         | Operating clock<br>frequency                     | without sample and hold function                                                                        | 0.25  |      | 16               | MHz           |
|                     |                                                  | with sample and hold function                                                                           | 1     |      | 16               | MHz           |
| R <sub>PU(AS)</sub> | Pull-up resistor for open-<br>circuit detection  |                                                                                                         | 5     | 10   | 15               | k $\Omega$    |
| R <sub>PD(AS)</sub> | Pull-down resistor for<br>open-circuit detection |                                                                                                         | 5     | 10   | 15               | k $\Omega$    |

$$V_{CC} = 5 \text{ V}$$

Timing Requirements ( $V_{CC} = 4.2$  to  $5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.20 External Clock Input**

| Symbol      | Characteristic                              | Value |      | Unit |
|-------------|---------------------------------------------|-------|------|------|
|             |                                             | Min.  | Max. |      |
| $t_{C(X)}$  | External clock input period                 | 125   | 250  | ns   |
| $t_{W(XH)}$ | External clock input high level pulse width | 50    |      | ns   |
| $t_{W(XL)}$ | External clock input low level pulse width  | 50    |      | ns   |
| $t_{r(X)}$  | External clock input rise time              |       | 5    | ns   |
| $t_{f(X)}$  | External clock input fall time              |       | 5    | ns   |
| $t_W / t_C$ | External clock input duty                   | 40    | 60   | %    |

$$V_{CC} = 5\text{ V}$$

Timing Requirements ( $V_{CC} = 4.2$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.21 Timer A Input (Counting input in event counter mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{C(TA)}$  | TAiIN input clock period           | 200   |      | ns   |
| $t_{W(TAH)}$ | TAiIN input high level pulse width | 80    |      | ns   |
| $t_{W(TAL)}$ | TAiIN input low level pulse width  | 80    |      | ns   |

**Table 5.22 Timer A Input (Gating input in timer mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{C(TA)}$  | TAiIN input clock period           | 400   |      | ns   |
| $t_{W(TAH)}$ | TAiIN input high level pulse width | 180   |      | ns   |
| $t_{W(TAL)}$ | TAiIN input low level pulse width  | 180   |      | ns   |

**Table 5.23 Timer A Input (External trigger input in one-shot timer mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{C(TA)}$  | TAiIN input clock period           | 200   |      | ns   |
| $t_{W(TAH)}$ | TAiIN input high level pulse width | 80    |      | ns   |
| $t_{W(TAL)}$ | TAiIN input low level pulse width  | 80    |      | ns   |

**Table 5.24 Timer A Input (External trigger input in pulse-width modulation mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{W(TAH)}$ | TAiIN input high level pulse width | 80    |      | ns   |
| $t_{W(TAL)}$ | TAiIN input low level pulse width  | 80    |      | ns   |

**Table 5.25 Timer A Input (Increment/decrement count switching input in event counter mode)**

| Symbol           | Characteristic                      | Value |      | Unit |
|------------------|-------------------------------------|-------|------|------|
|                  |                                     | Min.  | Max. |      |
| $t_{C(UP)}$      | TAiOUT input clock period           | 2000  |      | ns   |
| $t_{W(UPH)}$     | TAiOUT input high level pulse width | 1000  |      | ns   |
| $t_{W(UPL)}$     | TAiOUT input low level pulse width  | 1000  |      | ns   |
| $t_{Su(UP-TIN)}$ | TAiOUT input setup time             | 400   |      | ns   |
| $t_h(TIN-UP)$    | TAiOUT input hold time              | 400   |      | ns   |

$$V_{CC} = 5\text{ V}$$

Timing Requirements ( $V_{CC} = 4.2$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.26 Timer B Input (Counting input in event counter mode)**

| Symbol       | Characteristic                                           | Value |      | Unit |
|--------------|----------------------------------------------------------|-------|------|------|
|              |                                                          | Min.  | Max. |      |
| $t_{C(TB)}$  | TBiIN input clock period (one edge counting)             | 200   |      | ns   |
| $t_{W(TBH)}$ | TBiIN input high level pulse width (one edge counting)   | 80    |      | ns   |
| $t_{W(TBL)}$ | TBiIN input low level pulse width (one edge counting)    | 80    |      | ns   |
| $t_{C(TB)}$  | TBiIN input clock period (both edges counting)           | 200   |      | ns   |
| $t_{W(TBH)}$ | TBiIN input high level pulse width (both edges counting) | 80    |      | ns   |
| $t_{W(TBL)}$ | TBiIN input low level pulse width (both edges counting)  | 80    |      | ns   |

**Table 5.27 Timer B Input (Pulse period measure mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{C(TB)}$  | TBiIN input clock period           | 400   |      | ns   |
| $t_{W(TBH)}$ | TBiIN input high level pulse width | 180   |      | ns   |
| $t_{W(TBL)}$ | TBiIN input low level pulse width  | 180   |      | ns   |

**Table 5.28 Timer B Input (Pulse-width measure mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{C(TB)}$  | TBiIN input clock period           | 400   |      | ns   |
| $t_{W(TBH)}$ | TBiIN input high level pulse width | 180   |      | ns   |
| $t_{W(TBL)}$ | TBiIN input low level pulse width  | 180   |      | ns   |

$$V_{CC} = 5\text{ V}$$

Timing Requirements ( $V_{CC} = 4.2$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.29 Serial Interface**

| Symbol        | Characteristic                    | Value |      | Unit |
|---------------|-----------------------------------|-------|------|------|
|               |                                   | Min.  | Max. |      |
| $t_{C(CK)}$   | CLKi input clock period           | 200   |      | ns   |
| $t_{W(CKH)}$  | CLKi input high level pulse width | 80    |      | ns   |
| $t_{W(CKL)}$  | CLKi input low level pulse width  | 80    |      | ns   |
| $t_{Su(D-C)}$ | RXD <sub>i</sub> input setup time | 80    |      | ns   |
| $t_{h(C-D)}$  | RXD <sub>i</sub> input hold time  | 90    |      | ns   |

**Table 5.30 A/D Trigger Input**

| Symbol       | Characteristic                                                                      | Value                 |      | Unit |
|--------------|-------------------------------------------------------------------------------------|-----------------------|------|------|
|              |                                                                                     | Min.                  | Max. |      |
| $t_{W(ADH)}$ | ADTRG input high level pulse width<br>Hardware trigger input high level pulse width | $\frac{3}{\phi_{AD}}$ |      | ns   |
| $t_{W(ADL)}$ | ADTRG input low level pulse width<br>Hardware trigger input high level pulse width  | 125                   |      | ns   |

**Table 5.31 External Interrupt INT<sub>i</sub> Input**

| Symbol       | Characteristic                                    |                 | Value              |      | Unit |
|--------------|---------------------------------------------------|-----------------|--------------------|------|------|
|              |                                                   |                 | Min.               | Max. |      |
| $t_{W(INH)}$ | INT <sub>i</sub> input high level pulse width (1) | Edge sensitive  | 250                |      | ns   |
|              |                                                   | Level sensitive | $t_{C(CPU)} + 200$ |      | ns   |
| $t_{W(INL)}$ | INT <sub>i</sub> input low level pulse width (1)  | Edge sensitive  | 250                |      | ns   |
|              |                                                   | Level sensitive | $t_{C(CPU)} + 200$ |      | ns   |

Note:

1. The values are applied in case filtering function is disabled.

$$V_{CC} = 5\text{ V}$$

Timing Requirements ( $V_{CC} = 4.2$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.32 Serial Bus Interface**

| Symbol             | Characteristic                     | Value                     |                          | Unit          |
|--------------------|------------------------------------|---------------------------|--------------------------|---------------|
|                    |                                    | Min.                      | Max.                     |               |
| $f_{(SSCK)}$       | SSCKi frequency                    |                           | 4                        | MHz           |
| $t_{c(SSCK)}$      | SSCKi clock period                 | 250                       |                          | ns            |
| $t_{w(SSCKH)}$     | SSCKi input high level pulse width | $0.35 \times t_{c(SSCK)}$ | $0.6 \times t_{c(SSCK)}$ | ns            |
| $t_{w(SSCKL)}$     | SSCKi input low level pulse width  | $0.35 \times t_{c(SSCK)}$ | $0.6 \times t_{c(SSCK)}$ | ns            |
| $t_{r(SSCK)}$      | SSCKi input rising time            |                           | 1                        | $\mu\text{s}$ |
| $t_{f(SSCK)}$      | SSCKi input falling time           |                           | 1                        | $\mu\text{s}$ |
| $t_{su(SCS-SSCK)}$ | SCSi input setup time              | $t_{c(BCLK)} + 50$        |                          | ns            |
| $t_{h(SSCK-SCS)}$  | SCSi input hold time               | $t_{c(BCLK)} + 50$        |                          | ns            |
| $t_{su(SSi-SSCK)}$ | SSi input setup time               | 80                        |                          | ns            |
| $t_{h(SSCK-SSi)}$  | SSi input hold time                | 10                        |                          | ns            |
| $t_{su(SSO-SSCK)}$ | SSO input setup time               | 80                        |                          | ns            |
| $t_{h(SSCK-SSO)}$  | SSO input hold time                | 20                        |                          | ns            |

$$V_{CC} = 5\text{ V}$$

Switching Characteristics ( $V_{CC} = 4.2$  to  $5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.33 Serial Interface**

| Symbol       | Characteristic         | Measurement condition | Value |      | Unit |
|--------------|------------------------|-----------------------|-------|------|------|
|              |                        |                       | Min.  | Max. |      |
| $t_{d(C-Q)}$ | TXDi output delay time | Refer to Figure 5.6   |       | 80   | ns   |
| $t_{h(C-Q)}$ | TXDi output hold time  |                       | 0     |      | ns   |

**Table 5.34 Serial Bus Interface**

| Symbol             | Characteristic                                           | Measurement condition | Value                         |                                | Unit |
|--------------------|----------------------------------------------------------|-----------------------|-------------------------------|--------------------------------|------|
|                    |                                                          |                       | Min.                          | Max.                           |      |
| $t_{w(SSCKH)}$     | SSCKi output high level pulse width                      | Refer to Figure 5.6   | $0.35 \times t_{c(SSCK)}$     | $0.6 \times t_{c(SSCK)}$       | ns   |
| $t_{w(SSCKL)}$     | SSCKi output low level pulse width                       |                       | $0.35 \times t_{c(SSCK)}$     | $0.6 \times t_{c(SSCK)}$       | ns   |
| $t_{r(SSCK)}$      | SSCKi output rising time                                 |                       |                               | 20                             | ns   |
| $t_{f(SSCK)}$      | SSCKi output falling time                                |                       |                               | 20                             | ns   |
| $t_{d(SCS-SSCK)}$  | SSCKi output delay time for SCSi                         |                       |                               | $0.5 \times t_{c(SSCK)} + 20$  | ns   |
| $t_{d(SSCK-SCS)}$  | SCSi output delay time for SSCKi                         |                       | $0.5 \times t_{c(SSCK)} - 20$ |                                | ns   |
| $t_{en(SCS-SSO)}$  | SSOi output enable time                                  |                       |                               | $1.5 \times t_{c(BCLK)} + 100$ | ns   |
| $t_{dis(SCS-SSO)}$ | SSOi output disable time                                 |                       |                               | $1.5 \times t_{c(BCLK)} + 100$ | ns   |
| $t_{en(SCS-SSI)}$  | SSLi output enable time                                  |                       |                               | $1.5 \times t_{c(BCLK)} + 100$ | ns   |
| $t_{dis(SCS-SSI)}$ | SSLi output disable time                                 |                       |                               | $1.5 \times t_{c(BCLK)} + 100$ | ns   |
| $t_{d(SSCK-SSO)}$  | SSOi output delay time for SSCKi                         |                       |                               | 30                             | ns   |
| $t_{d(SSCK-SSI)}$  | SSLi output delay time for SSCKi                         |                       |                               | 85                             | ns   |
| $t_{rec(SCS)}$     | SCSi output high level period in continuous transmission |                       |                               | $0.625 \times t_{c(SSCK)}$     | ns   |

$$V_{CC} = 3.3 \text{ V}$$

**Table 5.35 Electrical Characteristics (1/3) ( $V_{CC} = 3.0$  to  $3.6 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_a = T_{opr}$ , and  $f_{(CPU)} = 48 \text{ MHz}$ , unless otherwise noted)**

| Symbol   | Characteristic            |                                                                                                                                                            | Measurement condition    | Value          |      |          | Unit |
|----------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------|------|----------|------|
|          |                           |                                                                                                                                                            |                          | Min.           | Typ. | Max.     |      |
| $V_{OH}$ | High level output voltage | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_3 to P9_7 | $I_{OH} = -1 \text{ mA}$ | $V_{CC} - 0.6$ |      | $V_{CC}$ | V    |
| $V_{OL}$ | Low level output voltage  | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_3 to P9_7 | $I_{OL} = 1 \text{ mA}$  |                |      | 0.5      | V    |

$$V_{CC} = 3.3 \text{ V}$$

**Table 5.36 Electrical Characteristics (2/3) ( $V_{CC} = 3.0$  to  $3.6 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_a = T_{opr}$ , and  $f_{CPU} = 48 \text{ MHz}$ , unless otherwise noted)**

| Symbol            | Characteristic           | Measurement condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Value                 |      |      | Unit             |
|-------------------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|------|------|------------------|
|                   |                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Min.                  | Typ. | Max. |                  |
| $V_{T+} - V_{T-}$ | Hysteresis               | NMI, $\overline{\text{INT0}}$ to $\overline{\text{INT5}}$ , TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, $\overline{\text{CTS0}}$ to $\overline{\text{CTS4}}$ , CLK0 to CLK4, RXD0 to RXD4, SCL0 to SCL2, SDA0 to SDA2, $\overline{\text{SS0}}$ to $\overline{\text{SS2}}$ , SRXD0 to SRXD2, $\overline{\text{ADTRG}}$ , IIO0_0 to IIO0_7, UD0A, UD0B, $\overline{\text{SCS0}}$ , SSCK0, SSI0, SSO0, LININ, CAN0IN, CAN1IN, $\overline{\text{CAN0WU}}$ , $\overline{\text{CAN1WU}}$ | 0.2                   |      | 1.0  | V                |
|                   |                          | $\overline{\text{RESET}}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0.2                   |      | 1.8  | V                |
| $I_{IH}$          | High level input current | XIN, $\overline{\text{RESET}}$ , CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_7, P9_1, P9_3 to P9_7                                                                                                                                                                                                                                                                                        | $V_I = 3.3 \text{ V}$ |      |      | $\mu\text{A}$    |
| $I_{IL}$          | Low level input current  | XIN, $\overline{\text{RESET}}$ , CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_7, P9_1, P9_3 to P9_7                                                                                                                                                                                                                                                                                        | $V_I = 0 \text{ V}$   |      |      | $\mu\text{A}$    |
| $R_{PULLUP}$      | Pull-up resistor         | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_5, P6_7, P7_0, P7_4 to P7_6, P8_2 to P8_4, P8_6, P8_7, P9_1, P9_3 to P9_7                                                                                                                                                                                                                                                                                                                         | $V_I = 0 \text{ V}$   |      |      | $\text{k}\Omega$ |
| $R_{fXIN}$        | Feedback resistor        | XIN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                       | 3    |      | $\text{M}\Omega$ |
| $R_{fXCIN}$       | Feedback resistor        | XCIN                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                       | 25   |      | $\text{M}\Omega$ |

$$V_{CC} = 3.3 \text{ V}$$

**Table 5.37 Electrical Characteristics (3/3)****( $V_{CC} = 3.0$  to  $3.6 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)**

| Symbol   | Characteristic       | Measurement condition                                                                                                                                                       | Value |      |      | Unit          |
|----------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|------|---------------|
|          |                      |                                                                                                                                                                             | Min.  | Typ. | Max. |               |
| $I_{CC}$ | Power supply current | In single-chip mode, output pins are left open and others are connected to $V_{SS}$                                                                                         |       |      |      |               |
|          |                      | $f_{(CPU)} = 48 \text{ MHz}$ , $f_{(BCLK)} = 24 \text{ MHz}$ ,<br>$f_{(XIN)} = 8 \text{ MHz}$ ,<br>Active: XIN, PLL,<br>Stopped: XCIN, OCO                                  |       | 31   | 48   | mA            |
|          |                      | XIN-XOUT<br>Drive power: low                                                                                                                                                |       | 7    |      | mA            |
|          |                      | $f_{(CPU)} = f_{SO(PLL)}/24 \text{ MHz}$ ,<br>Active: PLL (self-oscillation),<br>Stopped: XIN, XCIN, OCO                                                                    |       |      |      |               |
|          |                      | XCIN-XCOUT<br>Drive power: low                                                                                                                                              |       |      |      |               |
|          |                      | $f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256 \text{ MHz}$ ,<br>$f_{(XIN)} = 8 \text{ MHz}$ ,<br>Active: XIN,<br>Stopped: PLL, XCIN, OCO                                          |       | 670  |      | $\mu\text{A}$ |
|          |                      | $f_{(CPU)} = f_{(BCLK)} = 32.768 \text{ kHz}$ ,<br>Active: XCIN,<br>Stopped: XIN, PLL, OCO,<br>Main regulator: shutdown                                                     |       | 180  |      | $\mu\text{A}$ |
|          |                      | $f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4 \text{ kHz}$ ,<br>Active: OCO,<br>Stopped: XIN, PLL, XCIN,<br>Main regulator: shutdown                                                |       | 190  |      | $\mu\text{A}$ |
|          |                      | $f_{(CPU)} = f_{(BCLK)} = f_{(XIN)}/256 \text{ MHz}$ ,<br>$f_{(XIN)} = 8 \text{ MHz}$ ,<br>Active: XIN,<br>Stopped: PLL, XCIN, OCO,<br>$T_a = 25^\circ\text{C}$ , Wait mode |       | 500  | 900  | $\mu\text{A}$ |
|          |                      | $f_{(CPU)} = f_{(BCLK)} = 32.768 \text{ kHz}$ ,<br>Active: XCIN,<br>Stopped: XIN, PLL, OCO,<br>Main regulator: shutdown,<br>$T_a = 25^\circ\text{C}$ , Wait mode            |       | 8    | 140  | $\mu\text{A}$ |
|          |                      | $f_{(CPU)} = f_{(BCLK)} = f_{(OCO)}/4 \text{ kHz}$ ,<br>Active: OCO,<br>Stopped: XIN, PLL, XCIN,<br>Main regulator: shutdown,<br>$T_a = 25^\circ\text{C}$ , Wait mode       |       | 10   | 150  | $\mu\text{A}$ |
|          |                      | Stopped: all clocks,<br>Main regulator: shutdown,<br>$T_a = 25^\circ\text{C}$                                                                                               |       | 5    | 70   | $\mu\text{A}$ |
|          |                      | Stopped: all clocks,<br>Main regulator: shutdown,<br>$T_a = 85^\circ\text{C}$                                                                                               |       |      | 400  | $\mu\text{A}$ |
|          |                      | Stopped: all clocks,<br>Main regulator: shutdown,<br>$T_a = 105^\circ\text{C}$                                                                                              |       |      | 1200 | $\mu\text{A}$ |
|          |                      | Stopped: all clocks,<br>Main regulator: shutdown,<br>$T_a = 125^\circ\text{C}$                                                                                              |       |      | 2000 | $\mu\text{A}$ |

$$V_{CC} = 3.3 \text{ V}$$

**Table 5.38 A/D Conversion Characteristics** ( $V_{CC} = AV_{CC} = V_{REF} = 3.0 \text{ to } 3.6 \text{ V}$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  
 $T_a = T_{opr}$ , and  $f_{(BCLK)} = 24 \text{ MHz}$ , unless otherwise noted)

| Symbol               | Characteristic                                | Measurement condition                                                                                  | Value |      |                  | Unit |
|----------------------|-----------------------------------------------|--------------------------------------------------------------------------------------------------------|-------|------|------------------|------|
|                      |                                               |                                                                                                        | Min.  | Typ. | Max.             |      |
| —                    | Resolution                                    | $V_{REF} = V_{CC}$                                                                                     |       |      | 10               | Bits |
| —                    | Absolute error                                | $V_{REF} = V_{CC} = 3.3 \text{ V}$ AN_0 to AN_4,<br>AN0_0 to AN0_7,<br>AN2_0 to AN2_7,<br>ANEX0, ANEX1 |       |      | ±5               | LSB  |
|                      |                                               | External op-amp connection mode                                                                        |       |      | ±7               | LSB  |
| INL                  | Integral non-linearity error                  | $V_{REF} = V_{CC} = 3.3 \text{ V}$ AN_0 to AN_4,<br>AN0_0 to AN0_7,<br>AN2_0 to AN2_7,<br>ANEX0, ANEX1 |       |      | ±5               | LSB  |
|                      |                                               | External op-amp connection mode                                                                        |       |      | ±7               | LSB  |
| DNL                  | Differential non-linearity error              | $V_{REF} = V_{CC} = 3.3 \text{ V}$                                                                     |       |      | ±1               | LSB  |
| —                    | Offset error                                  |                                                                                                        |       |      | ±3               | LSB  |
| —                    | Gain error                                    |                                                                                                        |       |      | ±3               | LSB  |
| R <sub>LADDER</sub>  | Resistor ladder                               | $V_{REF} = V_{CC}$                                                                                     | 4     |      | 20               | kΩ   |
| t <sub>CONV</sub>    | Conversion time (10 bits)                     | $\phi_{AD} = 10 \text{ MHz}$ ,<br>with sample and hold function                                        | 3.3   |      |                  | μs   |
| t <sub>CONV</sub>    | Conversion time (8 bits)                      | $\phi_{AD} = 10 \text{ MHz}$ ,<br>with sample and hold function                                        | 2.8   |      |                  | μs   |
| t <sub>SAMP</sub>    | Sampling time                                 | $\phi_{AD} = 10 \text{ MHz}$                                                                           | 0.3   |      |                  | μs   |
| V <sub>IA</sub>      | Analog input voltage                          |                                                                                                        | 0     |      | V <sub>REF</sub> | V    |
| $\phi_{AD}$          | Operating clock frequency                     | without sample and hold function                                                                       | 0.25  |      | 10               | MHz  |
|                      |                                               | with sample and hold function                                                                          | 1     |      | 10               | MHz  |
| R <sub>PU(AST)</sub> | Pull-up resistor for open-circuit detection   |                                                                                                        | 5     | 10   | 15               | kΩ   |
| R <sub>PD(AST)</sub> | Pull-down resistor for open-circuit detection |                                                                                                        | 5     | 10   | 15               | kΩ   |

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ( $V_{CC} = 3.0$  to  $3.6 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.39 External Clock Input**

| Symbol      | Characteristic                              | Value |      | Unit |
|-------------|---------------------------------------------|-------|------|------|
|             |                                             | Min.  | Max. |      |
| $t_{C(X)}$  | External clock input period                 | 125   | 250  | ns   |
| $t_{W(XH)}$ | External clock input high level pulse width | 50    |      | ns   |
| $t_{W(XL)}$ | External clock input low level pulse width  | 50    |      | ns   |
| $t_{r(X)}$  | External clock input rise time              |       | 5    | ns   |
| $t_{f(X)}$  | External clock input fall time              |       | 5    | ns   |
| $t_W / t_C$ | External clock input duty                   | 40    | 60   | %    |

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ( $V_{CC} = 3.0$  to  $3.6 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.40 Timer A Input (Counting input in event counter mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{c(TA)}$  | TAiIN input clock period           | 200   |      | ns   |
| $t_{w(TAH)}$ | TAiIN input high level pulse width | 80    |      | ns   |
| $t_{w(TAL)}$ | TAiIN input low level pulse width  | 80    |      | ns   |

**Table 5.41 Timer A Input (Gating input in timer mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{c(TA)}$  | TAiIN input clock period           | 400   |      | ns   |
| $t_{w(TAH)}$ | TAiIN input high level pulse width | 180   |      | ns   |
| $t_{w(TAL)}$ | TAiIN input low level pulse width  | 180   |      | ns   |

**Table 5.42 Timer A Input (External trigger input in one-shot timer mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{c(TA)}$  | TAiIN input clock period           | 200   |      | ns   |
| $t_{w(TAH)}$ | TAiIN input high level pulse width | 80    |      | ns   |
| $t_{w(TAL)}$ | TAiIN input low level pulse width  | 80    |      | ns   |

**Table 5.43 Timer A Input (External trigger input in pulse-width modulation mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{w(TAH)}$ | TAiIN input high level pulse width | 80    |      | ns   |
| $t_{w(TAL)}$ | TAiIN input low level pulse width  | 80    |      | ns   |

**Table 5.44 Timer A Input (Increment/decrement count switching input in event counter mode)**

| Symbol           | Characteristic                      | Value |      | Unit |
|------------------|-------------------------------------|-------|------|------|
|                  |                                     | Min.  | Max. |      |
| $t_{c(UP)}$      | TAiOUT input clock period           | 2000  |      | ns   |
| $t_{w(UPH)}$     | TAiOUT input high level pulse width | 1000  |      | ns   |
| $t_{w(UPL)}$     | TAiOUT input low level pulse width  | 1000  |      | ns   |
| $t_{su(UP-TIN)}$ | TAiOUT input setup time             | 400   |      | ns   |
| $t_h(TIN-UP)$    | TAiOUT input hold time              | 400   |      | ns   |

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ( $V_{CC} = 3.0$  to  $3.6 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.45 Timer B Input (Counting input in event counter mode)**

| Symbol       | Characteristic                                           | Value |      | Unit |
|--------------|----------------------------------------------------------|-------|------|------|
|              |                                                          | Min.  | Max. |      |
| $t_{c(TB)}$  | TBiIN input clock period (one edge counting)             | 200   |      | ns   |
| $t_{w(TBH)}$ | TBiIN input high level pulse width (one edge counting)   | 80    |      | ns   |
| $t_{w(TBL)}$ | TBiIN input low level pulse width (one edge counting)    | 80    |      | ns   |
| $t_{c(TB)}$  | TBiIN input clock period (both edges counting)           | 200   |      | ns   |
| $t_{w(TBH)}$ | TBiIN input high level pulse width (both edges counting) | 80    |      | ns   |
| $t_{w(TBL)}$ | TBiIN input low level pulse width (both edges counting)  | 80    |      | ns   |

**Table 5.46 Timer B Input (Pulse period measure mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{c(TB)}$  | TBiIN input clock period           | 400   |      | ns   |
| $t_{w(TBH)}$ | TBiIN input high level pulse width | 180   |      | ns   |
| $t_{w(TBL)}$ | TBiIN input low level pulse width  | 180   |      | ns   |

**Table 5.47 Timer B Input (Pulse-width measure mode)**

| Symbol       | Characteristic                     | Value |      | Unit |
|--------------|------------------------------------|-------|------|------|
|              |                                    | Min.  | Max. |      |
| $t_{c(TB)}$  | TBiIN input clock period           | 400   |      | ns   |
| $t_{w(TBH)}$ | TBiIN input high level pulse width | 180   |      | ns   |
| $t_{w(TBL)}$ | TBiIN input low level pulse width  | 180   |      | ns   |

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ( $V_{CC} = 3.0$  to  $3.6 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.48 Serial Interface**

| Symbol        | Characteristic                    | Value |      | Unit |
|---------------|-----------------------------------|-------|------|------|
|               |                                   | Min.  | Max. |      |
| $t_{c(CK)}$   | CLKi input clock period           | 200   |      | ns   |
| $t_{w(CKH)}$  | CLKi input high level pulse width | 80    |      | ns   |
| $t_{w(CKL)}$  | CLKi input low level pulse width  | 80    |      | ns   |
| $t_{su(D-C)}$ | RXDi input setup time             | 80    |      | ns   |
| $t_{h(C-D)}$  | RXDi input hold time              | 90    |      | ns   |

**Table 5.49 A/D Trigger Input**

| Symbol       | Characteristic                                                                      | Value                 |      | Unit |
|--------------|-------------------------------------------------------------------------------------|-----------------------|------|------|
|              |                                                                                     | Min.                  | Max. |      |
| $t_{w(ADH)}$ | ADTRG input high level pulse width<br>Hardware trigger input high level pulse width | $\frac{3}{\phi_{AD}}$ |      | ns   |
| $t_{w(ADL)}$ | ADTRG input low level pulse width<br>Hardware trigger input high level pulse width  | 125                   |      | ns   |

**Table 5.50 External Interrupt INTi Input**

| Symbol       | Characteristic                                   |                 | Value              |      | Unit |
|--------------|--------------------------------------------------|-----------------|--------------------|------|------|
|              |                                                  |                 | Min.               | Max. |      |
| $t_{w(INH)}$ | INTi input high level pulse width <sup>(1)</sup> | Edge sensitive  | 250                |      | ns   |
|              |                                                  | Level sensitive | $t_{C(CPU)} + 200$ |      | ns   |
| $t_{w(INL)}$ | INTi input low level pulse width <sup>(1)</sup>  | Edge sensitive  | 250                |      | ns   |
|              |                                                  | Level sensitive | $t_{C(CPU)} + 200$ |      | ns   |

Note:

1. The values are applied in case filtering function is disabled.

$$V_{CC} = 3.3 \text{ V}$$

Timing Requirements ( $V_{CC} = 3.0$  to  $3.6 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.51 Serial Bus Interface**

| Symbol             | Characteristic                     | Value                     |                          | Unit          |
|--------------------|------------------------------------|---------------------------|--------------------------|---------------|
|                    |                                    | Min.                      | Max.                     |               |
| $f_{(SSCK)}$       | SSCKi frequency                    |                           | 4                        | MHz           |
| $t_{c(SSCK)}$      | SSCKi clock period                 | 250                       |                          | ns            |
| $t_{w(SSCKH)}$     | SSCKi input high level pulse width | $0.35 \times t_{c(SSCK)}$ | $0.6 \times t_{c(SSCK)}$ | ns            |
| $t_{w(SSCKL)}$     | SSCKi input low level pulse width  | $0.35 \times t_{c(SSCK)}$ | $0.6 \times t_{c(SSCK)}$ | ns            |
| $t_{r(SSCK)}$      | SSCKi input rising time            |                           | 1                        | $\mu\text{s}$ |
| $t_{f(SSCK)}$      | SSCKi input falling time           |                           | 1                        | $\mu\text{s}$ |
| $t_{su(SCS-SSCK)}$ | SCSi input setup time              | $t_{c(BCLK)} + 50$        |                          | ns            |
| $t_h(SSCK-SCS)$    | SCSi input hold time               | $t_{c(BCLK)} + 50$        |                          | ns            |
| $t_{su(SSi-SSCK)}$ | SSi input setup time               | 100                       |                          | ns            |
| $t_h(SSCK-SSi)$    | SSi input hold time                | 10                        |                          | ns            |
| $t_{su(SSO-SSCK)}$ | SSO input setup time               | 100                       |                          | ns            |
| $t_h(SSCK-SSO)$    | SSO input hold time                | 20                        |                          | ns            |

$$V_{CC} = 3.3 \text{ V}$$

Switching Characteristics ( $V_{CC} = 3.0$  to  $3.6 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ , and  $T_a = T_{opr}$ , unless otherwise noted)

**Table 5.52 Serial Interface**

| Symbol       | Characteristic         | Measurement condition | Value |      | Unit |
|--------------|------------------------|-----------------------|-------|------|------|
|              |                        |                       | Min.  | Max. |      |
| $t_{d(C-Q)}$ | TXDi output delay time | Refer to Figure 5.6   |       | 80   | ns   |
| $t_{h(C-Q)}$ | TXDi output hold time  |                       | 0     |      | ns   |

**Table 5.53 Serial Bus Interface**

| Symbol             | Characteristic                                           | Measurement condition | Value                         |                                | Unit |
|--------------------|----------------------------------------------------------|-----------------------|-------------------------------|--------------------------------|------|
|                    |                                                          |                       | Min.                          | Max.                           |      |
| $t_{w(SSCKH)}$     | SSCKi output high level pulse width                      | Refer to Figure 5.6   | $0.35 \times t_{c(SSCK)}$     | $0.6 \times t_{c(SSCK)}$       | ns   |
| $t_{w(SSCKL)}$     | SSCKi output low level pulse width                       |                       | $0.35 \times t_{c(SSCK)}$     | $0.6 \times t_{c(SSCK)}$       | ns   |
| $t_{r(SSCK)}$      | SSCKi output rising time                                 |                       |                               | 35                             | ns   |
| $t_{f(SSCK)}$      | SSCKi output falling time                                |                       |                               | 35                             | ns   |
| $t_{d(SCS-SSCK)}$  | SSCKi output delay time for SCSi                         |                       |                               | $0.5 \times t_{c(SSCK)} + 40$  | ns   |
| $t_{d(SSCK-SCS)}$  | SCSi output delay time for SSCKi                         |                       | $0.5 \times t_{c(SSCK)} - 40$ |                                | ns   |
| $t_{en(SCS-SSO)}$  | SSOi output enable time                                  |                       |                               | $1.5 \times t_{c(BCLK)} + 100$ | ns   |
| $t_{dis(SCS-SSO)}$ | SSOi output disable time                                 |                       |                               | $1.5 \times t_{c(BCLK)} + 100$ | ns   |
| $t_{en(SCS-SSI)}$  | SSLi output enable time                                  |                       |                               | $1.5 \times t_{c(BCLK)} + 100$ | ns   |
| $t_{dis(SCS-SSI)}$ | SSLi output disable time                                 |                       |                               | $1.5 \times t_{c(BCLK)} + 100$ | ns   |
| $t_{d(SSCK-SSO)}$  | SSOi output delay time for SSCKi                         |                       |                               | 50                             | ns   |
| $t_{d(SSCK-SSI)}$  | SSLi output delay time for SSCKi                         |                       |                               | 120                            | ns   |
| $t_{rec(SCS)}$     | SCSi output high level period in continuous transmission |                       |                               | $0.625 \times t_{c(SSCK)}$     | ns   |

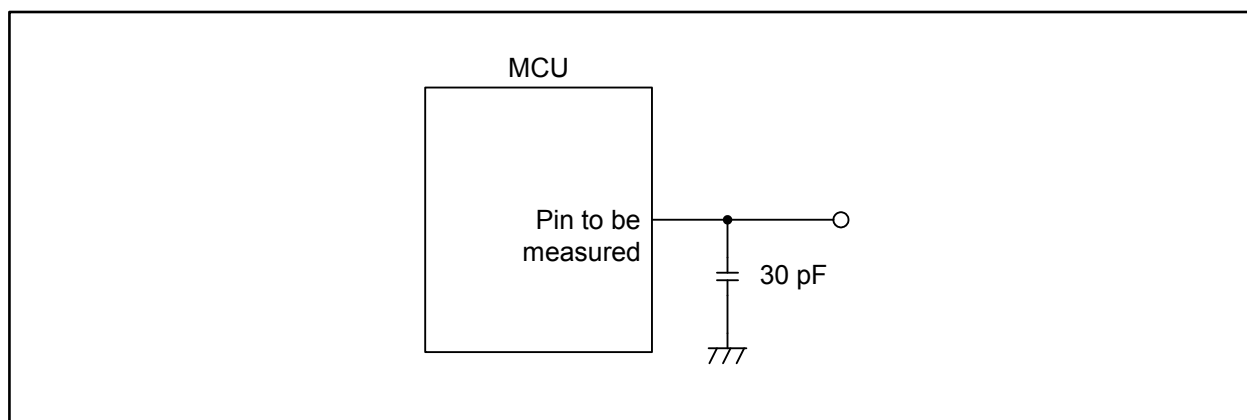


Figure 5.6 Switching Characteristic Measurement Circuit

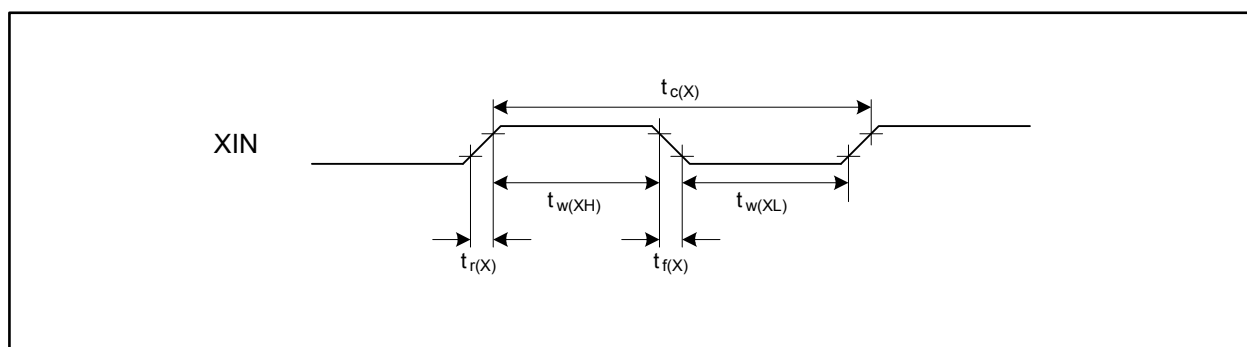


Figure 5.7 External Clock Input Timing

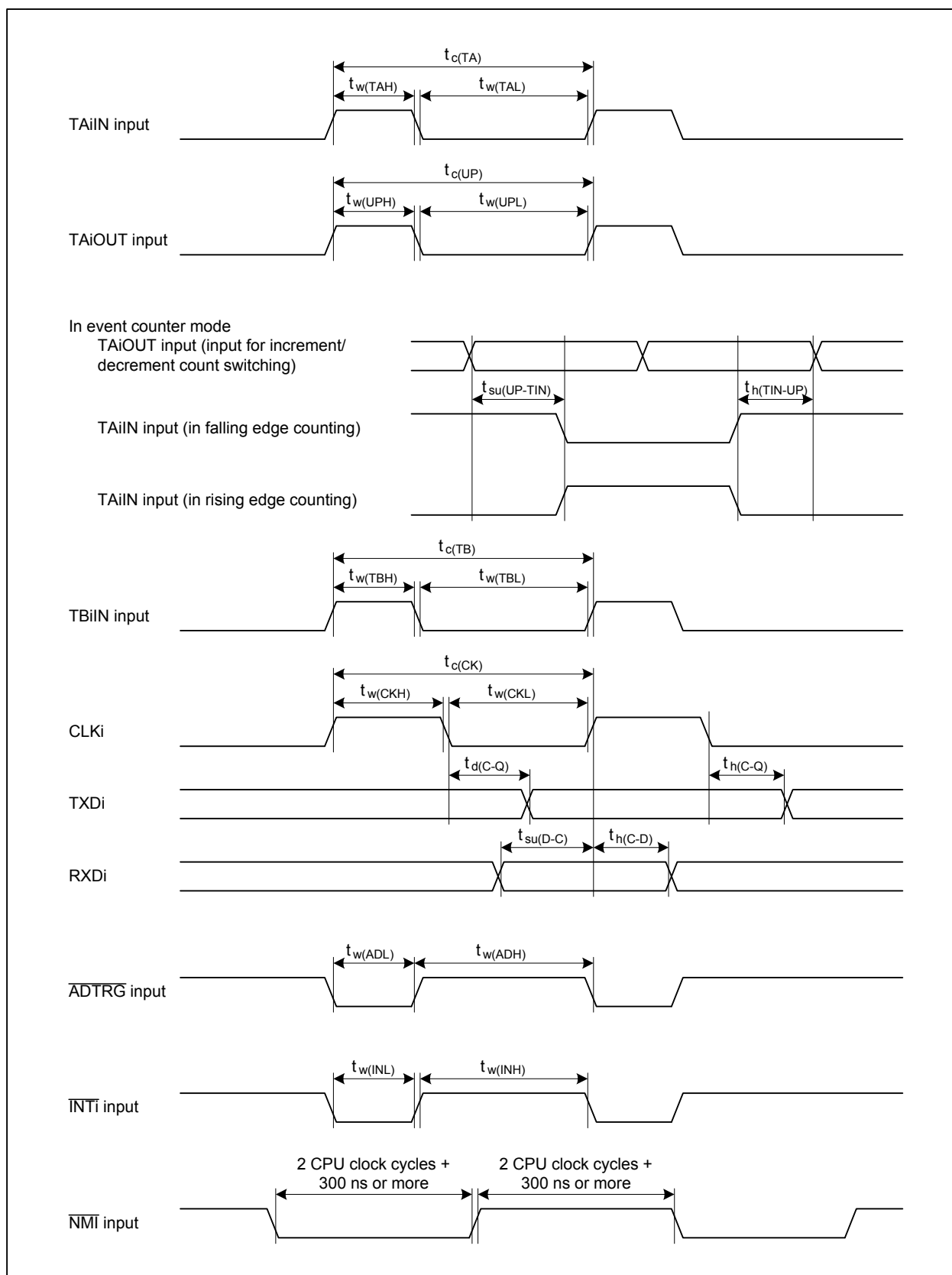


Figure 5.8 Timing of Peripheral Functions

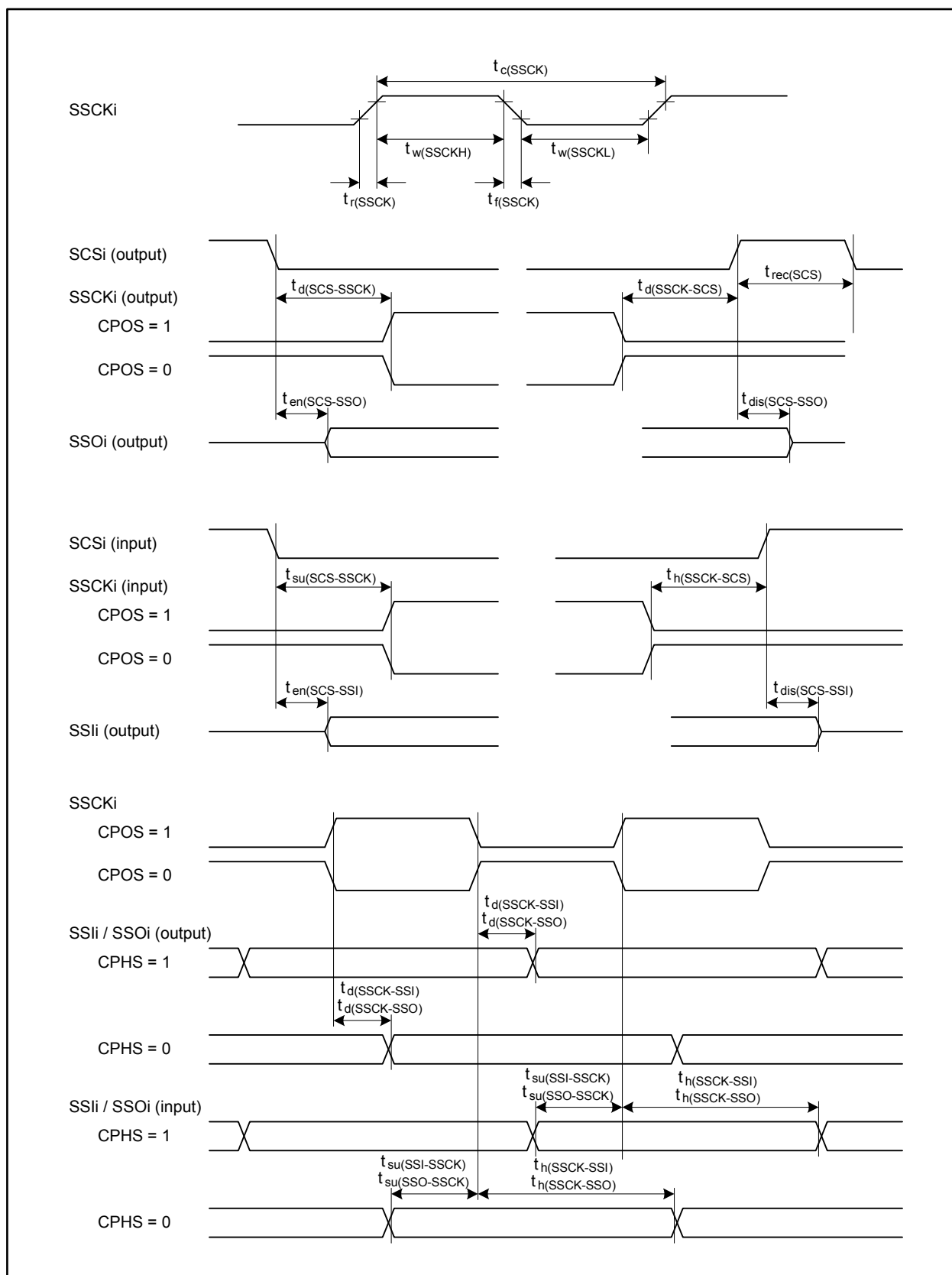
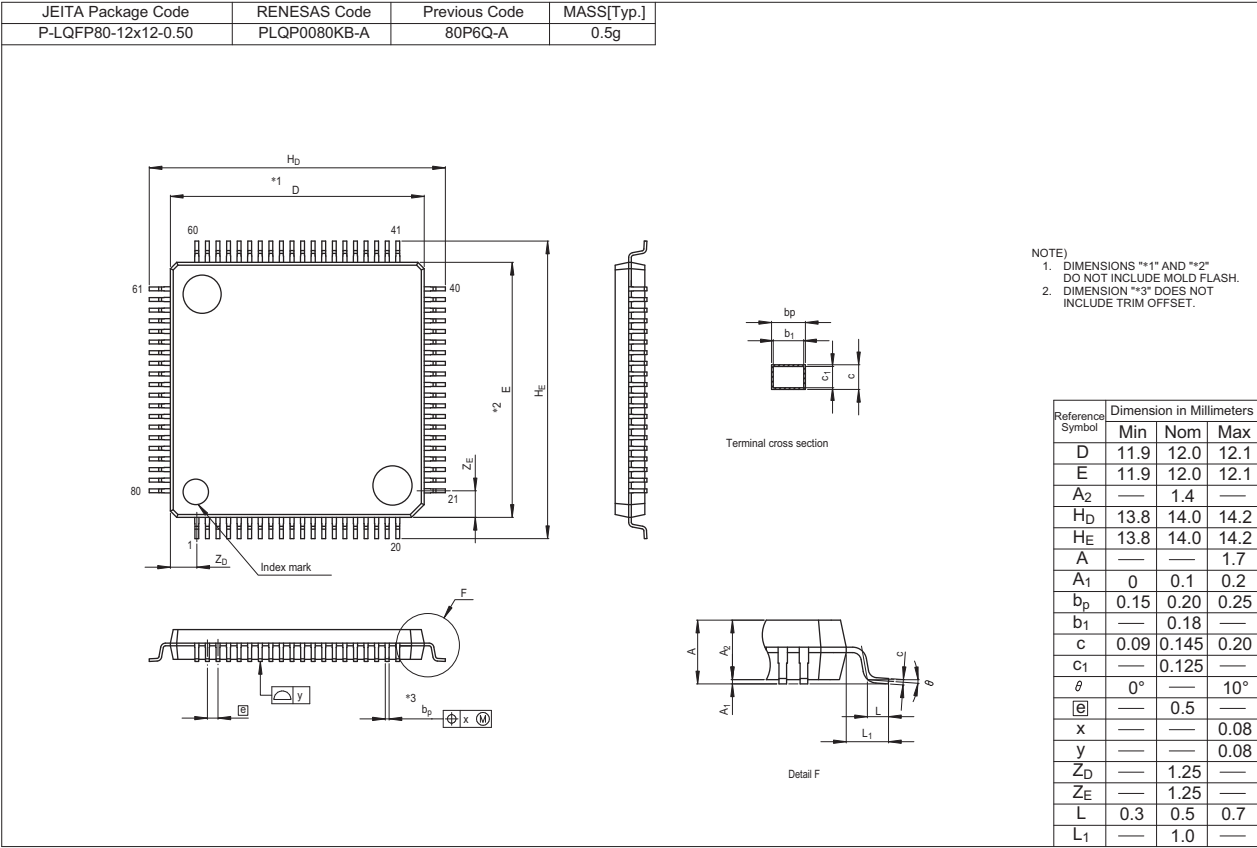


Figure 5.9 Timing of Serial Bus Interface

Appendix 1. Package Dimensions



| REVISION HISTORY | R32C/161 Group Datasheet |
|------------------|--------------------------|
|------------------|--------------------------|

| Rev. | Date         | Description |                                                                                                                                                                                                                                                                                          |
|------|--------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |              | Page        | Summary                                                                                                                                                                                                                                                                                  |
| 0.10 | Feb 14, 2008 | —           | Initial release                                                                                                                                                                                                                                                                          |
| 1.01 | Dec 07, 2009 | —           | Second edition released                                                                                                                                                                                                                                                                  |
|      |              |             | <b>Chapter 1. Overview</b>                                                                                                                                                                                                                                                               |
|      |              | 1           | • Added “(MCUs)” to line 1 of <b>1.1</b>                                                                                                                                                                                                                                                 |
|      |              | 3           | • Changed the following expressions in <b>Table 1.2</b> : “sample & hold” to “sample and hold”, “erase/program” to “program/erase”, “Read protection” to “Security protection”, “ID code check” to “ID code protect”, and “on-board flash reprogramming” to “on-board flash programming” |
|      |              |             | • Added “(SBI)” to unit “Serial Bus Interface” in <b>Table 1.2</b> ; Specified values for current consumption                                                                                                                                                                            |
|      |              | 4           | • Completed “under development” phase of part number R5F64610JFP in <b>Table 1.3</b> ; Updated the table                                                                                                                                                                                 |
|      |              | 5           | • Deleted hyphen before ROM number in <b>Figure 1.1</b>                                                                                                                                                                                                                                  |
|      |              | 6           | • Changed <b>Figure 1.2</b>                                                                                                                                                                                                                                                              |
|      |              | 8           | • Moved four SBI signal lines (pin numbers 36 to 39) in <b>Table 1.4</b> to column “UART / SBI Pin”                                                                                                                                                                                      |
|      |              | 10, 11      | • Changed descriptions “Functional Category” and “Function” in <b>Tables 1.6 and 1.7</b> to “Function” and “Description”, respectively                                                                                                                                                   |
|      |              |             | <b>Chapter 2. Central Processing Unit</b>                                                                                                                                                                                                                                                |
|      |              | —           | • Made major text modifications to this chapter                                                                                                                                                                                                                                          |
|      |              | 12, 13      | • Changed description “interrupt table register” in <b>Figure 2.1 and 2.1.6</b> to “interrupt vector table base register”                                                                                                                                                                |
|      |              |             | <b>Chapter 3. Memory</b>                                                                                                                                                                                                                                                                 |
|      |              | —           | • Made major text modifications to this chapter                                                                                                                                                                                                                                          |
|      |              |             | <b>Chapter 4. Special Function Registers</b>                                                                                                                                                                                                                                             |
|      |              | —           | • Changed expression “Start/Stop Condition” to “Start Condition/Stop Condition”                                                                                                                                                                                                          |
|      |              | 17          | • Changed hexadecimal format of reset values for registers CCR and FMCR in <b>Table 4.1</b> to binary                                                                                                                                                                                    |
|      |              | 18, 19      | • Changed expression “DMAi Interrupt” in <b>Tables 4.2 and 4.3</b> to “DMAi Transfer Complete Interrupt”                                                                                                                                                                                 |
|      |              | 24          | • Changed binary format of reset values for U3RB and U4RB in <b>Table 4.8</b> to hexadecimal                                                                                                                                                                                             |
|      |              | 26          | • Changed expression of register name “Xi Register Yi Register” and symbol “XiR, YiR” in <b>Table 4.10</b> to “Xi Register/Yi Register” and to “XiR/YiR”, respectively                                                                                                                   |
|      |              | 30          | • Deleted ADC0N4 in <b>Table 4.14</b>                                                                                                                                                                                                                                                    |
|      |              | 31          | • Changed reset value for PDi register in <b>Table 4.15</b> to binary                                                                                                                                                                                                                    |
|      |              | 33          | • Modified reset value for PLS in <b>Table 4.17</b> to “1XXX XX00b”                                                                                                                                                                                                                      |
|      |              | 35, 36      | • Modified register name “Port Pi_j Port Function Select Register” in <b>Table 4.19 and 4.20</b> to “Port Pi_j Function Select Register”                                                                                                                                                 |

|                         |                                 |
|-------------------------|---------------------------------|
| <b>REVISION HISTORY</b> | <b>R32C/161 Group Datasheet</b> |
|-------------------------|---------------------------------|

| Rev. | Date | Description                                  |                                                                                                                                                                                                                                                                                                                                                                  |
|------|------|----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |      | Page                                         | Summary                                                                                                                                                                                                                                                                                                                                                          |
|      |      | 38                                           | <ul style="list-style-type: none"> <li>Modified register names in <b>Table 4.22</b> “DMAi Source Select Register 1” to “DMAi Request Source Select Register” and “DMAi Source Select Register 2” to “DMAi Request Source Select Register 2”; Changed expression “Wake-up/Interrupt Priority Level Control Register” to “Wake-up IPL Setting Register”</li> </ul> |
|      |      | 39                                           | <ul style="list-style-type: none"> <li>Modified “X” in reset values for unassigned bits to “0” for the following registers in <b>Table 4.23</b>: LCW, LBRG, LMD0, LBRK, LSPC, LRFC, LSC, LTC, LST, and LEST</li> </ul>                                                                                                                                           |
|      |      | 55, 69                                       | <ul style="list-style-type: none"> <li>Modified reset value “00h” for C1CLKR in <b>Table 4.39</b> and C0CLKR in <b>Table 4.53</b> to “000X 0000b”; Added addresses “047F60h to 047FFFh” and “048000h to 04FFFFh”</li> </ul>                                                                                                                                      |
|      |      | <b>Chapter 5. Electrical Characteristics</b> |                                                                                                                                                                                                                                                                                                                                                                  |
|      |      | —                                            | <ul style="list-style-type: none"> <li>Added initially</li> </ul>                                                                                                                                                                                                                                                                                                |

All trademarks and registered trademarks are the property of their respective owners.

Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (<http://www.renesas.com>)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guarantees regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
  - (1) artificial life support devices or systems
  - (2) surgical implantations
  - (3) healthcare intervention (e.g., excision, administration of medication, etc.)
  - (4) any other purposes that pose a direct threat to human lifeRenesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.



**RENESAS SALES OFFICES**

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

**Renesas Technology America, Inc.**  
450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**  
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120  
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

**Renesas Technology Hong Kong Ltd.**  
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2377-3473

**Renesas Technology Taiwan Co., Ltd.**  
10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

**Renesas Technology Singapore Pte. Ltd.**  
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**  
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**  
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510