R8A66171DD/SP

A^{2}RT (ADVANCED ASYNCHRONOUS RECEIVER & TRANSMITTER)

REJ03F0269-0100
Rev. 1.00
Feb.19.2008

DESCRIPTION

The R8A66171 is an integrated circuit for asynchronous serial data communications. It is used in combination with an 8-bit microprocessor and is produced using the silicon gate CMOS technology. R8A66171 is the succession product of M66230.

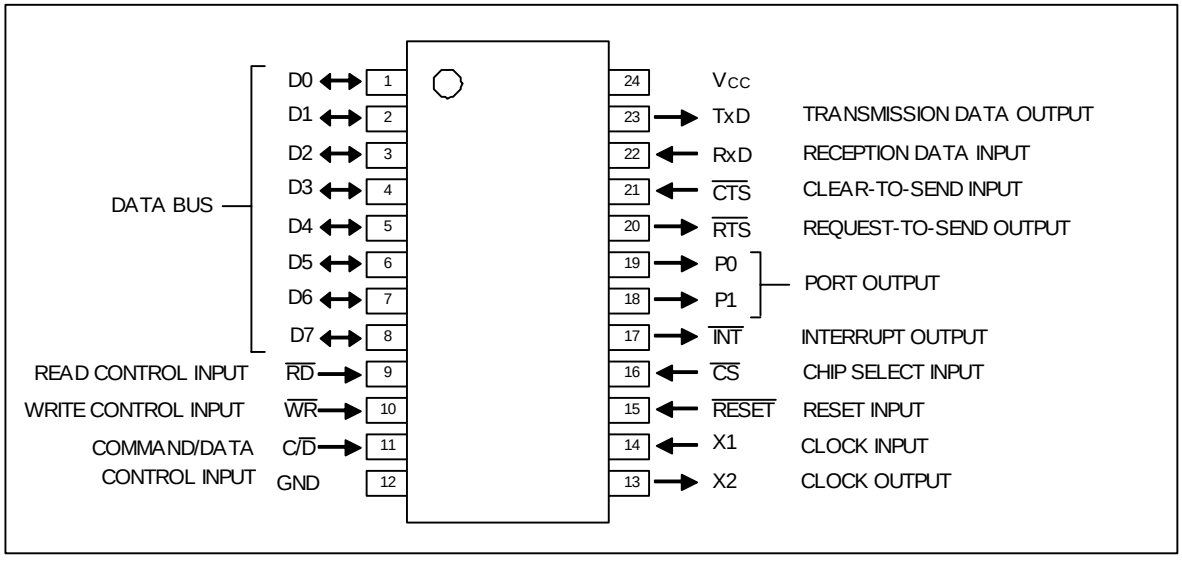
FEATURES

- Baud rate generator
- 4-byte FIFO data buffer for transmission and reception
- Error detection : CRC-CCITT
- Wakeup function
- Majority-voting system by sampling three points of received data
- Transmission / reception data format (number of bits)
  - Start bit 1
  - Data bit 8
  - Wakeup bit 1 or nil
  - Parity bit 1 or nil
  - Stop bit 1 or 2
- Transmission speed 500Kbps (max)
- Access time ta (/RD-D) : 100ns
- High output current I_{OH}=-24mA I_{OL}=24mA TxD, /RTS, P0, P1 pins
- Schmitt triggered input RxD, /CTS, /RESET pins
- Wide operating supply voltage range (Vcc=3.0~3.6V or Vcc=4.5~5.5V)
- Wide operating temperature range (Ta=-40~85^{o}C)

APPLICATION

Data communication control that uses microprocessor

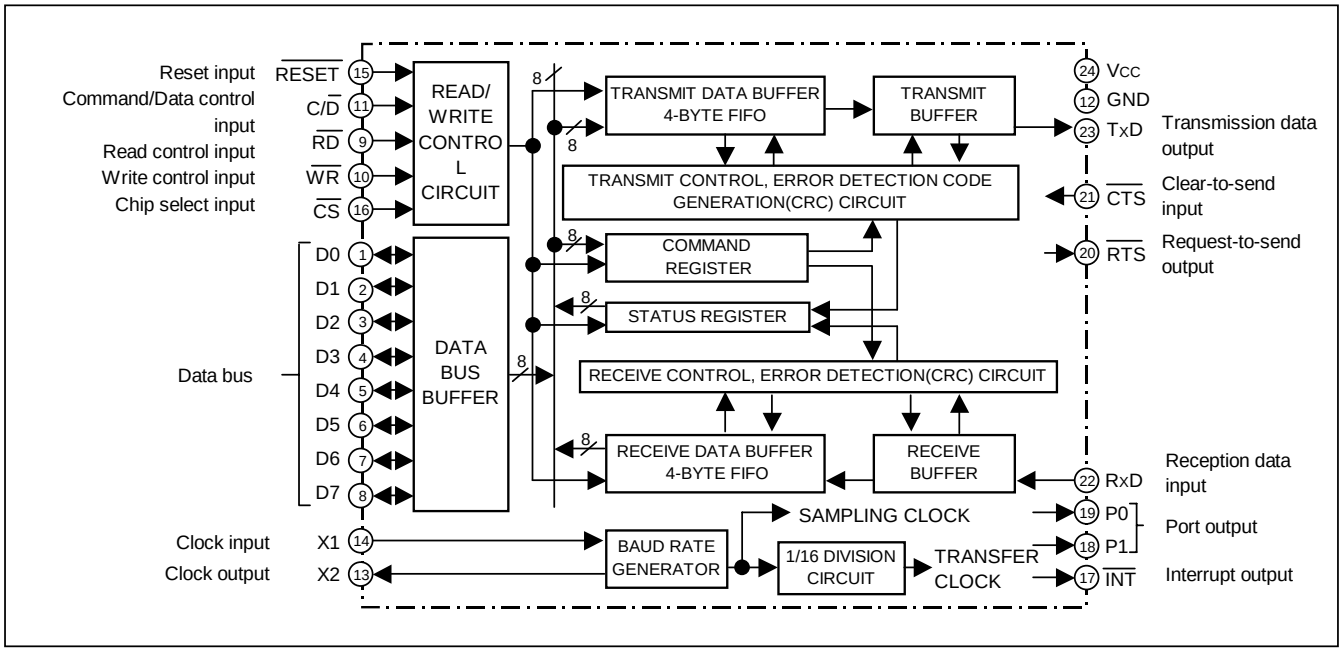
PIN CONFIGURATION (TOP VIEW)



FUNCTION

The R8A66171 is a UART (Universal Asynchronous Receiver/Transmitter) and is used in the peripheral circuit of a MCU. The R8A66171 receives parallel data, converts into serial format, and then transmits the serial data via the TxD pin. The device also receives data via the RxD pin from external circuits and converts it into parallel format, and sends the parallel data via the data bus.

BLOCK DIAGRAM



OPERATION

The R8A66171 is interfaced to a system bus and provides all functions needed for data communication.

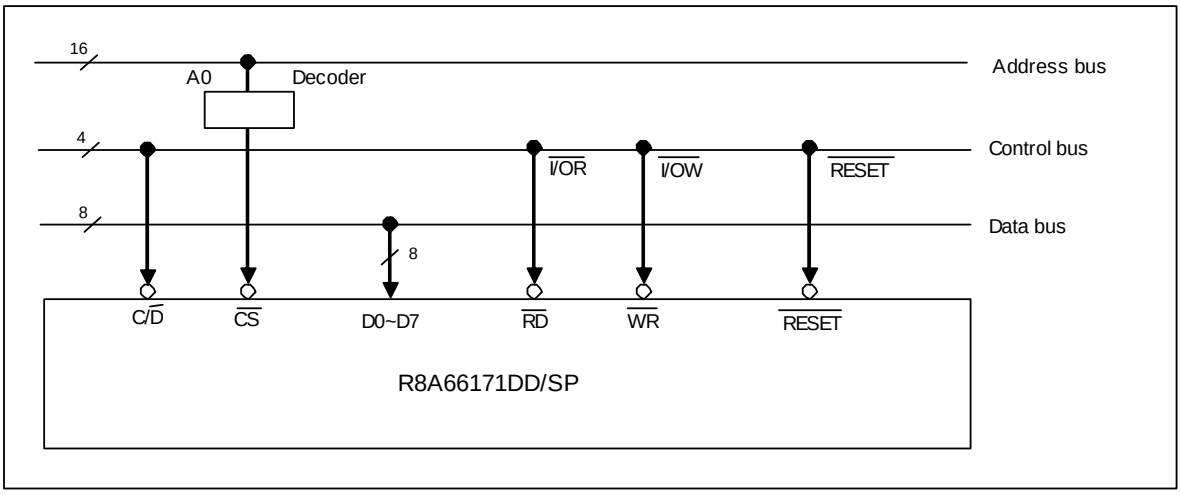


Fig.1 Interface between the R8A66171 and MCU system bus

When using the R8A66171, it is necessary to program the initial setting, baud rate, character length, CRC, parity, in accordance with the communication system. Once programmed, the communication system functions are executed continuously.
When initial setting of R8A66171 is completed, data communication becomes possible. When the transmitter is transmit-enabled (TXEN) by a command instruction and /CTS is low-level, data transfer starts up. If these conditions are not satisfied, data transmission is not executed. Reception is possible when the receiver is receive-enabled (RXEN) by a command instruction.
The MCU is able to read data when the interrupt output, /INT, goes low by packet end (PE) or buffer full (BF). While receiving data, the R8A66171 checks for errors and provides status information. It checks for four types of errors : CRC, parity, overrun and framing errors. When an error occurs, R8A66171 continues operation. The error status is maintained until the error reset, (ER) is modified by a command instruction.
The access method of the R8A66171 is shown Table 1.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	R8A66171 operation	MPU operation
L	L	H	L	Data bus ← Receiving data buffer(FIFO)	Read receive data
L	H	L	L	Data bus → Transmit data buffer(FIFO)	Write transmit data
H	L	H	L	Data bus ← Status register	Read the status
H	H	L	L	Data bus → Command register	Write the command
X	H	H	L	Data bus : High impedance	-
X	X	X	H	Data bus : High impedance	-

Note : X="L" or "H"

TABLE 1. Access method of the R8A66171

PIN DESCRIPTIONS

Pin	Name	I/O	Function
X1	Clock input	Input	A crystal is externally connected to these pins for generating an internal clock. An external clock signal can be input to X1 instead of a crystal. Then X2 output opened.
X2	Clock output	Output	
$\overline{\text{RESET}}$	Reset input	Input	This reset is a master reset, therefore commands should be loaded after the reset.
$\overline{\text{CS}}$	Chip select input	Input	A low level signal on the chip select input enables the R8A66171. The device can not be accessed when the signal is high-level.
C/$\overline{\text{D}}$	Command/Data control input	Input	This signal distinguishes whether the information on the R8A66171 data bus is data, command or status information. When the signal is high-level, the data bus has command or status information. When the signal is low-level, the data bus has data.
$\overline{\text{RD}}$	Read control input	Input	The receiving data or status information is output to the data bus from the R8A66171 by a low-level signal.
$\overline{\text{WR}}$	Write control input	Input	The data or command output from the MCU is written to the R8A66171 by a low-level signal.
D0~D7	Data bus	Input/ Output	This is an 8-bit bi-directional bus buffer. Command, status information, and transfer data are transferred to/from the MCU via this data bus buffer.
$\overline{\text{INT}}$	Interrupt output	Output	This is used as an interrupt request to MCU. The interrupt request is generated when the receive FIFO is full, the transmit FIFO is empty or the block reception is complete. D2 bit of command 6 controls the switching of low-level and high-level interrupt.
RxD	Reception data input	Input	The serial data is sent to this pin.
TxD	Transmission data output	Output	The serial data is transmitted from this pin.
P0	Port output	Output	This is an ordinary port pin. This pin is controlled by the D0 bit of command 6.
P1	Port output	Output	This pin has the same function as that of P0 pin and provides information of packet transmission's completion. The switching of this function is controlled by command 6, D1 bit.
$\overline{\text{CTS}}$	Clear-to-send input	Input	When the TXEN bit (D0) of command 4 is set to 1 and the /CTS input is low-level, serial data is sent from the TxD pin. This is used as the clear-to-send signal.
$\overline{\text{RTS}}$	Request-to-send output	Output	This is used as the request-to-send signal. This pin is controlled by the D3 bit of command 4.

DISCRIPTION OF FUNCTION

● Baud rate generator

The 8-bit programmable divider (baud rate generator) generates the baud rate for transmit or receive. The division rate is (n+1) with a range of n=0~255. The baud rate is calculated by the following formula:

$$\text{baud rate} = \frac{f(X1)}{\text{prescaler division (2 or 32)} \cdot \text{baud rate generator division rate (n+1)} \cdot 16}$$

The prescaler division rate is set by the D0 bit of command1. The baud rate generator division rate is set by command2.
Example as follows:

$$9600\text{bps} = \frac{9.8304\text{MHz}}{2 \cdot (31+1) \cdot 16}$$

● Block length counter

The R8A66171 can handle multiple-bytes of data as one block (packet).
Therefore, CRC of bytes is possible. The block length counter is a 6-bit programmable counter. The block length is (m+1) bytes with the allowed values of m=0~63.

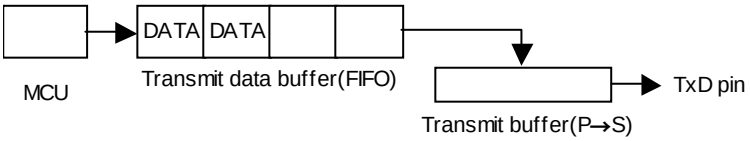
● Transmit data buffer (FIFO)

The transmit data buffer (FIFO) consists of 4-bytes.
The transmit data buffer (FIFO) functions according to the block length.

Block length=1~3

When the transmit data buffer (FIFO) becomes empty (buffer empty) and /INT is set to low-active, the interrupt output /INT is set to a low-level. The MCU verifies the buffer is empty when the D2 bit of the status1 information is read. The MCU should write the block length data to the transmit data buffer (FIFO) at this moment.
When a block of data is written to the transmit data buffer (FIFO), /CTS is low-level and TXEN is high-level, the data in the transmit data buffer (FIFO) is sent to the transmit buffer. If /CTS is high-level while data is transmitted, all data is transmitted (including the data in the transmit data buffer (FIFO)). When the buffer becomes empty, the data in the transmit data buffer (FIFO) is not be sent to the transmit buffer until MCU writes a new block of data to the transmit data buffer (FIFO). The MCU can not write new data to the transmit data buffer (FIFO) until the buffer becomes empty.

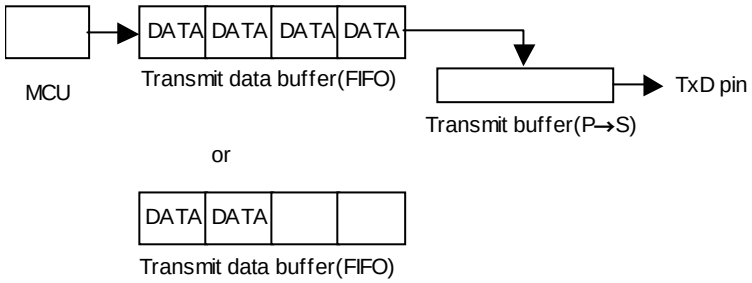
Example : Block length=2



Block length=4 or more

When the transmit data buffer (FIFO) becomes empty and /INT is set low-active, the interrupt output /INT becomes low. The MCU verifies the buffer is empty by reading the D2 bit of the status1 information.
When this happens, the MCU should write the 4-bytes of data to the transmit data buffer (FIFO). The data in the transmit data buffer (FIFO) is sent to the transmit buffer when /CTS is low-level and TXEN is high-level. When the number of bytes from the MCU becomes less than 4 at the last stage of the block transmission, the same operation should be made as the block length=1~3.
When the buffer becomes empty, the data in the transmit data buffer (FIFO) is not be sent to the transmit buffer until MCU writes data of the fixed block length to the transmit data buffer (FIFO). The MCU cannot write data to the transmit data buffer (FIFO) until the buffer becomes empty.

Example : Block length=6



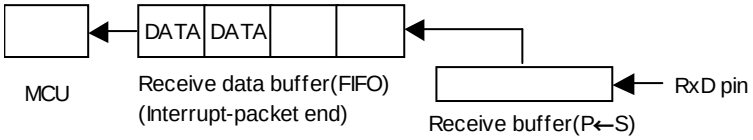
- Receive data buffer (FIFO)

  The receive data buffer (FIFO) consists of 4-bytes. The receive data buffer (FIFO) functions according to the block length.

  Block length=1~3

  When the data of the block length is received and /INT is set to low-level, the interrupt output /INT becomes low-level. The MCU acknowledges the packet end by setting the D0 bit of the status1 information.
  In this case, the MCU should read all data from the receive data buffer (FIFO).
  At the packet end, the data from the receive buffer cannot be transmitted to the receive data buffer (FIFO) until the MCU reads all data in the receive data buffer (FIFO). The MCU cannot read data in the receive data buffer until the packet end.

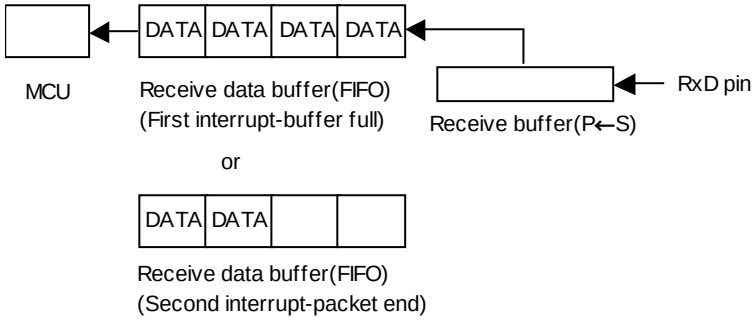
  Example : Block length=2



  Block length=4 or more

  When 4-byte data enters the receive data buffer (FIFO) (buffer full) and /INT is set to low-active, the interrupt output /INT becomes low-level. The MCU acknowledges the buffer full status by setting the D1 bit of the status1 information.
  In this case, the MCU should read all data in the receive data buffer (FIFO).
  When the last data enters the receive data buffer (FIFO), the packet end becomes the same operation as for 1~3 byte block length. If the block length is a multiple of four, the D0 and D1 bits of the status1 information are set when the last data enters the receive data buffer (FIFO). At packet end or buffer full, the new data cannot be transferred from the receive buffer to the receive data buffer (FIFO). The MCU cannot read data in the receive data buffer (FIFO) until packet end or buffer full occurs.

  Example : Block length=6



SUPPLEMENTARY DESCRIPTION

FIFO

The major purpose is not to interrupt the MCU by each character. The MCU is interrupted when:
Transmit data buffer (FIFO) empty
Receive data buffer (FIFO) full or packet end
The MCU interruption interval is as follows:
Approximately 90µs (min) until the FIFO becomes full at 500kbps.
Approximately 36.7ms (min) until the FIFO becomes full at 1.2kbps.
Read/write operation by the MCU should be made for all data in FIFO at once.

- Wakeup

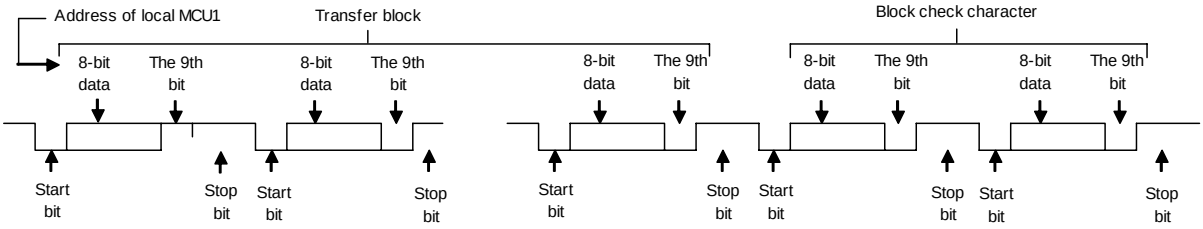
The wakeup mode of the R8A66171 can be set by setting the D2 bit of command4 to “1”. In wakeup mode, a 9th bit is automatically added (the wakeup bit).
Only the 9th bit of the first byte is “1”, and the remainder blocks 9th bits are set to “0”.
The wakeup is used when one master MCU and multiple local MCU are connected by serial I/O.
Examples of wakeup are shown below.

① Initial setting
The initial setting should be made by the input of each command.

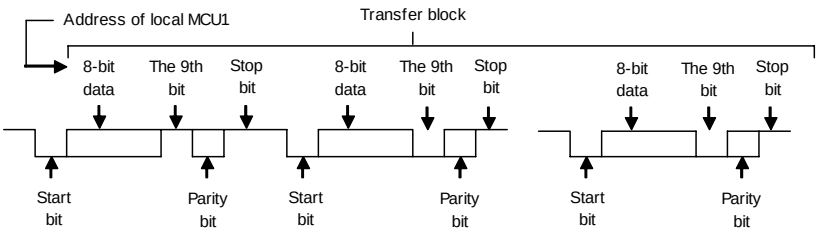
② Wakeup mode
The wakeup mode of the R8A66171 is activated by setting D2 bit of the command4 to “1”. Command5 can be input as the second byte of command4 by setting D2 bit of the command4 to “1” and each address is input. In the wakeup mode, the 9th bit is automatically added. Others remain the same.

③ Wakeup and data transfer (between master MCU and local MCU1)
Data is transmitted from the master MCU to each local MCU.
The first byte should hold the address of the local MCU. (in this case local MCU1.)
Each local R8A66171 checks the data (address) against command5 (each address) when the first byte (address) is received. The R8A66171 which matches the address starts to accept the following data (wakeup).
The R8A66171 which does not match the address, only accepts data, where the 9th bit is “1”.

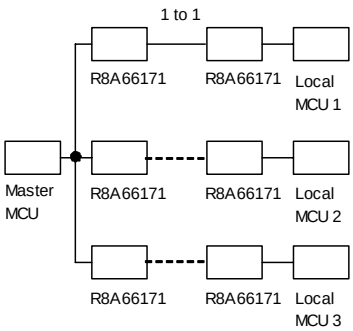
When CRC is enabled



When parity is enabled



Note : The wakeup function is automatically canceled when the transfer block data has been read by the MCU. (The wakeup mode continues.)



● Error detection

(1)Parity error
When a parity error occurs, D5 bit of status1 information is set. The data is send to the receive data buffer (FIFO).

(2)Framing error
When a framing error occurs, D3 bit of the status1 information is set. The data is sent to the receive data buffer (FIFO).

(3)Overrun error
When data is received before all data in the receive data buffer (FIFO) has been read by MCU, D4 bit of the status1 information is set as an overrun error.
In this case, the new data in the receive buffer are lost.

(4)CRC error
When an error occurs after receiving block check character, D6 bit of the status1 information is set.
The above error information is maintained until D4 bit of command4 is set.

● Error reset

When D4 bit of command4 is 1, D3 bit, D4 bit, D5 bit and D6 bit of status1 are reset.
When an error reset pulse occurs, D4 bit of command4 becomes 0.
Again, D4 bit of command4 need not be adjusted to 0.

● Internal reset

When D5 bit of command4 becomes 1, all command status information is reset, and the signal based on reset command status information is output to each output.
When an internal reset pulse occurs, D5 bit of command4 becomes 0.
Again, D5 bit of command4 need not be adjusted to 0.

SUPPLEMENTARY DESCRIPTION

Comparison between parity check and CRC

● Parity check

Parity check needs only one additional bit and is highly efficient. The formula is straightforward, and includes even parity and odd parity checks. In both cases, one bit is added.

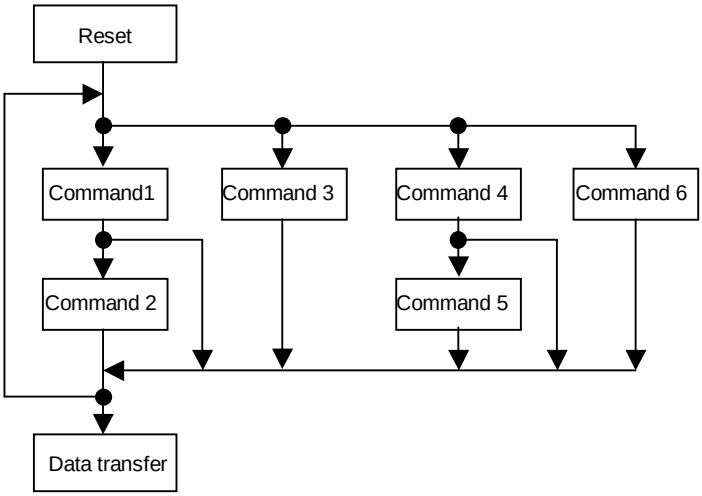
● CRC

The CRC poly-nominal expression is CRC-CCITT $X^{16}+X^{12}+X^5+1$.
CRC deals with data characters in transmitted or received blocks. (Start, stop and wakeup bits are excluded.)
When the CRC is enabled, the transmit and receive data consists of block length (1~64 bytes) + 2 bytes (block check characters). The following table shows the comparison between parity check and CRC.

Parity check	Burst error is not detected. (50% of which can be detected.)
CRC	Burst error can be detected. (Burst error detection rate is more than 99.9%.)

PROGRAMMING

The command must be loaded first to the R8A66171 by the MCU before data communication. R8A66171 has 6 command registers.
Data transfer is possible when commands have been loaded to these command registers after reset.
The flowchart of the initial setting is shown in the following diagram.

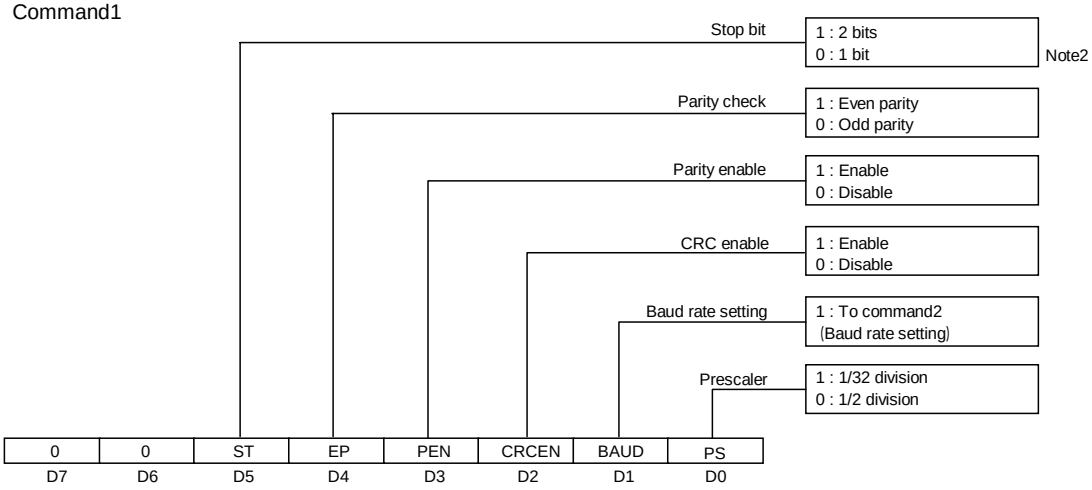


Flowchart of the R8A66171 initial setting

COMMAND-INSTRUCTION FORMAT

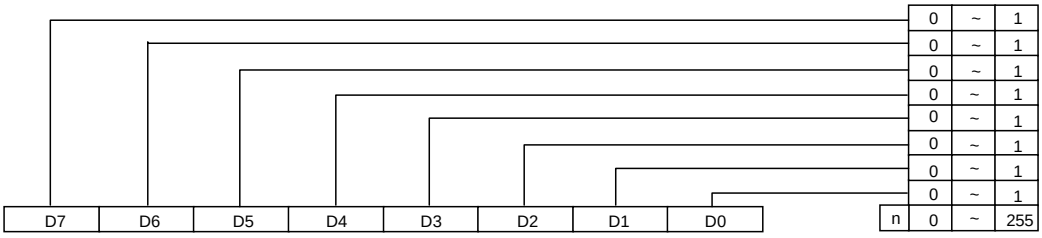
The commands are decoded by D7 and D6.

Command1

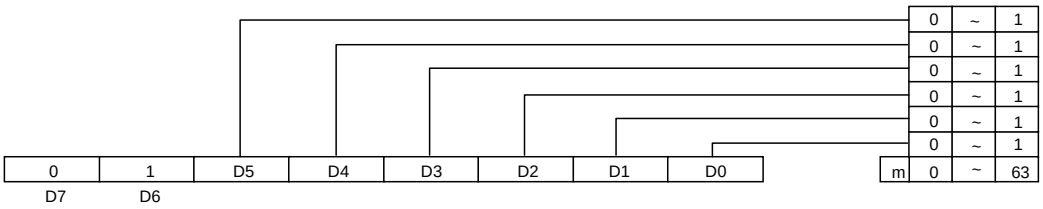


Note 1 : Priority is given to parity enable, if parity enable and CRC enable are both "1" (D3, D2=1).
Note 2 : TxD output wave is Stop bit (D5) setup value +1 (always).

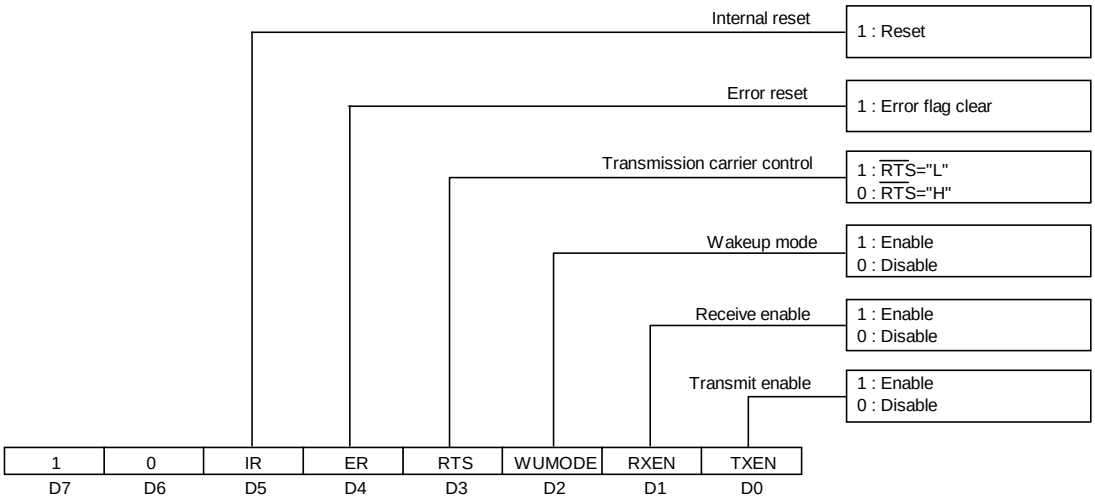
Command2 (Baud rate setting. The second byte when D1 bit of the command1 is set to "1".)



Command3 (Block length setting)



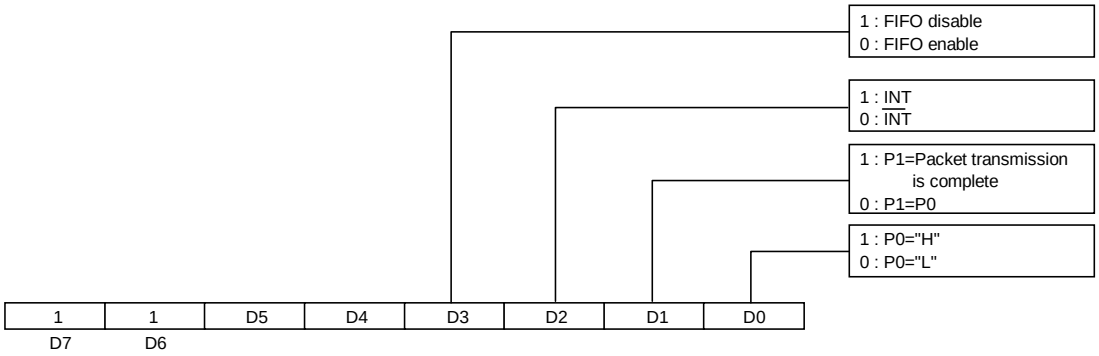
Command4



Command5 (Address setting. The second byte when D2 bit of the command4 is set to “1”.)

D7	D6	D5	D4	D3	D2	D1	D0

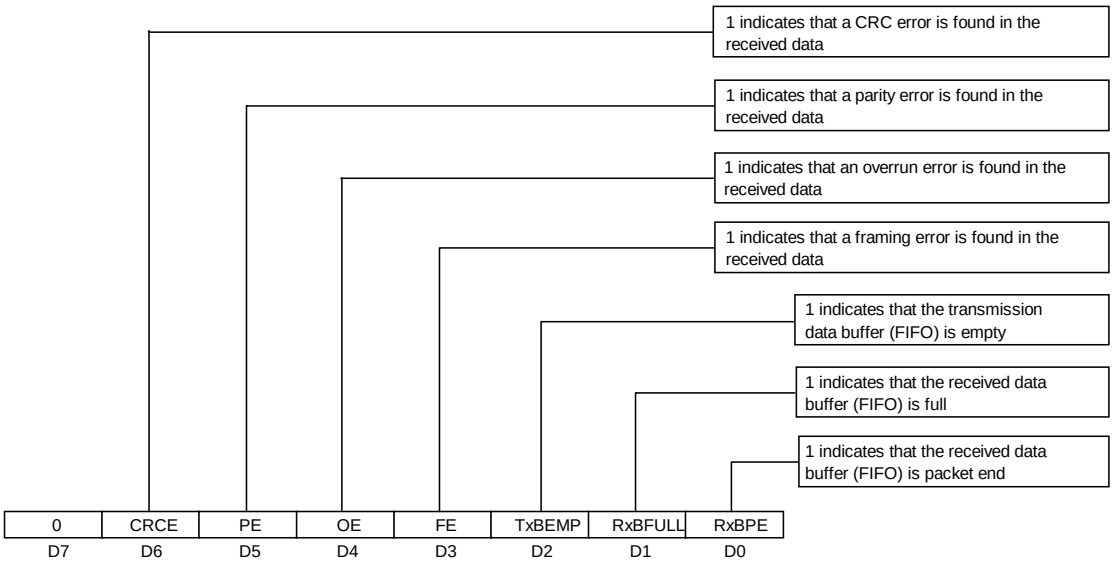
Command6



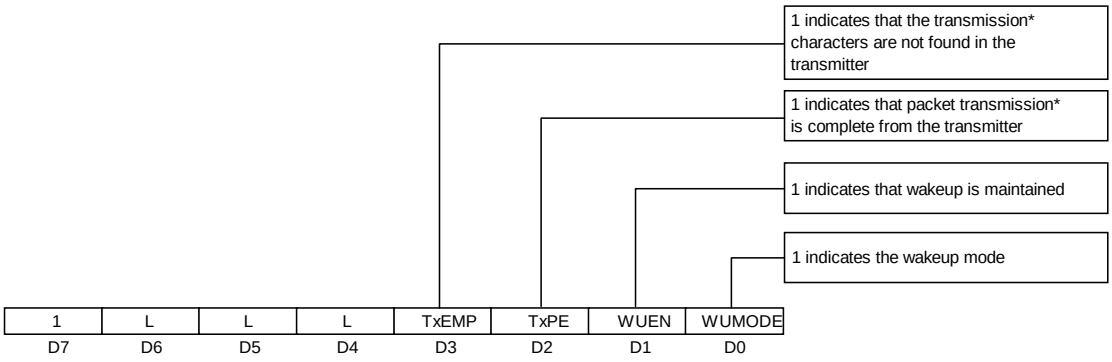
STATUS INFORMATION

- Status 1 and 2 cannot address setting from external pin. Discrimination of status used to D7 bit.
- Status 1 and 2 has read mutually. (There are not continuity read of same status.)

Status1



Status2



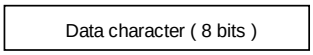
* Transmitter = Transmit data buffer (FIFO) + Transmit buffer

TRANSMISSION FORMAT

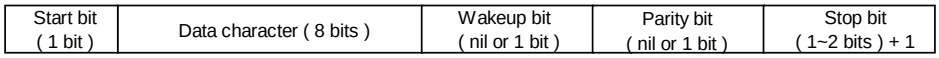
Transmit format

Parity enabled

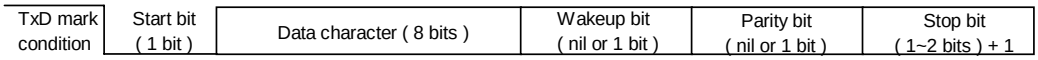
MCU→R8A66171



Assembled data format

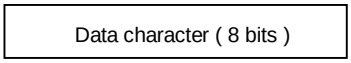


Transmitter output

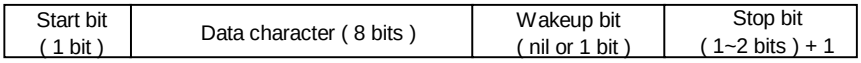


CRC enabled

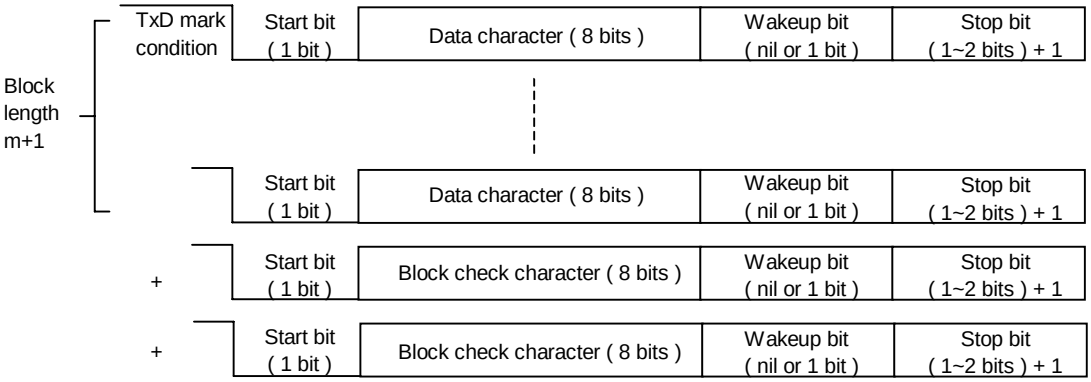
MCU→R8A66171



After assembly



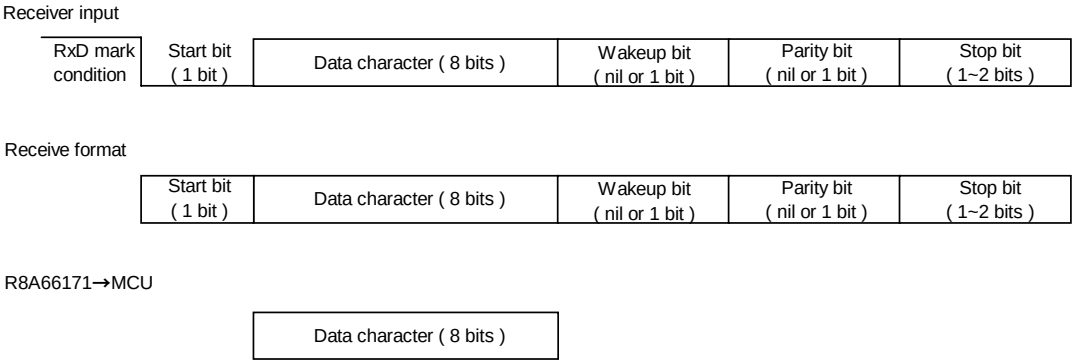
Transmitter output



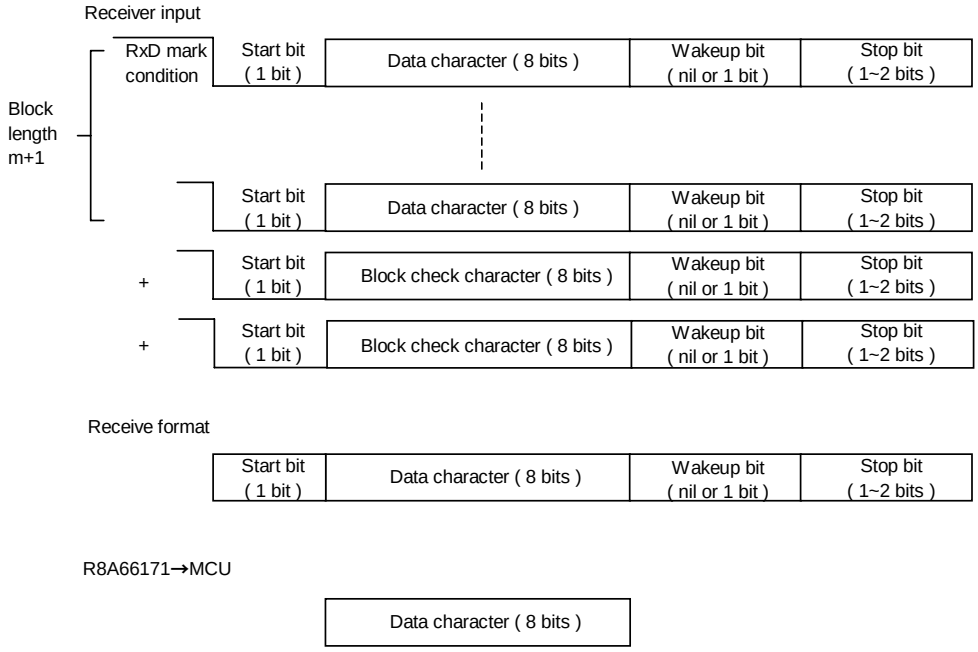
TRANSMISSION FORMAT

Receive format

Parity enabled



CRC enabled



ABSOLUTE MAXIMUM RATINGS (Ta=-40~85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	Value using the GND pin as reference	-0.5~+7.0	V
VI	Input voltage		-0.5~Vcc+0.5	V
VO	Output voltage		-0.5~Vcc+0.5	V
Pd	Power dissipation	Actually mounted	500	mW
Tstg	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-40~85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
Vcc	Supply voltage	5.0V	4.5	5.0	5.5	V
		3.3V	3.0	3.3	3.6	V
GND	Ground			0		V
Topr	Operating temperature		-40		85	°C

ELECTRICAL CHARACTERISTICS

5.0V version support specifications (Ta=-40~85°C,Vcc=3.0~3.6V,GND=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
VIH	High-level input voltage	/RD, /WR, C//D, /CS, D0~D7	0.75×Vcc			V
VIL	Low-level input voltage				0.25×Vcc	V
VIH	High-level input voltage	X1	0.8×Vcc			V
VIL	Low-level input voltage				0.2×Vcc	V
VT+	Positive threshold voltgage	RxD, /CTS, /RESET	0.35×Vcc		0.8×Vcc	V
VT-	Negative threshold voltage		0.2×Vcc		0.65×Vcc	V
VH	Hysteresis width		0.4			V
VOH	High-level output voltage	IOH=-8mA /INT, D0~D7	Vcc-0.8			V
		IOH=-24mA TxD, /RTS, P0, P1				
VOL	Low-level output voltage	IOL=8mA /INT, D0~D7			0.55	V
		IOL=24mA TxD, /RTS, P0, P1				
IIH	High-level input current	VI=Vcc			1.0	µA
IIL	Low-level input current	VI=GND			-1.0	µA
IOZH	Off-state high-level output current	VO=Vcc			5.0	µA
IOZL	Off-state low-level output current	VO=GND			-5.0	µA
ICC	Static supply current	VI=Vcc, GND			40	mA

3.3V version support specifications (Ta=-40~85°C,Vcc=3.0~3.6V,GND=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
VIH	High-level input voltage	/RD, /WR, C//D, /CS, D0~D7	0.75×Vcc			V
VIL	Low-level input voltage				0.25×Vcc	V
VIH	High-level input voltage	X1	0.8×Vcc			V
VIL	Low-level input voltage				0.2×Vcc	V
VT+	Positive threshold voltgage	RxD, /CTS, /RESET	0.35×Vcc		0.8×Vcc	V
VT-	Negative threshold voltage		0.2×Vcc		0.65×Vcc	V
VH	Hysteresis width		0.4			V
VOH	High-level output voltage	IOH=-4mA /INT, D0~D7	Vcc-0.6			V
		IOH=-12mA TxD, /RTS, P0, P1				
VOL	Low-level output voltage	IOL=4mA /INT, D0~D7			0.4	V
		IOL=12mA TxD, /RTS, P0, P1				
IIH	High-level input current	VI=Vcc			1.0	µA
IIL	Low-level input current	VI=GND			-1.0	µA
IOZH	Off-state high-level output current	VO=Vcc			5.0	µA
IOZL	Off-state low-level output current	VO=GND			-5.0	µA
ICC	Static supply current	VI=Vcc, GND			25	mA

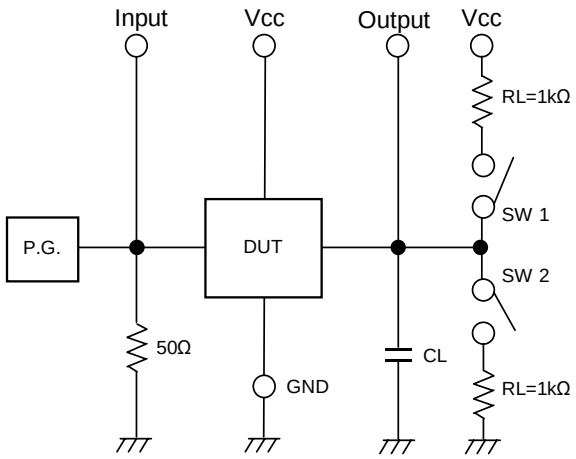
TIMING REQUIREMENTS (Ta=-40~85°C,Vcc=4.5~5.5V or Vcc=3.0~3.6V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits for 5.0V			Limits for 3.3V			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{C1}(X1)	Clock frequency	(Except Wakeup, CRC mode)		62.5			66.6			ns
t_{WH1}(X1)	Clock high-level pulse width			30			32			ns
t_{WL1}(X1)	Clock low-level pulse width			30			32			ns
t_{C2}(X1)	Clock frequency	(Wakeup, CRC mode)		80			90			ns
t_{WH2}(X1)	Clock high-level pulse width			38			42			ns
t_{WL2}(X1)	Clock low-level pulse width			38			42			ns
tr(X1)	Clock rise time					20			25	ns
tf(X1)	Clock fall time					20			25	ns
tsu(A-/R)	Address setup time before read (/CS, C//D)			0			0			ns
th(/R-A)	Address hold time after read (/CS, C//D)			0			0			ns
tw(/R)	Read pulse width			100			110			ns
tsu(A-/W)	Address setup time before write (/CS, C//D)			0			0			ns
th(/W-A)	Address hold time after write (/CS, C//D)			0			0			ns
tw(/W)	Write pulse width			100			110			ns
tsu(DQ-/W)	Data setup time before write			50			55			ns
th(/W-DQ)	Data hold time after write			5			6			ns
trec(/RESET)	Recovery time between write			100			110			ns
tw(/RESET)	Reset pulse width			100			110			ns

SWITCHING CHARACTERISTICS (Ta=-40~85°C,Vcc=4.5~5.5V or Vcc=3.0~3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits for 5.0V			Limits for 3.3V			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{PZH}(/R-DQ)	Data output enable time after read				100			110	ns
t_{PZL}(/R-DQ)					100			110	ns
t_{PHZ}(/R-DQ)	Data output disable time after read				85			95	ns
t_{PLZ}(/R-DQ)					85			95	ns
t_{PLH}(/R-/INT)	/INT output propagation time after read data				170			185	ns
t_{PHL}(/R-/INT)					170			185	ns
t_{PLH}(/W-/INT)	/INT output propagation time after write data				150			165	ns
t_{PHL}(/W-/INT)					150			165	ns
t_{PLH}(/W-/INT)	/INT output propagation time after write command (command 4)				100			110	ns
t_{PHL}(/W-/INT)					100			110	ns
t_{PLH}(/W-/INT)	/INT output propagation time after write command (command 6)				100			110	ns
t_{PHL}(/W-/INT)					100			110	ns
t_{PLH}(/W-P0)	P0 output propagation time after write command				70			75	ns
t_{PHL}(/W-P0)					70			75	ns
t_{PLH}(/W-P1)	P1 output propagation time after write command				70			75	ns
t_{PHL}(/W-P1)					70			75	ns
t_{PLH}(/W-/RTS)	/RTS output propagation time after write command				70			75	ns
t_{PHL}(/W-/RTS)					70			75	ns

TEST CIRCUIT



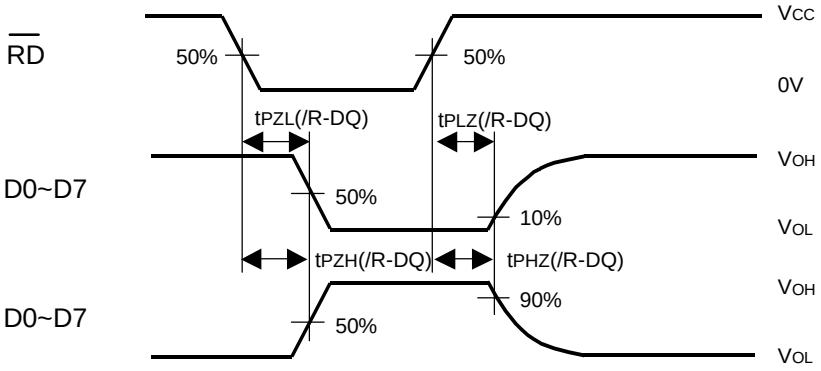
Parameter	SW 1	SW 2
tPLH, tPHL	Open	Open
tPLZ	Closed	Open
tPHZ	Open	Closed
tPZL	Closed	Open
tPZH	Open	Closed

(1) The pulse generator (PG) has the following characteristics (10%~90%) tr=3ns, tf=3ns

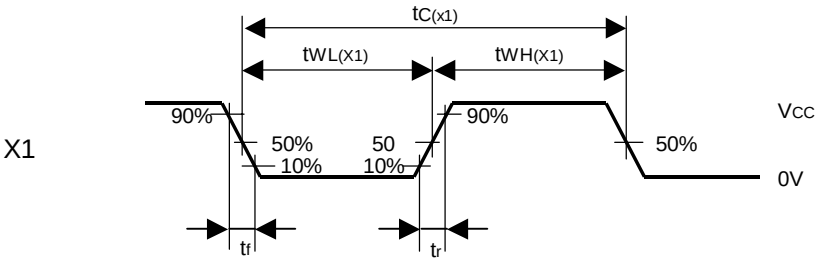
(2) The capacitance CL=150pF includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM

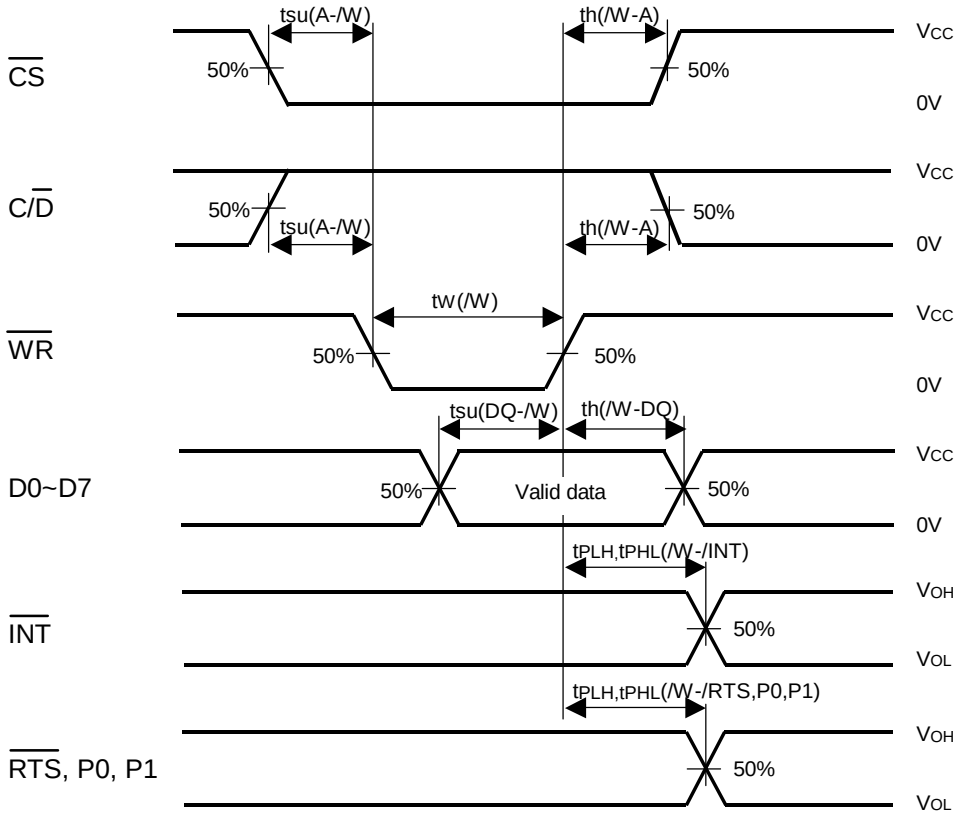
Input/output waveform at read data and read status



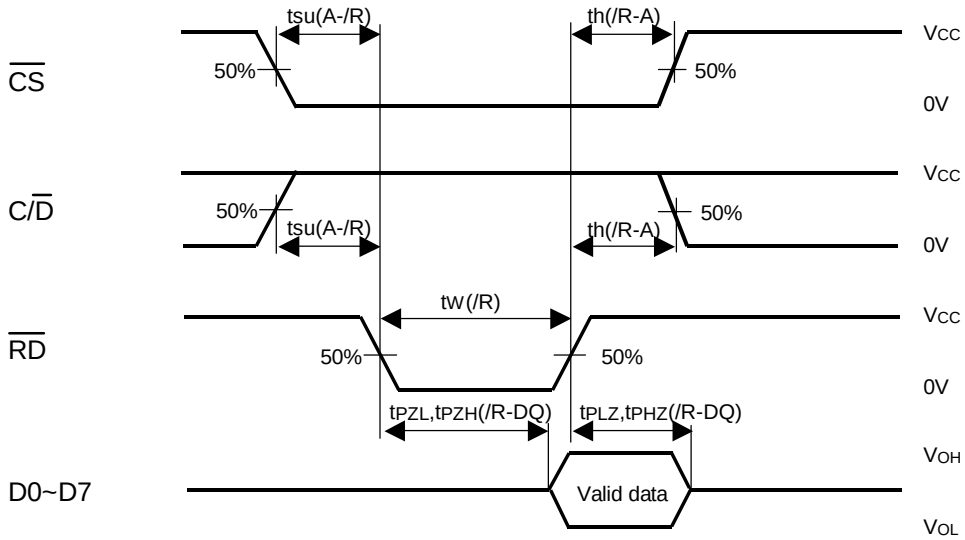
Clock Timing



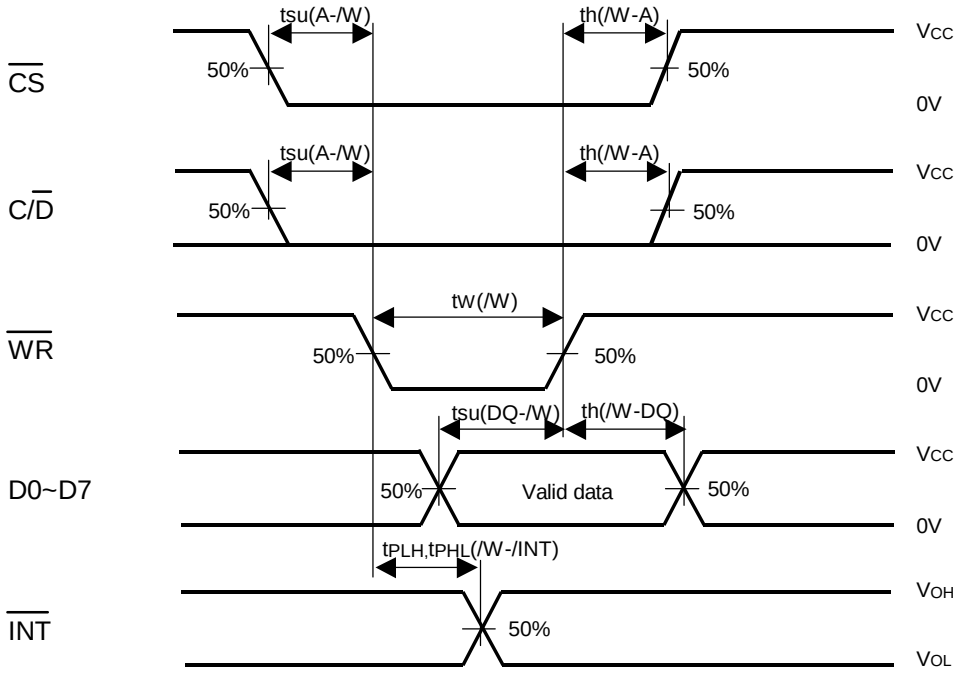
Write control cycle (MCU→R8A66171)



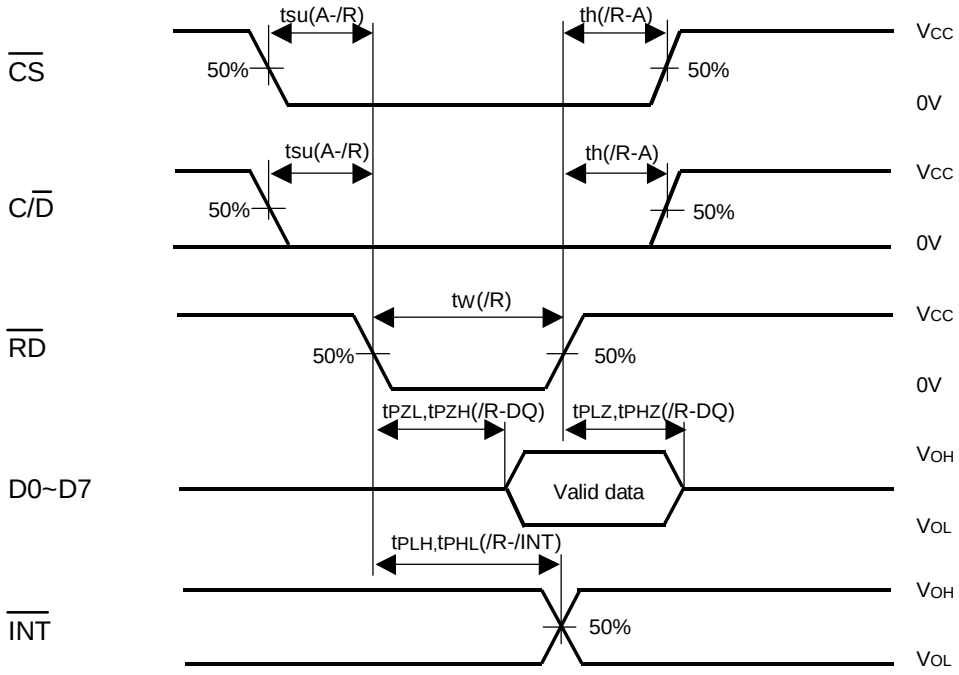
Read control cycle (R8A66171→MCU)



Write data cycle (MCU→R8A66171)

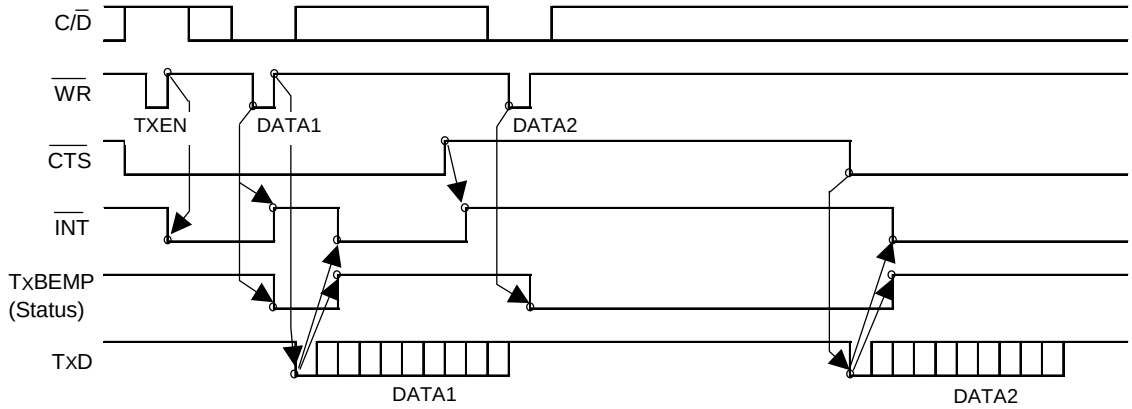


Read data cycle (R8A66171→MCU)

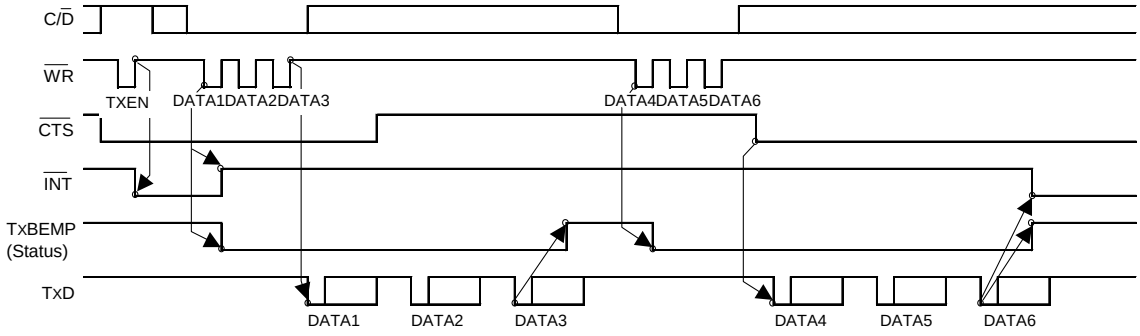


Transmitter control and flag timing

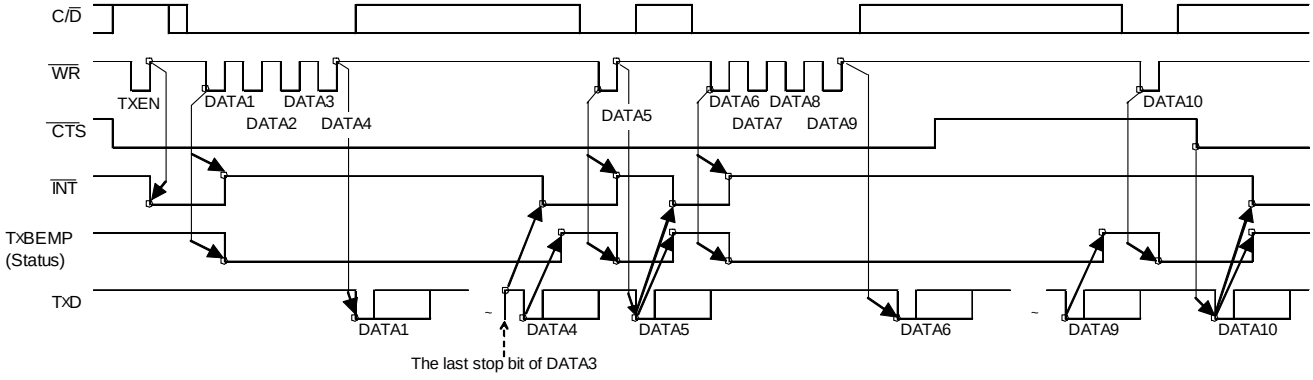
(1) Block length=1



(2) Block length=3

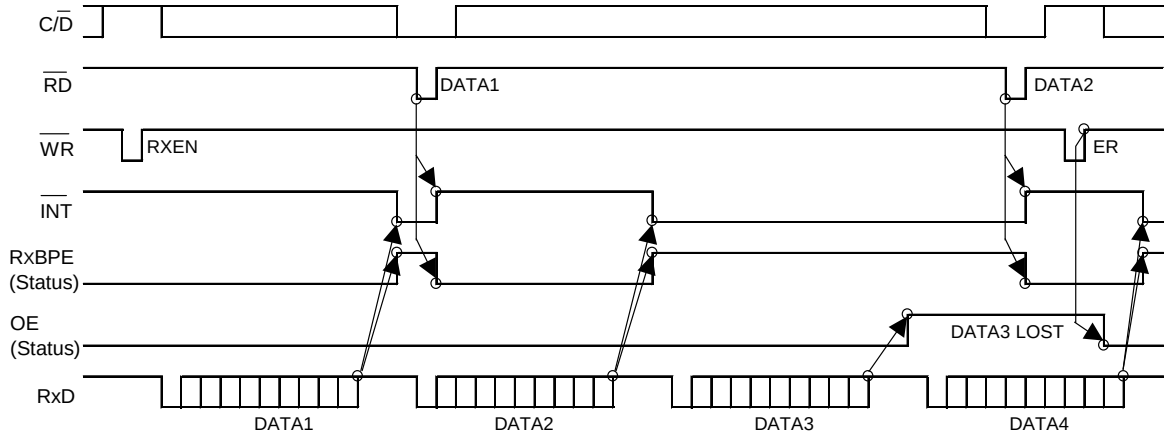


(3) Block length=5

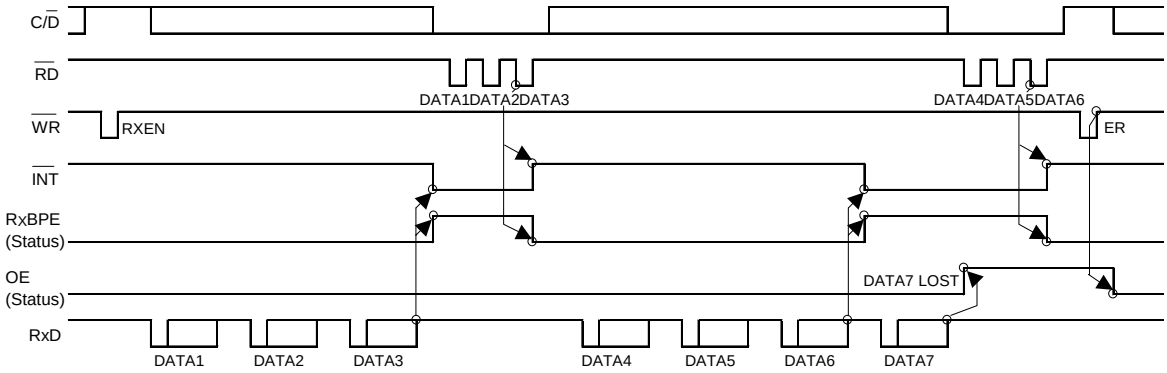


Receiver control and flag timing

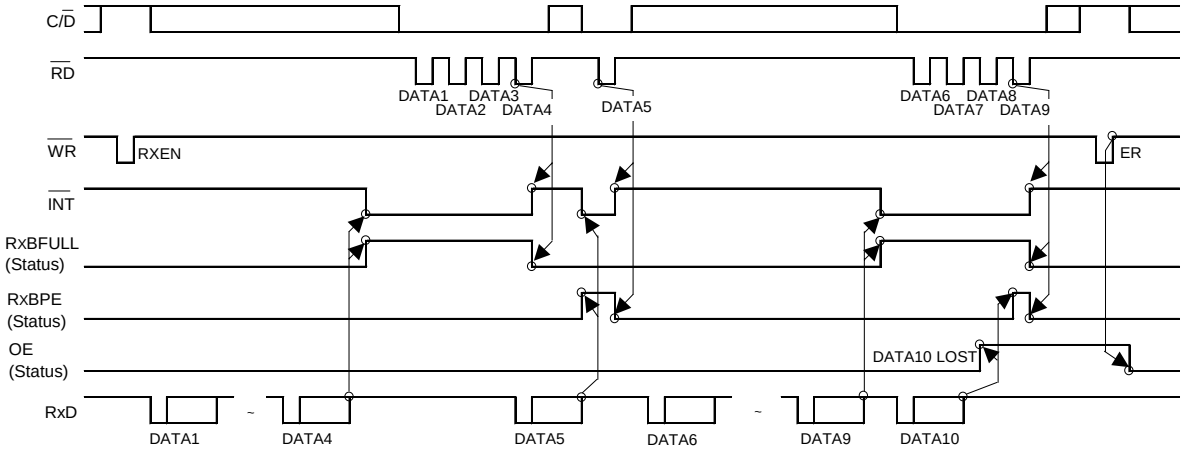
(1) Block length=1



(2) Block length=3

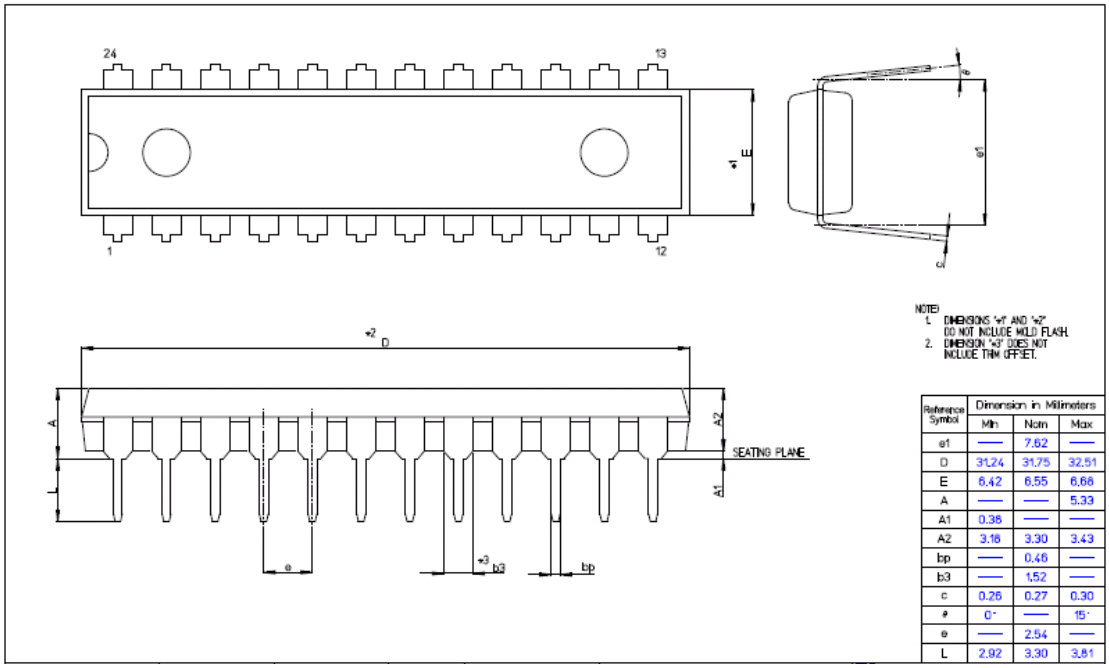


(3)Block length=5

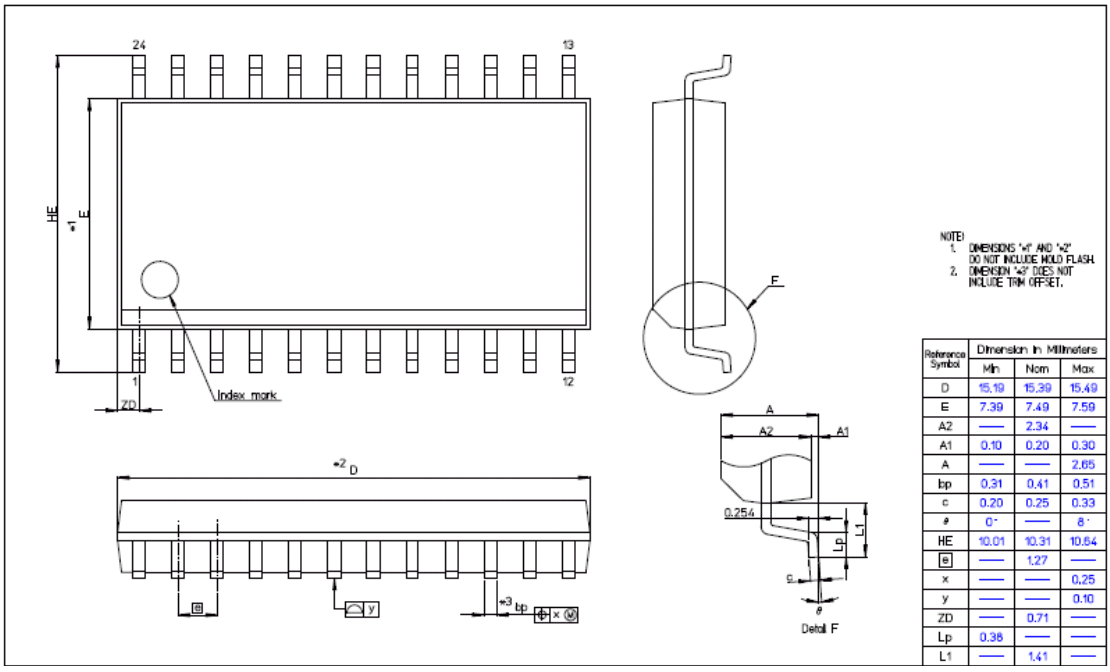


PACKAGE OUTLINE

Product Name	Package	RENESAS Code	Previous Code
R8A66171DD	24pin DIP	PRDP0024AF-A	24P4X-A
R8A66171SP	24pin SOP	PRSP0024DF-A	24P2X-B



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e1	—	7.62	—
D	31.24	31.75	32.51
E	6.42	6.55	6.68
A	—	—	5.33
A1	0.38	—	—
A2	3.18	3.30	3.43
bp	—	0.46	—
b3	—	1.52	—
c	0.26	0.27	0.30
θ	0°	—	15°
e	—	2.54	—
L	2.92	3.30	3.81



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.19	15.39	15.49
E	7.39	7.49	7.59
A2	—	2.34	—
A1	0.10	0.20	0.30
A	—	—	2.65
bp	0.31	0.41	0.51
c	0.20	0.25	0.33
θ	0°	—	8°
HE	10.01	10.31	10.64
e	—	1.27	—
x	—	—	0.25
y	—	—	0.10
ZD	—	0.71	—
Lp	0.38	—	—
L1	—	1.41	—

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