



GS1528B HD-LINX® II Multi-Rate Dual Slew-Rate Cable Driver

Features

- SMPTE 292M, SMPTE 344M and SMPTE 259M compliant
- Dual coaxial cable driving outputs with selectable slew rate
- 50Ω differential PECL input
- Pb-free and RoHS compliant
- Seamless interface to other HD-LINX II family products
- Single 3.3V power supply operation
- Operating temperature range: 0°C to 70°C

Applications

- SMPTE 292M, SMPTE 344M and SMPTE 259M Coaxial Cable Serial Digital Interfaces

Description

The GS1528B is a second generation high-speed BiCMOS integrated circuit designed to drive one or two 75Ω co-axial cables.

The GS1528B may drive data rates up to 1.485Gb/s and provides two selectable slew rates in order to achieve compliance to SMPTE 259M, SMPTE 344M and SMPTE 292M.

The GS1528B accepts a LVPECL level differential input that may be AC coupled. External biasing resistors at the inputs are not required.

Power consumption is typically 168mW using a 3.3V power supply.

The GS1528B is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.

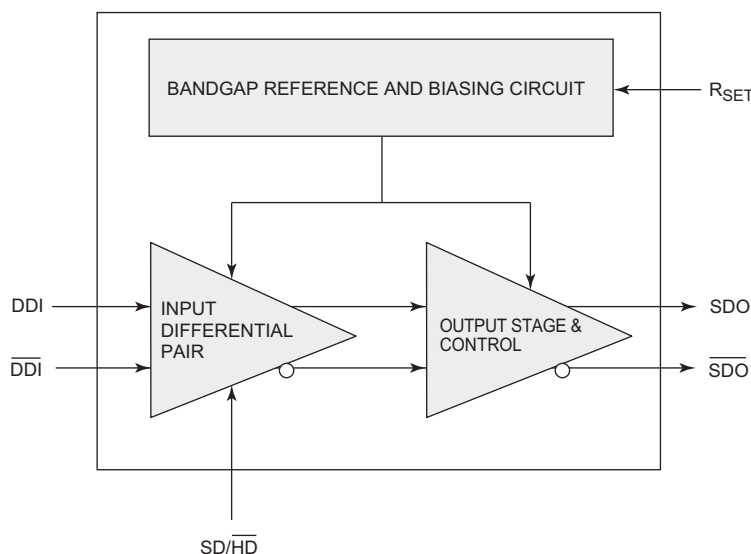


Figure A: GS1528B Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
4	154633	–	August 2010	Correction to 7.1 Package Dimensions. Added 250pc tape & reel part number to 7.4 Ordering Information.
3	153754	–	November 2009	Updated to latest Gennum template.
2	142319	–	April 2007	Converting to Data Sheet. Added section 7.3 Marking Diagram. Added typical ORL value in Table 2-3: AC Electrical Characteristics.
1	141659	–	August 2006	Removed power consumption and supply current data for SDO/ $\overline{\text{SDO}}$ disabled in Table 2-2: DC Electrical Characteristics.
0	140615	–	May 2006	New document.

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1. Pin Out

1.1 GS1528B Pin Assignment

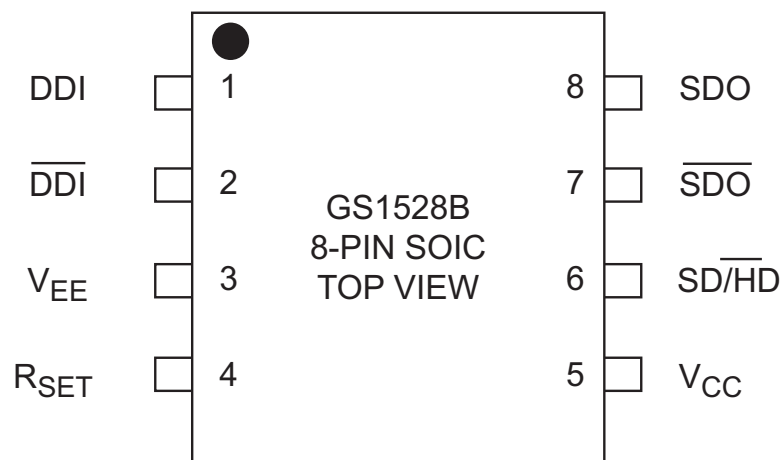


Figure 1-1: 8-Pin SOIC

1.2 GS1528B Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1,2	DDI, $\overline{\text{DDI}}$	Analog	Input	Serial digital differential input.
3	V_{EE}	–	Power	Most negative power supply connection. Connect to GND.
4	R_{SET}	Analog	Input	External output amplitude control resistor.
5	V_{CC}	–	Power	Most positive power supply connection. Connect to +3.3V.
6	SD/HD	Non Synchronous	Input	Output slew rate control. When set HIGH, the output will meet SMPTE 259M rise/fall time specifications. When set LOW, the serial outputs will meet SMPTE 292M rise/fall time specifications.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1 lists the absolute maximum ratings for the GS1528B. Conditions exceeding the limits listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to 3.6 V _{DC}
Input ESD Voltage	4kV
Storage Temperature Range	-50°C < T _s < 125°C
Input Voltage Range (any input)	-0.3 to (V _{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Solder Reflow Temperature	260°C
Power Dissipation	300mW

2.2 DC Electrical Characteristics

Table 2-2 shows the DC electrical characteristics of the GS1528B where conditions are V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, unless otherwise shown.

Table 2-2: DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V _{CC}	–	3.135	3.3	3.465	V
Power Consumption	P _D	T _A = 25°C	–	168	–	mW
Supply Current	I _s	T _A = 25°C	–	51	64	mA
Output Voltage	V _{CMOUT}	Common mode	–	V _{CC} - V _{OUT}	–	V
Input Voltage	V _{CMIN}	Common mode	1.4 + ΔV _{DDI} /2	–	V _{CC} - ΔV _{DDI} /2	V
SD/HD Input	V _{IH}	I _{IH} ≤ 10uA	2.0	–	–	V
	V _{IL}	I _{IL} ≤ 10uA	–	–	0.8	V

2.3 AC Electrical Characteristics

Table 2-3 shows the AC electrical characteristics of the GS1528B where conditions are $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$, unless otherwise shown.

Table 2-3: AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	–	–	1.485	Gb/s	1
Additive jitter	–	1.485Gb/s	–	20	–	ps _{p-p}	–
	–	270Mb/s	–	16	–	ps _{p-p}	–
Rise/Fall time	t_r, t_f	$SD/\overline{HD}=0$	–	–	220	ps	2
	t_r, t_f	$SD/\overline{HD}=1$	400	–	800	ps	2
Mismatch in rise/fall time	$\Delta t_r, \Delta t_f$	–	–	–	30	ps	–
Duty cycle distortion	–	$SD/\overline{HD}=0$	–	–	30	ps	3
	–	$SD/\overline{HD}=1$	–	–	100	ps	3
Overshoot	–	$SD/\overline{HD}=0$	–	–	10	%	3
	–	$SD/\overline{HD}=1$	–	–	8	%	3
Output Return Loss	ORL	–	15	20	–	dB	4
Output Voltage Swing	V_{OUT}	$R_{SET} = 750\Omega$	750	800	850	mV _{p-p}	3
Input Voltage Swing	ΔV_{DDI}	Differential	300	–	2200	mV _{p-p}	–

NOTES:

1. The input coupling capacitor must be set accordingly for lower data rates.
2. Rise/Fall time measured between 20% and 80%.
3. Single Ended into 75Ω external load.
4. ORL depends on board design. The GS1528B achieves this specification on Gennum's evaluation boards.

3. Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 3-1. The recommended standard Pb reflow profile is shown in Figure 3-2.

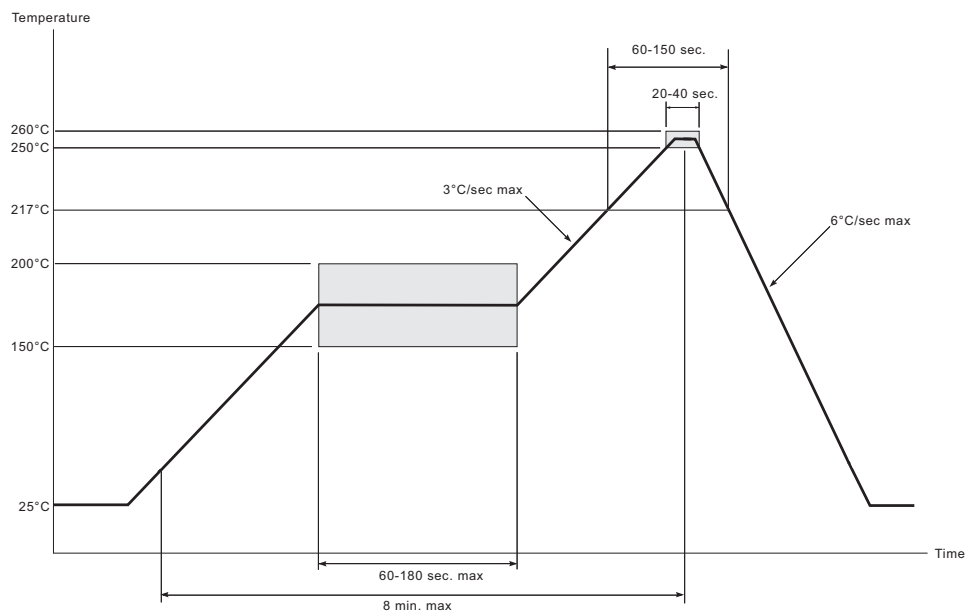


Figure 3-1: Maximum Pb-free Solder Reflow Profile (Preferred)

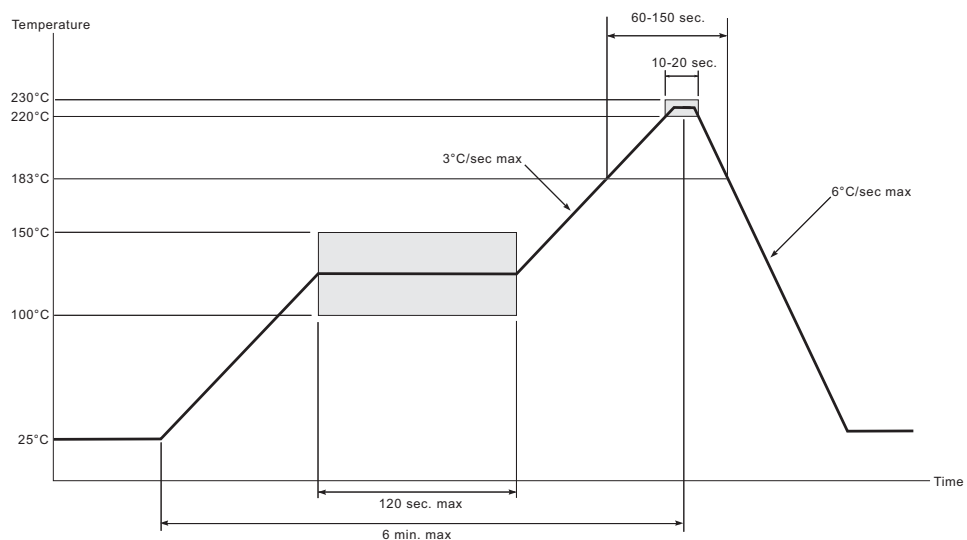


Figure 3-2: Standard Pb Reflow Profile

4. Input / Output Circuits

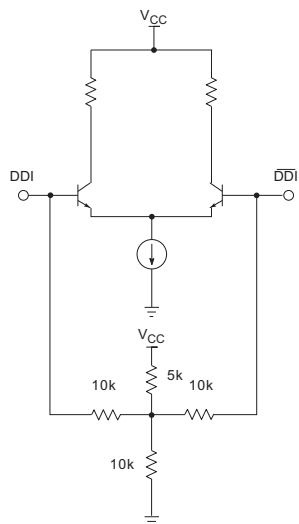


Figure 4-1: Differential Input Stage (DDI/DDI)

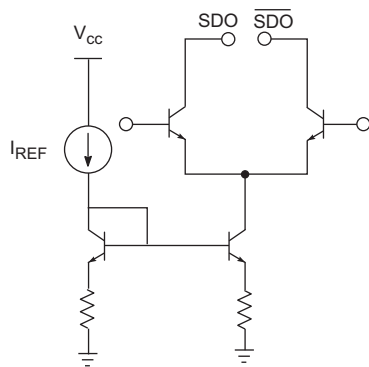


Figure 4-2: Differential Output Stage (SDO/SDO) I_{REF} Derived Using R_{SET}

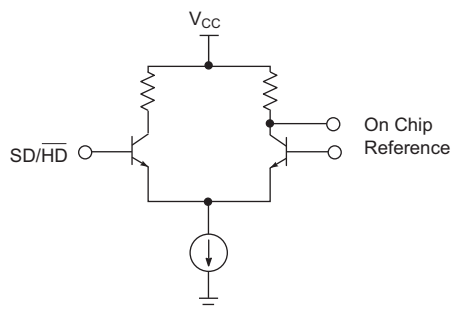


Figure 4-3: Slew Rate Select Input Stage

5. Detailed Description

5.1 Input Interfacing

DDI/ $\overline{\text{DDI}}$ are high impedance differential inputs. The equivalent input circuit is shown in [Figure 4-1](#).

Several conditions must be observed when interfacing to these inputs:

- The differential input signal amplitude must be between 300 and 2200mVpp.
- The common mode voltage range must be as specified in the [Table 2.2](#).
- For input trace lengths longer than approximately 1cm, the inputs should be terminated as shown in the Typical Application Circuit.

The GS1528B inputs are self-biased, allowing for simple AC coupling to the device. For serial digital video, a minimum capacitor value of 4.7 μ F should be used to allow coupling of pathological test signals. A tantalum capacitor is recommended.

SD/ $\overline{\text{HD}}$ Input Pin

The GS1528B SDO rise and fall times can be set to comply with both SMPTE 259M/344M and SMPTE 292M. For all SMPTE 259M standards, or any data rate that requires longer rise and fall time characteristics, the SD/ $\overline{\text{HD}}$ pin must be set HIGH by the application layer. For SMPTE 292M standards and signals which require faster rise and fall times, this pin should be set LOW.

5.2 Output Interfacing

The GS1528B outputs are current mode, and will drive 800mV into a 75 Ω load. These outputs are protected from accidental static damage with internal ESD protection diodes.

The SMPTE 292M, SMPTE 344M and SMPTE 259M standards require that the output of a cable driver have a source impedance of 75 Ω and a return loss of at least 15dB between 5MHz and 1.485GHz.

In order for a DDI output circuit using the GS1528B to meet this specification, the output application circuit shown in the [Typical Application Circuit on page 11](#) is recommended.

The value of L_{COMP} will vary depending on the PCB layout, with a typical value of 5.6nH. A 4.7 μ F capacitor is used for AC coupling the output of the device. This value is chosen to ensure that pathological signals can be coupled without a significant DC component occurring. Please see [Application Information on page 11](#) for more details.

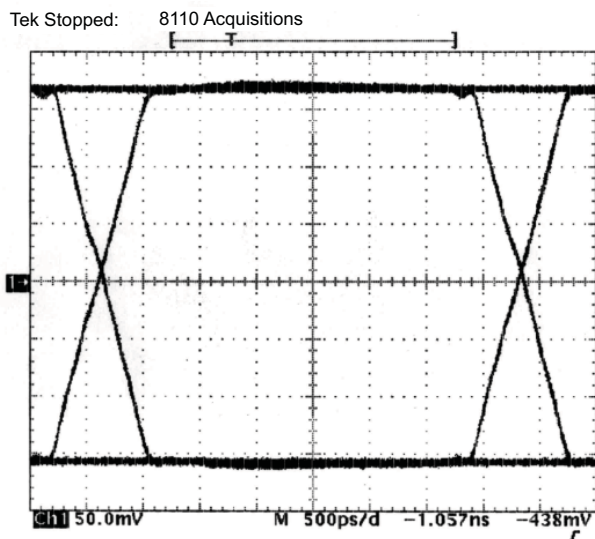


Figure 5-1: Output signal for 270Mb/s input

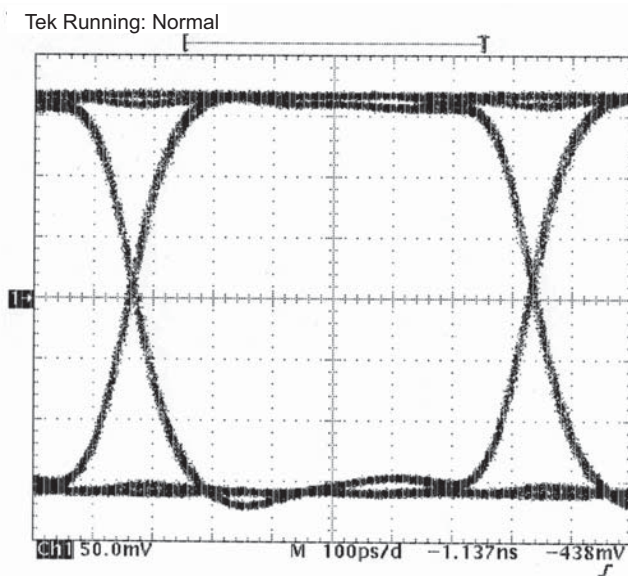


Figure 5-2: Output signal for 1.485Gb/s input

The output protection diodes act as a varactor (voltage controlled capacitor) as shown in [Figure 5-3](#). Therefore, when measuring return loss at the GS1528B output, it is necessary to take the measurement for both a logic high and a logic low output condition.

Consequently, the output capacitance of the device is dependent on the logic state of the output.

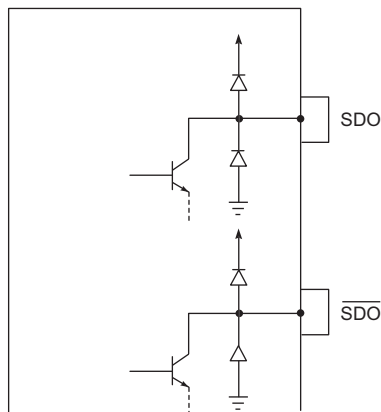


Figure 5-3: Static Protection Diodes

5.3 Output Return Loss Measurement

To perform a practical return loss measurement, it is necessary to force the GS1528B output to a DC high or low condition. The actual measured return loss will be based on the outputs being static at V_{CC} or $V_{CC}-1.6V$. Under normal operating conditions the outputs of the device swing between $V_{CC}-0.4V$ and $V_{CC}-1.2V$.

5.4 Output Amplitude Adjustment

The output amplitude of the GS1528B can be adjusted by changing the value of the R_{SET} resistor as shown in Table 5-1. For an $800mV_{p-p}$ output with a nominal $\pm 7\%$ tolerance, a value of 750Ω is required. A $\pm 1\%$ SMT resistor should be used.

The R_{SET} resistor is part of the high speed output circuit of the GS1528B. The resistor should be placed as close as possible to the R_{SET} pin. In addition, the PCB capacitance should be minimized at this node by removing the PCB groundplane beneath the R_{SET} resistor and the R_{SET} pin.

Table 5-1: R_{SET} vs V_{OD}

$R_{SET} R (\Omega)$	Output Swing (mVp-p)
995	608
824	734
750	800
680	884
573	1040

NOTE: For reliable operation of the GS1528B over the full temperature range, do not use an R_{SET} value below 573Ω .

6. Application Information

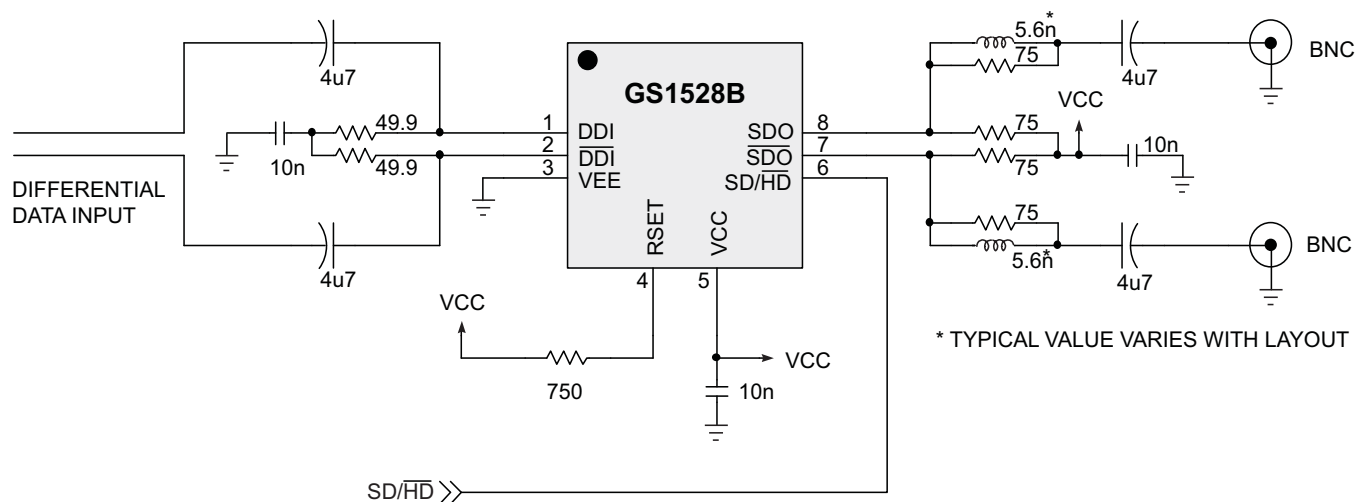
6.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV.

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- The PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to changes in trace impedance.
- The PCB groundplane is removed under the GS1528B output components to minimize parasitic capacitance.
- The PCB ground plane is removed under the GS1528B R_{SET} pin and resistor to minimize parasitic capacitance.
- Input and output BNC connectors are surface mounted in-line to eliminate a transmission line stub caused by a BNC mounting via high speed traces which are curved to minimize impedance variations due to change of PCB trace width.

6.2 Typical Application Circuit



NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.

Figure 6-1: GS1528B Typical Application Circuit

7. Package and Ordering Information

7.1 Package Dimensions

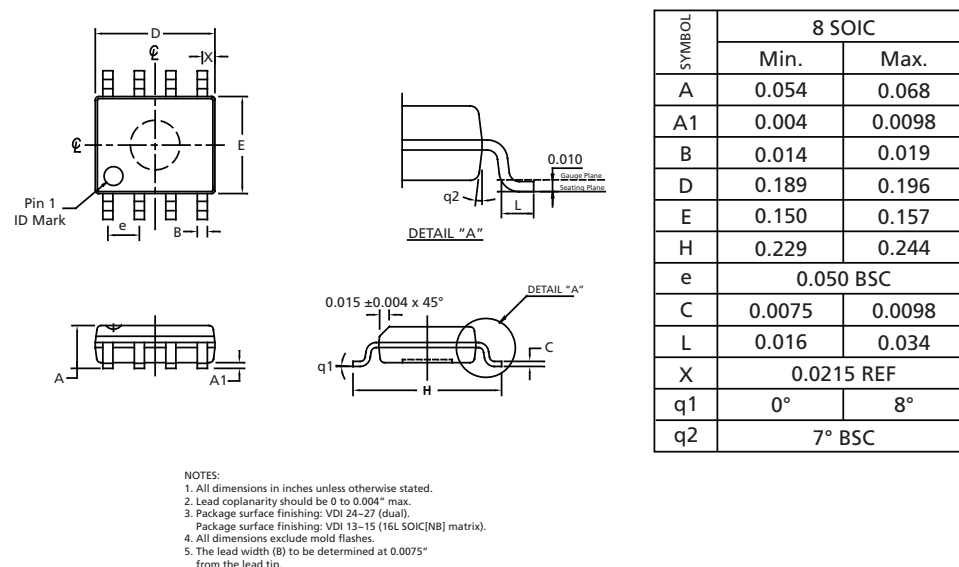


Figure 7-1: GS1528B Package Dimensions

7.2 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	8-pin SOIC
Moisture Sensitivity Level	2
Junction to Case Thermal Resistance, θ_{j-c}	72°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	116°C/W
Pb-free and RoHS Compliant	Yes

7.3 Marking Diagram



Figure 7-2: GS1528B Marking Diagram

7.4 Ordering Information

Table 7-2: Ordering Information

	Part Number	Package	Temperature Range
GS1528B	GS1528BCKAE3	8-pin SOIC	0°C to 70°C
GS1528B	GS1528BCTAE3 250pc tape & reel	8-pin SOIC	0°C to 70°C

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DATA SHEET**

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