

# RD30LDT595

## 8-bit Serial-in Parallel-out LED Driver IC

REJ03D0906-0200

Rev.2.00

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### Description

The RD30LDT595 has eight edge trigger D-type Flip-Flops with eight latches in 16-pin package. Data is input to the serial data input and the clock pulse is input to the clock input. When the clock is changed from "L" to "H", the signal of the data input enters an internal shift register. The data of the shift register is shifted one by one. In addition, output load circuit is added so that power supply prevents a wrong action in on/off. When  $V_{CC}$  is less than a fixed level, the output ( $\overline{Q1}$  to  $\overline{Q8}$ ) compulsorily is off state. Low-voltage and high-speed operation is suitable for battery-powered product (e.g., notebook computers), and the low-power consumption extends the battery life.

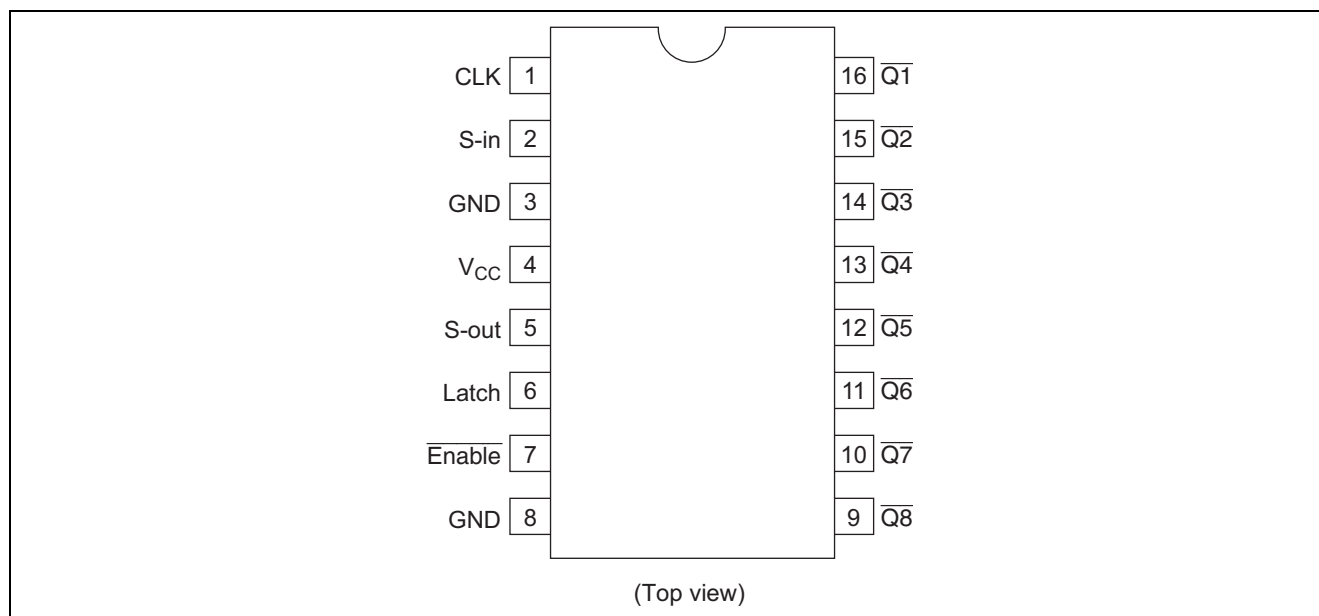
### Features

- Supply voltage range : 4.5 to 5.5 V,  $V_O = 30V$
- Output current :  $I_O = 100\text{ mA}$  (@ $V_{CC} = 5\text{ V}$ )
- All the logical input has hysteresis voltage for the slow transition.
- Input with pull-up resistance. (Enable, Latch terminal)
- Input with pull-down resistance. (CLK, S-in terminal)
- Ordering Information

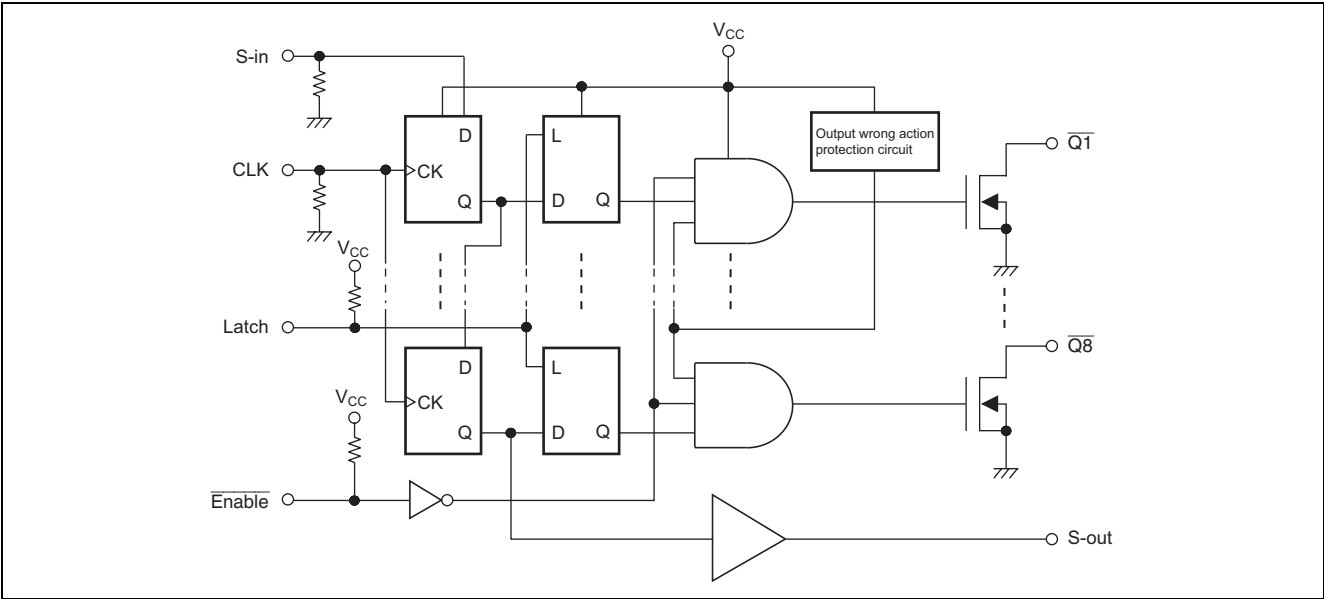
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)	Surface Treatment
RD30LDT595PT0	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	T (1,000 pcs/reel)	0 (Ni/Pd/Au)
RD30LDT595FPH0	SOP-16 pin	PRSP0016DH-B (FP-16DAV)	FP	H (2,000 pcs/reel)	0 (Ni/Pd/Au)

Note: Please consult the sales office for the above package availability.

### Pin Arrangement



Logic Diagram



Function Table

Inputs				Outputs	
S-in	CLK <sup>*1</sup>	Latch	Enable	Q1 to Q8	S-out
L	IN	L	L	t - 1	L
L	IN	H	L	Z	L
H	IN	L	L	t - 1	H
H	IN	H	L	L	H
H	IN	H	H	Z	H

<sup>\*1</sup> IN : Input the following signal in CLK



H : High level

L : Low level

Z : High impedance

t - 1 : Output level before the indicated steady state input conditions were established.

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	$V_{CC}$	-0.5 to 7	V	
Input voltage range	$V_I$	-0.5 to $V_{CC} + 0.5$	V	
Output voltage range <sup>*1</sup> ,	$V_O$	-0.5 to 30	V	Output : Z (OFF)
		-0.5 to $V_{CC} + 0.5$	V	S-out
Continuous output current	$I_O$	100	mA	$V_O = 0$ to $V_{CC}$
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) <sup>*2</sup>	$P_d$	1.19	W	DILP
		0.79		SOP
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

1. This value is limited to 30 V maximum.

2. The maximum package power dissipation was calculated using a junction temperature of  $150^\circ\text{C}$ .

## Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions		
Supply voltage range	V <sub>CC</sub>	4.5	5.5	V			
Output voltage range	V <sub>O</sub>	—	30	V	Q1 to Q8 : Z (OFF)		
Output current (per pin)	I <sub>O</sub>	0	100	mA	DILP	Duty cycle ≤ 100%	Q1 to Q8 : ON
		0	100	mA	SOP	Duty cycle ≤ 60%	
Operating free-air temperature	T <sub>a</sub>	−40	85	°C			

Note: Unused or floating inputs must be held high or low.

## Electrical Characteristic

Item	Symbol	$V_{CC}$ (V) *	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $85^\circ\text{C}$			Unit	Test condition
			Min	Typ	Max	Min	Typ	Max		
Input voltage	$V_{IH}$	4.5 to 5.5	2.0	—	$V_{CC}$	2.0	—	$V_{CC}$	V	
	$V_{IL}$	4.5 to 5.5	0	—	0.8	0	—	0.8	V	
Input current	$I_{IH}$	5.5	—	—	25	—	—	30	$\mu\text{A}$	$V_{IH} = 5.5\text{ V}$
	$I_{IL}$	5.5	—	—	-25	—	—	-30	$\mu\text{A}$	$V_{IL} = 0\text{ V}$
Output voltage (S-out)	$V_{OH}$	5.0	4.9	—	—	4.9	—	—	V	$I_{OH} = -1\text{ }\mu\text{A}$
	$V_{OL}$	5.0	—	—	0.1	—	—	0.1	V	$I_{OL} = 1\text{ }\mu\text{A}$
Output voltage ( $\overline{Q1}$ to $\overline{Q8}$ )	$V_{OL}$	5.0	—	—	0.55	—	—	0.77	V	$I_{OL} = 100\text{ mA}$
Output leakage current	$I_{OLK}$	5.5	—	—	50	—	—	100	$\mu\text{A}$	$V_O = 30\text{ V}$ (Output : Z (OFF))
Quiescent supply current	$I_{CC1}$	5.5	—	—	300	—	—	500	$\mu\text{A}$	Input : Open All driver output : OFF
	$I_{CC2}$	5.5	—	—	300	—	—	500	$\mu\text{A}$	Driver output one circuit : ON
Driver output wrong action protection voltage	$V_{T+}$	—	2.9	3.4	3.9	2.6	3.4	4.2	V	
	$V_{T-}$	—	2.6	3.1	3.6	2.3	3.1	3.9	V	

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

## Timing Characteristics

( $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $R_L(\text{S-out}) = \infty$ ,  $R_L(\overline{\text{Qn}}) = 100\ \Omega$ ,  $t_r = t_f = 20\text{ ns}$ )

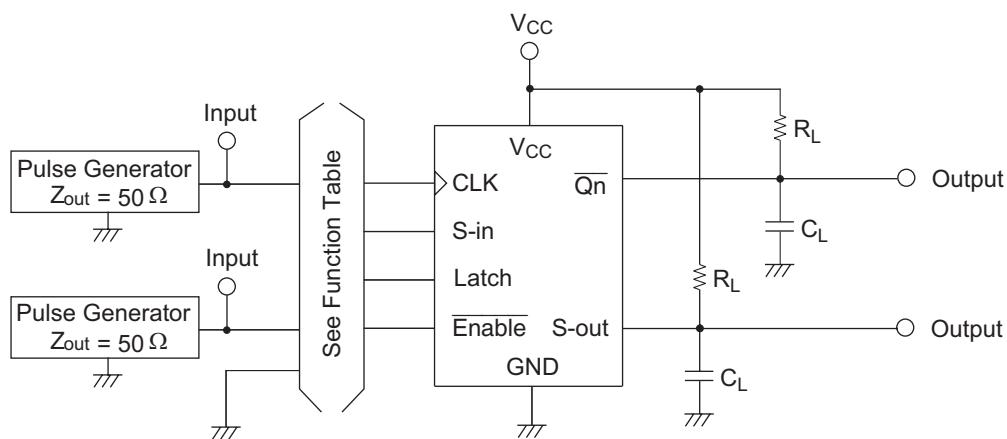
Item	Symbol	Ta = 25°C			Ta = -40 to 85°C			Unit	Test condition
		Min	Typ	Max	Min	Typ	Max		
Maximum clock frequency	$f_{\text{max}}$	—	—	12.5	—	—	12.5	MHz	Duty cycle = 45 % to 55 %
Pulse width	$t_W$	30	—	—	30	—	—	ns	CLK
Pulse width	$t_W$	30	—	—	30	—	—	ns	Latch
Setup time	$t_{\text{su}}$	30	—	—	30	—	—	ns	S-in to CLK
Hold time	$t_h$	20	—	—	20	—	—	ns	S-in to CLK
Setup time	$t_{\text{su}}$	60	—	—	60	—	—	ns	Latch to CLK
Clock pulse rise time	$t_r$	—	—	500	—	—	500	ns	
Clock pulse fall time	$t_f$	—	—	500	—	—	500	ns	

## Switching Characteristics

( $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $R_L(\text{S-out}) = \infty$ ,  $R_L(\overline{\text{Qn}}) = 100\ \Omega$ ,  $t_r = t_f = 20\text{ ns}$ )

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C			Unit	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Typ	Max			
Propagation delay time	$t_{\text{PLH}}$	—	—	60	—	—	60	ns	CLK	S-out
	$t_{\text{PHL}}$	—	—	60	—	—	60			
	$t_{\text{PLH}}$	—	—	70	—	—	70	ns	CLK	$\overline{\text{Qn}}$
	$t_{\text{PHL}}$	—	—	70	—	—	70			
	$t_{\text{PLH}}$	—	—	70	—	—	70	ns	$\overline{\text{Enable}}$	$\overline{\text{Qn}}$
	$t_{\text{PHL}}$	—	—	70	—	—	70			

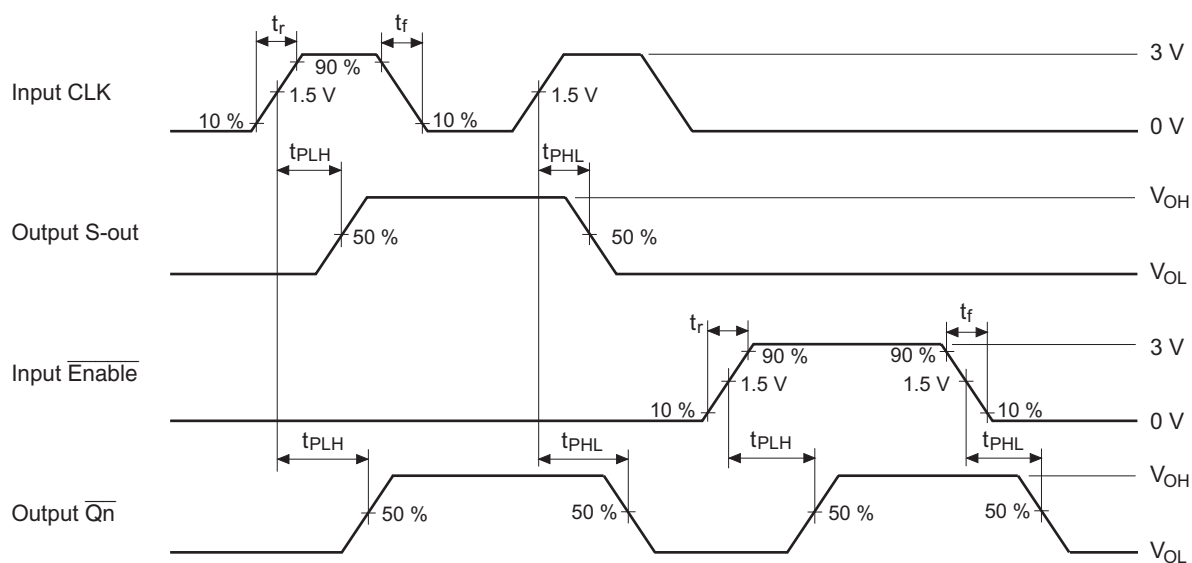
## Test Circuit



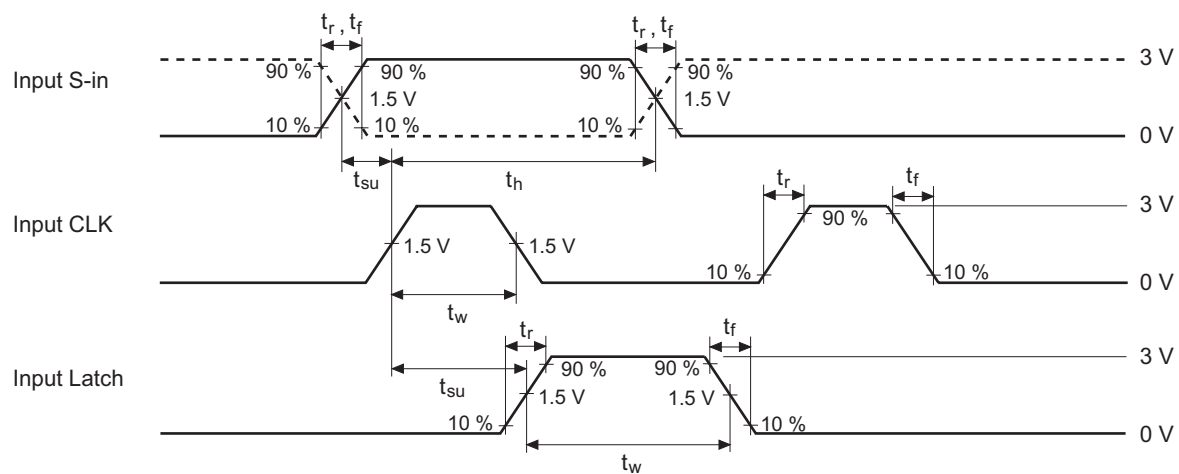
- Notes 1. Input waveform : PRR  $\leq 1\text{ MHz}$ , Duty Cycle = 50%,  $t_r \leq 20\text{ ns}$ ,  $t_f \leq 20\text{ ns}$   
 2.  $C_L$  includes probe and jig capacitance.

## Waveforms

## • Waveform – 1



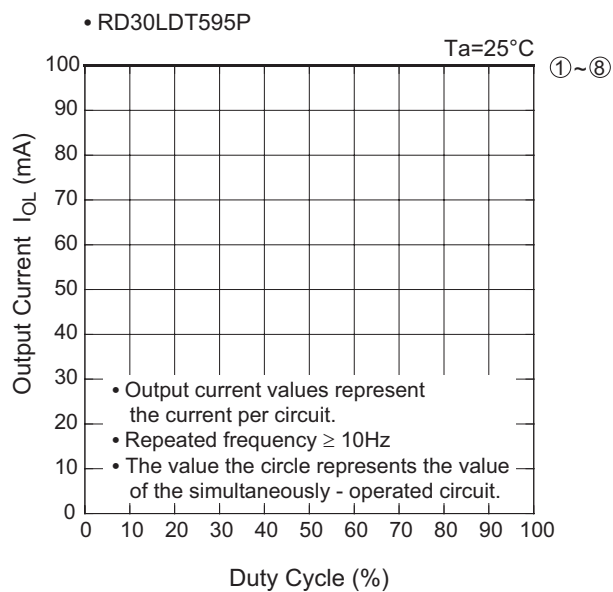
## • Waveform – 2



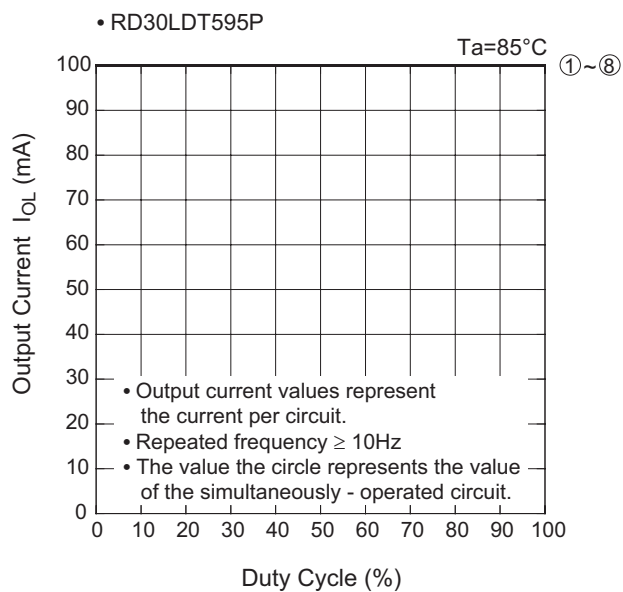
- Notes
1. Input waveform :  $\text{PRR} \leq 1 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 20 \text{ ns}$ ,  $t_f \leq 20 \text{ ns}$
  2. The output are measured one at a time with one transition per measurement.

## Application Data

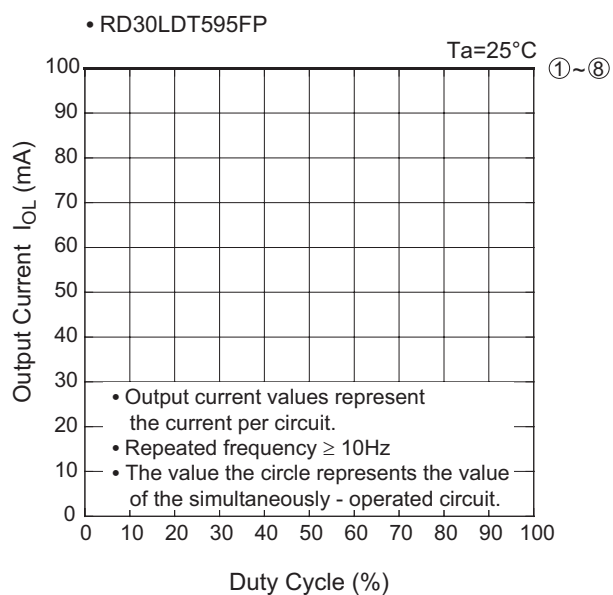
Duty Cycle – Output Current Characteristics



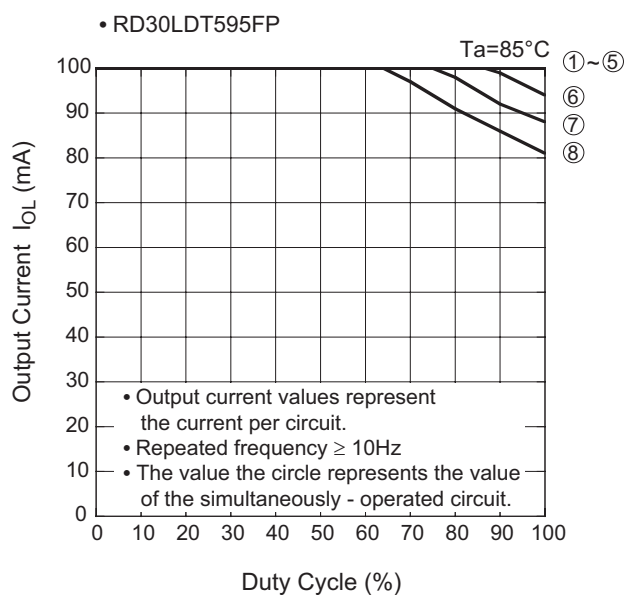
Duty Cycle – Output Current Characteristics



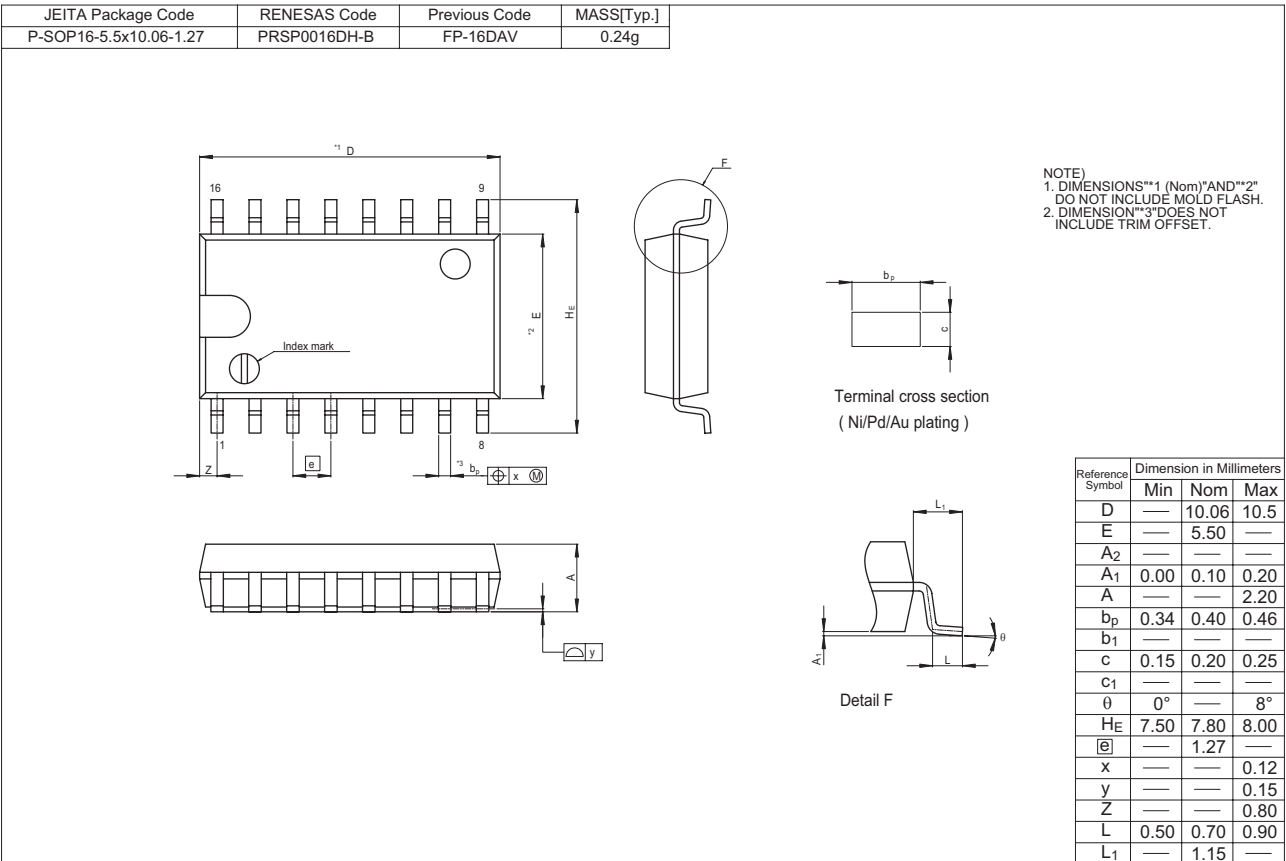
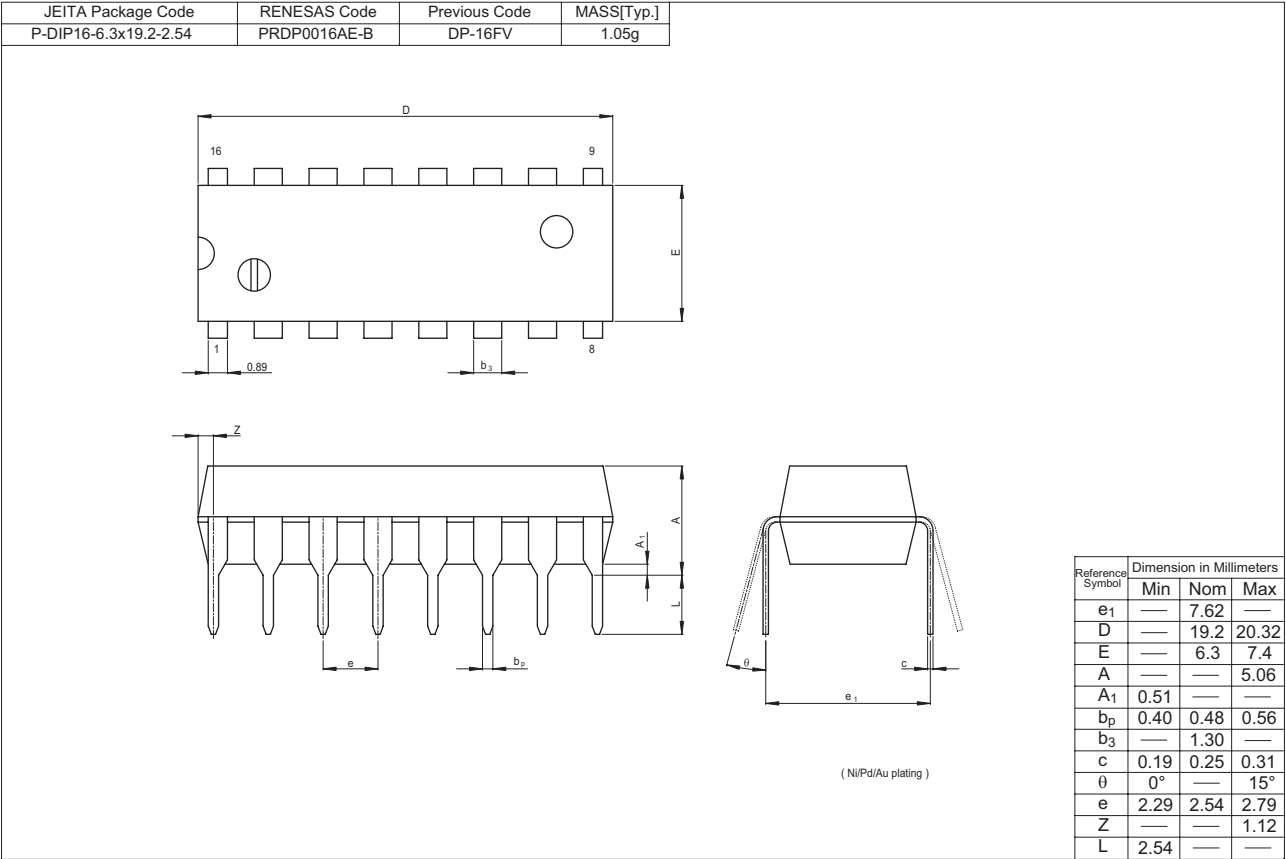
Duty Cycle – Output Current Characteristics



Duty Cycle – Output Current Characteristics



Package Dimensions



Notes:

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Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120  
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**Renesas Technology Taiwan Co., Ltd.**  
10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
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**Renesas Technology Singapore Pte. Ltd.**  
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**  
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**  
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510