RD30LDT595

8–bit Serial–in Parallel–out LED Driver IC

REJ03D0906-0200
Rev.2.00
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Description

The RD30LDT595 has eight edge trigger D–type Flip–Flops with eight latches in 16–pin package. Data is input to the serial data input and the clock pulse is input to the clock input. When the clock is changed from ”L” to ”H”, the signal of the data input enters an internal shift register. The data of the shift register is shifted one by one. In addition, output load circuit is added so that power supply prevents a wrong action in on/off. When Vcc is less than a fixed level, the output ($\overline{Q1}$ to $\overline{Q8}$) compulsorily is off state. Low–voltage and high–speed operation is suitable for battery–powered product (e.g., notebook computers), and the low–power consumption extends the battery life.

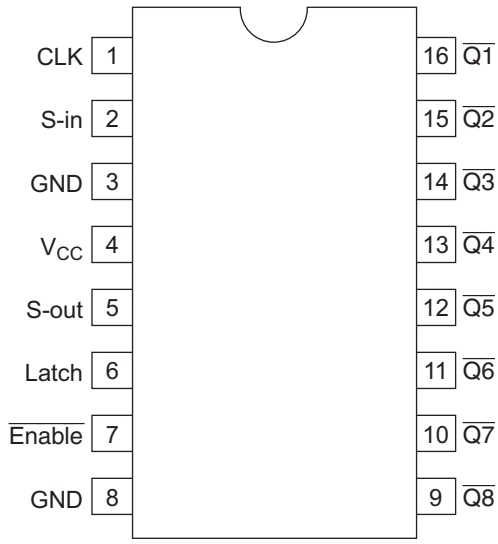
Features

- Supply voltage range : 4.5 to 5.5 V, V_O = 30V
- Output current : I_O = 100 mA (@V_{CC} = 5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Input with pull-up resistance. ($\overline{Enable}$, Latch terminal)
- Input with pull-down resistance. (CLK, S-in terminal)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)	Surface Treatment
RD30LDT595PT0	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	T (1,000 pcs/reel)	0 (Ni/Pd/Au)
RD30LDT595FPH0	SOP-16 pin	PRSP0016DH-B (FP-16DAV)	FP	H (2,000 pcs/reel)	0 (Ni/Pd/Au)

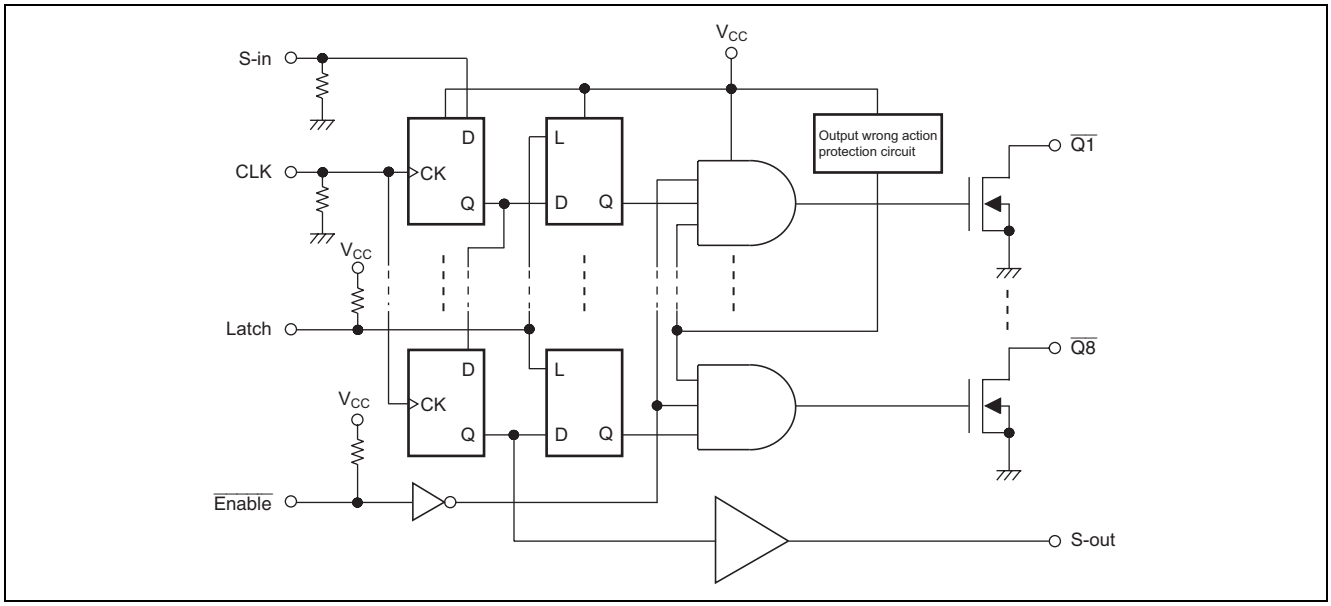
Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

Logic Diagram



Function Table

Inputs				Outputs	
S-in	CLK *1	Latch	$\overline{\text{Enable}}$	$\overline{Q1}$ to $\overline{Q8}$	S-out
L	IN	L	L	t - 1	L
L	IN	H	L	Z	L
H	IN	L	L	t - 1	H
H	IN	H	L	L	H
H	IN	H	H	Z	H

*1 IN : Input the following signal in CLK

H : High level
L : Low level
Z : High impedance
t - 1 : Output level before the indicated steady state input conditions were established.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	V_{CC}	–0.5 to 7	V	
Input voltage range	V_I	–0.5 to V_{CC} + 0.5	V	
Output voltage range [*1,]	V_O	–0.5 to 30	V	Output : Z (OFF)
		–0.5 to V_{CC} + 0.5	V	S-out
Continuous output current	I_O	100	mA	V_O = 0 to V_{CC}
Maximum power dissipation at Ta = 25°C (in still air) [*2]	P_d	1.19	W	DILP
		0.79		SOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

1. This value is limited to 30 V maximum.
2. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions		
Supply voltage range	V_{CC}	4.5	5.5	V			
Output voltage range	V_O	—	30	V	$\overline{Q1}$ to $\overline{Q8}$: Z (OFF)		
Output current (per pin)	I_O	0	100	mA	DILP	Duty cycle ≤ 100%	$\overline{Q1}$ to $\overline{Q8}$: ON
		0	100	mA	SOP	Duty cycle ≤ 60%	
Operating free-air temperature	T_a	–40	85	°C			

Note: Unused or floating inputs must be held high or low.

Electrical Characteristic

Item	Symbol	V_{CC} (V) *	Ta = 25°C			Ta = –40 to 85°C			Unit	Test condition
			Min	Typ	Max	Min	Typ	Max		
Input voltage	V_{IH}	4.5 to 5.5	2.0	—	V_{CC}	2.0	—	V_{CC}	V	
	V_{IL}	4.5 to 5.5	0	—	0.8	0	—	0.8	V	
Input current	I_{IH}	5.5	—	—	25	—	—	30	µA	V_{IH} = 5.5 V
	I_{IL}	5.5	—	—	–25	—	—	–30	µA	V_{IL} = 0 V
Output voltage (S-out)	V_{OH}	5.0	4.9	—	—	4.9	—	—	V	I_{OH} = –1 µA
	V_{OL}	5.0	—	—	0.1	—	—	0.1	V	I_{OL} = 1 µA
Output voltage ($\overline{Q1}$ to $\overline{Q8}$)	V_{OL}	5.0	—	—	0.55	—	—	0.77	V	I_{OL} = 100 mA
Output leakage current	I_{OLK}	5.5	—	—	50	—	—	100	µA	V_O = 30 V (Output : Z (OFF))
Quiescent supply current	$I_{CC}1$	5.5	—	—	300	—	—	500	µA	Input : Open All driver output : OFF
	$I_{CC}2$	5.5	—	—	300	—	—	500	µA	Driver output one circuit : ON
Driver output wrong action protection voltage	V_T+	—	2.9	3.4	3.9	2.6	3.4	4.2	V	
	V_T-	—	2.6	3.1	3.6	2.3	3.1	3.9	V	

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Timing Characteristics

(V_{CC} = 5 V, C_L = 15 pF, R_L (S-out) = ∞, R_L ($\overline{Qn}$) = 100 Ω, $t_r = t_f$ = 20 ns)

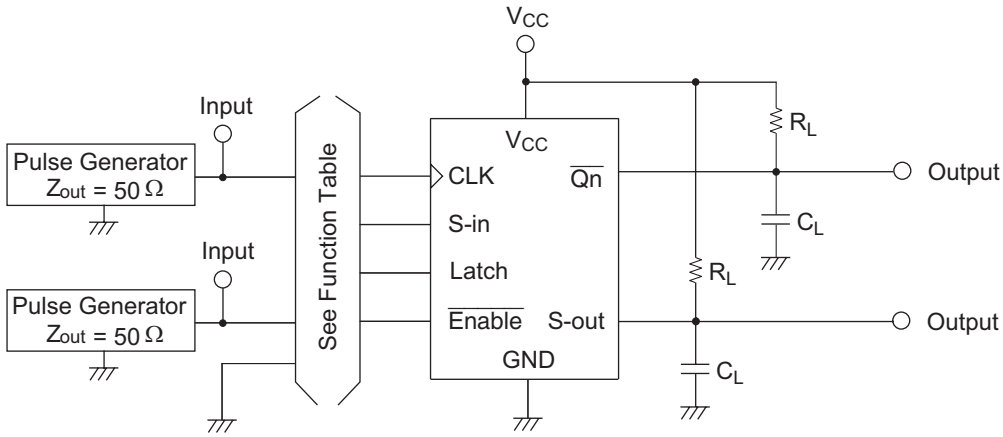
Item	Symbol	Ta = 25°C			Ta = –40 to 85°C			Unit	Test condition
		Min	Typ	Max	Min	Typ	Max		
Maximum clock frequency	f_{max}	—	—	12.5	—	—	12.5	MHz	Duty cycle = 45 % to 55 %
Pulse width	t_W	30	—	—	30	—	—	ns	CLK
Pulse width	t_W	30	—	—	30	—	—	ns	Latch
Setup time	t_{su}	30	—	—	30	—	—	ns	S-in to CLK
Hold time	t_h	20	—	—	20	—	—	ns	S-in to CLK
Setup time	t_{su}	60	—	—	60	—	—	ns	Latch to CLK
Clock pulse rise time	t_r	—	—	500	—	—	500	ns	
Clock pulse fall time	t_f	—	—	500	—	—	500	ns	

Switching Characteristics

(V_{CC} = 5 V, C_L = 15 pF, R_L (S-out) = ∞, R_L ($\overline{Qn}$) = 100 Ω , $t_r = t_f$ = 20 ns)

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C			Unit	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Typ	Max			
Propagation delay time	t_{PLH}	—	—	60	—	—	60	ns	CLK	S-out
	t_{PHL}	—	—	60	—	—	60			
	t_{PLH}	—	—	70	—	—	70	ns	CLK	$\overline{Qn}$
	t_{PHL}	—	—	70	—	—	70			
	t_{PLH}	—	—	70	—	—	70	ns	$\overline{Enable}$	$\overline{Qn}$
	t_{PHL}	—	—	70	—	—	70			

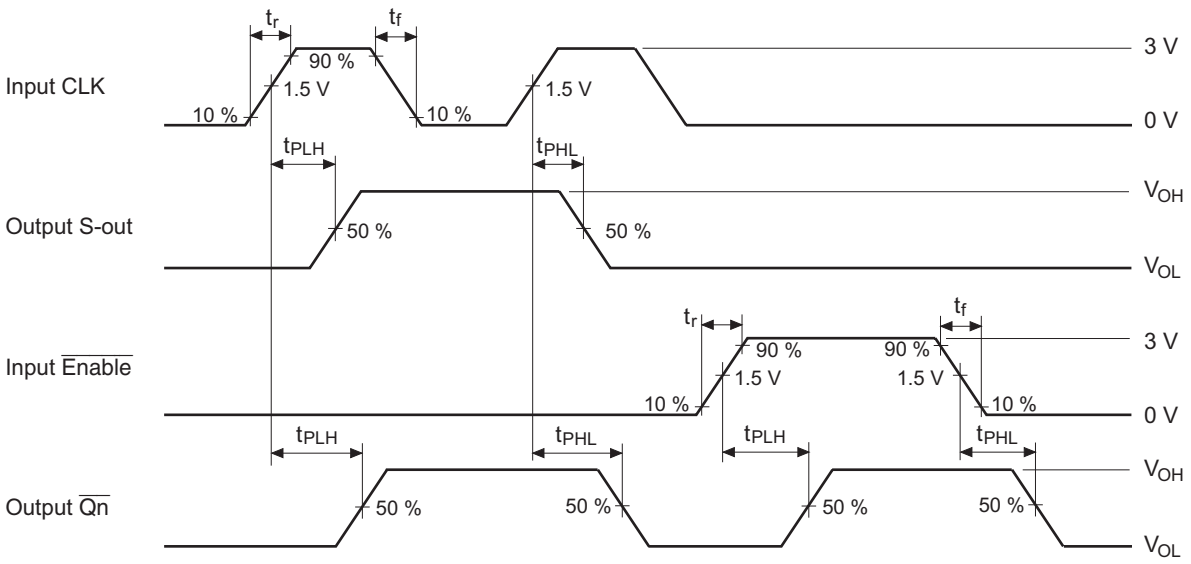
Test Circuit



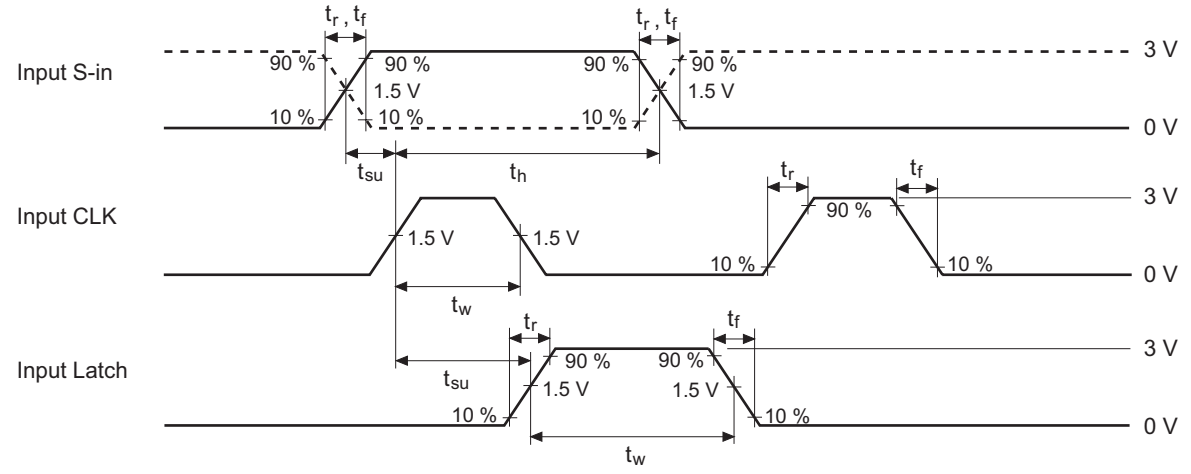
Notes 1. Input waveform : PRR ≤ 1MHz, Duty Cycle = 50%, tr ≤ 20ns, tf ≤ 20ns
2. C_L includes probe and jig capacitance.

Waveforms

• Waveform – 1



• Waveform – 2



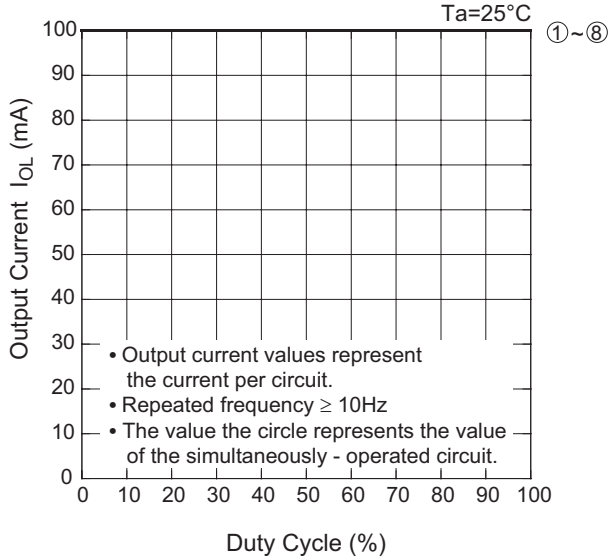
Notes 1. Input waveform : PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 20 ns, t_f ≤ 20 ns
2. The output are measured one at a time with one transition per measurement.

Application Data

Duty Cycle – Output Current Characteristics

• RD30LDT595P

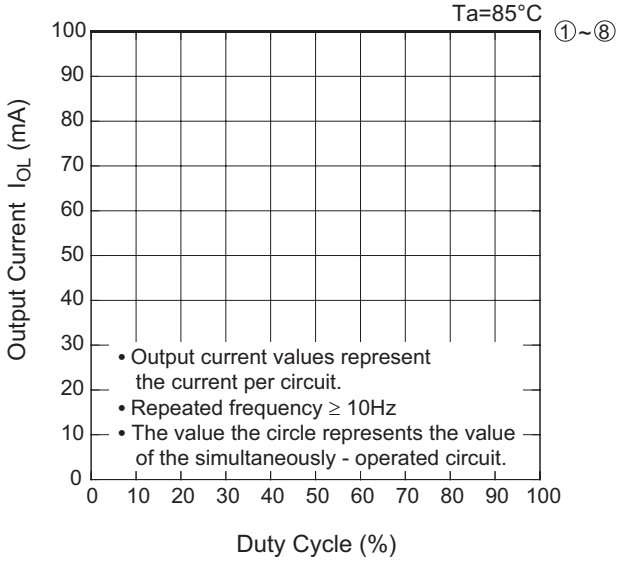
Ta=25°C



Duty Cycle – Output Current Characteristics

• RD30LDT595P

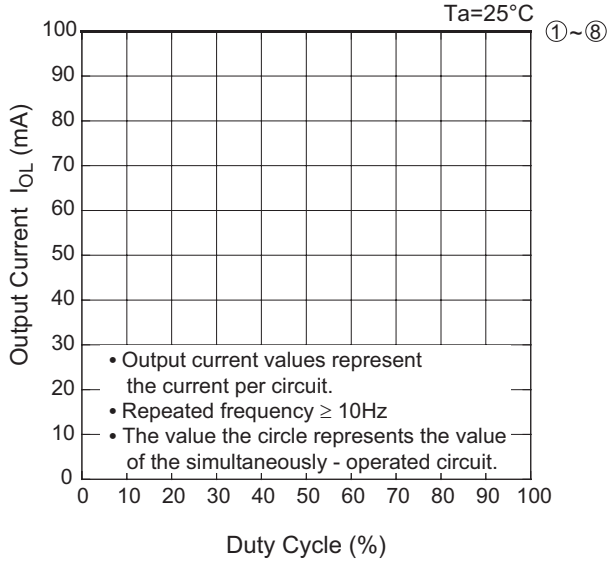
Ta=85°C



Duty Cycle – Output Current Characteristics

• RD30LDT595FP

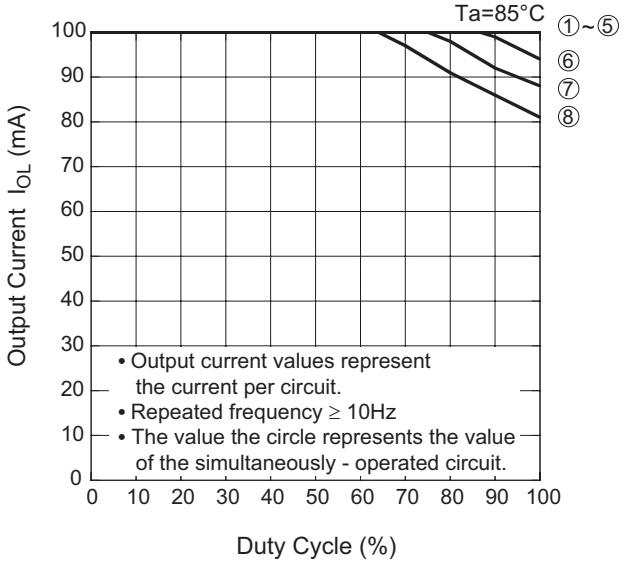
Ta=25°C



Duty Cycle – Output Current Characteristics

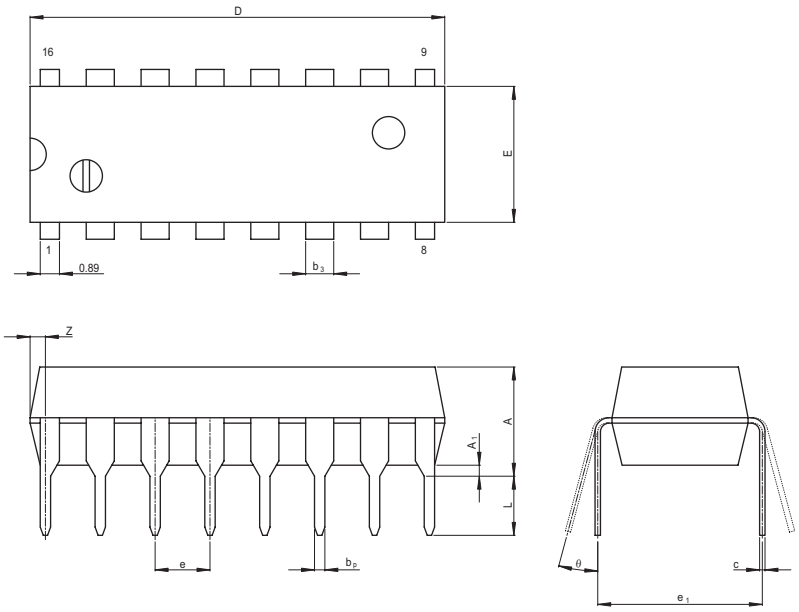
• RD30LDT595FP

Ta=85°C



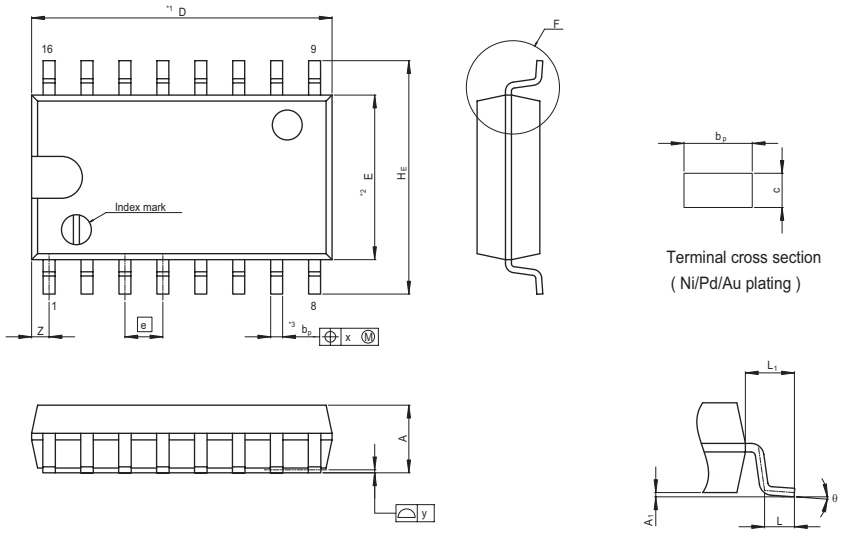
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.62	—
D	—	19.2	20.32
E	—	6.3	7.4
A	—	—	5.06
A_1	0.51	—	—
b_p	0.40	0.48	0.56
b_3	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.12
L	2.54	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L_1	—	1.15	—

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http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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Colophon .7.2