

RQJ0304DQDQA

Silicon P Channel MOS FET
Power Switching

REJ03G1717-0100

Rev.1.00

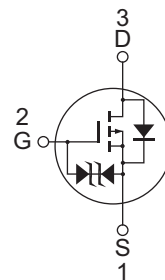
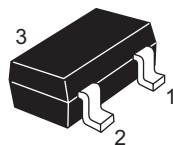
Jul 28, 2008

Features

- Low gate drive
 $V_{DSS} : -30 \text{ V}$ and 2.5 V gate drive
- Low drive current
- High speed switching
- Small traditional package (MPAK)

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Notes: Marking is "DQ".

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	+8 / -12	V
Drain current	I_D	-1.8	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-8	A
Body - drain diode reverse drain current	I_{DR}	1.8	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4 $40 \times 40 \times 1 \text{ mm}$)

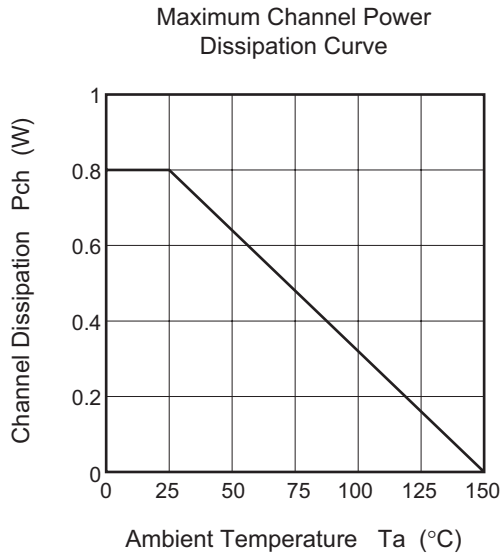
Electrical Characteristics

(Ta = 25°C)

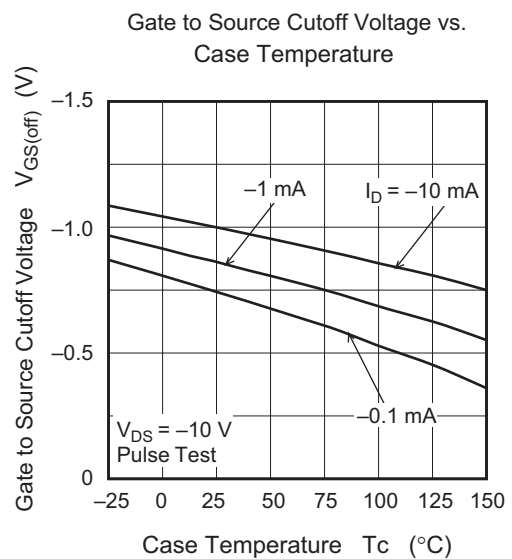
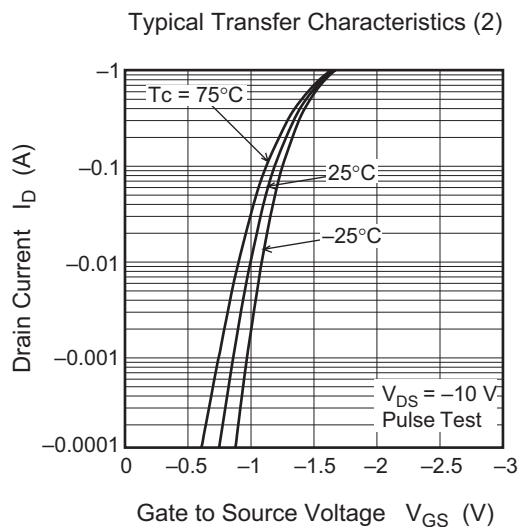
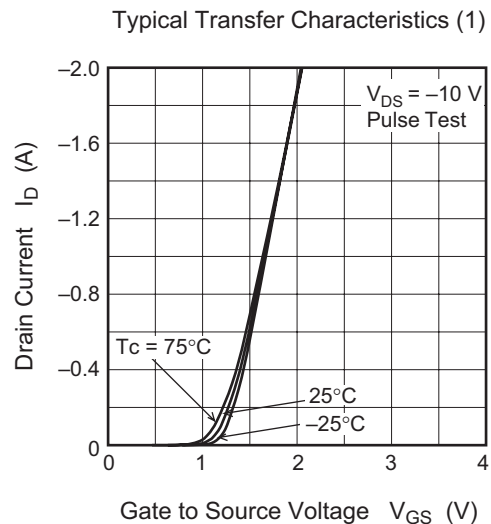
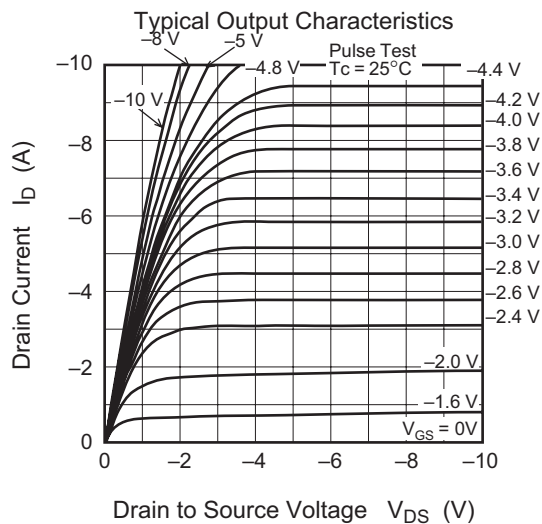
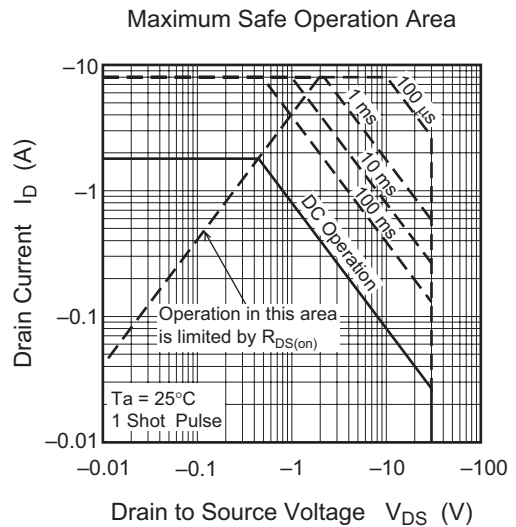
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+8	—	—	V	$I_G = +100 \mu\text{A}$, $V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-12	—	—	V	$I_G = -100 \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +6 \text{ V}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-10	μA	$V_{GS} = -10 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	—	-1.4	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	195	245	$\text{m}\Omega$	$I_D = -1.0 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note3}
Drain to source on state resistance	$R_{DS(on)}$	—	300	420	$\text{m}\Omega$	$I_D = -1.0 \text{ A}$, $V_{GS} = -2.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	1.8	2.5	—	S	$I_D = -1.0 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	185	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	45	—	pF	
Reverse transfer capacitance	C_{rss}	—	25	—	pF	
Turn - on delay time	$t_{d(on)}$	—	18	—	ns	$I_D = -1.0 \text{ A}$ $V_{GS} = -4.5 \text{ V}$ $R_L = 10 \Omega$ $R_g = 4.7 \Omega$
Rise time	t_r	—	33	—	ns	
Turn - off delay time	$t_{d(off)}$	—	22	—	ns	
Fall time	t_f	—	5	—	ns	
Total gate charge	Q_g	—	1.9	—	nC	$V_{DD} = -10 \text{ V}$
Gate to Source charge	Q_{gs}	—	0.4	—	nC	$V_{GS} = -4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	0.7	—	nC	$I_D = -2.0 \text{ A}$
Body - drain diode forward voltage	V_{DF}	—	-0.9	-1.3	V	$I_F = -2.0 \text{ A}$, $V_{GS} = 0$ ^{Note3}

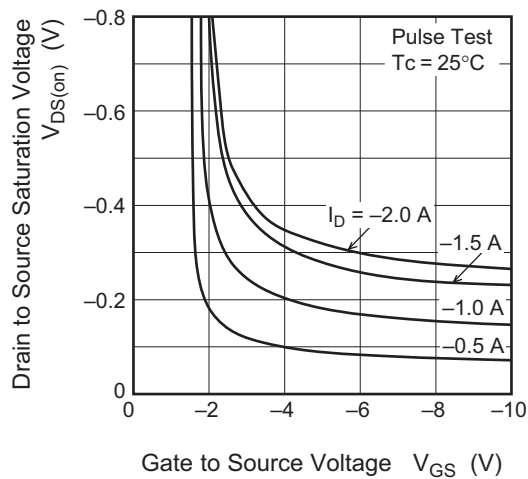
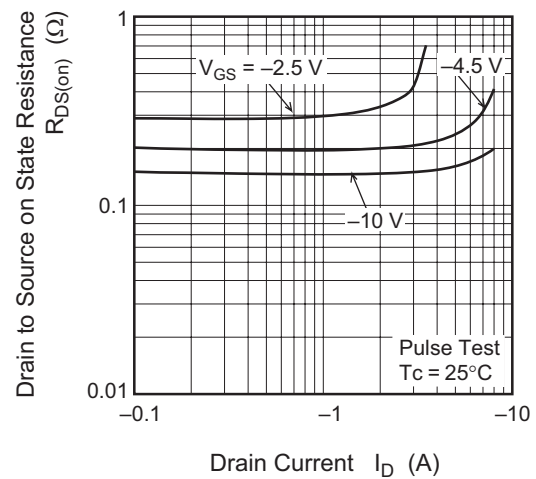
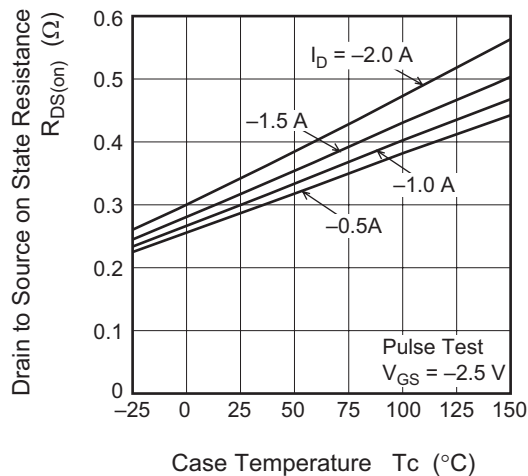
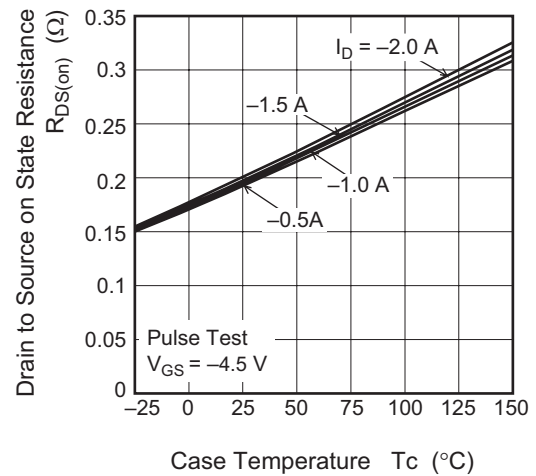
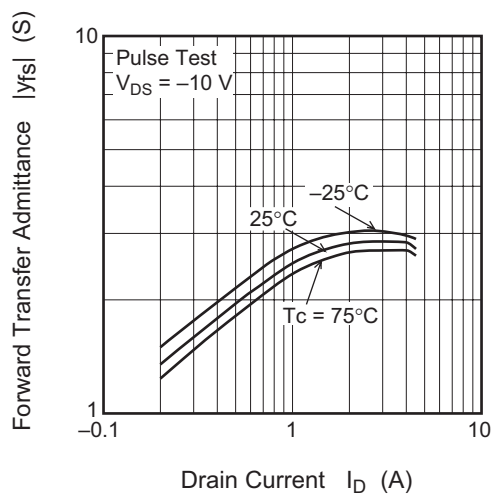
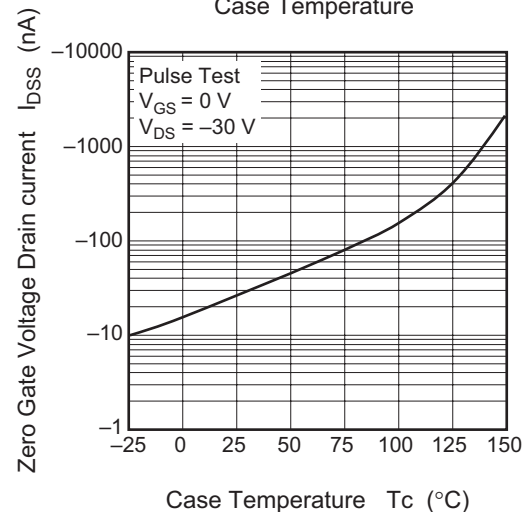
Notes: 3. Pulse test

Main Characteristics

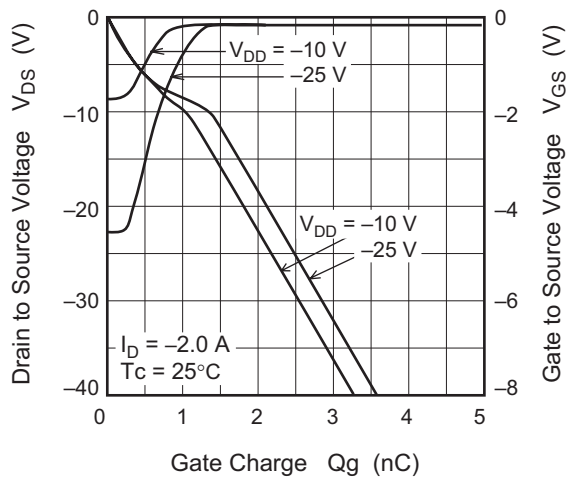


*When using the glass epoxy board (FR-4 40 x 40 x 1 mm)

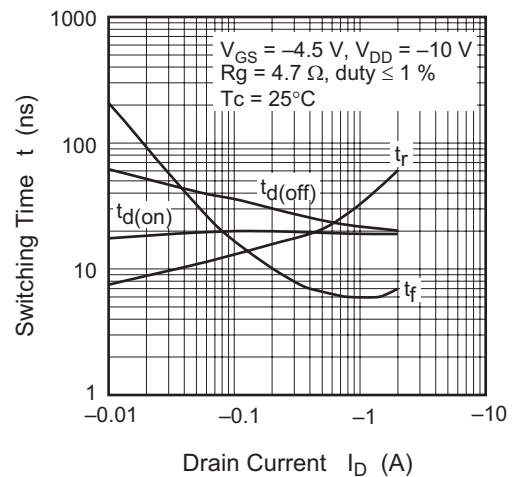


Drain to Source Saturation Voltage vs.
Gate to Source VoltageStatic Drain to Source on State Resistance
vs. Drain CurrentStatic Drain to Source on State Resistance
vs. Case Temperature (1)Static Drain to Source on State Resistance
vs. Case Temperature (2)Forward Transfer Admittance vs.
Drain CurrentZero Gate Voltage Drain current vs.
Case Temperature

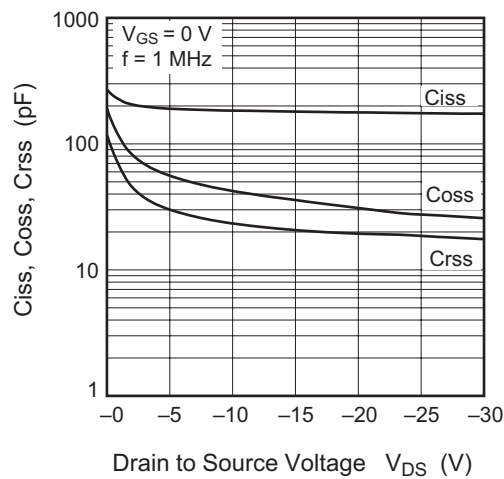
Dynamic Input Characteristics



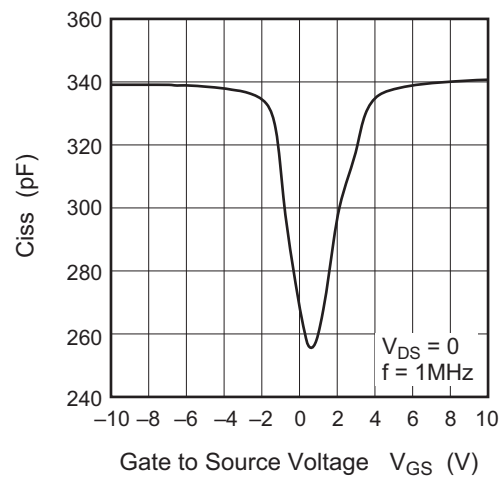
Switching Characteristics



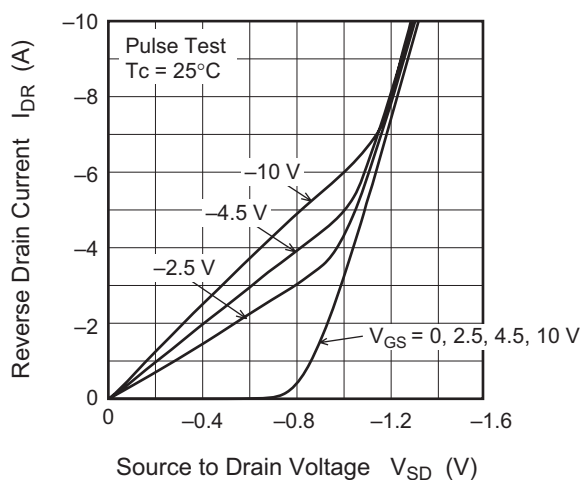
Typical Capacitance vs. Drain to Source Voltage



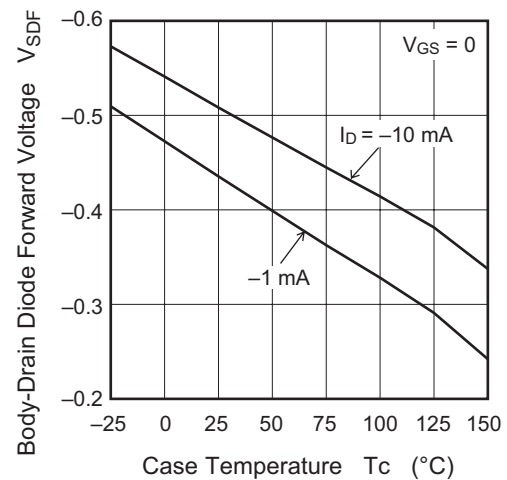
Input Capacitance vs. Gate to Source Voltage



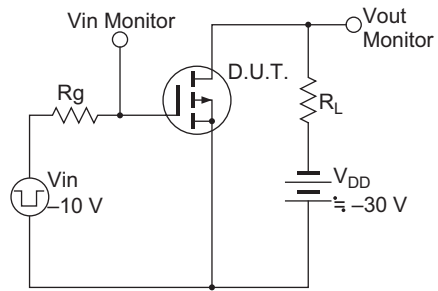
Reverse Drain Current vs. Source to Drain Voltage



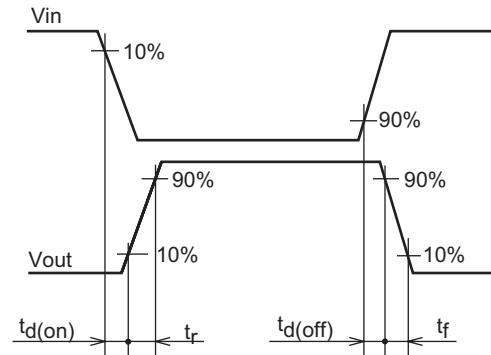
Body-Drain Diode Forward Voltage vs. Case Temperature



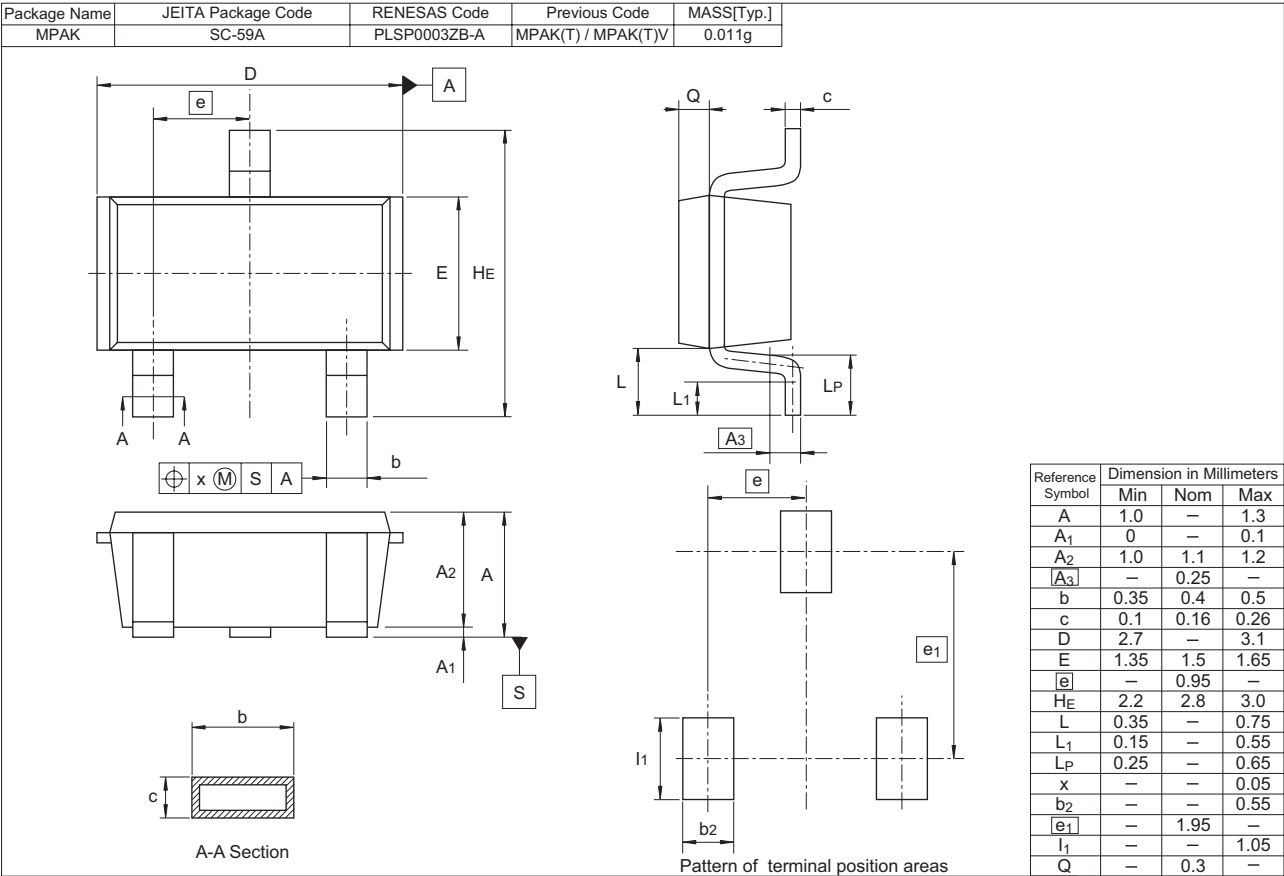
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RQJ0304DQDQATL-E	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

Notes:

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