

RQK0203SGDQA

Silicon N Channel MOS FET
Power Switching

REJ03G1323-0300

Rev.3.00

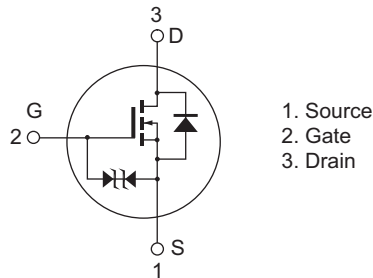
Jun 12, 2006

Features

- Low on-resistance
 $R_{DS(on)} = 68 \text{ m}\Omega$ typ ($V_{GS} = 4.5 \text{ V}$, $I_D = 1.5 \text{ A}$)
- Low drive current
- High speed switching
- 2.5 V gate drive

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



Note: Marking is "SG".

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	± 12	V
Drain current	I_D	2.9	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	10	A
Body - drain diode reverse drain current	I_{DR}	2.9	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. When using the glass epoxy board (FR-4: 40 x 40 x 1 mm)

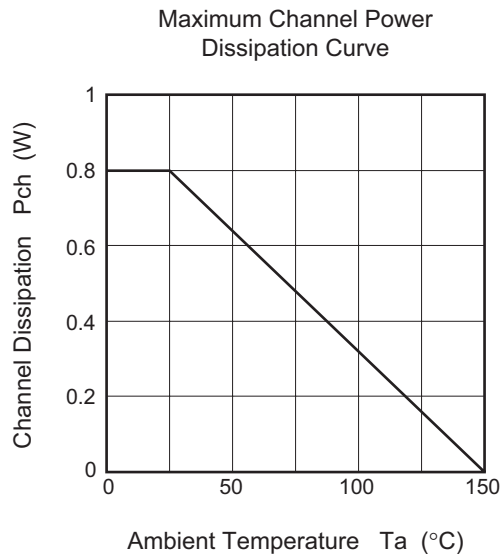
Electrical Characteristics

(Ta = 25°C)

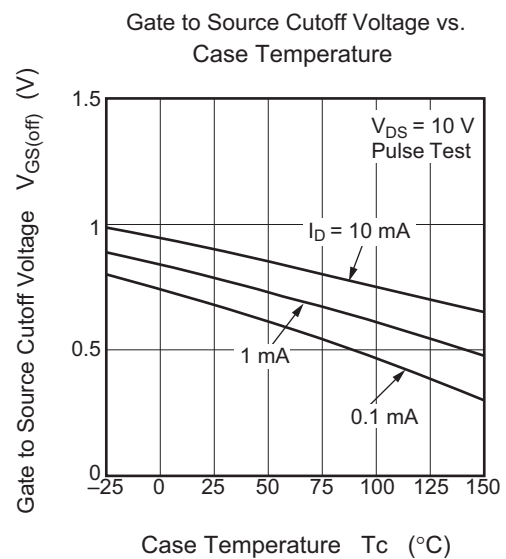
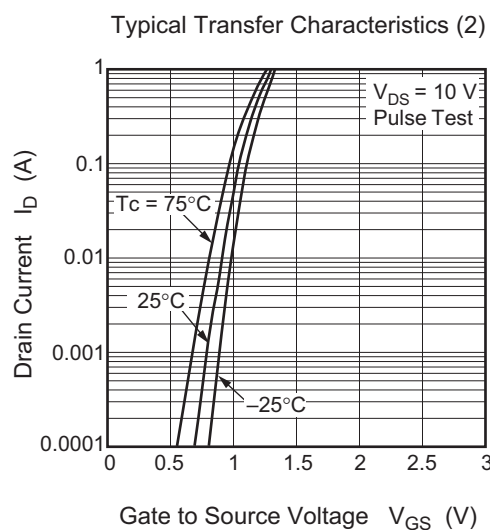
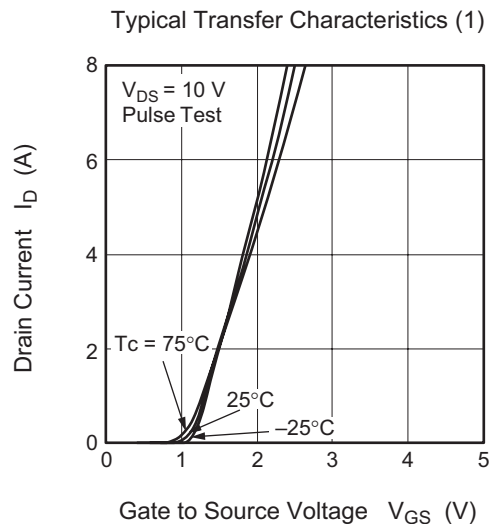
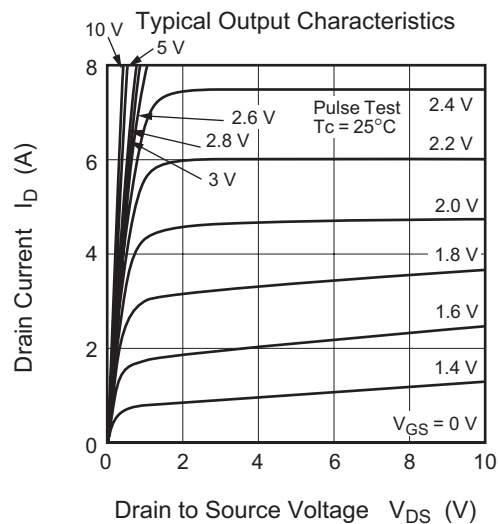
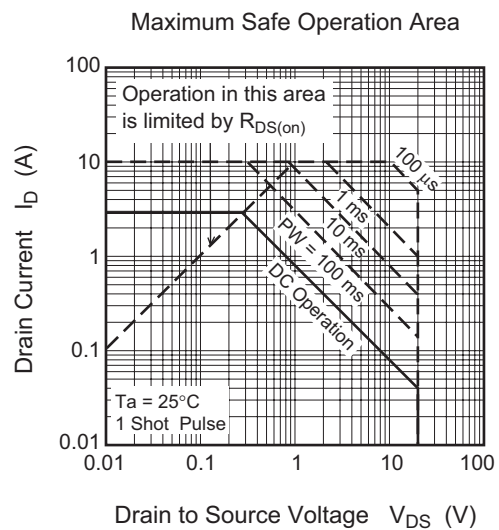
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 12	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 10 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	1	μA	$V_{DS} = 20 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	68	90	$\text{m}\Omega$	$I_D = 1.5 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	105	150	$\text{m}\Omega$	$I_D = 1.5 \text{ A}$, $V_{GS} = 2.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	3.0	5.0	—	S	$I_D = 1.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	159	—	pF	$V_{DS} = 10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	48	—	pF	
Reverse transfer capacitance	C_{rss}	—	20	—	pF	
Turn - on delay time	$t_{d(on)}$	—	11	—	ns	$I_D = 1.5 \text{ A}$ $V_{GS} = 4.5 \text{ V}$ $R_L = 6.6 \text{ }\Omega$ $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	81	—	ns	
Turn - off delay time	$t_{d(off)}$	—	27	—	ns	
Fall time	t_f	—	8	—	ns	
Total gate charge	Q_g	—	1.9	—	nC	$V_{DD} = 10 \text{ V}$ $V_{GS} = 4.5 \text{ V}$ $I_D = 2.9 \text{ A}$
Gate to source charge	Q_{gs}	—	0.4	—	nC	
Gate to drain charge	Q_{gd}	—	0.5	—	nC	
Body - drain diode forward voltage	V_{DF}	—	0.85	1.1	V	$I_F = 2.9 \text{ A}$, $V_{GS} = 0$ ^{Note3}

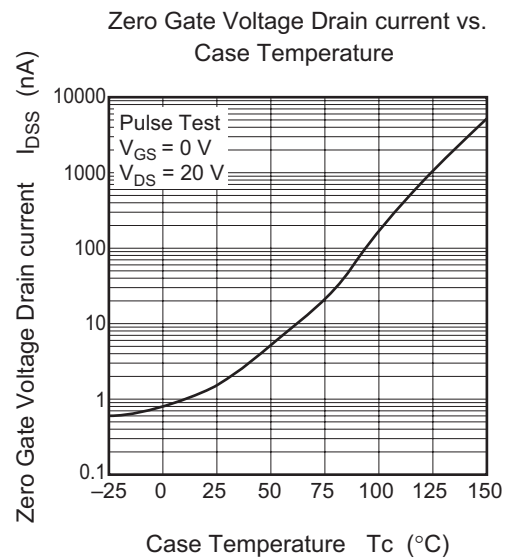
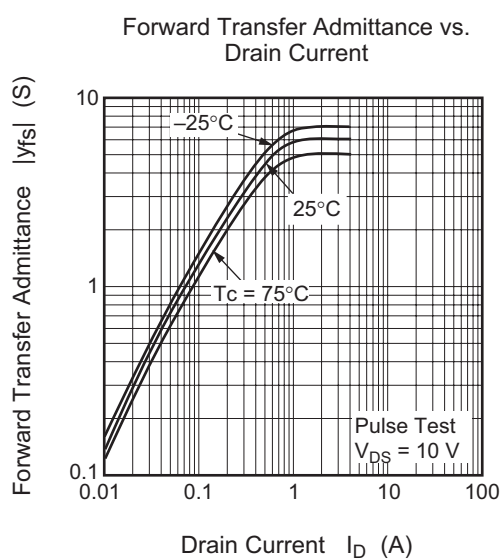
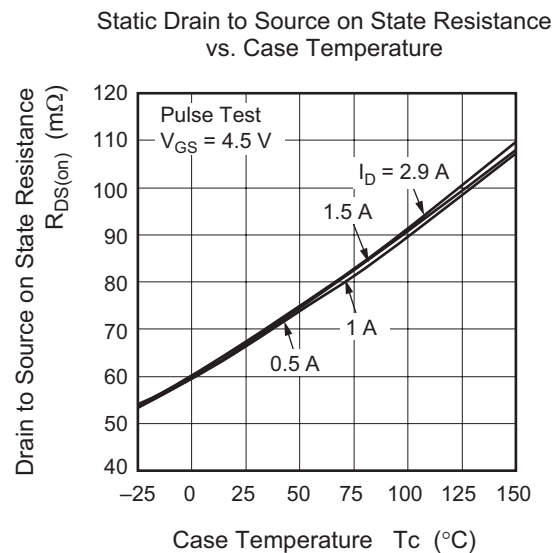
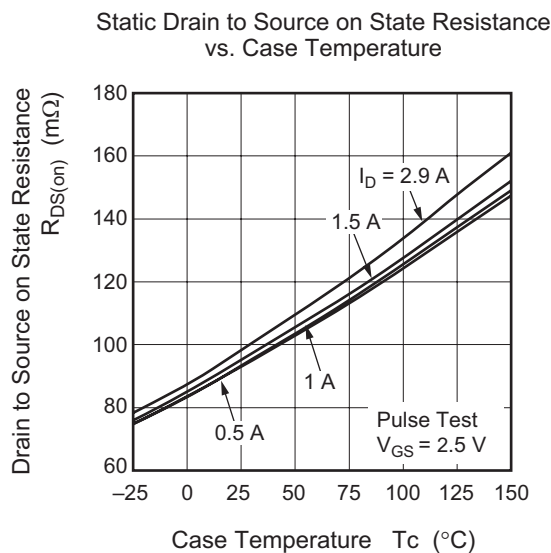
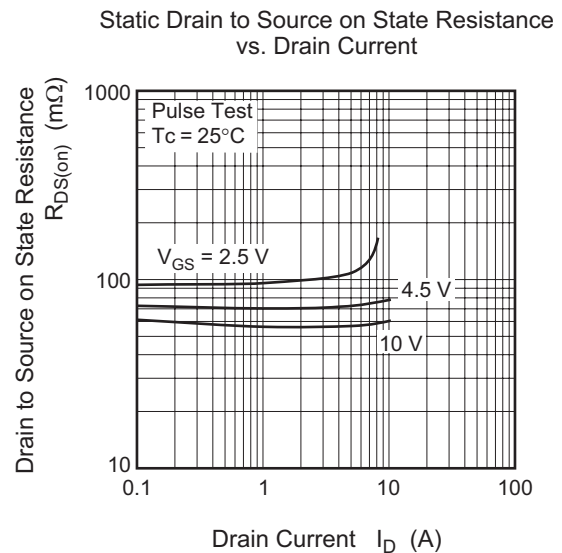
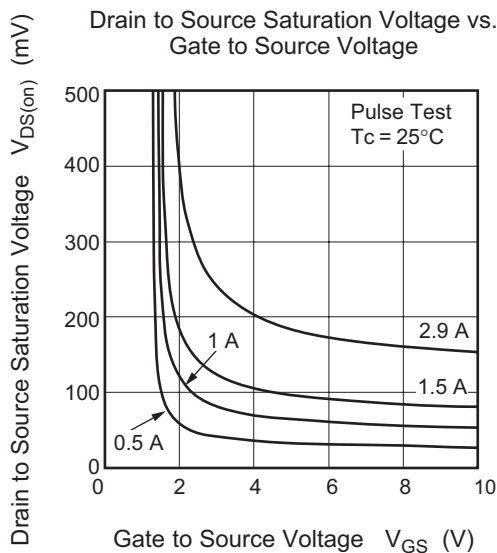
Notes: 3. Pulse test

Main Characteristics

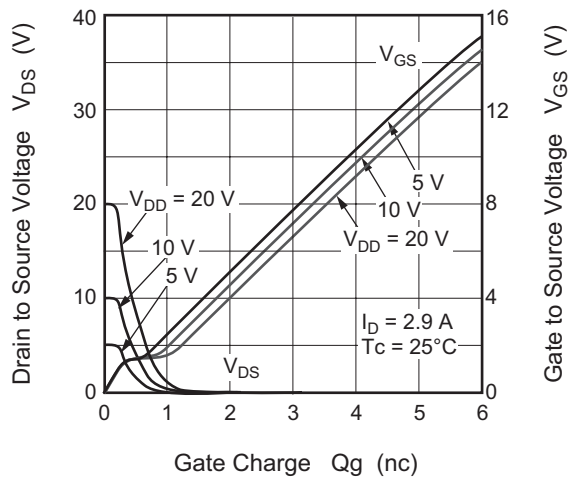


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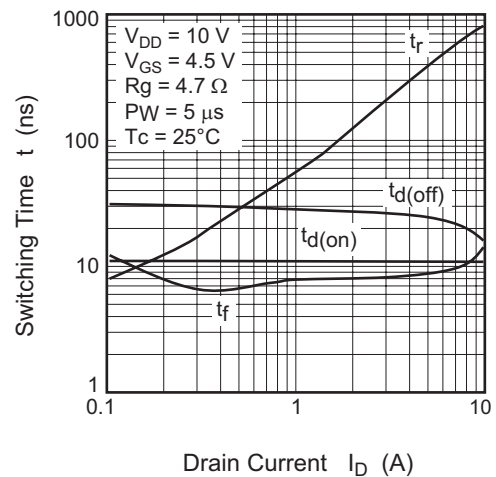




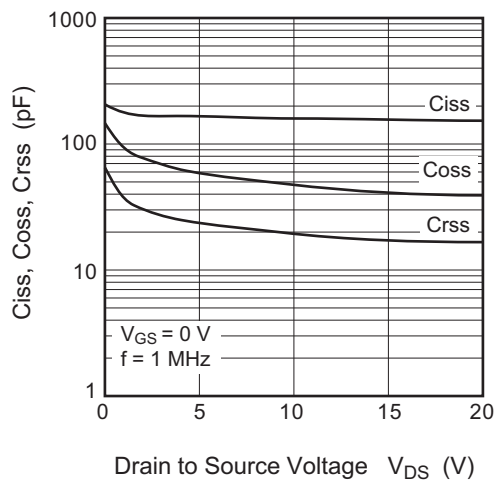
Dynamic Input Characteristics



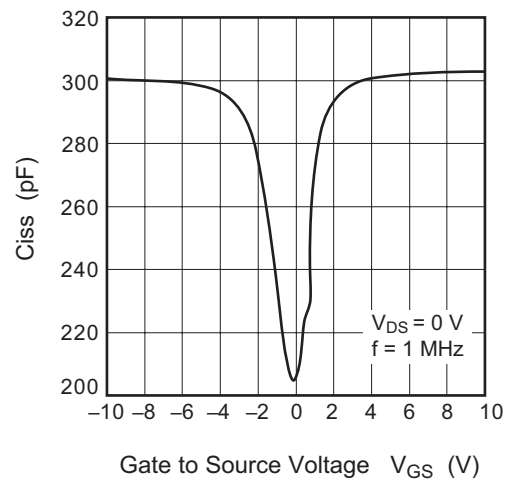
Switching Characteristics



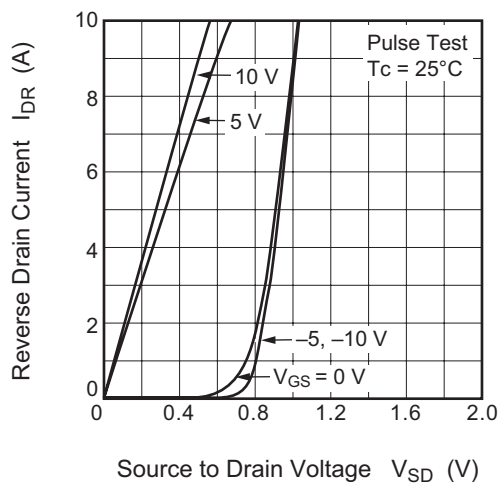
Typical Capacitance vs. Drain to Source Voltage



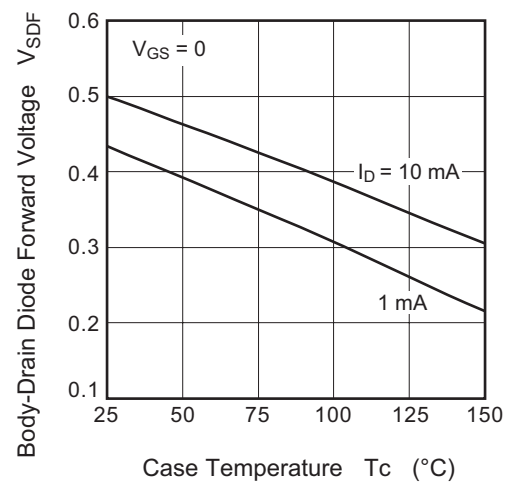
Input Capacitance vs. Gate to Source Voltage



Reverse Drain Current vs. Source to Drain Voltage



Body-Drain Diode Forward Voltage vs. Case Temperature



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450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510