Composite Transistor For high speed switching Silicon P-channel MOSFET

DESCRIPTION

RT3J55M is a composite transistor built with two INJ0011AX $\,$ chips in SC-88 package.

FEATURE

- •Input impedance is high, and not necessary to consider a drive electric current.
- •Vth is low, and drive by low voltage is possible.

Vth=-1.0~-2.0V

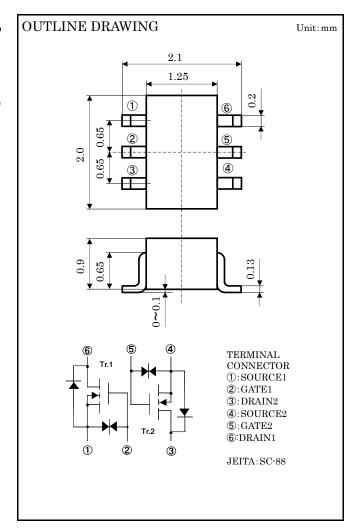
·Low on Resistance.

$$\begin{split} &R_{DS}(on) = 7.0 \,\Omega \,(TYP)@I_{_{D}} = -100 \text{mA}, \ V_{_{GS}} = -4.0 \text{V} \\ &R_{DS}(on) = 4.8 \,\Omega \,(TYP)@I_{_{D}} = -100 \text{mA}, \ V_{_{GS}} = -10 \text{V} \end{split}$$

- ·High speed switching.
- •Small package for easy mounting.

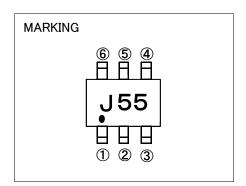
APPLICATION

High speed switching, Analog switching



MAXIMUM RATING (Ta=25°C)

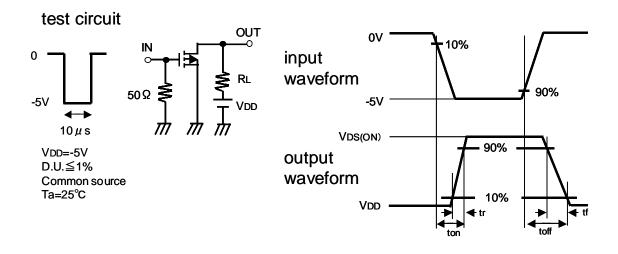
SYMBOL	PARAMETER	RATING	UNIT	
V_{DSS}	Drain-source voltage	-50	V	
VGSS	Gate-source voltage	±20	V	
ID	Drain current	-100	mA	
PD	Total power dissipation (Ta=25°C)	150	mW	
T_{ch}	Channel temperature	+150	°C	
T_{stg}	Range of Storage temperature	-55~+150	°C	



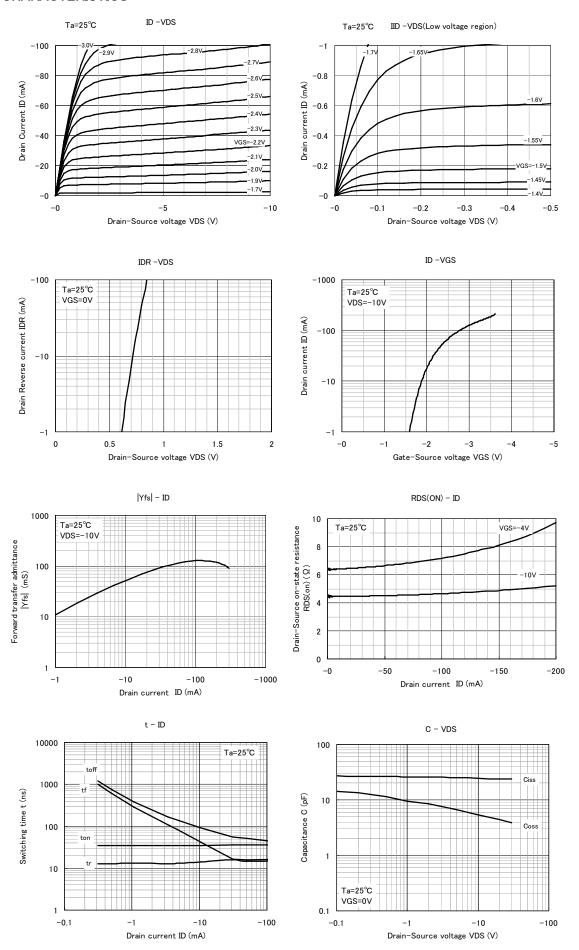
ELECTRICAL CHARACTERISTICS (Ta=25°C)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	Uillt
V(BR)DSS	Drain-source breakdown voltage	$I_D=-100 \mu A, V_{GS}=0V$	-50	-	-	٧
I GSS	Gate-source leak current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	_	±10	μΑ
I DSS	Zero gate voltage drain current	V _{DS} =-50V ,V _{GS} =0V	_	_	-1.0	μΑ
V_{th}	Gate threshold voltage	$I_D=-250 \mu A, V_{DS}=V_{GS}$	-1.0	-	-2.0	٧
Yfs	Forward transfer admittance	V _{DS} =-10V, I _D =-100mA	-	145	-	mS
RDS(on)	Static drain-source on-state resistance	I _D =-100mA, V _{GS} =-4.0V	-	7.0	-	Ω
		I _D =-100mA, V _{GS} =-10V	-	4.8	-	
Ciss	Input capacitance	- V _{DS} =-10V, V _{GS} =0V,f=1MHz	-	25	-	pF
Coss	Output capacitance		_	6.0	-	pF
ton	Citalian tima	V _{DD} =-5V , I _D =-10mA	_	35	-	
toff	Switching time	V _{GS} =0 ~ −5V	_	90	_	ns

Switching time test condition



TYPICAL CHARACTERISTICS





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