

**PRELIMINARY**

SC5104 - 64K X 4 BiCMOS ECL I/O STATIC RAM

GENERAL DESCRIPTION

Silicon Connection's SC5104 is a fully static, asynchronous random access memory, organized 65,536 words by 4 bits. The device is built using SCC's 1.0 micron BiCMOS and features advanced circuit techniques that result in 12 nS access times.

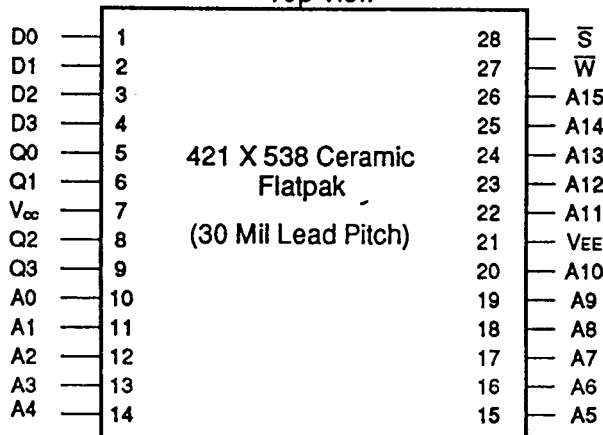
Writing and reading the memory is accomplished via industry standard timing and signals. To write the memory the device must first be selected ($\overline{S}$ pulled LOW) while enabling a write cycle ($\overline{W}$ pulled LOW). Data on the input pins (D0 - D3) will then be written into the memory address specified on the address pins (A0 - A15).

To read the memory the device is selected ($\overline{S}$ pulled LOW) while the write enable ($\overline{W}$) remains in the HIGH state. This will allow the memory contents of the current address (A0 - A15) to be presented on output pins Q0 - Q3. The output pins (Q0 - Q3) will remain LOW (inactive) if either the chip select ($\overline{S}$) is HIGH or write enable ($\overline{W}$) is LOW.

FEATURES

- 12 nS/15 nS speed grades
- Power Supply $-5.2V \pm 10\%$
- 100K compatible ECL I/O's
- Balanced read and write cycle times
- Up to 33% of write cycle timing is allowed for system skews
- Power dissipation $< 1.1W$
- Soft Error rate less than 100 FITs
- ESD protection greater than 2000 V with latch-up immunity $> 200\text{ mA}$
- High density, high performance 28-pin flatpack
- 1.0 micron BiCMOS Technology

Top View



Pin Names

A0 - A15	Address Inputs
$\overline{S}$	Chip Select
Q0 - Q3	Data Outputs
D0 - D3	Data Inputs
$\overline{W}$	Write Enable
V _{EE}	Power
V _{cc}	Ground

Absolute Maximum Ratings

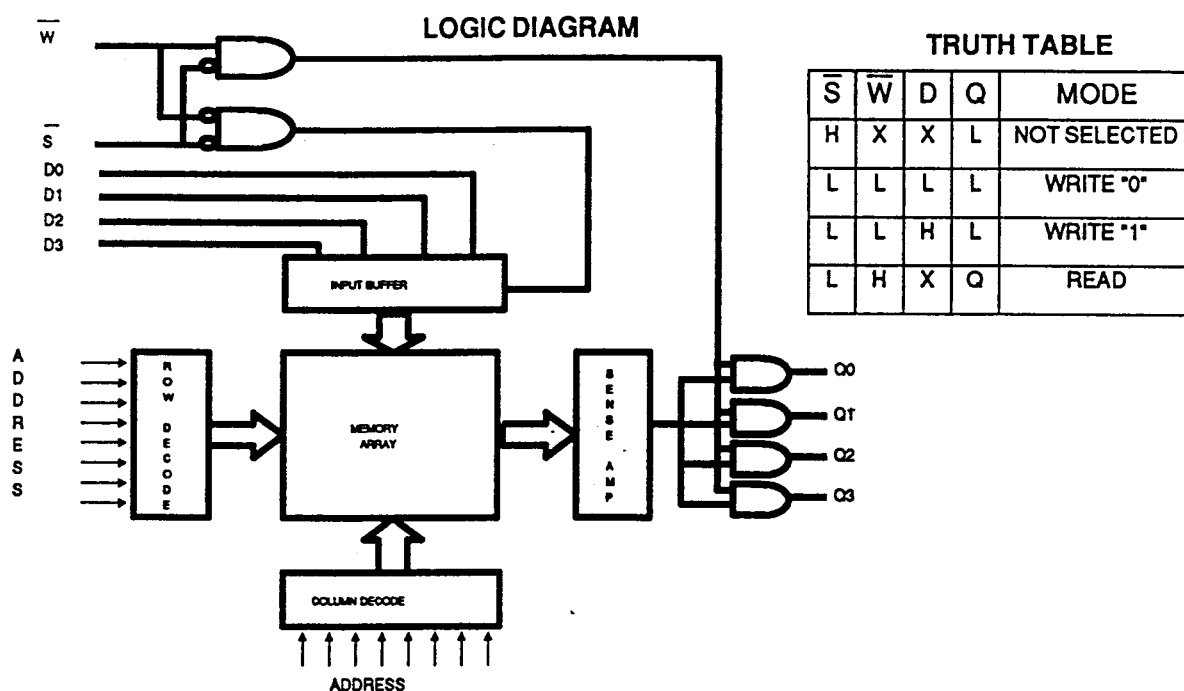
Storage Temperature -65°C to +150°C
 VEE Pin Potential to Ground -7.0V to +0.5V
 Input Voltage (DC) VEE to +0.5V
 Static Discharge Voltage >2000V
 Maximum Junction Temperature +150°C
 Output Current (DC Output High) -50 mA
 Latch-up Current >200 mA

AC Test Conditions

Input Rise and Fall Times 0.7 nS
 Output Timing Reference 50% of Input
 Input Pulse Levels Figure 1
 AC Test Circuit Figure 2

Capacitance

Input Pin (C_{IN}) 5.0 pF
 Output Pin (C_{OUT}) 8.0 pF



DC Electrical Characteristics

V_{EE} = -5.2V ± 10%, V_{CC} = Ground, T_C = 0°C to +85°C

Symbol	Parameter	Conditions	Min	Max	Units
V _{OH}	Output HIGH Voltage	V _{IN} = V _{IH} (MAX) or V _{IL} (MIN)	-1025	-880	mV
V _{OL}	Output LOW Voltage	Loading with 50 ohms to -2.0V	-1810	-1620	mV
V _{IH}	Input HIGH Voltage		-1165	-880	mV
V _{IL}	Input LOW Voltage		-1810	-1475	mV
V _{OHc}	Output HIGH Voltage	V _{IN} = V _{IH} (MIN) or V _{IL} (MAX)	-1025		mV
V _{OLc}	Output LOW Voltage	Loading with 50 ohms to -2.0V		-1620	mV
I _{IH}	Input HIGH Current	V _{IN} = V _{IH} (MAX)		220	uA
I _{IL}	Input LOW Current	V _{IN} = V _{IL} (MAX)	-50	170	uA
I _{EE}	Power Supply Current	f _o = 50 MHz	-250		mA

Read Cycle

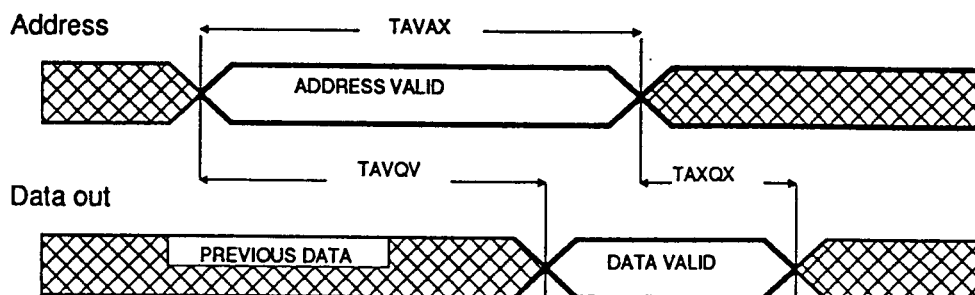
AC Timing Characteristics

 $V_{EE} = -5.2V \pm 10\%$, $V_{CC} = \text{Ground}$, $T_C = 0^\circ\text{C to } +85^\circ\text{C}$

Symbol	Parameter	SC5104-12		SC5104-15		Units
		Min	Max	Min	Max	
TAVAX	Address Valid to Address Invalid	12		15		nS
TAVQV	Address Valid to Output Valid		12		15	nS
TAXQX	Address Invalid to Output Invalid	3	8	3	10	nS
TSLSH	Chip Select LOW to Chip Select HIGH	7		7		nS
TSLQV	Chip Select LOW to Output Valid		4		4	nS
TSHQL	Chip Select HIGH to Output LOW		4		4	nS

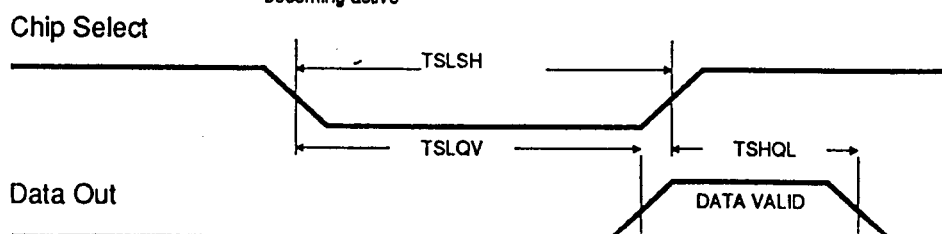
Read Cycle 1

Chip Select is active prior to or within TAVQV-TSLQV after address valid



Read Cycle 2

Address is valid a minimum of TAVQV-TSLQV prior to Chip Select becoming active



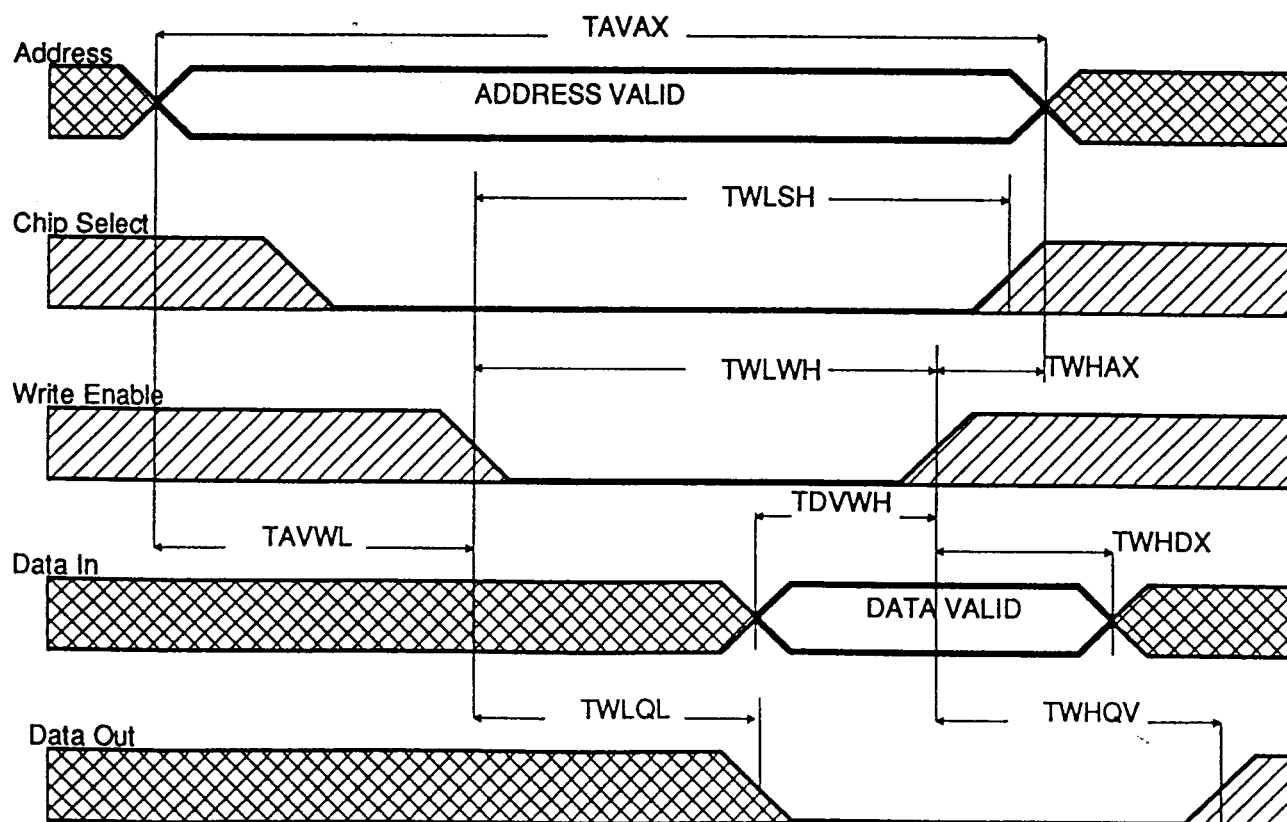
Write Cycle 1

Write Cycle 1 is $\overline{W}$ controlled. This is established by $\overline{S}$ being held active (LOW) prior to $\overline{W}$ becoming active (LOW). T_{WLQL} must be observed in Write Cycle 1 in order to avoid data bus contention in common I/O applications. At the end of Write Cycle 1 data out may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{S}$ becoming inactive (HIGH).

AC Timing Characteristics

$V_{EE} = -5.2V \pm 10\%$, $V_{CC} = \text{Ground}$, $T_c = 0^\circ\text{C to } +85^\circ\text{C}$

Symbol	Parameter	SC5104-12		SC5104-15		Units
		Min	Max	Min	Max	
TAVAX	Address Valid to Address Invalid	12		15		nS
TWLSH	Write Enable LOW to Chip Select HIGH	8		10		nS
TWHAX	Write HIGH to Address Don't Care	0		0		nS
TWLWH	Write LOW to Write HIGH	8		10		nS
TAVWL	Address Valid to Write LOW	0		0		nS
TDVWH	Data Valid to Write HIGH	8		10		nS
TWHDX	Write HIGH to Data Don't Care	0		0		nS
TWLQL	Write LOW to Output LOW		4		4	nS
TWHQV	Write HIGH to Output Valid		12		15	nS



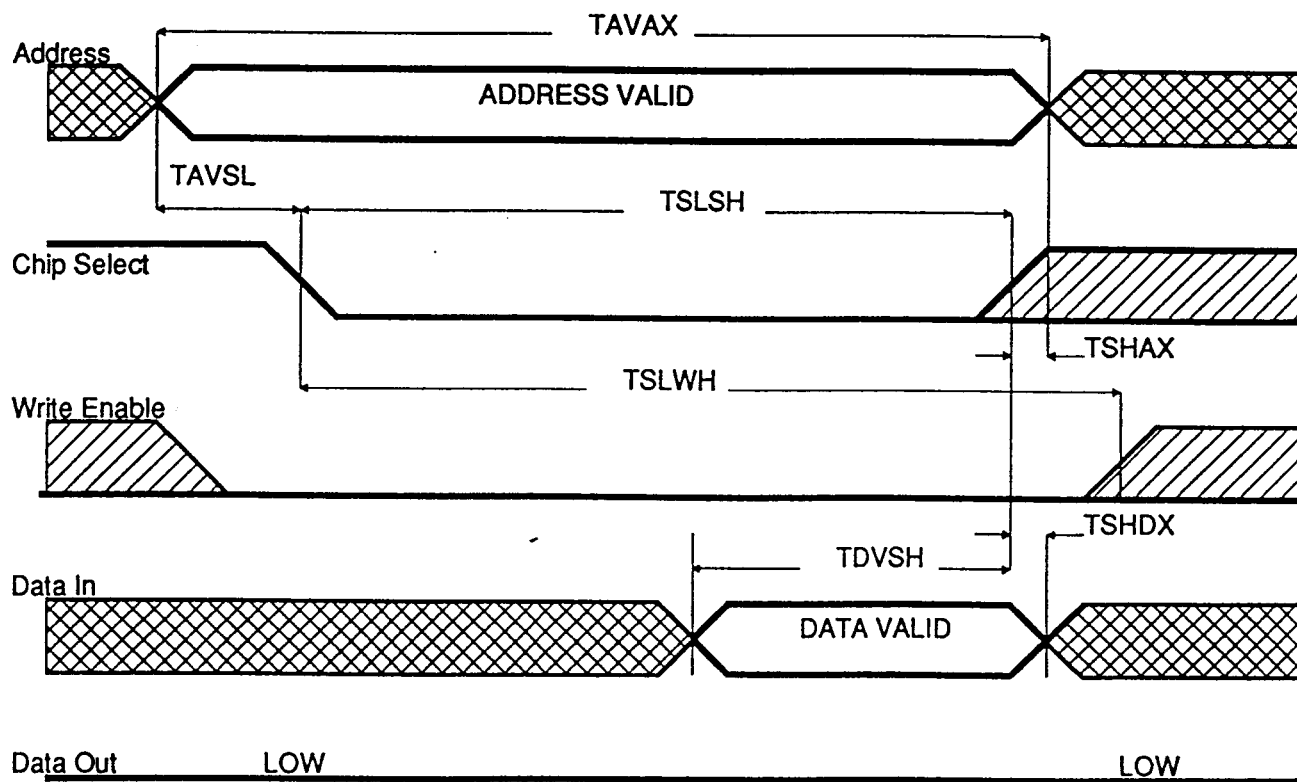
Write Cycle 2

Write Cycle 2 is $\overline{S}$ controlled. This is established by $\overline{W}$ being active coincident with or prior to $\overline{S}$ becoming active (LOW). This cycle has identical specifications to Write Cycle 1 with the exceptions of S and W being interchanged. For common I/O applications this cycle may be more appropriate, as the data bus restrictions are eliminated.

AC Timing Characteristics

$V_{EE} = -5.2V \pm 10\%$, $V_{CC} = \text{Ground}$, $T_c = 0^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	SC5104-12		SC5104-15		Units																					
		Min	Max	Min	Max																						
TAVSL	Address Valid to Chip Select LOW	0		0		nS																					
TSLSH	Chip Select LOW to Chip Select HIGH	8		10		nS																					
TSHAX	Chip Select HIGH to Address Don't Care	0		0		nS </tr <tr> <td>TSLWH</td><td>Chip Select LOW to Write Enable HIGH</td><td>8</td><td></td><td>10</td><td></td><td>nS</td></tr> <tr> <td>TDVSH</td><td>Data Valid to Chip Select HIGH</td><td>8</td><td></td><td>10</td><td></td><td>nS</td></tr> <tr> <td>TSHDX</td><td>Chip Select HIGH to Data Don't Care</td><td>0</td><td></td><td>0</td><td></td><td>nS</td></tr>	TSLWH	Chip Select LOW to Write Enable HIGH	8		10		nS	TDVSH	Data Valid to Chip Select HIGH	8		10		nS	TSHDX	Chip Select HIGH to Data Don't Care	0		0		nS
TSLWH	Chip Select LOW to Write Enable HIGH	8		10		nS																					
TDVSH	Data Valid to Chip Select HIGH	8		10		nS																					
TSHDX	Chip Select HIGH to Data Don't Care	0		0		nS																					

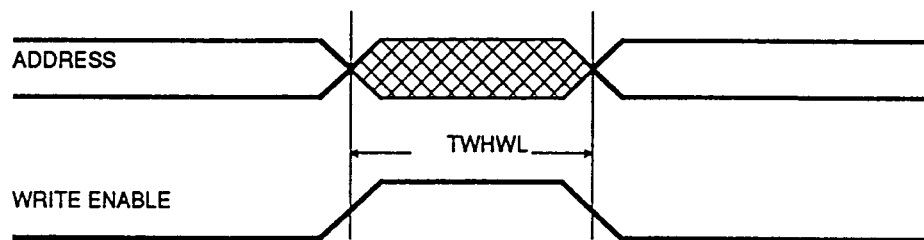


Consecutive Write Cycles AC Timing Characteristics

$V_{EE} = -5.2V \pm 10\%$, $V_{CC} = \text{Ground}$, $T_c = 0^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	SC5104-12		SC5104-15		Units
		Min	Max	Min	Max	
TWHWL	Write Enable HIGH to Write Enable LOW	4		4		nS
TSHSL	Chip Select HIGH to Chip Select LOW	4		4		nS

Minimum Write Pulse Disable



Minimum Select Pulse Disable

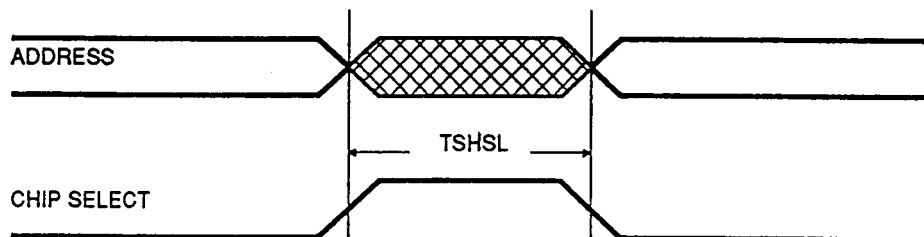
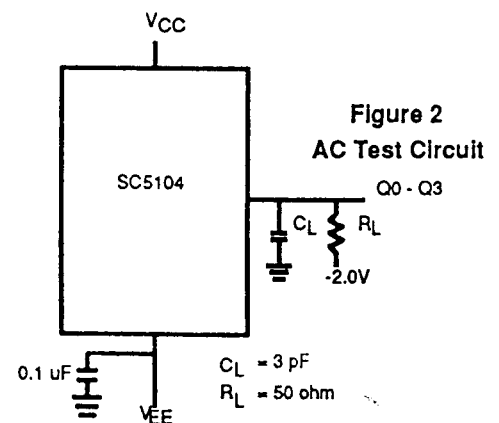
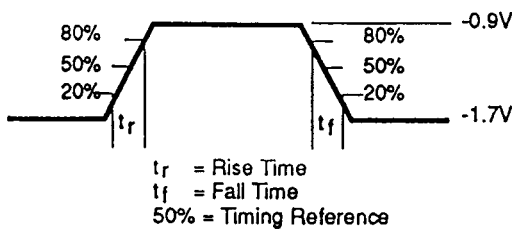
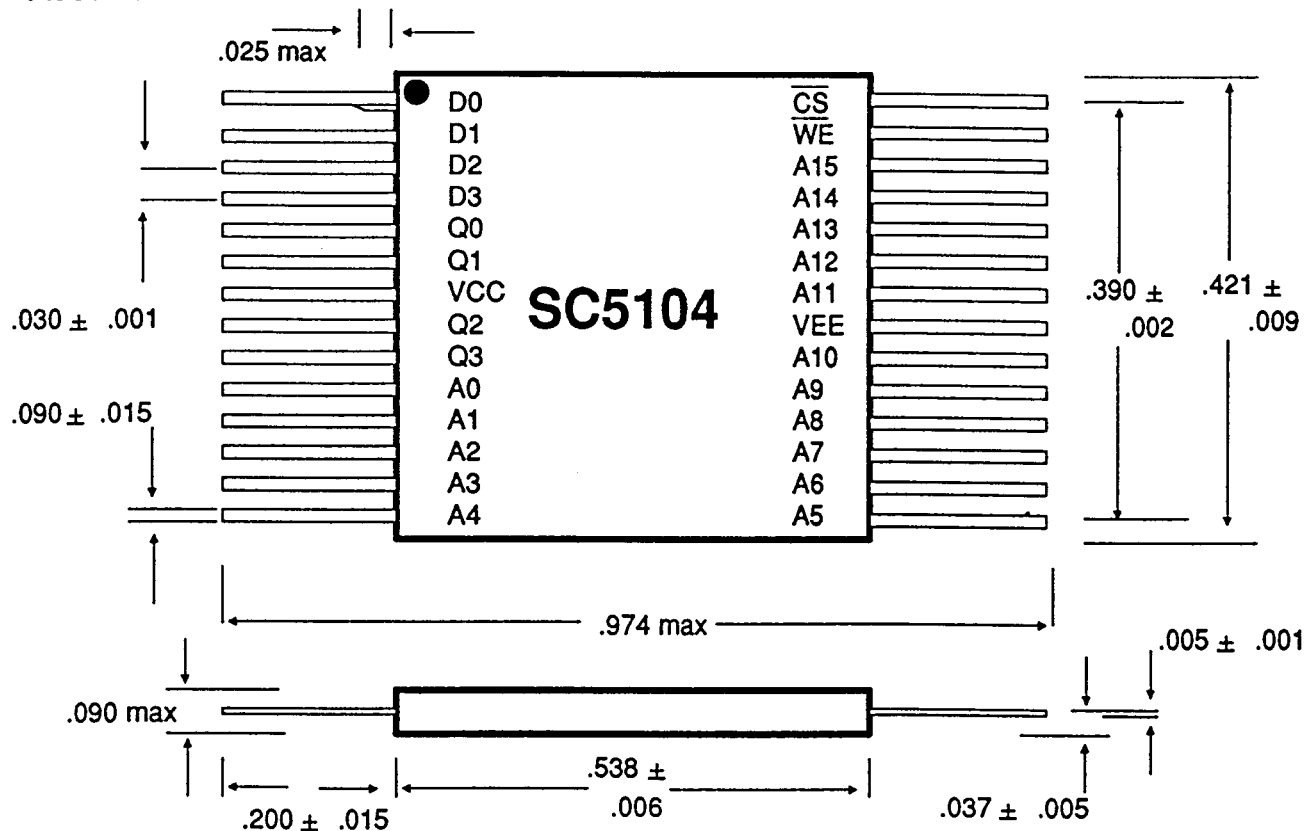


FIGURE 1



Package

Flat Pack



Ordering Codes

Package Type	Part Number
28 Pin Ceramic Flatpack	SC5104F-12/15
28 Pin Ceramic Dual-In-Line Package	SC5104D-12/15

Order Placement**Attention: Order Entry****Silicon Connections Corporation****6160 Lusk Blvd., Suite C-204****San Diego, CA 92121****Phone: 619 - 535 - 0442****FAX: 619 - 535 - 1635**