ELECTRONIC POWER METER IC WITH ELECTRICITY PROOF

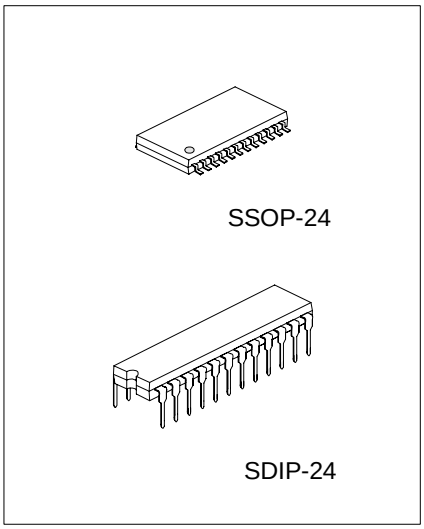
DESCRIPTION

The SC7751 is a high accuracy fault-tolerant electrical energy measurement IC that can provides superior stability and accuracy over extremes in environmental conditions and over time. The SC7751 does not exhibit any creep when there is no load.

The SC7751 supplies average real power information on the low frequency outputs F1 and F2. This logic outputs may be used to directly drive an electromecanical counter or interface to an MCU. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes, or interfacing to an MCU. The SC7751 incorporates the fault detection scheme that warns when the two input currents differ by more than 12.5%. Billing is continued using the larger of the two currents.

The SC7751 includes a power supply monitoring circuit on the AVDD supply pin. If the supply falls below 4V, the SC7751 will be reset and F1, F2 will be set to logic high, CF will be set to logic low at the same time.

The SC7751 provides synchronous frequency output for auto-reading meter system. The CF logic output is synchronous with the F1 and F2 logic output to ensure the show value of the meter is consonant with the real value.



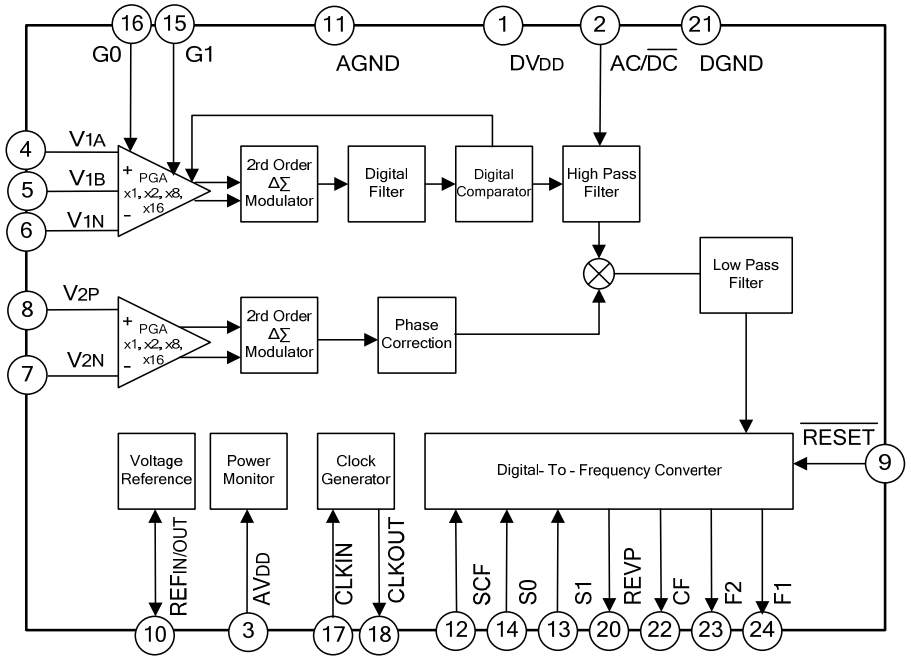
FEATURES

* Single 5V supply, low power.
* On-chip power supply monitoring.
* On-chip reference with external overdrive capability.
* Supplies average real power on the frequency outputs F1 and F2, which can drive for electromechanical counters directly.
* The high frequency output CF is intended for calibration and supplies instantaneous real power.
* Fault is indicated when the currents differ by more than 12.5%.
* Less than 0.1% error over a dynamic range of 500 to 1.
* On-chip creep protection (No load threshold).
*The logic output REVP can be used to indicate a potential miswiring or negative power.
* A PGA in the current channel make flexible to select the shunt and burden resistance.

ORDERING INFORMATION

Device	Package
SC7751S	SSOP-24-300-0.65
SC7751	SDIP-24-300-2.54

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Tamb=25°C, unless otherwise specified)

Characteristics	Symbol	Value	Unit
AVDD to AGND	AVDD	-0.3 ~ +7	V
DVDD to DGND	DVDD	-0.3 ~ +7	V
Analog Input Voltage to AGND V1P, V1N, V2P and V2N	AVIN	-6 ~ +6	V
Reference Input voltage to AGND	VREF	-0.3 ~ AVDD+0.3	V
Digital Input Voltage to DGND	DVIN	-0.3 ~ DVDD+0.3	V
Digital Output Voltage to DGND	DVOUT	-0.3 ~ DVDD+0.3	V
Power Dissipation	PD	450	mW
Operating Temperature Range Industrial (A, B version)	TOPR	-40~ +85	°C
Storage Temperature	TSTG	-65~ +150	°C
Junction Temperature	TJ	+150	°C

ELECTRICAL CHARACTERISTICS (Tamb=25°C, unless otherwise specified)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Power Supply						
Analog Power Supply	AVDD	5V±5%	4.75	--	5.25	V
Digital Power Supply	DVDD	5V±5%	4.75	--	5.25	
Analog Input Current	AIDD	(2mA) TYP.	--	--	3	mA
Digital Input Current	DIDD	(1.5mA) TYP.	--	--	2.5	

(To be continued)

(Continued)

Characteristics		Symbol	Test conditions	Min.	Typ.	Max.	Unit
ACCURACY							
Measurement Error on Channel 1	Gain=1	EM	Over a dynamic range 500 to 1	--	0.1	--	%
	Gain=2		Over a dynamic range 500 to 1	--	0.1	--	%
	Gain=8		Over a dynamic range 500 to 1	--	0.1	--	%
	Gain=16		Over a dynamic range 500 to 1	--	0.1	--	%
Phase Error between Channels	V1 Phase Lead 37°	EP	AC/$\overline{DC}$=0 and AC/$\overline{DC}$=1	--	--	±0.1	°
	V1 Phase Lag 60°			--	--	±0.1	°
Output Frequency Rejection (AC)		CFA	V1=100mV, V2=100mV, AC/$\overline{DC}$=1 S0=S1=1 G0=G1=0	--	0.01	--	%
Output Frequency Rejection (DC)		CFD	V1=100mV, V2=100mV, V_{DD}=DV_{DD}=5V±250mV	--	0.01	--	%
The MIN. frequency of output (F1, F2)		Fmin	--			0.014% *Fbase	Hz
FAULT DETECTION							
Fault detection threshold, Inactive i/p < active i/p			(V1A or V1B active)		12.5		%
Input swap threshold Inactive i/p > active i/p			(V1A or V1B active)		14		%
Accuracy fault mode operation	V1A active, V1B=AGND		Over a dynamic range 500 to 1		0.1		%
	V1B active, V1A=AGND		Over a dynamic range 500 to 1		0.1		%
Fault detection delay					3		s
Swap delay					3		s
ANALOG INPUTS							
Maximum Signal Levels		LEVS	V1P, VIN V2N and V2P to AGND	--	--	±1	V
Input Impedance (DC)		IMIN	CLKIN=3.58MHz	400	--	--	kΩ
Bandwidth (-3dB)		BW	CLKIN/256, CLKIN=3.58MHz	--	14	--	kHz
ADC Offset Error		EADC		--	--	15	mV
Gain Error		EG	V1=660mV, V2=660mV	--	±4	--	%
Gain Error Match		EGM	External 2.5V reference	--	±0.2	--	%
REFERENCE INPUT							
REFIN/OUT Input Voltage Range		VINR	2.5V±8%	2.3	--	2.7	V
Input Impedance		IMIN	--	3.7	--	--	kΩ
Input Capacitance		CIN	--	--	--	10	pF
ON-CHIP REFERENCE							
Reference Error		ER	Nominal 2.5V	--	--	200	mV
Temperature Coefficient		TC		--	30	60	ppm/°C
CLKIN							
Input Clock Frequency		CLKIN	Note all specifications for CLKIN of 3.58MHz	1	--	4	MHz

(To be continued)

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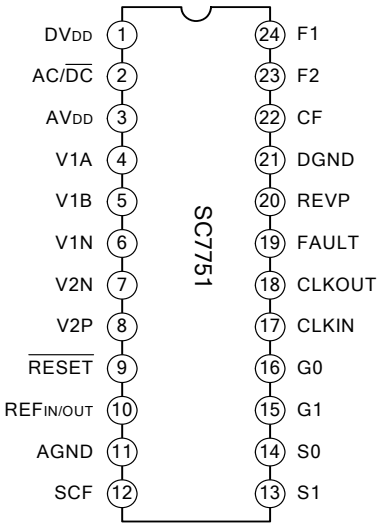
Characteristics		Symbol	Test conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS							
Input High Voltage		V_{INH}	DV_{DD}=5V±5%	2.4	--	--	V
Input Low Voltage		V_{INL}	DV_{DD}=5V±5%	--	--	0.8	V
Input Current		I_{IN}	Typically 10nA, V_{IN}=0V to DV_{DD}	--	--	±3	μA
Input Capacitance		C_{IN}		--	--	10	pF
LOGIC OUTPUTS							
F1 and F2	Output High Voltage	V_{OH}	I_{SOURCE}=10mA DV_{DD}=5V	4.5	--	--	V
	Output Low Voltage	V_{OL}	I_{SINK}=10mA DV_{DD}=5V	--	--	0.5	V
CF and REVP and FAULT	Output High Voltage	V_{OH}	I_{SOURCE}=5mA DV_{DD}=5V	4	--	--	V
	Output Low Voltage	V_{OL}	I_{SINK}=5mA DVDD=5V	--	--	0.5	V

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN No.	Symbol	Description
1	DV_{DD}	Digital Power Supply.
2	AC/$\overline{DC}$	High Pass Filter Select. The pin should be high in power metering applications.
3	AVDD	Analog Power Supply.
4	V1A	Positive Inputs for Channel 1 (Current Channel). Channel 1 has a PGA and the gain selections are outlined in Table I. The maximum differential input voltage is ±660mV with respect to Pin V1N. The maximum signal level at these pins is ±1V with respect to AGND.
5	V1B	
6	V1N	Negative Inputs for Channel 1 (Current Channel). The maximum signal level at these pins is ±1V with respect to AGND.

(To be continued)

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PIN No.	Symbol	Description
7	V2N	Negative and Positive Inputs for Channel 2 (Voltage Channel). The maximum differential input voltage is ±660mV for specified operation. The maximum signal level at these pins is ±1V with respect to AGND.
8	V2P	
9	$\overline{\text{RESET}}$	Reset Pin for the SC7751. A logic low is valid;
10	REFIN/OUT	Reference voltage input/output pin.
11	AGND	Analog ground.
12	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table III shows how the calibration frequencies are selected.
13	S1	Select one of four possible frequencies for the digital-to-frequency conversion. See Table II and Table III
14	S0	
15	G1	Select gains for Channel 1, See Table I
16	G0	
17	CLKIN	3.58MHZ crystal oscillator input pin
18	CLKOUT	3.58MHZ crystal oscillator output pin
19	FAULT	State indication pin. When the signals on V1A and V1B differ by more than 12.5%, it will be set to logic high.
20	REVP	State indication pin. While negative power or a potential miswriting occurs, it will be set to logic high.
21	DGND	Digital ground.
22	CF	Calibration Frequency Logic Output..
23	F2	Low Frequency Logic Outputs. They can be used to directly drive a stepper motor or electromechanical impulse counter
24	F1	

TIMIING CHARACTERISTICS[1,2]

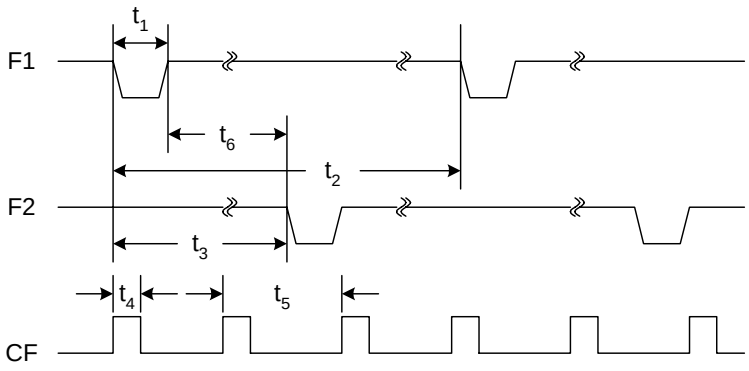
(AV_{DD}=DV_{DD}=5V±5%, AGND=DGND=0V, On-chip Reference, CLK_{IN}=3.58MHZ, T_{MIN} to T_{MAX}=-40°C~+85°C.)

Parameter	Test Condition	Test Data	Units
t1[3]	F1 and F2 Pulse-width	275	ms
t2	F1 and F2 Pulse Period.	See Table II	sec
t3	Time Between F1 Falling Edge and F2 Falling Edge	1/2 t2	sec
t4[3]	CF Pulse-width	90	ms
t5	CF Pulse Period.	See Table III	sec
t6	Minimum Time Between F1 and F2 Pulse	CLKIN/4	sec

NOTE: 1. Sample tested during initial release and after any redesign or process change that may after this parameter.

2. See the following figure.

3. The pulse-widths of F1, F2 and CF are not fixed for higher output frequencies.



Timing Diagram for Frequency outputs

Timing Diagram for Frequency Outputs shows a timing diagram for the various frequency outputs of the SC7751. The low frequency outputs, F1 and F2 can drive electromechanical counters and two phase stepper motors directly. As the figure show, the F1 and F2 outputs provide two alternating low going pulses. The pulse width (t1) is set at 275ms and the time between the falling edges of F1 and F2 (t3) is approximately half the period of F1 (t2). If however the period of F1 and F2 falls below 550 ms (1.81Hz) the pulse width of F1 and F2 is set to half of their period. The frequency of F1 and F2 corresponds to the input voltages, and F=（8.06*V1*V2*G*F_{base}）/ $VREF^2$， The values of G and F_{base} can be set by consumers, and the selection of G and F_{base} please refer to the table I and table III , V1 and V2 are the rms value of the two inputs, VREF is the voltage of reference, whose value is 2.5±0.2v when the internal bandgap reference of SCE7755 is valid. The maximum output frequencies for F1 and F2 are shown in Table II.

The high frequency output, CF is intended for calibration and supplies instantaneous real power. CF produces a 90ms wide active high pulse (t4) at a frequency proportional to active power. The CF output frequencies are given in Table III. As in the case of F1 and F2, if the period of CF (t5) falls below 180ms, the CF pulse-width is set to half the period.

Table I. gain selection for channel 1

G1	G0	G	Maximum Differential Signal
0	0	1	±660mV
0	1	2	±330mV
1	0	8	±82mV
1	1	16	±41mV

Table II. Maximum output frequency on F1 and F2

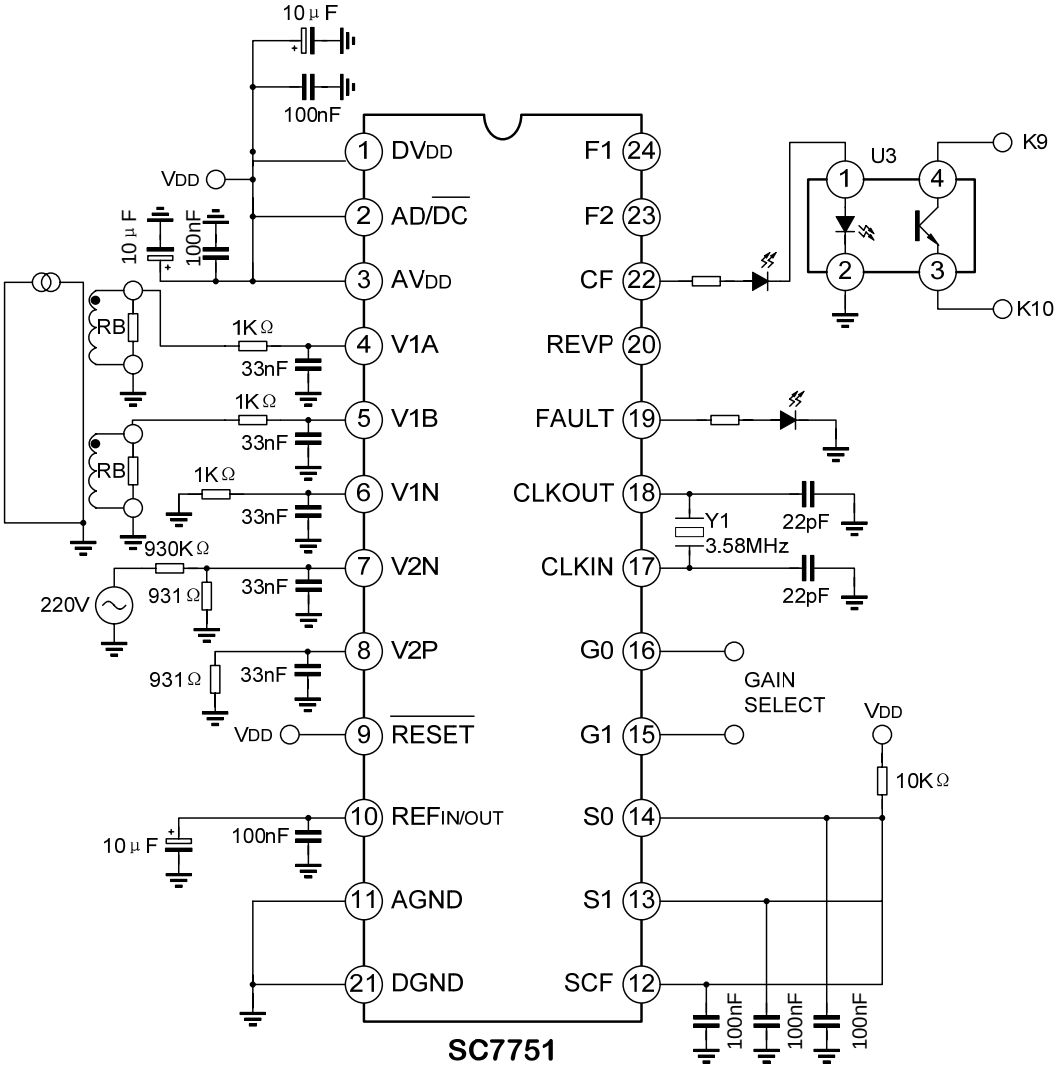
S1	S2	Max Frequency for DC Inputs (Hz)	Max Frequency for AC Inputs (Hz)
0	0	0.68	0.34
0	1	1.36	0.68
1	0	2.72	1.36
1	1	5.44	2.72

Table III. Maximum output frequency on CF

SCF	S1	S0	Fbase(Hz)	XTAL/CLKIN*	CF Max for AC signals (Hz)
1	0	0	1.7	3.579MHz/2^{21}	128×F1, F2
0	0	0	1.7	3.579MHz/2^{21}	64×F1, F2
1	0	1	3.4	3.579MHz/2^{20}	64×F1, F2
0	0	1	3.4	3.579MHz/2^{20}	32×F1, F2
1	1	0	6.8	3.579MHz/2^{19}	32×F1, F2
0	1	0	6.8	3.579MHz/2^{19}	16×F1, F2
1	1	1	13.6	3.579MHz/2^{18}	16×F1, F2
0	1	1	13.6	3.579MHz/2^{18}	8×F1, F2

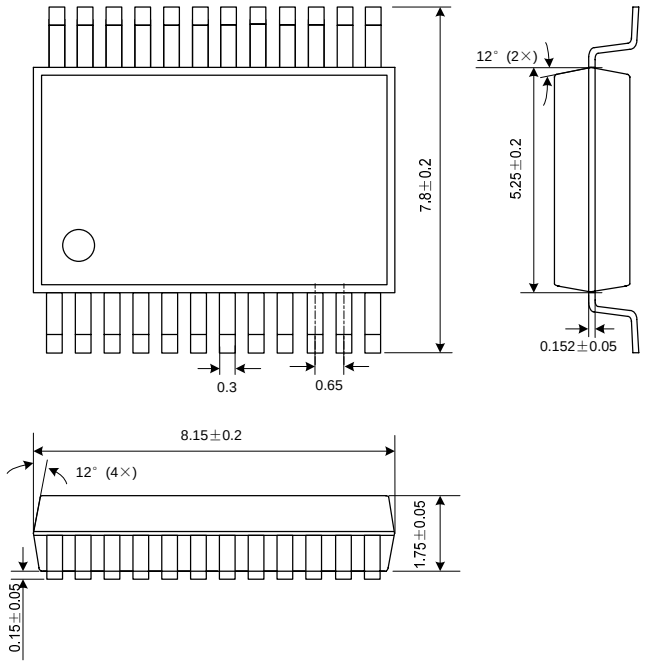
NOTE: *Fbase is a binary fraction of the master clock and therefore will vary if the specified CLKIN frequency is altered.

TYPICAL APPLICATION CIRCUIT

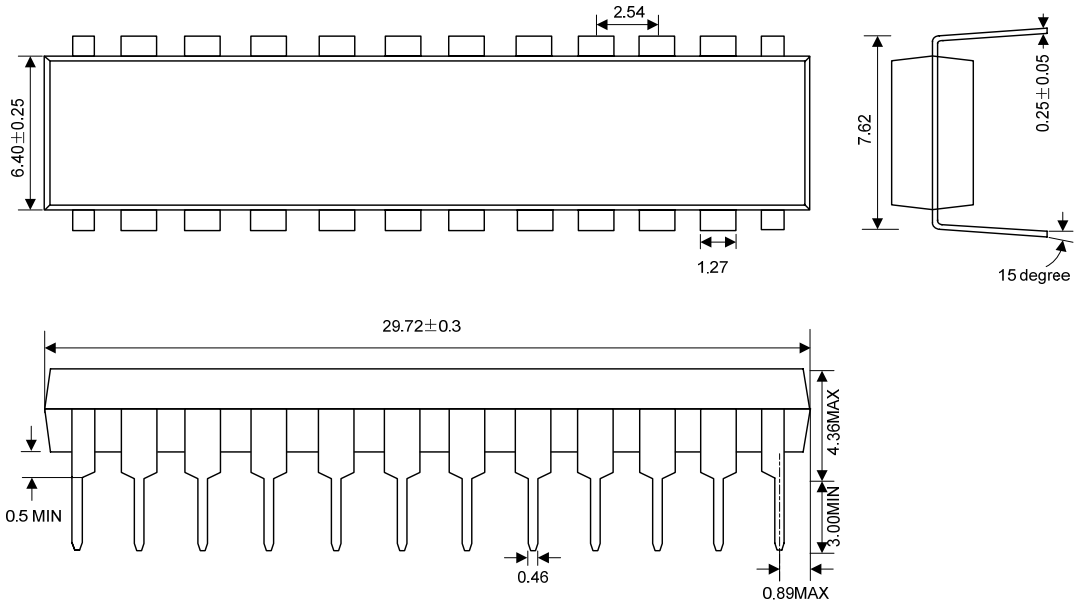


PACKAGE OUTLINE

SSOP-24-300-0.65 UNIT: mm



SDIP-24-300-2.54 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

Note：Silan reserves the right to make changes without notice in this specification for the improvement of the design and performance. Silan will supply the best possible product for customers.