

REMOTE CONTROL TRANSMITTER OF 9012 CODE FORMAT

DESCRIPTION

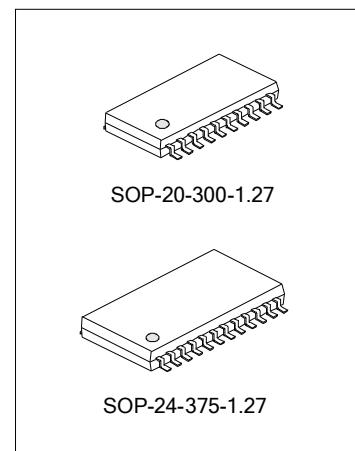
SC9244 is an infrared remote control transmitter utilizing CMOS Technology specially designed for infrared remote control system. It provides 16 selectable system code, and 14 selectable data code. The circuit has SOP20 and SOP24 two kind of package. The pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantage.

FEATURES

- * CMOS Technology
- * Low Power Consumption (<1μA)
- * System code and data code selectable
- * Internal 38KHz carrier, used for infrared transmitting

APPLICATIONS

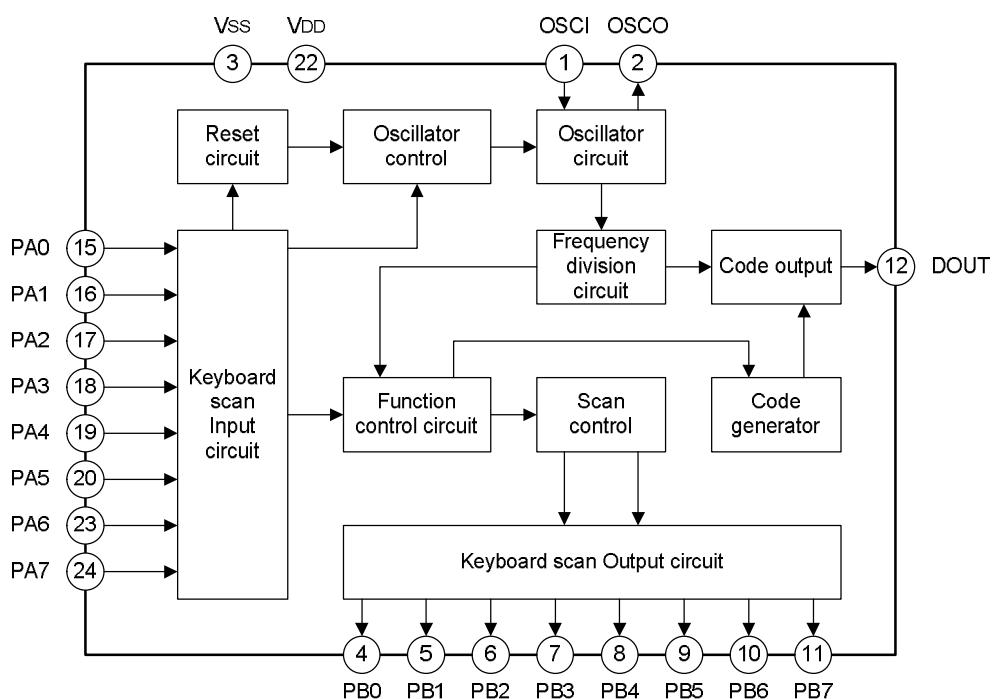
- * Infrared transmitting remote controller
- * TV remote controller
- * Video Recorder remote controller
- * VCD audio remote controller



ORDERING INFORMATION

Device	Package
SC9244	SOP-20-300-1.27
SC9244A	SOP-24-375-1.27

BLOCK DIAGRAM



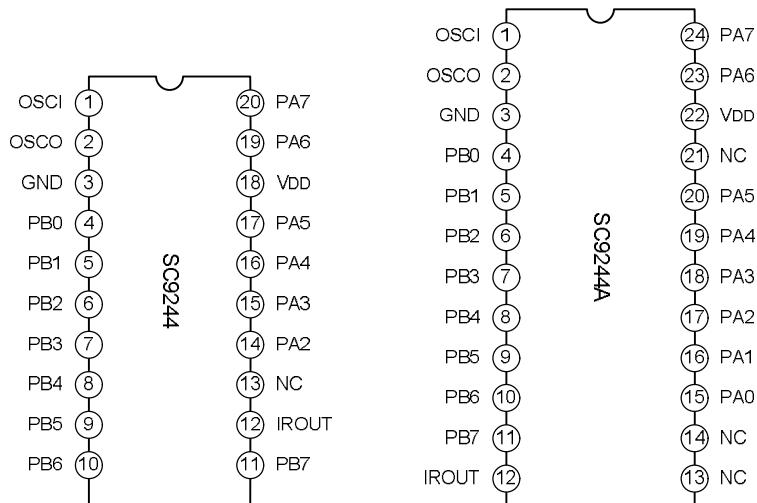
ABSOLUTE MAXIMUM RATING

Characteristics	Symbol	Ratings			Unit
Operating Voltage	VDD	-0.3~7.0			V
Input Voltage	VIN	VSS-0.3~VDD+0.3			V
Operating Temperature	Tamb	-40~85			°C
Storage Temperature	Tstg	-65~150			°C

DC ELECTRICAL CHARACTERISTICS (VDD=3.0V±10%, VSS=0)

Characteristics	Symbol	Test conditions		Min.	Typ.	Max.	Unit
		Pin	Conditions				
High Level Output Voltage	V _{OH}	PA7~PA0 PB7~PB0 I _{ROUT}	I _{load} =-0.8mA	VDD-0.5	-	-	V
Low Level Output Voltage	V _{OL}	PA7~PA0 PB7~PB0 I _{ROUT}	I _{load} =0.8mA	-	0.1	0.5	V
High Level Output Driving Current	I _{OH}	PA7~PA0 PB7~PB0 I _{ROUT}	V _{OH} =2V	2	3	-	mA
Low Level Output Driving Current	I _{OL}	PA7~PA0 PB7~PB0 I _{ROUT}	V _{OL} =1V	3	5	-	mA
High Level Input Voltage	V _{IH}	PA7~PA0 PB7~PB0		0.7VDD		VDD	V
Low Level Input Voltage	V _{IL}	PA7~PA0 PB7~PB0		0		0.2VDD	V
Dynamic Power Dissipation	I _{ddd}	VDD	Main oscillator 455KHz		0.5	1	mA
Quiescent Power Dissipation	I _{dds}	VDD	Oscillator stops		0.2	1	μA
Pull-up Resistor	R _{up}	PA7~PA0		150		200	KΩ

PIN CONFIGURATION



PIN DESCRIPTIONS

Pin no.		Pin name	I/O	Functions
SOP24	SOP20			
1	1	OSCI	I	Oscillator input pin
2	2	OSCO	O	Oscillator output pin
3	3	GND	--	Ground
4~11	4~11	PB0~PB7	O	Key scan signal output pin
12	12	IROUT	O	Infrared transmitting output pin
15~16	--	PA0~PA1	I	Key scan signal input pin, when in SOP20 package, do not have these two pins
17~20	14~17	PA2~PA5	I	Key scan signal input pin
22	18	VDD	--	Positive power supply
23~24	19~20	PA6~PA7	I	Key scan signal input pin

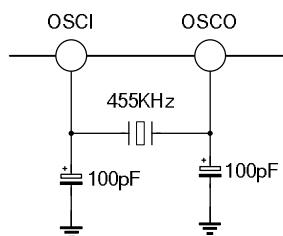
FUNCTION DESCRIPTIONS

1. OSCILLATOR CIRCUIT

There is a ceramic oscillator between OSCI and OSCO, and a 100pF capacitor whose capacitance is 455KHz between two oscillator pins and GND. To reduce the power dissipation, the oscillator circuit will work when press the key, or else it stops. It can generate 38KHz carrier by internal frequency division.

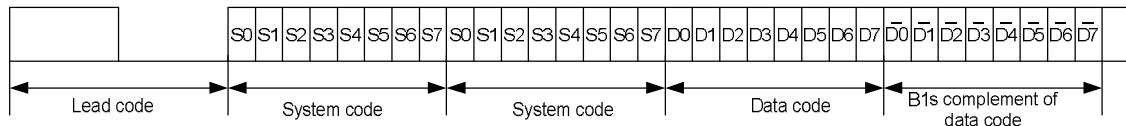
$$FIR=455\text{KHz}/12=37.92\text{KHz}$$

Duty=1/3



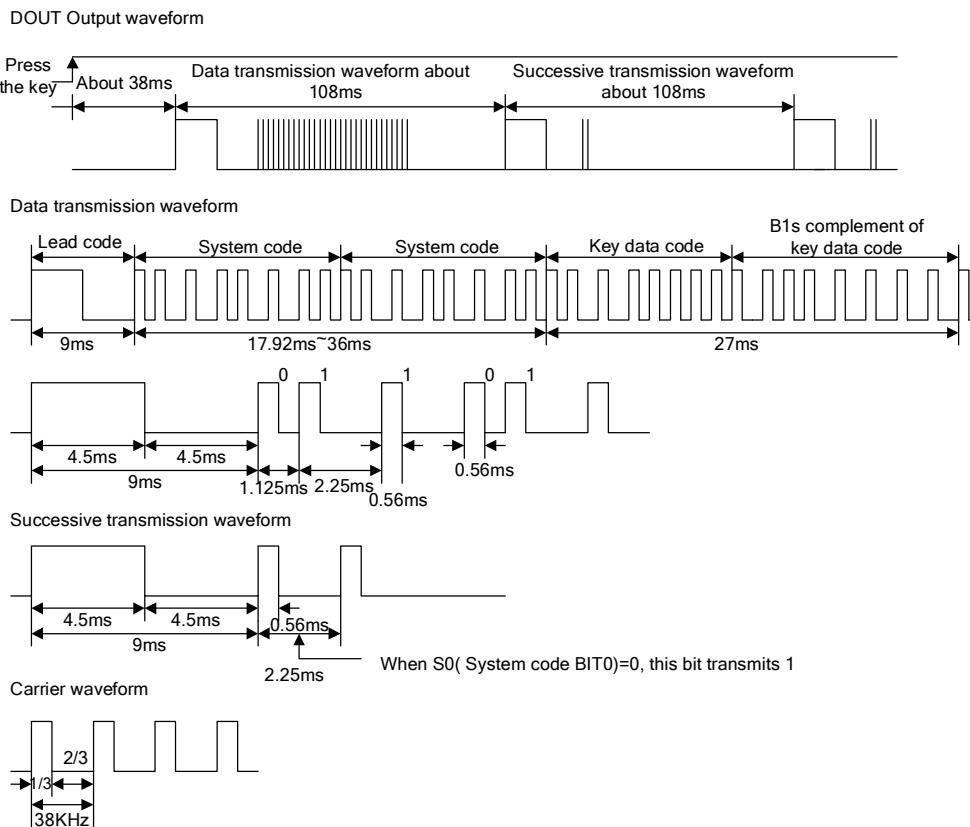
2. CODE TRANSMISSION

The transmitting code includes a lead code, 16-bit system code, 8-bit data code and 8-bit b1s complement of data code.



The lead code is composed of 4.5ms high level and 4.5ms low level, thus 9ms in total, and it is used as the leader for the following codes. Thus, when reception is configured by a microcomputer, it will time the various operations such as decoding. The code uses the PPM (Pulse Phase Modulation) Method, with "0" and "1" differentiated by the time between pulses.

3. REMOTE OUTPUT WAVEFORM



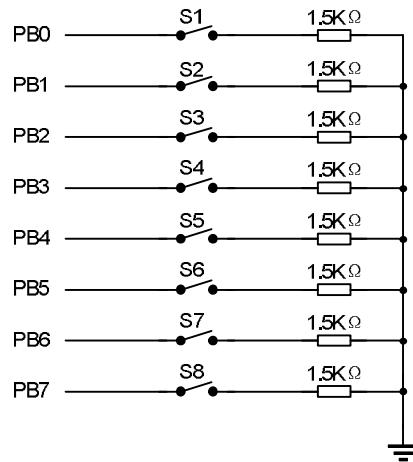
When oscillation frequency is 455 KHz, the output signal is modulated by 38 KHz of duty 1/3 (which is 1/12 of the carrier generation circuit).

Note: In designing the firmware of the receiving and decoding circuit, please strictly follow the following instructions:

- 1) System Codes: The same code is transmitted twice and therefore, and then decodes system codes for two times and check if they are in agreement with each other.
- 2) Key Data Codes: The Key Data Code and its inverted code are always transmitted together, therefore, check if they are in agreement with each other.

4. ACHIEVEMENT SELECTION CIRCUIT

As the following picture, S1, S2, S3, and S4 are the selection bits of system code; S5, S6, S7, and S8 are selecting bits of data code.



5. SYSTEM CODE TABLE

Priority	S4	S3	S2	S1	System code
1	0	0	0	0	0EH
2	0	0	0	1	1EH
3	0	0	1	0	2EH
4	0	1	0	0	3EH
5	1	0	0	0	17H
6	0	0	1	1	18H
7	0	1	0	1	19H
8	0	1	1	0	1AH
9	1	0	0	1	1BH
10	1	0	1	0	1CH
11	1	1	0	0	1DH
12	0	1	1	1	1FH
13	1	0	1	1	20H
14	1	1	0	1	21H
15	1	1	1	0	22H
16	1	1	1	1	23H

Note: Si=1 denotes press the key, Si=0 denotes open.

6. DATA CODE TABLE

No.	Keyboard	DATA CODE(Next row shows the value of S8~S5)													
		00	01	02	04	08	03	05	06	09	0A	0C	07	0B	0D
K1	PA7	PB0									00				
K2		PB1									01				
K3		PB2									02				
K4		PB3									03				
K5		PB4									04				
K6		PB5									05				
K7		PB6									06				
K8		PB7									07				
K9	PA6	PB0									08				
K10		PB1									09				
K11		PB2									0A				
K12		PB3									0B				
K13		PB4									0C				
K14		PB5									0D				
K15		PB6									0E				
K16		PB7									0F				
K17	PA5	PB0									10				
K18		PB1									11				
K19		PB2									12				
K20		PB3									13				
K21		PB4									14				
K22		PB5									15				
K23		PB6									16				
K24		PB7									17				
K25	PA4	PB0									18				
K26		PB1									19				
K27		PB2									1A				
K28		PB3									1B				
K29		PB4									1C				
K30		PB5									1D				
K31		PB6									1E				
K32		PB7									1F				

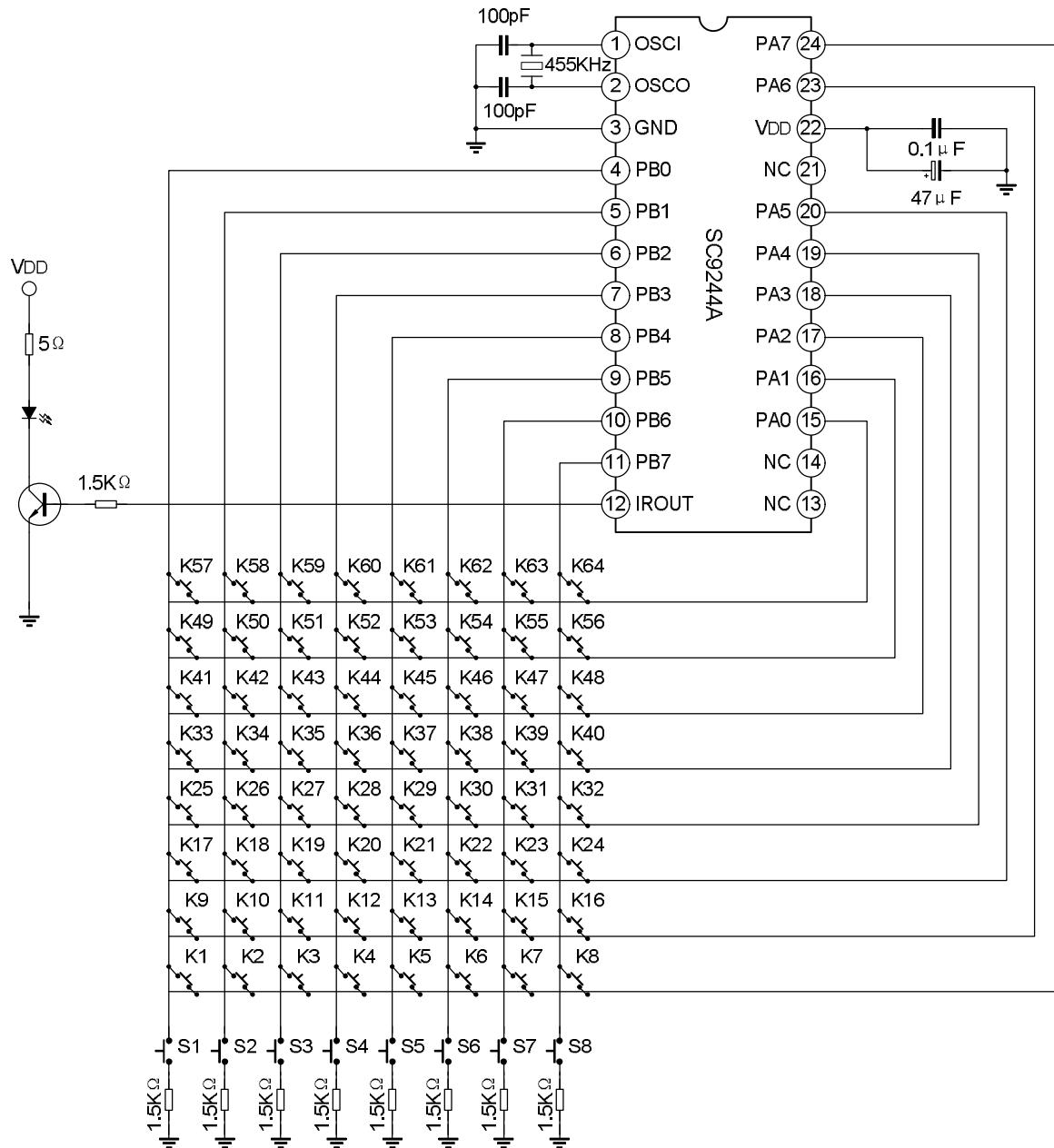
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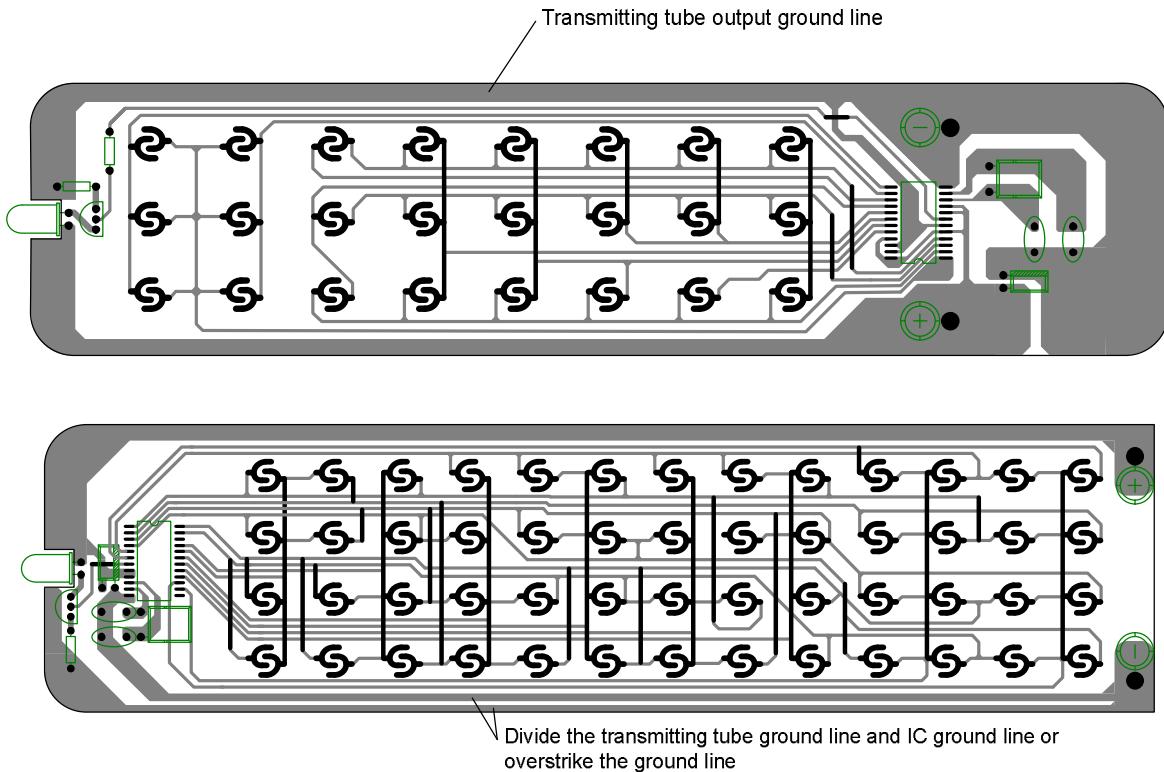
No.	Keyboard	DATA CODE(Next row shows the value of S8~S5)														
		00	01	02	04	08	03	05	06	09	0A	0C	07	0B	0D	
K33	PA3	PB0	40	20	30	50	60	70	80	90	A0	B0	C0	D0	E0	F0
K34		PB1	41	21	31	51	61	71	81	91	A1	B1	C1	D1	E1	F1
K35		PB2	42	22	32	52	62	72	82	92	A2	B2	C2	D2	E2	F2
K36		PB3	43	23	33	53	63	73	83	93	A3	B3	C3	D3	E3	F3
K37		PB4	44	24	34	54	64	74	84	94	A4	B4	C4	D4	E4	F4
K38		PB5	45	25	35	55	65	75	85	95	A5	B5	C5	D5	E5	F5
K39		PB6	46	26	36	56	66	76	86	96	A6	B6	C6	D6	E6	F6
K40		PB7	47	27	37	57	67	77	87	97	A7	B7	C7	D7	E7	F7
K41	PA2	PB0	48	28	38	58	68	78	88	98	A8	B8	C8	D8	E8	F8
K42		PB1	49	29	39	59	69	79	89	99	A9	B9	C9	D9	E9	F9
K43		PB2	4A	2A	3A	5A	6A	7A	8A	9A	AA	BA	CA	DA	EA	FA
K44		PB3	4B	2B	3B	5B	6B	7B	8B	9B	AB	BB	CB	DB	EB	FB
K45		PB4	4C	2C	3C	5C	6C	7C	8C	9C	AC	BC	CC	DC	EC	FC
K46		PB5	4D	2D	3D	5D	6D	7D	8D	9D	AD	BD	CD	DD	ED	FD
K47		PB6	4E	2E	3E	5E	6E	7E	8E	9E	AE	BE	CE	DE	EE	FE
K48		PB7	4F	2F	3F	5F	6F	7F	8F	9F	AF	BF	CF	DF	EF	FF
K49	PA1	PB0	50	30	40	60	70	80	90	A0	B0	C0	D0	E0	F0	00
K50		PB1	51	31	41	61	71	81	91	A1	B1	C1	D1	E1	F1	01
K51		PB2	52	32	42	62	72	82	92	A2	B2	C2	D2	E2	F2	02
K52		PB3	53	33	43	63	73	83	93	A3	B3	C3	D3	E3	F3	03
K53		PB4	54	34	44	64	74	84	94	A4	B4	C4	D4	E4	F4	04
K54		PB5	55	35	45	65	75	85	95	A5	B5	C5	D5	E5	F5	05
K55		PB6	56	36	46	66	76	86	96	A6	B6	C6	D6	E6	F6	06
K56		PB7	57	37	47	67	77	87	97	A7	B7	C7	D7	E7	F7	07
K57	PA0	PB0	58	38	48	68	78	88	98	A8	B8	C8	D8	E8	F8	08
K58		PB1	59	39	49	69	79	89	99	A9	B9	C9	D9	E9	F9	09
K59		PB2	5A	3A	4A	6A	7A	8A	9A	AA	BA	CA	DA	EA	FA	0A
K60		PB3	5B	3B	4B	6B	7B	8B	9B	AB	BB	CB	DB	EB	FB	0B
K61		PB4	5C	3C	4C	6C	7C	8C	9C	AC	BC	CC	DC	EC	FC	0C
K62		PB5	5D	3D	4D	6D	7D	8D	9D	AD	BD	CD	DD	ED	FD	0D
K63		PB6	5E	3E	4E	6E	7E	8E	9E	AE	BE	CE	DE	EE	FE	0E
K64		PB7	5F	3F	4F	6F	7F	8F	9F	AF	BF	CF	DF	EF	FF	0F

Note: Si=1 denotes press the key, Si=0 denotes open. The data in the table is all in hex.

TYPICAL APPLICATION CIRCUIT



PCB WIRE LAYOUT SCHEMATIC

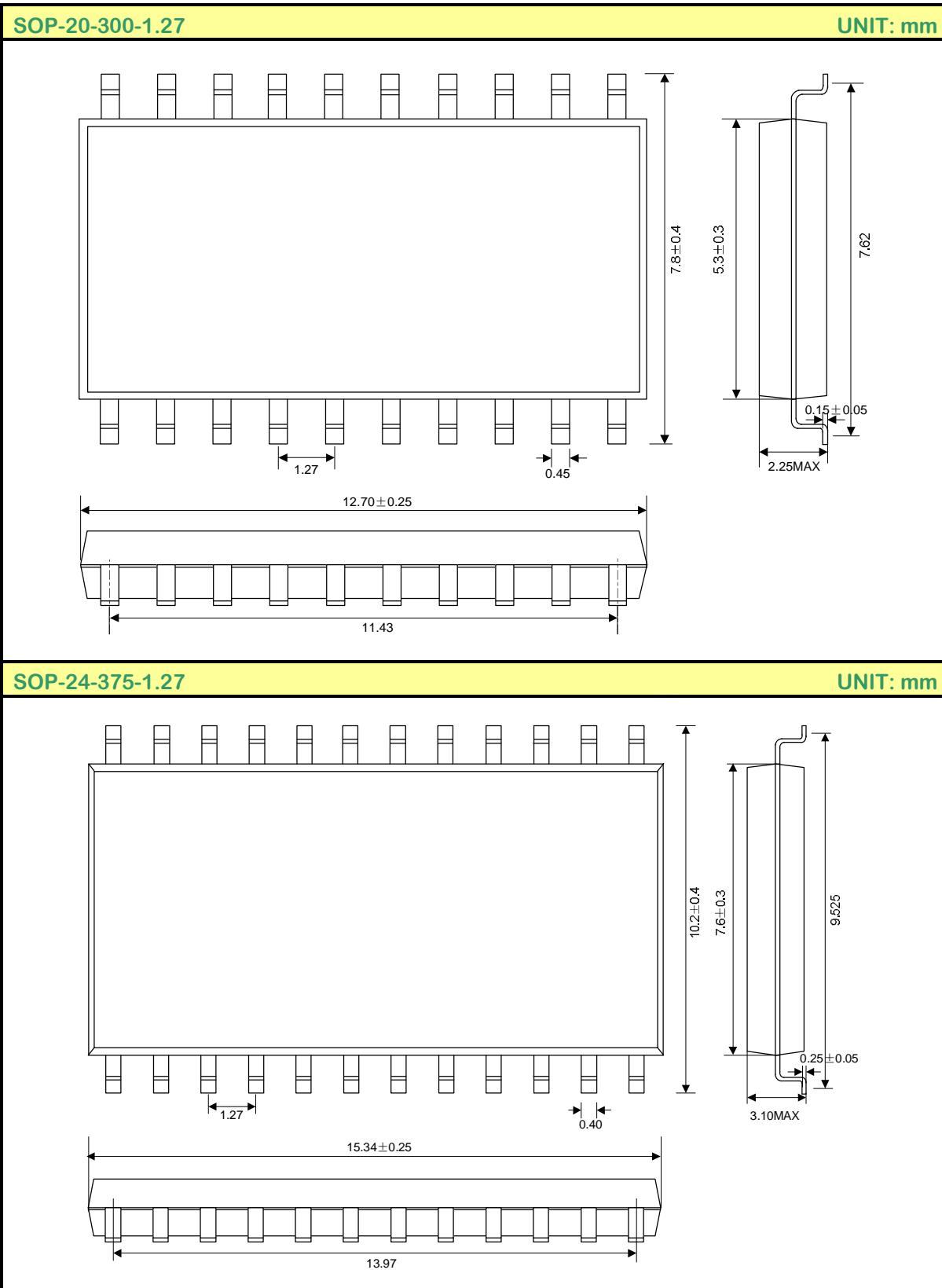


Note: The above IC only use to hint, not to specify.

Panel layout Notice:

- * In wire layout, the power filter capacitor should near to IC.
- * In wire layout, should avoid power line and ground line too long.
- * Recommended infrared transmit unit and IC ground line should layout separated, or overstriking lines.
- * The emitter of triode connect 1Ω resistor at least.

PACKAGE OUTLINE





HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.