

Dual N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.040 @ $V_{GS} = 4.5$ V	5.9
	0.045 @ $V_{GS} = 2.5$ V	5.6
	0.052 @ $V_{GS} = 1.8$ V	5.2

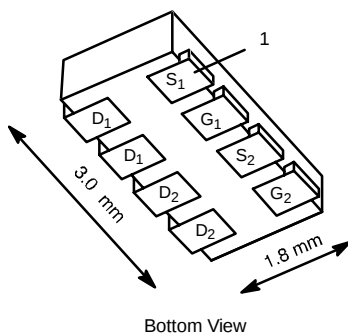
FEATURES

- TrenchFET® Power MOSFETS
- Ultra Low $r_{DS(on)}$ and Excellent Power Handling In Compact Footprint

APPLICATIONS

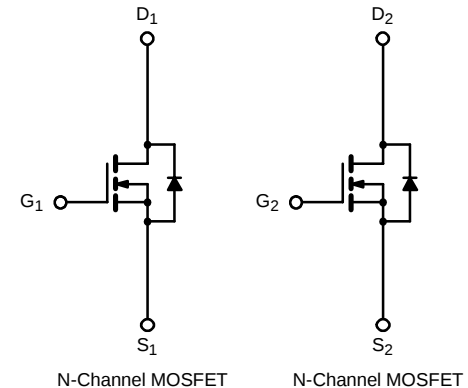
- Load Switch
- PA Switch
- Battery Switch

1206-8 ChipFET®



Ordering Information: Si5908DC-T1—E3

Marking Code
CC XXX
Lot Traceability and Date Code
Part # Code



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	20		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	5.9	4.4	A
	T _A = 85°C		4.2	3.1	
Pulsed Drain Current		I _{DM}	20		
Continuous Source Current (Diode Conduction) ^a		I _S	1.8	0.9	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.1	1.1	W
	T _A = 85°C		1.1	0.6	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	60	$^\circ\text{C/W}$
		90	110	
Maximum Junction-to-Foot (Drain)	R_{thJF}	30	40	

Notes

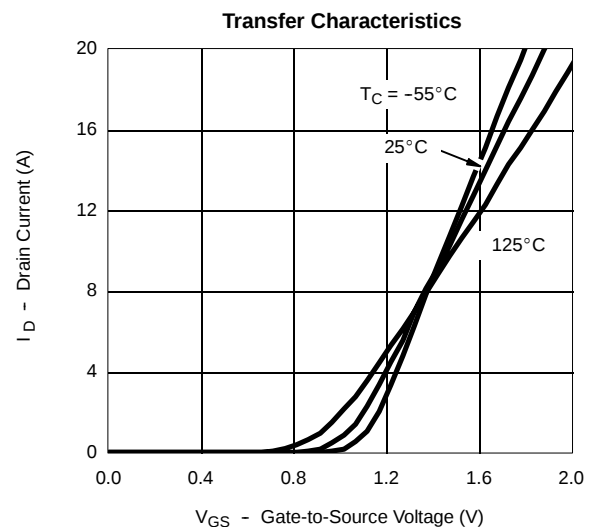
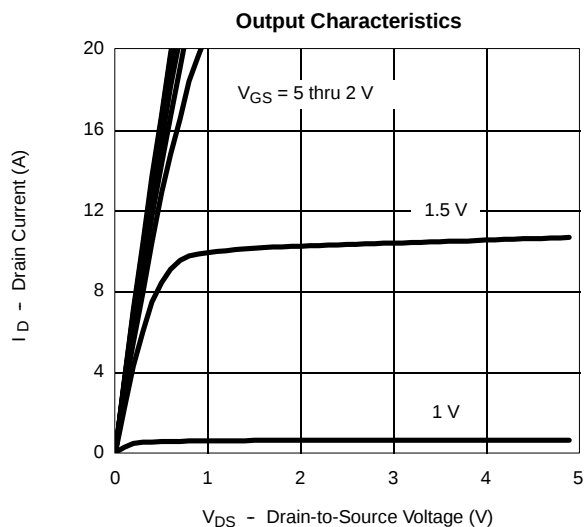
- Surface Mounted on 1" x 1" FR4 Board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

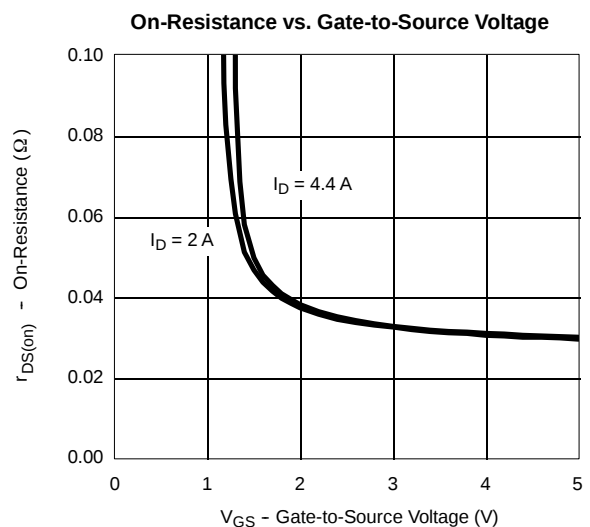
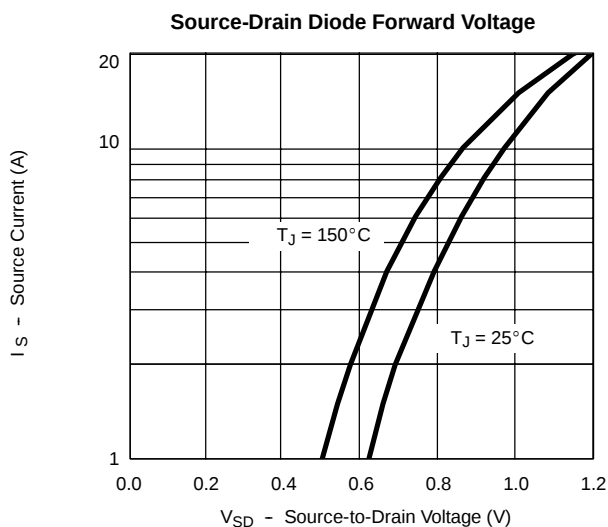
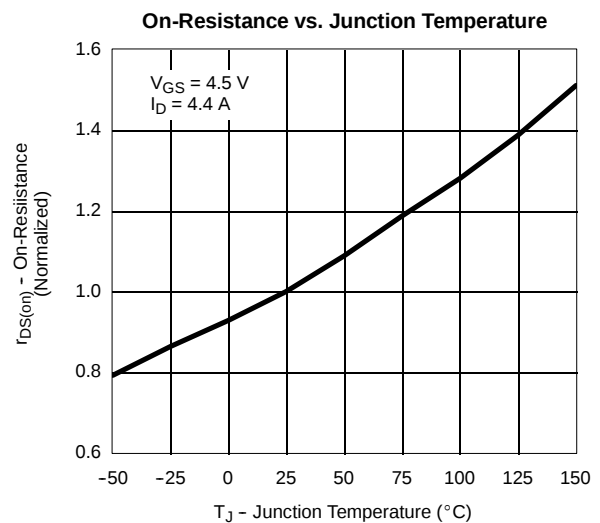
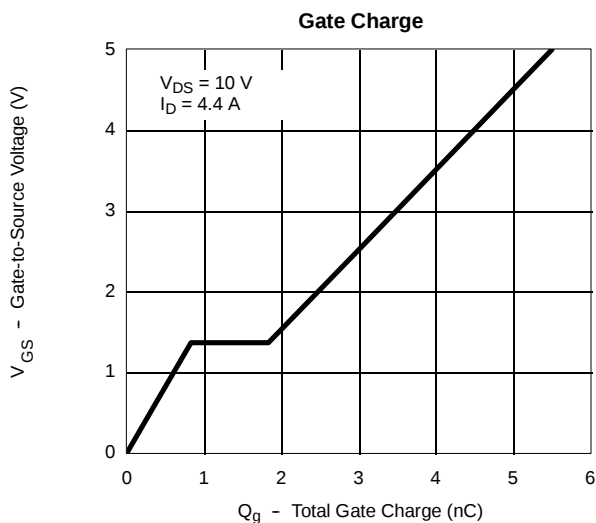
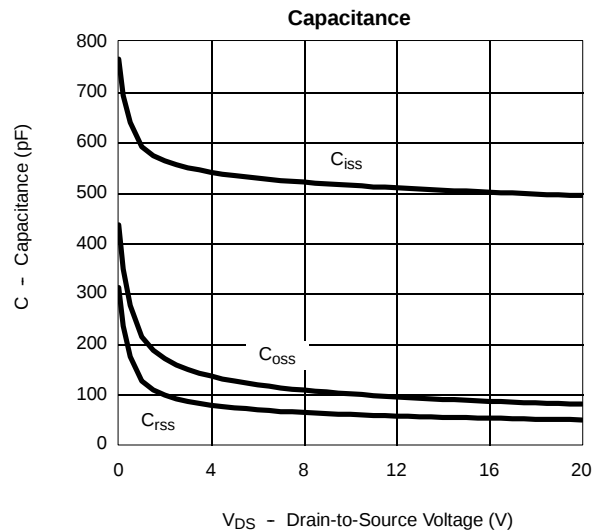
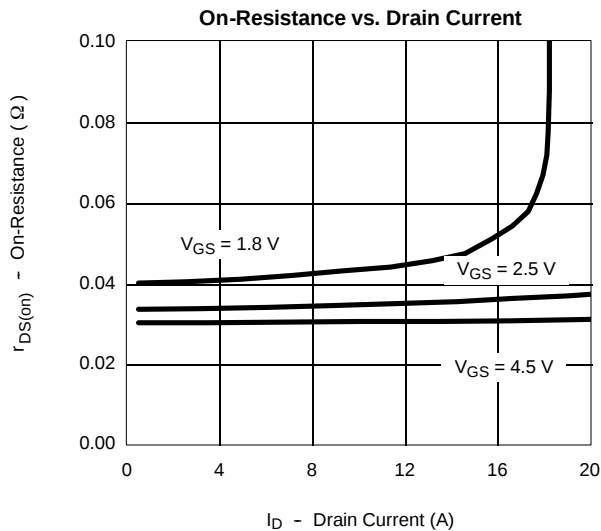
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.4		1.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 8\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 85^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 4.5\ \text{V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5\ \text{V}$, $I_D = 4.4\ \text{A}$		0.032	0.040	Ω
		$V_{GS} = 2.5\ \text{V}$, $I_D = 4.1\ \text{A}$		0.036	0.045	
		$V_{GS} = 1.8\ \text{V}$, $I_D = 1.9\ \text{A}$		0.042	0.052	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}$, $I_D = 4.4\ \text{A}$		22		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 0.9\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 4.4\ \text{A}$		5	7.5	nC
Gate-Source Charge	Q_{gs}			0.85		
Gate-Drain Charge	Q_{gd}			1		
Gate Resistance	R_g			1.9		Ω
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\ \text{V}$, $R_L = 10\ \Omega$ $I_D \approx 1\ \text{A}$, $V_{GEN} = 4.5\ \text{V}$, $R_g = 6\ \Omega$		20	30	ns
Rise Time	t_r			36	55	
Turn-Off Delay Time	$t_{d(off)}$			30	45	
Fall Time	t_f			12	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 0.9\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		45	90	

Notes

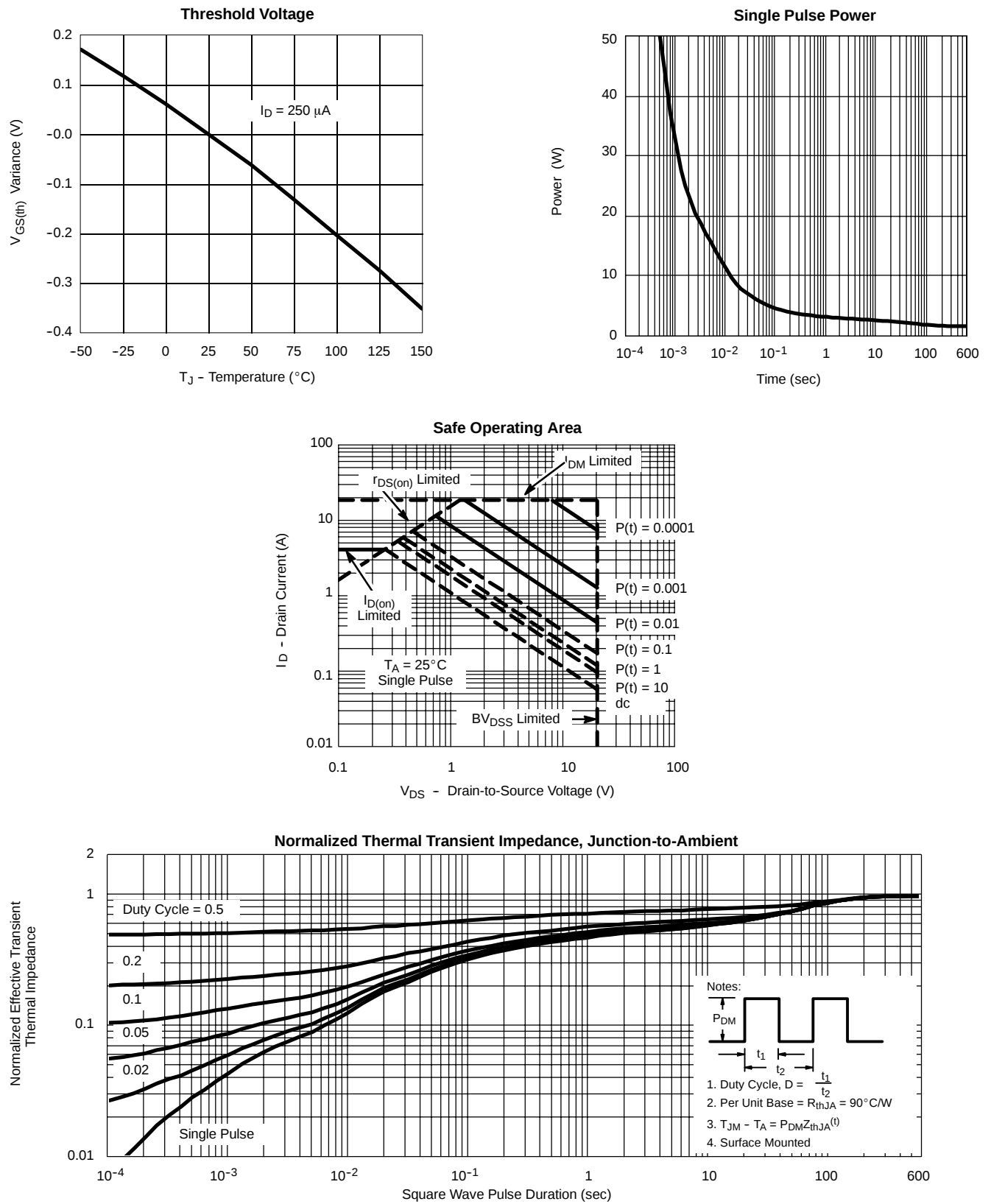
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$,
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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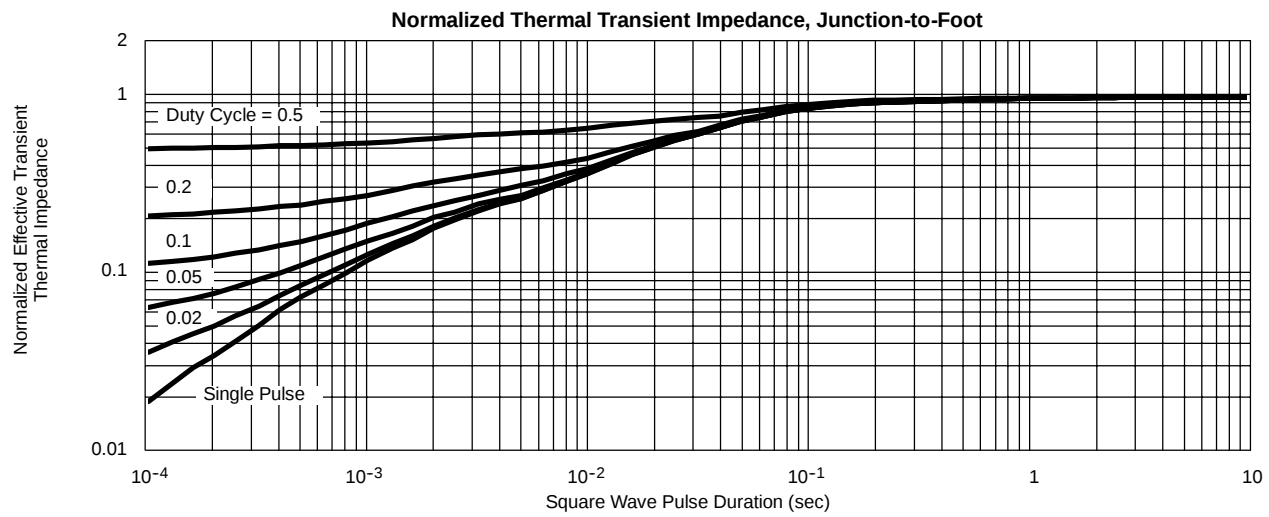
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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