

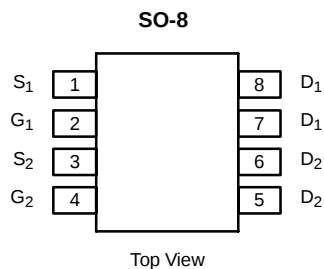


Dual N-Channel 2.5-V (G-S) MOSFET

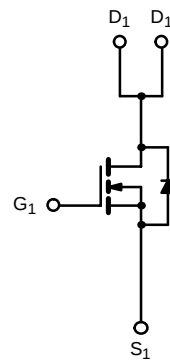
PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.05 @ $V_{GS} = 4.5$ V	5.0
	0.06 @ $V_{GS} = 3.0$ V	4.2
	0.08 @ $V_{GS} = 2.5$ V	3.6

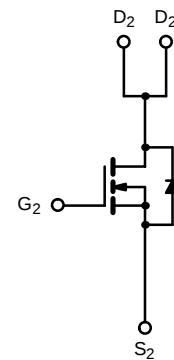
2.5-V Rated



Ordering Information: Si9925DY
Si9925DY-T1 (with Tape and Reel)



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	5.0	A
		4.0	
Pulsed Drain Current	I_{DM}	48	
Continuous Source Current (Diode Conduction) ^a	I_S	1.7	
Maximum Power Dissipation ^a	P_D	2	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

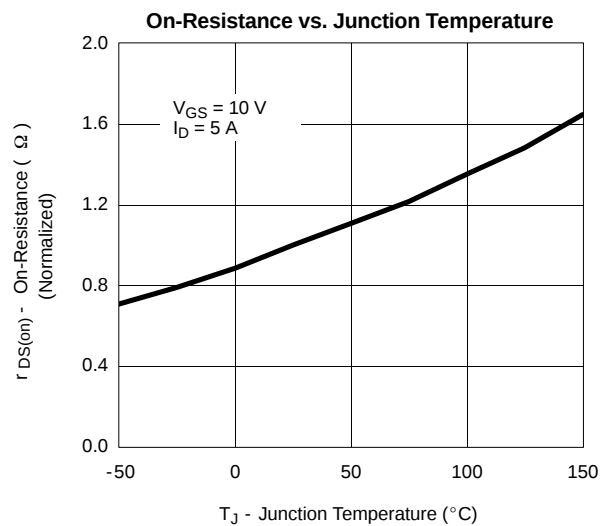
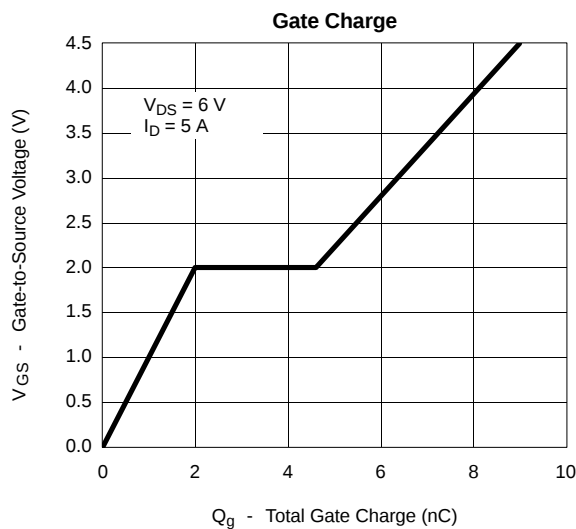
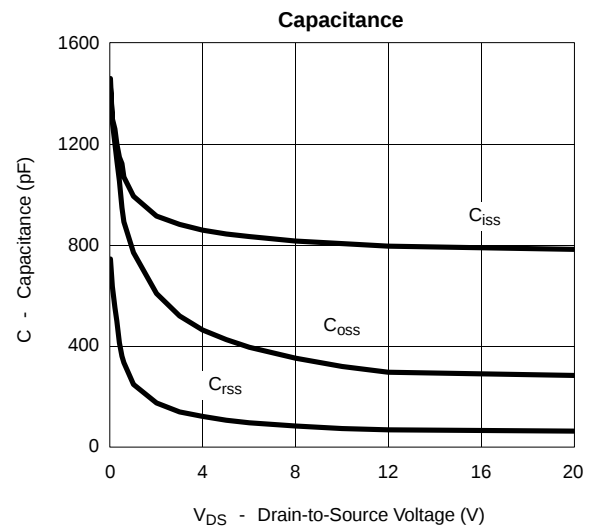
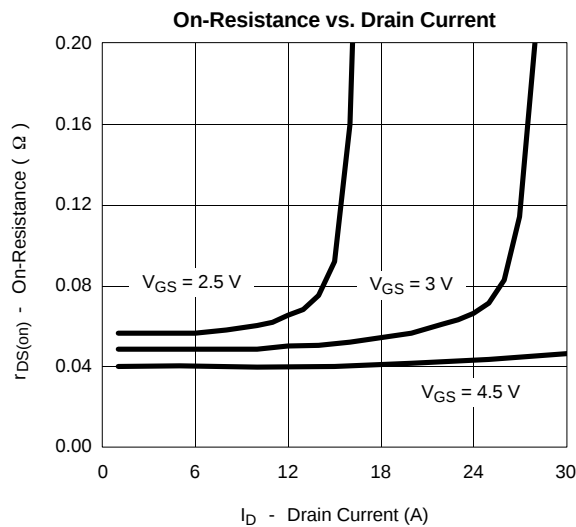
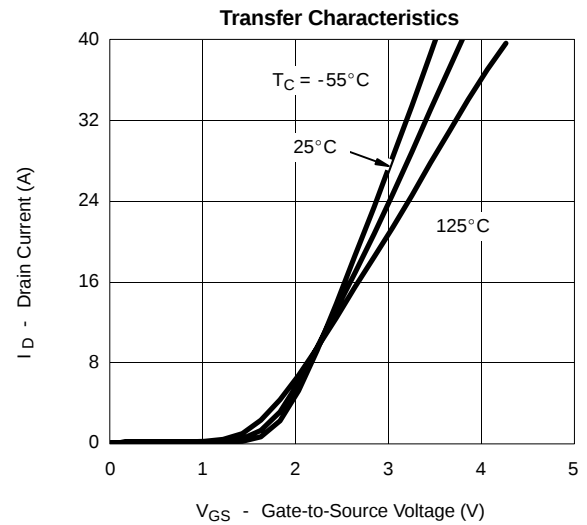
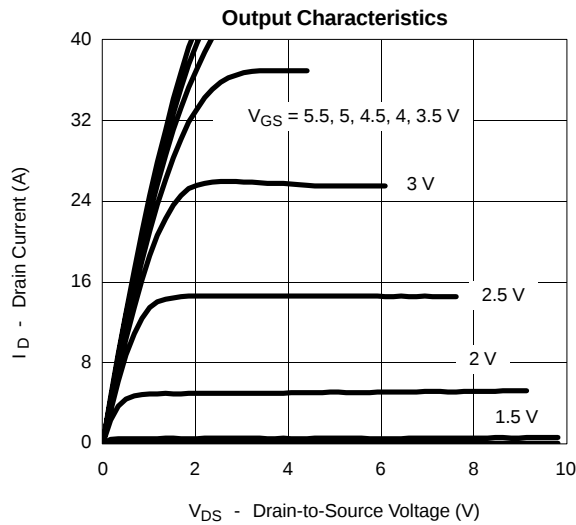
Specifications (T _J = 25°C Unless Otherwise Noted)						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.8			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 10 V, V _{GS} = 0 V			1	μA
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 70°C			5	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 5 V	30			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 7.2 V, I _D = 5.0 A	0.025	0.038	0.045	Ω
		V _{GS} = 4.5 V, I _D = 5.0 A		0.041	0.05	
		V _{GS} = 3.0 V, I _D = 3.9 A		0.050	0.06	
		V _{GS} = 2.5 V, I _D = 1 A		0.062	0.08	
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 5.0 A		14		S
Diode Forward Voltage ^b	V _{SD}	I _S = 5.0 A, V _{GS} = 0 V		0.81	1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 5.0 A		9	20	nC
Gate-Source Charge	Q _{gs}			2		
Gate-Drain Charge	Q _{gd}			2.6		
Gate Resistance	R _g		1		2.9	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 6 V, R _L = 6 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω		14	40	ns
Rise Time	t _r			13	30	
Turn-Off Delay Time	t _{d(off)}			35	60	
Fall Time	t _f			9	30	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 5.0 A, di/dt = 100 A/μs		60	150	

Notes

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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