

# RF Power Field Effect Transistor

## N-Channel Enhancement-Mode Lateral MOSFET

RF Power transistor designed for applications operating at frequencies between 960 and 1400 MHz, 1% to 20% duty cycle. This device is suitable for use in pulsed applications.

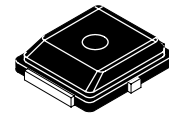
- Typical Pulsed Performance:  $V_{DD} = 50$  Volts,  $I_{DQ} = 10$  mA,  $P_{out} = 10$  Watts Peak (2 W Avg.),  $f = 1090$  MHz, Pulse Width = 100  $\mu$ sec, Duty Cycle = 20%  
Power Gain — 25 dB  
Drain Efficiency — 69%

### Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Qualified Up to a Maximum of 50  $V_{DD}$  Operation
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- RoHS Compliant
- In Tape and Reel. R4 Suffix = 100 Units per 12 mm, 7 inch Reel.

**MRF6V10010NR4**

**1090 MHz, 10 W, 50 V  
PULSED  
LATERAL N-CHANNEL  
RF POWER MOSFET**



**CASE 466-03, STYLE 1  
PLD-1.5  
PLASTIC**

**Table 1. Maximum Ratings**

| Rating                         | Symbol    | Value        | Unit |
|--------------------------------|-----------|--------------|------|
| Drain-Source Voltage           | $V_{DSS}$ | -0.5, +100   | Vdc  |
| Gate-Source Voltage            | $V_{GS}$  | -6.0, +10    | Vdc  |
| Storage Temperature Range      | $T_{stg}$ | - 65 to +150 | °C   |
| Case Operating Temperature     | $T_C$     | 150          | °C   |
| Operating Junction Temperature | $T_J$     | 200          | °C   |

**Table 2. Thermal Characteristics**

| Characteristic                                                                                                        | Symbol          | Value (1,2) | Unit |
|-----------------------------------------------------------------------------------------------------------------------|-----------------|-------------|------|
| Thermal Resistance, Junction to Case<br>Case Temperature 79°C, 10 W Pulsed, 100 $\mu$ sec Pulse Width, 20% Duty Cycle | $Z_{\theta JC}$ | 1.6         | °C/W |

- MTTF calculator available at <http://www.freescal.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
- Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescal.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

| Test Methodology                      | Class        |
|---------------------------------------|--------------|
| Human Body Model (per JESD22-A114)    | 1C (Minimum) |
| Machine Model (per EIA/JESD22-A115)   | A (Minimum)  |
| Charge Device Model (per JESD22-C101) | IV (Minimum) |

**Table 4. Moisture Sensitivity Level**

| Test Methodology                     | Rating | Package Peak Temperature | Unit |
|--------------------------------------|--------|--------------------------|------|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3      | 260                      | °C   |

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

**Off Characteristics**

|                                                                                                    |               |     |   |     |                 |
|----------------------------------------------------------------------------------------------------|---------------|-----|---|-----|-----------------|
| Gate-Source Leakage Current<br>( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )               | $I_{GSS}$     | —   | — | 10  | $\mu\text{Adc}$ |
| Drain-Source Breakdown Voltage<br>( $V_{GS} = 0\text{ Vdc}$ , $I_D = 7\text{ mA}$ )                | $V_{(BR)DSS}$ | 100 | — | —   | Vdc             |
| Zero Gate Voltage Drain Leakage Current<br>( $V_{DS} = 50\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )  | $I_{DSS}$     | —   | — | 50  | $\mu\text{Adc}$ |
| Zero Gate Voltage Drain Leakage Current<br>( $V_{DS} = 100\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ ) | $I_{DSS}$     | —   | — | 2.5 | mA              |

**On Characteristics**

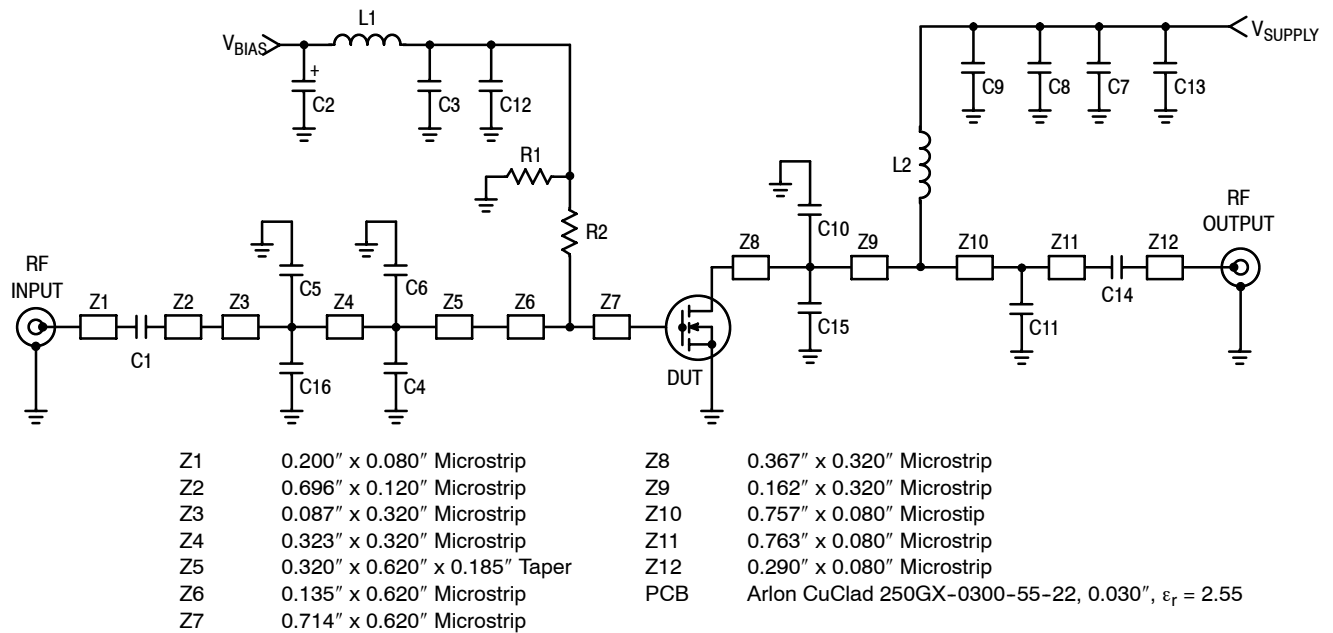
|                                                                                                              |              |     |     |     |     |
|--------------------------------------------------------------------------------------------------------------|--------------|-----|-----|-----|-----|
| Gate Threshold Voltage<br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 36\text{ }\mu\text{Adc}$ )                     | $V_{GS(th)}$ | 1   | 1.7 | 2.5 | Vdc |
| Gate Quiescent Voltage<br>( $V_{DD} = 50\text{ Vdc}$ , $I_D = 10\text{ mAdc}$ , Measured in Functional Test) | $V_{GS(Q)}$  | 1.7 | 2.4 | 3.2 | Vdc |
| Drain-Source On-Voltage<br>( $V_{GS} = 10\text{ Vdc}$ , $I_D = 70\text{ mAdc}$ )                             | $V_{DS(on)}$ | —   | 0.2 | —   | Vdc |

**Dynamic Characteristics**

|                                                                                                                       |           |   |      |   |    |
|-----------------------------------------------------------------------------------------------------------------------|-----------|---|------|---|----|
| Reverse Transfer Capacitance<br>( $V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ ) | $C_{rss}$ | — | 0.1  | — | pF |
| Output Capacitance<br>( $V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )           | $C_{oss}$ | — | 3.38 | — | pF |
| Input Capacitance<br>( $V_{DS} = 50\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz)            | $C_{iss}$ | — | 9.55 | — | pF |

**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 50\text{ Vdc}$ ,  $I_{DQ} = 10\text{ mA}$ ,  $P_{out} = 10\text{ W Peak}$  (2 W Avg.),  $f = 1090\text{ MHz}$ , Pulsed, 100  $\mu\text{sec}$  Pulse Width, 20% Duty Cycle

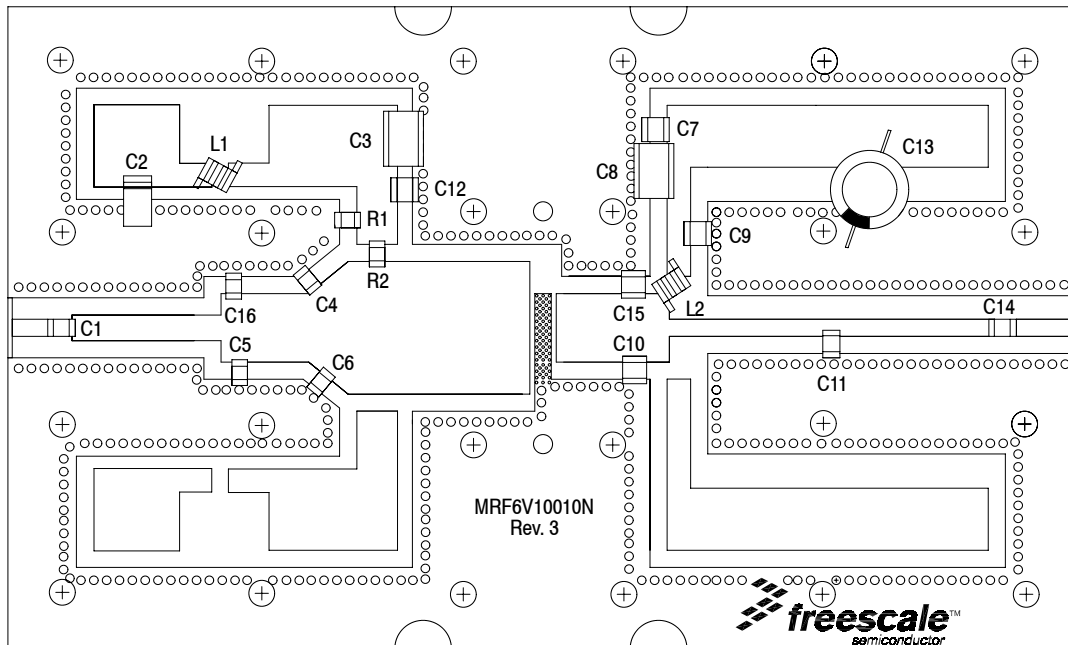
|                   |          |    |     |    |    |
|-------------------|----------|----|-----|----|----|
| Power Gain        | $G_{ps}$ | 23 | 25  | 28 | dB |
| Drain Efficiency  | $\eta_D$ | 66 | 69  | —  | %  |
| Input Return Loss | IRL      | —  | -12 | -8 | dB |



**Figure 1. MR6V10010NR4 Test Circuit Schematic**

**Table 6. MR6V10010NR4 Test Circuit Component Designations and Values**

| Part        | Description                         | Part Number        | Manufacturer       |
|-------------|-------------------------------------|--------------------|--------------------|
| C1, C9, C12 | 43 pF Chip Capacitors               | ATC100B430JT500XT  | ATC                |
| C2          | 10 $\mu$ F, 35 V Tantalum Capacitor | T491D106K035AT     | Kemet              |
| C3, C8      | 2.2 $\mu$ F, 100 V Chip Capacitors  | GQM1885C2A2R2CB01B | Murata             |
| C4, C6      | 7.5 pF Chip Capacitors              | ATC100B7R5CT500XT  | ATC                |
| C5, C16     | 3.0 pF Chip Capacitors              | ATC100B3R0CT500XT  | ATC                |
| C7          | 0.1 $\mu$ F Chip Capacitor          | C1206C104K5RACTR   | Kemet              |
| C10, C15    | 0.3 pF Chip Capacitors              | ATC100B0R3BT500XT  | ATC                |
| C11         | 5.6 pF Chip Capacitor               | ATC100B5R6CT500XT  | ATC                |
| C13         | 470 $\mu$ F, 63 V Chip Capacitor    | 477KXM063M         | Illinois Capacitor |
| C14         | 47 pF Chip Capacitor                | ATC100B470JT500XT  | ATC                |
| L1          | 8 nH Inductor                       | A03TKLC            | Coilcraft          |
| L2          | 5 nH Inductor                       | A02TKLC            | Coilcraft          |
| R1          | 3300 $\Omega$ , 1/4 W Chip Resistor | CRCW12063301FKEA   | Vishay             |
| R2          | 10 $\Omega$ , 1/4 W Chip Resistor   | CRCW120610R0FKEA   | Vishay             |



**Figure 2. MRF6V10010NR4 Test Circuit Component Layout**

## TYPICAL CHARACTERISTICS

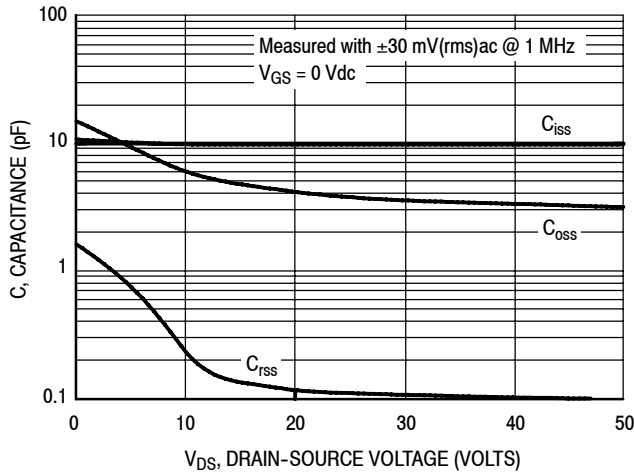


Figure 3. Capacitance versus Drain-Source Voltage

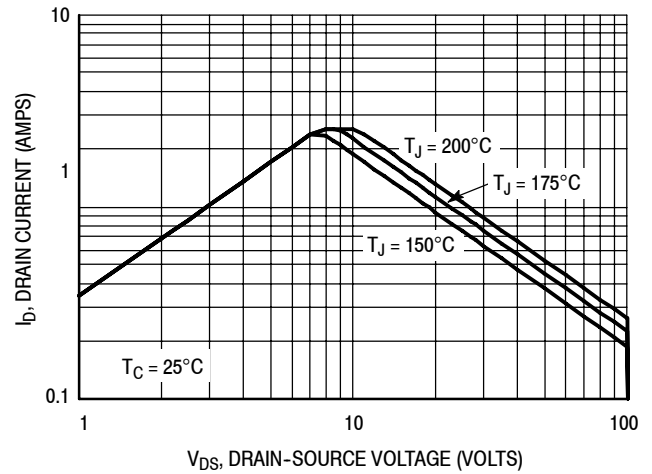


Figure 4. DC Safe Operating Area

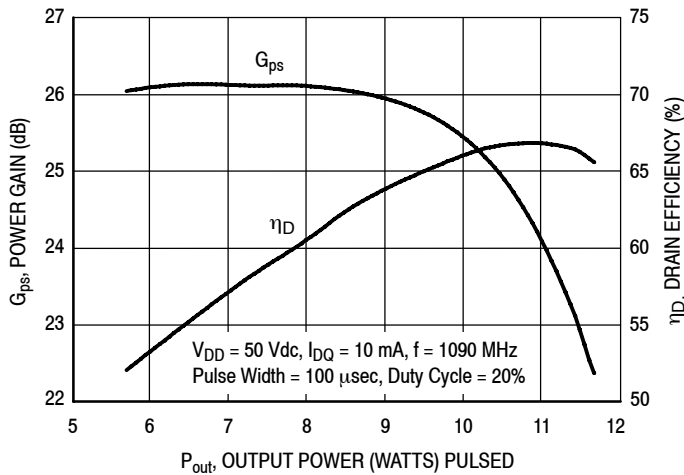


Figure 5. Pulsed Power Gain and Drain Efficiency versus Output Power

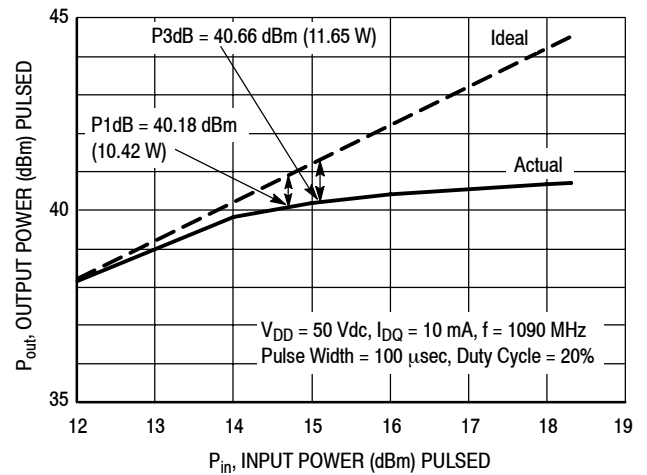


Figure 6. Pulsed Output Power versus Input Power

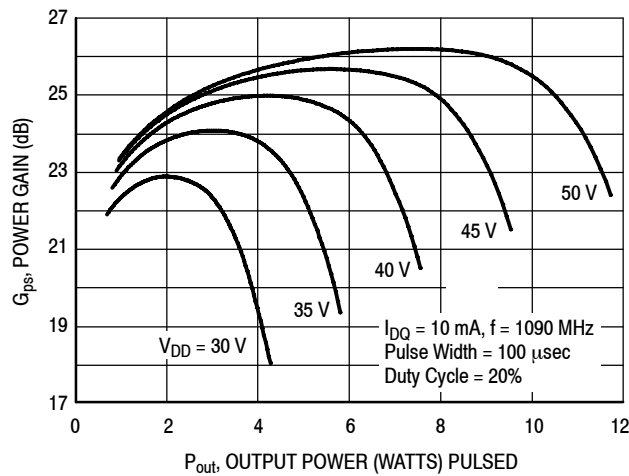


Figure 7. Pulsed Power Gain versus Output Power

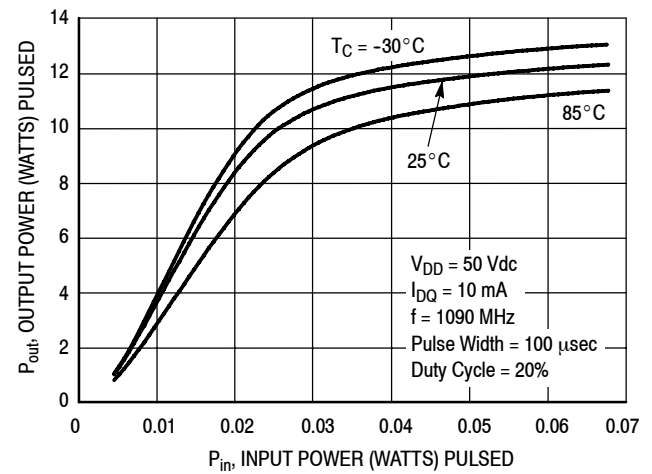
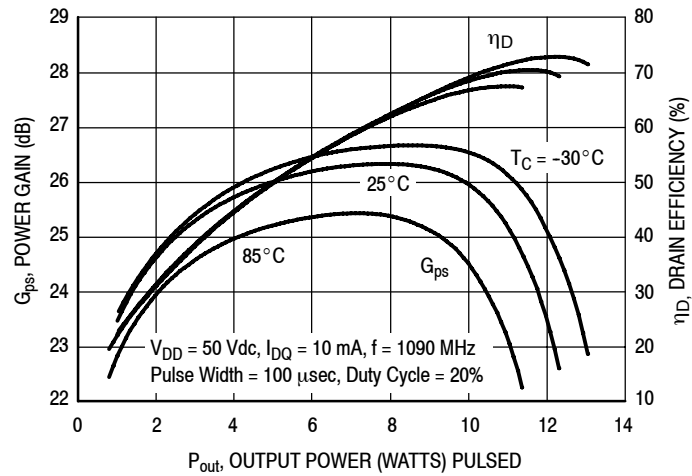
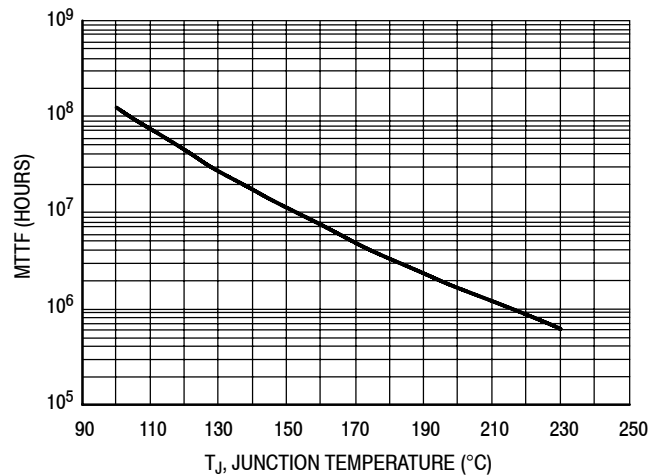


Figure 8. Pulsed Output Power versus Input Power

## TYPICAL CHARACTERISTICS



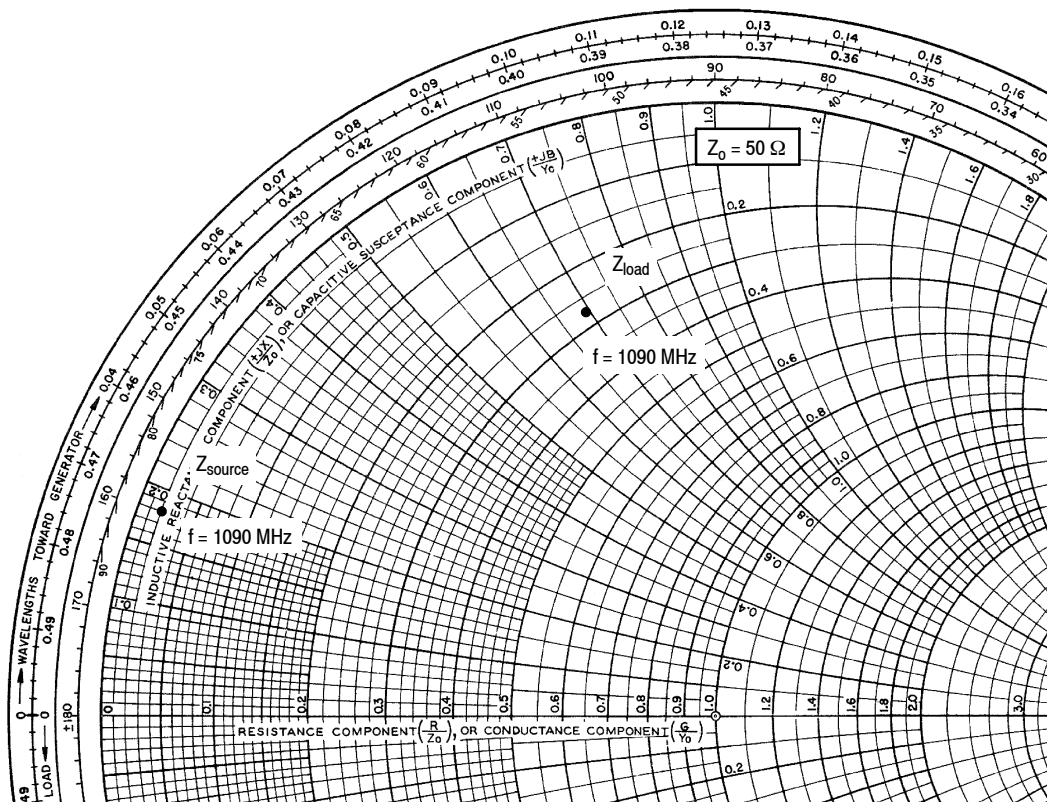
**Figure 9. Pulsed Power Gain and Drain Efficiency versus Output Power**



This above graph displays calculated MTTF in hours when the device is operated at  $V_{DD} = 50\text{ Vdc}$ ,  $P_{out} = 10\text{ W Peak}$ , Pulse Width =  $100\text{ }\mu\text{sec}$ , Duty Cycle = 20%, and  $\eta_D = 69\%$ .

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

**Figure 10. MTTF versus Junction Temperature**



$V_{DD} = 50 \text{ Vdc}$ ,  $I_{DQ} = 10 \text{ mA}$ ,  $P_{out} = 10 \text{ W Peak}$

| f<br>MHz | $Z_{source}$<br>$\Omega$ | $Z_{load}$<br>$\Omega$ |
|----------|--------------------------|------------------------|
| 1090     | $1.15 + j8.96$           | $13.47 + j34.32$       |

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

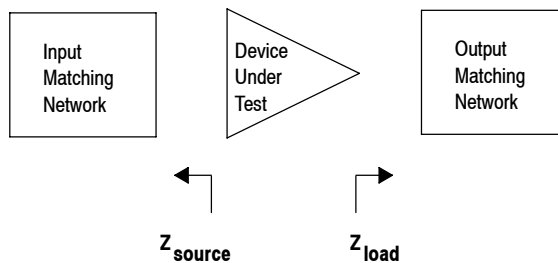
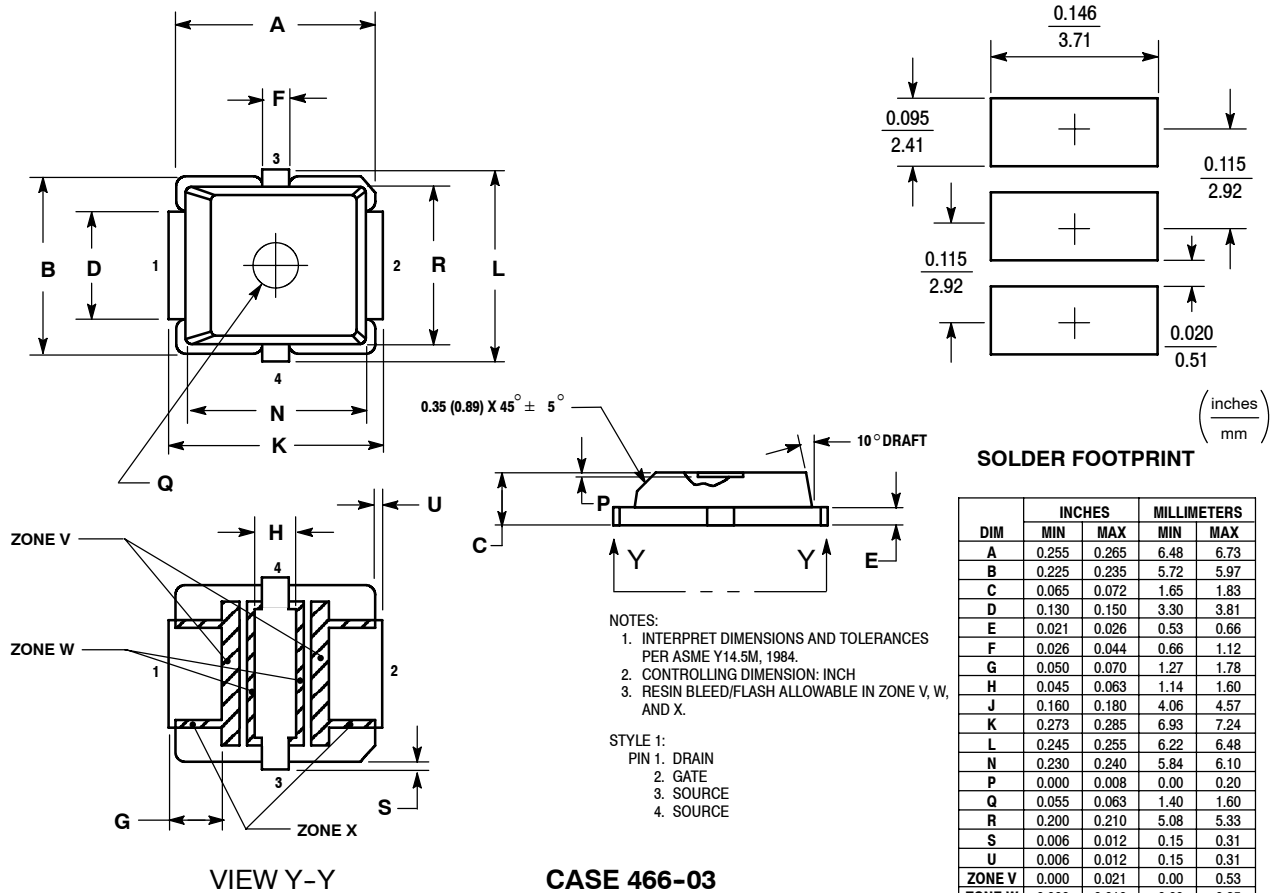


Figure 11. Series Equivalent Source and Load Impedance

## PACKAGE DIMENSIONS



**CASE 466-03**  
**ISSUE D**  
**PLD-1.5**  
**PLASTIC**

## PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator

For Software, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date      | Description                                                                                                                                                                                                                                                                                                                                                          |
|----------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0        | June 2008 | <ul style="list-style-type: none"><li>• Initial Release of Data Sheet</li></ul>                                                                                                                                                                                                                                                                                      |
| 1        | Feb. 2009 | <ul style="list-style-type: none"><li>• Corrected <math>Z_{\text{source}}</math>, “2.57 – j7.33” to “1.15 + j8.96” and <math>Z_{\text{load}}</math>, “14.10 – j34.77” to “13.47 + j34.32” in Fig. 11, Series Equivalent Source and Load Impedance data table and replotted data, p. 7</li></ul>                                                                      |
| 2        | June 2009 | <ul style="list-style-type: none"><li>• Modified data sheet to reflect MSL rating change from 1 to 3 as a result of the standardization of packing process as described in Product and Process Change Notification number, PCN13516, p. 2</li><li>• Added Electromigration MTTF Calculator availability to Product Documentation, Tools and Software, p. 9</li></ul> |
| 3        | July 2010 | <ul style="list-style-type: none"><li>• Reporting of pulsed thermal data now shown using the <math>Z_{\theta\text{JC}}</math> symbol, Table 2, Thermal Characteristics, p. 1</li><li>• Corrected errors made in the translation of the printed circuit board to the schematic, Fig. 1, Test Circuit Schematic and Z list, p. 3</li></ul>                             |

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Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

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