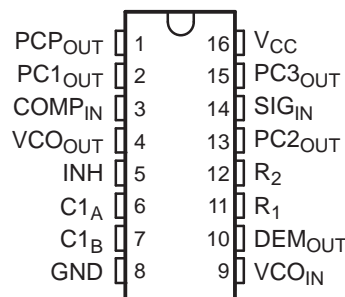


FEATURES

- **Choice of Three Phase Comparators**
 - Exclusive OR
 - Edge-Triggered J-K Flip-Flop
 - Edge-Triggered RS Flip-Flop
- **Excellent VCO Frequency Linearity**
- **VCO-Inhibit Control for ON/OFF Keying and for Low Standby Power Consumption**
- **Optimized Power-Supply Voltage Range From 3 V to 5.5 V**
- **Wide Operating Temperature Range . . . –40°C to 125°C**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

D, DGV, NS, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74LV4046A is a high-speed silicon-gate CMOS device that is pin compatible with the CD4046B and the CD74HC4046. The device is specified in compliance with JEDEC Std 7.

The SN74LV4046A is a phase-locked loop (PLL) circuit that contains a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2, and PC3). A signal input and a comparator input are common to each comparator.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the SN74LV4046A forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear operational amplifier techniques.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOP – NS	Tube of 50	SN74LV4046ANS	74LV4046A
		Reel of 2000	SN74LV4046ANSR	
	SOIC – D	Tube of 40	SN74LV4046AD	LV4046A
		Reel of 2500	SN74LV4046ADR	
	TSSOP – PW	Tube of 90	SN74LV4046APW	LW046A
		Reel of 2000	SN74LV4046APWR	
	TVSOP – DGV	Reel of 2000	SN74LV4046ADGVR	LW046A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LV4046A

HIGH-SPEED CMOS LOGIC PHASE-LOCKED LOOP WITH VCO

SCES656C—FEBRUARY 2006—REVISED APRIL 2007

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PCP _{OUT}	Phase comparator pulse output
2	PC1 _{OUT}	Phase comparator 1 output
3	COMP _{IN}	Comparator input
4	VCO _{OUT}	VCO output
5	INH	Inhibit input
6	C1 _A	Capacitor C1 connection A
7	C1 _B	Capacitor C1 connection B
8	GND	Ground (0 V)
9	VCO _{IN}	VCO input
10	DEM _{OUT}	Demodulator output
11	R ₁	Resistor R1 connection
12	R ₂	Resistor R2 connection
13	PC2 _{OUT}	Phase comparator 2 output
14	SIG _{IN}	Signal input
15	PC3 _{OUT}	Phase comparator 3 output
16	V _{CC}	Positive supply voltage

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	DC supply voltage range	−0.5	7	V
V _I	Input voltage range	−0.5	V _{CC} + 0.5	V
V _O	Output voltage range	−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−20	mA
I _{OK}	Output clamp current	V _O < 0	−50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±35	mA
I _{CC}	DC V _{CC} or ground current		±70	mA
θ _{JA}	Package thermal impedance ⁽²⁾	D package	73	°C/W
		DGV package	120	
		NS package	64	
		PW package	108	
T _{stg}	Storage temperature range	−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

	PARAMETER	MIN	MAX	UNIT
T _A	Operating free-air temperature	−40	125	°C
V _{CC}	Supply voltage	3	5.5	V
V _I , V _O	DC input or output voltage	0	V _{CC}	V

Electrical Specifications

PARAMETER			TEST CONDITIONS		V _{CC} (V)	MIN TYP MAX		UNIT	
			V _I (V)	I _O (mA)					
VCO									
V _{IH}	High-level input voltage	INH				3 to 3.6 4.5 to 5.5	V _{CC} × 0.7 V _{CC} × 0.7	V	
V _{IL}	Low-level input voltage	INH				3 to 5.5 4.5 to 5.5	V _{CC} × 0.3 V _{CC} × 0.3	V	
V _{OH}	High-level output voltage	VCO _{OUT}	CMOS	V _{IL} or V _{IH}	−0.05	3 to 3.6 4.5 to 5.5	V _{CC} − 0.1 V _{CC} − 0.1	V	
			TTL		−12	4.5 to 5.5	3.8		
V _{OL}	Low-level output voltage	VCO _{OUT}	CMOS	V _{IL} or V _{IH}	0.05	3 to 3.6 4.5 to 5.5	0.1 0.1	V	
			TTL		12	4.5 to 5.5	0.55		
		C1A, C1B (test purposes only)			12	4.5 to 5.5	0.65		
I _I	Input leakage current	INH, VCO _{IN}		V _{CC} or GND		5.5	±1	μA	
R1 range ⁽¹⁾						3 to 5.5	3	50	kΩ
R2 range ⁽¹⁾						3 to 5.5	3	50	kΩ
C1 capacitance range						3 to 3.6 4.5 to 5.5	40 40	No Limit	pF
Operating voltage range		VCO _{IN}		Over the range specified for R1 for linearity ⁽²⁾		3 to 3.6 4.5 to 5.5	1.1 1.1	1.9 3.2	V
Phase Comparator									
V _{IH}	DC-coupled high-level input voltage		SIG _{IN} , COMP _{IN}			3 to 3.6 4.5 to 5.5	V _{CC} × 0.7 V _{CC} × 0.7		
V _{IL}	DC-coupled low-level input voltage		SIG _{IN} , COMP _{IN}			3 to 3.6 4.5 to 5.5	V _{CC} × 0.3 V _{CC} × 0.3	V	
V _{OH}	High-level output voltage	PCP _{OUT} , PCN _{OUT}	CMOS	V _{IL} or V _{IH}	−0.05	3 to 5.5	V _{CC} − 0.1	V	
					−6	3 to 3.6	2.48		
					−12	4.5 to 5.5	3.8		
V _{OL}	Low-level output voltage	PCP _{OUT} , PCN _{OUT}	CMOS	V _{IL} or V _{IH}	0.02	3 to 3.6 4.5 to 5.5	0.1 0.1	V	
					4	4.5 to 5.5			0.4
I _I	Input leakage current		SIG _{IN} , COMP _{IN}	V _{CC} or GND		3 to 3.6 4.5 to 5.5	±11 ±29	μA	
I _{OZ}	3-state off-state current		PC2 _{OUT}	V _{IL} or V _{IH}		3 to 5.5	±5	μA	
R _I	Input resistance		SIG _{IN} , COMP _{IN}	V _I at self-bias operating point, V _I = 0.5 V		3 4.5	800 250	kΩ	
Demodulator									
R _S	Resistor range			R _S > 300 kΩ, Leakage current can influence V _{DEMOUT}		3 to 3.6 4.5 to 5.5	50 50	300 300	kΩ
V _{OFF}	Offset voltage VCO _{IN} to V _{DEM}			V _I = V _{VCOIN} = V _{CC} /2, Values taken over R _S range		3 to 3.6 4.5 to 5.5	±30 ±20	mV	
I _{CC}	Quiescent device current			Pins 3, 5, and 14 at V _{CC} , Pin 9 at GND, I _I at pins 3 and 14 to be excluded		5.5		50	μA

(1) The value for R1 and R2 in parallel should exceed 2.7 k Ω .

(2) The maximum operating voltage can be as high as $V_{CC} - 0.9$ V; however, this may result in an increased offset voltage.

SN74LV4046A

HIGH-SPEED CMOS LOGIC PHASE-LOCKED LOOP WITH VCO

SCES656C—FEBRUARY 2006—REVISED APRIL 2007

Switching Specifications

$C_L = 50$ pF, Input t_r , $t_f = 6$ ns

PARAMETER			TEST CONDITIONS	V _{CC} (V)	MIN	TYP	MAX	UNIT
Phase Comparator								
t _{PLH} , t _{PHL}	Propagation delay	SIG _{IN} , COMP _{IN} to PC1 _{OUT}		3 to 3.6			135	ns
				4.5 to 5.5			50	
t _{PLH} , t _{PHL}	Propagation delay	SIG _{IN} , COMP _{IN} to PCP _{OUT}		3 to 3.6			300	ns
				4.5 to 5.5			60	
t _{PLH} , t _{PHL}	Propagation delay	SIG _{IN} , COMP _{IN} to PC3 _{OUT}		3 to 3.6			200	ns
				4.5 to 5.5			50	
t _{THL} , t _{TLH}	Output transition time			3 to 3.6			75	ns
				4.5 to 5.5			15	
t _{PZH} , t _{PZL}	3-state output enable time	SIG _{IN} , COMP _{IN} to PC2 _{OUT}		3 to 3.6			270	ns
				4.5 to 5.5			54	
t _{PHZ} , t _{PLZ}	3-state output disable time	SIG _{IN} , COMP _{IN} to PC2 _{OUT}		3 to 3.6			320	ns
				4.5 to 5.5			65	
	AC-coupled input sensitivity	(P-P) at SIG _{IN} or COMP _{IN}	V _{I(P-P)}	3 to 3.6		11		mV
				4.5 to 5.5		15		
VCO								
Δf/ΔT	Frequency stability with temperature change		V _I = VCO _{IN} = 1/2 V _{CC} , R ₁ = 100 kΩ, R ₂ = ∞, C ₁ = 100 pF	3 to 3.6		0.11		%/ ^o C
				4.5 to 5.5		0.11		
f _{MAX}	Maximum frequency		C ₁ = 50 pF, R ₁ = 3.5 kΩ, R ₂ = ∞	3 to 3.6		24		MHz
				4.5 to 5.5		24		
				3 to 3.6		38		
				4.5 to 5.5		38		
	Center frequency (duty 50%)		C ₁ = 40 pF, R ₁ = 3 kΩ, R ₂ = ∞, VCO _{IN} = V _{CC} /2	3 to 3.6		7	10	MHz
				4.5 to 5.5		12	17	
				4.5 ⁽¹⁾		15 ⁽¹⁾	17.5 ⁽¹⁾	
ΔfVCO	Frequency linearity		C ₁ = 100 pF, R ₁ = 100 kΩ, R ₂ = ∞	3 to 3.6		0.4		%
				4.5 to 5.5		0.4		
	Offset frequency		C ₁ = 1 nF, R ₂ = 220 kΩ	3 to 3.6		400		kHz
				4.5 to 5.5		400		
Demodulator								
V _{OUT} vs f _{IN}			C ₁ = 100 pF, C ₂ = 100 pF, R ₁ = 100 kΩ, R ₂ = ∞, R ₃ = 100 kΩ	3		8		mV/kHz
				4.5		330		

(1) Data is specified at 25 $^{\circ}$ C

APPLICATION INFORMATION

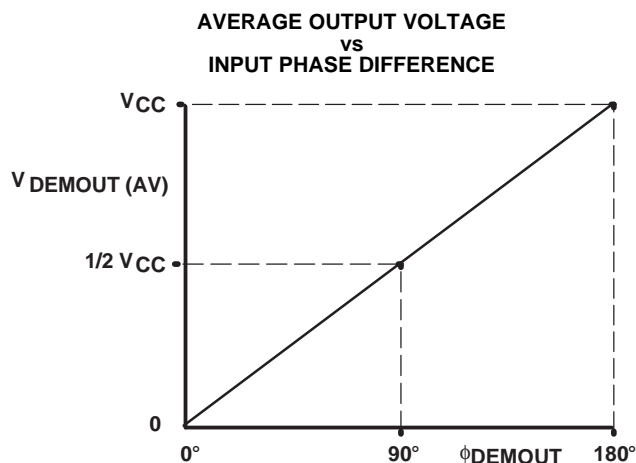


Figure 1. Phase Comparator 1:
 $V_{\text{DEMOUT}} = V_{\text{PC1OUT}} = (V_{\text{CC}}/\pi) (\text{SIG}_{\text{IN}} - \text{COMP}_{\text{IN}})$;
 $\text{DEMOUT} = (\text{SIG}_{\text{IN}} - \text{COMP}_{\text{IN}})$

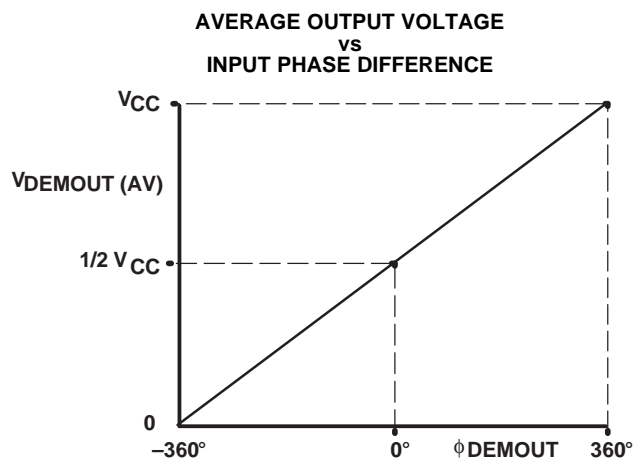


Figure 2. Phase Comparator 2:
 $V_{\text{DEMOUT}} = V_{\text{PC2OUT}} = (V_{\text{CC}}/4) (\text{SIG}_{\text{IN}} - \text{COMP}_{\text{IN}})$;
 $\text{DEMOUT} = (\text{SIG}_{\text{IN}} - \text{COMP}_{\text{IN}})$

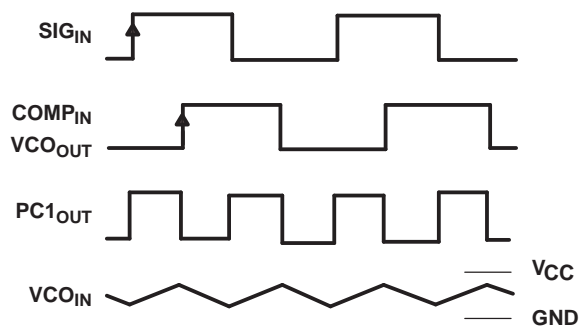


Figure 3. Typical Waveforms for PLL Using
Phase Comparator 1, Loop Locked at f_0

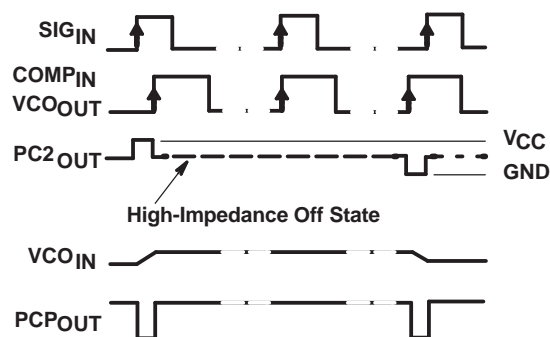


Figure 4. Typical Waveforms for PLL Using
Phase Comparator 2, Loop Locked at f_0

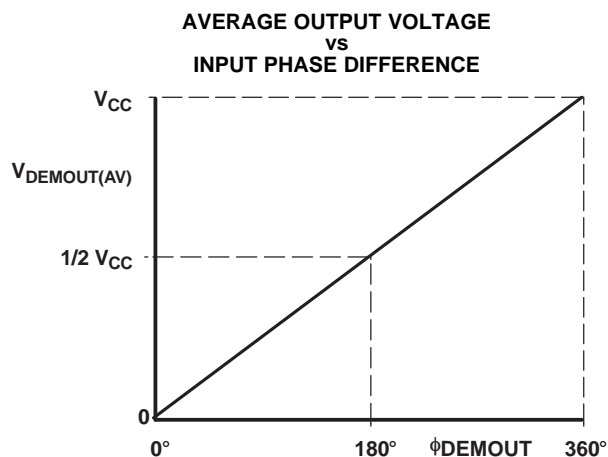


Figure 5. Phase Comparator 3:
 $V_{\text{DEMOUT}} = V_{\text{PC3OUT}} = (V_{\text{CC}}/2\pi) (\text{SIG}_{\text{IN}} - \text{COMP}_{\text{IN}})$;
 $\text{DEMOUT} = (\text{SIG}_{\text{IN}} - \text{COMP}_{\text{IN}})$

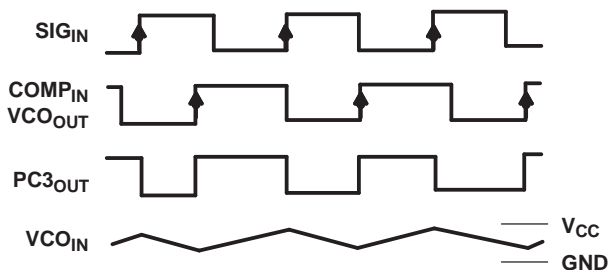


Figure 6. Typical Waveforms for PLL Using
Phase Comparator 3, Loop Locked at f_0

APPLICATION INFORMATION (continued)

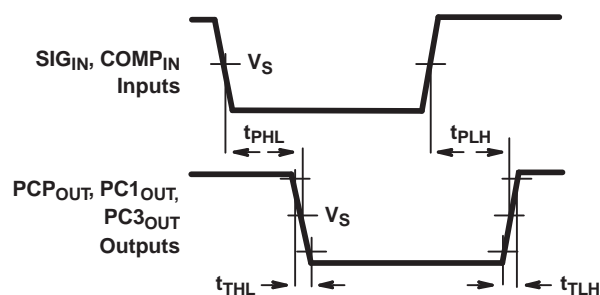


Figure 7. Input-to-Output Propagation Delays and Output Transition Times

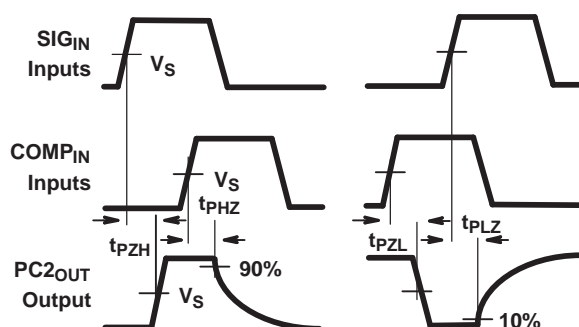


Figure 8. 3-State Enable and Disable Times for PC2_OUT

$C_{PD}^{(1)}$

CHIP SECTION	C_{PD}	UNIT
Comparator 1	120	pF
VCO	120	

- (1) R1 between 3 k Ω and 50 k Ω
R2 between 3 k Ω and 50 k Ω
R1 + R2 parallel value > 2.7 k Ω
C1 > 40 pF

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV4046AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV4046ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV4046ANS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046ANS4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV4046APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4046ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4046ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4046ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4046APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

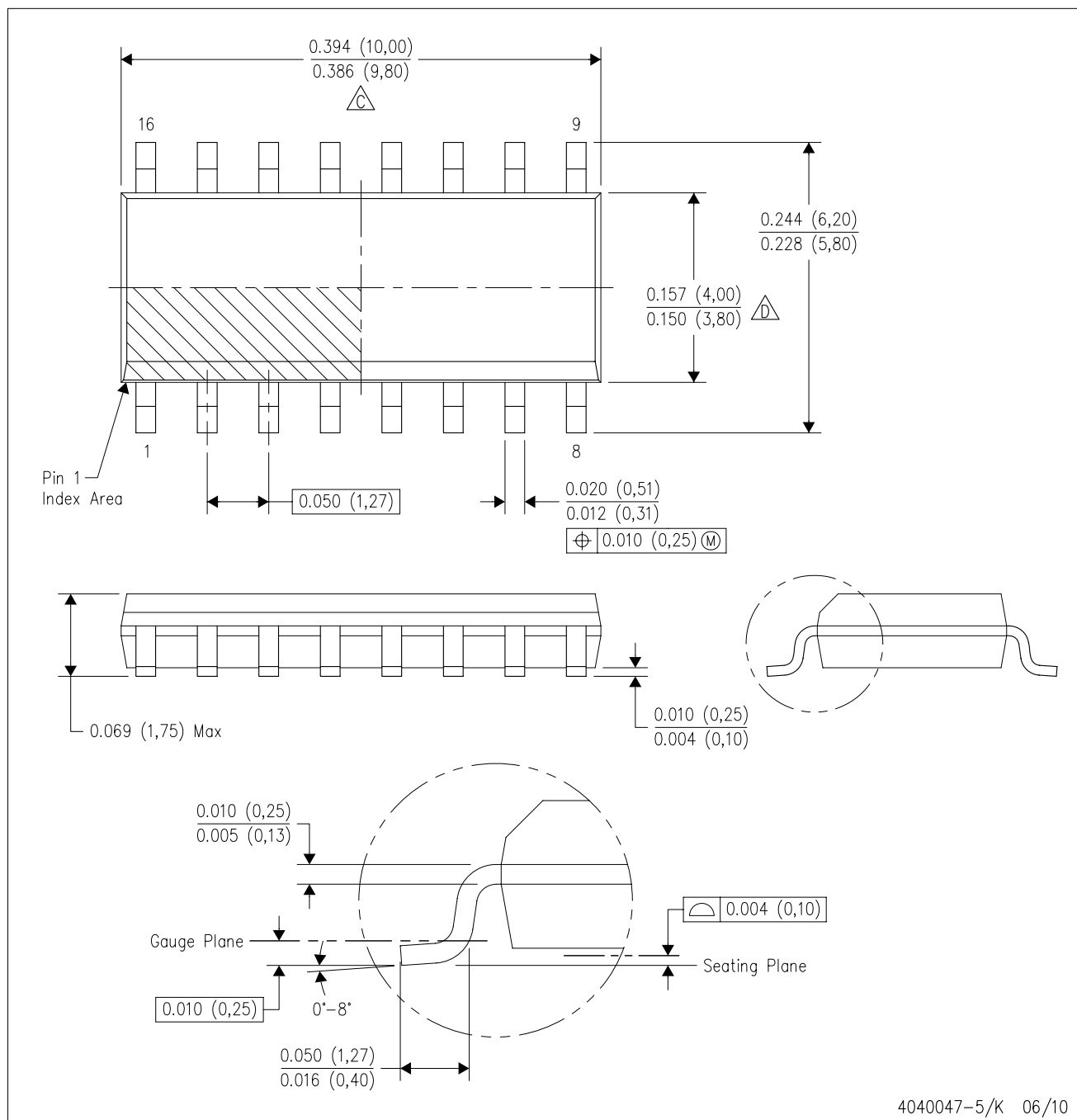


*All dimensions are nominal



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4046ADGVR	TVSOP	DGV	16	2000	346.0	346.0	29.0
SN74LV4046ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV4046ANSR	SO	NS	16	2000	346.0	346.0	33.0
SN74LV4046APWR	TSSOP	PW	16	2000	346.0	346.0	29.0

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps