

Sitronix

ST7624

65K Color Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7624 is a driver & controller LSI for 65k color graphic dot-matrix liquid crystal display systems. It generates 312 Segment and 104 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit/16-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

- ◆ 312 segment outputs / 104 common outputs

Applicable Duty Ratios

- ◆ Various partial display
- ◆ Partial window moving & data scrolling

Gray-Scale Display

- ◆ 4FRC & 31 PWM function circuit to display
- ◆ 64 gray-scale display.

On-chip Display Data RAM

- ◆ Capacity: 104X104X16 =173,056bits
- ◆ 65K colors (RGB)=(565) mode
- ◆ Dithered 262k colors (RGB)=(666) mode
- ◆ Dithered 16M colors (RGB)=(888) mode

Microprocessor Interface

- ◆ 8/16-bit parallel bi-directional interface with 6800-series or 8080-series
- ◆ 4-line serial interface (4-line-SIF)
- ◆ 3-line serial interface (3-line-SIF)

On-chip Low Power Analog Circuit

- ◆ On-chip oscillator circuit
- ◆ Voltage converter (x2, x3, x4, x5, x6, x7, x8)
- ◆ Voltage regulator (Temperature gradient = -0.119%/°C ±10%)
- ◆ On-chip electronic contrast control function
- ◆ Voltage follower (LCD bias: 1/5 to 1/12)

Operating Voltage Range

- ◆ Supply voltage (VDD, VDD1): 2.4 to 3.3V
(VDD2, VDD3, VDD4, VDD5): 2.4 to 3.3V
- ◆ LCD driving voltage (VOP = V0 - VSS): 3.76 to 18.0 V
- ◆ Suggested value of V0 is 12V~15V, bias = 1/11

LCD driving voltage (EEPROM)

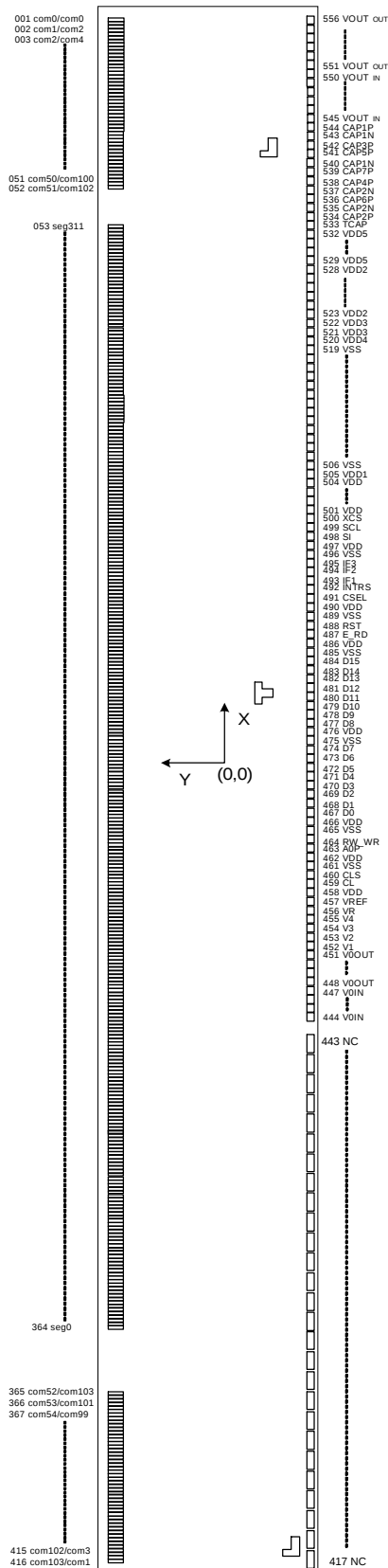
- ◆ To store contrast adjustment value for better display

Package Type

- ◆ Application for COG

ST7624	6800 , 8080 ,4-Line , 3-Line interface	
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Chip Size: 17,390 um x1,544 um

I Bump Pitch:

PAD NO 1 ~ 416: 40 um (COM/SEG)

PAD NO 417~443: 175um(NC)

PAD NO 444 ~ 556:110 um (I/O)

I Bump size:

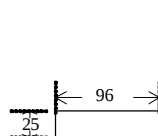
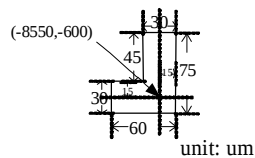
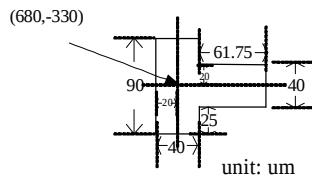
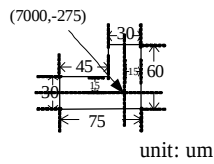
PAD NO.1~416: 25(x)um X 96(y)um

PAD No. 417~443: 158(x)um X 23(y)um

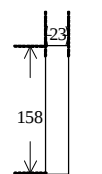
PAD NO. 444~556: 90(x)um X 40(y)um

I Bump Height: 17 um

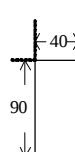
I Chip Thickness: 635um



Bump size of
PAD 1~416
unit: um



Bump size of
PAD 417~443
unit: um



Bump size of
PAD 444 ~ 556
unit: um

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4. Pad Center Coordinates

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
001	COM[0]	COM[0]	8557.0	642.5
002	COM[1]	COM[2]	8517.0	642.5
003	COM[2]	COM[4]	8477.0	642.5
004	COM[3]	COM[6]	8437.0	642.5
005	COM[4]	COM[8]	8397.0	642.5
006	COM[5]	COM[10]	8357.0	642.5
007	COM[6]	COM[12]	8317.0	642.5
008	COM[7]	COM[14]	8277.0	642.5
009	COM[8]	COM[16]	8237.0	642.5
010	COM[9]	COM[18]	8197.0	642.5
011	COM[10]	COM[20]	8157.0	642.5
012	COM[11]	COM[22]	8117.0	642.5
013	COM[12]	COM[24]	8077.0	642.5
014	COM[13]	COM[26]	8037.0	642.5
015	COM[14]	COM[28]	7997.0	642.5
016	COM[15]	COM[30]	7957.0	642.5
017	COM[16]	COM[32]	7917.0	642.5
018	COM[17]	COM[34]	7877.0	642.5
019	COM[18]	COM[36]	7837.0	642.5
020	COM[19]	COM[38]	7797.0	642.5
021	COM[20]	COM[40]	7757.0	642.5
022	COM[21]	COM[42]	7717.0	642.5
023	COM[22]	COM[44]	7677.0	642.5
024	COM[23]	COM[46]	7637.0	642.5
025	COM[24]	COM[48]	7597.0	642.5
026	COM[25]	COM[50]	7557.0	642.5
027	COM[26]	COM[52]	7517.0	642.5
028	COM[27]	COM[54]	7477.0	642.5
029	COM[28]	COM[56]	7437.0	642.5
030	COM[29]	COM[58]	7397.0	642.5
031	COM[30]	COM[60]	7357.0	642.5
032	COM[31]	COM[62]	7317.0	642.5
033	COM[32]	COM[64]	7277.0	642.5
034	COM[33]	COM[66]	7237.0	642.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
035	COM[34]	COM[68]	7197.0	642.5
036	COM[35]	COM[70]	7157.0	642.5
037	COM[36]	COM[72]	7117.0	642.5
038	COM[37]	COM[74]	7077.0	642.5
039	COM[38]	COM[76]	7037.0	642.5
040	COM[39]	COM[78]	6997.0	642.5
041	COM[40]	COM[80]	6957.0	642.5
042	COM[41]	COM[82]	6917.0	642.5
043	COM[42]	COM[84]	6877.0	642.5
044	COM[43]	COM[86]	6837.0	642.5
045	COM[44]	COM[88]	6797.0	642.5
046	COM[45]	COM[90]	6757.0	642.5
047	COM[46]	COM[92]	6717.0	642.5
048	COM[47]	COM[94]	6677.0	642.5
049	COM[48]	COM[96]	6637.0	642.5
050	COM[49]	COM[98]	6597.0	642.5
051	COM[50]	COM[100]	6557.0	642.5
052	COM[51]	COM[102]	6517.0	642.5
053	SEG[311]		6352.6	642.5
054	SEG[310]		6312.6	642.5
055	SEG[309]		6272.6	642.5
056	SEG[308]		6232.6	642.5
057	SEG[307]		6192.6	642.5
058	SEG[306]		6152.6	642.5
059	SEG[305]		6112.6	642.5
060	SEG[304]		6072.6	642.5
061	SEG[303]		6032.6	642.5
062	SEG[302]		5992.6	642.5
063	SEG[301]		5952.6	642.5
064	SEG[300]		5912.6	642.5
065	SEG[299]		5872.6	642.5
066	SEG[298]		5832.6	642.5
067	SEG[297]		5792.6	642.5
068	SEG[296]		5752.6	642.5

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PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
069	SEG[295]		5712.6	642.5
070	SEG[294]		5672.6	642.5
071	SEG[293]		5632.6	642.5
072	SEG[292]		5592.6	642.5
073	SEG[291]		5552.6	642.5
074	SEG[290]		5512.6	642.5
075	SEG[289]		5472.6	642.5
076	SEG[288]		5432.6	642.5
077	SEG[287]		5392.6	642.5
078	SEG[286]		5352.6	642.5
079	SEG[285]		5312.6	642.5
080	SEG[284]		5272.6	642.5
081	SEG[283]		5232.6	642.5
082	SEG[282]		5192.6	642.5
083	SEG[281]		5152.6	642.5
084	SEG[280]		5112.6	642.5
085	SEG[279]		5072.6	642.5
086	SEG[278]		5032.6	642.5
087	SEG[277]		4992.6	642.5
088	SEG[276]		4952.6	642.5
089	SEG[275]		4912.6	642.5
090	SEG[274]		4872.6	642.5
091	SEG[273]		4832.6	642.5
092	SEG[272]		4792.6	642.5
093	SEG[271]		4752.6	642.5
094	SEG[270]		4712.6	642.5
095	SEG[269]		4672.6	642.5
096	SEG[268]		4632.6	642.5
097	SEG[267]		4592.6	642.5
098	SEG[266]		4552.6	642.5
099	SEG[265]		4512.6	642.5
100	SEG[264]		4472.6	642.5
101	SEG[263]		4432.6	642.5
102	SEG[262]		4392.6	642.5
103	SEG[261]		4352.6	642.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
104	SEG[260]		4312.6	642.5
105	SEG[259]		4272.6	642.5
106	SEG[258]		4232.6	642.5
107	SEG[257]		4192.6	642.5
108	SEG[256]		4152.6	642.5
109	SEG[255]		4112.6	642.5
110	SEG[254]		4072.6	642.5
111	SEG[253]		4032.6	642.5
112	SEG[252]		3992.6	642.5
113	SEG[251]		3952.6	642.5
114	SEG[250]		3912.6	642.5
115	SEG[249]		3872.6	642.5
116	SEG[248]		3832.6	642.5
117	SEG[247]		3792.6	642.5
118	SEG[246]		3752.6	642.5
119	SEG[245]		3712.6	642.5
120	SEG[244]		3672.6	642.5
121	SEG[243]		3632.6	642.5
122	SEG[242]		3592.6	642.5
123	SEG[241]		3552.6	642.5
124	SEG[240]		3512.6	642.5
125	SEG[239]		3472.6	642.5
126	SEG[238]		3432.6	642.5
127	SEG[237]		3392.6	642.5
128	SEG[236]		3352.6	642.5
129	SEG[235]		3312.6	642.5
130	SEG[234]		3272.6	642.5
131	SEG[233]		3232.6	642.5
132	SEG[232]		3192.6	642.5
133	SEG[231]		3152.6	642.5
134	SEG[230]		3112.6	642.5
135	SEG[229]		3072.6	642.5
136	SEG[228]		3032.6	642.5
137	SEG[227]		2992.6	642.5
138	SEG[226]		2952.6	642.5

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PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
139	SEG[225]		2912.6	642.5
140	SEG[224]		2872.6	642.5
141	SEG[223]		2832.6	642.5
142	SEG[222]		2792.6	642.5
143	SEG[221]		2752.6	642.5
144	SEG[220]		2712.6	642.5
145	SEG[219]		2672.6	642.5
146	SEG[218]		2632.6	642.5
147	SEG[217]		2592.6	642.5
148	SEG[216]		2552.6	642.5
149	SEG[215]		2512.6	642.5
150	SEG[214]		2472.6	642.5
151	SEG[213]		2432.6	642.5
152	SEG[212]		2392.6	642.5
153	SEG[211]		2352.6	642.5
154	SEG[210]		2312.6	642.5
155	SEG[209]		2272.6	642.5
156	SEG[208]		2232.6	642.5
157	SEG[207]		2192.6	642.5
158	SEG[206]		2152.6	642.5
159	SEG[205]		2112.6	642.5
160	SEG[204]		2072.6	642.5
161	SEG[203]		2032.6	642.5
162	SEG[202]		1992.6	642.5
163	SEG[201]		1952.6	642.5
164	SEG[200]		1912.6	642.5
165	SEG[199]		1872.6	642.5
166	SEG[198]		1832.6	642.5
167	SEG[197]		1792.6	642.5
168	SEG[196]		1752.6	642.5
169	SEG[195]		1712.6	642.5
170	SEG[194]		1672.6	642.5
171	SEG[193]		1632.6	642.5
172	SEG[192]		1592.6	642.5
173	SEG[191]		1552.6	642.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
174	SEG[190]		1512.6	642.5
175	SEG[189]		1472.6	642.5
176	SEG[188]		1432.6	642.5
177	SEG[187]		1392.6	642.5
178	SEG[186]		1352.6	642.5
179	SEG[185]		1312.6	642.5
180	SEG[184]		1272.6	642.5
181	SEG[183]		1232.6	642.5
182	SEG[182]		1192.6	642.5
183	SEG[181]		1152.6	642.5
184	SEG[180]		1112.6	642.5
185	SEG[179]		1072.6	642.5
186	SEG[178]		1032.6	642.5
187	SEG[177]		992.6	642.5
188	SEG[176]		952.6	642.5
189	SEG[175]		912.6	642.5
190	SEG[174]		872.6	642.5
191	SEG[173]		832.6	642.5
192	SEG[172]		792.6	642.5
193	SEG[171]		752.6	642.5
194	SEG[170]		712.6	642.5
195	SEG[169]		672.6	642.5
196	SEG[168]		632.6	642.5
197	SEG[167]		592.6	642.5
198	SEG[166]		552.6	642.5
199	SEG[165]		512.6	642.5
200	SEG[164]		472.6	642.5
201	SEG[163]		432.6	642.5
202	SEG[162]		392.6	642.5
203	SEG[161]		352.6	642.5
204	SEG[160]		312.6	642.5
205	SEG[159]		272.6	642.5
206	SEG[158]		232.6	642.5
207	SEG[157]		192.6	642.5
208	SEG[156]		152.6	642.5

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PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
209	SEG[155]		112.6	642.5
210	SEG[154]		72.6	642.5
211	SEG[153]		32.6	642.5
212	SEG[152]		-7.4	642.5
213	SEG[151]		-47.4	642.5
214	SEG[150]		-87.4	642.5
215	SEG[149]		-127.4	642.5
216	SEG[148]		-167.4	642.5
217	SEG[147]		-207.4	642.5
218	SEG[146]		-247.4	642.5
219	SEG[145]		-287.4	642.5
220	SEG[144]		-327.4	642.5
221	SEG[143]		-367.4	642.5
222	SEG[142]		-407.4	642.5
223	SEG[141]		-447.4	642.5
224	SEG[140]		-487.4	642.5
225	SEG[139]		-527.4	642.5
226	SEG[138]		-567.4	642.5
227	SEG[137]		-607.4	642.5
228	SEG[136]		-647.4	642.5
229	SEG[135]		-687.4	642.5
230	SEG[134]		-727.4	642.5
231	SEG[133]		-767.4	642.5
232	SEG[132]		-807.4	642.5
233	SEG[131]		-847.4	642.5
234	SEG[130]		-887.4	642.5
235	SEG[129]		-927.4	642.5
236	SEG[128]		-967.4	642.5
237	SEG[127]		-1007.4	642.5
238	SEG[126]		-1047.4	642.5
239	SEG[125]		-1087.4	642.5
240	SEG[124]		-1127.4	642.5
241	SEG[123]		-1167.4	642.5
242	SEG[122]		-1207.4	642.5
243	SEG[121]		-1247.4	642.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
244	SEG[120]		-1287.4	642.5
245	SEG[119]		-1327.4	642.5
246	SEG[118]		-1367.4	642.5
247	SEG[117]		-1407.4	642.5
248	SEG[116]		-1447.4	642.5
249	SEG[115]		-1487.4	642.5
250	SEG[114]		-1527.4	642.5
251	SEG[113]		-1567.4	642.5
252	SEG[112]		-1607.4	642.5
253	SEG[111]		-1647.4	642.5
254	SEG[110]		-1687.4	642.5
255	SEG[109]		-1727.4	642.5
256	SEG[108]		-1767.4	642.5
257	SEG[107]		-1807.4	642.5
258	SEG[106]		-1847.4	642.5
259	SEG[105]		-1887.4	642.5
260	SEG[104]		-1927.4	642.5
261	SEG[103]		-1967.4	642.5
262	SEG[102]		-2007.4	642.5
263	SEG[101]		-2047.4	642.5
264	SEG[100]		-2087.4	642.5
265	SEG[99]		-2127.4	642.5
266	SEG[98]		-2167.4	642.5
267	SEG[97]		-2207.4	642.5
268	SEG[96]		-2247.4	642.5
269	SEG[95]		-2287.4	642.5
270	SEG[94]		-2327.4	642.5
271	SEG[93]		-2367.4	642.5
272	SEG[92]		-2407.4	642.5
273	SEG[91]		-2447.4	642.5
274	SEG[90]		-2487.4	642.5
275	SEG[89]		-2527.4	642.5
276	SEG[88]		-2567.4	642.5
277	SEG[87]		-2607.4	642.5
278	SEG[86]		-2647.4	642.5

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PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
279	SEG[85]		-2687.4	642.5
280	SEG[84]		-2727.4	642.5
281	SEG[83]		-2767.4	642.5
282	SEG[82]		-2807.4	642.5
283	SEG[81]		-2847.4	642.5
284	SEG[80]		-2887.4	642.5
285	SEG[79]		-2927.4	642.5
286	SEG[78]		-2967.4	642.5
287	SEG[77]		-3007.4	642.5
288	SEG[76]		-3047.4	642.5
289	SEG[75]		-3087.4	642.5
290	SEG[74]		-3127.4	642.5
291	SEG[73]		-3167.4	642.5
292	SEG[72]		-3207.4	642.5
293	SEG[71]		-3247.4	642.5
294	SEG[70]		-3287.4	642.5
295	SEG[69]		-3327.4	642.5
296	SEG[68]		-3367.4	642.5
297	SEG[67]		-3407.4	642.5
298	SEG[66]		-3447.4	642.5
299	SEG[65]		-3487.4	642.5
300	SEG[64]		-3527.4	642.5
301	SEG[63]		-3567.4	642.5
302	SEG[62]		-3607.4	642.5
303	SEG[61]		-3647.4	642.5
304	SEG[60]		-3687.4	642.5
305	SEG[59]		-3727.4	642.5
306	SEG[58]		-3767.4	642.5
307	SEG[57]		-3807.4	642.5
308	SEG[56]		-3847.4	642.5
309	SEG[55]		-3887.4	642.5
310	SEG[54]		-3927.4	642.5
311	SEG[53]		-3967.4	642.5
312	SEG[52]		-4007.4	642.5
313	SEG[51]		-4047.4	642.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
314	SEG[50]		-4087.4	642.5
315	SEG[49]		-4127.4	642.5
316	SEG[48]		-4167.4	642.5
317	SEG[47]		-4207.4	642.5
318	SEG[46]		-4247.4	642.5
319	SEG[45]		-4287.4	642.5
320	SEG[44]		-4327.4	642.5
321	SEG[43]		-4367.4	642.5
322	SEG[42]		-4407.4	642.5
323	SEG[41]		-4447.4	642.5
324	SEG[40]		-4487.4	642.5
325	SEG[39]		-4527.4	642.5
326	SEG[38]		-4567.4	642.5
327	SEG[37]		-4607.4	642.5
328	SEG[36]		-4647.4	642.5
329	SEG[35]		-4687.4	642.5
330	SEG[34]		-4727.4	642.5
331	SEG[33]		-4767.4	642.5
332	SEG[32]		-4807.4	642.5
333	SEG[31]		-4847.4	642.5
334	SEG[30]		-4887.4	642.5
335	SEG[29]		-4927.4	642.5
336	SEG[28]		-4967.4	642.5
337	SEG[27]		-5007.4	642.5
338	SEG[26]		-5047.4	642.5
339	SEG[25]		-5087.4	642.5
340	SEG[24]		-5127.4	642.5
341	SEG[23]		-5167.4	642.5
342	SEG[22]		-5207.4	642.5
343	SEG[21]		-5247.4	642.5
344	SEG[20]		-5287.4	642.5
345	SEG[19]		-5327.4	642.5
346	SEG[18]		-5367.4	642.5
347	SEG[17]		-5407.4	642.5
348	SEG[16]		-5447.4	642.5

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PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
349	SEG[15]		-5487.4	642.5
350	SEG[14]		-5527.4	642.5
351	SEG[13]		-5567.4	642.5
352	SEG[12]		-5607.4	642.5
353	SEG[11]		-5647.4	642.5
354	SEG[10]		-5687.4	642.5
355	SEG[9]		-5727.4	642.5
356	SEG[8]		-5767.4	642.5
357	SEG[7]		-5807.4	642.5
358	SEG[6]		-5847.4	642.5
359	SEG[5]		-5887.4	642.5
360	SEG[4]		-5927.4	642.5
361	SEG[3]		-5967.4	642.5
362	SEG[2]		-6007.4	642.5
363	SEG[1]		-6047.4	642.5
364	SEG[0]		-6087.4	642.5
365	COM[52]	COM[103]	-6485.75	642.5
366	COM[53]	COM[101]	-6525.75	642.5
367	COM[54]	COM[99]	-6565.75	642.5
368	COM[55]	COM[97]	-6605.75	642.5
369	COM[56]	COM[95]	-6645.75	642.5
370	COM[57]	COM[93]	-6685.75	642.5
371	COM[58]	COM[91]	-6725.75	642.5
372	COM[59]	COM[89]	-6765.75	642.5
373	COM[60]	COM[87]	-6805.75	642.5
374	COM[61]	COM[85]	-6845.75	642.5
375	COM[62]	COM[83]	-6885.75	642.5
376	COM[63]	COM[81]	-6925.75	642.5
377	COM[64]	COM[79]	-6965.75	642.5
378	COM[65]	COM[77]	-7005.75	642.5
379	COM[66]	COM[75]	-7045.75	642.5
380	COM[67]	COM[73]	-7085.75	642.5
381	COM[68]	COM[71]	-7125.75	642.5
382	COM[69]	COM[69]	-7165.75	642.5
383	COM[70]	COM[67]	-7205.75	642.5

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
384	COM[71]	COM[65]	-7245.75	642.5
385	COM[72]	COM[63]	-7285.75	642.5
386	COM[73]	COM[61]	-7325.75	642.5
387	COM[74]	COM[59]	-7365.75	642.5
388	COM[75]	COM[57]	-7405.75	642.5
389	COM[76]	COM[55]	-7445.75	642.5
390	COM[77]	COM[53]	-7485.75	642.5
391	COM[78]	COM[51]	-7525.75	642.5
392	COM[79]	COM[49]	-7565.75	642.5
393	COM[80]	COM[47]	-7605.75	642.5
394	COM[81]	COM[45]	-7645.75	642.5
395	COM[82]	COM[43]	-7685.75	642.5
396	COM[83]	COM[41]	-7725.75	642.5
397	COM[84]	COM[39]	-7765.75	642.5
398	COM[85]	COM[37]	-7805.75	642.5
399	COM[86]	COM[35]	-7845.75	642.5
400	COM[87]	COM[33]	-7885.75	642.5
401	COM[88]	COM[31]	-7925.75	642.5
402	COM[89]	COM[29]	-7965.75	642.5
403	COM[90]	COM[27]	-8005.75	642.5
404	COM[91]	COM[25]	-8045.75	642.5
405	COM[92]	COM[23]	-8085.75	642.5
406	COM[93]	COM[21]	-8125.75	642.5
407	COM[94]	COM[19]	-8165.75	642.5
408	COM[95]	COM[17]	-8205.75	642.5
409	COM[96]	COM[15]	-8245.75	642.5
410	COM[97]	COM[13]	-8285.75	642.5
411	COM[98]	COM[11]	-8325.75	642.5
412	COM[99]	COM[9]	-8365.75	642.5
413	COM[100]	COM[7]	-8405.75	642.5
414	COM[101]	COM[5]	-8445.75	642.5
415	COM[102]	COM[3]	-8485.75	642.5
416	COM[103]	COM[1]	-8525.75	642.5
417	NC		-8534.45	-679.5
418	NC		-8359.45	-679.5

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PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
419	NC		-8184.45	-679.5
420	NC		-8009.45	-679.5
421	NC		-7834.45	-679.5
422	NC		-7659.45	-679.5
423	NC		-7484.45	-679.5
424	NC		-7309.45	-679.5
425	NC		-7134.45	-679.5
426	NC		-6959.45	-679.5
427	NC		-6784.45	-679.5
428	NC		-6609.45	-679.5
429	NC		-6434.45	-679.5
430	NC		-6259.45	-679.5
431	NC		-6084.45	-679.5
432	NC		-5909.45	-679.5
433	NC		-5734.45	-679.5
434	NC		-5559.45	-679.5
435	NC		-5384.45	-679.5
436	NC		-5209.45	-679.5
437	NC		-5034.45	-679.5
438	NC		-4859.45	-679.5
439	NC		-4684.45	-679.5
440	NC		-4509.45	-679.5
441	NC		-4334.45	-679.5
442	NC		-4159.45	-679.5
443	NC		-3984.45	-679.5
444	VOIN		-3795.58	-671.0
445	VOIN		-3685.58	-671.0
446	VOIN		-3575.58	-671.0
447	VOIN		-3465.58	-671.0
448	V0OUT		-3355.58	-671.0
449	V0OUT		-3245.58	-671.0
450	V0OUT		-3135.58	-671.0
451	V0OUT		-3025.58	-671.0
452	V1		-2915.58	-671.0
453	V2		-2805.58	-671.0

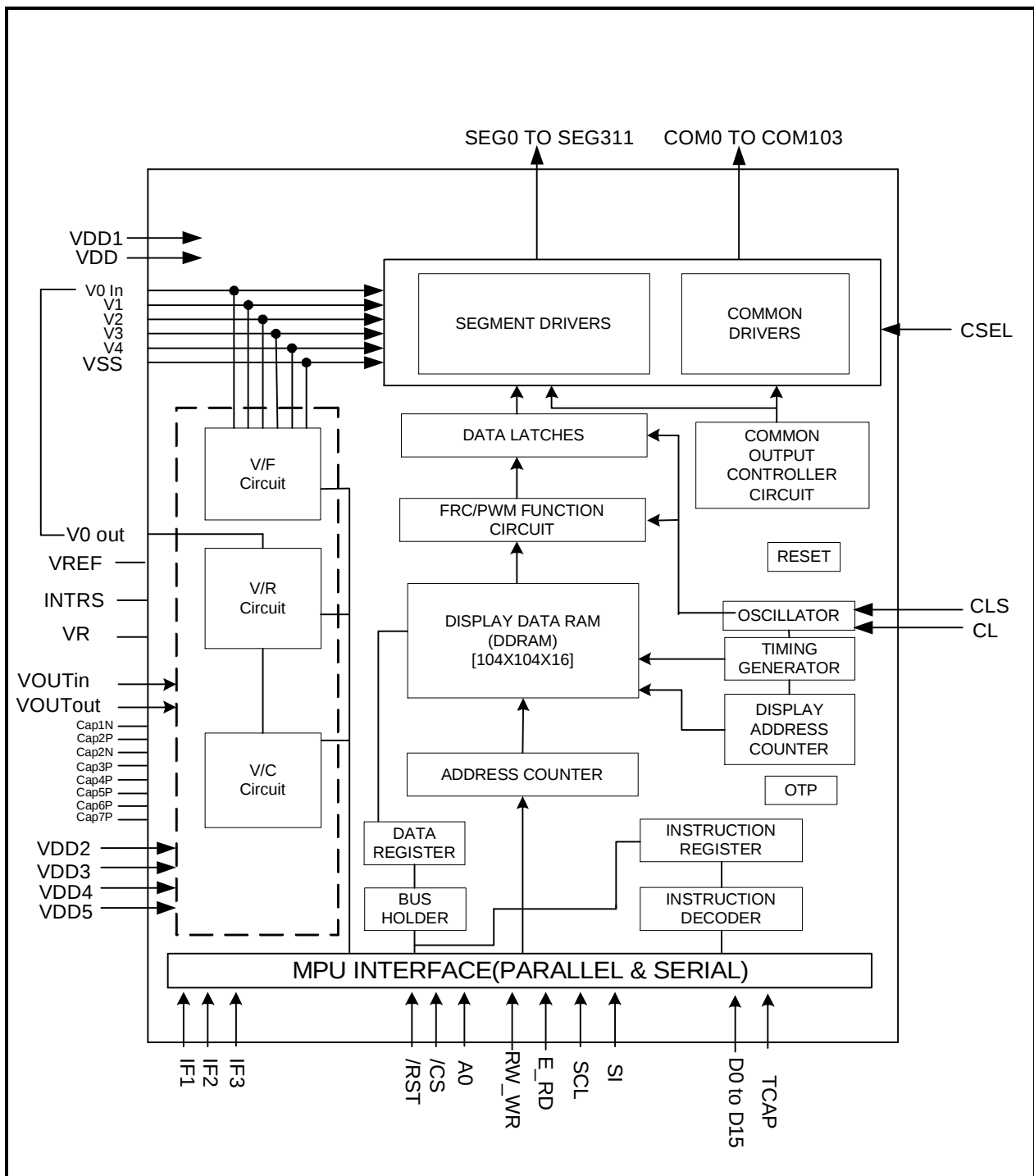
PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
454	V3		-2695.58	-671.0
455	V4		-2585.58	-671.0
456	VR		-2475.58	-671.0
457	VREF		-2365.58	-671.0
458	VDD		-2255.58	-671.0
459	CL		-2145.58	-671.0
460	CLS		-2035.58	-671.0
461	VSS		-1925.58	-671.0
462	VDD		-1815.58	-671.0
463	A0		-1705.58	-671.0
464	RW_WR		-1595.58	-671.0
465	VSS		-1485.58	-671.0
466	VDD		-1375.58	-671.0
467	D0		-1265.58	-671.0
468	D1		-1155.58	-671.0
469	D2		-1045.58	-671.0
470	D3		-935.58	-671.0
471	D4		-825.58	-671.0
472	D5		-715.58	-671.0
473	D6		-605.58	-671.0
474	D7		-495.58	-671.0
475	VSS		-385.58	-671.0
476	VDD		-275.58	-671.0
477	D8		-165.58	-671.0
478	D9		-55.58	-671.0
479	D10		54.42	-671.0
480	D11		164.42	-671.0
481	D12		274.42	-671.0
482	D13		384.42	-671.0
483	D14		494.42	-671.0
484	D15		604.42	-671.0
485	VSS		714.42	-671.0
486	VDD		824.42	-671.0
487	E_RD		934.42	-671.0
488	RST		1044.42	-671.0

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PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
489	VSS		1154.42	-671.0
490	VDD		1264.42	-671.0
491	CSEL		1374.42	-671.0
492	INTRS		1484.42	-671.0
493	IF1		1594.42	-671.0
494	IF2		1704.42	-671.0
495	IF3		1814.42	-671.0
496	VSS		1924.42	-671.0
497	VDD		2034.42	-671.0
498	SI		2144.42	-671.0
499	SCL		2254.42	-671.0
500	/CS		2364.42	-671.0
501	VDD		2474.42	-671.0
502	VDD		2584.42	-671.0
503	VDD		2694.42	-671.0
504	VDD		2804.42	-671.0
505	VDD1		2914.42	-671.0
506	VSS		3024.42	-671.0
507	VSS		3134.42	-671.0
508	VSS		3244.42	-671.0
509	VSS		3354.42	-671.0
510	VSS		3464.42	-671.0
511	VSS		3574.42	-671.0
512	VSS		3684.42	-671.0
513	VSS		3794.42	-671.0
514	VSS		3904.42	-671.0
515	VSS		4014.42	-671.0
516	VSS		4124.42	-671.0
517	VSS		4234.42	-671.0
518	VSS		4344.42	-671.0
519	VSS		4454.42	-671.0
520	VDD4		4564.42	-671.0
521	VDD3		4674.42	-671.0
522	VDD3		4784.42	-671.0

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
523	VDD2		4894.42	-671.0
524	VDD2		5004.42	-671.0
525	VDD2		5114.42	-671.0
526	VDD2		5224.42	-671.0
527	VDD2		5334.42	-671.0
528	VDD2		5444.42	-671.0
529	VDD5		5554.42	-671.0
530	VDD5		5664.42	-671.0
531	VDD5		5774.42	-671.0
532	VDD5		5884.42	-671.0
533	TCAP		5994.42	-671.0
534	CAP2P		6104.42	-671.0
535	CAP2N		6214.42	-671.0
536	CAP6P		6324.42	-671.0
537	CAP2N		6434.42	-671.0
538	CAP4P		6544.42	-671.0
539	CAP7P		6654.42	-671.0
540	CAP1N		6764.42	-671.0
541	CAP5P		6874.42	-671.0
542	CAP3P		6984.42	-671.0
543	CAP1N		7094.42	-671.0
544	CAP1P		7204.42	-671.0
545	VOUT _{IN}		7314.42	-671.0
546	VOUT _{IN}		7424.42	-671.0
547	VOUT _{IN}		7534.42	-671.0
548	VOUT _{IN}		7644.42	-671.0
549	VOUT _{IN}		7754.42	-671.0
550	VOUT _{IN}		7864.42	-671.0
551	VOUT _{OUT}		7974.42	-671.0
552	VOUT _{OUT}		8084.42	-671.0
553	VOUT _{OUT}		8194.42	-671.0
554	VOUT _{OUT}		8304.42	-671.0
555	VOUT _{OUT}		8414.42	-671.0
556	VOUT _{OUT}		8524.42	-671.0

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 POWER SUPPLY

Name	I/O	Description										
VDD	Supply	Power supply for logic circuit										
VDD1	Supply	Power supply for OSC circuit										
VDD2	Supply	Power supply for Booster Circuit										
VDD3	Supply	Power supply for LCD.										
VDD4	Supply	Power supply for LCD.										
VDD5	Supply	Power supply for LCD.										
VSS	Supply	Ground. Ground system should be connected together.										
VOUT _{OUT}	Supply	If the internal voltage generator is used, the VOUT _{IN} & VOUT _{OUT} must be connected together. If an external supply is used, this pin must be left open.										
VOUT _{IN}	Supply	An external LCD supply voltage can be supplied using the VOUT _{IN} pad. In this case, VOUT _{OUT} has to be left open, and the internal voltage generator has to be programmed to zero. (SET register VC=0)										
V0In V0out V1 V2 V3 V4	I/O	LCD driver supply voltages The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. V0In & V0out should be connected together. Voltages should have the following relationship; $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$ When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias. <table><tr><th>LCD bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr><tr><td>1/N bias</td><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr></table> NOTE: N = 5 to 12	LCD bias	V1	V2	V3	V4	1/N bias	(N-1) / N x V0	(N-2) / N x V0	(2/N) x V0	(1/N) x V0
LCD bias	V1	V2	V3	V4								
1/N bias	(N-1) / N x V0	(N-2) / N x V0	(2/N) x V0	(1/N) x V0								

6.2 LCD Power Supply Pins

Pin Name	I/O	Function
CAP1P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
CAP1N	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.
CAP2P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
CAP2N	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.
CAP3P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
CAP4P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
CAP5P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.

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CAP6P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
CAP7P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
VREF	O	Reference voltage output for monitor only. Left it open.

6.3 SYSTEM CONTROL

Name	I/O	Description
CLS	I	When using internal clock oscillator, connect CLS to VDD. When using external clock oscillator, connect CLS to VSS.
CL	I/O	When using internal clock oscillator, it's oscillator output. When using external clock oscillator, it's clock input.
INTRS	I	This terminal selects the resistors for the V0 voltage level adjustment. INTRS = "H": Use the internal resistors
VR	I	No use. Left it open.
CSEL	I	Select Common output direction. CSEL="L", COM0~COM51 is in one side, COM52~COM103 is in the opposite side. CSEL="H", COM2n(even number) is in the one side, COM2n+1 (odd number) is in the opposite side. Reference "Pad Center Coordinates"
TCAP	I/O	Test pin. Left it open.

6.4 MICROPROCESSOR INTERFACE

Name	I/O	Description																												
RST	I	Reset input pin When RST is “L”, initialization is executed.																												
IF[3:1]	I	Parallel / Serial data input select input <table><tr><th>IF1</th><th>IF2</th><th>IF3</th><th>MPU interface type</th></tr><tr><td>H</td><td>H</td><td>H</td><td>80 series 16-bit parallel</td></tr><tr><td>H</td><td>H</td><td>L</td><td>80 series 8-bit parallel</td></tr><tr><td>H</td><td>L</td><td>L</td><td>68 series 16-bit parallel</td></tr><tr><td>L</td><td>H</td><td>H</td><td>68 series 8-bit parallel</td></tr><tr><td>L</td><td>L</td><td>H</td><td>9-bit serial (3 line)</td></tr><tr><td>L</td><td>L</td><td>L</td><td>8-bit serial (4 line)</td></tr></table>	IF1	IF2	IF3	MPU interface type	H	H	H	80 series 16-bit parallel	H	H	L	80 series 8-bit parallel	H	L	L	68 series 16-bit parallel	L	H	H	68 series 8-bit parallel	L	L	H	9-bit serial (3 line)	L	L	L	8-bit serial (4 line)
IF1	IF2	IF3	MPU interface type																											
H	H	H	80 series 16-bit parallel																											
H	H	L	80 series 8-bit parallel																											
H	L	L	68 series 16-bit parallel																											
L	H	H	68 series 8-bit parallel																											
L	L	H	9-bit serial (3 line)																											
L	L	L	8-bit serial (4 line)																											
/CS	I	Chip select input pins Data/instruction I/O is enabled only when /CS is "L". When chip select is non-active, D0 to D15 become high impedance while parallel interface.																												
A0	I	Register select input pin – A0 = "H": D0 to D15 or SI are display data																												

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		– A0 = "L": D0 to D15 or SI are control data In 3-line interface contact A0 to VSS or VDD, do not let it floating.									
RW_WR	I	Read / Write execution control pin <table border="1"> <thead> <tr> <th>MPU type</th><th>RW_WR</th><th>Description</th></tr> </thead> <tbody> <tr> <td>6800-series</td><td>RW</td><td> Read / Write control input pin RW = "H" : read RW = "L" : write </td></tr> <tr> <td>8080-series</td><td>/WR</td><td> Write enable clock input pin The data on D0 to D15 are latched at the rising edge of the /WR signal. </td></tr> </tbody> </table> When in serial interface, must contact it to VSS or VDD.	MPU type	RW_WR	Description	6800-series	RW	Read / Write control input pin RW = "H" : read RW = "L" : write	8080-series	/WR	Write enable clock input pin The data on D0 to D15 are latched at the rising edge of the /WR signal.
MPU type	RW_WR	Description									
6800-series	RW	Read / Write control input pin RW = "H" : read RW = "L" : write									
8080-series	/WR	Write enable clock input pin The data on D0 to D15 are latched at the rising edge of the /WR signal.									
E_RD	I	Read / Write execution control pin <table border="1"> <thead> <tr> <th>MPU Type</th><th>E_RD</th><th>Description</th></tr> </thead> <tbody> <tr> <td>6800-series</td><td>E</td><td> Read / Write control input pin RW = "H": When E is "H", D0 to D15 are in an output status. RW = "L": The data on D0 to D15 are latched at the falling edge of the E signal. </td></tr> <tr> <td>8080-series</td><td>/RD</td><td> Read enable clock input pin When /RD is "L", D0 to D15 are in an output status. </td></tr> </tbody> </table> When in serial interface, must contact it to VSS or VDD.	MPU Type	E_RD	Description	6800-series	E	Read / Write control input pin RW = "H": When E is "H", D0 to D15 are in an output status. RW = "L": The data on D0 to D15 are latched at the falling edge of the E signal.	8080-series	/RD	Read enable clock input pin When /RD is "L", D0 to D15 are in an output status.
MPU Type	E_RD	Description									
6800-series	E	Read / Write control input pin RW = "H": When E is "H", D0 to D15 are in an output status. RW = "L": The data on D0 to D15 are latched at the falling edge of the E signal.									
8080-series	/RD	Read enable clock input pin When /RD is "L", D0 to D15 are in an output status.									

Name	I/O	Description
D15 to D0	I/O	They connect to the standard 8-bit or 16 bit MPU bus via the 8/16 –bit bi-directional bus. When the following interface is selected and the /CS pin is high, the following pins become high impedance. 8-bit parallel: D15-D8 are in the state of high impedance, should contact to "H" or "L" level. - Serial interface: D15-D0 are in the state of high impedance, should contact to "H" or "L" level.
SI	I	This pin is used to input serial data when the serial interface is selected.(3 line and 4 line) When not use contact it to VSS or VDD.
SCL	I	This pin is used to input serial clock when the serial interface is selected. The data is converted in the rising edge. (3 line and 4 line) When not use contact it to VSS or VDD.

NOTE: Microprocessor interface pins should not be floating in any operation mode.

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6.6 LCD DRIVER OUTPUTS

Name	I/O	Description																										
SEG0 to SEG311	O	LCD segment driver outputs The display data and the M signal control the output voltage of segment driver.																										
		<table><tr><th rowspan="2">Display data</th><th rowspan="2">M (Internal)</th><th colspan="2">Segment driver output voltage</th></tr><tr><th>Normal display</th><th>Reverse display</th></tr><tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr><tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr><tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr><tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr><tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr></table>	Display data	M (Internal)	Segment driver output voltage		Normal display	Reverse display	H	H	V0	V2	H	L	VSS	V3	L	H	V2	V0	L	L	V3	VSS	Power save mode		VSS	VSS
		Display data			M (Internal)	Segment driver output voltage																						
			Normal display	Reverse display																								
		H	H	V0	V2																							
		H	L	VSS	V3																							
		L	H	V2	V0																							
		L	L	V3	VSS																							
Power save mode		VSS	VSS																									
COM0 to COM103	O	LCD common driver outputs The internal scanning data and M signal control the output voltage of common driver.																										
		<table><tr><th>Scan data</th><th>M (Internal)</th><th>Common driver output voltage</th></tr><tr><td>H</td><td>H</td><td>VSS</td></tr><tr><td>H</td><td>L</td><td>V0</td></tr><tr><td>L</td><td>H</td><td>V1</td></tr><tr><td>L</td><td>L</td><td>V4</td></tr><tr><td colspan="2">Power save mode</td><td>VSS</td></tr></table>	Scan data	M (Internal)	Common driver output voltage	H	H	VSS	H	L	V0	L	H	V1	L	L	V4	Power save mode		VSS								
		Scan data	M (Internal)	Common driver output voltage																								
		H	H	VSS																								
		H	L	V0																								
		L	H	V1																								
		L	L	V4																								
Power save mode		VSS																										

ST7624 I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
INTRS,IF[3:1],CLS,CSEL	No Limitation
VREF, TCAP	Floating
Vdd, Vdd1~Vdd5, Vss, VOUT _{IN} , VOUT _{OUT} ,V0in,V0out,CL,VR	<100Ω
V0in,V0out,V1,V2, V3, V4 CAP1P,CAP1N,CAP2P,CAP2N,CAP3P,CAP4P,CAP5P,CAP6P,CAP7P	<100Ω
A0, RW_WR, E_RD, /CS, D0 ...D15, SCL, SI	<1KΩ
RST	<10KΩ

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7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

There is /CS pin for chip selection. The ST7624 can interface with an MPU when /CS is "L". In case of serial interface, the internal shift register and the counter are reset.

7.1.1 Selecting Parallel / Serial Interface

ST7624 has seven types of interface with an MPU, which are three serial and four parallel interfaces. This parallel or serial interface is determined by IF pin as shown in table 7.1.1.

Table 7.1.1 Parallel / Serial Interface Mode

IF1	IF2	IF3	Interface type	/CS	A0	/RD(E)	/WR(R/W)	D15 to D8	D7 to D0	SI	SCL
H	H	H	80 serial 16-bit parallel	/CS	A0	/RD	/WR	D15 to D8	D7 to D0	--	--
H	H	L	80 serial 8-bit parallel	/CS	A0	/RD	/WR	--	D7 to D0	--	--
H	L	L	68 serial 16-bit parallel	/CS	A0	E	R/W	D15 to D8	D7 to D0	--	--
L	H	H	68 serial 8-bit parallel	/CS	A0	E	R/W	--	D7 to D0	--	--
L	L	H	9-bit SPI mode (3 line)	/CS	--	--	--	--	--	SI	SCL
L	L	L	8-bit SPI mode (4 line)	/CS	A0	--	--	--	--	SI	SCL

--:Must be fixed to either H or L.

NOTE: When these pins are set to any other combination, A0, E_RD, and RW_WR inputs are disabled and D0 to D15 are to be high impedance.

7.1.2 8- or 16-bit Parallel Interface

The ST7624 identifies type of the data bus signals according to combinations of A0, /RD (E) and /WR (W/R) signals, as shown in table 7.1.2.

Table 7.1.2 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	R/W	E	/RD	/WR	
H	H	H	L	H	Display data read out
H	L	H	H	L	Display data write
L	H	H	L	H	Register status read
L	L	H	H	L	Writes to internal register (instruction)

Relation between Data Bus and Gradation Data

ST7624 offers the 65K color display, dithered 262K color display, and dithered 16M color display.

When using 65K, 262K, and 16M color, you can specify color for each of R, G, B using the palette function.

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Use the command for switching between these modes.

(1) 65K color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGG 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGBBBBB 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGGGGGBBBBBB (16 bits)

Data is acquired through signal write operation and then written to the display RAM.

(2) 262K color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXX 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGXX 2nd write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBXX 3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXXGGGGGGXX

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBXXXXXXXXXXXXXXXX

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

“XXXX” are dummy bits, and they are ignored for display.

(3) 16M color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRR 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGGG 2nd write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBB 3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRRGGGGGGGG

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBBXXXXXXXX

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

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7.1.3 8- and 9-bit Serial Interface

The 8-bit serial interface uses four pins /CS, SI, SCL, and A0 to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins /CS, SI and SCL for the same purpose.

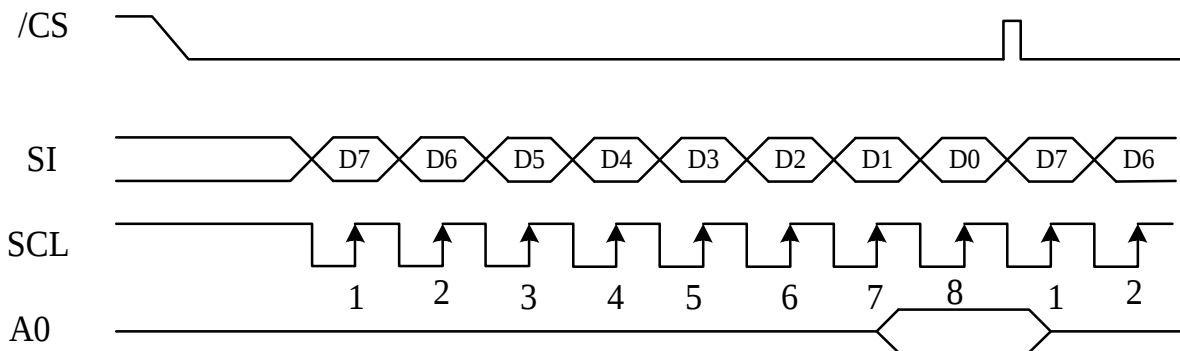
Data read is not available with the serial interface. Data entered must be 8 bits. Refer to the following chart for entering commands, parameters or gray-scale data.

The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4 line)

When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.

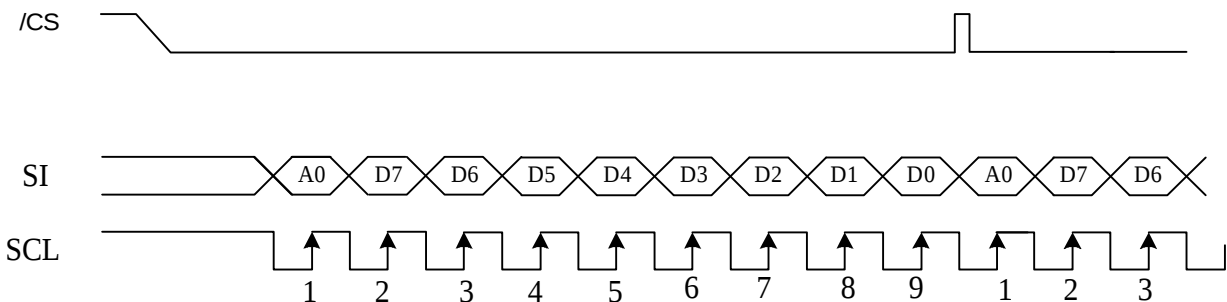
When entering command: A0= LOW at the rising edge of the 8th SCL



(2) 9-bit serial interface (3 line)

When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.

When entering command: SI= LOW at the rising edge of the 1st SCL.



- I If /CS is caused to HIGH before 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- I In order to avoid data transfer error due to incoming noise, it is recommended to set /CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.
- I When executing the command RAMWR, set /CS to HIGH after writing the last address (after starting the 9th pulse in case of 9-bit serial input or after starting the 8th pulse in case of 8-bit serial input).

7-2 ACCESS TO DDRAM AND INTERNAL REGISTERS

ST7624 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Fig. 7.2.1 illustrates these relations.

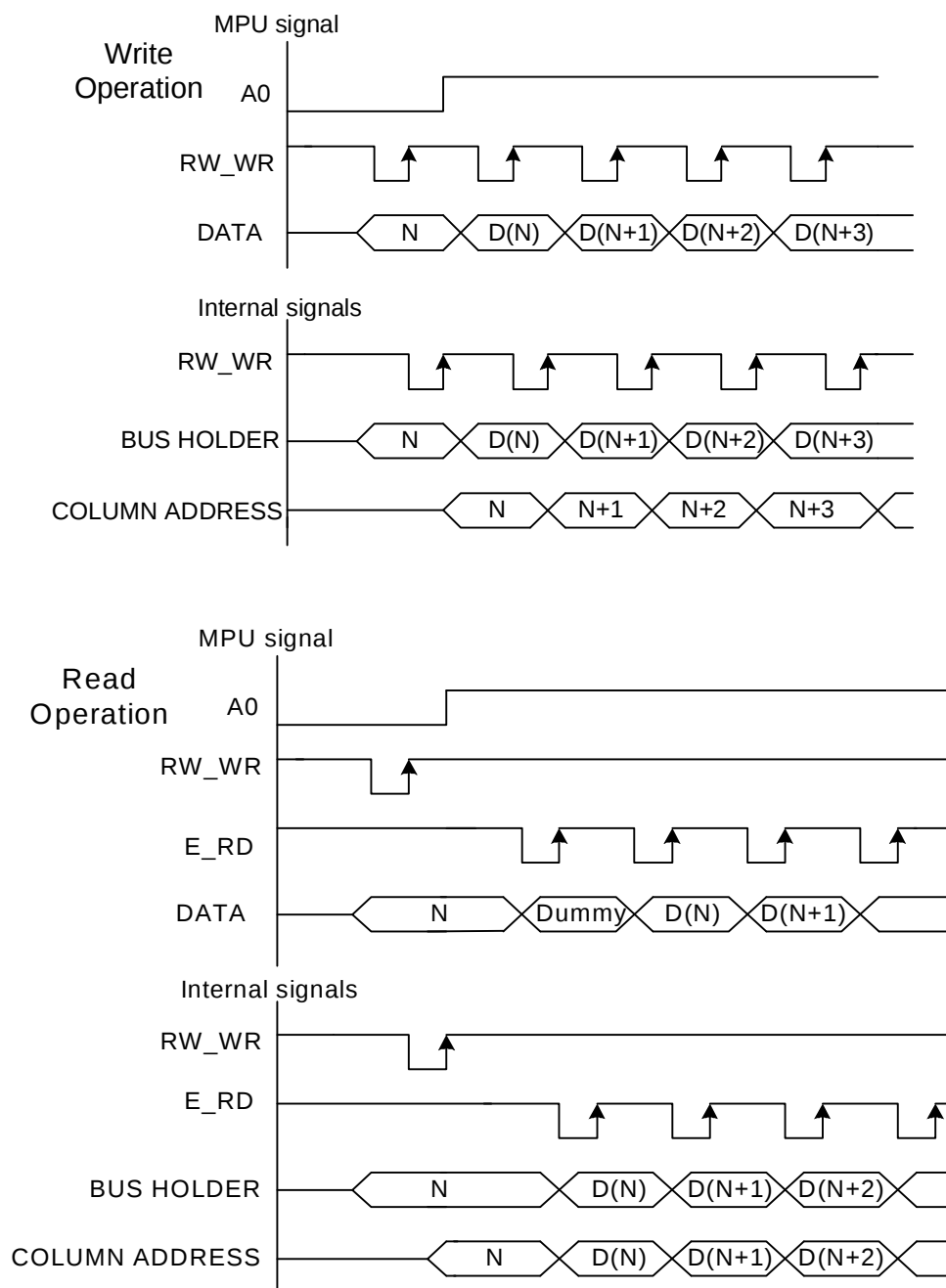


Fig 7.2.1

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7-3 DISPLAY DATA RAM (DDRAM)

7.3.1 DDRAM

It is 104 X 104 X 16 bits capacity RAM prepared for storing dot data. You can access a desired bit by specifying the page address and column address. Since display data from MCU D7 to D0 and D15 to D8 correspond to one or two pixels of RGB, data transfer related restrictions are reduced, realizing the display flexing.

The RAM on ST7624 is separated to a block per 4 lines to allow the display system to process data on the block basis.

MPU's read and write operations to and from the RAM are performed via the I/O buffer circuit; Reading of the RAM for the liquid crystal drive is controlled from another separate circuit. Refer to the following memory map for the RAM configuration.

Memory Map (When using the 65Kcolor. 8-bit mode,)

RGB alignment (Command of data control parameter2=000)														
Data control command (BCH)				Column										
LCD read direction	P11:0(DATCTL)			0		1				103				
														
	P11:1(DATCTL)			103		102				0				
														
	Color			R	G	B	R	G	B		R	G	B	
Data			D7	D2	D4	D7	D2	D4		D7	D2	D4		
Page			D6	D1	D3	D6	D1	D3		D6	D1	D3		
Block	P10:0 (DATCTL)		P10:1 (DATCTL)	D5	D0	D2	D5	D0	D2		D5	D0	D2	
				D4	D7	D1	D4	D7	D1		D4	D7	D1	
				D3	D6	D0	D3	D6	D0		D3	D6	D0	
0	0		103											
	1		102											
	2		101											
	3		100											
1	4		99											
	5		98											
	6		97											
	7		96											
24	96		7											
	97		6											
	98		5											
	99		4											
25	100	3												
	101	2												
	102	1												
	103	0												
SEGout				0	1	2	3	4	5		309	310	311	

You can change position of R and B with DATCTL command.

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Memory Map (When using the 65K color. 16-bit mode)

RGB alignment (Command of data control parameter2=000)															
Data control command (BCH)				Column											
LCD read direction	P11:0(DATCTL)			0		1				103					
															
	P11:1(DATCTL)			103		102				0					
															
	Color			R	G	B	R	G	B		R	G	B		
Data			D15	D10	D4	D15	D10	D4		D15	D10	D4			
Page			D14	D9	D3	D14	D9	D3		D14	D9	D3			
Block	P10:0 (DATCTL)		P10:1 (DATCTL)		D13	D8	D2	D13	D8	D2		D13	D8	D2	
					D12	D7	D1	D12	D7	D1		D12	D7	D1	
					D11	D6	D0	D11	D6	D0		D11	D6	D0	
0	0		103												
	1		102												
	2		101												
	3		100												
1	4		99												
	5		98												
	6		97												
	7		96												
24	96		7												
	97		6												
	98		5												
	99	4													
25	100	3													
	101	2													
	102	1													
	103	0													
SEGout				0	1	2	3	4	5		309	310	311		

You can change position of R and B with DATCTL command.

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Memory Map (When using the 262K color. 8-bit mode,)

RGB alignment (Command of data control parameter2=000)														
Data control command (BCH)				Column										
LCD read direction	P11:0(DATCTL)			0		1				103				
														
	P11:1(DATCTL)			103		102				0				
														
	Color			R	G	B	R	G	B		R	G	B	
Data			D7	D7	D7	D7	D7	D7		D7	D7	D7		
Page			D6	D6	D6	D6	D6	D6		D6	D6	D6		
Block	P10:0 (DATCTL)		P10:1 (DATCTL)		D5	D5	D5	D5	D5	D5		D5	D5	D5
					D4	D4	D4	D4	D4	D4		D4	D4	D4
					D3	D3	D3	D3	D3	D3		D3	D3	D3
					D2	D2	D2	D2	D2	D2		D2	D2	D2
0	0		103											
	1													
	2													
	3													
1	4				99									
	5				98									
	6				97									
	7				96									
24	96				7									
	97		6											
	98		5											
	99		4											
25	100		3											
	101		2											
	102		1											
	103		0											
SEGout				0	1	2	3	4	5		309	310	311	

You can change position of R and B with DATCTL command.

ST7624

Memory Map (When using the 262K color. 16-bit mode)

RGB alignment (Command of data control parameter2=000)																
Data control command (BCH)					Column											
LCD read direction	P11:0(DATCTL)				0		1				103					
																
	P11:1(DATCTL)				103		102				0					
																
Color					R	G	B	R	G	B		R	G	B		
Data					D15	D7	D15	D15	D7	D15		D15	D7	D15		
					D14	D6	D14	D14	D6	D14		D14	D6	D14		
Block	P10:0 (DATCTL)		P10:1 (DATCTL)		D13	D5	D13	D13	D5	D13		D13	D5	D13		
					D12	D4	D12	D12	D4	D12		D12	D4	D12		
					D11	D3	D11	D11	D3	D11		D11	D3	D11		
					D10	D2	D10	D10	D2	D10		D10	D2	D10		
0	0		103													
	1		102													
	2		101													
	3		100													
1	4		99													
	5		98													
	6		97													
	7		96													
24	96		7													
	97		6													
	98		5													
	99		4													
25	100		3													
	101		2													
	102		1													
	103		0													
SEGout					0	1	2	3	4	5		309	310	311		

You can change position of R and B with DATCTL command.

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Memory Map (When using the 16M color. 8-bit mode,)

RGB alignment (Command of data control parameter2=000)															
Data control command (BCH)				Column											
LCD read direction	P11:0(DATCTL)			0			1			103					
															
	P11:1(DATCTL)			103			102			0					
															
	Color			R	G	B	R	G	B		R	G	B		
Data			D7	D7	D7	D7	D7	D7		D7	D7	D7			
Page			D6	D6	D6	D6	D6	D6		D6	D6	D6			
Block	P10:0 (DATCTL)		P10:1 (DATCTL)	D5	D5	D5	D5	D5	D5		D5	D5	D5		
				D4	D4	D4	D4	D4	D4		D4	D4	D4		
				D3	D3	D3	D3	D3	D3		D3	D3	D3		
				D2	D2	D2	D2	D2	D2		D2	D2	D2		
				D1	D1	D1	D1	D1	D1		D1	D1	D1		
				D0	D0	D0	D0	D0	D0		D0	D0	D0		
0	0		103												
	1		102												
	2		101												
	3		100												
1	4		99												
	5		98												
	6		97												
	7		96												
24	96		7												
	97		6												
	98		5												
	99		4												
25	100	3													
	101	2													
	102	1													
	103	0													
SEGout				0	1	2	3	4	5		309	310	311		

You can change position of R and B with DATCTL command.

ST7624

Memory Map (When using the 16M color, 16-bit mode)

RGB alignment (Command of data control parameter2=000)																		
Data control command (BCH)					Column													
LCD read direction	P11:0(DATCTL)				0		1				103							
																		
	P11:1(DATCTL)				103		102				0							
																		
	Color				R	G	B	R	G	B		R	G	B				
Data				D15	D7	D15	D15	D7	D15		D15	D7	D15					
Page				D14	D6	D14	D14	D6	D14		D14	D6	D14					
Block	P10:0 (DATCTL)		P10:1 (DATCTL)		D13	D5	D13	D13	D5	D13		D13	D5	D13				
					D12	D4	D12	D12	D4	D12		D12	D4	D12				
					D11	D3	D11	D11	D3	D11		D11	D3	D11				
					D10	D2	D10	D10	D2	D10		D10	D2	D10				
					D9	D1	D9	D9	D1	D9		D9	D1	D9				
					D8	D0	D8	D8	D0	D8		D8	D0	D8				
					0	0		103										
						1		102										
2	101																	
3	100																	
1	4	99																
	5	98																
	6	97																
	7	96																
24	96		7															
	97		6															
	98		5															
	99		4															
25	100		3															
	101		2															
	102		1															
	103		0															
SEGout					0	1	2	3	4	5		309	310	311				

You can change position of R and B with DATCTL command.

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7.3.2 Page Address Control Circuit

This circuit is used to control the address in the page direction when MPU accesses the DDRAM or when reading the DDRAM to display image on the LCD.

You can specify a scope of the page address with page address set command. When the page-direction scan is specified with DATCTL command and the address are incremented from the start up to the end page, the column address is incremented by 1 and the page address returns to start page.

The DDRAM supports up to 104 lines, and thus the total page becomes 104.

In the read operation, as the end page is reached, the column address is automatically incremented by 1 and the page address is returned to start page.

Using the address normal/reverse parameter of DATCTL command allows you to reverse the correspondence between the DDRAM address and command output.

7.3.3 Column Address Control Circuit

This circuit is used to control the address in the column direction when MPU accesses the DDRAM. You can specify a scope of the column address using column address set command. When the column-direction scan is specified with DATCTL command and the address are incremented from the start up to the end page, the page address is incremented by 1 and the column address returns to start column.

In the read operation, too, the column address is automatically incremented by 1 and returned to start page as the end column is reached.

Just like the page address control circuit, using the column address normal/reverse parameter of DATCTL command enables to reverse the correspondence between the DDRAM column address and segment output. This arrangement relaxes restrictions in the chip layout on the LCD module.

7.3.4 I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM while the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.5 Block Address Circuit

The circuit associates pages on DDRAM with COM output. ST7624 processes signals for the liquid crystal display on 4-page basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in block.

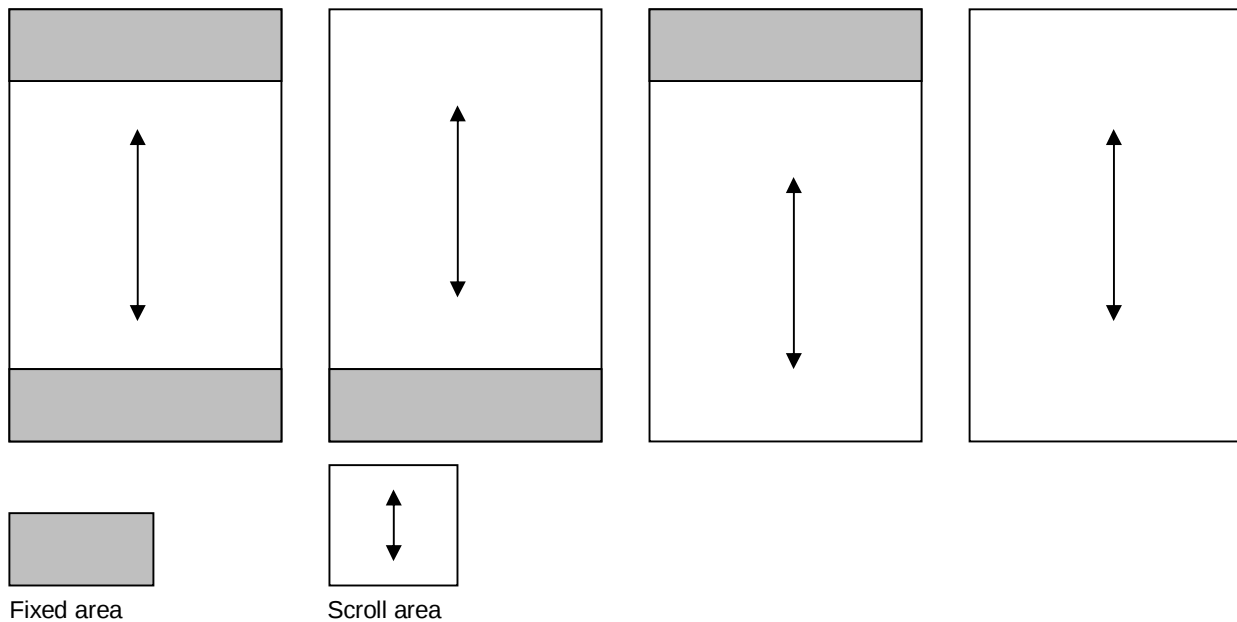
7.3.6 Display data Latch Circuit

This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

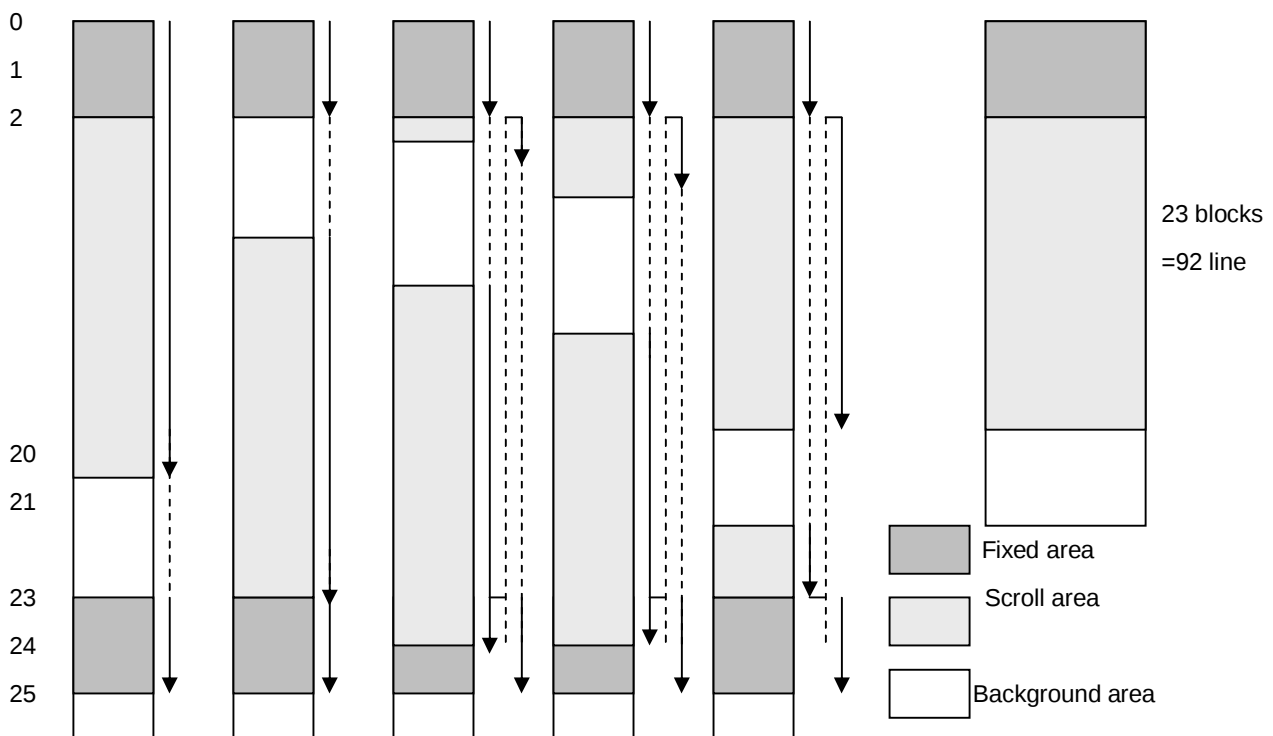
ST7624

7.4 Area Scroll Display

Using area scroll set and scroll start set commands allows you to scroll the display screen partially. You can select any one of the following four scroll patterns.



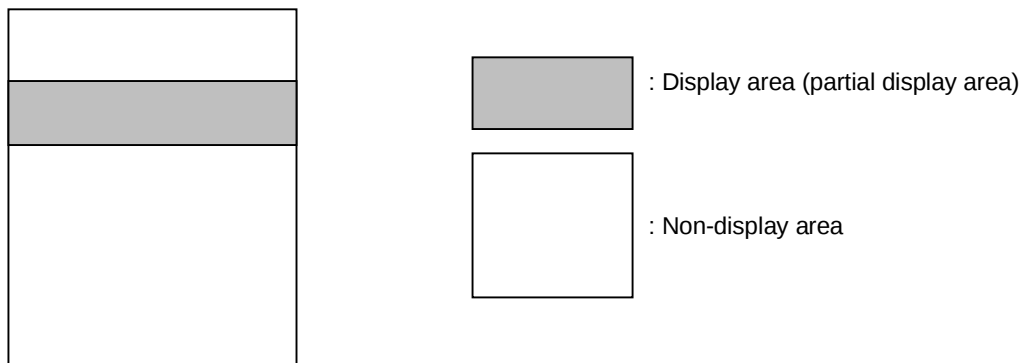
DDRAM



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7.5 Partial Display

Using partial in command allows you turn on the partial display (division by line) of the screen. This mode requires less current consumption than the whole screen display, making it suitable for the equipment in the standby state.



If the partial display region is out of the Max. Display range, it would be no operation

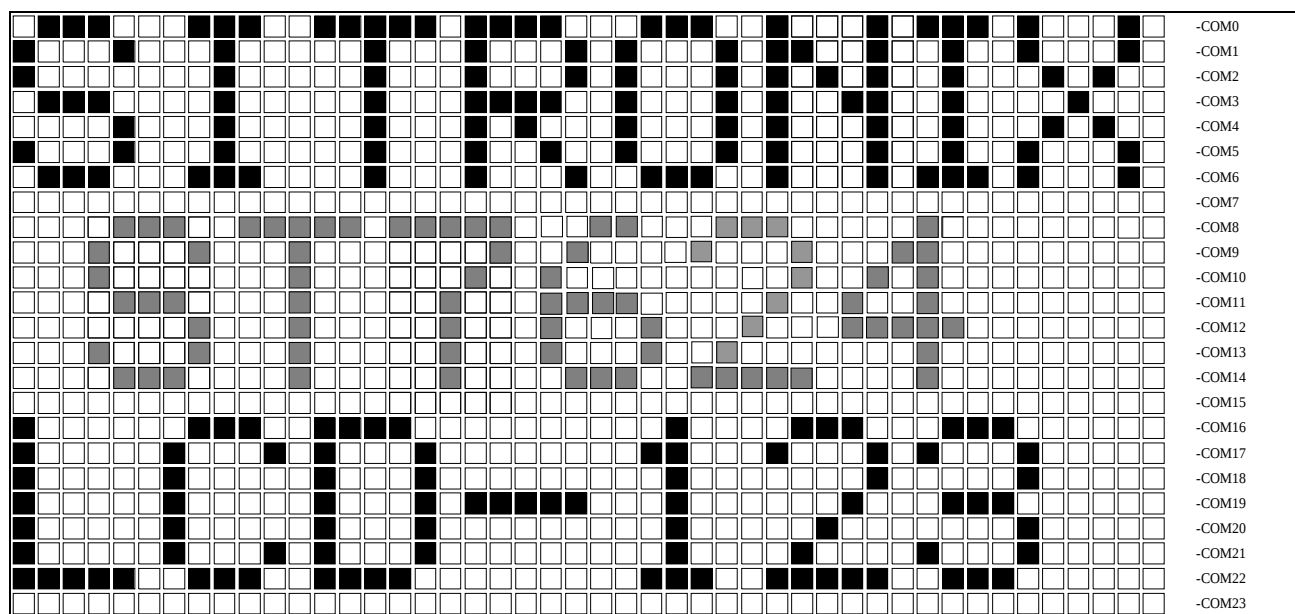


Figure 7.5.1.Reference Example for Partial Display

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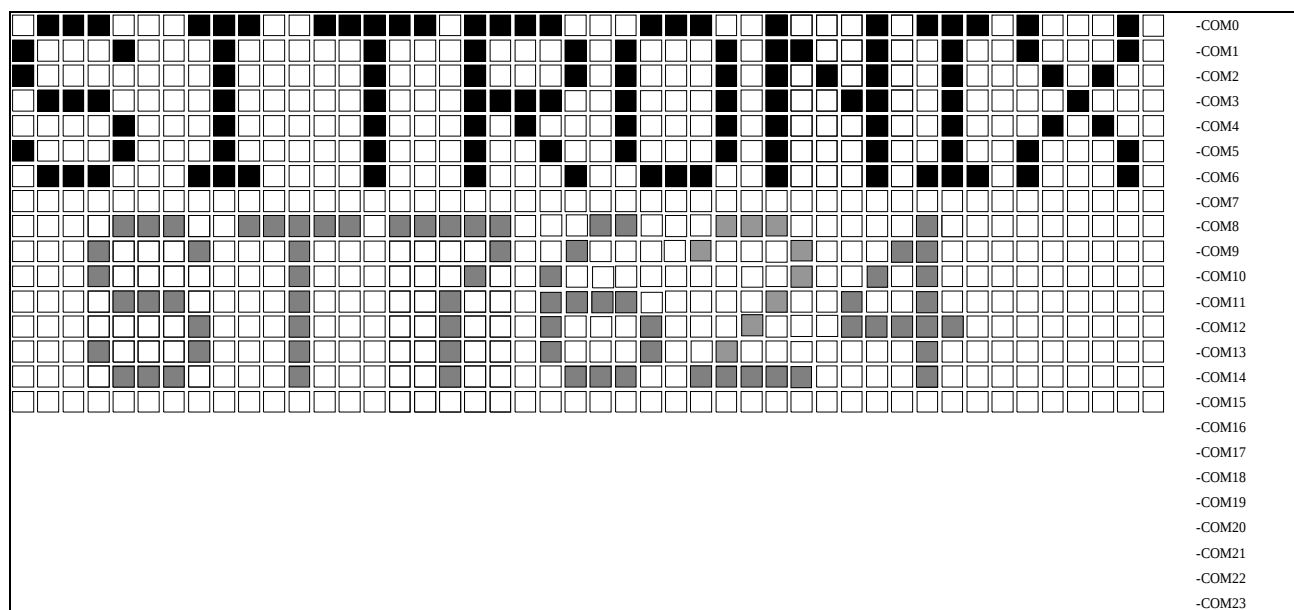


Figure 7.5.2. Partial Display (Partial Display Duty=16, initial COM0=0)

7.6 Gray-Scale Display

ST7624 incorporates a 4FRC & 31 PWM function circuit to display a 64 gray-scale display.

7.7 Oscillation circuit

This is on-chip Oscillator without external resistor. When the internal oscillator is used, CLS must connect to VDD; when the external oscillator is used, CL could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.8 Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 104-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.8.1.

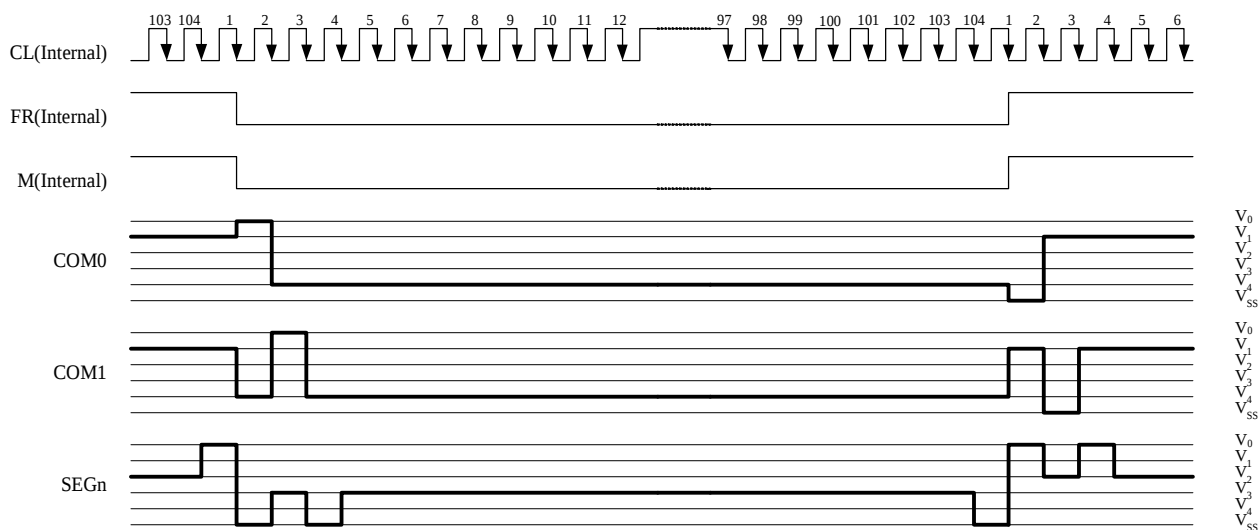


Figure 7.8.1 2-frame AC Driving Waveform (Duty Ratio: 1/104)

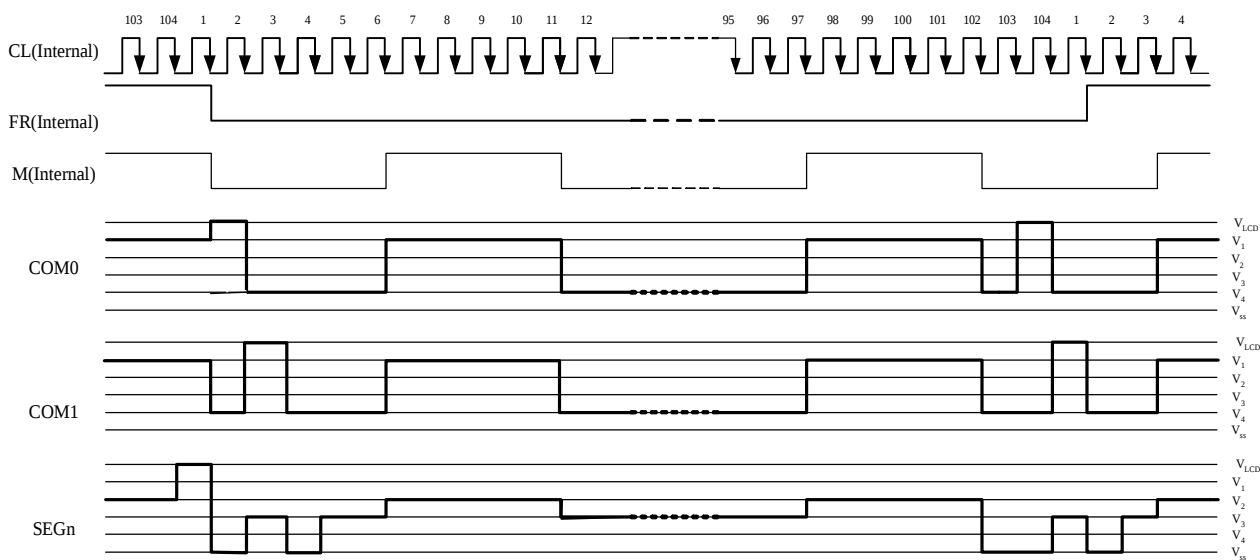
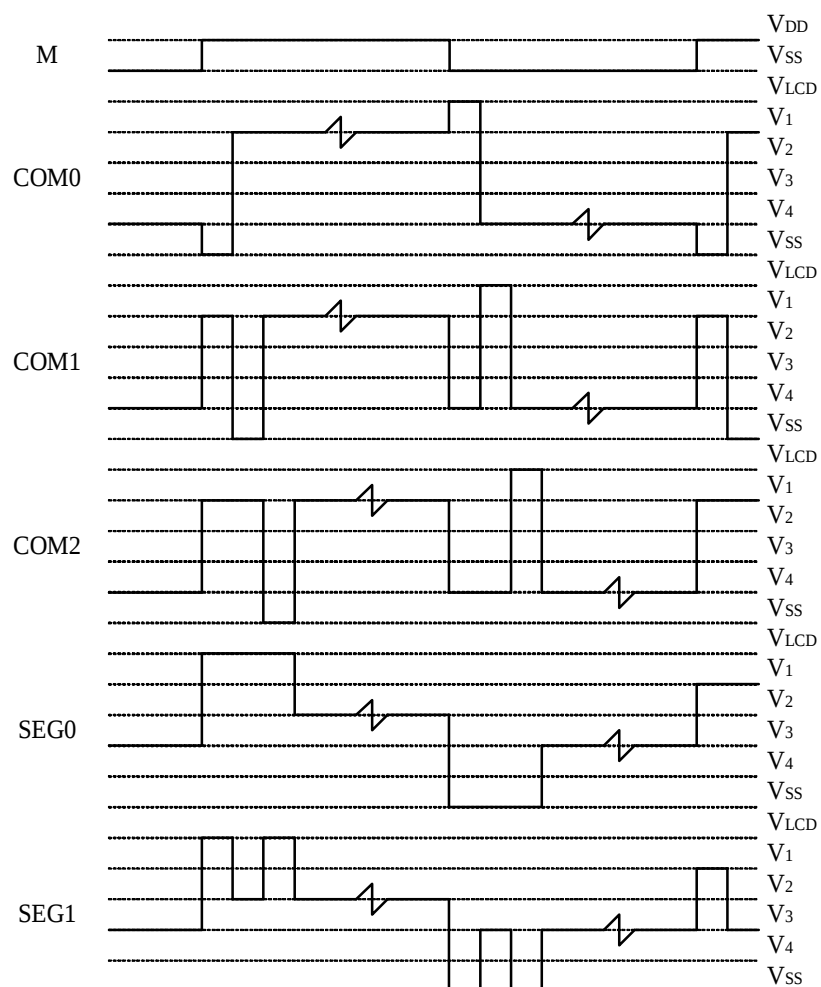
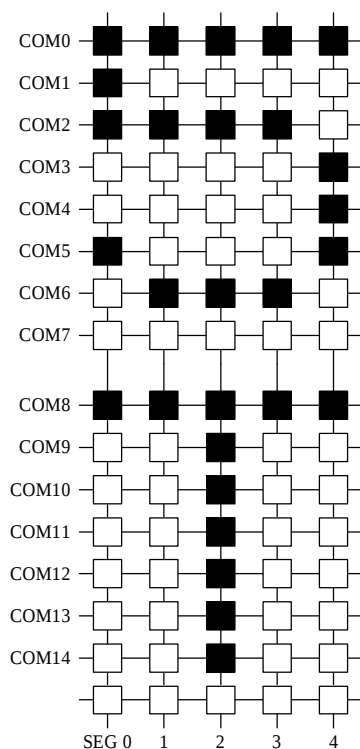


Figure 7.8.2 N-Line Inversion Driving Waveform (N=5, Duty Ratio=1/104)

7.9 Liquid Crystal drive Circuit

This driver circuit is configured by 104-channel common drivers and 312-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.

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7.10 Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 7.10.1 shows the referenced combinations in using Power Supply circuits.

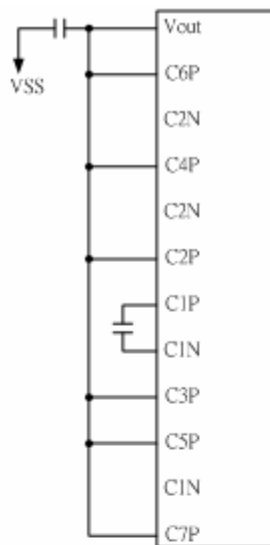
Table 7.10.1 Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

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7.10.1 Voltage Converter Circuits

The Step-up Voltage Circuits



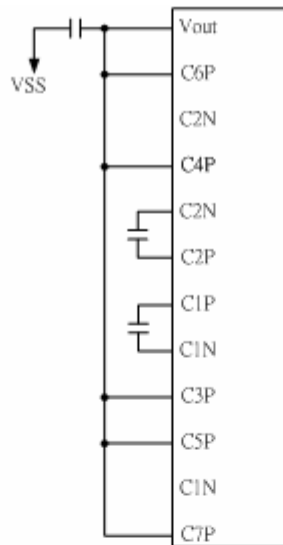
2x step-up voltage circuit

$$V_{OUT}=2 \times V_{DD2}=6V$$

$$V_{DD2}=3V$$

$$V_{SS}=0V$$

2x step-up voltage relationships



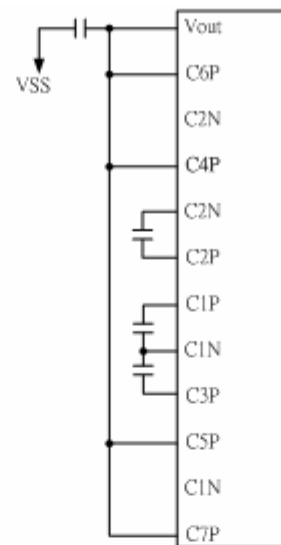
3x step-up voltage circuit

$$V_{OUT}=3 \times V_{DD2}=9V$$

$$V_{DD2}=3V$$

$$V_{SS}=0V$$

3x step-up voltage relationships



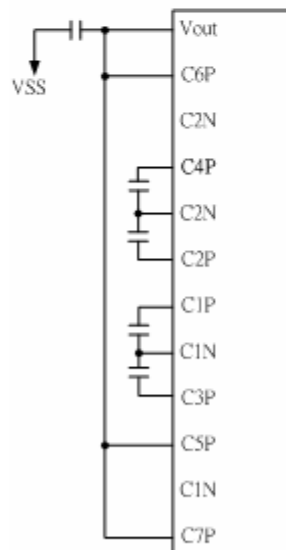
4x step-up voltage circuit

$$V_{OUT}=4 \times V_{DD2}=12V$$

$$V_{DD2}=3V$$

$$V_{SS}=0V$$

4x step-up voltage relationships



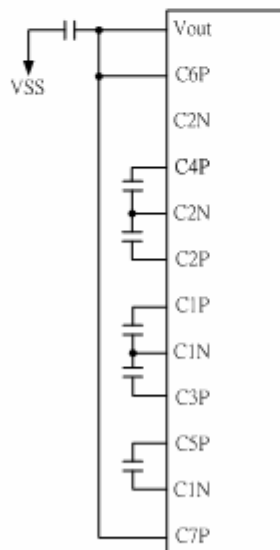
5x step-up voltage circuit

$$V_{OUT}=5 \times V_{DD2}=15V$$

$$V_{DD2}=3V$$

$$V_{SS}=0V$$

5x step-up voltage relationships



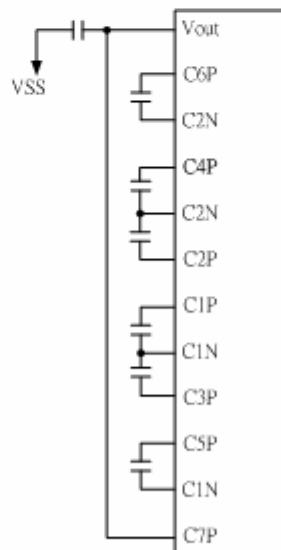
6x step-up voltage circuit

$$V_{OUT}=6 \times V_{DD2}=18V$$

$$V_{DD2}=3V$$

$$V_{SS}=0V$$

6x step-up voltage relationships



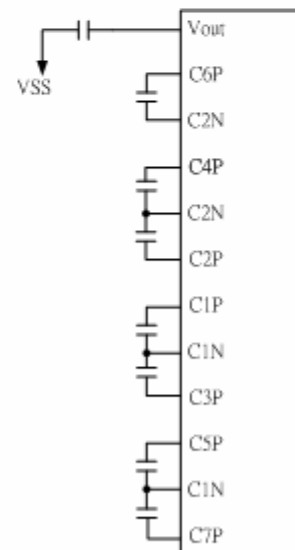
7x step-up voltage circuit

$$V_{OUT}=7 \times V_{DD2}=16.8V$$

$$V_{DD2}=2.4V$$

$$V_{SS}=0V$$

7x step-up voltage relationships



8x step-up voltage circuit

$$V_{OUT}=8 \times V_{DD2}=19.2V$$

$$V_{DD2}=2.4V$$

$$V_{SS}=0V$$

8x step-up voltage relationships

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7.10.2 Voltage Regulator Circuits

SET VOP (SETVOP)

The set VOP function is used to program the optimum LCD supply voltage V_o .

SETVOP

Reset state of Vop[8:0] is 257_{DEC} = 13.88V.

The VOP value is programmed via the Vop[8:0] register.

$$V0 = a + (Vop[8:6]Vop[5:0]) \cdot b$$

Ex: Vop[5:0]=000001, Vop[8:6]=100

→ Vop [8:0]=100000001

→ $3.6 + 257 \times 0.04 = 13.88$

- I a is a fixed constant value (see table 7.10.2).
- I b is a fixed constant value (see table 7.10.2).
- I Vop[8:0] is the programmed VOP value. The programming range for Vop[8:0] is 4 to 410 (19Ah_{hex}).
- I Vop[5:0] is the set contrast value which can be set via the interface and is in two's complement format. (See command VOLUP & VOLDOWN)

Table 7.10.2

SYMBOL	VALUE	UNIT
a	3.6	V
b	0.04	V

The VOP[8:0] value must be in the V_{LCD} programming range as given in Fig.7.10.2. Evaluating equation (1), values outside the programming range indicated in Fig.7.10.2 may result. Calculated values below VOP[8:0]=4 will be mapped to VOP[8:0]=4, resulting VOP values higher than VOP[8:0]=410 will be mapped to VOP[8:0]=410.

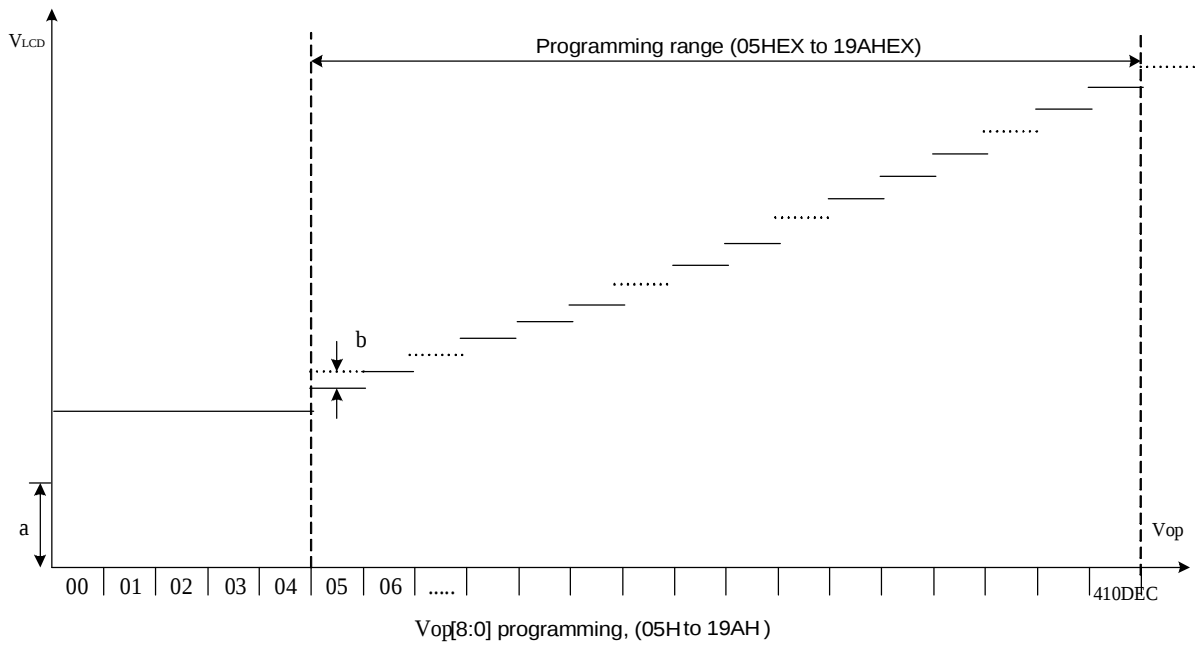


Fig. 7.10.2 VLCD programming range

As the programming range for the internally generated V_0 allows values above the max(18V). Allowed V_0 (18V) the user has to ensure while setting the VOP register and the temperature compensation, that under all conditions and including all tolerances the V_0 remains below 18V.

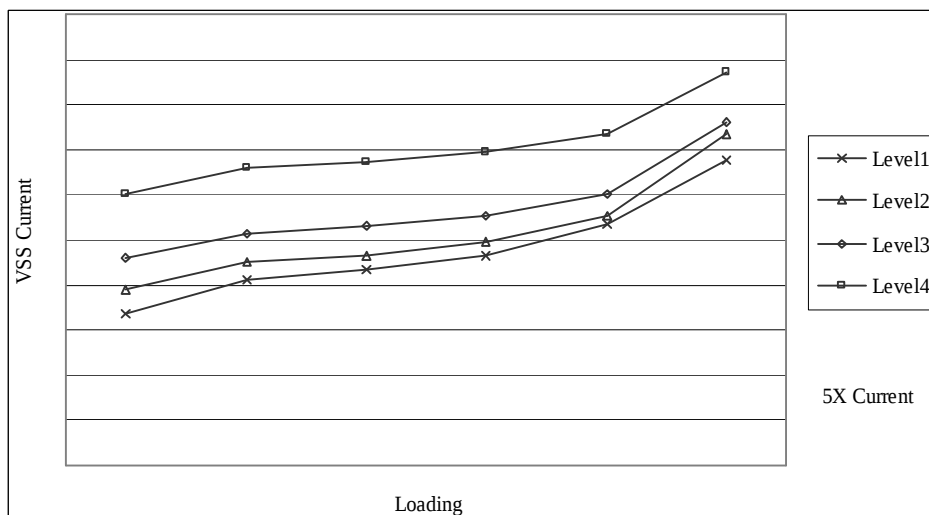
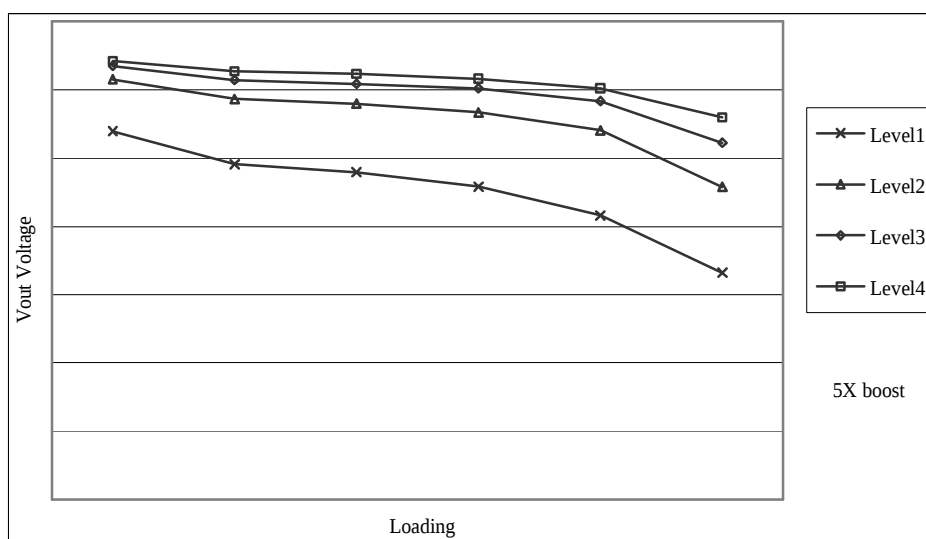
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Booster Efficiency

By Booster Stages (2X, 3X, 4X, 5X, 6X, 7X, 8X) and Booster Efficiency (Level1~4) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level4 is higher than level1), The Boost Efficiency is better than lower level, and it just needs few more power consumption current. It could be applied to each multiple voltage Condition.

When the LCD Panel loading is heavier, the performance of Booster will be not in a good working condition. Users could set the BE level to be higher and just need few more current. Never consider to change to higher Booster Stage at beginning stage unless it really necessary.

The Booster Efficiency Command could be used together with Booster Stage Command to choose one best Boost output condition. Users could see the Booster Stage Command as a large scale operation, and see the Booster Efficiency Command as a small scale operation. These commands are very convenient for using.



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RESET CIRCUIT

When Power is Turned On

Input power (VDD, VDD1~VDD5)



Be sure to apply POWER-ON RESET (RES = LOW)



<Display Setting>

Display control (DISCTL)

Setting clock dividing ratio:

Duty setting:

Setting reverse rotation number of line:

Common scan direction (COMSCN)

Setting scan direction:

Oscillation ON (OSCON)



Sleep-out (SLIPOUT)



<Power Supply Setting>

Electronic volume control (VOLCTR)

Setting volume value:

Setting built-in resistance value:

Power control (PWRCTR)

Setting operation of power supply circuit:



<Display Setting 2>

Normal rotation of display (DISNOR)/Inversion of display (DISINV): Normal rotation of display

Partial-in (PTLIN)/Partial-out (PTLOUT)

Setting fix area:

Area scroll set (ASSET)

Setting area scroll region:

Setting area scroll type:

Scroll start set (SCSTART)

Setting scroll start address:



<Display Setting 3>

Data control (DATCTL)

Setting normal rotation/reversion of page address:

Setting normal rotation/reversion of column address:

Setting direction of address scanner:

Ver 1.8

<<State after resetting>>

1 dividing

1/4

11h reverse rotations

COM0 -> COM51, COM52 -> COM103

Oscillation OFF

Sleep-in

<<State after resetting>>

0

0 (3.76)

All OFF

<<State after resetting>>

Partial-out

0

0

Full-screen scroll

0

<<State after resetting>>

Normal rotation

Normal rotation

Column direction

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Setting RGB arrangement: RGB
Setting gradation: 65K



<RAM Setting>

<<State after resetting>>

Page address set (PASET)

Setting start page address: 0

Setting end page address: 0

Column address set (CASET)

Setting start column address: 0

Setting end column address: 0



<RAM Write>

<<State after resetting>>

Memory write command (RAMWR)

Writing displayed data : Repeat as many as the number needed
and exit by entering other command.



<Waiting (approximately 100ms)>

Wait until the power supply voltage has stabilized.

Enter the power supply control command first, then wait at least
100ms before entering the display ON command when the built-in
power supply circuit operates.

If you do not wait, an unwanted display may appear on the
liquid crystal panel.



Display ON (DISON):

Display OFF

(Note) If changes are unnecessary after resetting, command input is unnecessary.

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8. COMMANDS

8.1 Command table

Ext=0																
Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter	Index	
DISON	0	1	0	1	0	1	0	1	1	1	1	Display On	AF	None	1	
DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display Off	AE	None	2	
DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal Display	A6	None	3	
DISINV	0	1	0	1	0	1	0	0	1	1	1	Inverse Display	A7	None	4	
COMSCN	0	1	0	1	0	1	1	1	0	1	1	Com Scan Direc.	BB	1 byte	5	
DISCTR	0	1	0	1	1	0	0	1	0	1	0	Display Control	CA	3 byte	6	
SLPP	0	1	0	0	0	0	0	0	1	0	0	Sleep In/Out Preparation	04	1 byte	7	
SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep In	95	None	8	
SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep Out	94	None	9	
PASET	0	1	0	0	1	1	1	0	1	0	1	Page Addr. Set	75	2 byte	10	
CASET	0	1	0	0	0	0	1	0	1	0	1	Column Addr. Set	15	2 byte	11	
DATCTL	0	1	0	1	0	1	1	1	1	0	0	Data Scan Direction	BC	3 byte	12	
RAMWR	0	1	0	0	1	0	1	1	1	0	0	Writing to Memory	5C	Data	13	
RAMRD	0	1	0	0	1	0	1	1	1	0	1	Reading from Memory	5D	Data	14	
PLTIN	0	1	0	1	0	1	0	1	0	0	0	Partial display in	A8	2 byte	15	
PLTOUT	0	1	0	1	0	1	0	1	0	0	1	Partial display out	A9	None	16	
RMWIN	0	1	0	1	1	1	0	0	0	0	0	Read and Modify Write	E0	None	17	
RMWOUT	0	1	0	1	1	1	0	1	1	1	0	RMW end	EE	None	18	
ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area Scroll Set	AA	4 byte	19	
SCSTART	0	1	0	1	0	1	0	1	0	1	1	Scroll Start Set	AB	1 byte	20	
OSCON	0	1	0	1	1	0	1	0	0	0	1	Internal OSC on	D1	None	21	
OSCOFF	0	1	0	1	1	0	1	0	0	1	0	Internal OSC off	D2	None	22	
PWRCTL	0	1	0	0	0	1	0	0	0	0	0	Power Control	20	1 byte	23	
VOLCTR	0	1	0	1	0	0	0	0	0	0	1	EC control	81	2 byte	24	
VOLUP	0	1	0	1	1	0	1	0	1	1	0	EC increase 1	D6	None	25	
VOLDOWN	0	1	0	1	1	0	1	0	1	1	1	EC decrease 1	D7	None	26	
EPSRRD1	0	1	0	0	1	1	1	1	1	0	0	READ Register1	7C	None	27	
EPSRRD2	0	1	0	0	1	1	1	1	1	0	1	READ Register2	7D	None	28	
NOP	0	1	0	0	0	1	0	0	1	0	1	NOP Instruction	25	None	29	
STREAD	0	0	1	Status Read								Status Read			30	
Initial code(1)	0	1	0	0	0	0	0	0	1	1	1	Initial code(1)	07	1 byte	31	
RESERVED	0	1	0	1	0	0	0	0	0	1	0	Not Use	82		32	

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Ext=1															
Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter	Index
Red1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 Red PWM Set	20	16 byte	1
Red2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 Red PWM Set	21	16 byte	2
Red3 Set	0	1	0	0	0	1	0	0	0	1	0	FRAME 3 Red PWM Set	22	16 byte	3
Red4 Set	0	1	0	0	0	1	0	0	0	1	1	FRAME 4 Red PWM Set	23	16 byte	4
Grn1 Set	0	1	0	0	0	1	0	0	1	0	0	FRAME 1 Grn PWM Set	24	16 byte	5
Grn2 Set	0	1	0	0	0	1	0	0	1	0	1	FRAME 2 Grn PWM Set	25	16 byte	6
Grn3 Set	0	1	0	0	0	1	0	0	1	1	0	FRAME 3 Grn PWM Set	26	16 byte	7
Grn4 Set	0	1	0	0	0	1	0	0	1	1	1	FRAME 4 Grn PWM Set	27	16 byte	8
Blu1 Set	0	1	0	0	0	1	0	1	0	0	0	FRAME 1 Blu PWM Set	28	16 byte	9
Blu2 Set	0	1	0	0	0	1	0	1	0	0	1	FRAME 2 Blu PWM Set	29	16 byte	10
Blu3 Set	0	1	0	0	0	1	0	1	0	1	0	FRAME 3 Blu PWM Set	2A	16 byte	11
Blu4 Set	0	1	0	0	0	1	0	1	0	1	1	FRAME 4 Blu PWM Set	2B	16 byte	12
ANASET	0	1	0	0	0	1	1	0	0	1	0	Analog	32	3 byte	13
DITHOFF	0	1	0	0	0	1	1	0	1	0	0	Dithering Circuit Off	34	None	14
DITHON	0	1	0	0	0	1	1	0	1	0	1	Dithering Circuit On	35	None	15
EPCTIN	0	1	0	1	1	0	0	1	1	0	1	Control EEPROM	CD	1 byte	17
EPCOUT	0	1	0	1	1	0	0	1	1	0	0	Cancel EEPROM	CC	None	18
EPMWR	0	1	0	1	1	1	1	1	1	0	0	Write to EEPROM	FC	None	19
EPMRD	0	1	0	1	1	1	1	1	1	0	1	Read from EEPROM	FD	None	20

Ext=1 or Ext=0															
Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter	Index
Ext In	0	1	0	0	0	1	1	0	0	0	0	Ext=0 Set	30	None	--
Ext Out	0	1	0	0	0	1	1	0	0	0	1	Ext=1 Set	31	None	--

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EXT="0"

(1) Display ON (DISON) Command: 1; Parameter: None (AFH)

It is used to turn the display on. When the display is turned on, segment outputs and common outputs are generated at the level corresponding to the display data and display timing. You can't turn on the display as long as the sleep mode is selected. Thus, whenever using this command, you must cancel the sleep mode first.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	1

(2) Display OFF (DISOFF) Command: 1; Parameter: None (AEH)

As long as the display is turned off, every segment and common outputs are forced to Vss level.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	0

(3) Normal display (DISNOR) Command: 1; Parameter: None (A6H)

It is used to normally highlight the display area without modifying contents of the display data RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	0

(4) Inverse display (DISINV) Command: 1; Parameter: None (A7)

It is used to inversely highlight the display area without modifying contents of the display data RAM. This command does not invert non-display areas in case of using partial display.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	1

(5) Common scan (COMSCAN) Command: 1; Parameter: 1 (BBH)

It is used to specify the direction the common output direction. This command helps increasing degrees of freedom of wiring on the LCD panel.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	0	1	1	—
Parameter1 (P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Common Scan direction

When 1/104 is selected for the display duty, pins and common output are scanned in the order shown below. When CSEL = "H", this function becomes no use.

P12	P11	P10	Common scan direction			
			COM0 pin	COM51 pin	COM52 pin	COM103 pin
0	0	0	0	à	51	52 à 103
0	0	1	0	à	51	103 à 52
0	1	0	51	à	0	52 à 103
0	1	1	51	à	0	103 à 52

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(6) Display control (DISCTL) Command: 1; Parameter: 3 (CAH)

This command and succeeding parameters are used to perform the display timing-related setups. This command must be selected before using SLPOUT. Don't change this command while the display is turned on.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	0	0	1	0	1	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	*	*	CL dividing ratio,
Parameter2(P2)	1	1	0	0	0	0	P24	P23	P22	P21	P20	Drive duty
Parameter3(P3)	1	1	0	*	*	*	P34	P33	P32	P31	P30	FR inverse-set value

P1: it is used to specify the CL dividing ratio.

P14, P13, P12: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.

P14	P13	P12	CL dividing ratio
0	0	0	Not divide
0	0	1	2 divisions
0	1	0	4 divisions
0	1	1	8 divisions

This command Decides the Oscillator frequency(default=7.8KHz),Related Command 32H.

P2: It is used to specify the duty of the module on block basis.

Duty	*	*	P25	P24	P23	P22	P21	P20	(Numbers of display lines)/4-1
Example: 1/104 duty	0	0	0	1	1	0	0	0	104/4-1=25

P3: It is used to specify number of lines to be inversely highlighted on LCD panel from P33 to P30 (lines can be inversely highlighted in the range of 2 to 16)

Inversely highlighted line	*	*	*	P34	P33	P32	P31	P30	Inversely highlighted lines-1
Example: 11H	0	0	0	0	1	0	1	0	11-1=10
Example: 13H	0	0	0	1	1	1	0	0	13-1=12

In the default, 11H inverse highlight is selected.

P34="0": Inversion occurs every frame. P34="1": Independent from frames.

(7) Sleep In/Out Preparation (SLPP) Command: 1; Parameter: 1

Using this command to setup ready status for sleep-in or sleep out.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	0	1	0	0	—
Parameter(P1)	1	1	0	0	0	1	1	1	1	1	P10	Sleep in/out ready

P10 = "1": Ready for sleep in. P10 = "0": Ready for sleep out.

Parameter 3FH is used to initialize sleep-in sequencing, and parameter 3EH is used to initialize sleep-out sequencing.

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(8)Sleep in (SPLIN) Command: 1; Parameter: None (95H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	1

(9)Sleep out (SLPOUT) Command: 1;Parameter: None (94H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	0

(10)Page address set (PASET) Command: 1; Parameter: 2 (75H)

When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the page address area. As the addresses are incremented from the start to the end page in the page-direction scan, the column address is incremented by 1 and the page address is returned to the start page. Note that the start and end page must be specified as a pair. Also, the relation “start page <end page” must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	1	1	0	1	0	1	—
Parameter1(P1)	1	1	0	0	P16	P15	P14	P13	P12	P11	P10	Start page
Parameter2(P2)	1	1	0	0	P26	P25	P24	P23	P22	P21	P20	End page

(11)Column address set (CASET) Command: 1; Parameter: 2 (15H)

When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the column address area. As the addresses are incremented from the start to the end column in the column-direction scan, the page address is incremented by 1 and the column address is returned to the start column. Note that the start and end page must be specified as a pair. Also, the relation “start column <end column” must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	1	0	1	0	1	—
Parameter1(P1)	1	1	0	0	P16	P15	P14	P13	P12	P11	P10	Start address
Parameter2(P2)	1	1	0	0	P26	P25	P24	P23	P22	P21	P20	End address

(12)Data control (DATCTL) Command: 1;Parameter: 3 (BCH)

This command and succeeding parameters are used to perform various setups needed when MPU operates display data stored on the built-in RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	1	0	0	—
Parameter1(P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Normal/reverse display of page address and page-address scan direction.
Parameter2(P2)	1	1	0	*	*	*	*	*	*	*	P20	RGB arrangement
Parameter3(P3)	1	1	0	*	*	*	*	*	P32	P31	P30	Gray-scale setup

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P1: It is used to specify the normal or inverse display of the page address and also to specify the page address scanning direction.

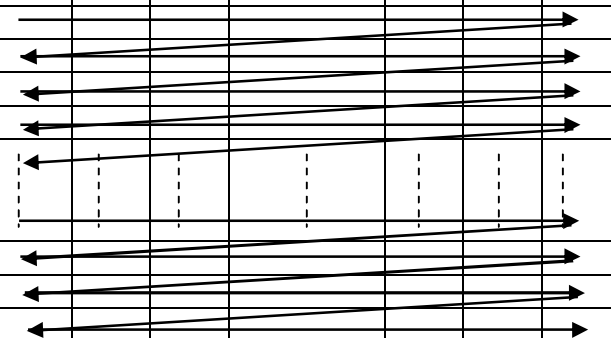
P10: Normal/reverse display of the page address. P10=0: Normal rotation and P10=1: Reverse rotation.

P11: Normal/reverse turn of column address. P11=0: Normal rotation and P11=1: Reverse rotation.

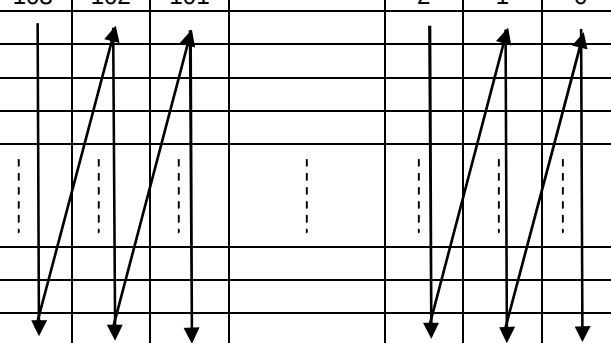
P12: Address-scan direction. P12=0: In the column direction and P12=1: In the page direction.

Page address and page-address scan direction.

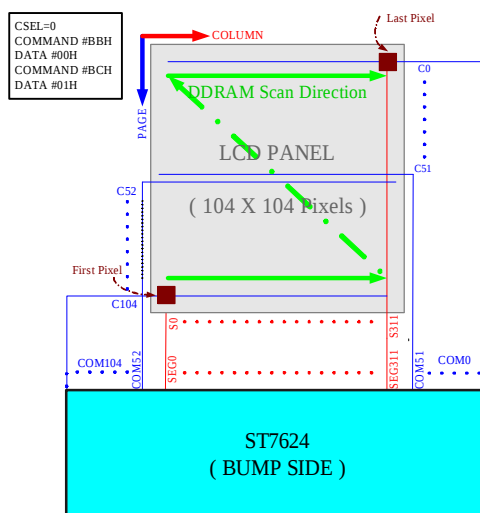
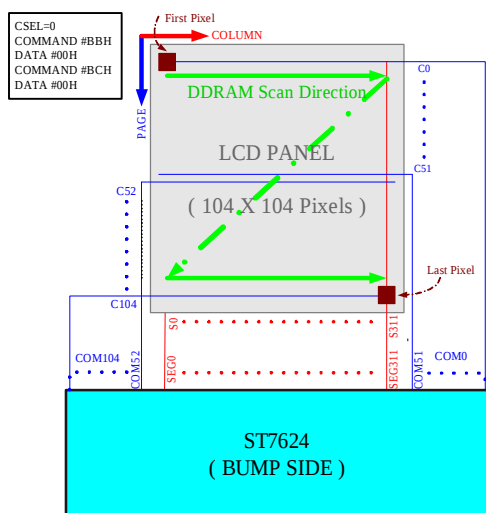
P12=0 Column direction

P11=0		0	1	2		101	102	103
P11=1		103	102	101		2	1	0
P10=0	P10=1							
0	103							
1	102							
2	101							
⋮	⋮							
101	2							
102	1							
103	0							

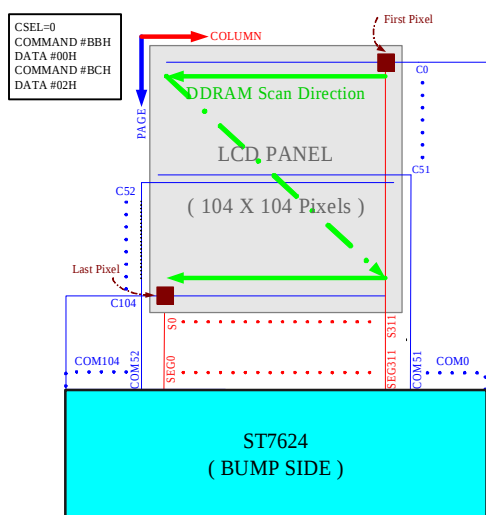
P12=1 Page direction

P11=0		0	1	2		101	102	103
P11=1		103	102	101		2	1	0
P10=0	P10=1							
0	103							
1	102							
2	101							
⋮	⋮							
101	2							
102	1							
103	0							

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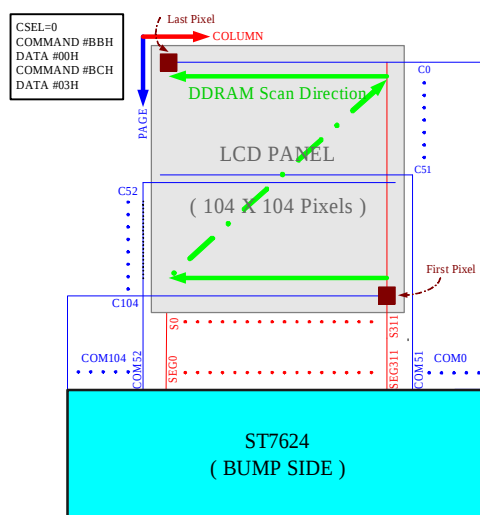


(a) COMMAND #BCH, DATA #00H



(c) COMMAND #BCH, DATA #02H

(b) COMMAND #BCH, DATA #01H

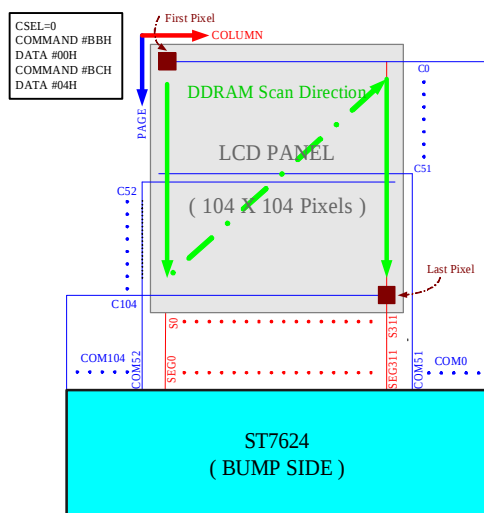


(d) COMMAND #BCH, DATA #03H

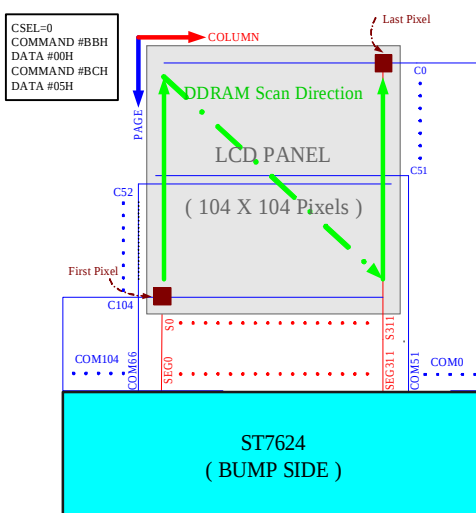
Figure 8.2.1 Different RAM accessing setup when CSEL=0 under COMMAND #BBH, DATA #00H

- (a) COMMAND #BCH, DATA #00H
- (b) COMMAND #BCH, DATA #01H
- (c) COMMAND #BCH, DATA #02H
- (d) COMMAND #BCH, DATA #03H

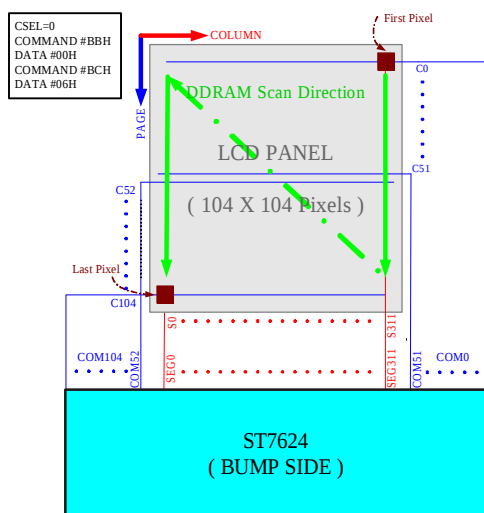
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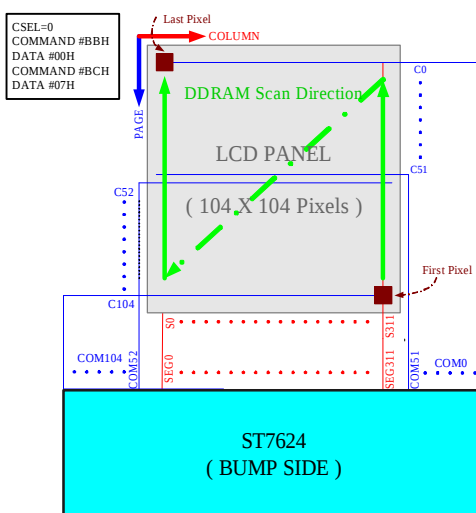
(e) COMMAND #BCH, DATA #04H



(f) COMMAND #BCH, DATA #05H



(g) COMMAND #BCH, DATA #06H



(h) COMMAND #BCH, DATA #07H

Figure 8.2.3 Different RAM accessing setup when CSEL=0 under COMMAND #BBH, DATA #00H (continue)

(e) COMMAND #BCH, DATA #04H

(f) COMMAND #BCH, DATA #05H

(g) COMMAND #BCH, DATA #06H

(h) COMMAND #BCH, DATA #07H

P2: RGB arrangement. This parameter allows you to change RGB arrangement of data which is going to be written into RAM, and therefore causes the inverse RGB rotation of the segment output of ST7624. You can fit RGB arrangement on the LCD panel according to this parameter setting.

P20	Line	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	...	SEG311
0	Even page	R	G	B	R	G	B	R	G	...	B
	Odd page	R	G	B	R	G	B	R	G	...	B
1	1	B	G	R	B	G	R	B	G	...	R
	2	B	G	R	B	G	R	B	G	...	R

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P3: Gray scale setup. Using this parameter, 64 gray-scale display, you can select the 65K, 262K, and 16M display mode depending on the difference in RGB data arrangement.

P32	P31	P30	Numbers of gray-scale
0	0	1	64-gray 65K
0	1	0	64-gray 262K
1	0	0	64-gray 16M

(13)Memory write (RAMWR) Command: 1;Parameter: Numbers of data written (5CH)

When MPU writes data to the display memory, this command turns on the data entry mode. Entering this command always sets the page and column address at the start address. You can rewrite contents of the display data RAM by entering data succeeding to this command. At the same time, this operation increments the page or column address as applicable. The write mode is automatically cancelled if any other command is entered.

1. 8-bit bus

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	0	—
Parameter	1	1	0	Data to be written							Data to be written	

2. 16-bit bus

	A0	RD	RW	D15	D14	...	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	...	*	*	0	1	0	1	1	1	0	0	Memory write
parameter	1	1	0	Data to be written												Write date	

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(14)Memory read (RAMRD) Command: 1; Parameter: Numbers of data read (5DH)

When MPU read data from the display memory, this command turns on the data read mode. Entering this command always sets the page and column address at the start address. After entering this command, you can read contents of the display data RAM. At the same time, this operation increments the page or column address as applicable. The data read mode is automatically cancelled if any other command is entered.

1. 8-bit bus

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	1	--
Parameter	1	0	1	Data to be read							Data to be read	

2. 16-bit bus

	A0	RD	RW	D15	D14		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	*	*	*	0	1	0	1	1	1	0	1	Memory read
parameter	1	0	1	Data to be read												Read date	

(15)Partial in (PTLIN) Command: 1; Parameter: 2 (A8H)

This command and succeeding parameters specify the partial display area. This command is used to turn on partial display of the screen (dividing screen by lines) in order to save power. Since ST7624 processes the liquid crystal display signal on 4-line basis (block basis), the display and non-display areas are also specified on 4-bit line (block basis).

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	0	0	--
Parameter(P1)	1	1	0	*	*	0	P14	P13	P12	P11	P10	Start block address
Parameter(P2)	1	1	0	*	*	0	P24	P23	P22	P21	P20	End block address

A block address that can be specified for the partial display must be the display one (don't try to specify an address not to be displayed when scrolled).

(16)Partial out (PTLOUT) Command: 1; Parameter: 0 (A9H)

This command is used to exit from the partial display mode.

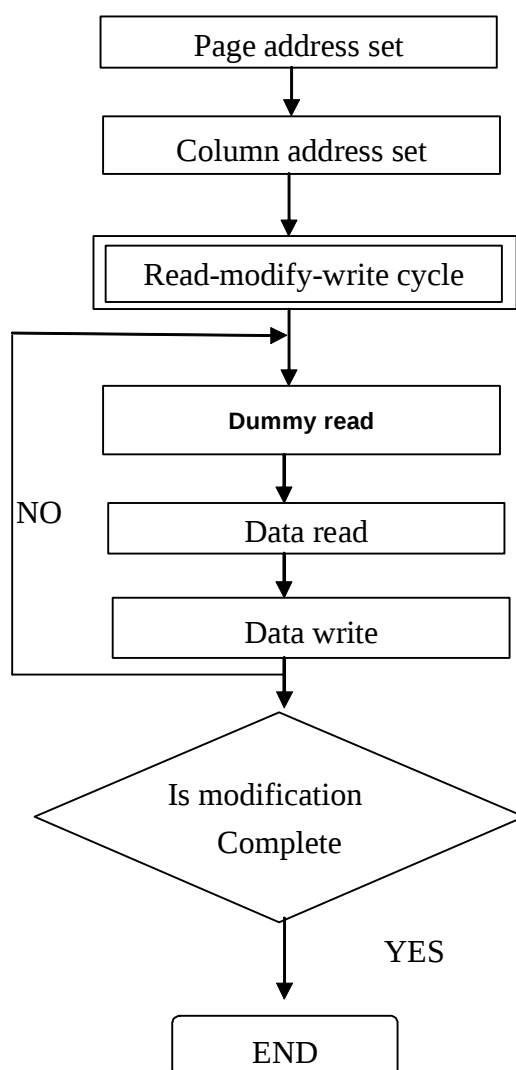
	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	0	0	1

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(17)Read modify write in (RMWIN) Command: 1; Parameter: 0 (E0H)

This command is used along with the column address set command, page address set command and read modify write out command. This function is used when frequently modifying data to specify a specific display area such as blinking cursor. First set a specific display area using the column and page address commands. Then, enter this command to set the column and page addresses at the start address of the specific area. When this operation is complete, the column (page) address won't be modified by the display data read command. It is incremented only when the display data write command is used. You can cancel this mode by entering the read modify write out or any other command.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	0	0	0



(18)Read modify write out (RMWOUT) Command: 1; Parameter: 0 (EEH)

Enter this command cancels the read modify write mode

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	1	1	1	0

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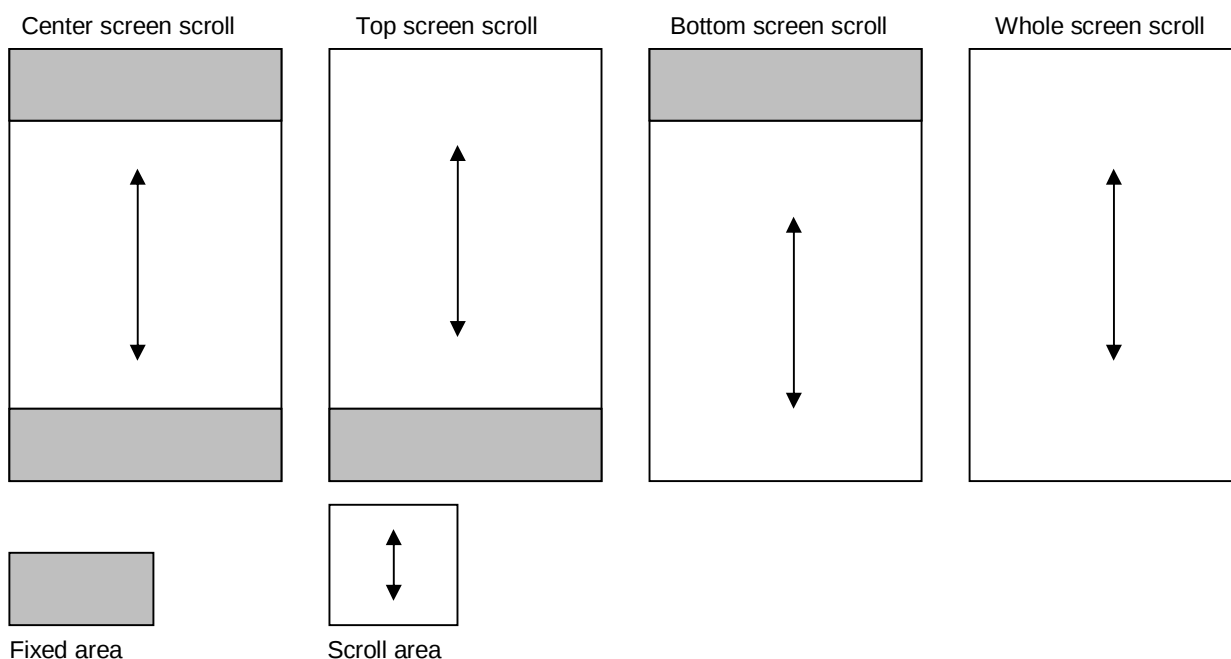
(19)Area scroll set (ASCSET) Command: 1; Parameter: 4 (AAH)

It is used when scrolling only the specified portion of the screen (dividing the screen by lines). This command and succeeding parameters specify the type of area scroll, FIX area and scroll area.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	0	--
Parameter(P1)	1	1	0	*	*	0	P14	P13	P12	P11	P10	Top block address
Parameter(P2)	1	1	0	*	*	0	P24	P23	P22	P21	P20	Bottom block address
Parameter(P3)	1	1	0	*	*	0	P34	P33	P32	P31	P30	Number of specified blocks
Parameter(P4)	1	1	0	*	*	*	*	*	*	P41	P40	Area scroll mode

P4: It is used to specify an area scroll mode.

P41	P40	Type of area scroll
0	0	Center screen scroll
0	1	Top screen scroll
1	0	Bottom screen scroll
1	1	Whole screen scroll



Since ST7624 processes the liquid crystal display signals on the four-line basis (block basis), FIX and scroll areas are also specified on the four-line basis (block basis).

DDRAM address corresponding to the top FIX area is set in the block address incrementing direction starting with 0 block.

DDRAM address corresponding to the bottom FIX area is set in the block address decreasing direction starting with 41st block. Other DDRAM blocks excluding the top and bottom FIX areas are assigned to the scroll + background areas.

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P1: It is used to specify the top block address of the scroll+ background areas. Specify the 0th block for the top screen scroll or whole screen scroll.

P2: It specifies the bottom address of the scroll+ background areas. Specify the 32th block for the bottom or whole screen scroll.

Required relation between the start and end blocks (top block address < bottom block address) must be maintained.

P3: It specifies a specific number of blocks {Numbers of (Top FIX area + Scroll area) block-1}. When the bottom scroll or whole screen scroll, the value is identical with P2.

You can turn on the area scroll function by executing the area scroll set command first and then specifying the display start block of the scroll area with the scroll start set command.

[Area Scroll Setup Example]

In the center screen scroll of 1/92 duty (display range: 92 lines=23 blocks), if 8 lines=2 blocks and 8 lines=2 blocks are specified for the top and bottom FIX areas, 76 lines =19 blocks is specified for the scroll areas, respectively, 12 lines = 3 blocks on the DDRAM are usable as the background area. Value of each parameter at this time is as shown below.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	
P1	1	1	0	*	*	0	0	0	0	1	0	Top block address = 2
P2	1	1	0	*	*	0	1	0	1	1	1	Bottom block address = 23
P3	1	1	0	*	*	0	1	0	1	0	0	Number of specific blocks = 23
P4	1	1	0	*	*	*	*	*	*	0	0	Area scroll mode = center

(20)Scroll start address set (SCSTART) Command:1 Parameter: 1 (ABH)

This command and succeeding parameters are used to specify the start block address of the scroll area. Note that you must execute this command after executing the area scroll set command. Scroll becomes available by dynamically changing the start block address.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	1	--
Parameter(P1)	1	1	0	*	*	0	P14	P13	P12	P11	P10	Start block address

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(21)Internal oscillation on (OSCON) Command: 1; Parameter: 0 (D1H)

This command turns on the internal oscillation circuit. It is valid only when the internal oscillation circuit of CLS = HIGH is used.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	0	1

(22)Internal oscillation off (OSOFF) Command: 1; Parameter: 0 (D2H)

It turns off the internal oscillation circuit. This circuit is turned off in the reset mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	1	0

(23)Power control set (PWRCTR) Command: 1; Parameter: 1 (20H)

This command is used to turn on or off the Booster circuit, voltage follower circuit, and voltage regulator circuit.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	1	0	0	1	0	0	0	0	0	--
Parameter(P1)	1	1	0	*	*	*	*	P13	*	P11	P10	LCD drive power

P10: It turns on or off the voltage regulator circuit.

P10 = "1": ON. P10 = "0": OFF

P11: It turns on or off the voltage follower circuit.

P11 = "1": ON. P11 = "0": OFF

P13:It turns on or off the Booster.

P13 = "1": ON. P13 = "0": OFF

(24)Electronic volume control (VOLCTR) Command: 1; Parameter: 2 (81H)

The command is used to program the optimum LCD supply voltage V_{LCD} . Reference to 7.10.2

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	0	0	0	0	0	1	--
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Set Vop[5:0]
Parameter(P2)	1	1	0	*	*	*	*	*	P18	P17	P16	Set Vop[8:6]

(25)Increment electronic control (VOLUP) Command: 1; Parameter: 0 (D6H)

With the VOLUP and VOLDOWN command the V_{LCD} voltage and therewith the contrast of the LCD can be adjusted.

This command increments electronic control value VOP[5:0] of voltage regulator circuit by 1.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	0

If you set the electronic control value to 111111, the control value is set to 000000 after this command has been executed.

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(26)Decrement electronic control (VOLDDOWN) Command: 1; Parameter: 0 (D7H)

With the VOLUP and VOLDDOWN command the VLCD voltage and therewith the contrast of the LCD can be adjusted.

This command decrements electronic control value VOP[5:0] of voltage regulator circuit by 1.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	1

If you set the electronic control value to 000000, the control value is set to 111111 after this command has been executed.

Table 8.1.1 Possible VOP[5:0] values

Electronic Control Value	Decimal Equivalent	VLCD Offset
111111	31	+1240 mV
111110	30	+1200 mV
111101	29	+1160 mV
...	...	...
000010	2	+80 mV
000001	1	+40 mV
000000	0	0 mV
111111	-1	-40 mV
111110	-2	-80 mV
...	...	...
100010	-30	-1200 mV
100001	-31	-1240 mV
100000	-32	-1280mV

(27)Read Register 1 (EPSRRD1) Command: 1; Parameter: 0 (7CH)

Issue the EPSRRD1 and STREAD (Status Read) commands in succession to read the Electronic Control value.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	0

Issue the Status Read command immediately after this command. Also, always issue the NOP command after the STREAD (Status Read) command.

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EXT="1"

(1)Set Red 1 value (Red1 set) Command: 1; Parameter: 16 (20H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 1st frame

(2)Set Red 2 value (Red2 set) Command: 1; Parameter: 16 (21H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 2nd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 2nd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 2nd frame

(3) Set Red 3 value (Red3 set) Command: 1; Parameter: 16 (22H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red3 Set	0	1	0	0	0	1	0	0	0	1	0	FRAME 3 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 3rd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 3rdframe
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 3rd frame

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(4) Set Red 4 value (Red4 set) Command: 1; Parameter: 16 (23H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red4 Set	0	1	0	0	0	1	0	0	0	1	1	FRAME 4 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 4th frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 4thframe
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 4th frame

The default value of Red level set

	RED1SET	RED2SET	RED3SET	RED4SET
	FRAM1	FRAM2	FRAM3	FRAME4
red level0	00	00	00	00
red level1	02	02	02	02
red level2	05	05	05	05
red level3	07	07	07	08
red level4	0A	0A	0A	0B
red level5	0D	0D	0D	0C
red level6	0F	10	0F	10
red level7	11	12	11	12
red level8	13	14	13	14
red level9	16	16	16	15
red level10	18	18	18	17
red level11	19	19	19	1A
red level12	1B	1B	1B	1A
red level13	1C	1C	1C	1D
red level14	1D	1D	1D	1E
red level15	1E	1E	1E	1E

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The modulation range of Red level set

	RED1SET	RED2SET	RED3SET	RED4SET
	FRAM1	FRAM2	FRAM3	FRAME4
red level0	0	0	0	0
red level1	0-7	0-7	0-7	0-7
red level2	0-F	0-F	0-F	0-F
red level3	0-F	0-F	0-F	0-F
red level4	8-F	8-F	8-F	8-F
red level5	0-1F	0-1F	0-1F	0-1F
red level6	0-1F	0-1F	0-1F	0-1F
red level7	0-1F	0-1F	0-1F	0-1F
red level8	10-17	10-17	10-17	10-17
red level9	10-1F	10-1F	10-1F	10-1F
red level10	10-1F	10-1F	10-1F	10-1F
red level11	10-1F	10-1F	10-1F	10-1F
red level12	10-1F	10-1F	10-1F	10-1F
red level13	10-1F	10-1F	10-1F	10-1F
red level14	10-1F	10-1F	10-1F	10-1F
red level15	18-1F	18-1F	18-1F	18-1F

(5) Set Green 1 value (Grn1 set) Command: 1; Parameter: 16 (24H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn 1 Set	0	1	0	0	0	1	0	0	1	0	0	FRAME 1 Grn PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 1st frame

(6) Set Green 2 value (Grn2 set) Command: 1;Parameter: 16 (25H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn2 Set	0	1	0	0	0	1	0	0	1	0	1	FRAME 2 Grn PWM Set

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	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 2nd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 2nd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 2nd frame

(7) Set Green 3 value (Grn3 set) Command: 1; Parameter: 16 (26H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn3 Set	0	1	0	0	0	1	0	0	1	0	1	FRAME 3 Grn PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 3rd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 3rdframe
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 3rd frame

(8) Set Green 4 value (Grn4 set) Command: 1;Parameter: 16 (27H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn4 Set	0	1	0	0	0	1	0	0	1	1	1	FRAME 4 Grn PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 4th frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 4thframe
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 4th frame

The default value of Green level set

	GRN1SET	GRN2SET	GRN3SET	GRN4SET
	FRAM1	FRAM2	FRAM3	FRAME4
green level0	00	00	00	00
green level1	02	02	02	02
green level2	05	05	05	05
green level3	07	07	07	08

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green level4	0A	0A	0A	0B
green level5	0D	0D	0D	0C
green level6	0F	10	0F	10
green level7	11	12	11	12
green level8	13	14	13	14
green level9	16	16	16	15
green level10	18	18	18	17
green level11	19	19	19	1A
green level12	1B	1B	1B	1A
green level13	1C	1C	1C	1D
green level14	1D	1D	1D	1E
green level15	1E	1E	1E	1E

The modulation range of Green level set

	GRN1SET	GRN2SET	GRN3SET	GRN4SET
	FRAM1	FRAM2	FRAM3	FRAME4
green level0	0	0	0	0
green level1	0-7	0-7	0-7	0-7
green level2	0-F	0-F	0-F	0-F
green level3	0-F	0-F	0-F	0-F
green level4	8-F	8-F	8-F	8-F
green level5	0-1F	0-1F	0-1F	0-1F
green level6	0-1F	0-1F	0-1F	0-1F
green level7	0-1F	0-1F	0-1F	0-1F
green level8	10-17	10-17	10-17	10-17
green level9	10-1F	10-1F	10-1F	10-1F
green level10	10-1F	10-1F	10-1F	10-1F
green level11	10-1F	10-1F	10-1F	10-1F
green level12	10-1F	10-1F	10-1F	10-1F
green level13	10-1F	10-1F	10-1F	10-1F
green level14	10-1F	10-1F	10-1F	10-1F
green level15	18-1F	18-1F	18-1F	18-1F

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(9) Set Blue 1 value (Blu 1 set) Command: 1; Parameter: 16 (28H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn 1 Set	0	1	0	0	0	1	0	0	1	0	0	FRAME 1 Blu PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 1st frame

(10) Set Blue 2 value (Blu2 set) Command: 1; Parameter: 16 (29H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn2 Set	0	1	0	0	0	1	0	0	1	0	1	FRAME 2 Blu PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 2nd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 2nd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 2nd frame

(11) Set Blue 3 value (Blu3 set) Command: 1; Parameter: 16 (2AH)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn3 Set	0	1	0	0	0	1	0	0	1	1	0	FRAME 3 Blu PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 3rd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 3rd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 3rd frame

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(12) Set Blue 4 value (Blu4 set) Command: 1; Parameter: 16 (2BH)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn4 Set	0	1	0	0	0	1	0	0	1	1	1	FRAME 4 Blu PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 4th frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 4thframe
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 4th frame

The default value of Blue level set

	GRN1SET	GRN2SET	GRN3SET	GRN4SET
	FRAM1	FRAM2	FRAM3	FRAME4
blue level0	00	00	00	00
blue level1	02	02	02	02
blue level2	05	05	05	05
blue level3	07	07	07	08
blue level4	0A	0A	0A	0B
blue level5	0D	0D	0D	0C
blue level6	0F	10	0F	10
blue level7	11	12	11	12
blue level8	13	14	13	14
blue level9	16	16	16	15
blue level10	18	18	18	17
blue level11	19	19	19	1A
blue level12	1B	1B	1B	1A
blue level13	1C	1C	1C	1D
blue level14	1D	1D	1D	1E
blue level15	1E	1E	1E	1E

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The modulation range of Blue level set

	GRN1SET	GRN2SET	GRN3SET	GRN4SET
	FRAM1	FRAM2	FRAM3	FRAME4
blue level0	0	0	0	0
blue level1	0-7	0-7	0-7	0-7
blue level2	0-F	0-F	0-F	0-F
blue level3	0-F	0-F	0-F	0-F
blue level4	8-F	8-F	8-F	8-F
blue level5	0-1F	0-1F	0-1F	0-1F
blue level6	0-1F	0-1F	0-1F	0-1F
blue level7	0-1F	0-1F	0-1F	0-1F
blue level8	10-17	10-17	10-17	10-17
blue level9	10-1F	10-1F	10-1F	10-1F
blue level10	10-1F	10-1F	10-1F	10-1F
blue level11	10-1F	10-1F	10-1F	10-1F
blue level12	10-1F	10-1F	10-1F	10-1F
blue level13	10-1F	10-1F	10-1F	10-1F
blue level14	10-1F	10-1F	10-1F	10-1F
blue level15	18-1F	18-1F	18-1F	18-1F

(13) ANASET Command 1; Parameter: 3 (32H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	1	0	0	1	0	—
Parameter1(P1)	1	1	0	*	*	*	*	*	P12	P11	P10	OSC frequency Adjustment
Parameter2(P2)	1	1	0	*	*	*	*	*	*	P21	P20	Booster Efficiency Set
Parameter3(P3)	1	1	0	*	*	*	*	*	P32	P31	P30	Bias setting

P1: Oscillator frequency adjustment(CL division ratio ,plz reference “Command CAH”)

P12	P11	P10	Frame frequency	OSC Frequency CL=X1(KHz)	Note
0	0	0	77 ± 5%	8.09 ± 5%	Default
0	0	1	80 ± 20%	8.40 ± 20%	
0	1	0	87 ± 20%	9.14 ± 20%	
0	1	1	100 ± 20%	10.50 ± 20%	
1	0	0	105 ± 20%	11.03 ± 20%	
1	0	1	118 ± 20%	12.39 ± 20%	
1	1	0	133 ± 20%	13.97 ± 20%	
1	1	1	155 ± 20%	16.28 ± 20%	

Frame Frequency = OSC Frequency/(Duty+1)

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Example: using 96duty ,(P12,P11,P10)=(000),Frame Frequency=8.085k/(96+1)=83.35Hz

P2: Booster Efficiency set(Suggest using default value)

P21	P20	Frequency(Hz)
0	0	Level 1
0	1	Level 2 (Default)
1	0	Level 3
1	1	Level 4

P3: Select LCD bias ratio of the voltage required for driving the LCD.

P32	P31	P30	LCD bias
0	0	0	1/12
0	0	1	1/11
0	1	0	1/10
0	1	1	1/9
1	0	0	1/8
1	0	1	1/7
1	1	0	1/6
1	1	1	1/5

(14) Color Dither OFF (DITHOFF) Command: 1; Parameter: None (34H)

Turn off the dithering circuit.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	1	0	0

(15) Color Dither ON (DITHON) Command: 1; Parameter: None (35H)

Turn on the dithering circuit.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	1	0	1

(16) Control EEPROM (EPCTIN) Command: 1; Parameter: 1 (CDH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	1
Parameter (P1)	1	1	0	0	0	P15	0	0	0	0	0

P15: when setting "1" è The Write Enable of EEPROM will be opened.

P15: when setting "0" è The Read Enable of EEPROM will be opened.

(17) Cancel EEPROM (EPCOUT) Command: 1;Parameter:None (CCH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	0

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(18) Write data to EEPROM (EPMWR) Command: 1; Parameter: None (FCH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	0

(19) Read data from EEPROM (EPMWR) Command: 1; Parameter: None (FDH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	1

EXT="1" or "0"

(1) Extension instruction disable (EXT IN) Command:1 Parameter: None (30H)

Use the "Ext=0" command table

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	0

(2) Extension instruction enable (EXT OUT) Command:1 Parameter: None (31H)

Use the extended command table (EXT="1")

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	1

8.5 Referential Instruction Setup Flow

8.5.1 EEPROM Setting Flow

The ST7624 chip provide the Write and Read function to write the Electronic Control value and Built-in resistance ratio into and read them from the built-in EEPROM. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.

Note: When “Writing” value to EEPROM, the voltage of $V_{OUT_{IN}}$ must be more than 17V.

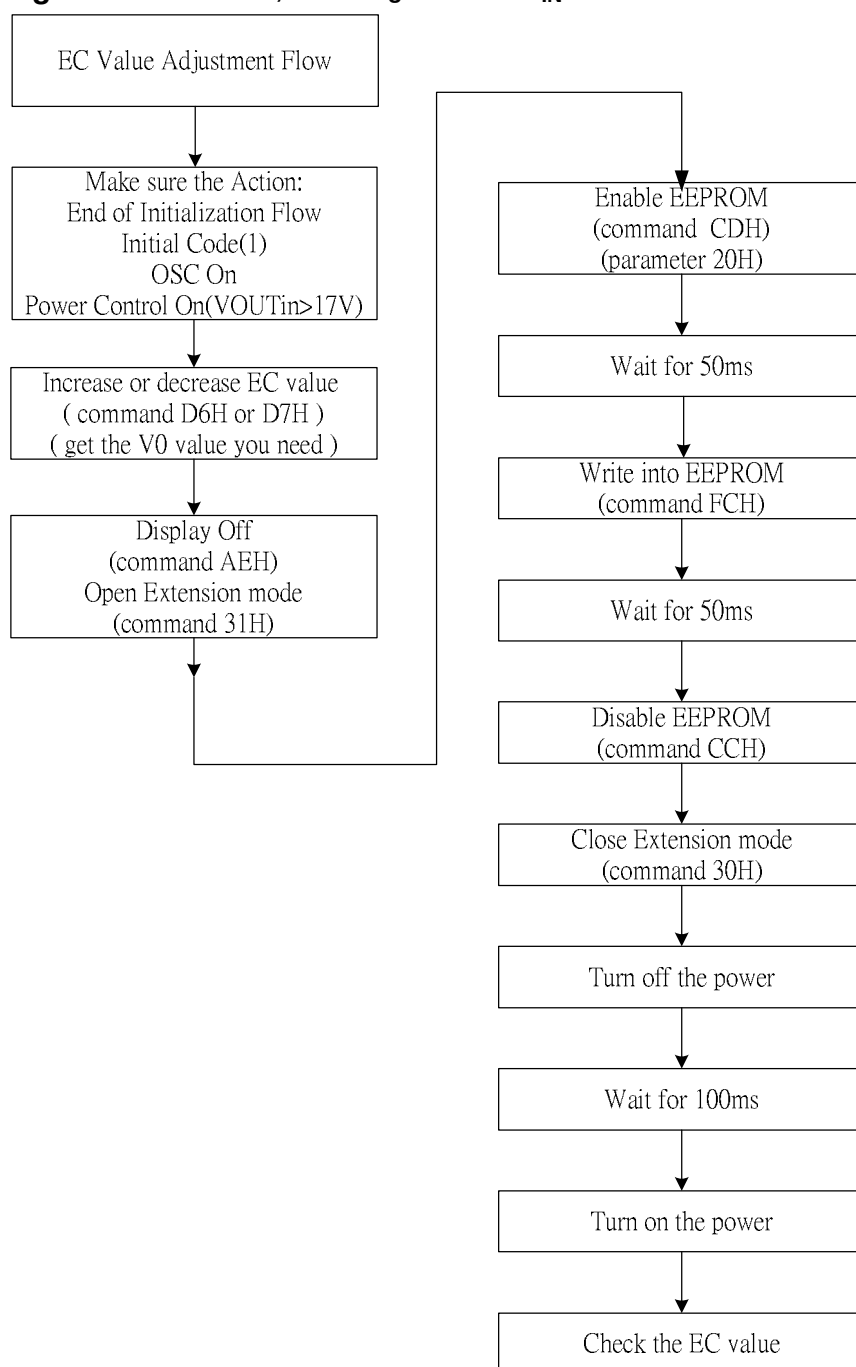


Figure 8.5.1.1 Flow of EC value adjustment and writing into EEPROM

Note: When “Reading” value from EEPROM, the voltage of V_{OUTIN} must be more than 10V.

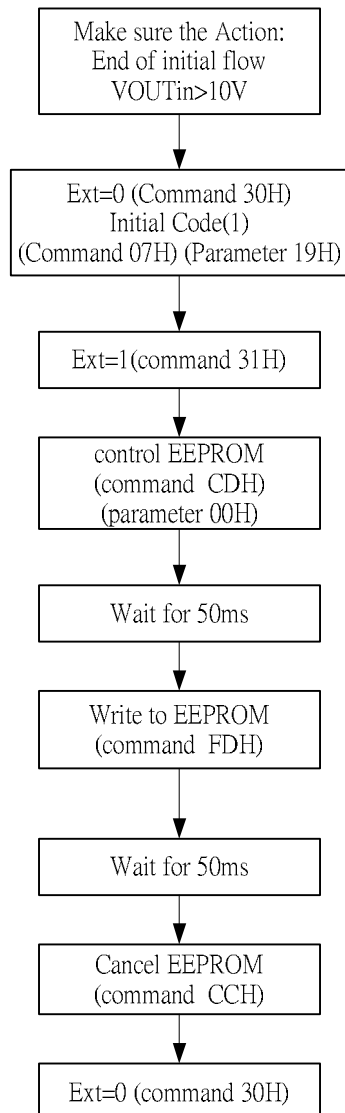


Figure 8.5.1.2 EEPROM Reading flow

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Example : EEPROM Read Operation

```
void ReadEEPROM( void )
{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x0007 );           // Initial code (1)
    Write( DATA, 0x0019 );

    Write( COMMAND, 0x0031 );           // Ext = 1
    Write( COMMAND, 0x00CD );           // EEPROM ON
    Write( DATA, 0x0000 );             // Entry "Read Mode"
    Delay( 50ms );                     // Waite for EEPROM Operation ( 50ms )
    Write( COMMAND, 0x00FD );           // Start EEPROM Reading Operation
    Delay( 50ms );                     // Waite for EEPROM Operation ( 50ms )
    Write( COMMAND, 0x00CC );           // Exist EEPROM Mode step.1
    Write( COMMAND, 0x0030 );           // Exist EEPROM Mode step.2
}
```

Example : EEPROM Write Operation

```
void WriteEEPROM( void )
{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x0007 );           // Initial code(1)
    Write( DATA, 0x0019 );

    Write( COMMAND, 0x00AE );           //Display Off
    Write( COMMAND, 0x0031 );           // Ext = 1
    Write( COMMAND, 0x00CD );           // EEPROM ON
    Write( DATA, 0x0020 );             // Entry "Write Mode"
    Delay( 50ms );                     // Waite for EEPROM Operation ( 50ms )
    Write( COMMAND, 0x00FC );           // Start EEPROM Writing Operation
    Delay( 50ms );                     // Waite for EEPROM Operation ( 50ms )
    Write( COMMAND, 0x00CC );           // Exist EEPROM Mode step.1
    Write( COMMAND, 0x0030 );           // Exist EEPROM Mode step.2
}
```

8.5.2 Initializing with the Built-in Power Supply Circuits

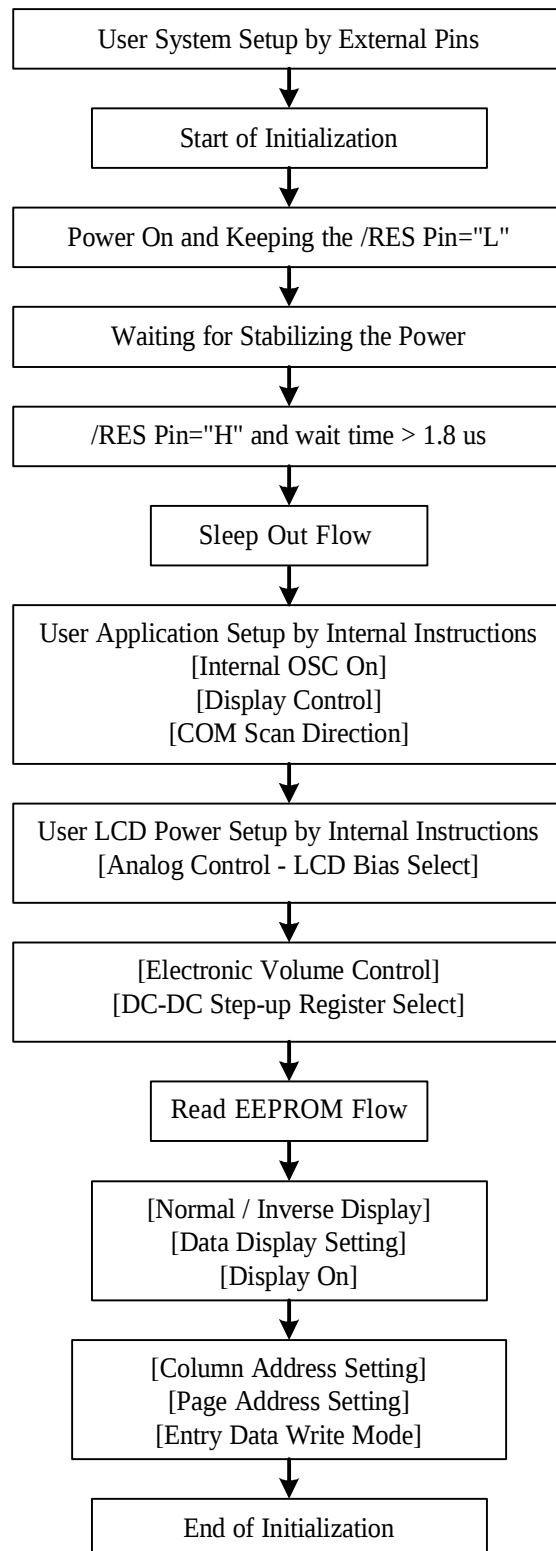


Figure 8.5.2.1 Initializing with the Built-in Power Supply Circuits

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Example : Initial code for 96X96

void ST7624_Init(void)

{	
Write(COMMAND, 0x0030);	//Ext = 0
SleepOut();	//Sleep Out Flow
Write(COMMAND, 0x00D1);	//OSC On
Write(COMMAND, 0x0020);	//Power Control Set
Write(DATA, 0x000B);	//Booster Regulator Follower On
Write(COMMAND, 0x0081);	//Electronic Control
Write(DATA, 0x0004);	//Vop=14.0V
Write(DATA, 0x0004);	
Write(COMMAND, 0x00CA);	//Display Control
Write(DATA, 0x0000);	//CL=X1
Write(DATA, 0x0017);	//Duty=96
Write(DATA, 0x0000);	//FR Inverse-Set Value
Write(COMMAND, 0x00A6);	// Normal Display
Write(COMMAND, 0x00BB);	//COM Scan Direction
Write(DATA, 0x0001);	// 0→51 103→52
Write(COMMAND, 0x00BC);	//Data Scan Direction
Write(DATA, 0x0000);	//Normal
Write(DATA, 0x0000);	//RGB Arrangement
Write(DATA, 0x0001);	//65K COLOR
Write(COMMAND, 0x0075);	// Page Address Set
Write(DATA, 0x0000);	//Start Page=0
Write(DATA, 0x005F);	//End Page =95
Write(COMMAND, 0x0015);	//Column Address Set
Write(DATA, 0x0000);	//Start Column=0
Write(DATA, 0x005F);	//End Column =95
Write(COMMAND, 0x0031);	//Ext = 1
Write(COMMAND, 0x0032);	//Analog Circuit Set
Write(DATA, 0x0000);	//OSC Frequency =000 (Default)
Write(DATA, 0x0001);	//Booster Efficiency=01(Default)
Write(DATA, 0x0001);	//Bias=1/11
Write(COMMAND, 0x0034);	//Dithering Off
ReadEEPROM();	//Read EEPROM Flow
Write(COMMAND, 0x00AF);	//Display On
}	

8.5.3 Sleep In/Out

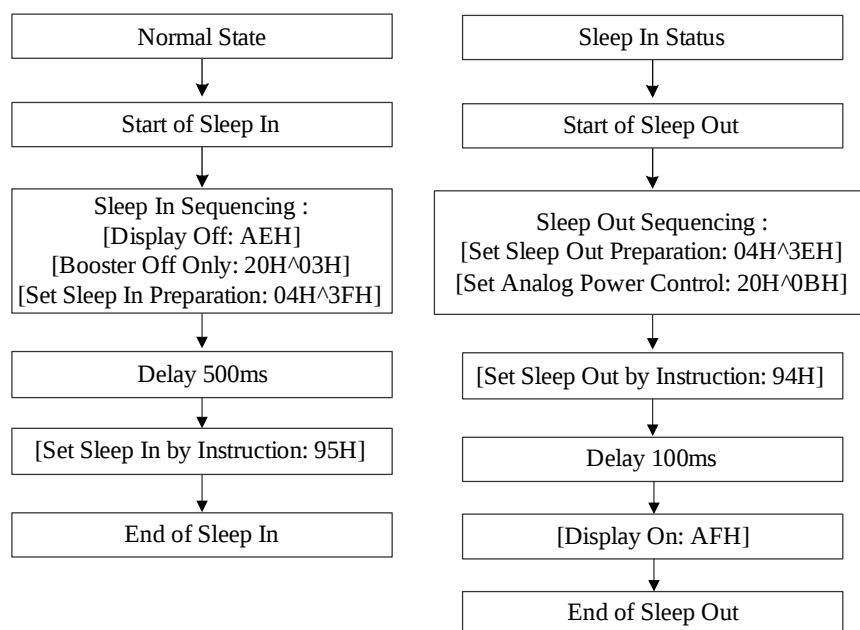


Fig 8.5.3.1 Sleep In/Out

Example : Sleep In Operation

```

void SleepIn( void )
{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x00AE );           // Display Off
    Write( COMMAND, 0x0020 );           // Power Control
    Write( DATA, 0x0003 );             // B/F/R = Off/On/On
    Write( COMMAND, 0x0004 );           // Sleep Preparation
    Write( DATA, 0x003F );             // Sleep In Ready
    Delay( 500ms );
    Write( COMMAND, 0x0095 );           // Sleep In
}
  
```

Example : Sleep Out Operation

```

void SleepOut( void )
{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x0004 );           // Sleep Preparation
    Write( DATA, 0x003E );             // Sleep Out Ready
    Write( COMMAND, 0x0020 );           // Power Control
    Write( DATA, 0x000B );             // B/F/R = On/On/On
    Write( COMMAND, 0x0094 );           // Sleep Out
    Delay( 100ms );
    Write( COMMAND, 0x00AF );           // Display On
}
  
```

8.5.4 Data Displaying

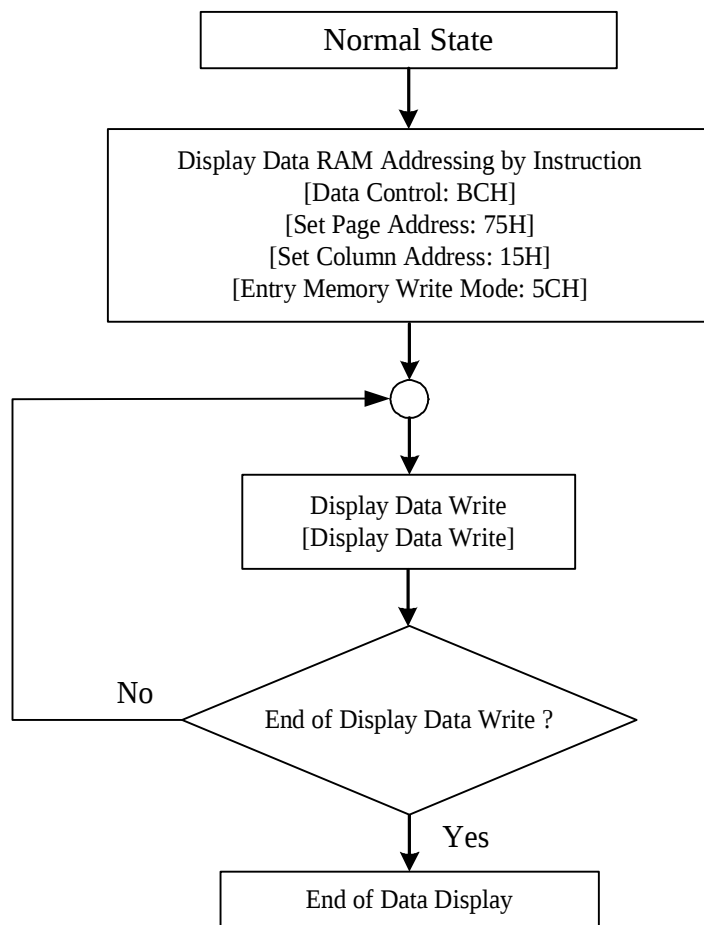


Figure 8.5.4.1 Data Displaying

Example : Display for 104X104

```

void Display( char *pattern )
{
    unsigned char i, j;

    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x0015 );           // Column address set
    Write( DATA, 0 );                  // From column0 to column103
    Write( DATA, 103 );
    Write( COMMAND, 0x0075 );           // Page address set
    Write( DATA, 0 );                  // From page0 to page103
    Write( DATA, 103 );
    Write( COMMAND, 0x005C )            // Entry Memory Write Mode
    for( j = 0; j < 104; j++ )
        for( i = 0; i < 104; i++ )
            Write( DATA, pattern[j*104+i] ); // Display Data Write
}
  
```

8.5.5 Partial Display In/Out

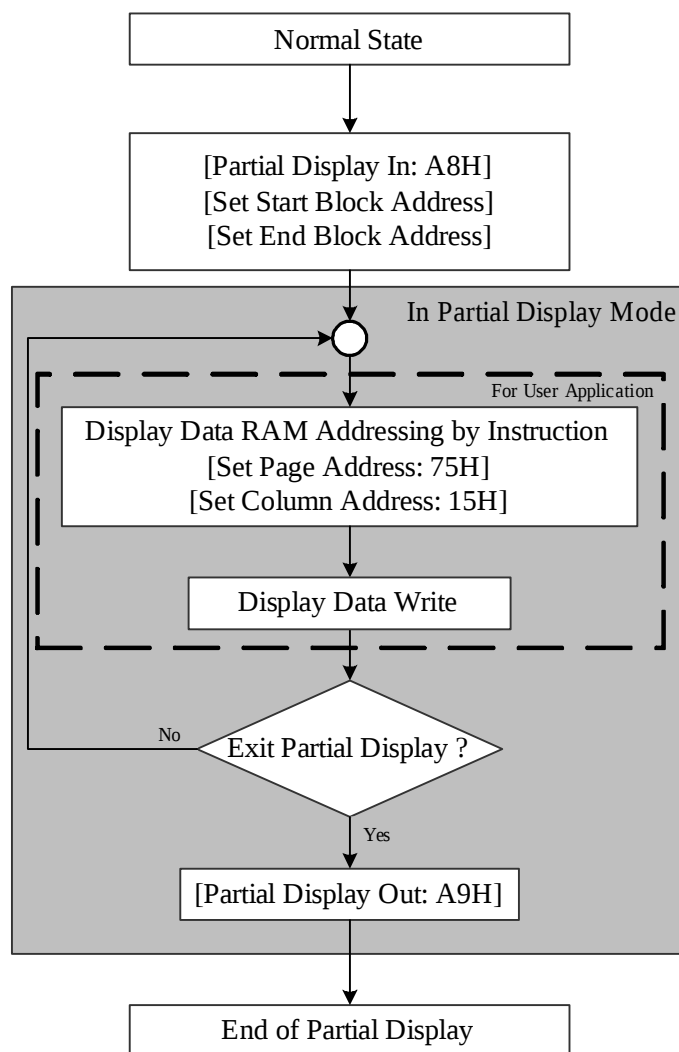


Figure 8.5.5.1 Partial Display In/Out

Example : Partial Display In Operation

```

void PartailIn( unsigned char start_block, unsigned char end_block )
{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x00A8 );           // Partial Display In Function
    Write( DATA, start_block );        // Start Block
    Write( DATA, end_block );          // End Block
}

void PartailOut( void )
{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x00A9 );           // Partial Display Out Function
}
  
```

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```
extern unsigned char *display_pattern;
void main()
{
    PartialIn( 11, 18 );           // entry partial display mode

    Windowing( 0, 11*4, 103, 18*4 ); // set the page and column range
    PartialDisplay( display_pattern ); // Fill the data into partial display area
    .
    .
    .
    PartialOut();                  // Out of partial display mode
}
```

8.5.6 Scroll Display

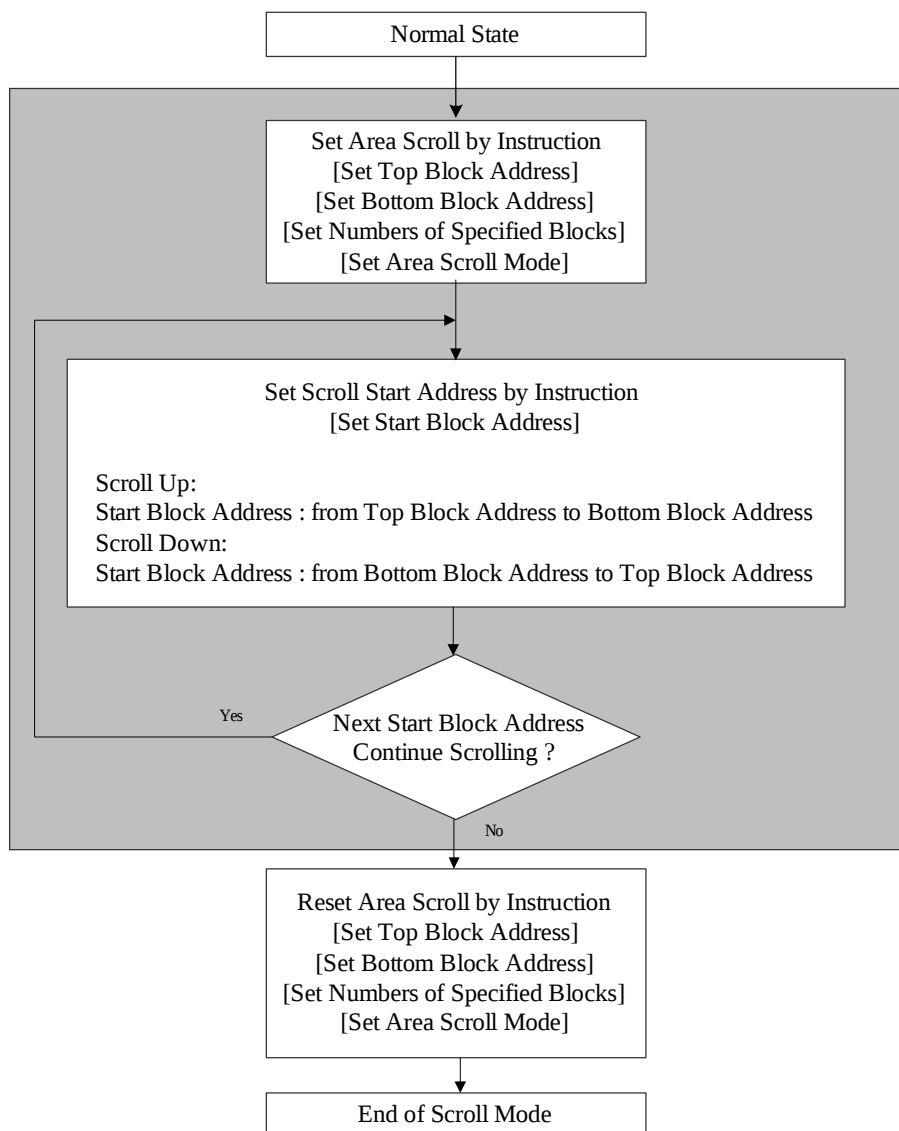


Figure 8.5.6.1 Scroll Display

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Example : Screen Scroll Operation

```
void CenterScreenScroll( void )  
{
```

```
    Write( COMMAND, 0x0030 );           // Ext = 0  
    Write( COMMAND, 0x00AA);           // Partial Display In Function  
    Write( DATA, 0x000A );            // Top_Block=10  
    Write( DATA, 0x0014 );            // Bottom_Block=20  
    Write( DATA, 0x0014 );            // Number of Specified Blocks=Bottom_Block=20  
    Write( DATA, 0x0000 );            // Area Scroll Type=Center Screen Scroll  
  
    ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down
```

```
}
```

```
void TopScreenScroll( void )  
{
```

```
    Write( COMMAND, 0x0030 );           // Ext = 0  
    Write( COMMAND, 0x00AA);           // Partial Display In Function  
    Write( DATA, 0x0000 );            // Top_Block=0  
    Write( DATA, 0x0014 );            // Bottom_Block=20  
    Write( DATA, 0x0014 );            // Number of Specified Blocks=Bottom_Block=20  
    Write( DATA, 0x0001 );            // Area Scroll Type=Top Screen Scroll  
  
    ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down
```

```
}
```

```
void BottomScreenScroll( void )  
{
```

```
    Write( COMMAND, 0x0030 );           // Ext = 0  
    Write( COMMAND, 0x00AA);           // Partial Display In Function  
    Write( DATA, 0x000A );            // Top_Block=10  
    Write( DATA, 0x0019 );            // Bottom_Block=25  
    Write( DATA, 0x0019 );            // Number of Specified Blocks=Bottom_Block=25  
    Write( DATA, 0x0002 );            // Area Scroll Type=Bottom Screen Scroll  
  
    ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down
```

```
}
```

```
void WholeScreenScroll( void )  
{
```

```
    Write( COMMAND, 0x0030 );           // Ext = 0  
    Write( COMMAND, 0x00AA);           // Partial Display In Function  
    Write( DATA, 0x0000 );            // Top_Block=0  
    Write( DATA, 0x0019 );            // Bottom_Block=25  
    Write( DATA, 0x0019 );            // Number of Specified Blocks=Bottom_Block=25  
    Write( DATA, 0x0003 );            // Area Scroll Type=Whole Screen Scroll  
  
    ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down
```

```
}
```

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```
void ScrollUp( void )
{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Top_Block);          // Start Block Address=Top_Block
    Delay();                           // Delay

    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Top_Block +1 );       // Start Block Address= Top_Block+1
    Delay();                           // Delay

    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Top_Block +2 );       // Start Block Address= Top_Block +2
    Delay();                           // Delay
    .....
    .....
    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Bottom_Block );       // Start Block Address= Bottom_Block
    Delay();                           // Delay
}

void ScrollDown( void )
{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Bottom_Block);        // Start Block Address= Bottom_Block
    Delay();                           // Delay

    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Bottom_Block -1 );    // Start Block Address= Bottom_Block -1
    Delay();                           // Delay

    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Bottom_Block -2 );    // Start Block Address= Bottom_Block -2
    Delay();                           // Delay
    .....
    .....
    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Top_Block );          // Start Block Address= Top_Block
    Delay();                           // Delay
}
```

8.5.7 Read-Modify-Write Cycle

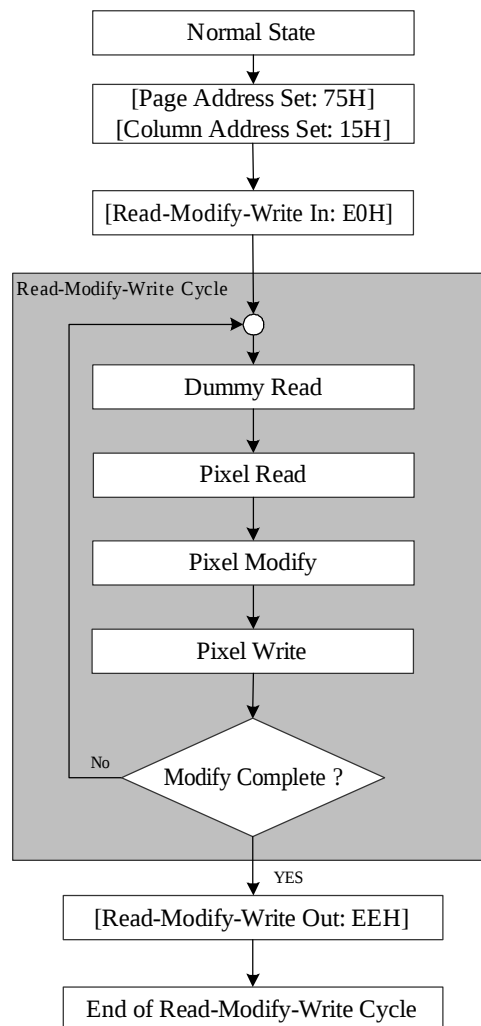


Figure 8.5.7.1 Read-Write-Modify Cycle

Example : Read-Write-Modify Cycle

```

void ReadModifyWriteIn( void )
{
    Write( COMMAND, 0x0030 );    // Ext = 0
    Write( COMMAND, 0x00E0 );    // Entry the Read-Modify-Write mode
}

void ReadModifyWriteOut( void )
{
    Write( COMMAND, 0x0030 );    // Ext = 0
    Write( COMMAND, 0x00EE );    // Out of partial display mode
}

extern unsigned char *display_pattern;
void main()
{
    unsigned pixel, i;

    Windowing( 11, 31, 80, 50 );    // set the page and column range
  
```

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```

ReadModifyWriteIn();                                // entry the Read-Modify-Write mode

for( i = 0 ; i < 1000 ; i++ )
{
    Read( DATA );                                // For dummy read
    pixel = Read( DATA );                        // Pixel read
    pixel = pixel & 0x07FF;                       // Pixel modify: red filter
    Write( DATA, pixel );
}

ReadModifyWriteOut();                              // Out of Read-Modify-Write mode
}

```

8.5.8 Display On / OFF

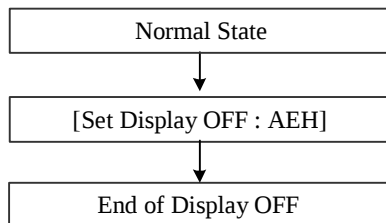


Figure 8.5.8.1 Display Off

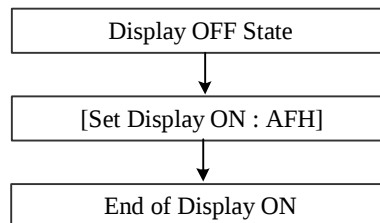


Figure 8.5.8.2 Display On

Example : Display OFF Operation

```

void DisplayOff( void )
{

```

Write(COMMAND, 0x0030);	// Ext = 0
Write(COMMAND, 0x00AE);	// Display Off

```

}

```

Example : Display ON Operation

```

void DisplayOn( void )
{

```

Write(COMMAND, 0x0030);	// Ext = 0
Write(COMMAND, 0x00AF);	// Display On

```

}

```

8.5.9 Power OFF

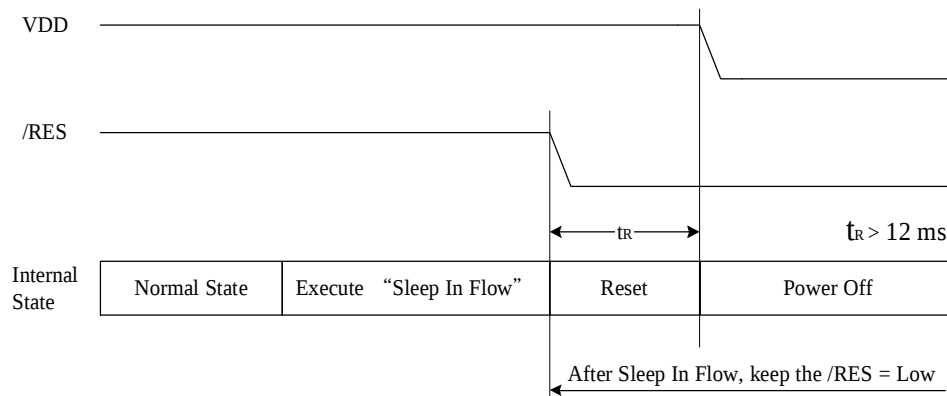
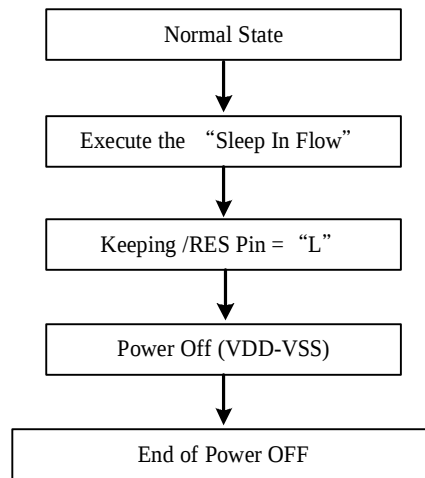


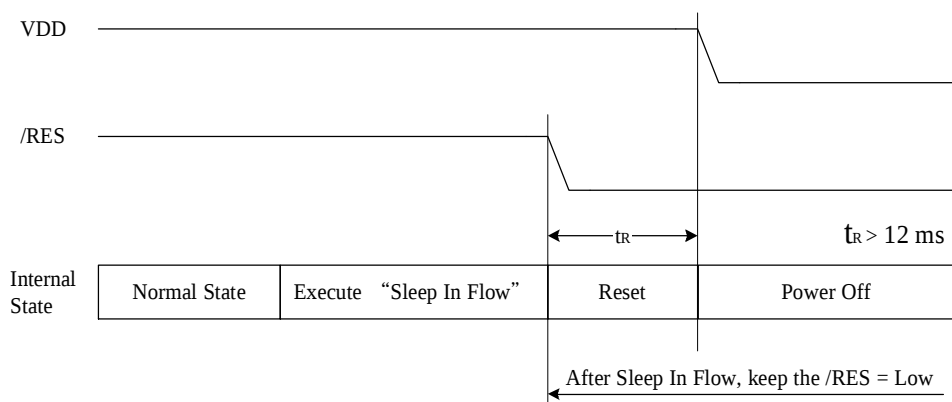
Figure 8.5.9.1 Power off

Note : The sequence is that users must set the VDD to low after keeping the /RES=low time longer than 12ms.

9. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD, VDD1~5	-0.5 ~ +4.0	V
Power supply voltage (VDD standard)	VOUT _{IN}	-0.5 ~ +20	V
Power supply voltage (VDD standard)	V1, V2, V3, V4	0.3 to VOUT _{IN}	V
Input voltage	VIN	-0.5 to VDD+0.5	V
Output voltage	VO	-0.5 to VDD+0.5	V
Operating temperature (Die)	TOPR	-30 to +85	°C
Storage temperature (Die)	TSTR	-40 to +125	°C



Notes

- Stresses above those listed under Limiting Values may cause permanent damage to the device.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
- Insure that the voltage levels of V1, V2, V3, and V4 are always such that
$$VOUT_{IN} \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V_{SS}$$
- V0 tolerance +/- 0.1V

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10. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS devices”).

11. DC CHARACTERISTICS

$V_{DD} = 2.4\text{ V to }3.3\text{V}$; $V_{SS} = 0\text{ V}$; $V_0 = 3.76\text{ to }18.0\text{V}$; $T_{amb} = -30^{\circ}\text{C to }+85^{\circ}\text{C}$; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		VDD VDD1			2.4	—	3.3	V	Vss
Operating Voltage (2)		VDD2 VDD3 VDD4 VDD5			2.4	—	3.3	V	VSS
High-level Input Voltage		VIHC			0.8 x VDD	—	VDD	V	*2
Low-level Input Voltage		VILC			VSS	—	0.2 x VDD	V	*2
High-level Output Voltage		VOHC			0.8 x VDD	—	VDD	V	*3
Low-level Output Voltage		VOLC			VSS	—	0.2 x VDD	V	*3
Input leakage current		ILI	VIN = VDD or VSS		−1.0	—	1.0	μA	*4
Output leakage current		ILO	VIN = VDD or VSS		−3.0	—	3.0	μA	*5
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C	VOUTIN = 15.0 V	—	2.0	—	KΩ	SEgN COMn *6
			(Relative To VSS)	VOUTIN = 8.0 V	—	3.2	—		
Oscillator Frequency	Internal Oscillator	fOSC	Ta = 25°C 1/104 duty 31 PWM		—	8.09	—	kHz	*7
	External Input	fCL			—	250.79	—	kHz	OSC
	Frame frequency	fFRAME			fFRAME=fOSC/(Duty+1)			Hz	

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	VDD	(Relative To VSS)	2.4	—	3.3	V	
	Supply Step-up output voltage Circuit	V_{OUT_OUT}	(Relative To VSS)	—	—	18	V	V_{OUT_OUT}
	Voltage regulator Circuit Operating Voltage	V_{OUT_IN}	(Relative To VSS)	—	—	18	V	V_{OUT_IN}

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Dynamic Consumption Current : During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used .

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern Normal	ISS	VDD = 2.8V, BoosterX7 V0 – VSS = 14.0 V, 1/11 Bias	—	350(die)	—	μ A	*8
Power Down	ISS	Ta = 25°C	—	—	10	μ A	die

PS.V0 tolerance +/- 0.1V

Notes to the DC characteristics

1. The maximum possible V_{OUT} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock
3. Power-down mode. During power down all static currents are switched off.
4. If external V_{OUT}, the display load current is not transmitted to I_{DD}.
5. V_{OUT} external voltage applied to VOUT_{IN} pin; VOUT_{IN} disconnected from VOUT_{OUT}

References for items market with *

- *1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.
- *2 The A0, D0 to D5, D6 (SI), D7 (SCL), D8 to D15, /RD (E), /WR ,/(R/W), /CS, and RESB terminals.
- *3 The D0 to D7 terminals.
- *4 The A0,/RD (E), /WR ,/(R/W), /CS, and RESB terminals.
- *5 Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.
- *6 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range.
RON = 0.1 V / Δ I (Where Δ I is the current that flows when 0.1 V is applied while the power supply is ON.)
- *7 The relationship between the oscillator frequency and the frame rate frequency.
- *8,9It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.

12. TIMING CHARACTERISTICS

Condition : Bare Die

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

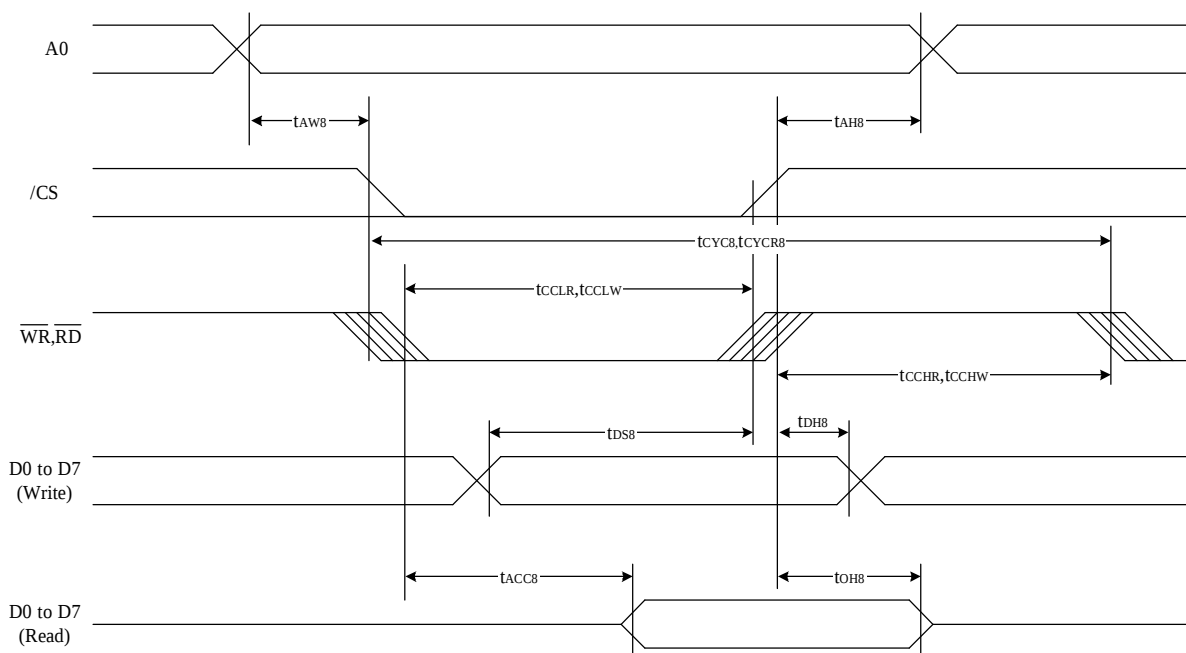


Figure 39.

(VDD = 3.3V , Ta = -30°C~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAW8		10	—	
System cycle time	WR	tCYC8		150	—	
System cycle frequency		fCYC8		6.67	—	MHz
Enable L pulse width (WRITE)		tCCLW		50	—	ns
Enable H pulse width (WRITE)		tCCHW		100	—	
System cycle time(READ)	RD	tCYCR8		490	—	
Enable L pulse width (READ)		tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		350	—	
WRITE data setup time	D0 to D7	tDS8		70	—	
WRITE data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	—	50	

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(VDD = 2.8 V , Ta = -30°C~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAW8		10	—	
System cycle time	WR	tCYC8		180	—	MHz
System cycle frequency		fCYC8		5.56	—	
Enable L pulse width (WRITE)		tCCLW		60	—	
Enable H pulse width (WRITE)		tCCHW		120	—	
System cycle time(READ)	RD	tCYCR8		620		ns
Enable L pulse width (READ)		tCCLR		190	—	
Enable H pulse width (READ)		tCCHR		420	—	
WRITE data setup time	D0 to D7	tDS8		80	—	
WRITE data hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	—	100	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(tr + tf) \leq (tCYC8 - tCCLW - tCCHW)$ for $(tr + tf) \leq (tCYC8 - tCCLR - tCCHR)$ are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between /CS being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

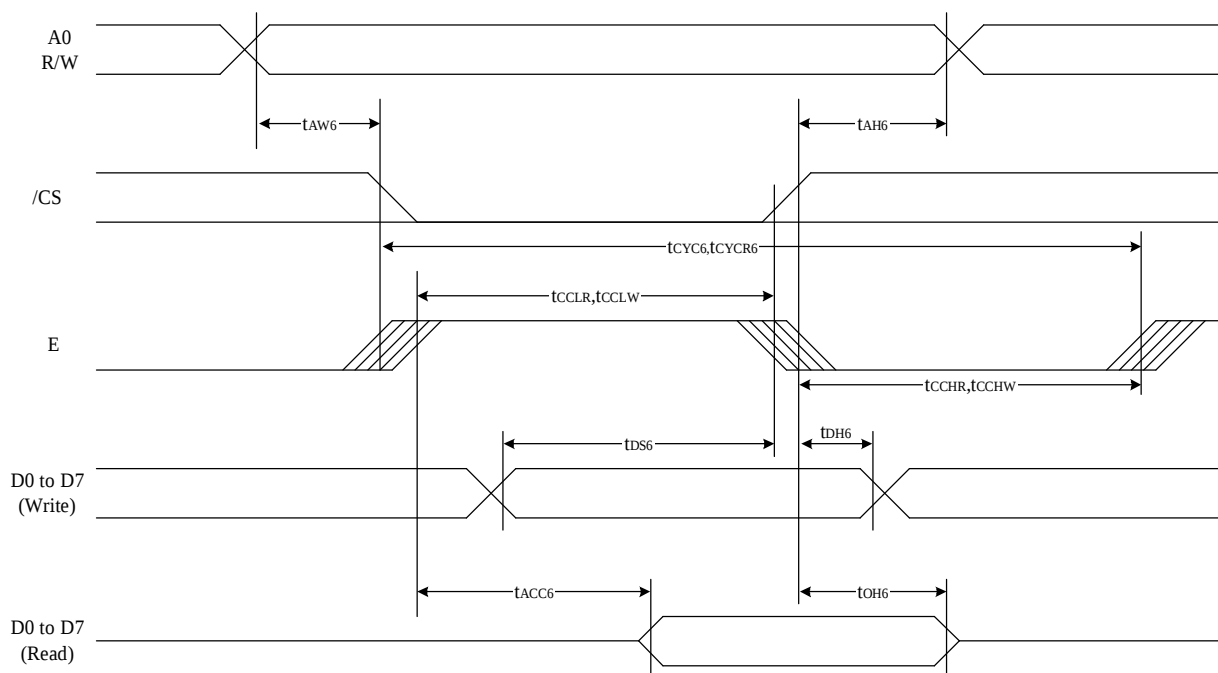


Figure 40.

(V_{DD} = 3.3 V , T_a = -30°C–85°C , die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAW6		10	—	
System cycle time	WR	tCYC6		150	—	
System cycle frequency		fCYC6		6.67	—	MHz
Enable L pulse width (WRITE)		tEWLW		90	—	ns
Enable H pulse width (WRITE)		tEWHW		60	—	
System cycle time(READ)	RD	tCYCR6		500	—	
Enable L pulse width (READ)		tEWLR		340	—	
Enable H pulse width (READ)		tEWHR		160	—	
WRITE data setup time	D0 to D7	tDS6		70	—	
WRITE data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	—	50	

(VDD = 2.8V , Ta = -30°C~85°C , die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAW6		10	—	
System cycle time	WR	tCYC6		180	—	MHz
System cycle frequency		fCYC6		5.56	—	
Enable L pulse width (WRITE)		tEWLW		110	—	
Enable H pulse width (WRITE)	RD	tEWHW		70	—	ns
System cycle time(READ)		tCYCR6		590	—	
Enable L pulse width (READ)		tEWLR		400	—	
Enable H pulse width (READ)	D0 to D7	tEWHR		190	—	
WRITE data setup time		tDS6		80	—	
WRITE data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	—	100	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(tr + tf) \leq (tCYC6 - tEWLW - tEWHW)$ for $(tr + tf) \leq (tCYC6 - tEWLR - tEWHR)$ are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between /CS being “L” and E.

SERIAL INTERFACE(4-Line Interface)

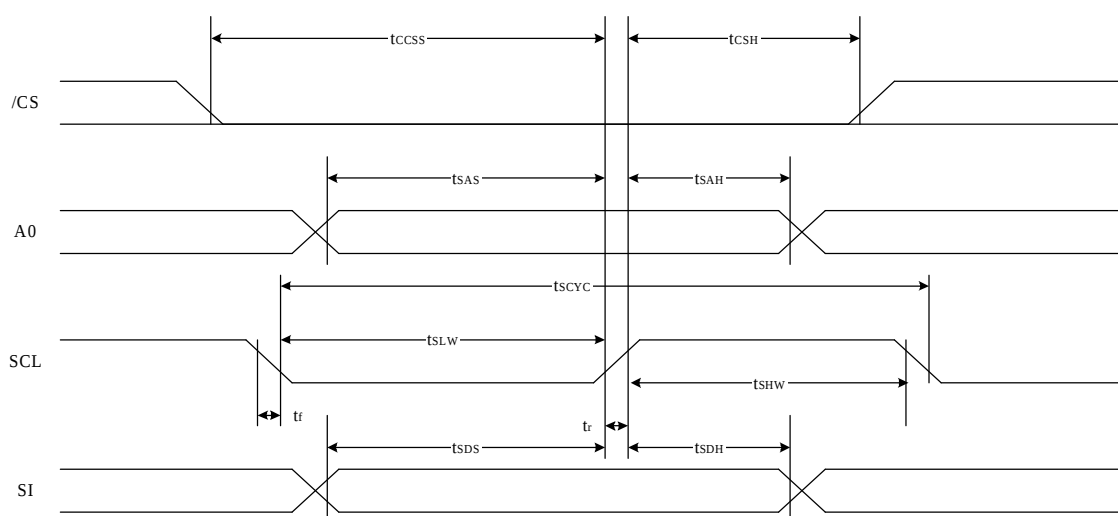


Fig 41.

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(V_{DD}=3.3V, Ta =-30°C~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		100	—	ns
Serial clock frequency		fSCYC		10		MHz
SCL “H” pulse width		tSHW		70	—	ns
SCL “L” pulse width		tSLW		30	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		50	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		30	—	
CS-SCL time	/CS	tCSS		20	—	
CS-SCL time		tCSH		50	—	

(V_{DD}=2.8V, Ta =-30°C~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		110	—	ns
Serial clock frequency		fSCYC		9.09		MHz
SCL “H” pulse width		tSHW		80	—	ns
SCL “L” pulse width		tSLW		30	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		50	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		30	—	
CS-SCL time	/CS	tCSS		20	—	
CS-SCL time		tCSH		60	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE(3-Line Interface)

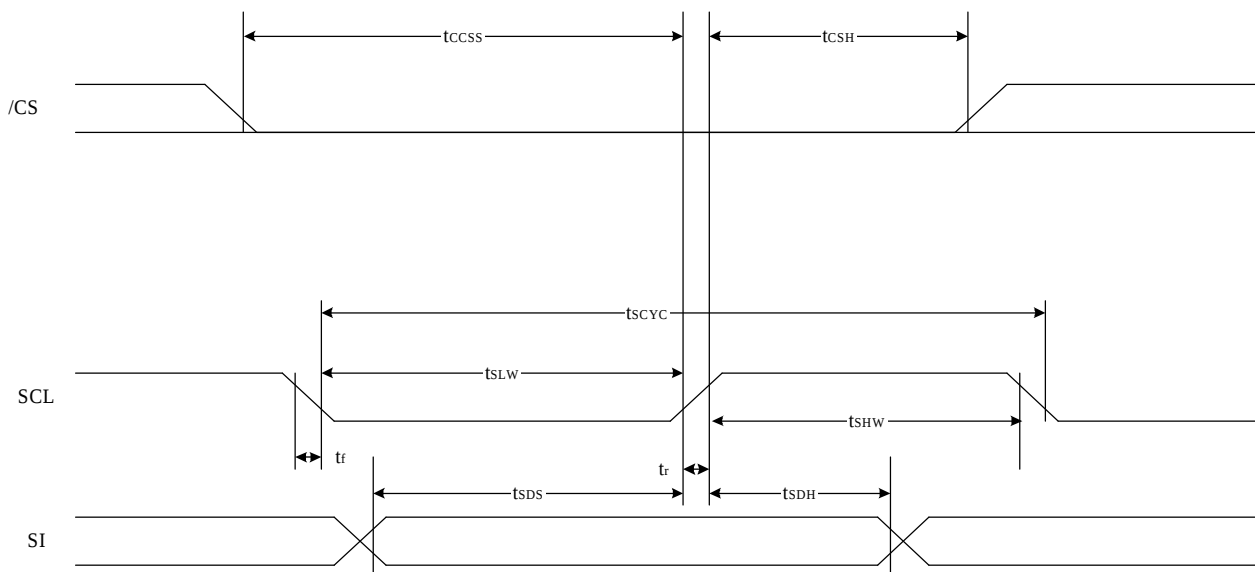


Fig 42.

($V_{DD}=3.3V$, $T_a = -30^{\circ}C \sim 85^{\circ}C$, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		100	—	ns
Serial clock frequency		fSCYC		10		MHz
SCL "H" pulse width		tSHW		70	—	ns
SCL "L" pulse width		tSLW		30	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		30	—	
CS-SCL time	$\overline{CS}$	tCSS		20	—	
CS-SCL time		tCSH		60	—	

($V_{DD}=2.8V$, $T_a = -30^{\circ}C \sim 85^{\circ}C$, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		110	—	ns
Serial clock frequency		fSCYC		9.09		MHz
SCL "H" pulse width		tSHW		80	—	ns
SCL "L" pulse width		tSLW		30	—	
Data setup time	SI	tSDS		20	—	
Data hold time		tSDH		40	—	
CS-SCL time	$\overline{CS}$	tCSS		20	—	
CS-SCL time		tCSH		60	—	

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*1 The input signal rise and fall time (t_r , t_f) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

13. RESET TIMING

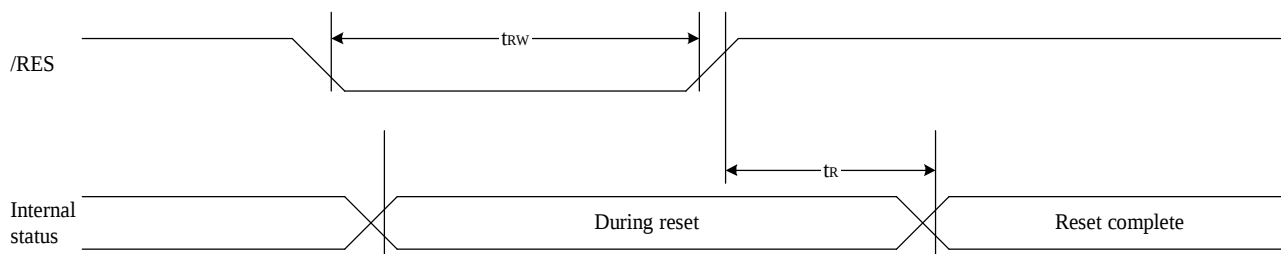


Fig 43.

($V_{DD} = 3.3V$, $T_a = -30$ to $85^\circ C$, die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1	us
Reset "L" pulse width	RESB	t_{RW}		1	—	—	us

($V_{DD} = 2.8V$, $T_a = -30$ to $85^\circ C$, die)

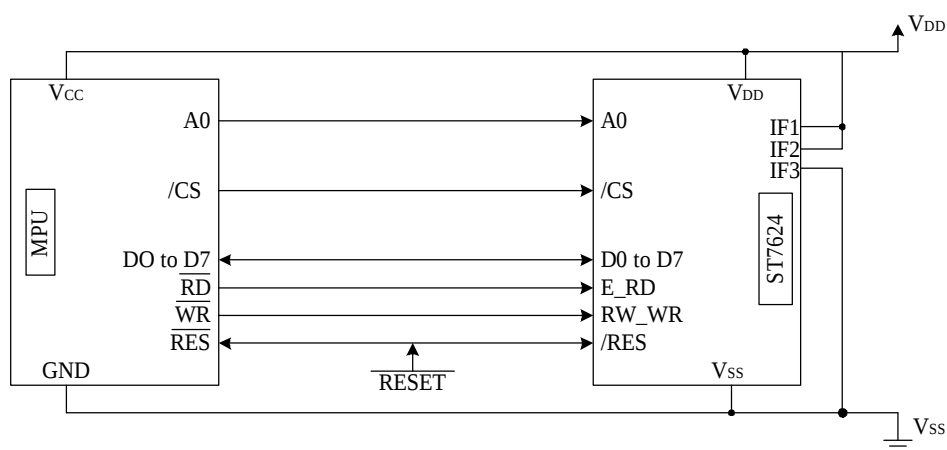
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.5	us
Reset "L" pulse width	RESB	t_{RW}		1.5	—	—	us

14. THE MPU INTERFACE (REFERENCE EXAMPLES)

The ST7624 Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7624 series chips with fewer signal lines.

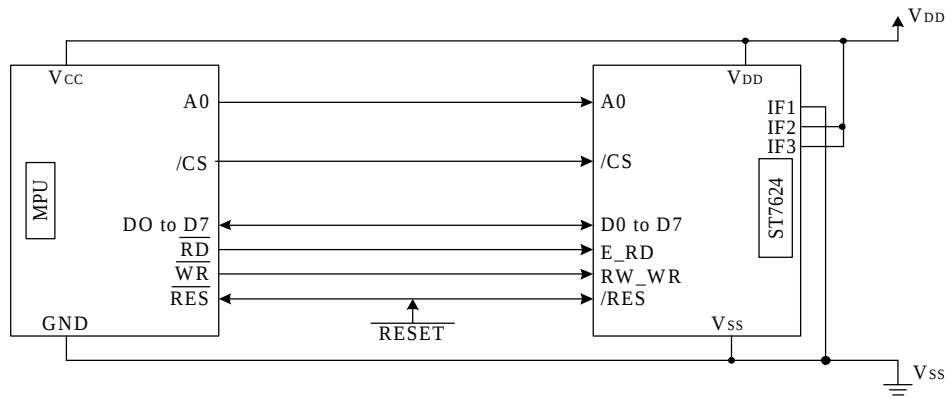
The display area can be enlarged by using multiple ST7624 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

(1) 8080-8bits Series MPUs

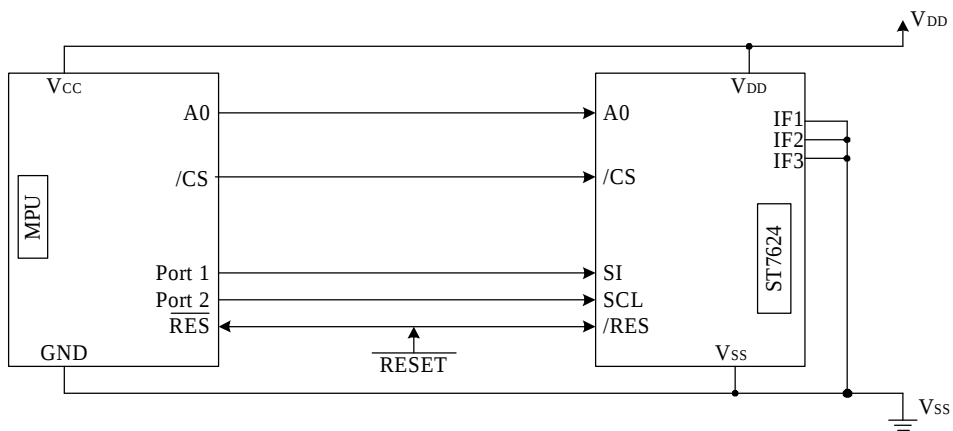


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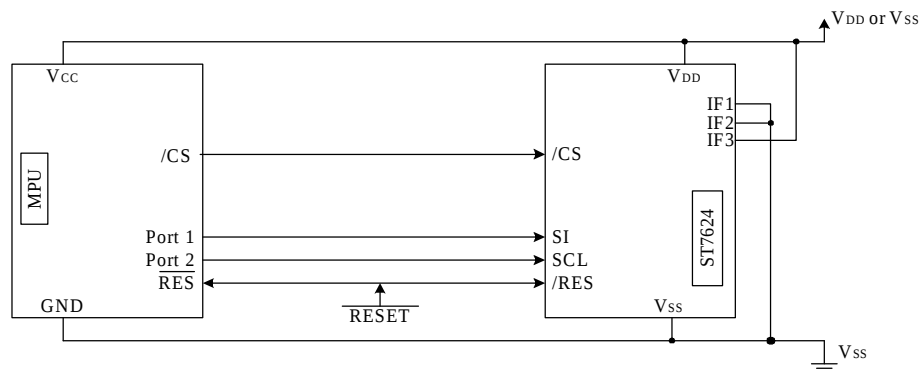
(2) 6800-8bits Series MPUs



(3) Using the Serial Interface (4-line interface)



(4) Using the Serial Interface (3-line interface)



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15.APPLICATION NOTE

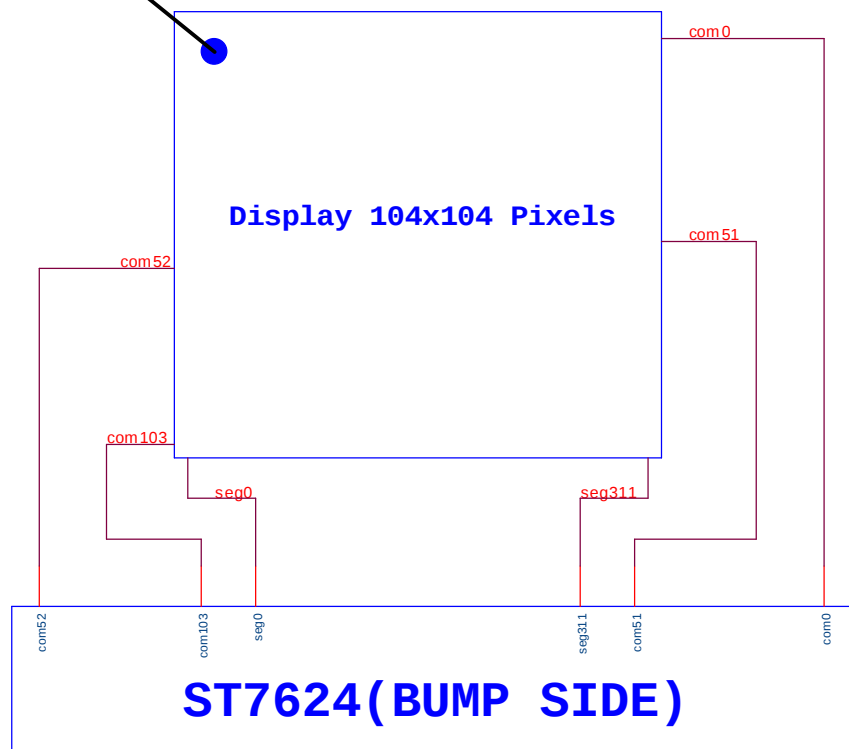
Resolution : 104 X 104 Color start pixel

CSEL = L

Common Scan Command : BBH

Parameter : P12,P11,P10=001

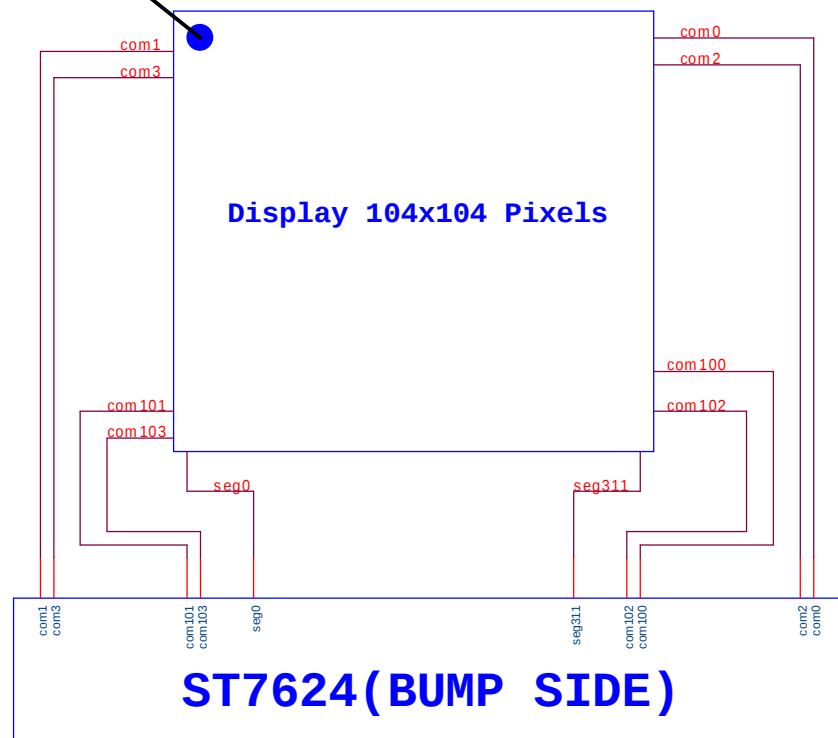
(Reference Page 45)



Resolution : 104 X 104 Color

CSEL = H

start pixel

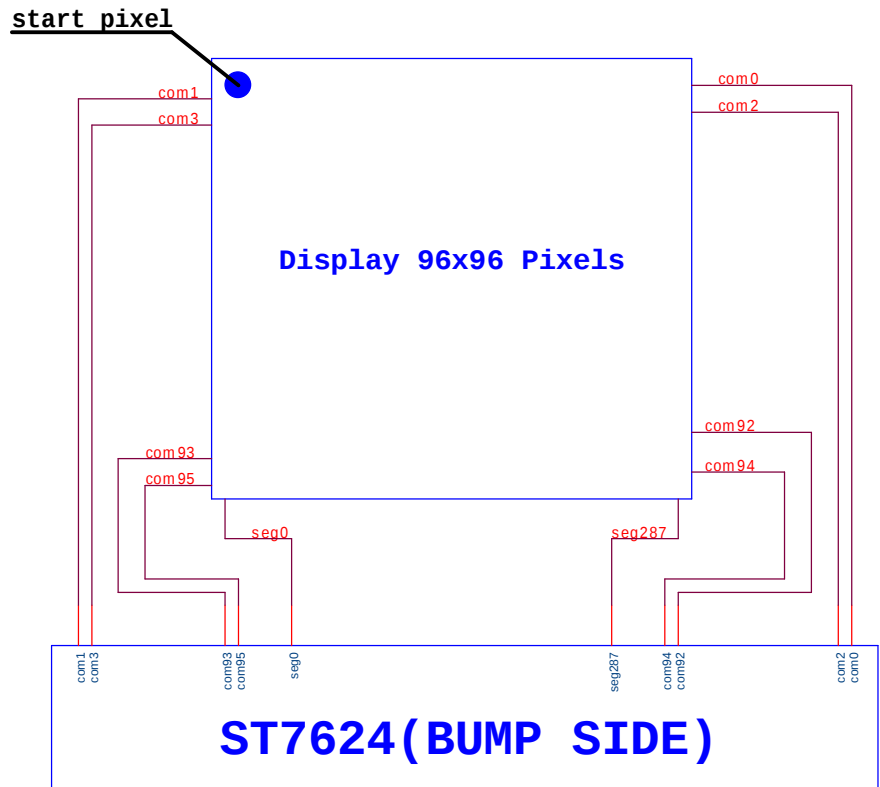


Note : the View Angle of panel can be changed by software(Command BCH)

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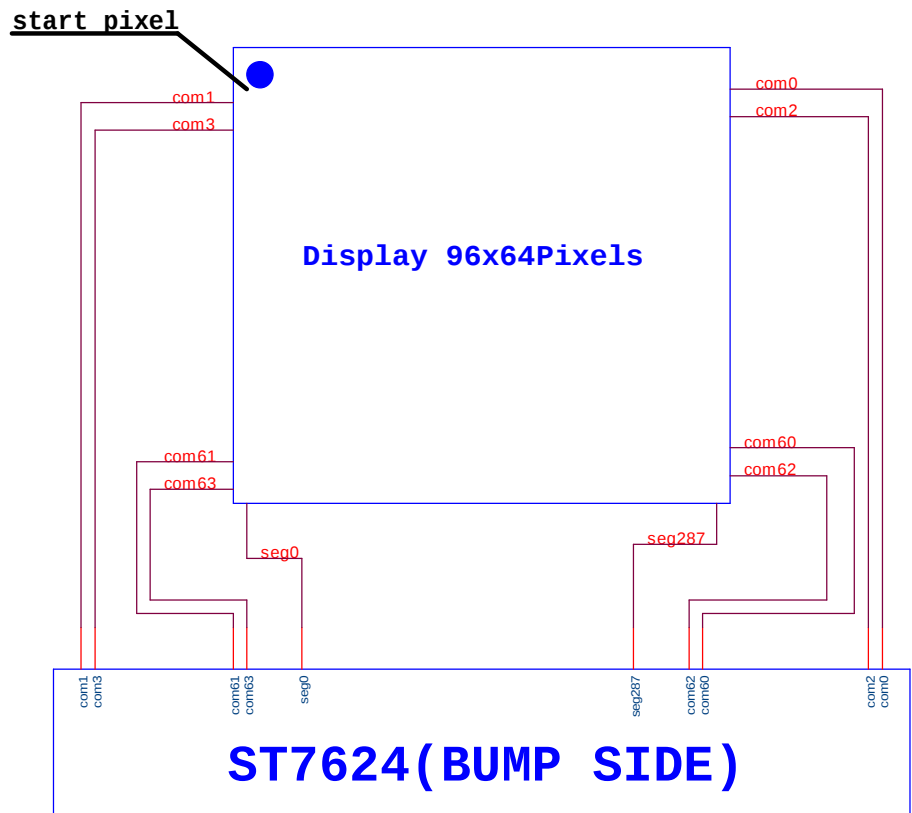
Resolution : 96 X 96 Color

CSEL = H



Resolution : 96 X 64 Color

CSEL = H



Note : the View Angle of panel can be changed by software(Command BCH)

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Interface : 8080series-8bits

VDD,VDD1=2.4V~3.3V

VDD2~VDD5=2.4V~3.3V

Booster : X7

CSEL = H

IF1 = H ; IF2 = H ; IF3 = L

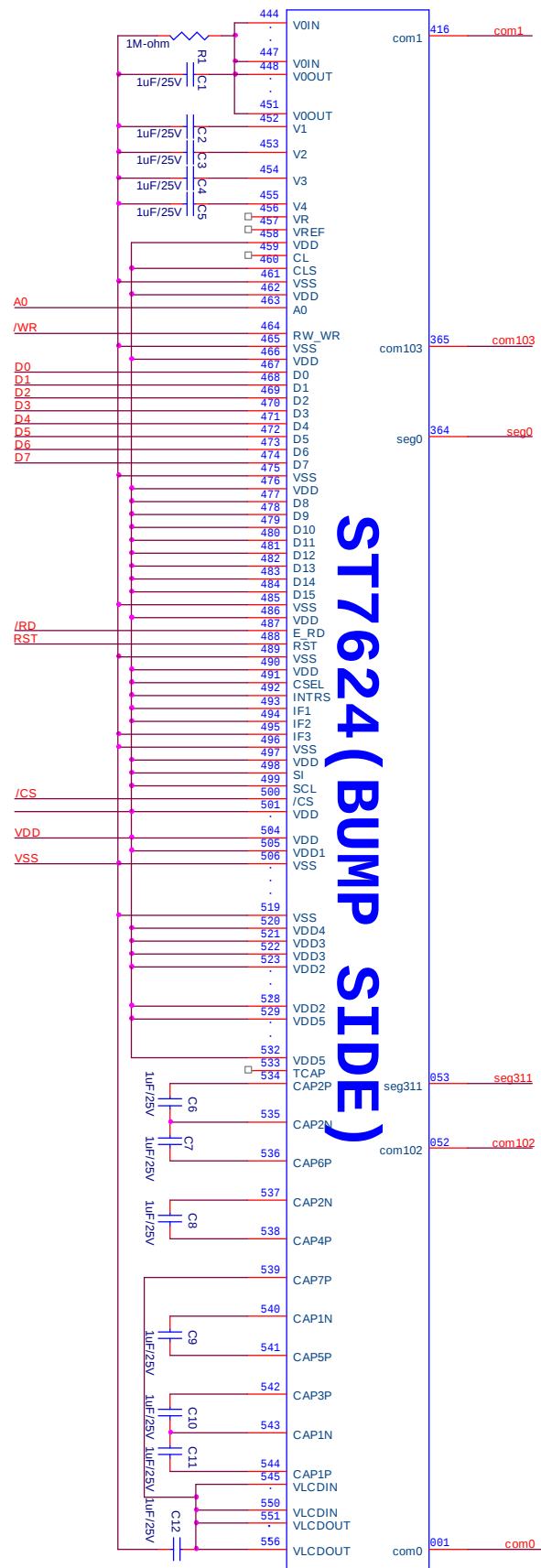
C1~C5 : 0.1uF~1.0uF/25V

C6~C13 : 1.0~2.2uF/25V

Vop = 12~15V

Bias = 1/11(under 1/104 duty)

R1=1M-ohm



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Interface : 8080series-16bits

VDD,VDD1=2.4V~3.3V

VDD2~VDD5=2.4V~3.3V

Booster : X7

CSEL = H

IF1 = H ; IF2 = H ; IF3 = H

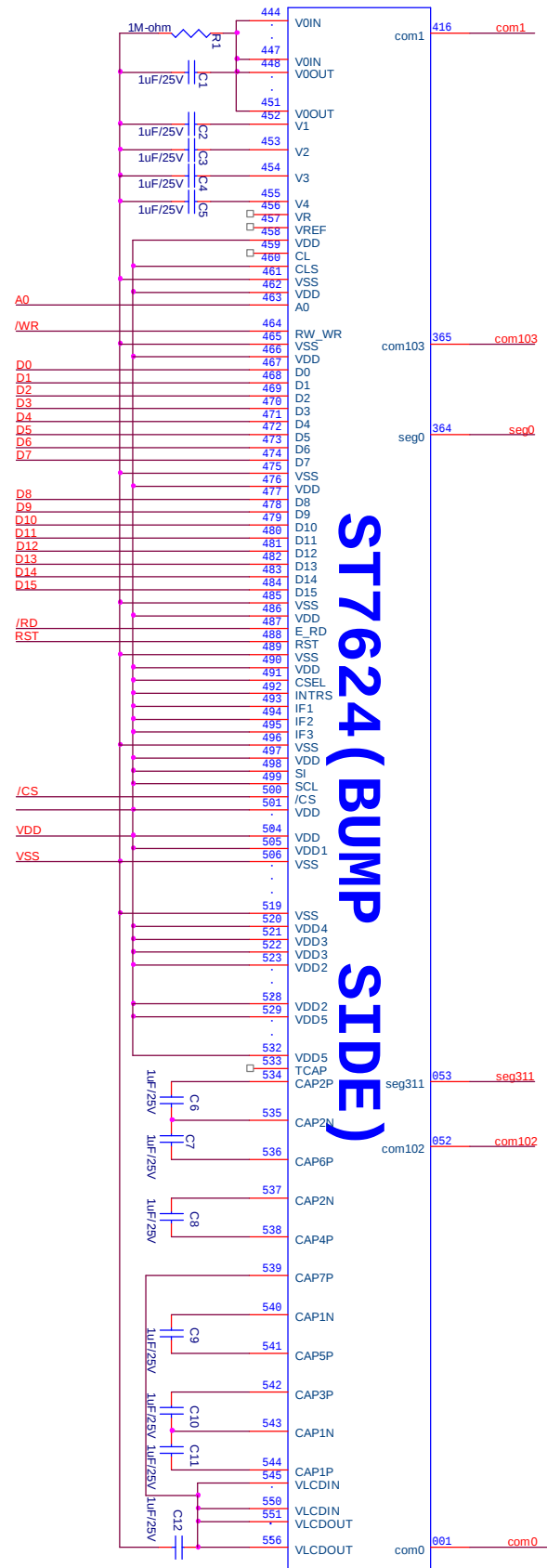
C1~C5 : 0.1uF~1.0uF/25V

C6~C13 : 1.0~2.2uF/25V

Vop = 12~15V

Bias = 1/11(under 1/104 duty)

R1=1M-ohm



ST7624

Interface : 6800series-8bits

VDD,VDD1=2.4V~3.3V

VDD2~VDD5=2.4V~3.3V

Booster : X7

CSEL = H

IF1 = L ; IF2 = H ; IF3 = H

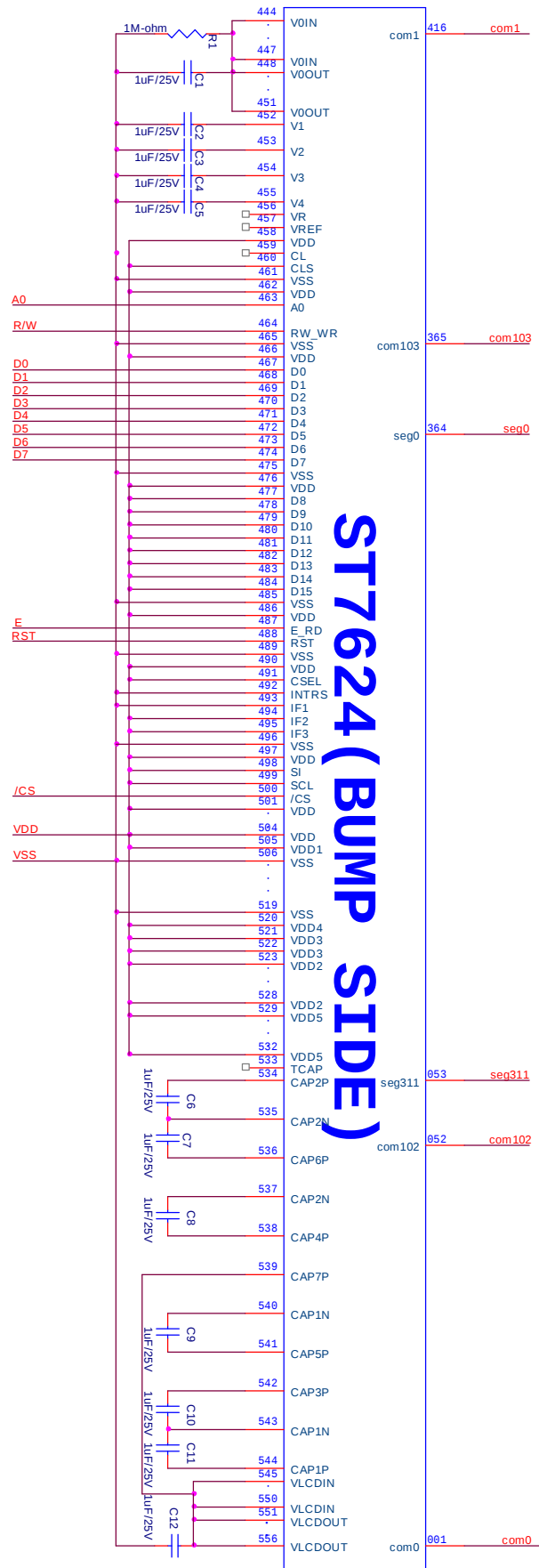
C1~C5 : 0.1uF~1.0uF/25V

C6~C13 : 1.0~2.2uF/25V

Vop = 12~15V

Bias = 1/11(under 1/104 duty)

R1=1M-ohm



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Interface : 6800series-16bits

VDD,VDD1=2.4V~3.3V

VDD2~VDD5=2.4V~3.3V

Booster : X7

CSEL = H

IF1 = H ; IF2 = L ; IF3 = L

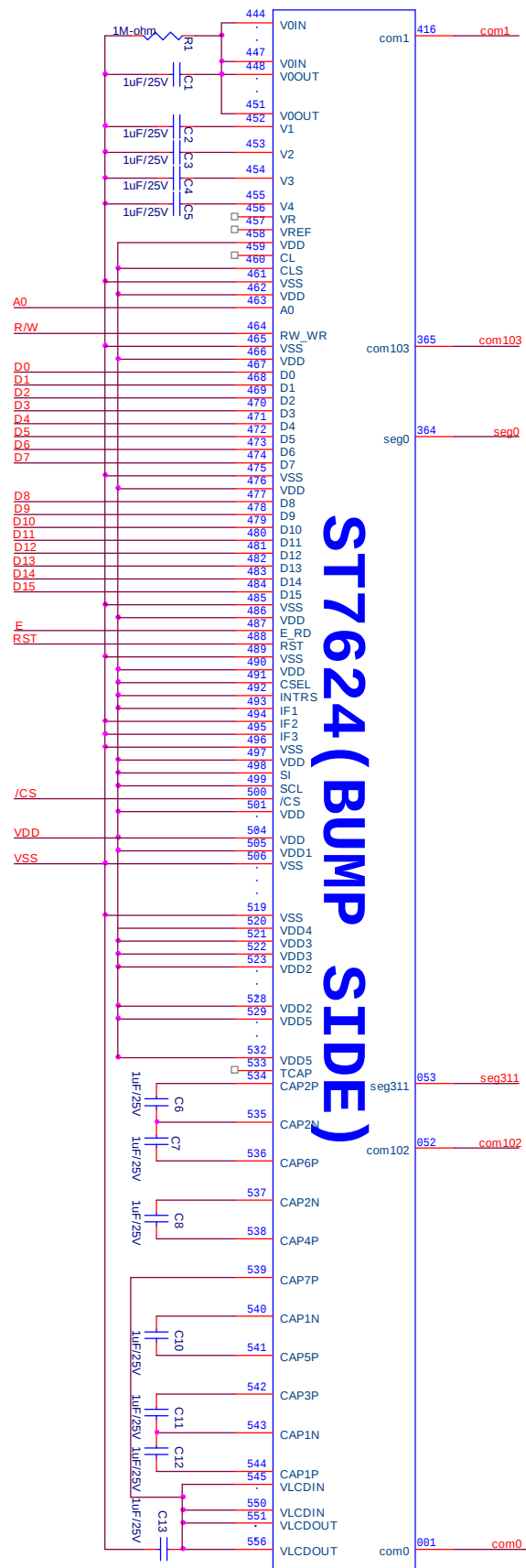
C1~C5 : 0.1uF~1.0uF/25V

C6~C13 : 1.0~2.2uF/25V

Vop = 12~15V

Bias = 1/11(under 1/104 duty)

R1=1M-ohm



ST7624

Interface : 4-line

VDD,VDD1=2.4V~3.3V

VDD2~VDD5=2.4V~3.3V

Booster : X7

CSEL = H

IF1 = L ; IF2 = L ; IF3 = L

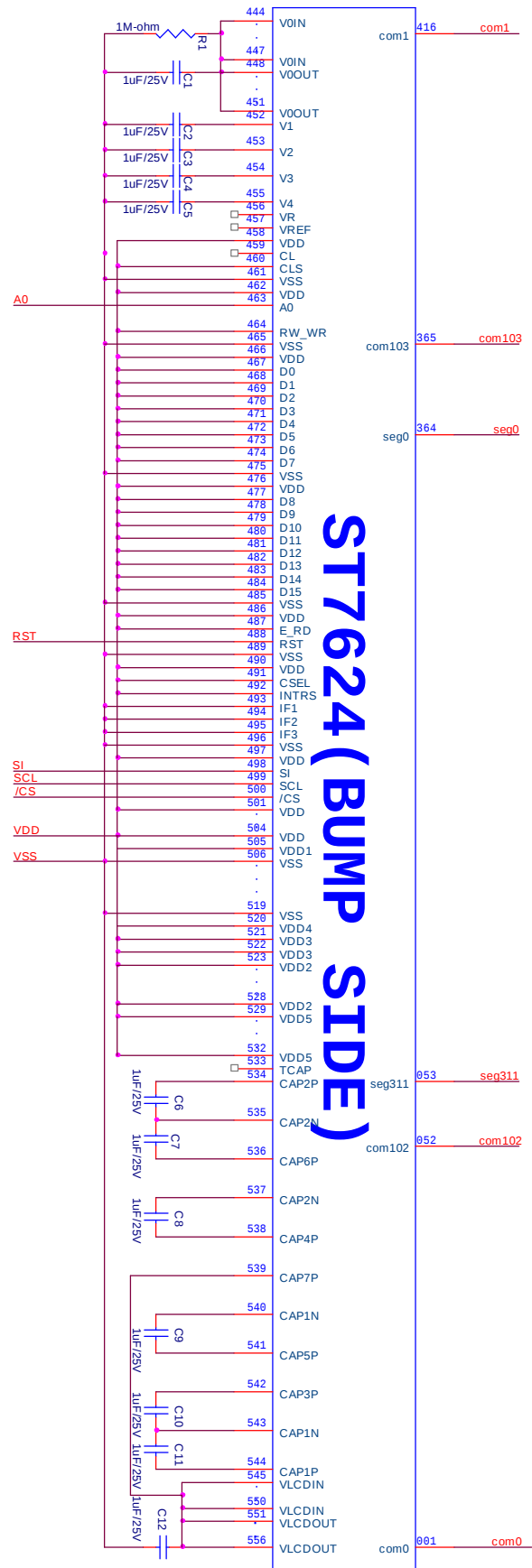
C1~C5 : 0.1uF~1.0uF/25V

C6~C13 : 1.0~2.2uF/25V

Vop = 12~15V

Bias = 1/11(under 1/104 duty)

R1=1M-ohm



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Interface : 3-line

VDD,VDD1=2.4V~3.3V

VDD2~VDD5=2.4V~3.3V

Booster : X7

CSEL = H

IF1 = L ; IF2 = L ; IF3 = H

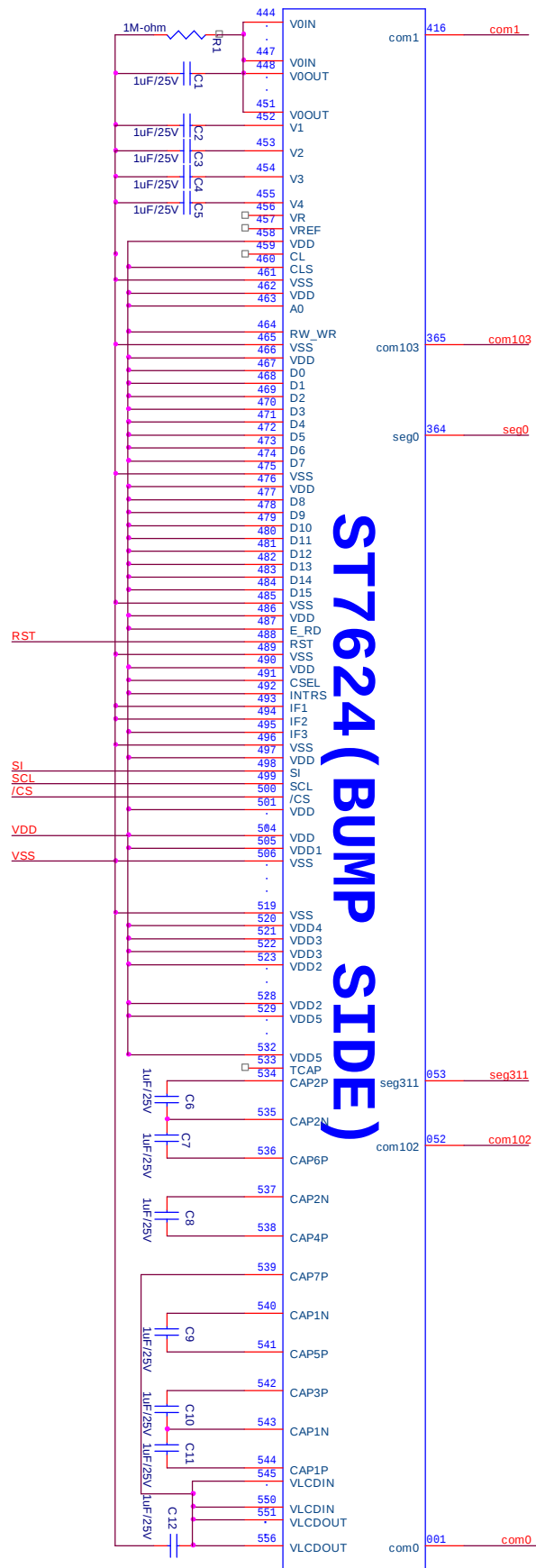
C1~C5 : 0.1uF~1.0uF/25V

C6~C13 : 1.0~2.2uF/25V

Vop = 12~15V

Bias = 1/11(under 1/104 duty)

R1=1M-ohm



NOTE: Microprocessor interface pins should not be floating in any operation mode.

ST7624

ST7624 Specification Revision History		
Version	Date	Description
1.0	2004/12/08	Remove Preliminary and modify Timing Characteristic
1.1	2005/01/14	Correct 8080/6800 interface Timing
1.2	2005/03/12	Modify EEPROM flow and Parallel Timing
1.3	2005/05/03	Remove IIC Interface
1.4	2005/05/18	Modify Program Flow
1.5	2005/06/02	Modify Application Note
1.6	2005/09/07	Modify Limiting Value and DC Characteristic 1. Temperature gradient (Add tolerance) on Page1 2. supply voltage (no tolerance). 3. Bump height on Page2 4. Operating and storage temperature.
1.7	2005/9/15	1. Add die in Temperature Range of Time 2. Add die in Display on Current (Typ)
1.8	2006/8/15	Add microprocessor notice item(p.14, p.97).