Sitronix

ST7626

65K Color Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7626 is a driver & controller LSI for 65K color graphic dot-matrix liquid crystal display systems. It generates 294 Segment and 68 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit/16-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

- 294 Segment Outputs / 68 Common Outputs

Applicable Duty Ratios

- Various Partial Display
- Partial Window Moving & Data Scrolling

Gray-Scale Display

- 4FRC & 31 PWM function circuit to display
- 64 gray-scale display.

On-chip Display Data RAM

- Capacity: 98 x 68 x 16 =106,624 bits
- 4K colors (RGB)=(444) mode
- 65K colors (RGB)=(565) mode
- Truncated 262K colors (RGB)=(666) mode
- Truncated 16M colors (RGB)=(888) mode

Microprocessor Interface

- 8/16-bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line serial interface (4-line-SIF)
- 3-line serial interface (3-line-SIF)

On-chip Low Power Analog Circuit

- On-chip Oscillator Circuit
- On-chip Voltage Converter (x2, x3, x4, x5) with internal booster capacitors.
- Extremely Few Outsider Compoment. (Minimum required outsider compoments: One Capacitor).
- On-chip Voltage Regulator (Temperature gradient = -0.065%/°C)
- On-chip Electronic Contrast Control Function (406 steps)
- Voltage Follower (LCD bias: 1/5 to 1/12)

Operating Voltage Range

- Supply Digital Voltage (VDD, VDD1): 1.8 to 3.3V
- Supply Analog Voltage (VDD2, VDD3, VDD4, VDD5): 2.4 to 3.3V
- LCD Driving Voltage (VOP = V0 - VSS): 3.76V to 18V
- The suggested value of V0 is under 11 V with bias =1/9.

LCD Driving Voltage (EEPROM)

- Contrast Adjustment Value is stored in the Built-In EEPROM for better display quility.

LCM Performance Adjustment (EEPROM)

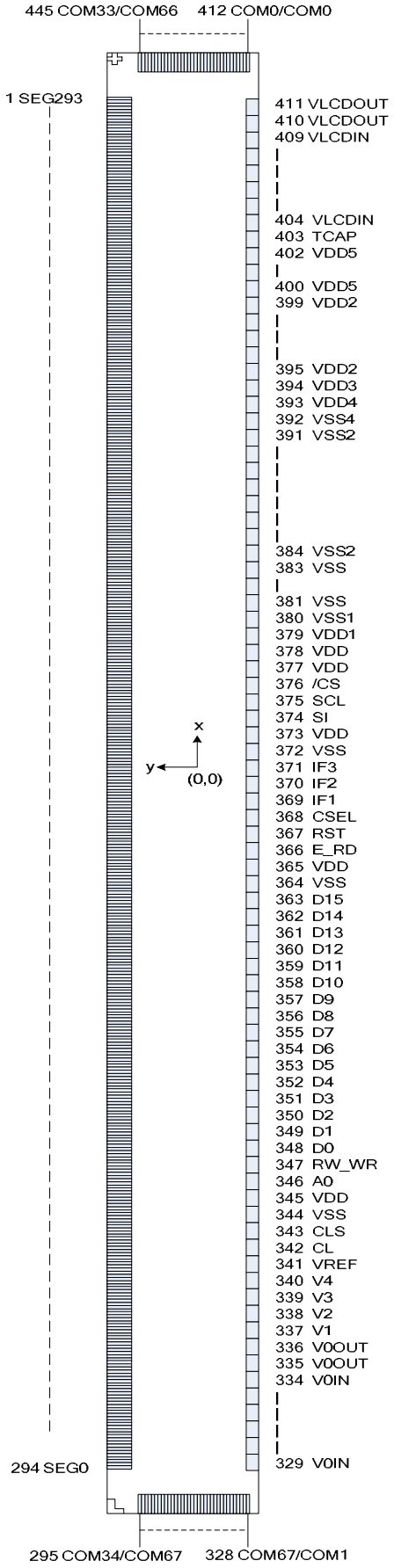
- Adjustment Value for best Display Performance is stored in the Built-In EEPROM.

Package Type

- Application for COG

ST7626	6800 , 8080 ,4-Line , 3-Line interface	ST

3. ST7626 Pad Arrangement (COG)



Chip Size : 9,717 um x 1,352.7 um

Bump Pitch :

PAD NO.1~328, 412~445 : 31 um (COM/SEG)

PAD NO.329~341, 342~411, : 110 um (I/O)

PAD NO.341~342 : 114.7 um (I/O)

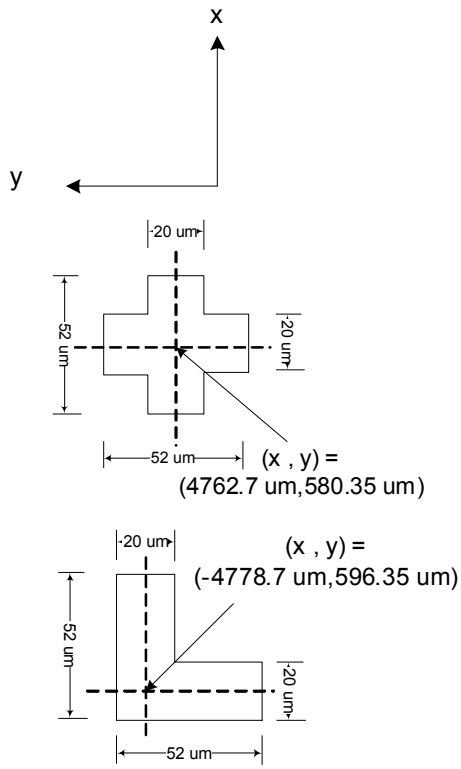
Bump Size :

PAD NO.1~328, 412~445 : 16 um(x) X 118 um(y)

PAD NO.329~411 : 95 um(x) X 50 um(y)

Bump Height : 15 um

Chip Thickness : 400 um



4. Pad Center Coordinates

PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
001	SEG[293]		4541.5	545.35
002	SEG[292]		4510.5	545.35
003	SEG[291]		4479.5	545.35
004	SEG[290]		4448.5	545.35
005	SEG[289]		4417.5	545.35
006	SEG[288]		4386.5	545.35
007	SEG[287]		4355.5	545.35
008	SEG[286]		4324.5	545.35
009	SEG[285]		4293.5	545.35
010	SEG[284]		4262.5	545.35
011	SEG[283]		4231.5	545.35
012	SEG[282]		4200.5	545.35
013	SEG[281]		4169.5	545.35
014	SEG[280]		4138.5	545.35
015	SEG[279]		4107.5	545.35
016	SEG[278]		4076.5	545.35
017	SEG[277]		4045.5	545.35
018	SEG[276]		4014.5	545.35
019	SEG[275]		3983.5	545.35
020	SEG[274]		3952.5	545.35
021	SEG[273]		3921.5	545.35
022	SEG[272]		3890.5	545.35
023	SEG[271]		3859.5	545.35
024	SEG[270]		3828.5	545.35
025	SEG[269]		3797.5	545.35
026	SEG[268]		3766.5	545.35
027	SEG[267]		3735.5	545.35
028	SEG[266]		3704.5	545.35
029	SEG[265]		3673.5	545.35
030	SEG[264]		3642.5	545.35
031	SEG[263]		3611.5	545.35
032	SEG[262]		3580.5	545.35
033	SEG[261]		3549.5	545.35

PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
034	SEG[260]		3518.5	545.35
035	SEG[259]		3487.5	545.35
036	SEG[258]		3456.5	545.35
037	SEG[257]		3425.5	545.35
038	SEG[256]		3394.5	545.35
039	SEG[255]		3363.5	545.35
040	SEG[254]		3332.5	545.35
041	SEG[253]		3301.5	545.35
042	SEG[252]		3270.5	545.35
043	SEG[251]		3239.5	545.35
044	SEG[250]		3208.5	545.35
045	SEG[249]		3177.5	545.35
046	SEG[248]		3146.5	545.35
047	SEG[247]		3115.5	545.35
048	SEG[246]		3084.5	545.35
049	SEG[245]		3053.5	545.35
050	SEG[244]		3022.5	545.35
051	SEG[243]		2991.5	545.35
052	SEG[242]		2960.5	545.35
053	SEG[241]		2929.5	545.35
054	SEG[240]		2898.5	545.35
055	SEG[239]		2867.5	545.35
056	SEG[238]		2836.5	545.35
057	SEG[237]		2805.5	545.35
058	SEG[236]		2774.5	545.35
059	SEG[235]		2743.5	545.35
060	SEG[234]		2712.5	545.35
061	SEG[233]		2681.5	545.35
062	SEG[232]		2650.5	545.35
063	SEG[231]		2619.5	545.35
064	SEG[230]		2588.5	545.35
065	SEG[229]		2557.5	545.35
066	SEG[228]		2526.5	545.35

PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
067	SEG[227]		2495.5	545.35
068	SEG[226]		2464.5	545.35
069	SEG[225]		2433.5	545.35
070	SEG[224]		2402.5	545.35
071	SEG[223]		2371.5	545.35
072	SEG[222]		2340.5	545.35
073	SEG[221]		2309.5	545.35
074	SEG[220]		2278.5	545.35
075	SEG[219]		2247.5	545.35
076	SEG[218]		2216.5	545.35
077	SEG[217]		2185.5	545.35
078	SEG[216]		2154.5	545.35
079	SEG[215]		2123.5	545.35
080	SEG[214]		2092.5	545.35
081	SEG[213]		2061.5	545.35
082	SEG[212]		2030.5	545.35
083	SEG[211]		1999.5	545.35
084	SEG[210]		1968.5	545.35
085	SEG[209]		1937.5	545.35
086	SEG[208]		1906.5	545.35
087	SEG[207]		1875.5	545.35
088	SEG[206]		1844.5	545.35
089	SEG[205]		1813.5	545.35
090	SEG[204]		1782.5	545.35
091	SEG[203]		1751.5	545.35
092	SEG[202]		1720.5	545.35
093	SEG[201]		1689.5	545.35
094	SEG[200]		1658.5	545.35
095	SEG[199]		1627.5	545.35
096	SEG[198]		1596.5	545.35
097	SEG[197]		1565.5	545.35
098	SEG[196]		1534.5	545.35
099	SEG[195]		1503.5	545.35
100	SEG[194]		1472.5	545.35
101	SEG[193]		1441.5	545.35

PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
102	SEG[192]		1410.5	545.35
103	SEG[191]		1379.5	545.35
104	SEG[190]		1348.5	545.35
105	SEG[189]		1317.5	545.35
106	SEG[188]		1286.5	545.35
107	SEG[187]		1255.5	545.35
108	SEG[186]		1224.5	545.35
109	SEG[185]		1193.5	545.35
110	SEG[184]		1162.5	545.35
111	SEG[183]		1131.5	545.35
112	SEG[182]		1100.5	545.35
113	SEG[181]		1069.5	545.35
114	SEG[180]		1038.5	545.35
115	SEG[179]		1007.5	545.35
116	SEG[178]		976.5	545.35
117	SEG[177]		945.5	545.35
118	SEG[176]		914.5	545.35
119	SEG[175]		883.5	545.35
120	SEG[174]		852.5	545.35
121	SEG[173]		821.5	545.35
122	SEG[172]		790.5	545.35
123	SEG[171]		759.5	545.35
124	SEG[170]		728.5	545.35
125	SEG[169]		697.5	545.35
126	SEG[168]		666.5	545.35
127	SEG[167]		635.5	545.35
128	SEG[166]		604.5	545.35
129	SEG[165]		573.5	545.35
130	SEG[164]		542.5	545.35
131	SEG[163]		511.5	545.35
132	SEG[162]		480.5	545.35
133	SEG[161]		449.5	545.35
134	SEG[160]		418.5	545.35
135	SEG[159]		387.5	545.35
136	SEG[158]		356.5	545.35

PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
137	SEG[157]		325.5	545.35
138	SEG[156]		294.5	545.35
139	SEG[155]		263.5	545.35
140	SEG[154]		232.5	545.35
141	SEG[153]		201.5	545.35
142	SEG[152]		170.5	545.35
143	SEG[151]		139.5	545.35
144	SEG[150]		108.5	545.35
145	SEG[149]		77.5	545.35
146	SEG[148]		46.5	545.35
147	SEG[147]		15.5	545.35
148	SEG[146]		-15.5	545.35
149	SEG[145]		-46.5	545.35
150	SEG[144]		-77.5	545.35
151	SEG[143]		-108.5	545.35
152	SEG[142]		-139.5	545.35
153	SEG[141]		-170.5	545.35
154	SEG[140]		-201.5	545.35
155	SEG[139]		-232.5	545.35
156	SEG[138]		-263.5	545.35
157	SEG[137]		-294.5	545.35
158	SEG[136]		-325.5	545.35
159	SEG[135]		-356.5	545.35
160	SEG[134]		-387.5	545.35
161	SEG[133]		-418.5	545.35
162	SEG[132]		-449.5	545.35
163	SEG[131]		-480.5	545.35
164	SEG[130]		-511.5	545.35
165	SEG[129]		-542.5	545.35
166	SEG[128]		-573.5	545.35
167	SEG[127]		-604.5	545.35
168	SEG[126]		-635.5	545.35
169	SEG[125]		-666.5	545.35
170	SEG[124]		-697.5	545.35
171	SEG[123]		-728.5	545.35

PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
172	SEG[122]		-759.5	545.35
173	SEG[121]		-790.5	545.35
174	SEG[120]		-821.5	545.35
175	SEG[119]		-852.5	545.35
176	SEG[118]		-883.5	545.35
177	SEG[117]		-914.5	545.35
178	SEG[116]		-945.5	545.35
179	SEG[115]		-976.5	545.35
180	SEG[114]		-1007.5	545.35
181	SEG[113]		-1038.5	545.35
182	SEG[112]		-1069.5	545.35
183	SEG[111]		-1100.5	545.35
184	SEG[110]		-1131.5	545.35
185	SEG[109]		-1162.5	545.35
186	SEG[108]		-1193.5	545.35
187	SEG[107]		-1224.5	545.35
188	SEG[106]		-1255.5	545.35
189	SEG[105]		-1286.5	545.35
190	SEG[104]		-1317.5	545.35
191	SEG[103]		-1348.5	545.35
192	SEG[102]		-1379.5	545.35
193	SEG[101]		-1410.5	545.35
194	SEG[100]		-1441.5	545.35
195	SEG[99]		-1472.5	545.35
196	SEG[98]		-1503.5	545.35
197	SEG[97]		-1534.5	545.35
198	SEG[96]		-1565.5	545.35
199	SEG[95]		-1596.5	545.35
200	SEG[94]		-1627.5	545.35
201	SEG[93]		-1658.5	545.35
202	SEG[92]		-1689.5	545.35
203	SEG[91]		-1720.5	545.35
204	SEG[90]		-1751.5	545.35
205	SEG[89]		-1782.5	545.35
206	SEG[88]		-1813.5	545.35

PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
207	SEG[87]		-1844.5	545.35
208	SEG[86]		-1875.5	545.35
209	SEG[85]		-1906.5	545.35
210	SEG[84]		-1937.5	545.35
211	SEG[83]		-1968.5	545.35
212	SEG[82]		-1999.5	545.35
213	SEG[81]		-2030.5	545.35
214	SEG[80]		-2061.5	545.35
215	SEG[79]		-2092.5	545.35
216	SEG[78]		-2123.5	545.35
217	SEG[77]		-2154.5	545.35
218	SEG[76]		-2185.5	545.35
219	SEG[75]		-2216.5	545.35
220	SEG[74]		-2247.5	545.35
221	SEG[73]		-2278.5	545.35
222	SEG[72]		-2309.5	545.35
223	SEG[71]		-2340.5	545.35
224	SEG[70]		-2371.5	545.35
225	SEG[69]		-2402.5	545.35
226	SEG[68]		-2433.5	545.35
227	SEG[67]		-2464.5	545.35
228	SEG[66]		-2495.5	545.35
229	SEG[65]		-2526.5	545.35
230	SEG[64]		-2557.5	545.35
231	SEG[63]		-2588.5	545.35
232	SEG[62]		-2619.5	545.35
233	SEG[61]		-2650.5	545.35
234	SEG[60]		-2681.5	545.35
235	SEG[59]		-2712.5	545.35
236	SEG[58]		-2743.5	545.35
237	SEG[57]		-2774.5	545.35
238	SEG[56]		-2805.5	545.35
239	SEG[55]		-2836.5	545.35
240	SEG[54]		-2867.5	545.35
241	SEG[53]		-2898.5	545.35

PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
242	SEG[52]		-2929.5	545.35
243	SEG[51]		-2960.5	545.35
244	SEG[50]		-2991.5	545.35
245	SEG[49]		-3022.5	545.35
246	SEG[48]		-3053.5	545.35
247	SEG[47]		-3084.5	545.35
248	SEG[46]		-3115.5	545.35
249	SEG[45]		-3146.5	545.35
250	SEG[44]		-3177.5	545.35
251	SEG[43]		-3208.5	545.35
252	SEG[42]		-3239.5	545.35
253	SEG[41]		-3270.5	545.35
254	SEG[40]		-3301.5	545.35
255	SEG[39]		-3332.5	545.35
256	SEG[38]		-3363.5	545.35
257	SEG[37]		-3394.5	545.35
258	SEG[36]		-3425.5	545.35
259	SEG[35]		-3456.5	545.35
260	SEG[34]		-3487.5	545.35
261	SEG[33]		-3518.5	545.35
262	SEG[32]		-3549.5	545.35
263	SEG[31]		-3580.5	545.35
264	SEG[30]		-3611.5	545.35
265	SEG[29]		-3642.5	545.35
266	SEG[28]		-3673.5	545.35
267	SEG[27]		-3704.5	545.35
268	SEG[26]		-3735.5	545.35
269	SEG[25]		-3766.5	545.35
270	SEG[24]		-3797.5	545.35
271	SEG[23]		-3828.5	545.35
272	SEG[22]		-3859.5	545.35
273	SEG[21]		-3890.5	545.35
274	SEG[20]		-3921.5	545.35
275	SEG[19]		-3952.5	545.35
276	SEG[18]		-3983.5	545.35

PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
277	SEG[17]		-4014.5	545.35
278	SEG[16]		-4045.5	545.35
279	SEG[15]		-4076.5	545.35
280	SEG[14]		-4107.5	545.35
281	SEG[13]		-4138.5	545.35
282	SEG[12]		-4169.5	545.35
283	SEG[11]		-4200.5	545.35
284	SEG[10]		-4231.5	545.35
285	SEG[9]		-4262.5	545.35
286	SEG[8]		-4293.5	545.35
287	SEG[7]		-4324.5	545.35
288	SEG[6]		-4355.5	545.35
289	SEG[5]		-4386.5	545.35
290	SEG[4]		-4417.5	545.35
291	SEG[3]		-4448.5	545.35
292	SEG[2]		-4479.5	545.35
293	SEG[1]		-4510.5	545.35
294	SEG[0]		-4541.5	545.35
295	COM[34]	COM[67]	-4727.7	469.65
296	COM[35]	COM[65]	-4727.7	438.65
297	COM[36]	COM[63]	-4727.7	407.65
298	COM[37]	COM[61]	-4727.7	376.65
299	COM[38]	COM[59]	-4727.7	345.65
300	COM[39]	COM[57]	-4727.7	314.65
301	COM[40]	COM[55]	-4727.7	283.65
302	COM[41]	COM[53]	-4727.7	252.65
303	COM[42]	COM[51]	-4727.7	221.65
304	COM[43]	COM[49]	-4727.7	190.65
305	COM[44]	COM[47]	-4727.7	159.65
306	COM[45]	COM[45]	-4727.7	128.65
307	COM[46]	COM[43]	-4727.7	97.65
308	COM[47]	COM[41]	-4727.7	66.65
309	COM[48]	COM[39]	-4727.7	35.65
310	COM[49]	COM[37]	-4727.7	4.65
311	COM[50]	COM[35]	-4727.7	-26.35

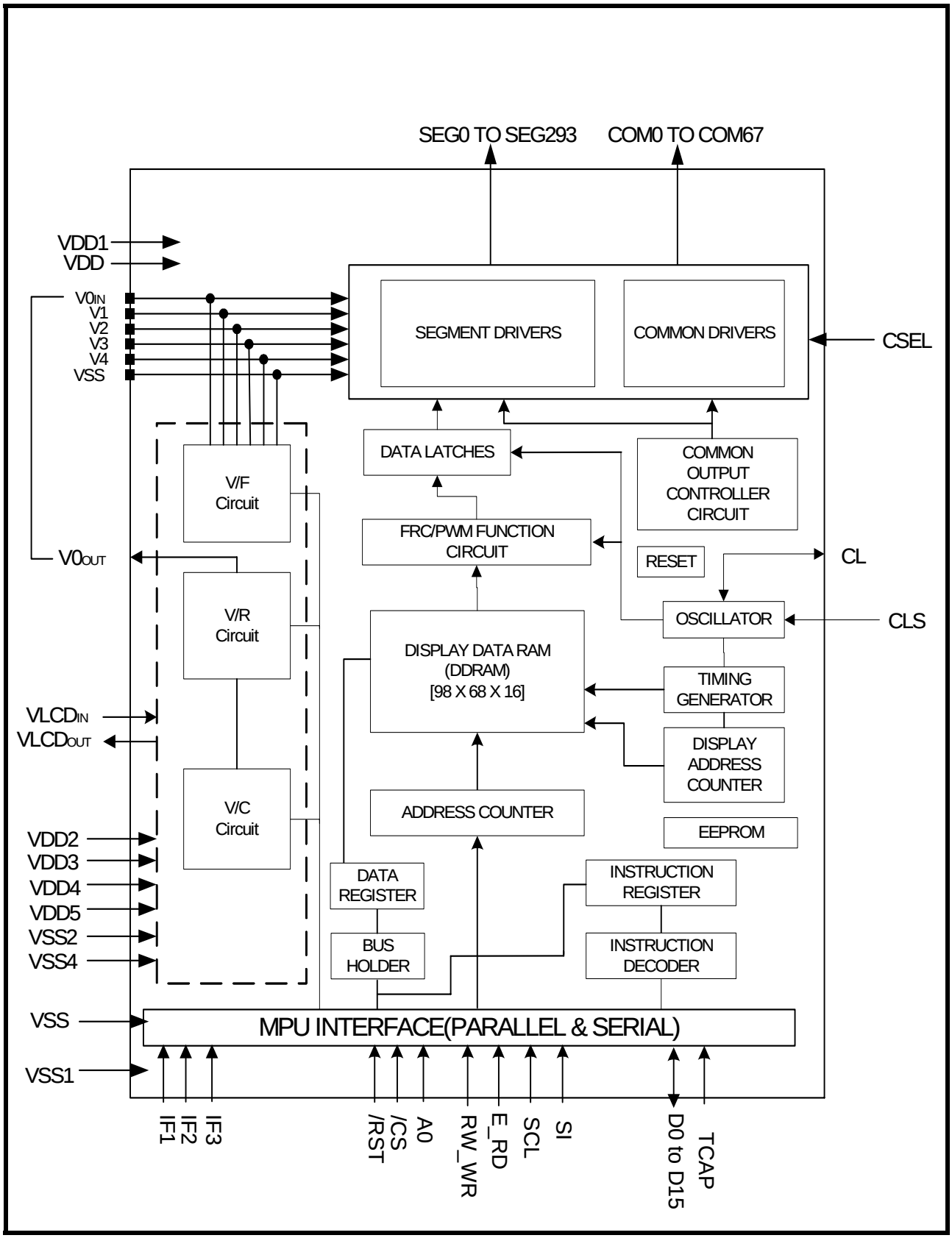
PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
312	COM[51]	COM[33]	-4727.7	-57.35
313	COM[52]	COM[31]	-4727.7	-88.35
314	COM[53]	COM[29]	-4727.7	-119.35
315	COM[54]	COM[27]	-4727.7	-150.35
316	COM[55]	COM[25]	-4727.7	-181.35
317	COM[56]	COM[23]	-4727.7	-212.35
318	COM[57]	COM[21]	-4727.7	-243.35
319	COM[58]	COM[19]	-4727.7	-274.35
320	COM[59]	COM[17]	-4727.7	-305.35
321	COM[60]	COM[15]	-4727.7	-336.35
322	COM[61]	COM[13]	-4727.7	-367.35
323	COM[62]	COM[11]	-4727.7	-398.35
324	COM[63]	COM[9]	-4727.7	-429.35
325	COM[64]	COM[7]	-4727.7	-460.35
326	COM[65]	COM[5]	-4727.7	-491.35
327	COM[66]	COM[3]	-4727.7	-522.35
328	COM[67]	COM[1]	-4727.7	-553.35
329	V0IN		-4510.0	-575.35
330	V0IN		-4400.0	-575.35
331	V0IN		-4290.0	-575.35
332	V0IN		-4180.0	-575.35
333	V0IN		-4070.0	-575.35
334	V0IN		-3960.0	-575.35
335	V0OUT		-3850.0	-575.35
336	V0OUT		-3740.0	-575.35
337	V1		-3630.0	-575.35
338	V2		-3520.0	-575.35
339	V3		-3410.0	-575.35
340	V4		-3300.0	-575.35
341	VREF		-3190.0	-575.35
342	CL		-3075.3	-575.35
343	CLS		-2965.3	-575.35
344	VSS		-2855.3	-575.35
345	VDD		-2745.3	-575.35
346	A0		-2635.3	-575.35

PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
347	RW_WR		-2525.3	-575.35
348	D0		-2415.3	-575.35
349	D1		-2305.3	-575.35
350	D2		-2195.3	-575.35
351	D3		-2085.3	-575.35
352	D4		-1975.3	-575.35
353	D5		-1865.3	-575.35
354	D6		-1755.3	-575.35
355	D7		-1645.3	-575.35
356	D8		-1535.3	-575.35
357	D9		-1425.3	-575.35
358	D10		-1315.3	-575.35
359	D11		-1205.3	-575.35
360	D12		-1095.3	-575.35
361	D13		-985.3	-575.35
362	D14		-875.3	-575.35
363	D15		-765.3	-575.35
364	VSS		-655.3	-575.35
365	VDD		-545.3	-575.35
366	E_RD		-435.3	-575.35
367	RST		-325.3	-575.35
368	CSEL		-215.3	-575.35
369	IF1		-105.3	-575.35
370	IF2		4.7	-575.35
371	IF3		114.7	-575.35
372	VSS		224.7	-575.35
373	VDD		334.7	-575.35
374	SI		444.7	-575.35
375	SCL		554.7	-575.35
376	/CS		664.7	-575.35
377	VDD		774.7	-575.35
378	VDD		884.7	-575.35
379	VDD1		994.7	-575.35
380	VSS1		1104.7	-575.35
381	VSS		1214.7	-575.35

PAD No.	PIN Name CSEL=0	PIN Name CSEL=1	X	Y
382	VSS		1324.7	-575.35
383	VSS		1434.7	-575.35
384	VSS2		1544.7	-575.35
385	VSS2		1654.7	-575.35
386	VSS2		1764.7	-575.35
387	VSS2		1874.7	-575.35
388	VSS2		1984.7	-575.35
389	VSS2		2094.7	-575.35
390	VSS2		2204.7	-575.35
391	VSS2		2314.7	-575.35
392	VSS4		2424.7	-575.35
393	VDD4		2534.7	-575.35
394	VDD3		2644.7	-575.35
395	VDD2		2754.7	-575.35
396	VDD2		2864.7	-575.35
397	VDD2		2974.7	-575.35
398	VDD2		3084.7	-575.35
399	VDD2		3194.7	-575.35
400	VDD5		3304.7	-575.35
401	VDD5		3414.7	-575.35
402	VDD5		3524.7	-575.35
403	TCAP		3634.7	-575.35
404	VLCDIN		3744.7	-575.35
405	VLCDIN		3854.7	-575.35
406	VLCDIN		3964.7	-575.35
407	VLCDIN		4074.7	-575.35
408	VLCDIN		4184.7	-575.35
409	VLCDIN		4294.7	-575.35
410	VLCDOUT		4404.7	-575.35
411	VLCDOUT		4514.7	-575.35
412	COM[0]	COM[0]	4727.7	-553.35
413	COM[1]	COM[2]	4727.7	-522.35
414	COM[2]	COM[4]	4727.7	-491.35
415	COM[3]	COM[6]	4727.7	-460.35
416	COM[4]	COM[8]	4727.7	-429.35

PAD No.	PIN Name		X	Y
	CSEL=0	CSEL=1		
417	COM[5]	COM[10]	4727.7	-398.35
418	COM[6]	COM[12]	4727.7	-367.35
419	COM[7]	COM[14]	4727.7	-336.35
420	COM[8]	COM[16]	4727.7	-305.35
421	COM[9]	COM[18]	4727.7	-274.35
422	COM[10]	COM[20]	4727.7	-243.35
423	COM[11]	COM[22]	4727.7	-212.35
424	COM[12]	COM[24]	4727.7	-181.35
425	COM[13]	COM[26]	4727.7	-150.35
426	COM[14]	COM[28]	4727.7	-119.35
427	COM[15]	COM[30]	4727.7	-88.35
428	COM[16]	COM[32]	4727.7	-57.35
429	COM[17]	COM[34]	4727.7	-26.35
430	COM[18]	COM[36]	4727.7	4.65
431	COM[19]	COM[38]	4727.7	35.65
432	COM[20]	COM[40]	4727.7	66.65
433	COM[21]	COM[42]	4727.7	97.65
434	COM[22]	COM[44]	4727.7	128.65
435	COM[23]	COM[46]	4727.7	159.65
436	COM[24]	COM[48]	4727.7	190.65
437	COM[25]	COM[50]	4727.7	221.65
438	COM[26]	COM[52]	4727.7	252.65
439	COM[27]	COM[54]	4727.7	283.65
440	COM[28]	COM[56]	4727.7	314.65
441	COM[29]	COM[58]	4727.7	345.65
442	COM[30]	COM[60]	4727.7	376.65
443	COM[31]	COM[62]	4727.7	407.65
444	COM[32]	COM[64]	4727.7	438.65
445	COM[33]	COM[66]	4727.7	469.65

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 POWER SUPPLY

Name	I/O	Description
VDD	Supply	Power supply for logic circuit
VDD1	Supply	Power supply for OSC circuit
VDD2	Supply	Power supply for Booster Circuit
VDD3	Supply	Power supply for LCD.
VDD4	Supply	Power supply for LCD.
VDD5	Supply	Power supply for LCD.
VSS	Supply	Ground for logic circuit. Ground system should be connected together.
VSS1	Supply	Ground for OSC circuit. Ground system should be connected together.
VSS2	Supply	Ground for Booster Circuit. Ground system should be connected together.
VSS4	Supply	Ground for LCD. Ground system should be connected together.

6.2 LCD Power Supply Pins

<table>
<tr><td>$VLCD_{OUT}$</td><td>O</td><td>If the internal voltage generator is used, the $VLCD_{IN}$ & $VLCD_{OUT}$ must be connected together.
If an external supply is used, this pin must be left open.</td></tr>
<tr><td>$VLCD_{IN}$</td><td>I</td><td>An external LCD supply voltage can be supplied using the $VLCD_{IN}$ pin. In this case, $VLCD_{OUT}$ has to be left open, and the internal voltage generator has to be programmed to zero. (SET register VC=0)</td></tr>
<tr><td>$V0_{IN}$
$V0_{OUT}$
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages
V0in & V0out should be connected together.
Voltages should have the following relationship;
V0 (V0in) ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ VSS.
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table>
<tr><th>LCD bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/N bias</td><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
NOTE: N = 5 to 12</td></tr>
</table>

6.3 SYSTEM CONTROL

Name	I/O	Description
CLS	I	When using internal clock oscillator, connect CLS to VDD. When using external clock oscillator, connect CLS to VSS.
CL	I/O	When using internal clock oscillator, it's oscillator output. When using external clock oscillator, it's clock input.
CSEL	I	Select Common output direction. CSEL="L", COM0~COM33 is in one side, COM34~COM67 is in the opposite side. CSEL="H", COM2n(even number) is in the one side, COM2n+1 (odd number) is in the opposite side.
TCAP	I/O	Test pin. Left it opens.
VREF	O	Reference voltage output for monitor only. Left it opened. Do NOT connect this PAD.

6.4 MICROPROCESSOR INTERFACE

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RST</td><td>I</td><td>Reset input pin. When RESETB is “L”, initialization is executed.</td></tr>
<tr><td>IF[3:1]</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><th>IF1</th><th>IF2</th><th>IF3</th><th>MPU interface type</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>80 series 16-bit parallel</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>68 series 16-bit parallel</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>68 series 8-bit parallel</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>9-bit serial (3 line)</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>8-bit serial (4 line)</td></tr>
</table></td></tr>
<tr><td>/CS</td><td>I</td><td>Chip select input pins
Data / Instruction I/O is enabled only when /CS is "L". When chip select is non-active, D0 to D15 become high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
A0 = "H": D0 to D15 or SI are display data
A0 = "L": D0 to D15 or SI are control data
In 3-line interface not let it floating, connect it to ”H” level.</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>RW</td><td>Read / Write control input pin
RW = “H” : read
RW = “L” : write</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D15 are latched at the rising edge of the /WR signal.</td></tr>
</table>
When in the serial interface, connect it to ”H” level.</td></tr>
<tr><td>E_RD</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Read / Write control input pin
RW = “H”: When E is “H”, D0 to D15 are in an output status.
RW = “L”: The data on D0 to D15 are latched at the falling edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, D0 to D15 are in an output status.</td></tr>
</table>
When in the serial interface, connect it to ”H” level .Signals Explaination Chart：see page 17</td></tr>
</table>

D15 to D0	I/O	They connect to the standard 8-bit or 16 bit MPU bus via the 8/16 –bit bi-directional bus. When the following interface is selected and the /CS pin is high, the following pins become high impedance. 1. In 8-bit parallel: D15-D8 pins are in the state of high impedance should connect to ”H” level. 2. In Serial interface: D15-D0 pins are in the state of high impedance should connect to ”H” level.
SI	I	This pin is used to input serial data when the serial interface is selected.(3 line and 4 line) When not use connect it to ”H” level.
SCL	I	This pin is used to input serial clock when the serial interface is selected. The data is converted in the rising edge. (3 line and 4 line) When not use connect it to ”H” level.

NOTE:

Microprocessor interfece pins should not be floating in any operation mode.

6.5 LCD DRIVER OUTPUTS

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG293</td><td>O</td><td>LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">M (Internal)</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Sleep-In mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM67</td><td>O</td><td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>M (Internal)</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Sleep-In mode</td><td>VSS</td></tr>
</table></td></tr>
</table>

ST7626 I/O PIN ITO Resister Limitation

Pin Name	ITO Resister
TCAP, CL	Floating
IF[3:1],CLS,CSEL	No Limitation
VDD, VDD1~VDD5, VSS,VSS1,VSS2,VSS4,$VLCD_{IN}$, $VLCD_{OUT}$	<100Ω
$V0_{IN}$, $V0_{OUT}$, V1, V2, V3, V4	<100Ω
A0, E_RD, RW_WR, /CS, D0 …D15, SCL, SI	<1KΩ
RST	<10KΩ

NOTE:

Make sure that the ITO resistance of COM0 ~ COM67 is equal, and so is it of SEG0 ~ SEG293.

Vref sould not connect to external. Therefore, no ITO resistance value listed.

7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

/CS pin is for chip selection. The ST7626 can function with an MPU when /CS is "L". In case of serial interface, the internal shift register and the counter are reset.

7.1.1 Selecting Parallel / Serial Interface

ST7626 has six types of interface with an MPU, which are two serial and four parallel interfaces. This parallel or serial interface is determined by IF pin as shown in table 7.1.1.

Table 7.1.1 Parallel / Serial Interface Mode

I/F Mode			I/F Description	Pin Assignment							
IF1	IF2	IF3		/CS	A0	E_RD	RW_WR	D15 to D8	D7 to D0	SI	SCL
H	H	H	80 serial 16-bit parallel	/CS	A0	/RD	/WR	D15 ~ D8	D7 ~ D0	--	--
H	H	L	80 serial 8-bit parallel	/CS	A0	/RD	/WR	--	D7 ~ D0	--	--
H	L	L	68 serial 16-bit parallel	/CS	A0	E	R/W	D15 ~ D8	D7 ~ D0	--	--
L	H	H	68 serial 8-bit parallel	/CS	A0	E	R/W	--	D7 ~ D0	--	--
L	L	L	8-bit SPI mode (4 line)	/CS	A0	--	--	--	--	SI	SCL
L	L	H	9-bit SPI mode (3 line)	/CS	--	--	--	--	--	SI	SCL

NOTE: When these pins are set to any other combination, A0, E_RD and RW_WR inputs are disabled and D0 to D15 are to be high impedance.

7.1.2 8-bit or 16-bit Parallel Interface

The ST7626 identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (W/R) signals, as shown in table 7.1.2.

Table 7.1.2 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	R/W	E	/RD	/WR	
H	H	H	L	H	Display data read out
H	L	H	H	L	Display data write
L	H	H	L	H	Register status read
L	L	H	H	L	Writes to internal register (instruction)

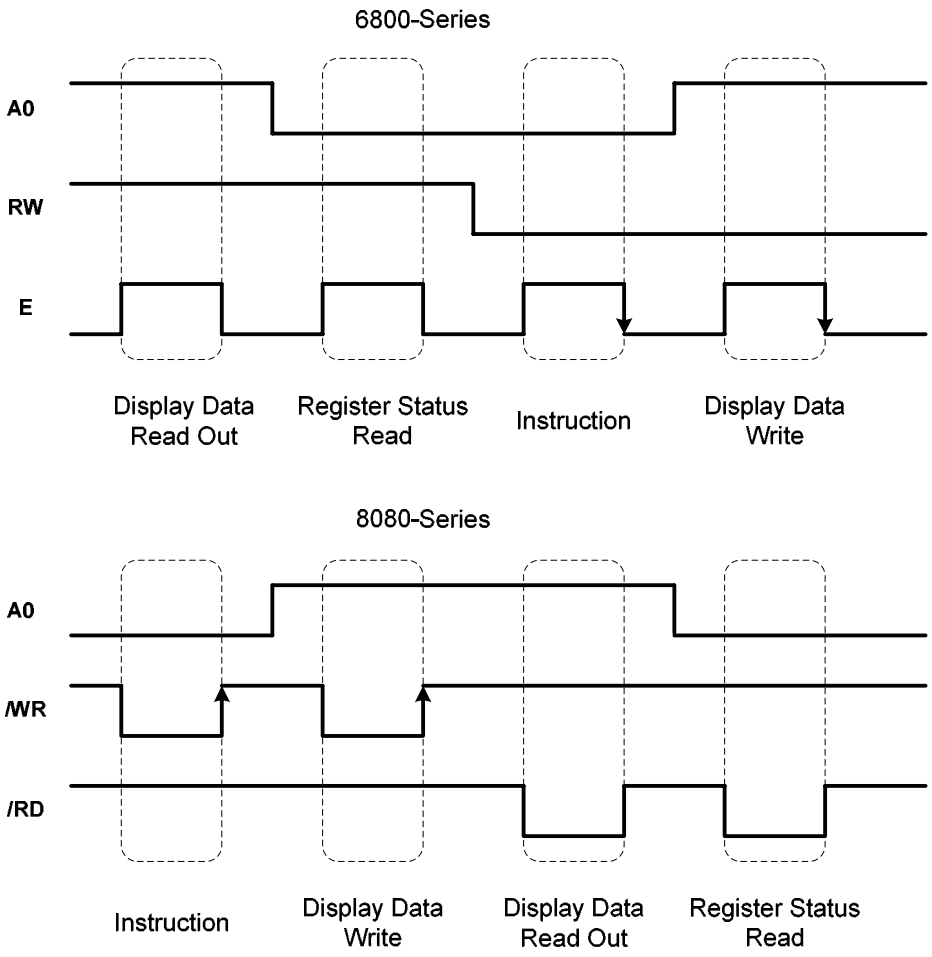


Figure 7.1.2 Parallel Data Transfer Example Chart

Relation between Data Bus and Gradation Data

ST7626 offers 4096 color display, 65K color display, truncated 262K color display, and truncated 16M color display. When using 4096, 65K, 262K, and 16M color display; you can specify color for each of R, G, B using the palette function. Use the command for switching between these modes.

(1) 4096-color display

(1-1) Type A 4096 color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRGGGG 1st write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBRRRR 2nd write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB 3rd write

2 pixels of data are read after the third write operation as shown, and it is written in the display RAM.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRGGGGBBBBXXXX

Data is acquired through signal write operation and then written to the display RAM.

"XXXX" are dummy bits, and they are ignored for display.

(1-2) Type B 4096 color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRR 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRRGGGGBBBB

A single pixel of data is read and written in the display RAM in a single write operation.

"XXXX" are dummy bits, and they are ignored for display.

(2) 65K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGG 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGBBBBB 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGGGGGBBBBB (16 bits)

Data is acquired through signal write operation and then written to the display RAM.

(3) Truncated 262K color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXX 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGXX 2nd write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXX 3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

"X" is dummy bit, and it is ignored for display.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXXGGGGGGXX 1st write

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXXXXXXXXXXXX 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

(4) Truncated 16M color input mode

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRR 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGGG 2nd write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBB 3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRRGGGGGGGG 1st write

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBBXXXXXXXX 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

7.1.3 8- and 9-bit Serial Interface

The 8-bit serial interface uses four pins /CS, SI, SCL, and A0 to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins /CS, SI and SCL for the same purpose.

Data read is not available in the serial interface. Data entered must be 8 bits. Refer to the following chart for entering commands, parameters or gray-scale data.

The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4-line)

When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.

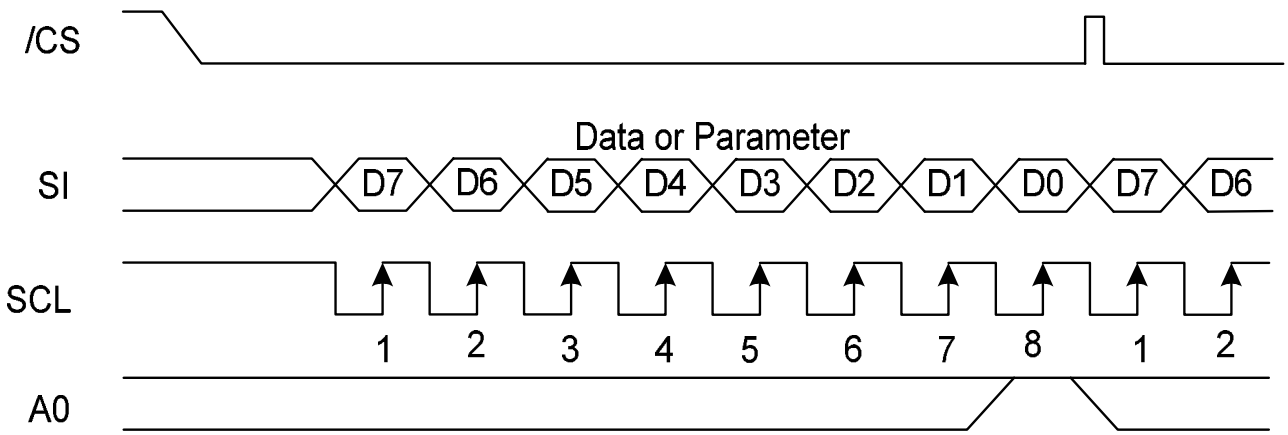


Figure 7.1.3 4-line explaination chart when entering data

When entering command: A0= LOW at the rising edge of the 8th SCL

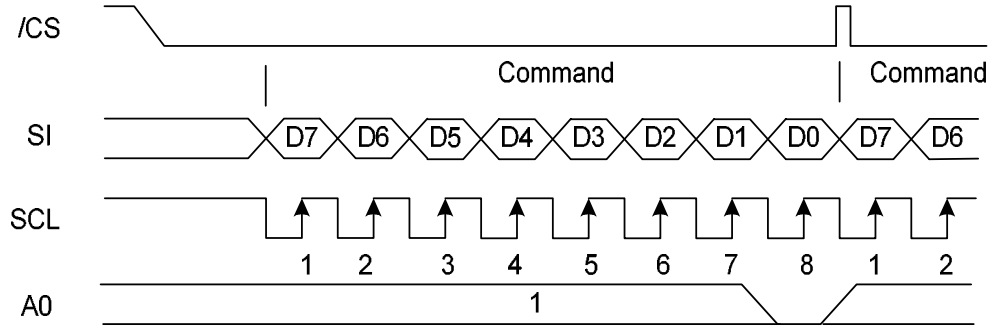


Figure 7.1.4 4-line explaination chart when entering command

(2) 9-bit serial interface (3-line)

When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.

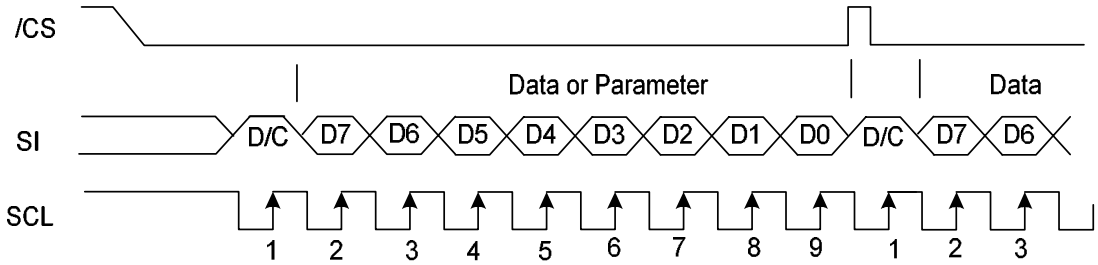


Figure 7.1.5 3-line explaination chart when entering data

When entering command: SI= LOW at the rising edge of the 1st SCL.

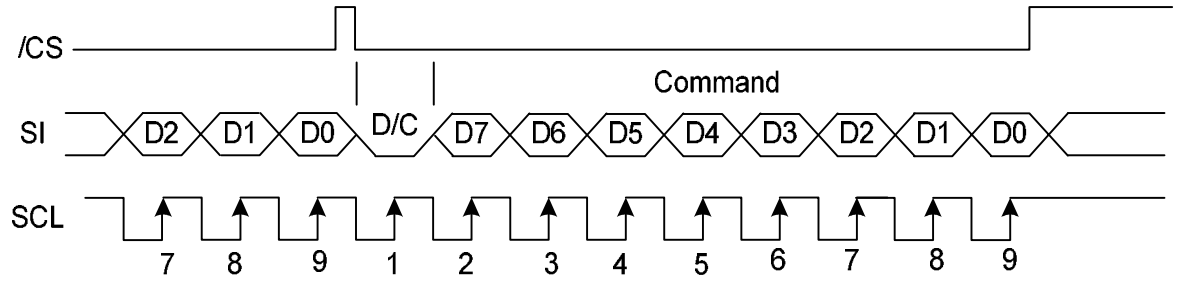


Figure 7.1.6 3-line explaination chart when entering command

- If /CS is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set /CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.
- When executing the command RAMWR, set /CS to HIGH after writing the last address (after starting the 9th pulse in case of 9-bit serial input or after starting the 8th pulse in case of 8-bit serial input).

7.2 ACCESS TO DDRAM AND INTERNAL REGISTERS

ST7626 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Figure 7.2.1 illustrates these relations.

In 80-series interface mode:

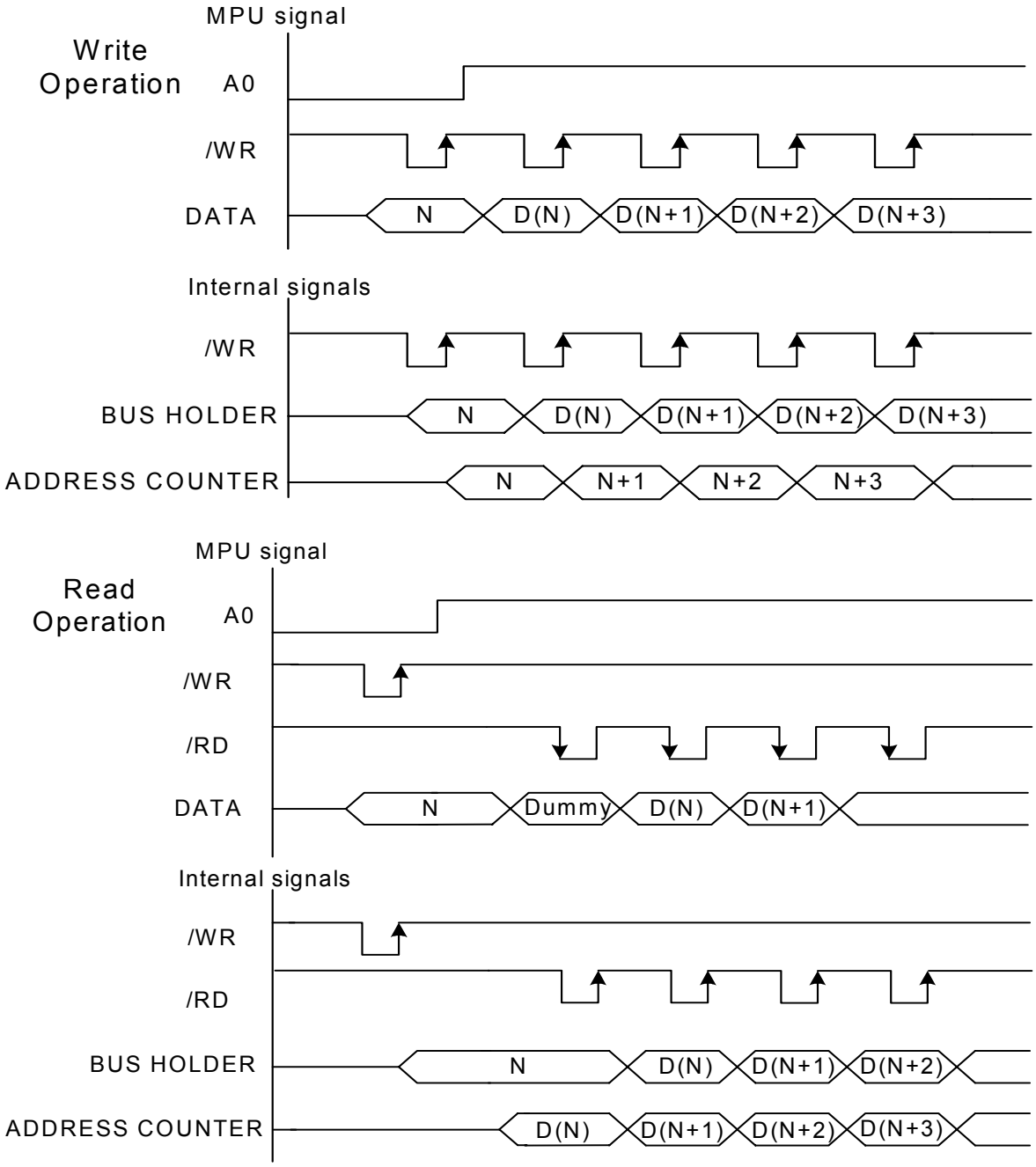


Figure 7.2.1 Access DDRAM chart

7.3 DISPLAY DATA RAM (DDRAM)

7.3.1 DDRAM

It is 98 X 68 X 16 bits capacity RAM prepared for storing dot data. You can access a desired bit by specifying the page address and column address. Since display data from MCU D7 to D0 and D15 to D8 correspond to one or two pixels of RGB, data transfer related restrictions are reduced, realizing the display flexing.

The RAM on ST7626 is separated to a block per 4 lines to allow the display system to process data on the block basis.

MPU's read and write operations to and from the RAM are performed via the I/O buffer circuit; Reading of the RAM for the liquid crystal drive is controlled from another separate circuit. Refer to the following memory map for the RAM configuration.

Memory Map (When using the Type A 4096 color. 8-bit mode)

RGB alignment (Command of data control parameter2=000)													
Data control command (BCH)				Column									
LCD read direction	P11:0(DATCTL)			0			1				97		
	P11:1(DATCTL)			97			96				0		
	Color			R	G	B	R	G	B		R	G	B
	Page \ Data			D0_7	D0_3	D1_7	D1_3	D2_7	D2_3		D146_3	D147_7	D147_3
				D0_6	D0_2	D1_6	D1_2	D2_6	D2_2		D146_2	D147_6	D147_2
Block	P10:0 (DATCTL)		P10:1 (DATCTL)	D0_5	D0_1	D1_5	D1_1	D2_5	D2_1		D146_1	D147_5	D147_1
				D0_4	D0_0	D1_4	D1_0	D2_4	D2_0		D146_0-	D147_4	D147_0
0	0		67										
	1		66										
	2		65										
	3		64										
1	4		63										
	5		62										
	6		61										
	7		60										
15	60		7										
	61		6										
	62		5										
	63		4										
16	64		3										
	65		2										
	66		1										
	67		0										
SEGout				0	1	2	3	4	5		291	292	293

Memory Map (When using the Type A 4096 color. 16-bit mode)

RGB alignment (Command of data control parameter2=000)													
Data control command (BCH)				Column									
LCD read direction	P11:0(DATCTL)			0			1				97		
				→									
	P11:1(DATCTL)			97			96				0		
				←									
	Color			R	G	B	R	G	B		R	G	B
	Page \ Data			D0_15	D0_11	D0_7	D1_15	D1_11	D1_7		D97_15	D97_11	D97_7
				D0_14	D0_10	D0_6	D1_14	D1_10	D1_6		D97_14	D97_10	D97_6
Block	P10:0 (DATCTL)		P10:1 (DATCTL)	D0_13	D0_9	D0_5	D1_13	D1_9	D1_5		D97_13	D97_9	D97_5
				D0_12	D0_8	D0_4	D1_12	D1_8	D1_4		D97_12	D97_8	D97_4
0	0	↓	67	↑									
	1		66										
	2		65										
	3		64										
1	4		63										
	5		62										
	6		61										
	7		60										
15	60		7										
	61		6										
	62		5										
	63		4										
16	64		3										
	65		2										
	66		1										
	67		0										
SEGout				0	1	2	3	4	5		291	292	293

Memory Map (When using the Type B 4096 color. 8-bit mode)

RGB alignment (Command of data control parameter2=000)														
Data control command (BCH)				Column										
LCD read direction	P11:0(DATCTL)			0			1				97			
				→										
	P11:1(DATCTL)			97			96				0			
				←										
	Color			R	G	B	R	G	B		R	G	B
	Page \ Data			D0_3	D1_7	D1_3	D2_3	D3_7	D3_3		D146_3	D147_7	D147_3
				D0_2	D1_6	D1_2	D2_2	D3_6	D3_2		D146_2	D147_6	D147_2
Block	P10:0 (DATCTL)		P10:1 (DATCTL)	D0_1	D1_5	D1_1	D2_1	D3_5	D3_1		D146_1	D147_5	D147_1
				D0_0	D1_4	D1_0	D2_0	D3_4	D3_0		D146_0	D147_4	D147_0
0	0	↓	67										
	1		66										
	2		65										
	3		64										
1	4		63										
	5		62										
	6		61										
	7		60										
15	60		7										
	61		6										
	62		5										
	63		4										
16	64		3										
	65		2										
	66		1										
	67		0										
SEGout				0	1	2	3	4	5		291	292	293

Note:

You can change position of R and B with DATACTL command.

Memory Map (When using the Type B 4096 color. 16-bit mode)

RGB alignment (Command of data control parameter2=000)													
Data control command (BCH)				Column									
LCD read direction	P11:0(DATCTL)			0			1				97		
				→									
	P11:1(DATCTL)			97			96				0		
				←									
	Color			R	G	B	R	G	B		R	G	B
	Page \ Data			D0_11	D0_7	D0_3	D1_11	D1_7	D1_3		D97_11	D97_7	D97_3
				D0_10	D0_6	D0_2	D1_10	D1_6	D1_2		D97_10	D97_6	D97_2
Block	P10:0 (DATCTL)		P10:1 (DATCTL)	D0_9	D0_5	D0_1	D1_9	D1_5	D1_1		D97_9	D97_5	D97_1
				D0_8	D0_4	D0_0	D1_8	D1_4	D1_0		D97_8	D97_4	D97_0
0	0	↓	67	↑									
	1		66										
	2		65										
	3		64										
1	4		63										
	5		62										
	6		61										
	7		60										
15	60		7										
	61		6										
	62		5										
	63		4										
16	64		3										
	65		2										
	66		1										
	67		0										
SEGout				0	1	2	3	4	5		291	292	293

Note:

You can change position of R and B with DATACTL command.

Memory Map (When using the 65Kcolor. 8-bit mode)

RGB alignment (Command of data control parameter2=000)														
Data control command (BCH)				Column										
LCD read direction	P11:0(DATCTL)			0			1				97			
				→										
	P11:1(DATCTL)			97			96				0			
				←										
	Color			R	G	B	R	G	B		R	G	B
	Page \ Data			D0_7	D0_2	D1_4	D2_7	D2_2	D3_4		D146_7	D146_2	D147_4
				D0_6	D0_1	D1_3	D2_6	D2_1	D3_3		D146_6	D146_1	D147_3
Block	P10:0 (DATCTL)	P10:1 (DATCTL)		D0_5	D0_0	D1_2	D2_5	D2_0	D3_2		D146_5	D146_0	D147_2
				D0_4	D1_7	D1_1	D2_4	D3_7	D3_1		D146_4	D147_7	D147_1
				D0_3	D1_6	D1_0	D2_3	D3_6	D3_0		D146_3	D147_6	D147_0
					D1_5			D3_5				D147_5	
0	0	67											
	1	66											
	2	65											
	3	64											
1	4	63											
	5	62											
	6	61											
	7	60											
15	60	7											
	61	6											
	62	5											
	63	4											
16	64	3											
	65	2											
	66	1											
	67	0											
SEGout				0	1	2	3	4	5		291	292	293

Note:

You can change position of R and B with DATACTL command.

Memory Map (When using the 65K color. 16-bit mode)

RGB alignment (Command of data control parameter2=000)													
Data control command (BCH)				Column									
LCD read direction	P11:0(DATCTL)			0			1				97		
				→									
	P11:1(DATCTL)			97			96				0		
				←									
	Color			R	G	B	R	G	B		R	G	B
	Page \ Data			D0_15	D0_10	D0_4	D1_15	D1_10	D1_4		D97_15	D97_10	D97_4
				D0_14	D0_9	D0_3	D1_14	D1_9	D1_3		D97_14	D97_9	D97_3
Block	P10:0 (DATCTL)		P10:1 (DATCTL)	D0_13	D0_8	D0_2	D1_13	D1_8	D1_2		D97_13	D97_8	D97_2
				D0_12	D0_7	D0_1	D1_12	D1_7	D1_1		D97_12	D97_7	D97_1
				D0_11	D0_6	D0_0	D1_11	D1_6	D1_0		D97_11	D97_6	D97_0
					D0_5			D1_5				D97_5	
0	0	↓	67	↑									
	1		66										
	2		65										
	3		64										
1	4		63										
	5		62										
	6		61										
	7		60										
15	60		7										
	61		6										
	62		5										
	63		4										
16	64		3										
	65		2										
	66		1										
	67		0										
SEGout				0	1	2	3	4	5		291	292	293

Note:

You can change position of R and B with DATACTL command.

Memory Map (When using the 262K/16Mcolor. 8-bit mode)

RGB alignment (Command of data control parameter2=000)														
Data control command (BCH)				Column										
LCD read direction	P11:0(DATCTL)			0			1				97			
	P11:1(DATCTL)			97			96				0			
	Color			R	G	B	R	G	B		R	G	B
	Page \ Data			D0_7	D1_7	D2_7	D3_7	D4_7	D5_7		D291_7	D292_7	D293_7
				D0_6	D1_6	D2_6	D3_6	D4_6	D5_6		D291_6	D292_6	D293_6
Block	P10:0 (DATCTL)		P10:1 (DATCTL)	D0_5	D1_5	D2_5	D3_5	D4_5	D5_5		D291_5	D292_5	D293_5
				D0_4	D1_4	D2_4	D3_4	D4_4	D5_4		D291_4	D292_4	D293_4
				D0_3	D1_3	D2_3	D3_3	D4_3	D5_3		D291_3	D292_3	D293_3
				D0_2	D1_2	D2_2	D3_2	D4_2	D5_2		D291_2	D292_2	D293_2
				D0_1	D1_1	D2_1	D3_1	D4_1	D5_1		D291_1	D292_1	D293_1
				D0_0	D1_0	D2_0	D3_0	D4_0	D5_0		D291_0	D292_0	D293_0
0	0		67										
	1		66										
	2		65										
	3		64										
1	4		63										
	5		62										
	6		61										
	7		60										
15	60		7										
	61		6										
	62		5										
	63		4										
16	64		3										
	65		2										
	66		1										
	67		0										
SEGout				0	1	2	3	4	5		291	292	293

Note:

You can change position of R and B with DATACTL command.

Memory Map (When using the 16 gray-scale, 262K/16M color. 16-bit mode)

RGB alignment (Command of data control parameter2=000)														
Data control command (BCH)				Column										
LCD read direction	P11:0(DATCTL)			0			1				97			
	P11:1(DATCTL)			97			96				0			
	Color			R	G	B	R	G	B		R	G	B	
	Page \ Data			D0_15	D0_7	D1_15	D1_7	D2_15	D2_7		D146_7	D147_15	D147_7	
				D0_14	D0_6	D1_14	D1_6	D2_14	D2_6		D146_6	D147_14	D147_6	
Block	P10:0 (DATCTL)		P10:1 (DATCTL)	D0_13	D0_5	D1_13	D1_5	D2_13	D2_5		D146_5	D147_13	D147_5	
				D0_12	D0_4	D1_12	D1_4	D2_12	D2_4		D146_4	D147_12	D147_4	
				D0_11	D0_3	D1_11	D1_3	D2_11	D2_3		D146_3	D147_11	D147_3	
				D0_10	D0_2	D1_10	D1_2	D2_10	D2_2		D146_2	D147_10	D147_2	
				D0_9	D0_1	D1_9	D1_1	D2_9	D2_1		D146_1	D147_9	D147_1	
				D0_8	D0_0	D1_8	D1_0	D2_8	D2_0		D146_0	D147_8	D147_0	
0	0		67											
	1		66											
	2		65											
	3		64											
1	4		63											
	5		62											
	6		61											
	7		60											
15	60		7											
	61		6											
	62		5											
	63		4											
16	64		3											
	65		2											
	66		1											
	67		0											
SEGout				0	1	2	3	4	5		291	292	293	

Note:

You can change position of R and B with DATACTL command.

7.3.2 Page Address Control Circuit

This circuit is used to control the address in the page direction when MPU accesses the DDRAM or when reading the DDRAM to display image on the LCD.

You can specify a scope of the page address with page address set command. When the page-direction scan is specified with DATACTL command and the address are incremented from the start up to the end page, the column address is incremented by 1 and the page address returns to start page.

The DDRAM supports up to 68 lines, and thus the total page becomes 68.

In the read operation, as the end page is reached, the column address is automatically incremented by 1 and the page address is returned to start page.

Using the address normal/inverse parameter of DATACTL command allows you to inverse the correspondence between the DDRAM address and command output.

7.3.3 Column Address Control Circuit

This circuit is used to control the address in the column direction when MPU accesses the DDRAM. You can specify a scope of the column address using column address set command. When the column-direction scan is specified with DATACTL command and the address are incremented from the start up to the end page, the page address is incremented by 1 and the column address returns to start column.

In the read operation, too, the column address is automatically incremented by 1 and returned to start page as the end column is reached.

Just like the page address control circuit, using the column address normal/inverse parameter of DATACTL command enables to inverse the correspondence between the DDRAM column address and segment output. This arrangement relaxes restrictions in the chip layout on the LCD module.

7.3.4 I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM when the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.5 Block Address Circuit

The circuit associates pages on DDRAM with COM output. ST7626 processes signals for the liquid crystal display on 4-page basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in block.

7.3.6 Display data Latch Circuit

This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.4 Area Scroll Display

Using area scroll set and scroll start set commands allows you to scroll the display screen partially. You can select any one of the following four scroll patterns.

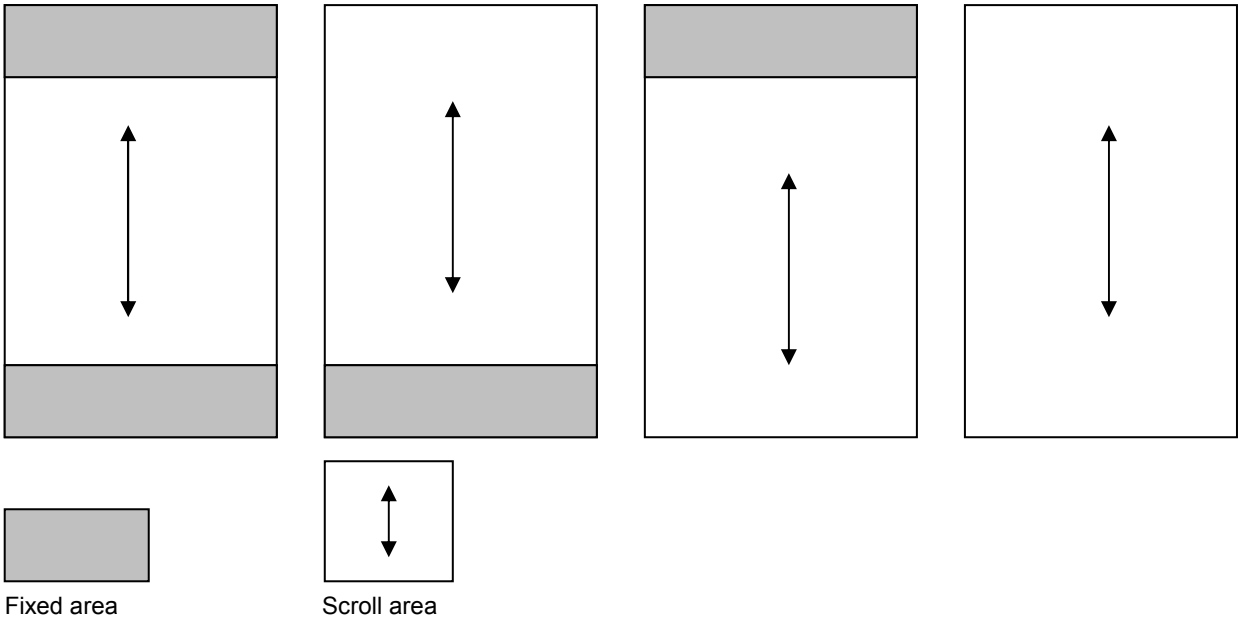


Figure 7.4.1 Scroll Mode explaination chart

Example：In the center screen scroll of 1/48 duty (display range: 48 lines = 12 blocks)

- Set Area Scroll command (0x00AA)
- Block 0 and block 1 (8-lines) are specified for the top fixed area.

  Top Block Address = Number of the top fixed area

  = 8 / 4 = 2 (0x0002) parameter (0x0002)
- Block 15 & block 16 (8-lines) are specified for the bottom fixed area.
- Block 10 to block 14 (20-lines) are specified for the background area.

  Bottom Block Address = Number of Background area + Bottom Block Address

  = (20 / 4) + 9 = 14 (0x000E) parameter (0x000E)
- Block 2 to Block 9 (32-lines) are specified for the scroll area

  Number of Specified Blocks = ((Top Fix Area + Scroll Area) – 1)

  = (2 + (12 - 2 - 2)) - 1 = 9 (0x000E) parameter (0x0009)
- Set area acroll mode – Center Screen Mode parameter (0x0000)

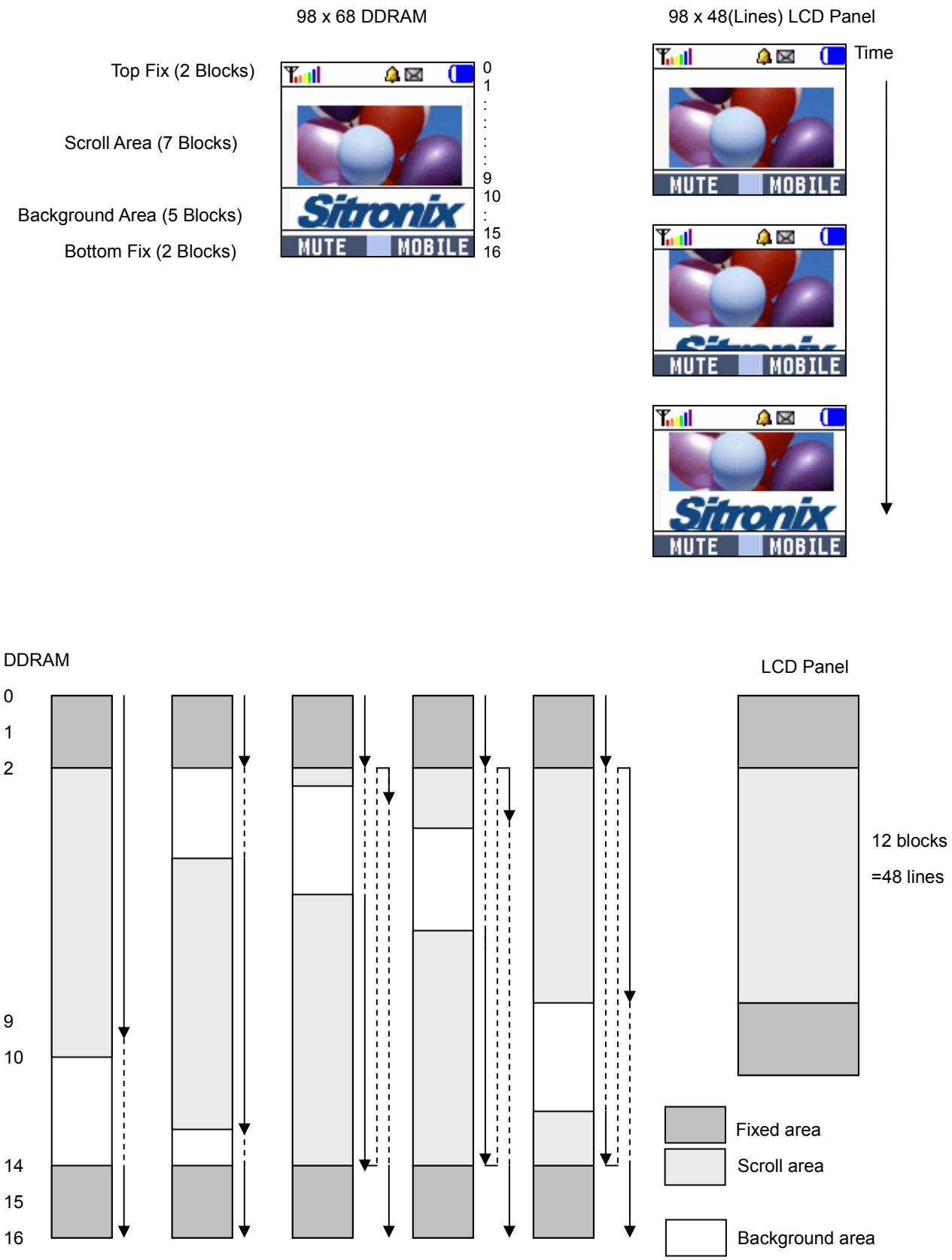


Figure 7.4.2 Reference Example for Scroll Display

7.5 Partial Display

Using partial in command allows you turn on the partial display (division by line) of the screen. This mode requires less current consumption than the whole screen display, making it suitable for the equipment in the standby state.

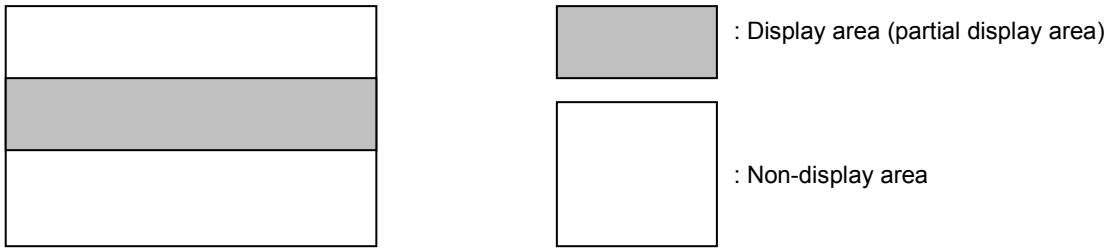


Figure 7.5.1 Partial Mode explaination chart

If the partial display region is out of the Max. Display range, it would be no operation

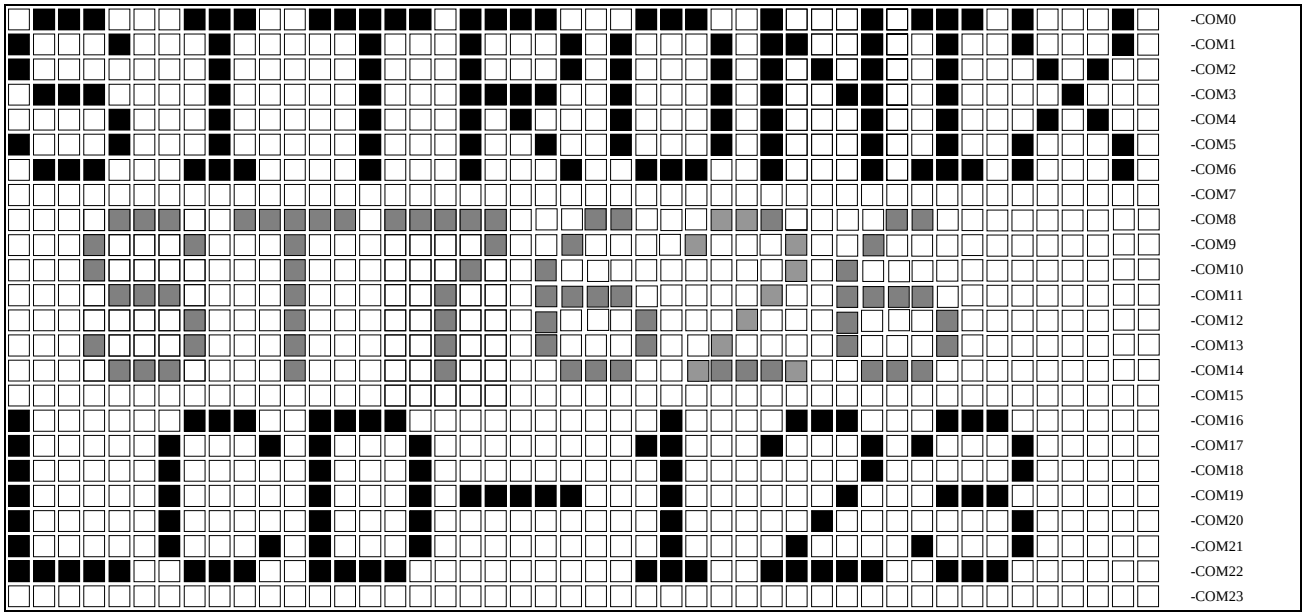


Figure 7.5.2 Reference Example for Partial Display

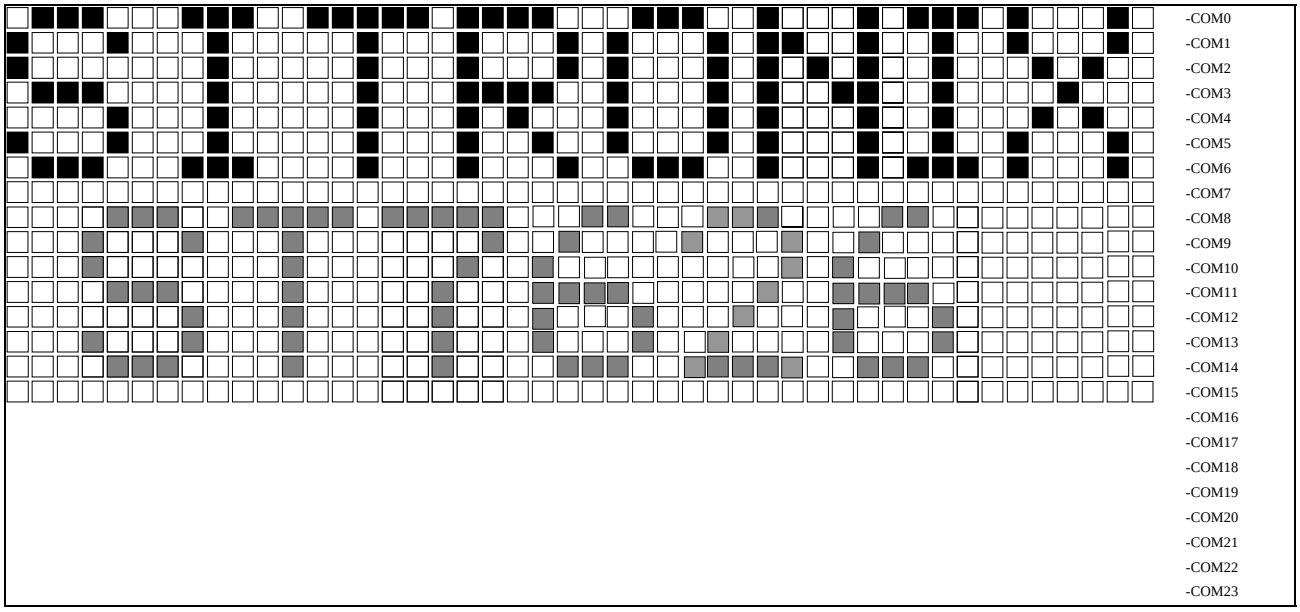


Figure 7.5.3 Partial Display (Partial Display Duty=16, initial COM0=0)

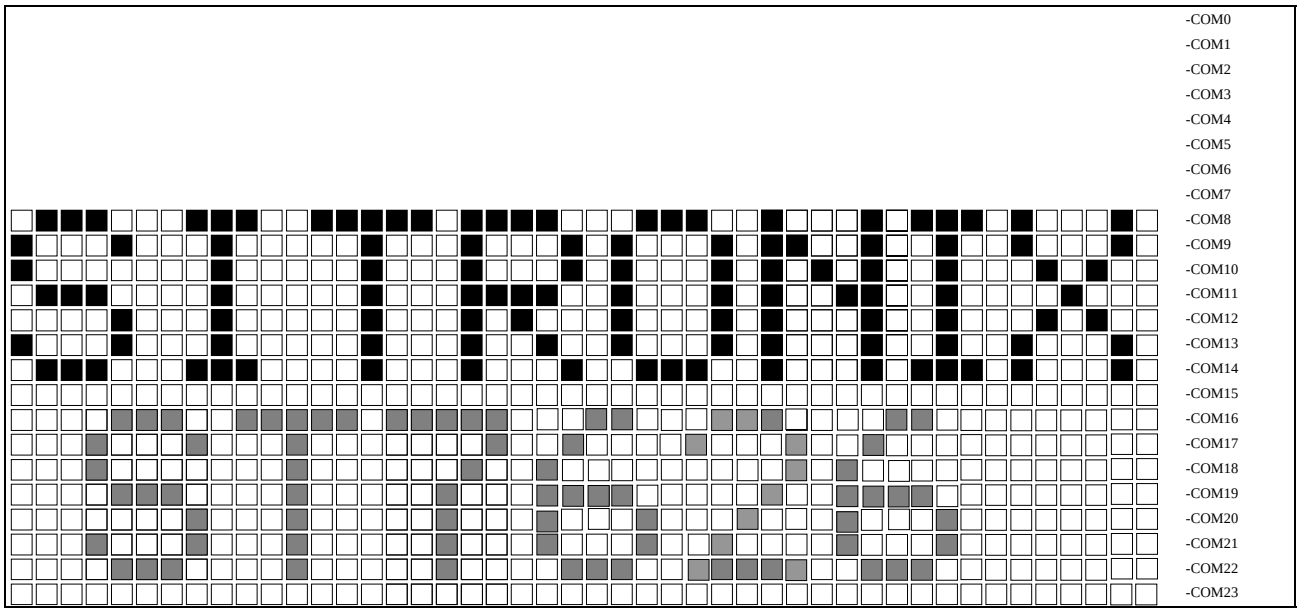


Figure 7.5.4 Moving Display (Partial Display Duty=16, initial COM0=8)

7.6 Gary-Scale Display

ST7626 incorporates a 4FRC & 31 PWM function circuit to display a 64 gray-scale display.

7.7 Oscillation circuit

This is on-chip Oscillator without external resistor. When the internal oscillator is used, CLS must connect to VDD; when the external oscillator is used, CL could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.8 Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 68-bits display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.8.1.

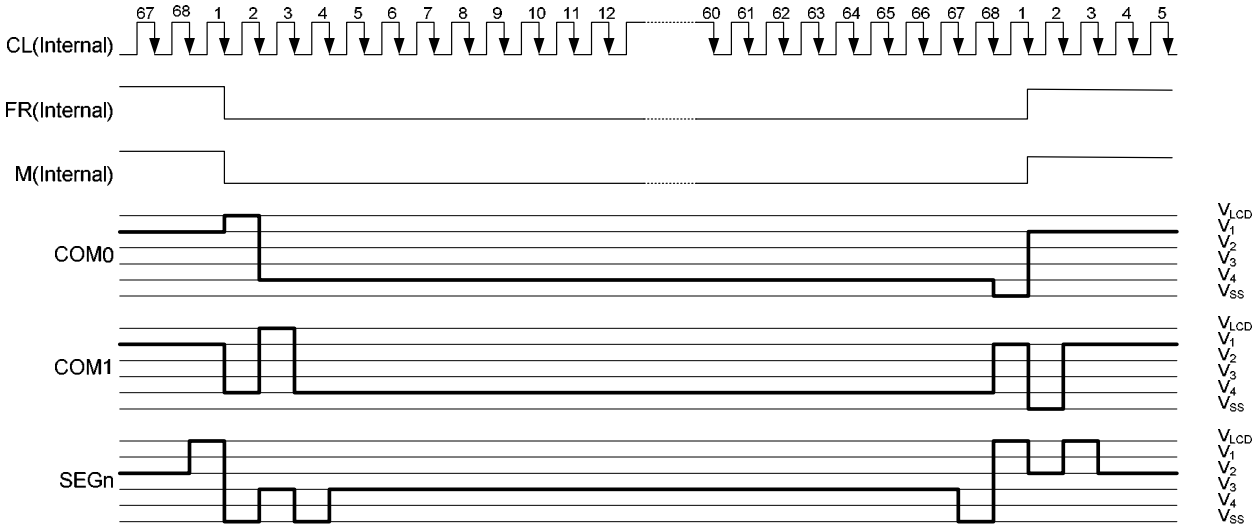


Figure 7.8.1 2-frame AC Driving Waveform (Duty Ratio: 1/68)

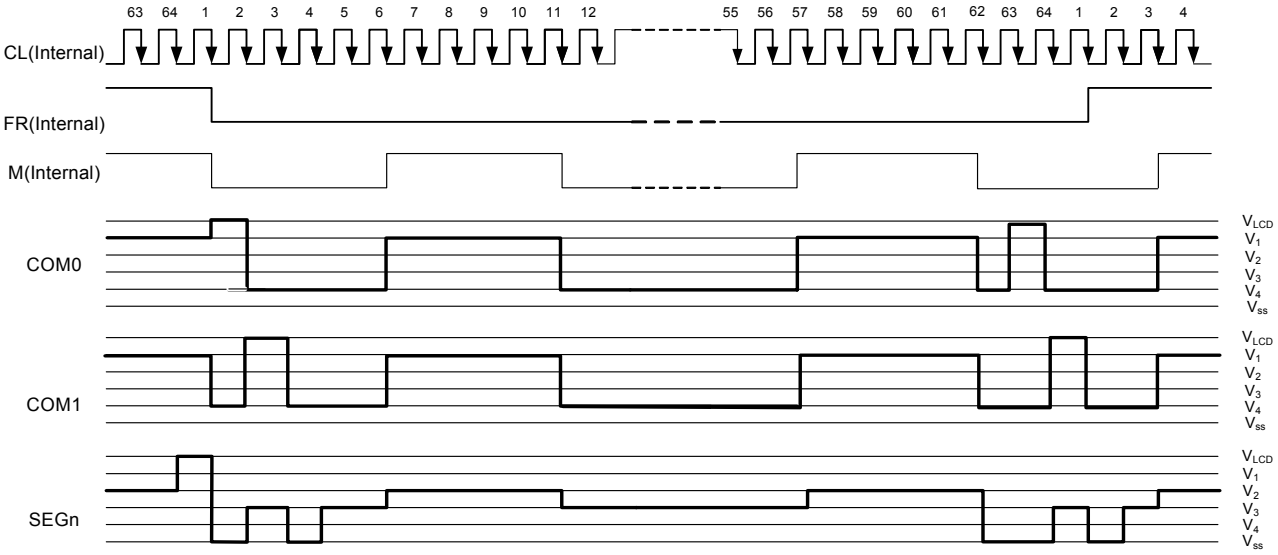


Figure 7.8.2 N-Line Inversion Driving Waveform (N=5, Duty Ratio=1/64)

7.9 Liquid Crystal drive Circuit

This driver circuit is configured by 68-channel common drivers and 294-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.

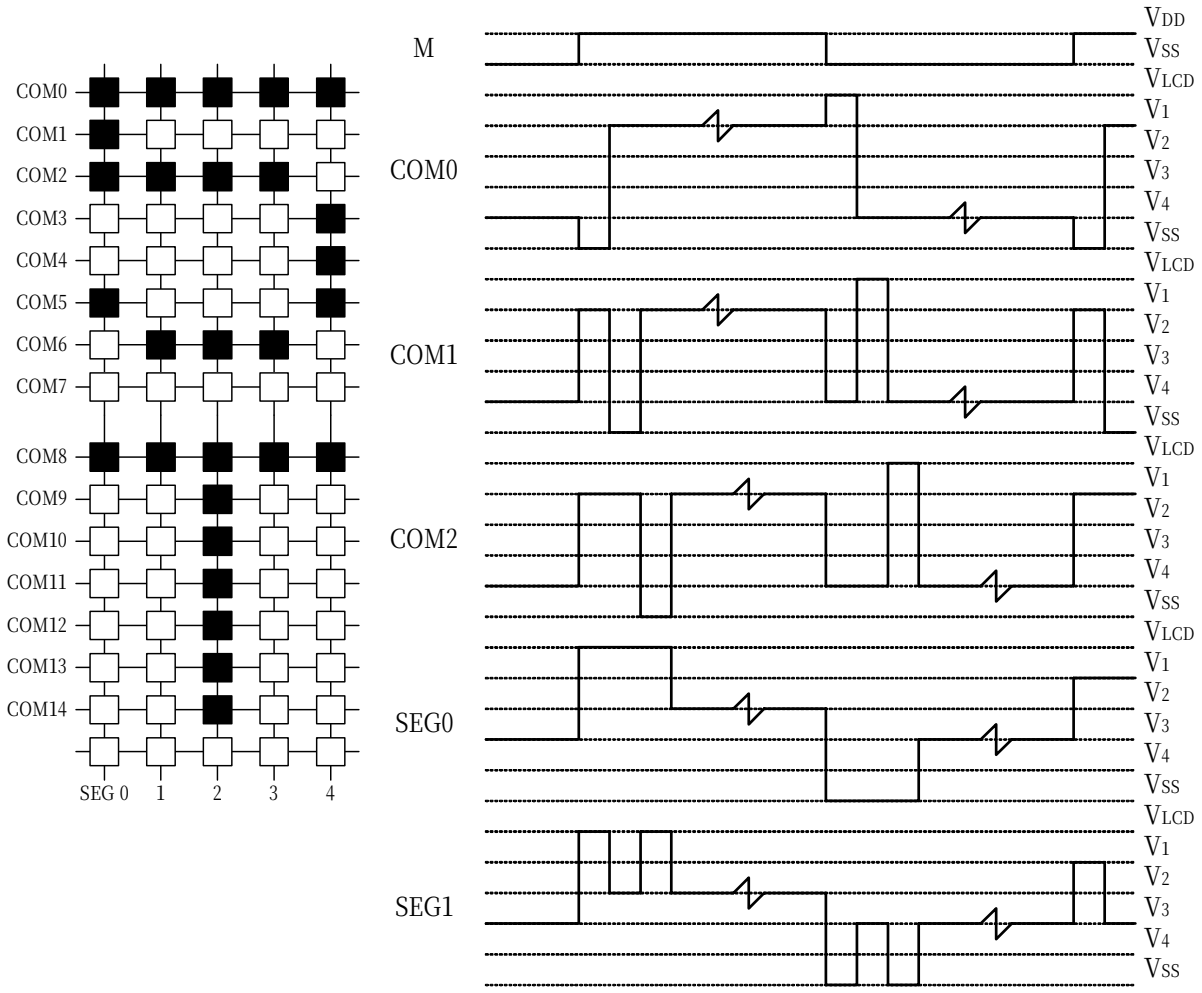


Figure 7.9.1 LCD Driving Waveform

7.10 Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 7.10.1 shows the referenced combinations in using Power Supply circuits.

Table 7.10.1 Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VLCD	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	a capacitor is series to GND	Open*1	Open*1
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open*1	Open*1
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open*1
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

*1 : ST7626 only needs one capacitor series VLCD to GND in normal situation. Add series-capacitors from V0~V4 to GND will improve display performance.

7.10.1 Voltage Converter Circuits

There is a built-in DC-DC voltage converter circuits in ST7626 for generating $VLCD_{OUT}$. Multiple of voltage converter is 2、3、4、5 times of Vdd2 toward positive side, and it can be controlled by software(Command ANASET). Please make sure that $VLCD_{OUT}$ must below 20V after turn on voltage converter circuit.

7.10.2 Voltage Regulator Circuits

There is a built-in voltage regulaor circuits in ST7626 for generating $V0_{OUT}$. After $VLCD_{OUT}$ is regulated by voltage regulator circuit, $V0_{OUT}$ is generated. Users also can use VOP function to program the optimum LCD supply voltage V0 by software (Command SETVOP). Detail explaination of VOP-set is listed below:

SETVOP

Reset state of Vop[8:0] is 160DEC = 10.00V.

The VOP value is programmed via the Vop[8:0] register.

V0=a+(Vop[8:6]Vop[5:0]). b

Ex:VOP[5:0]=100000, VOP[8:6]=010

→ Vop [8:0]=010100000

→ 3.6+210x0.04=10.00

- a is a fixed constant value (see table 7.10.2).
- b is a fixed constant value (see table 7.10.2).
- VOP[8:0] is the programmed VOP value. The programming range for VOP[8:0] is 5 to 410 (19Ahex).
- VOP[5:0] is the set-contrast value which can be set via the command SETVOP and EEPROM.(See command VOLUP & VOLDOWN)
- The suggested value of V0 is under 11 V with bias =1/9.

Table 7.10.2

SYMBOL	VALUE	UNIT
a	3.6	V
b	0.04	V

The VOP[8:0] value must be in the VOP programming range as given in Figure 7.10.2. Evaluating equation (1), values outside the programming range indicated in Figure 7.10.2 may result. Calculated values below 4 will be mapped to VOP[8:0] = 4, resulting VOP[8:0] values higher than 410 will be mapped to VOP[8:0] = 410. Sitronix suggestes Vop range equals 4.5V to 18V.

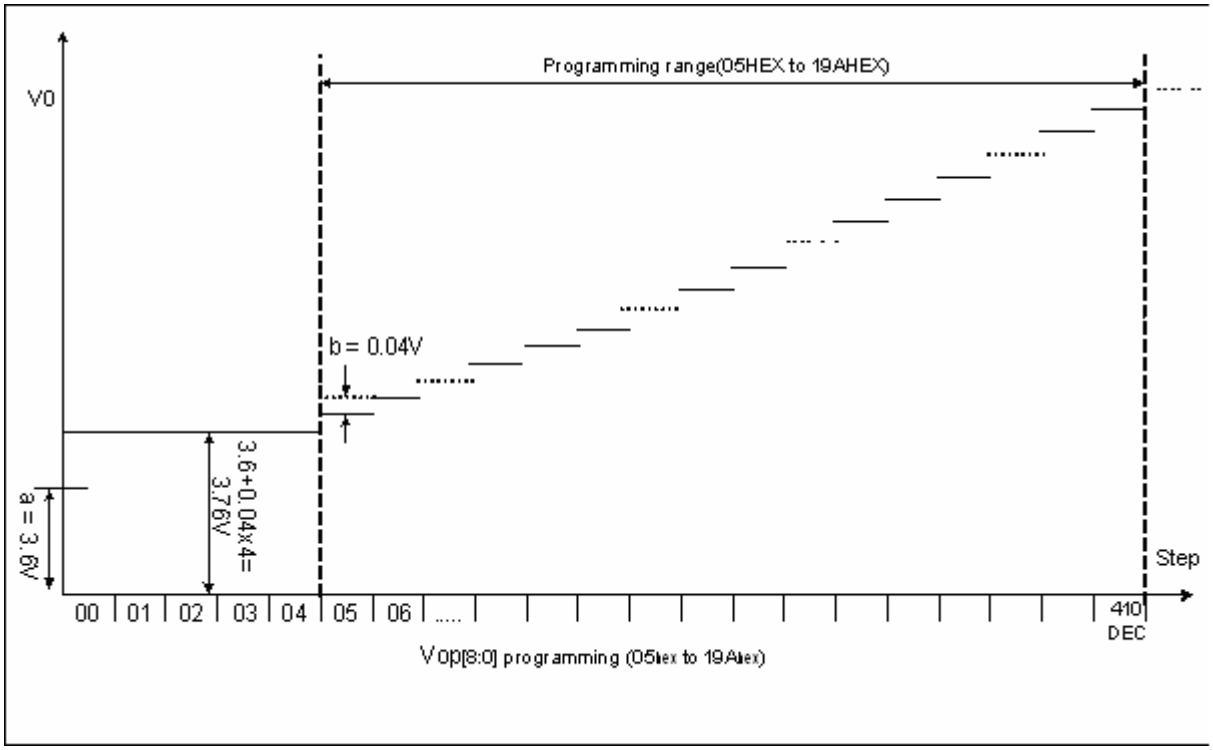


Figure 7.10.2 VOP programming range

As the programming range for the internally generated V0 voltage is above the limited V0 (18V), users has to ensure while setting the VOP register that under all conditions and including all tolerances that the V0 voltage remains below 18V.

Table 7.10.3

Par no.	Equipment Type	Thermal Gradient
ST7626	Internal Power Supply	-0.065%/^{0}C @ V0=10.52V, 25^{0}C

7.10.3 Voltage Follower Circuits

There is a built-in voltage follower circuits in ST7626 for generating V1、V2、V3 and V4. These voltages are decided by bias ratio selection circuitry which is set by users with software to control 1/5 to 1/12 bias ratios to match the optimum display performance of LCD panel. Bias driving rule is listed below:

Table 7.10.4

LCD bias	V1	V2	V3	V4
1/N bias	(N-1) / N x V0	(N-2) / N x V0	(2/N) x V0	(1/N) x V0

N=5 to 12

7.10.4 The Set-up Power Circuits

The ST7626 series has two modes of power circuit. One is 1 CAP with VLCDout, the other is 6 CAP with VLCDout/V0/V1/V2/V3/V4 (depend on panel loading). The detail circuit is as below.

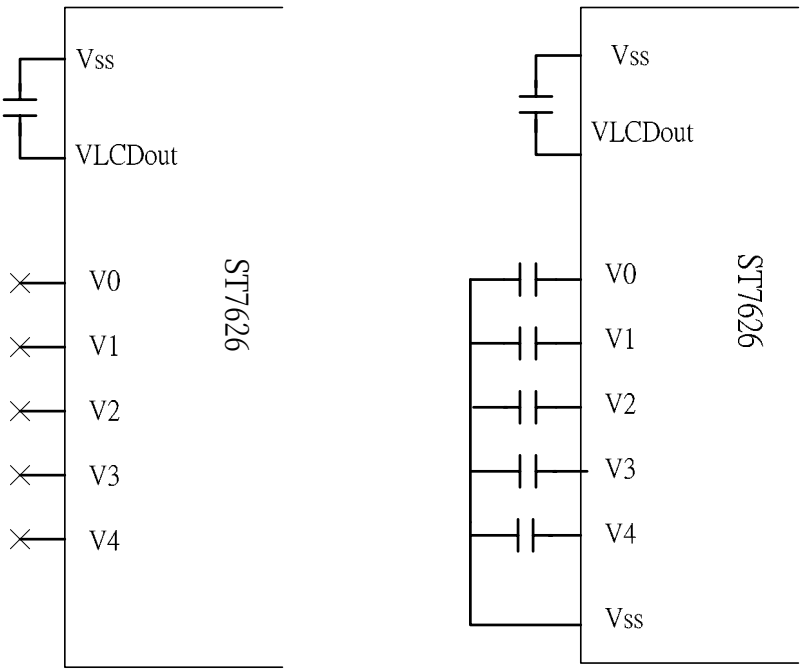


Figure 7.10.3 (a) 1 CAP power circuit (b) 6 CAP power circuit

Notes: 1. VLCDout: 1.0~2.2uF/25V

2. V0~V4:0.1~1.0uF/25V

7.10.5 EEPROM Setting Flow

♦ **EEPROM Setting Flow**

ST7626 provide the Write and Read function to write the Electronic Control value and Built-in resistance ratio into and read them from the built-in EEPROM. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage.

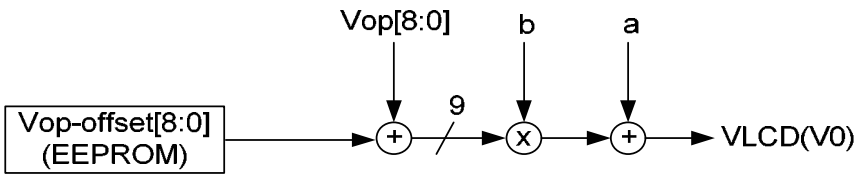


Figure 7.10.5 EC value control for different modules by loading EEPROM offset

Note1: This setting flow is used for LCM assembler.

Note2: EEPROM shouldn't be written without preceding loading correctly from EEPROM to avoid some errors during IC operation.

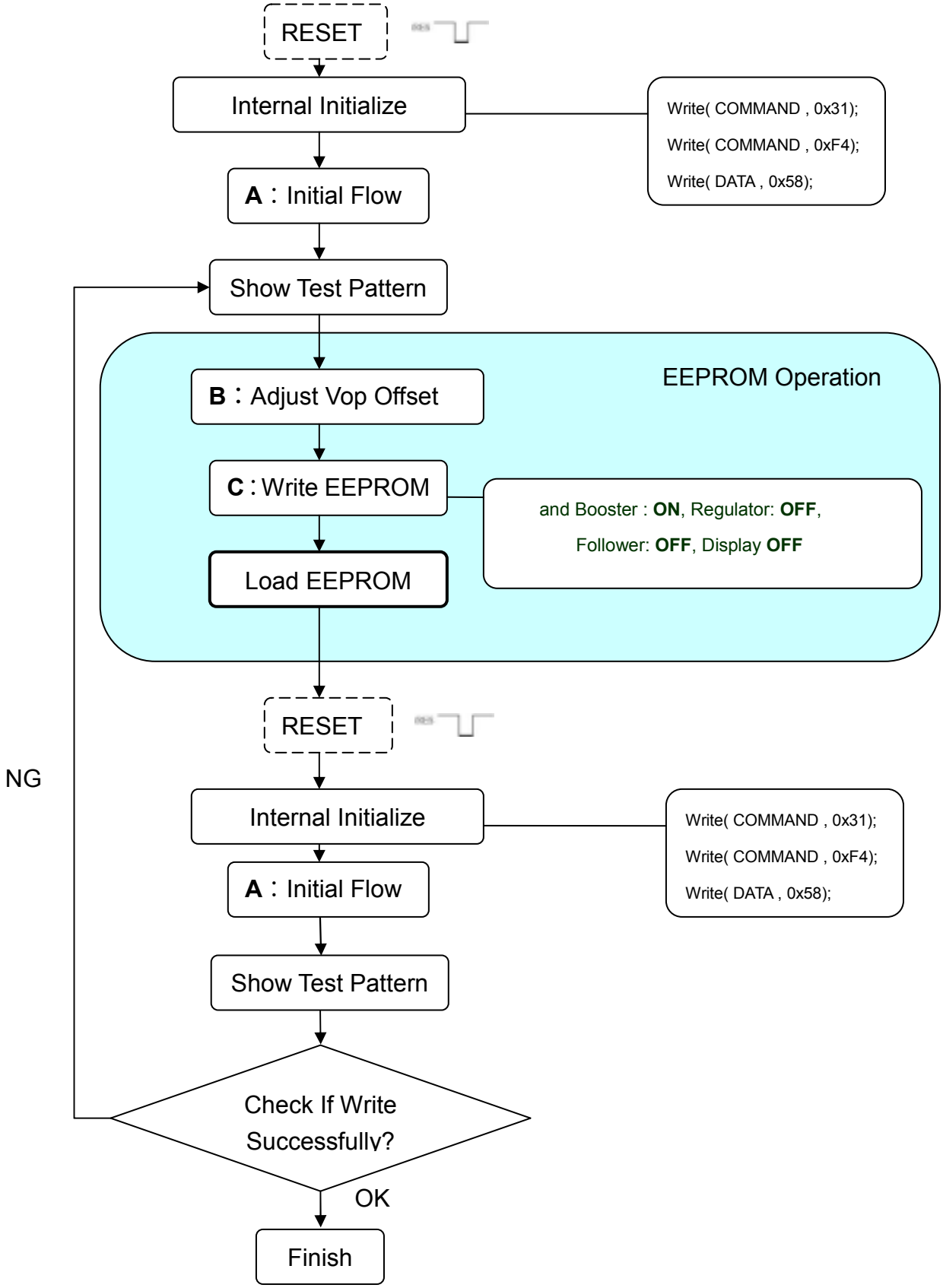
Note3: When writing value to EEPROM, the voltage of VLCDin must be more than 18V.

Note4: When writing value to EEPROM, the voltage of VDD2~VDD5 must be 2.8~3.3V.

Note5: When writing value to EEPROM, the Regulator and Follower must turn OFF, and Display also must turn OFF.

Note6: If the EEPROM is exposed to a high temperature for hours, data in the memory cell may probably be lost before the data retention guarantee period. To retain data in the memory cell, keep the mamory cell below 90℃. The data retention guarantee period is specified including the retention period.

♦ **EEPROM Flow Chart**



- **Software Program**

A. Initial Flow

```
void ST7626_Init( void )
{
```

Write(COMMAND, 0x30);	// Ext = 0
Write(COMMAND, 0x04);	// Sleep In/Out Preparation
Write(DATA, 0x3e);	// Sleep In/Out Sequencing
Write(COMMAND, 0x31);	// Ext = 1
Write(COMMAND, 0xf4);	// Internal Initialize Preparation
Write(DATA, 0x58);	// Internal Initialize Sequencing
Write(COMMAND, 0x30);	// Ext = 0
Write(COMMAND, 0x94);	// Sleep Out
Write(COMMAND, 0xd1);	// Internal OSC on
Write(COMMAND, 0xca);	// Display Control
Write(DATA, 0x00);	// CL divisions Ratio
Write(DATA, 0x10);	// Duty Setting (= 68)
Write(DATA, 0x00);	// N-Line Inverse-set value
Write(COMMAND, 0x31);	// Ext = 1
Write(COMMAND, 0x32);	// Analog Setting
Write(DATA, 0x00);	// OSC Freqency adjustment
Write(DATA, 0x02);	// Booster Efficiency Setting = Level 3
Write(DATA, 0x03);	// Bias Setting (=1/9)
Write(DATA, 0x04);	// Booster X 5
Write(COMMAND, 0x30);	// Ext = 0
Write(COMMAND, 0x81);	// Electronic Volume Control
Write(DATA, 0x2d);	// EV:Vop[5:0]_6bit
Write(DATA, 0x02);	// EV:Vop[8:6]_3bit
	// Vop is 10.52V under this condition for example
Write(COMMAND, 0x20);	// Power Control
Write(DATA, 0x0b);	// B/F/R = On/On/On
delay(50000);	// Delay 50ms
LoadEEPROM();	// Load EEPROM (refer page 68)
LoadPaint();	// Load Gamma Table Parameter (refer page 64)
Write(COMMAND, 0x30);	// Ext = 0
Write(COMMAND, 0xa7);	// Inverse Display
Write(COMMAND, 0xbb);	// Com Scan Direction
Write(DATA, 0x01);	// 0~33 / 67~34
Write(COMMAND, 0xbc);	// Data Scan Direction
Write(DATA, 0x00);	// Page / Column Address Setting
Write(DATA, 0x00);	// RGB arrangement (0:RGB 1:BGR)
Write(DATA, 0x01);	// Gray-scale setup (64-gray: 01H)
Write(COMMAND, 0x75);	// Page address set
Write(DATA, 0x00);	// From page address 0
Write(DATA, 0x43);	// to page address 67
Write(COMMAND, 0x15);	// Column address set
Write(DATA, 0x00);	// From column address 0
Write(DATA, 0x5f);	// to column address 97

```
                                        
Write( COMMAND, 0xaf );                 // Display On
Write( COMMAND, 0x30 );                 // Ext = 0
}
```

B. Adjust Vop Offset

```
void adj_Vop_offset(void)
{
int i,j=1;
while(j)
{
if (KeyScan1==0)i=1;                    // Define KeyScan1 for “D6” use
if (KeyScan2==0)i=2;                    // Define KeyScan2 for “D7” use
if (KeyScan3==0)i=3;                    // Define KeyScan3 for “write” use
if (KeyScan1==1 & KeyScan2==1 & KeyScan3==1)i=4;   // Jump to break
switch (i)
{
  Case 1:
  Write( COMMAND, 0xd6 );               // Vop Offset +1 step
  break;
  case 2:
  Write( COMMAND, 0xd7 );               // Vop Offset -1 step
  break;
  case 3:
  write_7626eeprom();                   // Write EEPROM Flow
  j=0;
  break;
  default:
  break;
}
}
}
```

C. Write EEPROM

```
void write_7626eeprom(void)
{
Write( COMMAND, 0x30 );                 // EXT=0
                                        
Write( COMMAND, 0xae );                 // Display Off
Write( COMMAND, 0x20 );                 // Power Control
Write( DATA, 0x08 );                    // B/F/R = ON/OFF/OFF
                                        
Write( COMMAND, 0x31 );                 // EXT=1
Write( COMMAND, 0xCD );                 // Enable EEPORM Write Mode
Write( DATA, 0x20 );                    //
delay(50000);                           //Delay 50 ms, the range is delay≥50ms
                                        
Write( COMMAND, 0xeb );                 // Select EEPROM
Write( DATA, 0x00 );                    // EEPROM 1st byte
Write( COMMAND, 0xfc );                 // Write Data to EEPROM
delay(50000);                           // Delay 50ms, the range is 10ms < delay < 80ms
                                        
Write( COMMAND, 0xeb );                 // Select EEPROM
Write( DATA, 0x01 );                    // EEPROM 2nd byte
```

Write(COMMAND, 0xfc);	// Write Data to EEPROM
delay(50000);	*//Delay 50 ms, the range is delay≥50ms*
Write(COMMAND, 0xeb);	// Select EEPROM
Write(DATA, 0x02);	// EEPROM 3rd byte
Write(COMMAND, 0xfc);	// Write Data to EEPROM
delay(50000);	*// Delay 50ms, the range is 10ms < delay < 80ms*
Write(COMMAND, 0xeb);	// Select EEPROM
Write(DATA, 0x03);	// EEPROM 4th byte
Write(COMMAND, 0xfc);	// Write Data to EEPROM
delay(50000);	*// Delay 50ms, the range is 10ms < delay < 80ms*
Write(COMMAND, 0xeb);	// Select EEPROM
Write(DATA, 0x04);	// EEPROM 5th byte
Write(COMMAND, 0xfc);	// Write Data to EEPROM
delay(50000);	*// Delay 50ms, the range is 10ms < delay < 80ms*
Write(COMMAND, 0xcc);	// Cancel EEPROM
delay(50000);	// Delay 50ms
Write(COMMAND, 0x30);	// EXT=0
Write(COMMAND, 0x20);	// Power Control
Write(DATA, 0x0b);	// B/F/R = On/On/On
Write(COMMAND, 0xaf);	// Display On

}

7.11 RESET CIRCUIT

When the RST pin reveives a negative reset pulse all internal circuitry will start to initialize. The minimum pulse width for completing the reset sequence is 3 us at Vdd=1.8V. The ststus of ST7626 after reset flow is listed below:

When Power is turned on

Input power (VDD1~VDD5)

↓

Be sure to apply POWER-ON RESET (RESET=LOW)

↓

< Display Setting 1 >	**<< State after reset >>**
Display control (DISCTL)	
Setting clock dividing ratio:	2 divisions
Duty setting:	1/4
Setting reverse rotation number of line:	11H reverse rotations
Common scan direction (COMSCN)	
Setting scan direction:	COM0→COM33, COM34→COM67
Oscillation on (OSCON):	Oscillation off

↓

Sleep-out (SLIPOUT):	Sleep-in

↓

< Power Supply Setting >	**<< State after reset >>**
Electronic volume control (VOLCTR)	
Setting volume value:	0
Setting built-in resistance value:	0 (3.76)
Power control (PWRCTR)	
Setting operation of power supply circuit:	ALL OFF

↓

< Display Setting 2 >	**<< State after reset >>**
Normal rotation of display (DISNOR) / inversion of display (DISINV):	Normal rotation of display
Partial-in (PTLIN) / Partial-out (PLOUT):	Partial-out
Setting fix area:	0
Area scroll set (ASCSET)	
Setting area scroll region:	0
Setting area scroll type:	Full-screen scroll
Scroll start set (SCSTART)	
Setting scroll start address:	0

↓

< Display Setting 3 >	**<< State after reset >>**
Data control (DATCTL)	

Setting normal radiation / inversion of page address:	Normal rotation
Setting normal radiation / inversion of column address:	Normal rotation
Setting direction of address scanner:	Column direction
Setting RGB arrangement:	RGB
Setting gradation:	65K
65K-color position set (RGBSET8)	
Setting color position at 65K-color:	All 0

↓

< RAM Setting >	**<< State after reset >>**
Page address set (PASET)	
Setting start page address:	0
Setting end page address:	0
Column address set (PASET)	
Setting start column address:	0
Setting end column address:	0

↓

< RAM Write >	**<< State after reset >>**
Memory write command (RAMWR)	
Writing displayed data: repeat as many as the number needed and exit by entering other command.	

↓

< Waiting (approximately 100ms) >

Wait until the power supply voltage has stabilized.

Enter the power supply control command first, then wait at least 100ms before entering the Display ON command when the built-in power supply circuit operates. If you do not wait, an unwanted display may appear on the liquid crystal panel.

↓

Display on (DISON):	Display off

Note: If changes are unnecessary after reset, command input is unnecessary.

8. COMMANDS

8.1 Command table

Ext=0															
Command	***A0***	***RD***	***WR***	***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0***	***Function***	***Hex***	***Parameter***	***Index***
DISON	0	1	0	1	0	1	0	1	1	1	1	Display On	AF	None	1
DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display Off	AE	None	2
DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal Display	A6	None	3
DISINV	0	1	0	1	0	1	0	0	1	1	1	Inverse Display	A7	None	4
COMSCN	0	1	0	1	0	1	1	1	0	1	1	Com Scan Direction	BB	1 byte	5
DISCTR	0	1	0	1	1	0	0	1	0	1	0	Display Control	CA	3 byte	6
SLPP	0	1	0	0	0	0	0	0	1	0	0	Sleep In/Out Preparation	04	1 byte	7
SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep In	95	None	8
SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep Out	94	None	9
PASET	0	1	0	0	1	1	1	0	1	0	1	Page Address Set	75	2 byte	10
CASET	0	1	0	0	0	0	1	0	1	0	1	Column Address Set	15	2 byte	11
DATCTL	0	1	0	1	0	1	1	1	1	0	0	Data Scan Direction	BC	3 byte	12
RAMWR	0	1	0	0	1	0	1	1	1	0	0	Writing to Memory	5C	Data	13
RAMRD	0	1	0	0	1	0	1	1	1	0	1	Reading from Memory	5D	Data	14
PLTIN	0	1	0	1	0	1	0	1	0	0	0	Partial display in	A8	2 byte	15
PLTOUT	0	1	0	1	0	1	0	1	0	0	1	Partial display out	A9	None	16
RMWIN	0	1	0	1	1	1	0	0	0	0	0	Read Modify Write In	E0	None	17
RMWOUT	0	1	0	1	1	1	0	1	1	1	0	Read Modify Write Out	EE	None	18
ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area Scroll Set	AA	4 byte	19
SCSTART	0	1	0	1	0	1	0	1	0	1	1	Scroll Start Set	AB	1 byte	20
OSCON	0	1	0	1	1	0	1	0	0	0	1	Internal OSC on	D1	None	21
OSCOFF	0	1	0	1	1	0	1	0	0	1	0	Internal OSC off	D2	None	22
PWRCTL	0	1	0	0	0	1	0	0	0	0	0	Power Control	20	1 byte	23
VOLCTR	0	1	0	1	0	0	0	0	0	0	1	EC control	81	2 byte	24
VOLUP	0	1	0	1	1	0	1	0	1	1	0	EC increase 1	D6	None	25
VOLDOWN	0	1	0	1	1	0	1	0	1	1	1	EC decrease 1	D7	None	26
STREAD	0	0	1	Status Read								Status Read			
EPSRRD1	0	1	0	0	1	1	1	1	1	0	0	READ Register1	7C	None	28
EPSRRD2	0	1	0	0	1	1	1	1	1	0	1	READ Register2	7D	None	29
NOP	0	1	0	0	0	1	0	0	1	0	1	NOP Instruction	25	None	30
EEOK	0	1	0	0	0	0	0	0	1	1	1	EEPROM Function Start	07	1 byte	31
RESERVED	0	1	0	1	0	0	0	0	0	1	0	Not Use	82		32

Ext=1															
Command	***A0***	***RD***	***WR***	***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0***	***Function***	***Hex***	***Parameter***	***Index***
Frame1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 PWM Set	20	16 byte	1
Frame2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 PWM Set	21	16 byte	2
Frame3 Set	0	1	0	0	0	1	0	0	0	1	0	FRAME 3 PWM Set	22	16 byte	3
Frame4 Set	0	1	0	0	0	1	0	0	0	1	1	FRAME 4 PWM Set	23	16 byte	4
ANASET	0	1	0	0	0	1	1	0	0	1	0	Analog Set	32	3 byte	5
EPCTIN	0	1	0	1	1	0	0	1	1	0	1	Control EEPROM	CD	1 byte	6
EPCOUT	0	1	0	1	1	0	0	1	1	0	0	Cancel EEPROM	CC	None	7
EPMWR	0	1	0	1	1	1	1	1	1	0	0	Write to EEPROM	FC	None	8
EPMRD	0	1	0	1	1	1	1	1	1	0	1	Read from EEPROM	FD	None	9
DISPADJ	0	1	0	1	1	1	1	1	0	1	0	Display Performance Adjustment	FA	1 byte	10
IIPP	0	1	0	1	1	1	1	0	1	0	0	Internal Initialize Preparation	F4	1 byte	11

Ext=1 or Ext=0															
Command	***A0***	***RD***	***WR***	***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0***	***Function***	***Hex***	***Parameter***	***Index***
Ext In	0	1	0	0	0	1	1	0	0	0	0	Ext=0 Set	30	None	--
Ext Out	0	1	0	0	0	1	1	0	0	0	1	Ext=1 Set	31	None	--

8.2 EXT="0" Function Description

(1) Display ON (DISON) Command: 1; Parameter: None (AFH)

It is used to turn the display on. When the display is turned on, segment outputs and common outputs are generated at the level corresponding to the display data and display timing. You can't turn on the display as long as the sleep mode is selected. Thus, whenever using this command, you must cancel the sleep mode first.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	1

(2) Display OFF (DISOFF) Command: 1; Parameter: None (AEH)

It is used to forcibly turn the display off. As long as the display is turned off, every on segment and common outputs are forced to VSS level.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	0

(3) Normal display (DISNOR) Command: 1; Parameter: None (A6H)

It is used to normally highlight the display area without modifying contents of the display data RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	0

(4) Inverse display (DISINV) Command: 1; Parameter: None (A7)

It is used to inversely highlight the display area without modifying contents of the display data RAM. This command does not invert non-display areas in case of using partial display.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	1

(5) Common scan (COMSCAN) Command: 1; Parameter: 1 (BBH)

It is used to specify the common output direction in the pin of CSEL = L. This command helps increasing degrees of freedom of wiring on the LCD panel.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	0	1	1	—
Parameter1 (P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Command Scan direction

When CSEL=0 configuration is selected, pins and common outputs are scanned in the order shown below.

P12	P11	P10	Common scan direction					
			COM0 pin		COM33 pin	COM34 pin		COM67 pin
0	0	0	0	→	33	34	→	67
0	0	1	0	→	33	67	→	34
0	1	0	33	→	0	34	→	67
0	1	1	33	→	0	67	→	34

Common scan direction

Original graphic:

P12:P11:P10:0:0:0 (0→33, 34→67)

P12:P11:P10:0:0:1 (0→33, 67→34)

P12:P11:P10:0:1:0 (33→0, 34→67)

P12:P11:P10:0:1:1 (33→0, 67→34)

(6) Display control (DISCTL) Command: 1; Parameter: 3 (CAH)

This command and succeeding parameters are used to perform the display timing-related setups. This command must be selected before using SLPOUT. Don't change this command while the display is turned on.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	0	0	1	0	1	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	*	*	CL dividing ratio, F1 and F2 drive pattern.
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Drive duty
Parameter3(P3)	1	1	0	0	P36	P35	P34	P33	P32	P31	P30	FR inverse-set value

P1: it is used to specify the CL dividing ratio.

P14, P13, P12: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.

P14	P13	P12	CL dividing ratio
0	0	0	Not divide
0	0	1	2 divisions
0	1	0	4 divisions
0	1	1	8 divisions

P2: It is used to specify the duty of the module on block basis.

Duty	*	*	*	P24	P23	P22	P21	P20	(Numbers of display lines)/4-1
Example: 1/68 duty	0	0	0	0	1	1	1	1	64/4-1=15

This will output driving voltage waveforms from com0 to com63.

P3: It is used to specify number of lines to be inversely highlighted on LCD panel from P36 to P30 (lines can be inversely highlighted in the range of 2 to 64)

Inversely highlighted line	P37	P36	P35	P34	P33	P32	P31	P30	Inversely highlighted lines-1
Example: 0AH	0	0	0	0	1	0	1	0	11 (lines)-1 = 10 (lines)
Example: 7CH	0	1	1	1	1	1	0	0	61 (lines)-1 = 60 (lines)

P34=”0”: Frame inversion occurs every frame; P34=”1”: Independent from frames.

In the default, 0 inverse highlighted line is selected.

(7) Sleep In/Out Preparation (SLPP) Command: 1; Parameter: 1

Using this command to setup ready status for sleep-in or sleep out.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	0	1	0	0	—
Parameter(P1)	1	1	0	0	0	1	1	1	1	1	P10	Sleep in/out ready

P10 =” 1”: Ready for sleep in. P10 = “0”: Ready for sleep out.

Parameter 3FH is used to initialize sleep-in sequencing, and parameter 3EH is used to initialize sleep-out sequencing.

(8) Sleep in (SPLIN) Command: 1; Parameter: None (95H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	1

(9) Sleep out (SLPOUT) Command: 1; Parameter: None (94H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	0

(10) Page address set (PASET) Command: 1; Parameter: 2 (75H)

When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the page address area. As the addresses are incremented from the start to the end page in the page-direction scan, the column address is incremented by 1 and the page address is returned to the start page.

Note: that the start and end page must be specified as a pair. Also, the relation “start page < end page” must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	1	1	0	1	0	1	—
Parameter1(P1)	1	1	0	*	P16	P15	P14	P13	P12	P11	P10	Start page
Parameter2(P2)	1	1	0	*	P26	P25	P24	P23	P22	P21	P20	End page

(11) Column address set (CASET) Command: 1; Parameter: 2 (15H)

When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the column address area. As the addresses are incremented from the start to the end column in the column-direction scan, the page address is incremented by 1 and the column address is returned to the start column.

Note: that the start and end column must be specified as a pair. Also, the relation “start column < end column” must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	1	0	1	0	1	—
Parameter1(P1)	1	1	0	*	P16	P15	P14	P13	P12	P11	P10	Start address
Parameter2(P2)	1	1	0	*	P26	P25	P24	P23	P22	P21	P20	End address

(12) Data control (DATCTL) Command: 1; Parameter: 3 (BCH)

This command and succeeding parameters are used to perform various setups needed when MPU operates display data stored on the built-in RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	1	0	0	—
Parameter1(P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Normal/inverse display of page/column address and address scan direction.
Parameter2(P2)	1	1	0	*	*	*	*	*	*	*	P20	RGB arrangement
Parameter3(P3)	1	1	0	*	*	*	*	*	P32	P31	P30	Gray-scale setup

P1: It is used to specify the normal or inverse display of the page / column address and also to specify the address scanning direction.

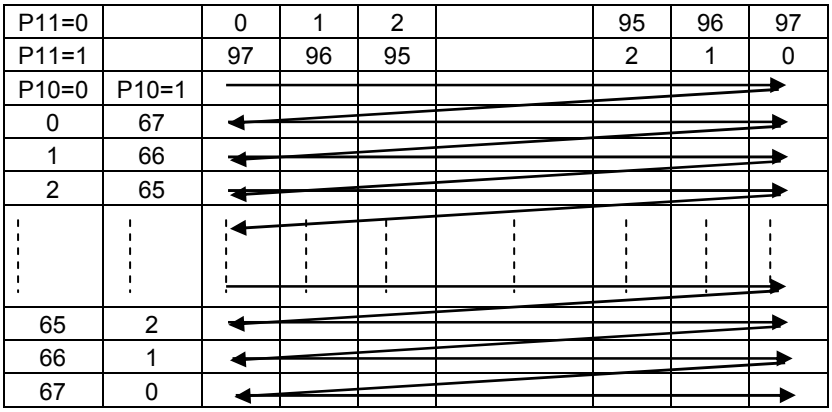
P10: Normal/inverse display of the page address. P10=0: Normal and P10=1: Inverse

P11: Normal/reverse turn of column address. P11=0: Normal rotation and P11=1: Reverse rotation.

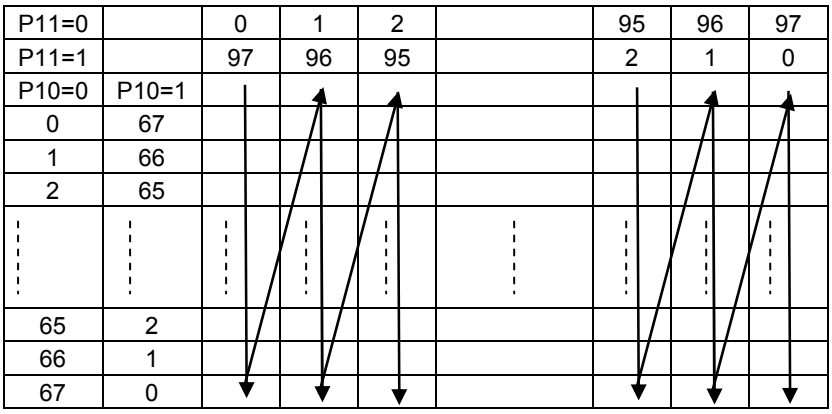
P12: Address-scan direction. P12=0: In the column direction and P12=1: In the page direction.

Page address and page-address scan direction

P12=0 Column direction



P12=1 Page direction



P2: RGB arrangement. This parameter allows you to change RGB arrangement of data which is going to be written into RAM, and therefore causes the inverse RGB rotation of the segment output of ST7626. You can fit RGB arrangement on the LCD panel according to this parameter setting.

P20	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	…	SEG293
0	R	G	B	R	G	B	R	G	…	B
1	B	G	R	B	G	R	B	G	…	R

P3: Gray scale setup. Using this parameter, you can select the 4K, 65K, 262K, and 16M display mode depending on the difference in RGB data arrangement.

P32	P31	P30	Numbers of gray-scale
0	0	1	64-gray 65K
0	1	0	64-gray 262K
1	0	0	64-gray 16M
1	0	1	16-gray 4K Type A
1	1	0	16-gray 4K Type B

(13) Memory write (RAMWR) Command: 1; Parameter: Numbers of data written (5CH)

When MPU writes data to the display memory, this command turns on the data entry mode. Entering this command always sets the page and column address at the start address. You can rewrite contents of the display data RAM by entering data succeeding to this command. At the same time, this operation increments the page or column address as applicable. The write mode is automatically cancelled if any other command is entered.

1. 8-bit bus

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	0	—
Parameter	1	1	0	Data to be written								Data to be written

2. 16-bit bus

	A0	RD	RW	D15	D14	…	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	…	*	*	0	1	0	1	1	1	0	0	Memory write
parameter	1	1	0	Data to be written													Write data

(14) Memory read (RAMRD) Command: 1; Parameter: Numbers of data read (5DH)

When MPU read data from the display memory, this command turns on the data read mode. Entering this command always sets the page and column address at the start address. After entering this command, you can read contents of the display data RAM. At the same time, this operation increments the page or column address as applicable. The data read mode is automatically cancelled if any other command is entered.

1. 8-bit bus

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	1	—
Parameter	1	0	1	Data to be read								Data to be read

2. 16-bit bus

	A0	RD	RW	D15	D14	….	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	*	*	*	0	1	0	1	1	1	0	1	Memory read
parameter	1	0	1	Data to be read													Read data

(15) Partial in (PTLIN) Command: 1; Parameter: 2 (A8H)

This command and succeeding parameters specify the partial display area. This command is used to turn on partial display of the screen (dividing screen by lines) in order to save power. Since ST7626 processes the liquid crystal display signal on 4-line basis (block basis), the display and non-display areas are also specified on 4-bit line (block basis).

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	0	0	—
Parameter(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Start block address
Parameter(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	End block address

A block address that can be specified for the partial display must be the display one (don't try to specify an address not to be displayed when scrolled).

(16) Partial out (PTLOUT) Command: 1; Parameter: 0 (A9H)

This command is used to exit from the partial display mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	0	0	1

(17) Read modify write in (RMWIN) Command: 1; Parameter: 0 (E0H)

This command is used along with the column address set command, page address set command and read modify write out command. This function is used when frequently modifying data to specify a specific display area such as blinking cursor. First set a specific display area using the column and page address commands. Then, enter this command to set the column and page addresses at the start address of the specific area. When this operation is complete, the column (page) address won't be modified by the display data read command. It is incremented only when the display data write command is used. You can cancel this mode by entering the read modify write out or any other command.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	0	0	0

(18) Read modify write out (RMWOUT) Command: 1; Parameter: 0 (EEH)

Enter this command cancels the read modify write mode

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	1	1	1	0

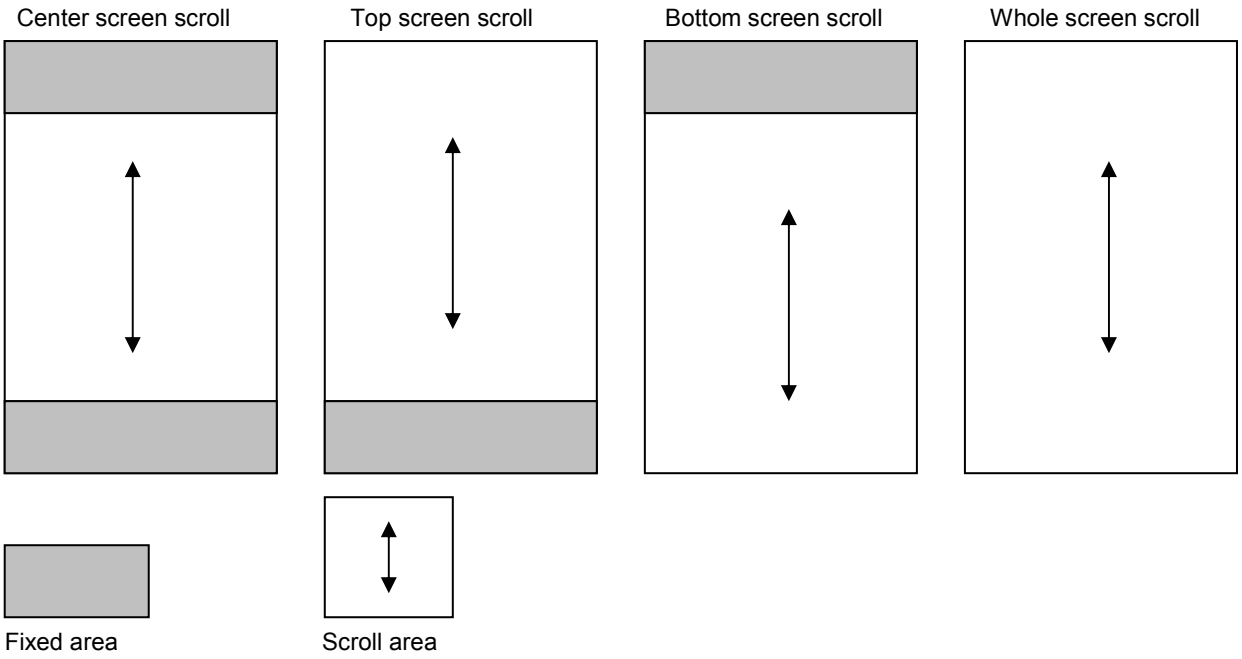
(19) Area scroll set (ASCSET) Command: 1; Parameter: 4 (AAH)

It is used when scrolling only the specified portion of the screen (dividing the screen by lines). This command and succeeding parameters specify the type of area scroll, fix area and scroll area.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	0	—
Parameter(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Top block address
Parameter(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Bottom block address
Parameter(P3)	1	1	0	*	*	*	P34	P33	P32	P31	P30	Number of specified blocks
Parameter(P4)	1	1	0	*	*	*	*	*	*	P41	P40	Area scroll mode

P4: It is used to specify an area scroll mode.

P41	P40	Type of area scroll
0	0	Center screen scroll
0	1	Top screen scroll
1	0	Bottom screen scroll
1	1	Whole screen scroll



Since ST7626 processes the liquid crystal display signals on the four-line basis (block basis), FIX and scroll areas are also specified on the four-line basis (block basis).

DDRAM address corresponding to the top FIX area is set in the block address incrementing direction starting with 0 block. DDRAM address corresponding to the bottom FIX area is set in the block address decreasing direction starting with 16st block. Other DDRAM blocks excluding the top and bottom FIX areas are assigned to the scroll + background areas.

P1: It is used to specify the top block address of the scroll + background areas. Specify the 0th block for the top screen scroll or whole screen scroll.

P2: It specifies the bottom address of the scroll+ background areas. Specify the 16th block for the bottom or whole screen scroll.

Required relation between the start and end blocks (top block address<bottom block address) must be maintained.

P3: It specifies a specific number of blocks {Numbers of (Top FIX area +Scroll area) block-1}. When the bottom scroll or whole screens scroll, the value is identical with P2.

You can turn on the area scroll function by executing the area scroll set command first and then specifying the display start block of the scroll area with the scroll start set command.

[Area Scroll Setup Example]

In the center screen scroll of 1/48 duty (display range: 48 lines = 12 blocks), if 8 lines = 2 blocks and 8 lines = 2 blocks are specified for the top and bottom FIX areas, 36 lines = 9 blocks is specified for the scroll areas, respectively, 16 lines = 4 blocks on the DDRAM are usable as the background area. Value of each parameter at this time is as shown below.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	
P1	1	1	0	*	*	*	0	0	0	1	0	Top block address = 02 H
P2	1	1	0	*	*	*	0	1	1	1	0	Bottom block address = 0E H
P3	1	1	0	*	*	*	0	1	1	0	0	Number of specific blocks = 09 H
P4	1	1	0	*	*	*	*	*	*	0	0	Area scroll mode = center

(20) Scroll start address set (SCSTART) Command:1 Parameter: 1 (ABH)

This command and succeeding parameters are used to specify the start block address of the scroll area.

Note: that you must execute this command after executing the area scroll set command. Scroll becomes available by dynamically changing the start block address.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	1	—
Parameter(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Start block address

(21) Internal oscillation on (OSCON) Command: 1; Parameter: 0 (D1H)

This command turns on the internal oscillation circuit. It is valid only when the internal oscillation circuit of CLS = HIGH is used.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	0	1

(22) Internal oscillation off (OSOFF) Command: 1; Parameter: 0 (D2H)

It turns off the internal oscillation circuit. This circuit is turned off in the reset mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	1	0

(23) Power control set (PWRCTR) Command: 1; Parameter: 1 (20H)

This command is used to turn on or off the Booster circuit, follower voltage, and voltage regulator circuit.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	1	0	0	1	0	0	0	0	0	—
Parameter(P1)	1	1	0	*	*	*	0	P13	0	P11	P10	LCD drive power

P10: It turns on or off the voltage regulator voltage.

P10 = “1”: ON. P10 =” 0”: OFF

P11: It turns on or off the follower circuit.

P11 = “1”: ON. P11 =” 0”: OFF

P13:It turns on or off the Booster.

P13 = “1”: ON. P13 =” 0”: OFF

(24) Electronic volume control (VOLCTR) Command: 1; Parameter: 2 (81H)

The command is used to program the optimum LCD supply voltage VOP. Reference to 7.10.2

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	0	0	0	0	0	1	—
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Set Vop[5:0]
Parameter(P2)	1	1	0	*	*	*	*	*	P18	P17	P16	Set Vop[8:6]

(25) Increment electronic control (VOLUP) Command: 1; Parameter: 0 (D6H)

With the VOLUP and VOLDOWN command the VOP voltage and therewith the contrast of the LCD can be adjusted.

This command increments electronic control value Vop[5:0] of voltage regulator circuit by 1.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	0

If you set the electronic control value to 111111, the control value is set to 000000 after this command has been executed.

(26) Decrement electronic control (VOLDOWN) Command: 1; Parameter: 0 (D7H)

With the VOLUP and VOLDOWN command the VOP voltage and therewith the contrast of the LCD can be adjusted.

This command decrements electronic control value Vop[5:0] of voltage regulator circuit by 1.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	1

If you set the electronic control value to 000000, the control value is set to 111111 after this command has been executed.

Table 8.1.1 Possible Vop[5:0] values

Electronic Control Value	Decimal Equivalent	VOP Offset
111111	31	+1240 mV
111110	30	+1200 mV
111101	29	+1160 mV
…	…	…
000010	2	+80 mV
000001	1	+40 mV
000000	0	0 mV
111111	-1	-40 mV
111110	-2	-80 mV
…	…	…
100010	-30	-1200 mV
100001	-31	-1240 mV
100000	-32	-1280mV

(27) Status read (STREAD) Command: 1; Parameter: None

It is the command for reading the internal condition of the IC.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	0	1	(8) Status data							

Issue STREAD (Status Read) command is only for reading the internal condition of the IC. One status data can be displayed depending on the setting. Issue the NOP command after the STREAD (Status Read) command.

The Status data will be composed of 8 bits below:

D7: Area scroll mode	Refer to P41 (ASCSET)	
D6: Area scroll mode	Refer to P40 (ASCSET)	
D5: RMW on/off	0 : Out	1 : In
D4: Scan direction	0 : Column	1 : Page
D3: Display ON/OFF	0 : OFF	1 : ON
D2: EEPROM access	0: OutAccess	1: InAccess
D1: Display normal/inverse	0 : Normal	1 : Inverse
D0: Partial display	0 : OFF	1 : ON

(28) Read Register 1 (EPSRRD1) Command: 1; Parameter: 0 (7CH)

It is the command for reading the Electronic Control values.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	0

Issue the EPSRRD1 and then STREAD (Status Read) commands in succession to read the Electronic Control values. One status data can be displayed depending on the setting. Also, always issue the NOP command after the STREAD (Status Read) command.

The Status data will be composed of 8 bits below:

D7: 0	
D6: 0	
D[5:0]: Vop[5:0]	Refer to electronic volume control values Vop[5:0]

(29) Read Register 2 (EPSRRD2) Command: 1 ;Parameter: 0 (7DH)

It is the command for reading ID codes of the ST7626 and the built-in resistance ratio.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	1

Issue the EPSRRD2 and then STREAD (Status Read) commands in succession to read IC's ID and the built-in resistance ratio. One status data can be displayed depending on the setting. Also, always issue the NOP command after the STREAD (Status Read) command.

The Status data will be composed of 8 bits below:

D[7:3]: ST7626 ID codes 00010

D[2:0]: Vop[8:6] Refer to the built-in resistance ratio Vop[8:6]

(30) Non-operating (NOP) Command: 1; Parameter: 0 (25H)

This command does not affect the operation.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	0	0	1	0	1

This command, however, has the function of canceling the IC test mode. Thus, it is recommended to enter it periodically to prevent malfunctioning due to noise and such.

(31) EEPROM Function Start (EEOK) Command:1;Parameter:1(07H)

In the EEPROM read/write flow, EEPROM is ready after issuing this command. Its parameter is set to 19H.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	0	1	1	1	—
Parameter(P1)	1	1	0	0	0	0	1	1	0	0	1	19H

(32) Reserved (82H)

Do not use this command

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	0	0	0	1	0

8.3 EXT="1" Function Description

(1) Set Frame1 value (Frame1 set) Command: 1; Parameter: 16 (20H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Frame1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set RGB level 0 of 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set RGB level 1 of 1st frame
Parameter15(P15)	1	1	0	*	*	*	P154	P153	P152	P151	P150	Set RGB level 14 of 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set RGB level 15 of 1st frame

(2)Set Frame2 value (Frame2 set) Command: 1; Parameter: 16 (21H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Frame2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set RGB level 0 of 2nd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set RGB level 1 of 2nd frame
Parameter15(P15)	1	1	0	*	*	*	P154	P153	P152	P151	P150	Set RGB level 14 of 2nd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set RGB level 15 of 2nd frame

(3) Set Frame3 value (Frame3 set) Command: 1; Parameter: 16 (22H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Frame3 Set	0	1	0	0	0	1	0	0	0	1	0	FRAME 3 PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set RGB level 0 of 3rd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set RGB level 1 of 3rd frame
Parameter15(P15)	1	1	0	*	*	*	P154	P153	P152	P151	P150	Set RGB level 14 of 3rd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set RGB level 15 of 3rd frame

(4) Set Frame4 value (Frame4 set) Command: 1; Parameter: 16 (23H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Frame4 Set	0	1	0	0	0	1	0	0	0	1	1	FRAME 4 PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set RGB level 0 of 4th frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set RGB level 1 of 4th frame
Parameter15(P15)	1	1	0	*	*	*	P154	P153	P152	P151	P150	Set RGB level 14 of 4th frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set RGB level 15 of 4th frame

The default value of RGB level set

	FRAM1 SET	FRAM2 SET	FRAM3 SET	FRAME4 SET
RGB level0	00	00	00	00
RGB level1	02	02	02	02
RGB level2	04	04	04	04
RGB level3	06	06	06	06
RGB level4	08	08	08	08
RGB level5	0A	0A	0A	0A
RGB level6	0C	0C	0C	0C
RGB level7	0E	0E	0E	0E
RGB level8	10	10	10	10
RGB level9	12	12	12	12
RGB level10	14	14	14	14
RGB level11	16	16	16	16
RGB level12	18	18	18	18
RGB level13	1A	1A	1A	1A
RGB level14	1C	1C	1C	1C
RGB level15	1E	1E	1E	1E

All the modulation range of each level for each frame is from 00'H to 1F'H.

Example：Paint setup

```
void LoadPaint( void )
{
        Write( COMMAND, 0x0031 );           // Ext = 1

        Write( COMMAND, 0x0020 );           // Palette FRC1 Setup
        Write( DATA, 0x0000 );              // RGB Level0 Setup
        Write( DATA, 0x0002 );              // RGB Level1 Setup
        Write( DATA, 0x0005 );              // RGB Level2 Setup
```

```
        …….                                  …….
        Write( DATA, 0x001E );              // RGB Level15 Setup

        Write( COMMAND, 0x0021 );           // Palette FRC2 Setup
        Write( DATA, 0x0000 );              // RGB Level0 Setup
        Write( DATA, 0x0002 );              // RGB Level1 Setup
        Write( DATA, 0x0005 );              // RGB Level2 Setup
        …….                                  …….
        Write( DATA, 0x001E );              // RGB Level15 Setup

        Write( COMMAND, 0x0022 );           // Palette FRC3 Setup
        Write( DATA, 0x0000 );              // RGB Level0 Setup
        Write( DATA, 0x0002 );              // RGB Level1 Setup
        Write( DATA, 0x0005 );              // RGB Level2 Setup
        …….                                  …….
        Write( DATA, 0x001E );              // RGB Level15 Setup

        Write( COMMAND, 0x0023 );           // Palette FRC4 Setup
        Write( DATA, 0x0000 );              // RGB Level0 Setup
        Write( DATA, 0x0002 );              // RGB Level1 Setup
        Write( DATA, 0x0005 );              // RGB Level2 Setup
        …….                                  …….
        Write( DATA, 0x001E );              // RGB Level15 Setup

        Write( COMMAND, 0x0030 );           // Ext = 0
}
```

(5) Analog set (ANASET) Command 1; Parameter: 3 (32H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	1	0	0	1	0	—
Parameter1(P1)	1	1	0	*	*	*	*	*	P12	P11	P10	OSC frequency Adjustment
Parameter2(P2)	1	1	0	*	*	*	*	*	*	P21	P20	Booster Efficiency Set
Parameter3(P3)	1	1	0	*	*	*	*	*	P32	P31	P30	Bias setting
Parameter4(P4)	1	1	0	*	*	*	*	*	P42	P41	P40	Booster setting

P1: OSC frequency adjustment

P12	P10	P10	CL pin frequency (KHz) : CL dividing ratio setting = 00H (No division)	CL pin frequency (KHz) : CL dividing ratio setting = 04H (Divided by 2)
0	0	0	5.39	2.70
0	0	1	5.64	2.82
0	1	0	6.18	3.09
0	1	1	6.83	3.42
1	0	0	7.65	3.82
1	0	1	8.68	4.34
1	1	0	10.10	5.05
1	1	1	12.02	6.01

OSC frequency can be adjusted by P1 setting and command CAH, see page 46.

The default OSC frequency (CL pin frequency) is 5.39 KHz.

And the frame frequency is from OSC frequency and duty setting, as the formula shown below:

Frame frequency = OSC frequency/(Duty+1)

Example:

1. duty=68, P1 setting=[000], frame frequency=5.39KHz/78.12Hz
2. duty=64, P1 setting=[101], frame frequency=8.68KHz/133.53Hz

P2: Booster Efficiency set

P21	P20	Frequency (Hz)
0	0	Level 1
0	1	Level 2
1	0	Level 3
1	1	Level 4

By Booster Stages (2X, 3X, 4X, 5X) and Booster Efficiency (Level1~4) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to lower level (level1 is higher than level4). The Boost Efficiency is better than higher level, and it just need few more power consumption current.

P3: Select LCD bias ratio of the voltage required for driving the LCD.

P32	P31	P30	LCD bias
0	0	0	1/12
0	0	1	1/11
0	1	0	1/10
0	1	1	1/9
1	0	0	1/8
1	0	1	1/7
1	1	0	1/6
1	1	1	1/5

P4: Booster setting.

P42	P41	P40	
0	0	0	Booster off
0	0	1	2 times boosting circuit
0	1	0	3 times boosting circuit
0	1	1	4 times boosting circuit
1	0	0	5 times boosting circuit

(6) Control EEPROM: 1; Parameter: 1 (CDH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	1
Parameter1(P1)	1	1	0	*	*	P15	*	*	*	*	*

P15: when setting "1" ➔ The Write Enable of EEPROM will be opened.

P15: when setting "0" ➔ The Read Enable of EEPROM will be opened.

(7) Cancel EEPROM Command: 1; Parameter: None (CCH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	0

(8) Write data to EEPROM (EPMWR) Command: 1; Parameter: None (FCH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	0

(9) Read data from EEPROM (EPMWR) Command: 1; Parameter: None (FDH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	1

(10) Display performance adjustment (DISPADJ) Command: 1; Parameter: 1 (FAH)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	1	1	1	0	1	0	Display performance adjustment
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Fine tuning level set

ST7626 provide the function of 32 levels fine tuning to adjust best crosstalk performance for each module. Just like Vop offset for different modules, the fine tuning level value can also be stored in EEPROM, and therefore each module can have its individual setup for best display performance.

Due to IC and module process variation, it's hard for all modules to have same display performance. By using this command, different modules can adjust to the best performance by having different parameters of DISPADJ. When loading EEPROM, this individual parameter can be loaded into IC and best display performance can be achieved. Detail using method please refer ST7626 EEPROM User Manual guide.

(11) Internal Initialize Preparation (IIPP) Command: 1; Parameter: 1 (F4H)

Use this command to set internal initializing for ready status.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	1	1	0	1	0	0	—
Parameter(P1)	1	1	0	0	1	0	1	1	0	0	0	Internal initialize sequencing

8.4 EXT=”0” or ”1” Function Description

(1) Extension instruction disable (EXT IN) Command:1 Parameter: None (30H)

Use the “Ext=0” command table

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	0

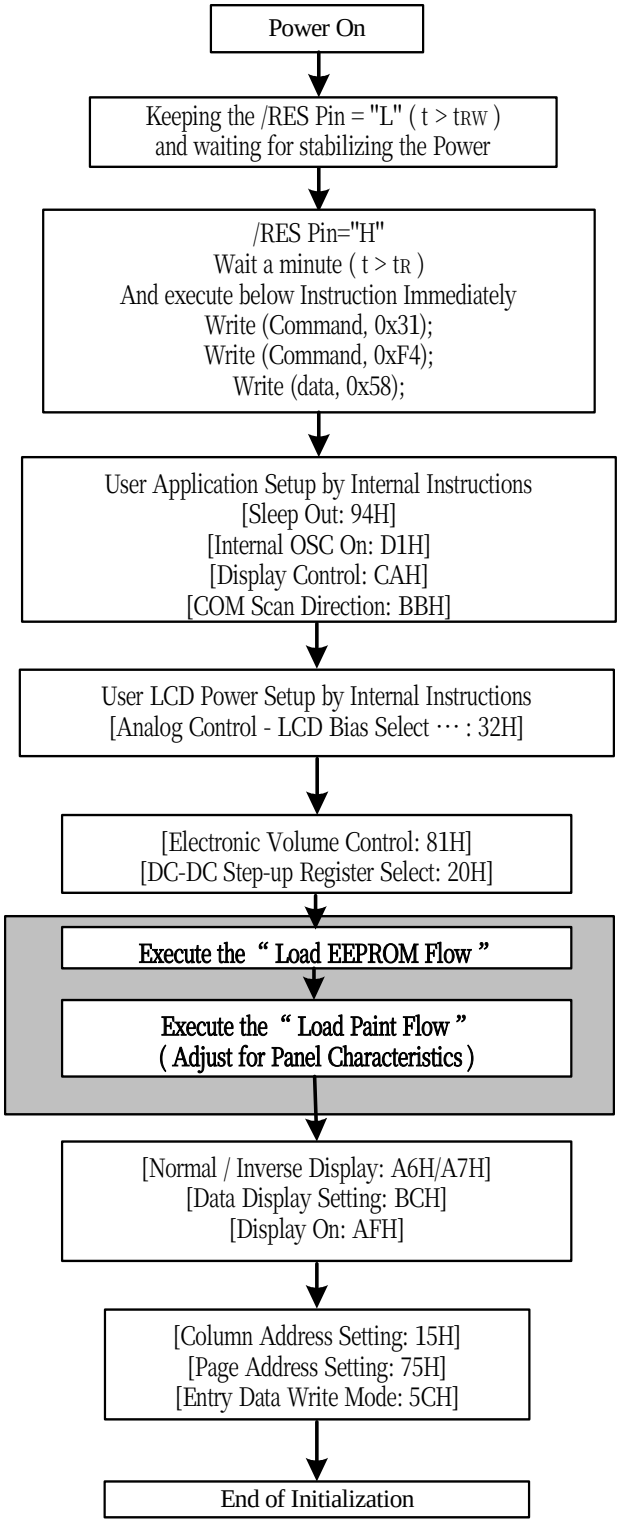
(2) Extension instruction enable (EXT OUT) Command:1 Parameter: None (31H)

Use the extended command table (EXT=”1”)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	1

8.5 Referential Instruction Setup Flow

8.5.1 Initializing with the Built-in Power Supply Circuits



Example：ST7626 Initial setting for 98X68

```
void ST7626_Init( void )
{
        Write( COMMAND, 0x30 );         // Ext = 0
        Write( COMMAND, 0x04 );         //Sleep In/Out Preparation
        Write( DATA, 0x3e );            //Sleep In/Out Sequencing

        Write( COMMAND, 0x31 );         // Ext = 1
        Write( COMMAND, 0xf4 );         // Internal Initialize Preparation
        Write( DATA, 0x58 );            // Internal Initialize Sequencing

        Write( COMMAND, 0x30 );         // Ext = 0
        Write( DATA, 0x10 );            // Duty Setting (= 68)
        Write( DATA, 0x00 );            // N-Line Inverse-set value

        Write( COMMAND, 0x31 );         // Ext = 1
        Write( COMMAND, 0x32 );         // Analog Setting
        Write( DATA, 0x00 );            // OSC Freqency adjustment
        Write( DATA, 0x02 );            // Booster Efficiency Setting is level3
        Write( DATA, 0x03 );            // Bias Setting (=1/9)
        Write( DATA, 0x04 );            // Booster is X5

        Write( COMMAND, 0x30 );         // Ext = 0
        Write( COMMAND, 0x81 );         // Electronic Volume Control
        Write( DATA, 0x2D );            // EV:Vop[5:0]_6bit
        Write( DATA, 0x02 );            // EV:Vop[8:6]_3bit
                                        // Vop is 10.52V under this condition for example
        Write( COMMAND, 0x20 );         // Power Control
        Write( DATA, 0x0b );            // B/F/R = On/On/On

        delayms(50);                    // Delay 50ms
        LoadEEPROM()                    // Load EEPROM example program (refer page 68)

        LoadPaint();                    // Load Gamma Table Parameter (refer page 61)

        Write( COMMAND, 0x30 );         // Ext = 0
        Write( COMMAND, 0xa7 );         // Inverse Display
        Write( COMMAND, 0xbb );         // Com Scan Direction
        Write( DATA, 0x01 );            // 0~33 / 67~34
        Write( COMMAND, 0xbc );         // Data Scan Direction
        Write( DATA, 0x00 );            // Page / Column Address Setting
        Write( DATA, 0x00 );            // RGB arrangement (0:RGB 1:BGR)
        Write( DATA, 0x01 );            // Gray-scale setup ( 64-gray: 01H)

        Write( COMMAND, 0x75 );         // Page address set
        Write( DATA, 0x00 );            // From page address 0
        Write( DATA, 67 );              // to page address 67
        Write( COMMAND, 0x15 );         // Column address set
        Write( DATA, 0x00 );            // From column address 0
        Write( DATA, 97 );              // to column address 97

        Write( COMMAND, 0xaf );         // Display On
        Write( COMMAND, 0x30 );         // Ext = 0
}
```

Example：Load EEPROM

```
void LoadEEPROM( void )
{
    Write( COMMAND, 0x31 );      // Ext = 1
    Write( COMMAND, 0xcd );      // Enable EEPROM
    Write( DATA, 0x00 );         //
    delayms(50);                 // Delay 50ms
    Write( COMMAND, 0xfd );      // Load EEPROM
    delayms(50);                 // Delay 50ms
    Write( COMMAND, 0xcc );      // Disable EEPROM
    Write( COMMAND, 0x30 );      // Ext = 0
}
```

8.5.2 Data Displaying

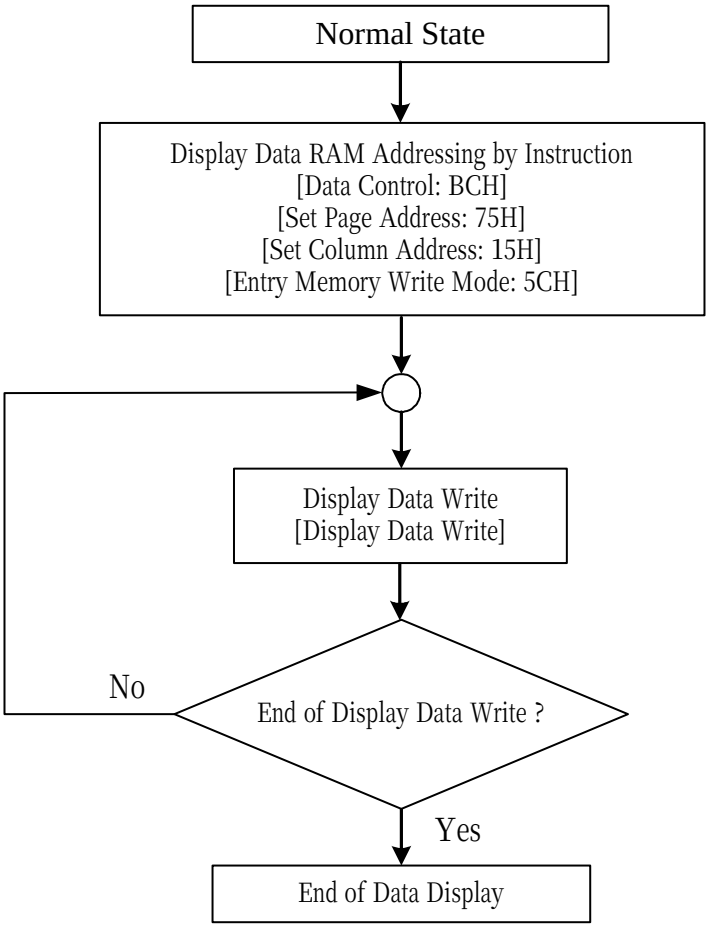


Figure 8.5.2.1 Data Displaying

Example：Display for 98X68

```
void Display( char *pattern )
{
        unsigned char i, j;

        Write( COMMAND, 0x30 );                 // Ext = 0
        Write( COMMAND, 0x15 );                 // Column address set
        Write( DATA, 0 );                       // From column address 0 to 97
        Write( DATA, 97 );
        Write( COMMAND, 0x75 );                 // Page address set
        Write( DATA, 0 );                       // From page address 0 to 67
        Write( DATA, 67 );
        Write( COMMAND, 0x5c )                  // Entry Memory Write Mode
        for( j = 0; j < 68 ; j++ )
            for( i = 0 ; i < 98 ; i++ )
                Write( DATA, pattern[ j ][ i ] );   // Display Data Write

    }
```

8.5.3 Partial Display In/Out

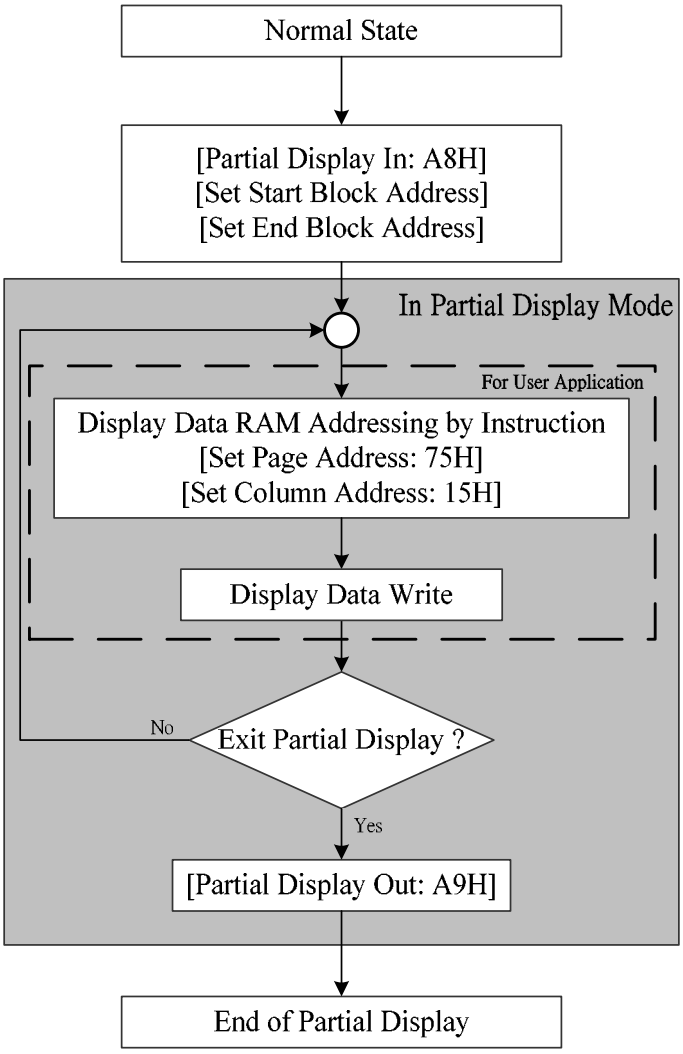


Figure 8.5.3.1 Partial Display In/Out

Example：Partial Display In Operation

```
void PartailIn( unsigned char start_block, unsigned char end_block )
{
        Write( COMMAND, 0x30 );             // Ext = 0
        Write( COMMAND, 0xA8);              // Partial Display In Function
        Write( DATA, start_block );         // Start Block
        Write( DATA, end_block );           // End Block

}

void PartailOut( void )
{
        Write( COMMAND, 0x30 );             // Ext = 0
        Write( COMMAND, 0xA9 );             // Partial Display Out Function
}

void main()
{

        PartialIn( 11, 18 );                // entry partial display mode

        Windowing( 0, 11*4, 131, 18*4 );    // set the page and column range
        PartialDisplay( display_pattern );  // Fill the data into partial display area
            .
            .
            .
        PartialOut();                       // Out of partial display mode

}
```

8.5.4 Scroll Display

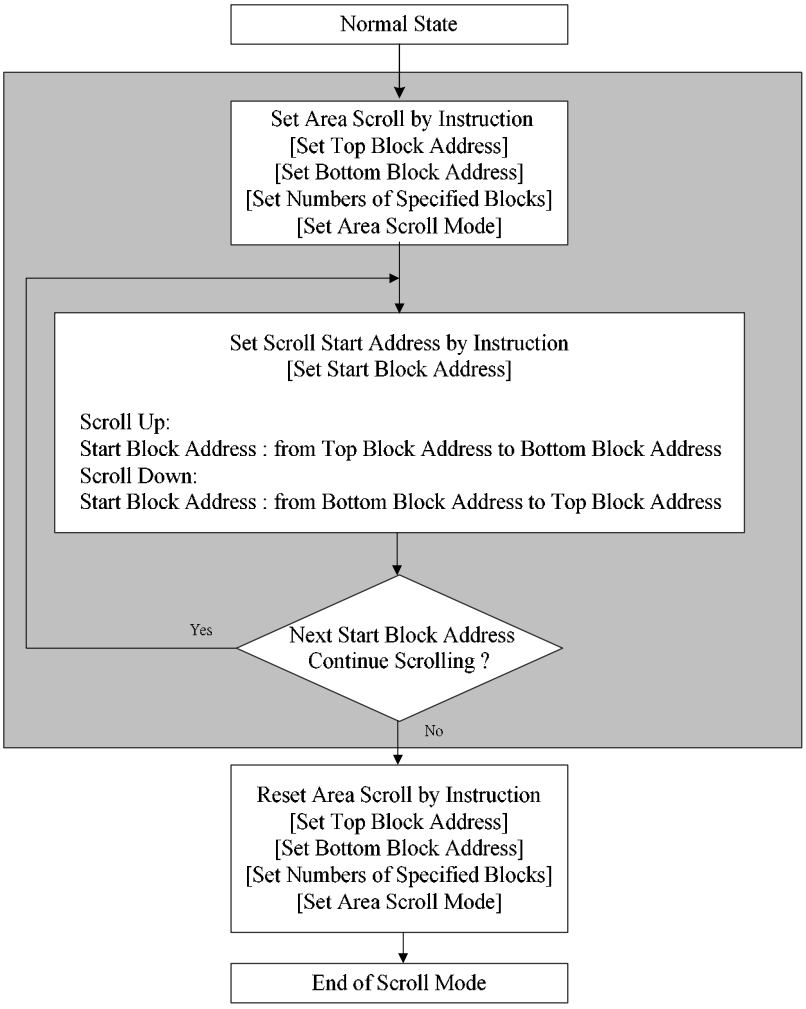


Figure 8.5.4.1 Scroll Display

Example：Screen Scroll Operation

```
void CenterScreenScroll( void )
{
        Write( COMMAND, 0x30 );         // Ext = 0
        Write( COMMAND, 0xAA);          // Partial Display In Function
        Write( DATA, 0x0a );            // Top_Block=10
        Write( DATA, 0x14 );            // Bottom_Block=20
        Write( DATA, 0x14 );            // Number of Specified Blocks=Bottom_Block=20
        Write( DATA, 0x00 );            // Area Scroll Type=Center Screen Scroll

        ScrollUp() or ScrollDown();     // Scroll Up or Scroll Down
}

void TopScreenScroll( void )
{
        Write( COMMAND, 0x30 );         // Ext = 0
        Write( COMMAND, 0xAA);          // Partial Display In Function
        Write( DATA, 0x00 );            // Top_Block=0
        Write( DATA, 0x14 );            // Bottom_Block=20
        Write( DATA, 0x14 );            // Number of Specified Blocks=Bottom_Block=20
        Write( DATA, 0x01 );            // Area Scroll Type=Top Screen Scroll
        ScrollUp() or ScrollDown();     // Scroll Up or Scroll Down
}
```

```
void BottomScreenScroll( void )
{
        Write( COMMAND, 0x30 );             // Ext = 0
        Write( COMMAND, 0xAA);              // Partial Display In Function
        Write( DATA, 0x0a );                // Top_Block=10
        Write( DATA, 0x20 );                // Bottom_Block=32
        Write( DATA, 0x20 );                // Number of Specified Blocks=Bottom_Block=32
        Write( DATA, 0x02 );                // Area Scroll Type=Bottom Screen Scroll
        ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down
}

void WholeScreenScroll( void )
{
        Write( COMMAND, 0x30 );             // Ext = 0
        Write( COMMAND, 0xAA);              // Partial Display In Function
        Write( DATA, 0x00 );                // Top_Block=0
        Write( DATA, 0x20 );                // Bottom_Block=32
        Write( DATA, 0x20 );                // Number of Specified Blocks=Bottom_Block=32
        Write( DATA, 0x03 );                // Area Scroll Type=Whole Screen Scroll
        ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down
}

void ScrollUp( void )
{
        Write( COMMAND, 0x30 );             // Ext = 0
        Write( COMMAND, 0xAB);              // Scroll Start Set
        Write( DATA, Top_Block);            // Start Block Address=Top_Block
        Delay();                            // Delay

        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Top_Block +1 );        // Start Block Address= Top_Block+1
        Delay();                            // Delay

        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Top_Block +2 );        // Start Block Address= Top_Block +2
        Delay();                            // Delay
        ......
        ......
        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Bottom_Block );        // Start Block Address= Bottom_Block
        Delay();                            // Delay
}
void ScrollDown( void )
{
        Write( COMMAND, 0x30 );             // Ext = 0
        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Bottom_Block);         // Start Block Address= Bottom_Block
        Delay();                            // Delay

        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Bottom_Block -1 );     // Start Block Address= Bottom_Block -1
        Delay();                            // Delay

        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Bottom_Block -2 );     // Start Block Address= Bottom_Block -2
        Delay();                            // Delay
        ......
        ......
        Write( COMMAND, 0x00AB);            // Scroll Start Set
        Write( DATA, Top _Block );          // Start Block Address= Top_Block
        Delay();                            // Delay
}
```

8.5.5 Read-Modify-Write Cycle

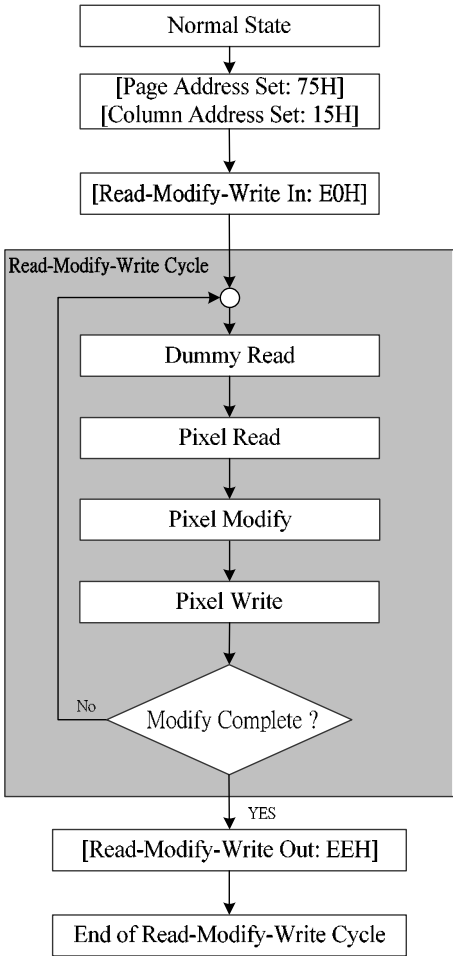


Figure 8.5.5.1 Read-Write-Modify Cycle

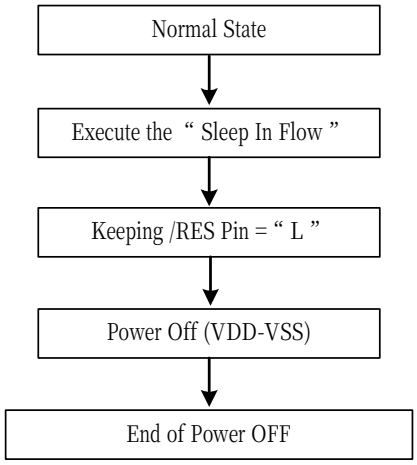
Example：Read-Write-Modify Cycle

```
void ReadModifyWriteIn( void )
{
        Write( COMMAND, 0x30 );        // Ext = 0
        Write( COMMAND, 0xE0 );        // Entry the Read-Modify-Write mode
}

void ReadModifyWriteOut( void )
{
        Write( COMMAND, 0x30 );        // Ext = 0
        Write( COMMAND, 0xEE );        // Out of partial display mode
}
```

```
extern unsigned char *display_pattern;
void main()
{
        unsigned pixel, i;

        Windowing( 11, 31, 80, 50 );          // set the page and column range
        ReadModifyWriteIn();                  // entry the Read-Modify-Write mode

        for( i = 0 ; i < 1400 ; i++ )
          {
           Read( DATA );                      // For dummy read
           pixel = Read( DATA );              // Pixel read
           pixel = pixel & 0x07ff;            // Pixel modify: red filter
           Write( DATA, pixel );
          }

        ReadModifyWriteOut();                 // Out of Read-Modify-Write mode

}
```

8.5.6 Power OFF

Power OFF



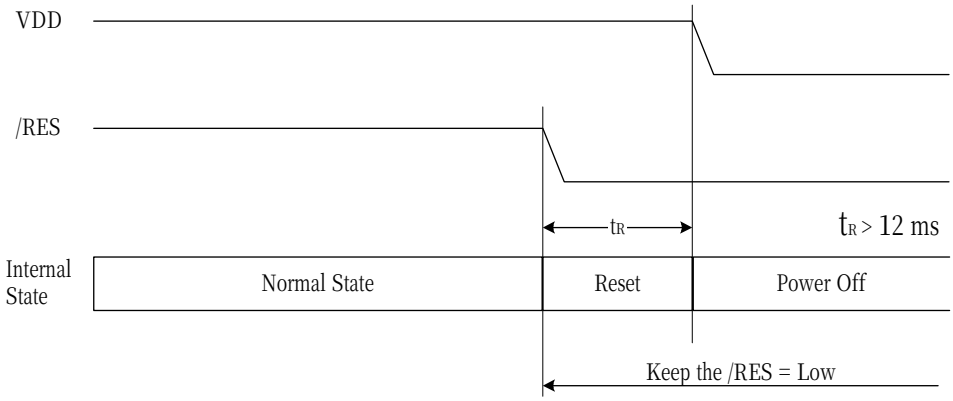


Figure 8.5.6.1 Power off

8.5.7 Sleep In/Out

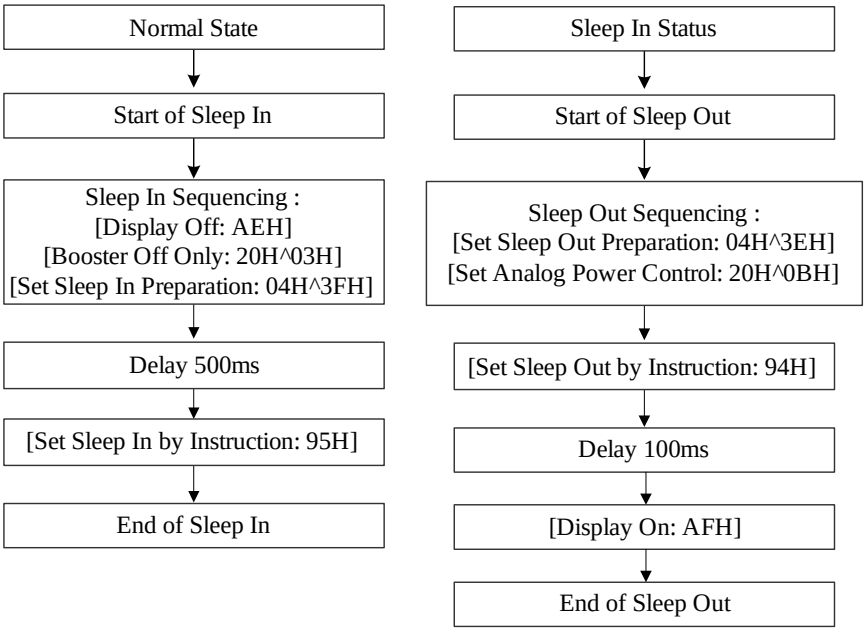


Fig 8.5.7.1 Sleep In/Out Flow

Example：Sleep In Operation

```
void SleepIn( void )
{
        Write( COMMAND, 0x30 );        // Ext = 0
        Write( COMMAND, 0xae );        // Display Off
        Write( COMMAND, 0x20);         // Power Control
        Write( DATA, 0x03 );           // B/F/R = Off/On/On
        Write( COMMAND, 0x04 );        // Sleep In Preparation
        Write( DATA, 0x3f );           // Sleep In Sequencing
        Delay( 500ms);                 // Delay 500ms
        Write( COMMAND, 0x95 );        // Sleep In
}
```

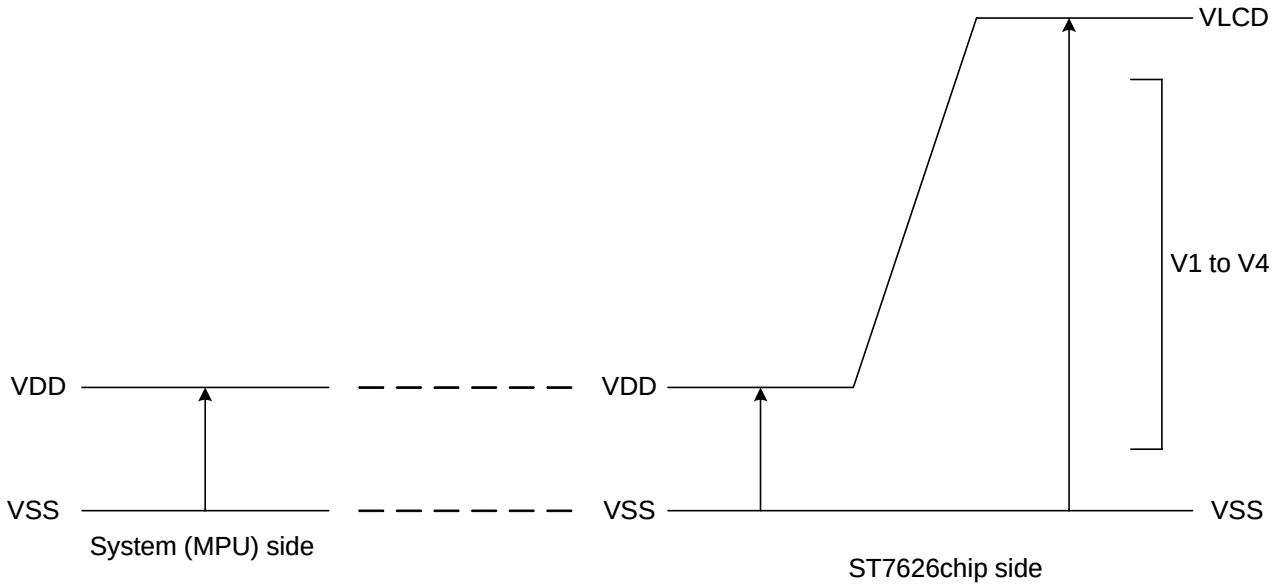
Example：Sleep Out Operation

```
void SleepOut( void )
{
        Write( COMMAND, 0x30 );        // Ext = 0
        Write( COMMAND, 0x04 );        // Sleep Out Preparation
        Write( DATA, 0x3e );           // Sleep Out Sequencing
        Write( COMMAND, 0x20 );        // Power Control
        Write( DATA, 0x0b );           // B/F/R = On/On/On
        Write( COMMAND, 0x94 );        // Sleep Out
        Delay( 100ms );                // Delay 100ms
        Write( COMMAND, 0xaf );        // Display On
}
```

9. LIMITING VALUES

In accordance with the Absolute Maximum Rating System of Bare Die; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power supply voltage	VDD, VDD1~VDD5	–0.5 ~ +4.0	V
Power supply voltage	$VLCD_{IN}$	–0.5 ~ +20	V
Power supply voltage	V1, V2, V3, V4	0.3 to $VLCD_{IN}$	V
Input voltage	VIN	–0.5 to VDD+0.5	V
Output voltage	VO	–0.5 to VDD+0.5	V
Operating temperature (die)	TOPR	–30 to +85	°C
Storage temperature (die)	TSTR	–40 to +125	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. Insure that the voltage levels of V1, V2, V3, and V4 are always such that

   $VLCD_{IN} \geqq V0 \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq VSS$

10. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS devices”).

11. DC CHARACTERISTICS

V_{DD} = 1.8 V to 3.3V; V_{SS} = 0 V; V0 = 3.76 to 18.0V; T_{amb} = -30℃ to +85℃; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
High-level Input Voltage		VIHC			0.7 x VDD	—	VDD	V	*1
Low-level Input Voltage		VILC			VSS	—	0.3 x VDD	V	*1
High-level Output Voltage		VOHC			0.7 x VDD	—	VDD	V	*2
Low-level Output Voltage		VOLC			VSS	—	0.3 x VDD	V	*2
Input leakage current		ILI	VIN = VDD or VSS		-1.0	—	1.0	μA	*3
Output leakage current		ILO	VIN = VDD or VSS		-3.0	—	3.0	μA	*4
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C (Relative To VSS)	$V0_{IN}$ = 15.0 V	—	1	—	KΩ	SEGn COMn *5
				$V0_{IN}$ = 8.0 V	—	1.3	—		
Oscillator Frequency	Internal Oscillator	fOSC	1/68 duty	Ta = 25°C 31 PWM	—	5.39	12.02	kHz	*6
	External Input	fCL			—	167.09	372.62	kHz	OSC
	Frame frequency	fFRAME			Internal OSC: fFRAME = fOSC /(Duty+1) External OSC: fFRAME = fCL /[31*(Duty+1)]			Hz	

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Operating Voltage (1)	VDD VDD1	(Relative to VSS)	1.7	—	3.4	V	VSS*7
	Operating Voltage (2)	VDD2 VDD3 VDD4 VDD5	(Relative to VSS)	2.4	—	3.4	V	VSS
	Supply Step-up output voltage Circuit	$VLCD_{OUT}$	(Relative To VSS)	—	—	20	V	$VLCD_{OUT}$
	Voltage regulator Circuit Operating Voltage	$VLCD_{IN}$	(Relative To VSS)	—	—	20	V	$VLCD_{IN}$

Dynamic Consumption Current : During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used .

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern Normal(Bare die)	ISS	Bare Die, VDD = 2.8 V, Booster x 5 @ 1/9 bias,1/68 duty,Vop=11V	—	350	—	μA	*8
Power Down (Bare die)	ISS	Ta = 25°C	—	—	10	μA	

Notes to the DC characteristics

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load Internal clock.
2. Power-down mode. During power down all static currents are switched off.
3. If external VLCD, the display load current is not transmitted to I_{DD}.
4. VLCD external voltage applied to $VLCD_{IN}$ pin; $VLCD_{IN}$ disconnected from $VLCD_{OUT}$

References for items market with *

*1 The A0, D0 to D5, D6, D7, SI, SCL, E_RD, RW_WR, /CS, RST terminals.

*2 The D0 to D7.

*3 The A0, E_RD, RW_WR, /CS, RST terminals.

*4 Applies when the D0 to D5, D6, D7, SI, SCL, terminals are in a high impedance state.

*5 These are the resistance values for when a 0.2 x V0 voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range.
RON = (0.2 V0)/ ΔI (Where ΔI is the current that flows when 0.2 V0 is applied while the power supply is ON.)

*6 The relationship between the oscillator frequency and the frame rate frequency under CL dividing ratio setting = 00H.

*7 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*8 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.

12. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

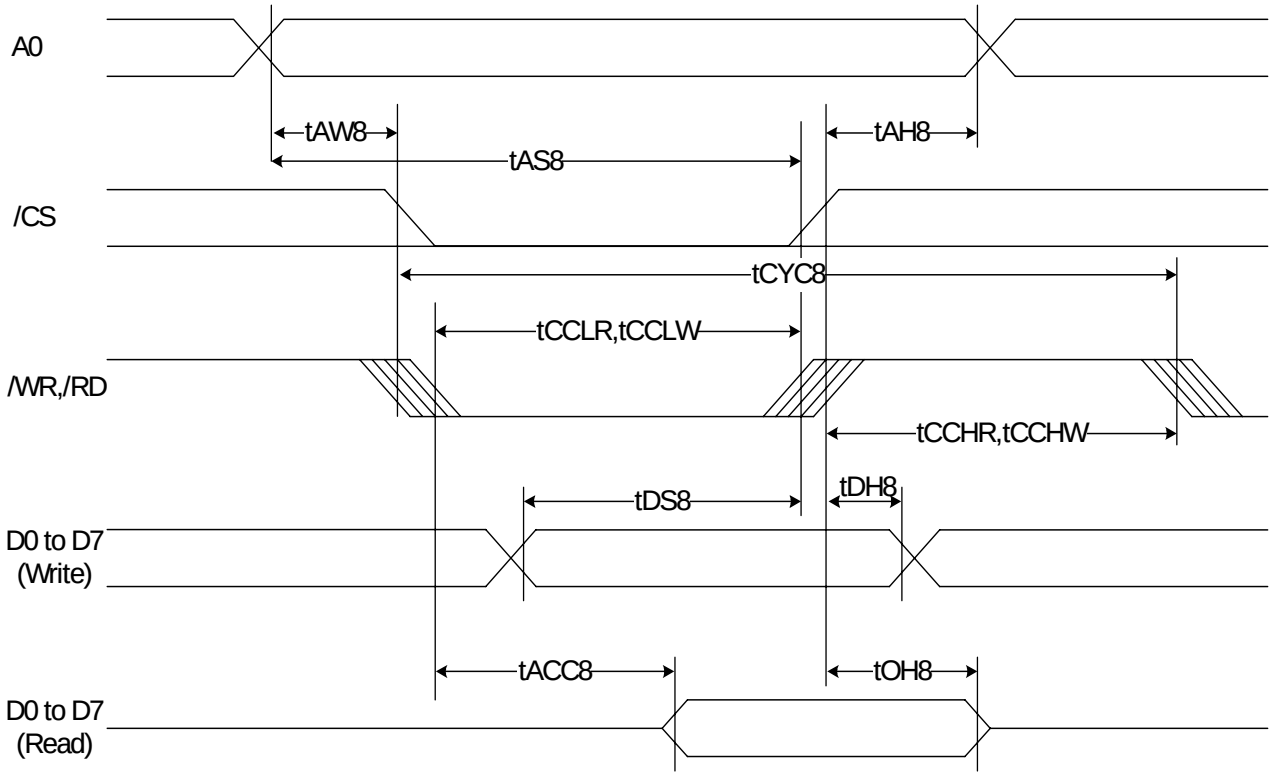


Figure 12.1

(V_{DD}=3.3V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAS8		60	—	
Address setup time		tAW8		0	—	
System cycle time (WRITE)	WR	tCYC8		180	—	
/WR L pulse width (WRITE)		tCCLW		60	—	
/WR H pulse width (WRITE)		tCCHW		120	—	
System cycle time (READ)	RD	tCYC8		200	—	
/RD L pulse width (READ)		tCCLR		80	—	
/RD H pulse width (READ)		tCCHR		120	—	
WRITE data setup time	D0 to D7	tDS8		60	—	
WRITE data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	—	60	

(V_{DD}=2.8V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAS8		80	—	
Address setup time		tAW8		0	—	
System cycle time (WRITE)	WR	tCYC8		220	—	
/WR L pulse width (WRITE)		tCCLW		80	—	
/WR H pulse width (WRITE)		tCCHW		140	—	
System cycle time (READ)	RD	tCYC8		280	—	
/RD L pulse width (READ)		tCCLR		100	—	
/RD H pulse width (READ)		tCCHR		180	—	
WRITE data setup time	D0 to D7	tDS8		80	—	
WRITE data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	75	
READ Output disable time		tOH8	CL = 100 pF	—	65	

(V_{DD}=1.8V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		10	—	ns
Address setup time		tAS8		180	—	
Address setup time		tAW8		30	—	
System cycle time (WRITE)	WR	tCYC8		430	—	
/WR L pulse width (WRITE)		tCCLW		150	—	
/WR H pulse width (WRITE)		tCCHW		280	—	
System cycle time (READ)	RD	tCYC8		450	—	
/RD L pulse width (READ)		tCCLR		190	—	
/RD H pulse width (READ)		tCCHR		230	—	
WRITE data setup time	D0 to D7	tDS8		150	—	
WRITE data hold time		tDH8		10	—	
READ access time		tACC8	CL = 100 pF	—	100	
READ Output disable time		tOH8	CL = 100 pF	—	80	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between /CS being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

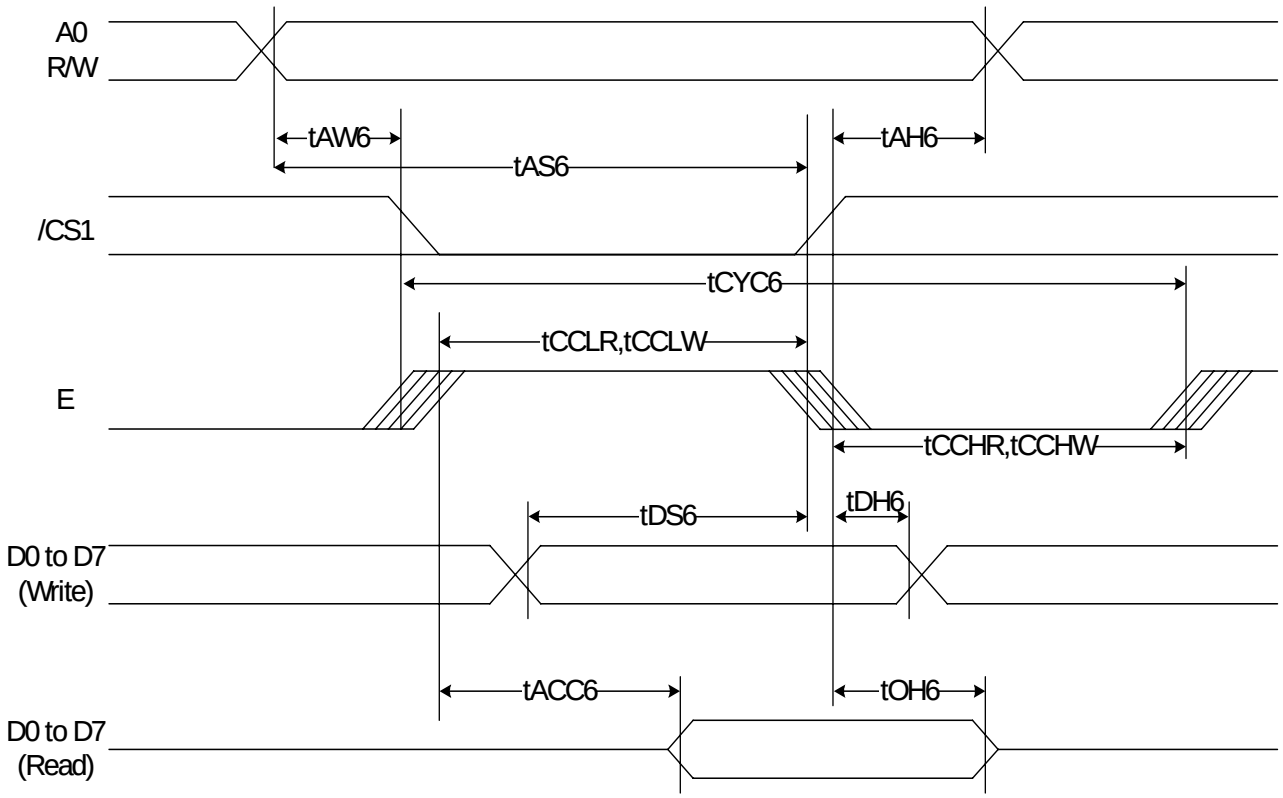


Figure 12.2

(V_{DD}=3.3V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAS6		60	—	
Address setup time		tAW6		0	—	
System cycle time (WRITE)	WR	tCYC6		180	—	
Enable L pulse width (WRITE)		tCCLW		120	—	
Enable H pulse width (WRITE)		tCCHW		60	—	
System cycle time (READ)	RD	tCYC6		200	—	
Enable L pulse width (READ)		tCCLR		120	—	
Enable H pulse width (READ)		tCCHR		80	—	
WRITE data setup time	D0 to D7	tDS6		60	—	
WRITE data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	—	60	

(V_{DD}=2.8V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAS6		80	—	
Address setup time		tAW6		0	—	
System cycle time (WRITE)	WR	tCYC6		220	—	
Enable L pulse width (WRITE)		tCCLW		140	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
System cycle time (READ)	RD	tCYC6		220	—	
Enable L pulse width (READ)		tCCLR		120	—	
Enable H pulse width (READ)		tCCHR		100	—	
WRITE data setup time	D0 to D7	tDS6		80	—	
WRITE data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	75	
READ Output disable time		tOH6	CL = 100 pF	—	65	

(V_{DD}=1.8V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		10	—	ns
Address setup time		tAS6		180	—	
Address setup time		tAW6		30	—	
System cycle time (WRITE)	WR	tCYC6		430	—	
Enable L pulse width (WRITE)		tCCLW		280	—	
Enable H pulse width (WRITE)		tCCHW		150	—	
System cycle time (READ)	RD	tCYC6		400	—	
Enable L pulse width (READ)		tCCLR		220	—	
Enable H pulse width (READ)		tCCHR		180	—	
WRITE data setup time	D0 to D7	tDS6		150	—	
WRITE data hold time		tDH6		10	—	
READ access time		tACC6	CL = 100 pF	—	100	
READ Output disable time		tOH6	CL = 100 pF	—	80	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between /CS being “L” and E.

Serial Interface Characteristics (For 4-Line Interface)

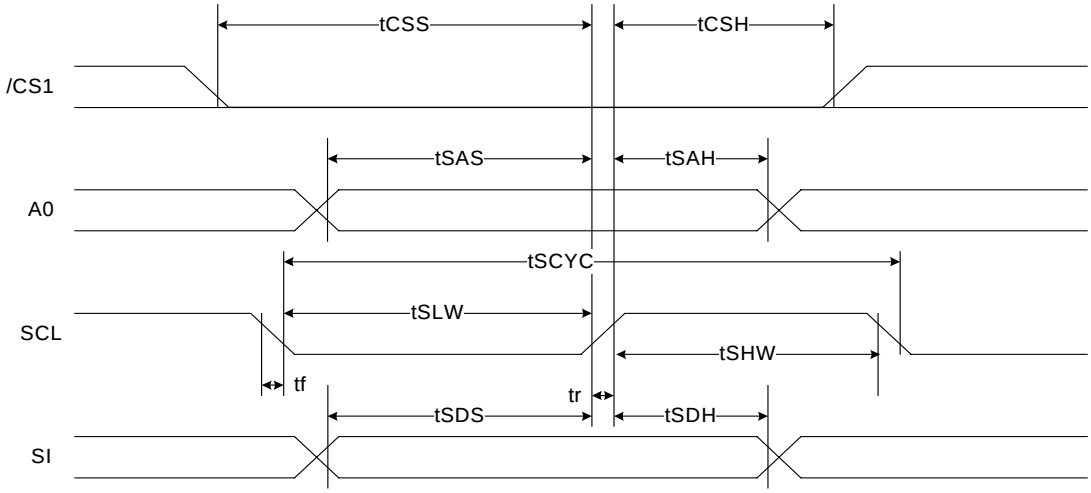


Fig 12.3

(V_{DD}=3.3V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		80	—	ns
SCL “H” pulse width		tSHW		40	—	
SCL “L” pulse width		tSLW		40	—	
Address setup time	A0	tSAS		10	—	
Address hold time		tSAH		10	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		30	—	
CS-SCL setup time	/CS	tCSS		20	—	
CS-SCL hold time		tCSH		30	—	

(V_{DD}=2.8V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		10	—	
Address hold time		tSAH		10	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		30	—	
CS-SCL setup time	/CS	tCSS		20	—	
CS-SCL hold time		tCSH		40	—	

(V_{DD}=1.8V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		180	—	ns
SCL “H” pulse width		tSHW		90	—	
SCL “L” pulse width		tSLW		90	—	
Address setup time	A0	tSAS		10	—	
Address hold time		tSAH		50	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		45	—	
CS-SCL time	/CS	tCSS		10	—	
CS-SCL time		tCSH		80	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

Serial Interface Characteristics (For 3-Line Interface)

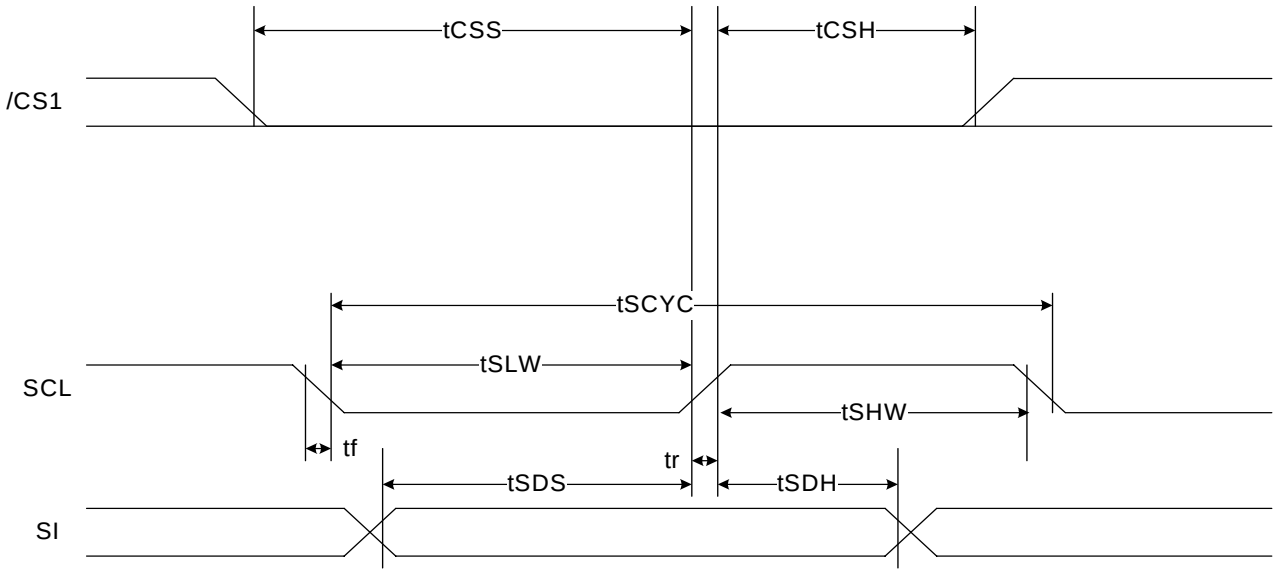


Fig 12.4

(V_{DD}=3.3V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		80	—	ns
SCL “H” pulse width		tSHW		40	—	
SCL “L” pulse width		tSLW		40	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		30	—	
CS-SCL setup time	/CS	tCSS		20	—	
CS-SCL hold time		tCSH		50	—	

(V_{DD}=2.8V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		30	—	
CS-SCL time	/CS	tCSS		20	—	
CS-SCL time		tCSH		50	—	

(V_{DD}=1.8V,Ta= –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial clock period	SCL	tSCYC		180	—	ns
SCL “H” pulse width		tSHW		90	—	
SCL “L” pulse width		tSLW		90	—	
Data setup time	SI	tSDS		10	—	
Data hold time		tSDH		45	—	
CS-SCL time	/CS	tCSS		10	—	
CS-SCL time		tCSH		80	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

13. RESET TIMING

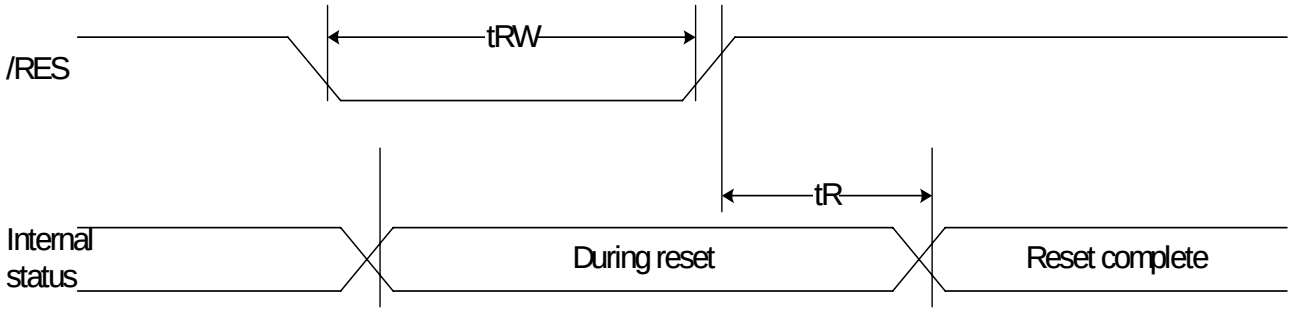


Fig 13.1

(VDD = 3.3V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	us
Reset “L” pulse width	RESB	tRW		1.2	—	—	us

(VDD = 2.8V , Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	us
Reset “L” pulse width	RESB	tRW		1.5	—	—	us

(VDD = 1.8V , Ta = –30 to 85°C)

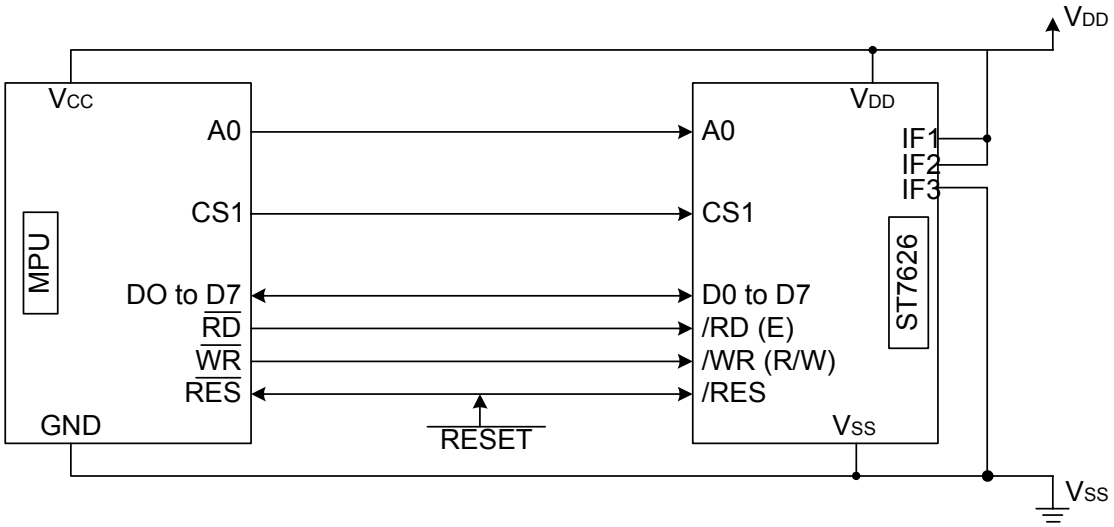
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2	us
Reset “L” pulse width	RESB	tRW		2	—	—	us

14. THE MPU INTERFACE (REFERENCE EXAMPLES)

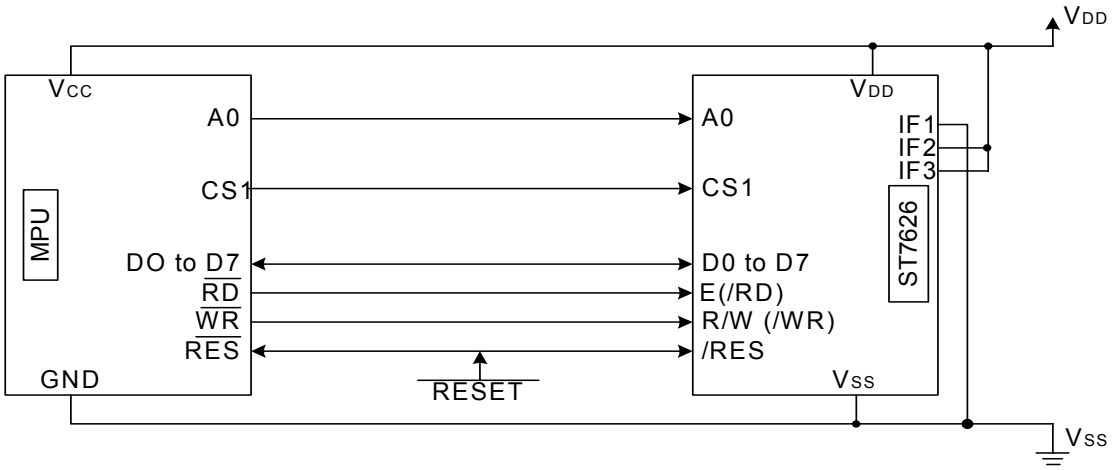
The ST7626 Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7626 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7626 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

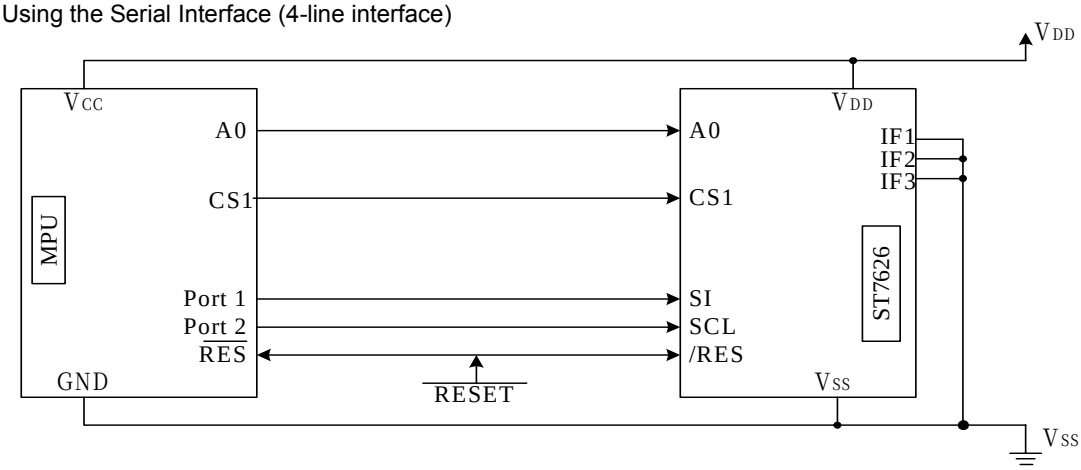
(1) 8080 Series MPUs



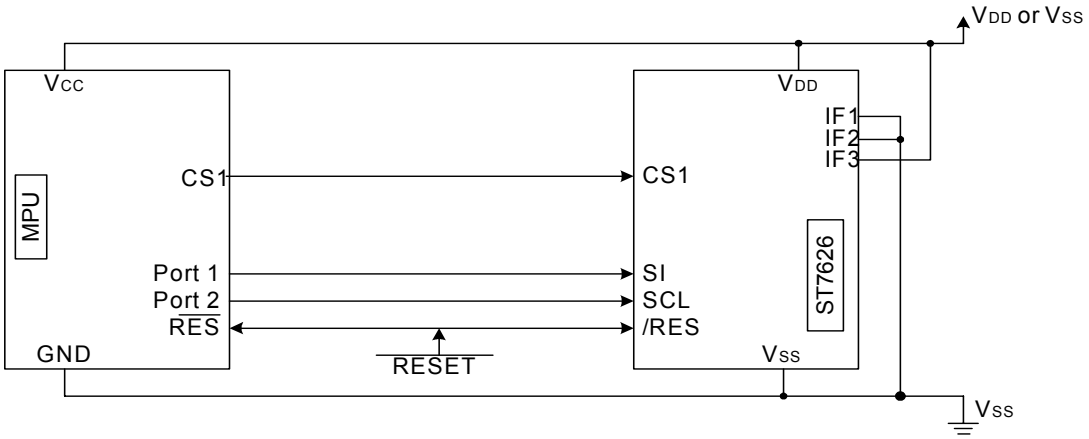
(2) 6800 Series MPUs



(3) Using the Serial Interface (4-line interface)

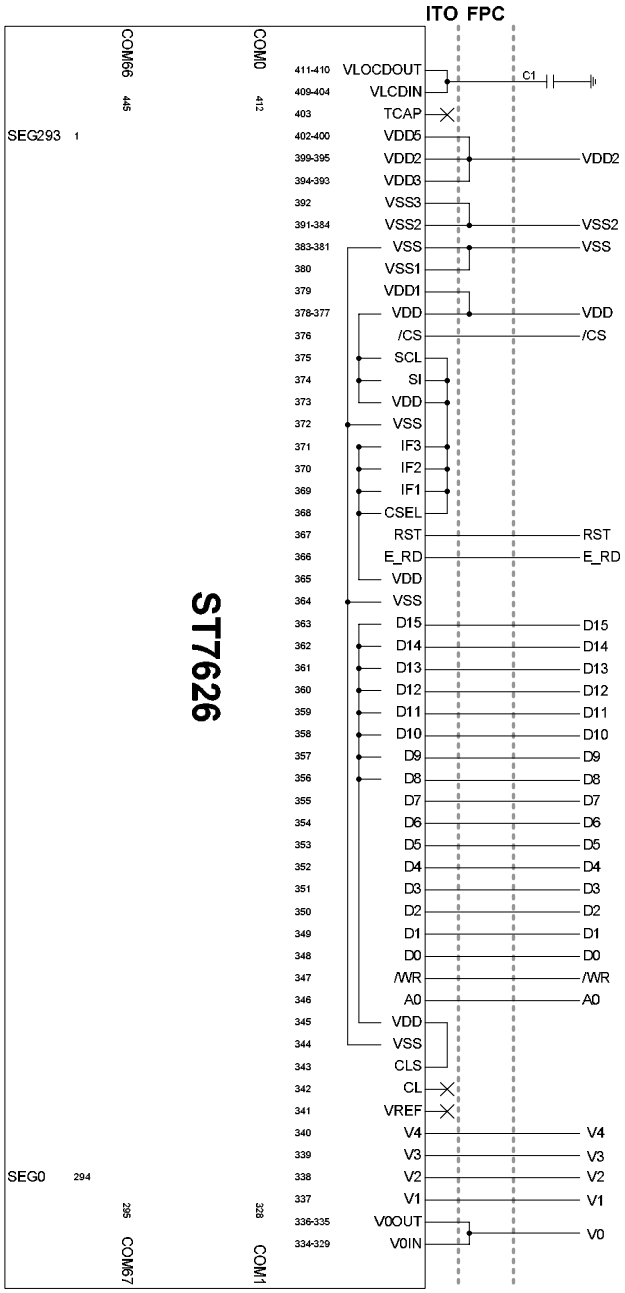


(4) Using the Serial Interface (3-line interface)



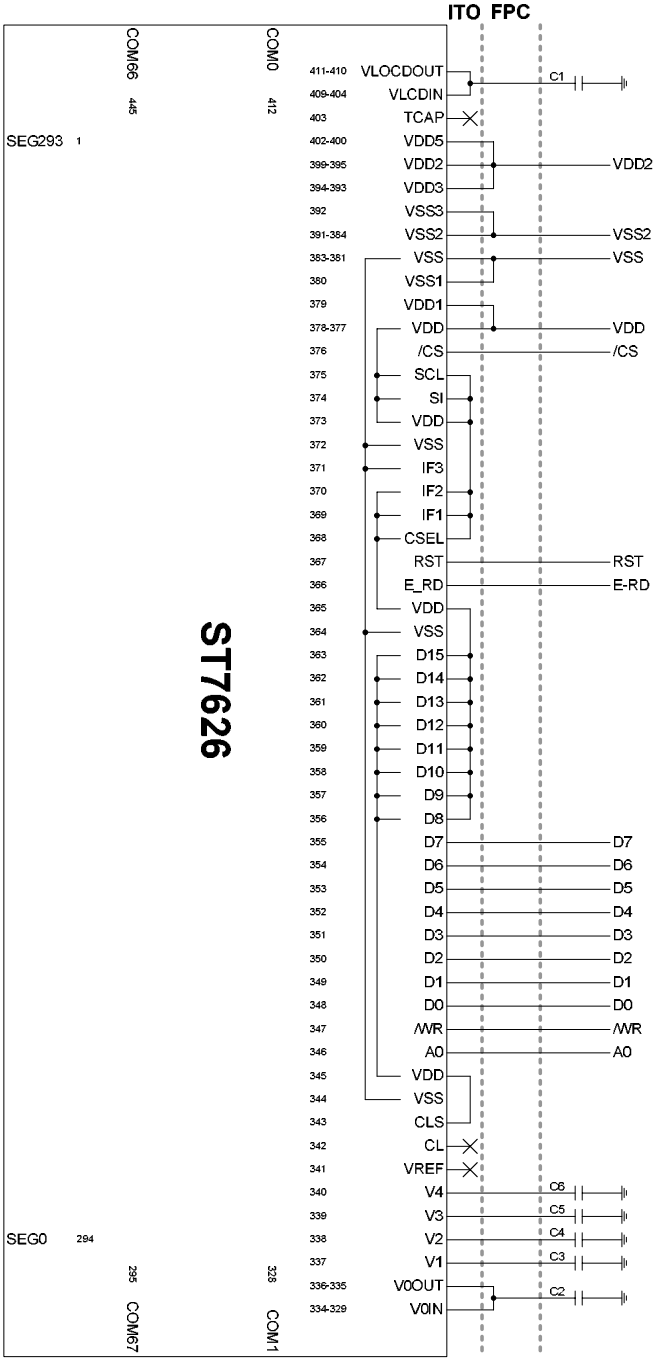
Application Circuits

(A) 80 Series 16-bit Parallel Interface:



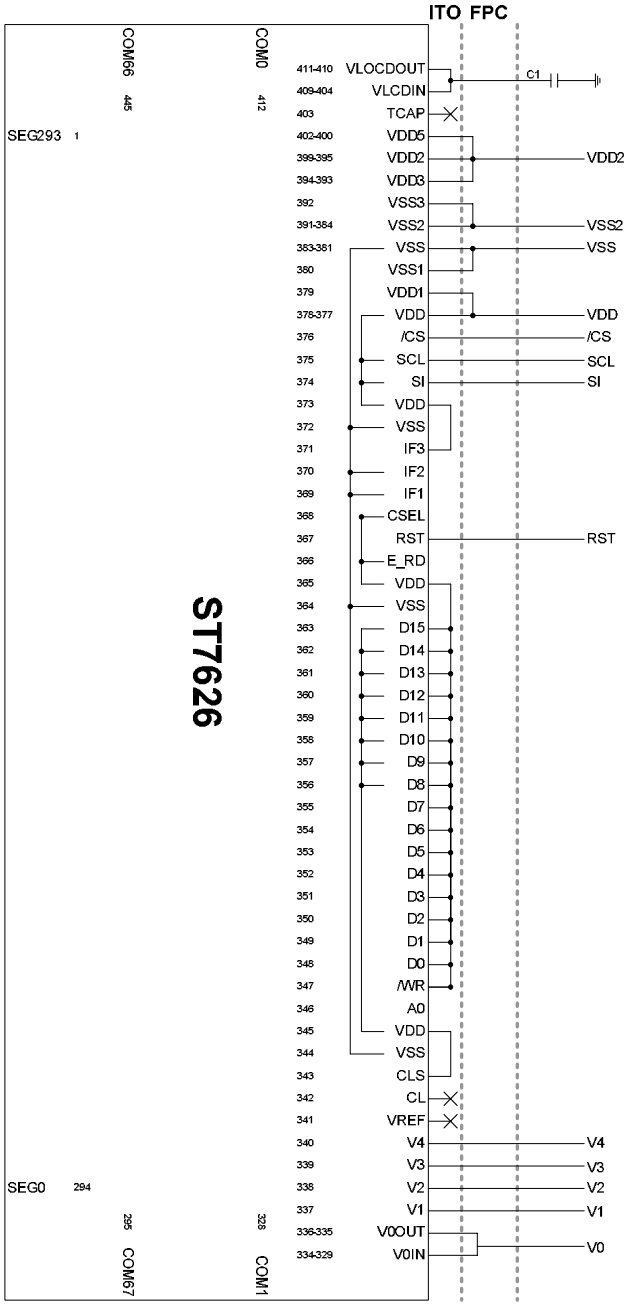
Interface : 8080series-16bits
VDD1(VDD,VDD1)=1.8~3.3V
VDD2(VDD2~VDD5)=2.4~3.3V
CSEL=H (Interlace Mode)
IF1=H;IF2=H;IF3=H
C0: 1.0~2.2uF/25V

(B) 80 Series 8-bit Parallel Interface:



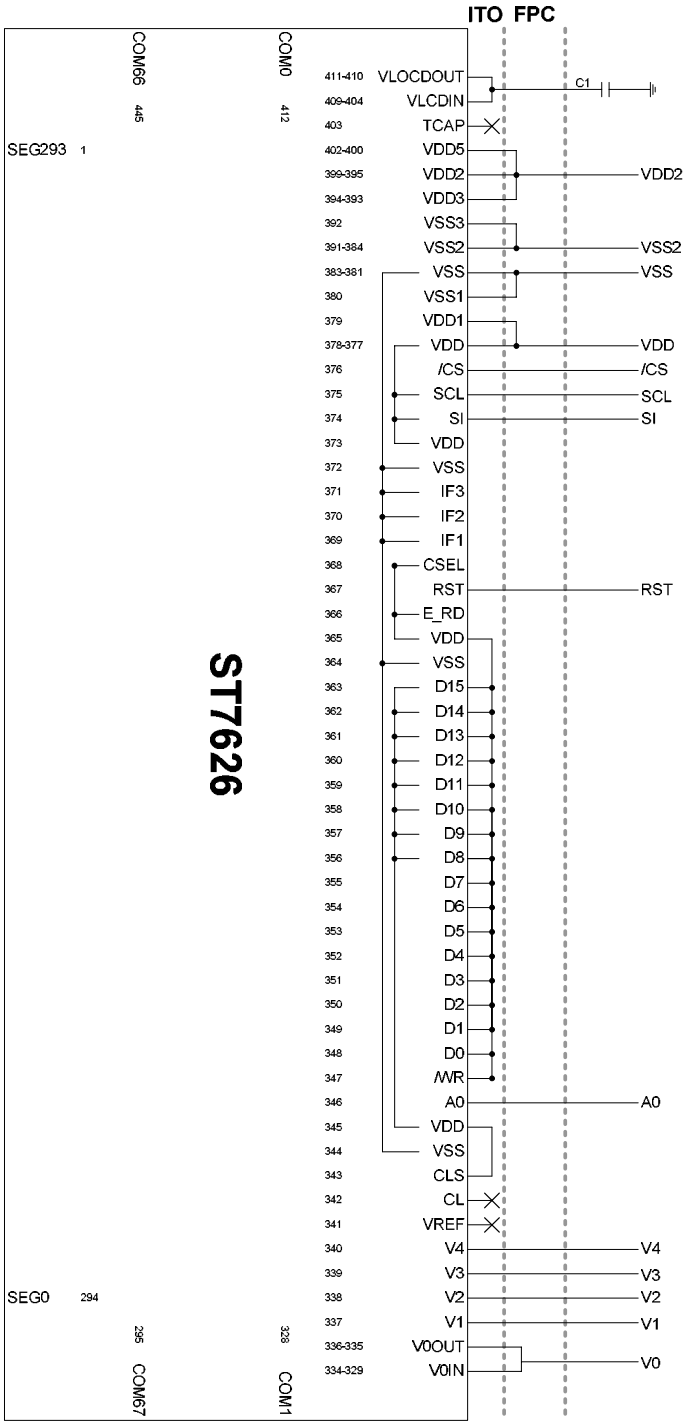
Interface : 8080series-8bits
VDD1(VDD,VDD1)=1.8~3.3V
VDD2(VDD2~VDD5)=2.4~3.3V
CSEL=H (Interlace Mode)
IF1=H;IF2=H;IF3=L
C0: 1.0~2.2uF/25V

(C) 3 Line Serial Peripheral Interface:



Interface : 9-bit Serial(3-Line)
VDD1(VDD,VDD1)=1.8~3.3V
VDD2(VDD2~VDD5)=2.4~3.3V
CSEL=H (Interlace Mode)
IF1=L;IF2=L;IF3=H
C0: 1.0~2.2uF/25V

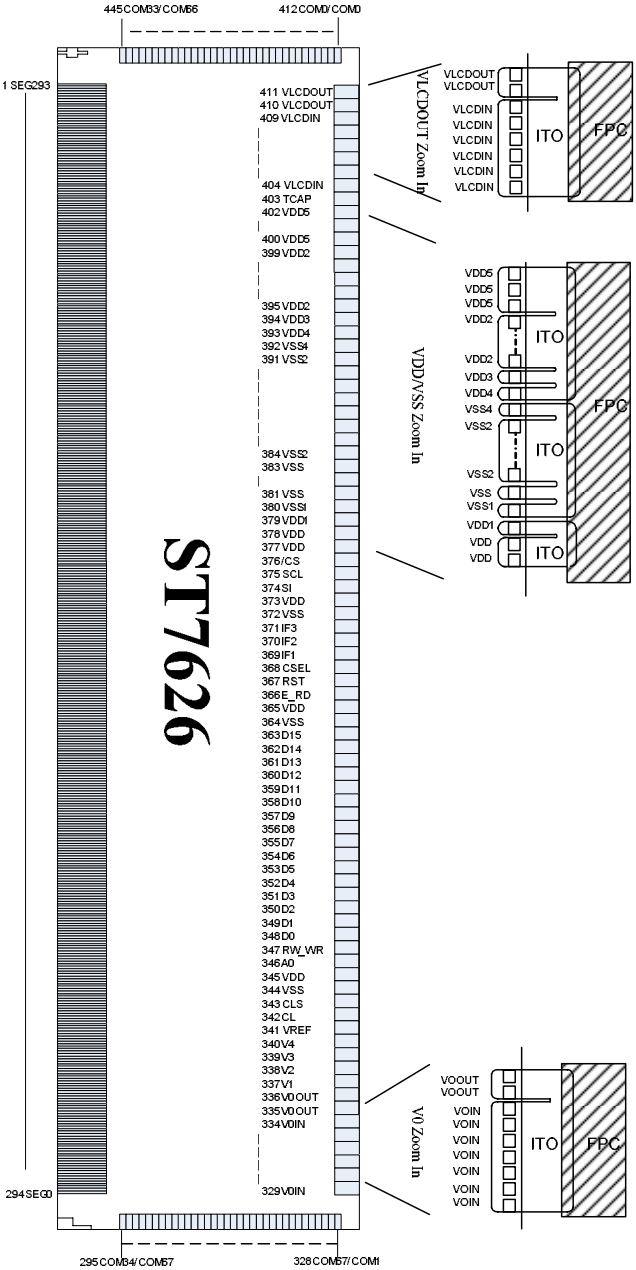
(D) 4 Line Serial Peripheral Interface:



Interface : 8-bit Serial(4-Line)
VDD1(VDD,VDD1)=1.8~3.3V
VDD2(VDD2~VDD5)=2.4~3.3V
CSEL=H (Interlace Mode)
IF1=L;IF2=L;IF3=L
C0: 1.0~2.2uF/25V

16. Application Note of VLCD and Vop (V0) ITO Layout

When using internal voltage generator, VLCDIN、VLCDOUT must be connected together. V0IN and V0OUT must be connected together too. In the following is the ITO layout for VLCDIN、VLCDOUT、V0IN and V0OUT individually. Please follow the way as below for these two LCD power voltages.



NOTE:

Microprocessor interfece pins should not be floating in any operation mode.

ST7626 Serial Specification Revision History		
Version	**Date**	**Description**
0.x	--	Preliminary version
1.0	2006/04/10	First issue.
1.1	2006/5/23	Change the limitation voltage (P77): VDD, VDD1=1.7V~3.4V VDD2,VDD3, VDD4, VDD5=2.4V~3.4V
1.2	2006/7/23	Change write EEPROM example program (P.43) Add microprossoer notice item (P.13,P93)
1.3	2006/09/25	Add Vref Pin notice item (P.14,P11) Modifty Application circuit vref Pin section (P89, P90,P91,P92)
1.4	2006/10/31	Modifty page 67: ST7626 initial code example program
1.5	2007/01/20	Modifty page application circuit : page 89~page 93