Sitronix

ST7632

4K Color Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7632 is a driver & controller LSI for 4K color graphic dot-matrix liquid crystal display systems. It generates 396 Segment and 132 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI) or 8-bit/16-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

–396 segment outputs / 132 common outputs

Applicable Duty Ratios

– Various partial display

– Partial window moving & data scrolling

On-chip Display Data RAM

– Capacity: 396 × 132 × 4 =209,088 bits

– 256 colors (RGB)=(332) mode

–4K colors (RGB)=(444) mode

–Dithered 65K colors (RGB)=(565) mode

–Dithered 262K colors (RGB)=(666) mode

–Dithered 16M colors (RGB)=(888) mode

Microprocessor Interface

– 8/16-bit parallel bi-directional interface with 6800-series or 8080-series

– 4-line serial interface (4-line-SIF)

– 3-line serial interface (3-line-SIF)

On-chip Low Power Analog Circuit

– On-chip oscillator circuit

– Voltage converter (x2, x3, x4, x5, x6, x7, x8)

– Voltage regulator

– On-chip electronic contrast control function

– Voltage follower (LCD bias: 1/5 to 1/12)

Operating Voltage Range

– Supply voltage (VDD, VDD1): 2.0 to 3.3V

(VDD2, VDD3, VDD4, VDD5): 2.6 to 3.3V

V3 & V4 must large than VDD5

– LCD driving voltage (VLCD = V0 - VSS): 3.76 to 18.0 V

– Suggest Vop range=12V~14V,LCD bias=1/12.

LCD driving voltage (EEPROM)

– To store contrast adjustment value for better display

Package Type

– Application for COG

Par no.	Equipment Type	Thermal Gradient
ST7632	Internal Power Supply	-0.125(+-10%)%/℃

3. ST7632 Pad Arrangement (COG)

Chip Size: 19,550 um × 1,473 um

Bump Pitch: PAD NO 1 ~ 496, 632~663: 40 um (COM/SEG), PAD NO 497 ~ 631: 110 um (I/O)

Bump size:

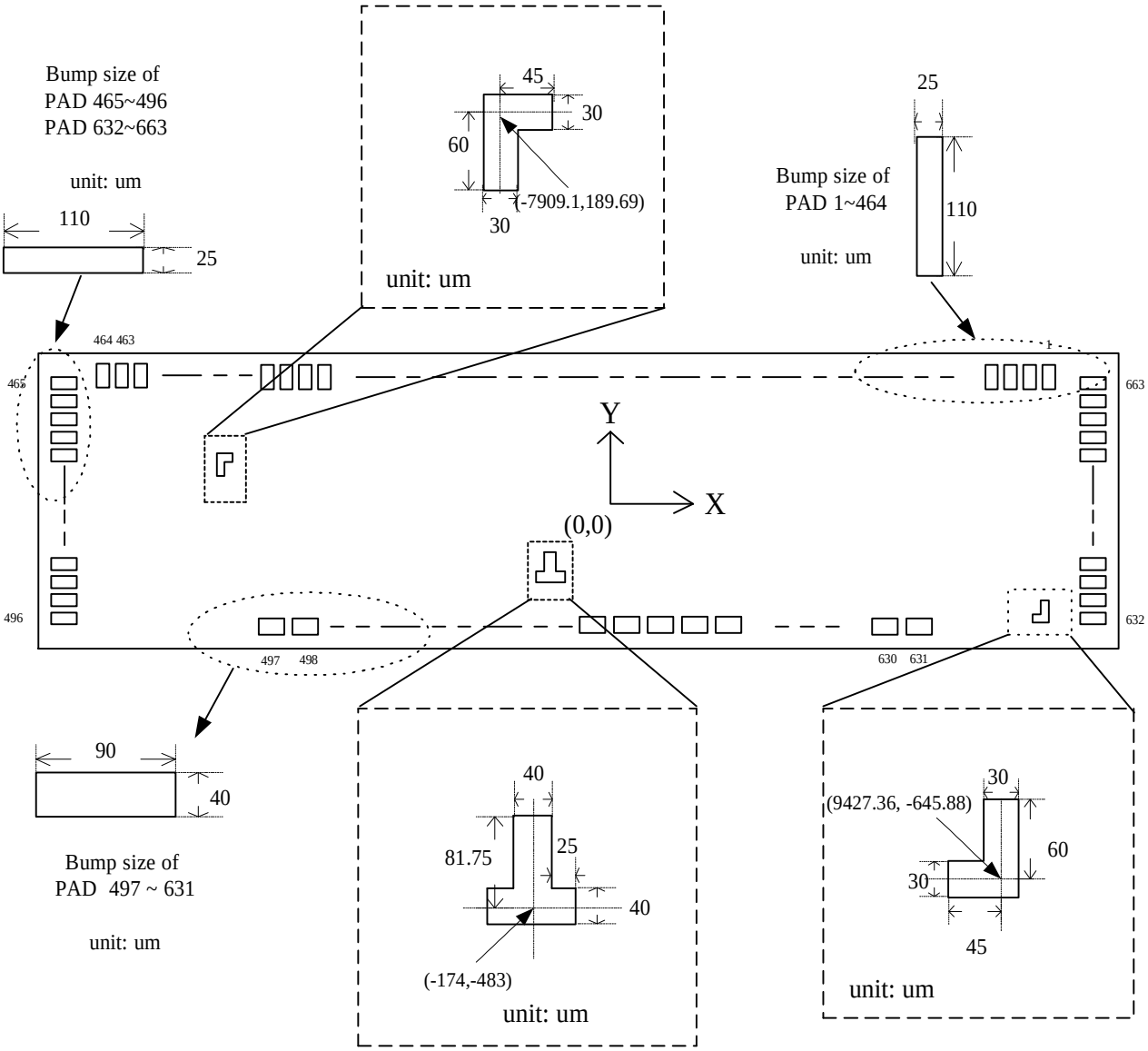
PAD NO.1~464: 25(x)um X 110(y)um

PAD No.465~496, 632~663: 110(x)um X 25(y)um

PAD N0. 497~631: 90(x)um X 40(y)um

Bump Height: 17um

Chip Thickness: 635 um



4. Pad Center Coordinates

PAD No.	PIN Name	X	Y
001	COM[32]	9384	625
002	COM[33]	9344	625
003	COM[34]	9304	625
004	COM[35]	9264	625
005	COM[36]	9224	625
006	COM[37]	9184	625
007	COM[38]	9144	625
008	COM[39]	9104	625
009	COM[40]	9064	625
010	COM[41]	9024	625
011	COM[42]	8984	625
012	COM[43]	8944	625
013	COM[44]	8904	625
014	COM[45]	8864	625
015	COM[46]	8824	625
016	COM[47]	8784	625
017	COM[48]	8744	625
018	COM[49]	8704	625
019	COM[50]	8664	625
020	COM[51]	8624	625
021	COM[52]	8584	625
022	COM[53]	8544	625
023	COM[54]	8504	625
024	COM[55]	8464	625
025	COM[56]	8424	625
026	COM[57]	8384	625
027	COM[58]	8344	625
028	COM[59]	8304	625
029	COM[60]	8264	625
030	COM[61]	8224	625
031	COM[62]	8184	625
032	COM[63]	8144	625
033	COM[64]	8104	625
034	COM[65]	8064	625
035	SEG[395]	7922	625

PAD No.	PIN Name	X	Y
036	SEG[394]	7882	625
037	SEG[393]	7842	625
038	SEG[392]	7802	625
039	SEG[391]	7762	625
040	SEG[390]	7722	625
041	SEG[389]	7682	625
042	SEG[388]	7642	625
043	SEG[387]	7602	625
044	SEG[386]	7562	625
045	SEG[385]	7522	625
046	SEG[384]	7482	625
047	SEG[383]	7442	625
048	SEG[382]	7402	625
049	SEG[381]	7362	625
050	SEG[380]	7322	625
051	SEG[379]	7282	625
052	SEG[378]	7242	625
053	SEG[377]	7202	625
054	SEG[376]	7162	625
055	SEG[375]	7122	625
056	SEG[374]	7082	625
057	SEG[373]	7042	625
058	SEG[372]	7002	625
059	SEG[371]	6962	625
060	SEG[370]	6922	625
061	SEG[369]	6882	625
062	SEG[368]	6842	625
063	SEG[367]	6802	625
064	SEG[366]	6762	625
065	SEG[365]	6722	625
066	SEG[364]	6682	625
067	SEG[363]	6642	625
068	SEG[362]	6602	625
069	SEG[361]	6562	625
070	SEG[360]	6522	625

PAD No.	PIN Name	X	Y
071	SEG[359]	6482	625
072	SEG[358]	6442	625
073	SEG[357]	6402	625
074	SEG[356]	6362	625
075	SEG[355]	6322	625
076	SEG[354]	6282	625
077	SEG[353]	6242	625
078	SEG[352]	6202	625
079	SEG[351]	6162	625
080	SEG[350]	6122	625
081	SEG[349]	6082	625
082	SEG[348]	6042	625
083	SEG[347]	6002	625
084	SEG[346]	5962	625
085	SEG[345]	5922	625
086	SEG[344]	5882	625
087	SEG[343]	5842	625
088	SEG[342]	5802	625
089	SEG[341]	5762	625
090	SEG[340]	5722	625
091	SEG[339]	5682	625
092	SEG[338]	5642	625
093	SEG[337]	5602	625
094	SEG[336]	5562	625
095	SEG[335]	5522	625
096	SEG[334]	5482	625
097	SEG[333]	5442	625
098	SEG[332]	5402	625
099	SEG[331]	5362	625
100	SEG[330]	5322	625
101	SEG[329]	5282	625
102	SEG[328]	5242	625
103	SEG[327]	5202	625
104	SEG[326]	5162	625
105	SEG[325]	5122	625
106	SEG[324]	5082	625

PAD No.	PIN Name	X	Y
107	SEG[323]	5042	625
108	SEG[322]	5002	625
109	SEG[321]	4962	625
110	SEG[320]	4922	625
111	SEG[319]	4882	625
112	SEG[318]	4842	625
113	SEG[317]	4802	625
114	SEG[316]	4762	625
115	SEG[315]	4722	625
116	SEG[314]	4682	625
117	SEG[313]	4642	625
118	SEG[312]	4602	625
119	SEG[311]	4562	625
120	SEG[310]	4522	625
121	SEG[309]	4482	625
122	SEG[308]	4442	625
123	SEG[307]	4402	625
124	SEG[306]	4362	625
125	SEG[305]	4322	625
126	SEG[304]	4282	625
127	SEG[303]	4242	625
128	SEG[302]	4202	625
129	SEG[301]	4162	625
130	SEG[300]	4122	625
131	SEG[299]	4082	625
132	SEG[298]	4042	625
133	SEG[297]	4002	625
134	SEG[296]	3962	625
135	SEG[295]	3922	625
136	SEG[294]	3882	625
137	SEG[293]	3842	625
138	SEG[292]	3802	625
139	SEG[291]	3762	625
140	SEG[290]	3722	625
141	SEG[289]	3682	625
142	SEG[288]	3642	625

PAD No.	PIN Name	X	Y
143	SEG[287]	3602	625
144	SEG[286]	3562	625
145	SEG[285]	3522	625
146	SEG[284]	3482	625
147	SEG[283]	3442	625
148	SEG[282]	3402	625
149	SEG[281]	3362	625
150	SEG[280]	3322	625
151	SEG[279]	3282	625
152	SEG[278]	3242	625
153	SEG[277]	3202	625
154	SEG[276]	3162	625
155	SEG[275]	3122	625
156	SEG[274]	3082	625
157	SEG[273]	3042	625
158	SEG[272]	3002	625
159	SEG[271]	2962	625
160	SEG[270]	2922	625
161	SEG[269]	2882	625
162	SEG[268]	2842	625
163	SEG[267]	2802	625
164	SEG[266]	2762	625
165	SEG[265]	2722	625
166	SEG[264]	2682	625
167	SEG[263]	2642	625
168	SEG[262]	2602	625
169	SEG[261]	2562	625
170	SEG[260]	2522	625
171	SEG[259]	2482	625
172	SEG[258]	2442	625
173	SEG[257]	2402	625
174	SEG[256]	2362	625
175	SEG[255]	2322	625
176	SEG[254]	2282	625
177	SEG[253]	2242	625
178	SEG[252]	2202	625

PAD No.	PIN Name	X	Y
179	SEG[251]	2162	625
180	SEG[250]	2122	625
181	SEG[249]	2082	625
182	SEG[248]	2042	625
183	SEG[247]	2002	625
184	SEG[246]	1962	625
185	SEG[245]	1922	625
186	SEG[244]	1882	625
187	SEG[243]	1842	625
188	SEG[242]	1802	625
189	SEG[241]	1762	625
190	SEG[240]	1722	625
191	SEG[239]	1682	625
192	SEG[238]	1642	625
193	SEG[237]	1602	625
194	SEG[236]	1562	625
195	SEG[235]	1522	625
196	SEG[234]	1482	625
197	SEG[233]	1442	625
198	SEG[232]	1402	625
199	SEG[231]	1362	625
200	SEG[230]	1322	625
201	SEG[229]	1282	625
202	SEG[228]	1242	625
203	SEG[227]	1202	625
204	SEG[226]	1162	625
205	SEG[225]	1122	625
206	SEG[224]	1082	625
207	SEG[223]	1042	625
208	SEG[222]	1002	625
209	SEG[221]	962	625
210	SEG[220]	922	625
211	SEG[219]	882	625
212	SEG[218]	842	625
213	SEG[217]	802	625
214	SEG[216]	762	625

PAD No.	PIN Name	X	Y
215	SEG[215]	722	625
216	SEG[214]	682	625
217	SEG[213]	642	625
218	SEG[212]	602	625
219	SEG[211]	562	625
220	SEG[210]	522	625
221	SEG[209]	482	625
222	SEG[208]	442	625
223	SEG[207]	402	625
224	SEG[206]	362	625
225	SEG[205]	322	625
226	SEG[204]	282	625
227	SEG[203]	242	625
228	SEG[202]	202	625
229	SEG[201]	162	625
230	SEG[200]	122	625
231	SEG[199]	82	625
232	SEG[198]	42	625
233	SEG[197]	2	625
234	SEG[196]	-38	625
235	SEG[195]	-78	625
236	SEG[194]	-118	625
237	SEG[193]	-158	625
238	SEG[192]	-198	625
239	SEG[191]	-238	625
240	SEG[190]	-278	625
241	SEG[189]	-318	625
242	SEG[188]	-358	625
243	SEG[187]	-398	625
244	SEG[186]	-438	625
245	SEG[185]	-478	625
246	SEG[184]	-518	625
247	SEG[183]	-558	625
248	SEG[182]	-598	625
249	SEG[181]	-638	625
250	SEG[180]	-678	625

PAD No.	PIN Name	X	Y
251	SEG[179]	-718	625
252	SEG[178]	-758	625
253	SEG[177]	-798	625
254	SEG[176]	-838	625
255	SEG[175]	-878	625
256	SEG[174]	-918	625
257	SEG[173]	-958	625
258	SEG[172]	-998	625
259	SEG[171]	-1038	625
260	SEG[170]	-1078	625
261	SEG[169]	-1118	625
262	SEG[168]	-1158	625
263	SEG[167]	-1198	625
264	SEG[166]	-1238	625
265	SEG[165]	-1278	625
266	SEG[164]	-1318	625
267	SEG[163]	-1358	625
268	SEG[162]	-1398	625
269	SEG[161]	-1438	625
270	SEG[160]	-1478	625
271	SEG[159]	-1518	625
272	SEG[158]	-1558	625
273	SEG[157]	-1598	625
274	SEG[156]	-1638	625
275	SEG[155]	-1678	625
276	SEG[154]	-1718	625
277	SEG[153]	-1758	625
278	SEG[152]	-1798	625
279	SEG[151]	-1838	625
280	SEG[150]	-1878	625
281	SEG[149]	-1918	625
282	SEG[148]	-1958	625
283	SEG[147]	-1998	625
284	SEG[146]	-2038	625
285	SEG[145]	-2078	625
286	SEG[144]	-2118	625

PAD No.	PIN Name	X	Y
287	SEG[143]	-2158	625
288	SEG[142]	-2198	625
289	SEG[141]	-2238	625
290	SEG[140]	-2278	625
291	SEG[139]	-2318	625
292	SEG[138]	-2358	625
293	SEG[137]	-2398	625
294	SEG[136]	-2438	625
295	SEG[135]	-2478	625
296	SEG[134]	-2518	625
297	SEG[133]	-2558	625
298	SEG[132]	-2598	625
299	SEG[131]	-2638	625
300	SEG[130]	-2678	625
301	SEG[129]	-2718	625
302	SEG[128]	-2758	625
303	SEG[127]	-2798	625
304	SEG[126]	-2838	625
305	SEG[125]	-2878	625
306	SEG[124]	-2918	625
307	SEG[123]	-2958	625
308	SEG[122]	-2998	625
309	SEG[121]	-3038	625
310	SEG[120]	-3078	625
311	SEG[119]	-3118	625
312	SEG[118]	-3158	625
313	SEG[117]	-3198	625
314	SEG[116]	-3238	625
315	SEG[115]	-3278	625
316	SEG[114]	-3318	625
317	SEG[113]	-3358	625
318	SEG[112]	-3398	625
319	SEG[111]	-3438	625
320	SEG[110]	-3478	625
321	SEG[109]	-3518	625
322	SEG[108]	-3558	625

PAD No.	PIN Name	X	Y
323	SEG[107]	-3598	625
324	SEG[106]	-3638	625
325	SEG[105]	-3678	625
326	SEG[104]	-3718	625
327	SEG[103]	-3758	625
328	SEG[102]	-3798	625
329	SEG[101]	-3838	625
330	SEG[100]	-3878	625
331	SEG[99]	-3918	625
332	SEG[98]	-3958	625
333	SEG[97]	-3998	625
334	SEG[96]	-4038	625
335	SEG[95]	-4078	625
336	SEG[94]	-4118	625
337	SEG[93]	-4158	625
338	SEG[92]	-4198	625
339	SEG[91]	-4238	625
340	SEG[90]	-4278	625
341	SEG[89]	-4318	625
342	SEG[88]	-4358	625
343	SEG[87]	-4398	625
344	SEG[86]	-4438	625
345	SEG[85]	-4478	625
346	SEG[84]	-4518	625
347	SEG[83]	-4558	625
348	SEG[82]	-4598	625
349	SEG[81]	-4638	625
350	SEG[80]	-4678	625
351	SEG[79]	-4718	625
352	SEG[78]	-4758	625
353	SEG[77]	-4798	625
354	SEG[76]	-4838	625
355	SEG[75]	-4878	625
356	SEG[74]	-4918	625
357	SEG[73]	-4958	625
358	SEG[72]	-4998	625

PAD No.	PIN Name	X	Y
359	SEG[71]	-5038	625
360	SEG[70]	-5078	625
361	SEG[69]	-5118	625
362	SEG[68]	-5158	625
363	SEG[67]	-5198	625
364	SEG[66]	-5238	625
365	SEG[65]	-5278	625
366	SEG[64]	-5318	625
367	SEG[63]	-5358	625
368	SEG[62]	-5398	625
369	SEG[61]	-5438	625
370	SEG[60]	-5478	625
371	SEG[59]	-5518	625
372	SEG[58]	-5558	625
373	SEG[57]	-5598	625
374	SEG[56]	-5638	625
375	SEG[55]	-5678	625
376	SEG[54]	-5718	625
377	SEG[53]	-5758	625
378	SEG[52]	-5798	625
379	SEG[51]	-5838	625
380	SEG[50]	-5878	625
381	SEG[49]	-5918	625
382	SEG[48]	-5958	625
383	SEG[47]	-5998	625
384	SEG[46]	-6038	625
385	SEG[45]	-6078	625
386	SEG[44]	-6118	625
387	SEG[43]	-6158	625
388	SEG[42]	-6198	625
389	SEG[41]	-6238	625
390	SEG[40]	-6278	625
391	SEG[39]	-6318	625
392	SEG[38]	-6358	625
393	SEG[37]	-6398	625
394	SEG[36]	-6438	625

PAD No.	PIN Name	X	Y
395	SEG[35]	-6478	625
396	SEG[34]	-6518	625
397	SEG[33]	-6558	625
398	SEG[32]	-6598	625
399	SEG[31]	-6638	625
400	SEG[30]	-6678	625
401	SEG[29]	-6718	625
402	SEG[28]	-6758	625
403	SEG[27]	-6798	625
404	SEG[26]	-6838	625
405	SEG[25]	-6878	625
406	SEG[24]	-6918	625
407	SEG[23]	-6958	625
408	SEG[22]	-6998	625
409	SEG[21]	-7038	625
410	SEG[20]	-7078	625
411	SEG[19]	-7118	625
412	SEG[18]	-7158	625
413	SEG[17]	-7198	625
414	SEG[16]	-7238	625
415	SEG[15]	-7278	625
416	SEG[14]	-7318	625
417	SEG[13]	-7358	625
418	SEG[12]	-7398	625
419	SEG[11]	-7438	625
420	SEG[10]	-7478	625
421	SEG[9]	-7518	625
422	SEG[8]	-7558	625
423	SEG[7]	-7598	625
424	SEG[6]	-7638	625
425	SEG[5]	-7678	625
426	SEG[4]	-7718	625
427	SEG[3]	-7758	625
428	SEG[2]	-7798	625
429	SEG[1]	-7838	625
430	SEG[0]	-7878	625

PAD No.	PIN Name	X	Y
431	COM[66]	-8020	625
432	COM[67]	-8060	625
433	COM[68]	-8100	625
434	COM[69]	-8140	625
435	COM[70]	-8180	625
436	COM[71]	-8220	625
437	COM[72]	-8260	625
438	COM[73]	-8300	625
439	COM[74]	-8340	625
440	COM[75]	-8380	625
441	COM[76]	-8420	625
442	COM[77]	-8460	625
443	COM[78]	-8500	625
444	COM[79]	-8540	625
445	COM[80]	-8580	625
446	COM[81]	-8620	625
447	COM[82]	-8660	625
448	COM[83]	-8700	625
449	COM[84]	-8740	625
450	COM[85]	-8780	625
451	COM[86]	-8820	625
452	COM[87]	-8860	625
453	COM[88]	-8900	625
454	COM[89]	-8940	625
455	COM[90]	-8980	625
456	COM[91]	-9020	625
457	COM[92]	-9060	625
458	COM[93]	-9100	625
459	COM[94]	-9140	625
460	COM[95]	-9180	625
461	COM[96]	-9220	625
462	COM[97]	-9260	625
463	COM[98]	-9300	625
464	COM[99]	-9340	625
465	COM[100]	-9664	606
466	COM[101]	-9664	566

PAD No.	PIN Name	X	Y
467	COM[102]	-9664	526
468	COM[103]	-9664	486
469	COM[104]	-9664	446
470	COM[105]	-9664	406
471	COM[106]	-9664	366
472	COM[107]	-9664	326
473	COM[108]	-9664	286
474	COM[109]	-9664	246
475	COM[110]	-9664	206
476	COM[111]	-9664	166
477	COM[112]	-9664	126
478	COM[113]	-9664	86
479	COM[114]	-9664	46
480	COM[115]	-9664	6
481	COM[116]	-9664	-34
482	COM[117]	-9664	-74
483	COM[118]	-9664	-114
484	COM[119]	-9664	-154
485	COM[120]	-9664	-194
486	COM[121]	-9664	-234
487	COM[122]	-9664	-274
488	COM[123]	-9664	-314
489	COM[124]	-9664	-354
490	COM[125]	-9664	-394
491	COM[126]	-9664	-434
492	COM[127]	-9664	-474
493	COM[128]	-9664	-514
494	COM[129]	-9664	-554
495	COM[130]	-9664	-594
496	COM[131]	-9664	-634
497	V0IN	-5444	-660
498	V0IN	-5334	-660
499	V0IN	-5224	-660
500	V0IN	-5114	-660
501	V0IN	-5004	-660
502	V0IN	-4894	-660

PAD No.	PIN Name	X	Y
503	V0OUT	-4784	-660
504	V0OUT	-4674	-660
505	V0OUT	-4564	-660
506	V0OUT	-4454	-660
507	V0OUT	-4344	-660
508	V0OUT	-4234	-660
509	V1	-4124	-660
510	V2	-4014	-660
511	V3	-3904	-660
512	V4	-3794	-660
513	VREF	-3684	-660
514	VSS	-3574	-660
515	VSS	-3464	-660
516	VSS	-3354	-660
517	VSS	-3244	-660
518	VSS	-3134	-660
519	VSS	-3024	-660
520	VSS1	-2914	-660
521	VSS1	-2804	-660
522	VDD1	-2694	-660
523	VDD1	-2584	-660
524	VDD	-2474	-660
525	VDD	-2364	-660
526	VDD	-2254	-660
527	VDD	-2144	-660
528	VDD	-2034	-660
529	VDD	-1924	-660
530	CL	-1814	-660
531	CLS	-1704	-660
532	VSS	-1594	-660
533	VDD	-1484	-660
534	A0	-1374	-660
535	RW_WR	-1264	-660
536	VSS	-1154	-660
537	VDD	-1044	-660
538	D0	-934	-660

PAD No.	PIN Name	X	Y
539	D1	-824	-660
540	D2	-714	-660
541	D3	-604	-660
542	D4	-494	-660
543	D5	-384	-660
544	D6	-274	-660
545	D7	-164	-660
546	VSS	-54	-660
547	VDD	56	-660
548	D8	166	-660
549	D9	276	-660
550	D10	386	-660
551	D11	496	-660
552	D12	606	-660
553	D13	716	-660
554	D14	826	-660
555	D15	936	-660
556	VSS	1046	-660
557	VDD	1156	-660
558	E_RD	1266	-660
559	RST	1376	-660
560	VSS	1486	-660
561	VDD	1596	-660
562	IF1	1706	-660
563	IF2	1816	-660
564	IF3	1926	-660
565	CSEL	2036	-660
566	VSS	2146	-660
567	VDD	2256	-660
568	SI	2366	-660
569	SCL	2476	-660
570	/CS	2586	-660
571	VDD	2696	-660
572	VDD	2806	-660
573	VDD	2916	-660
574	VDD	3026	-660

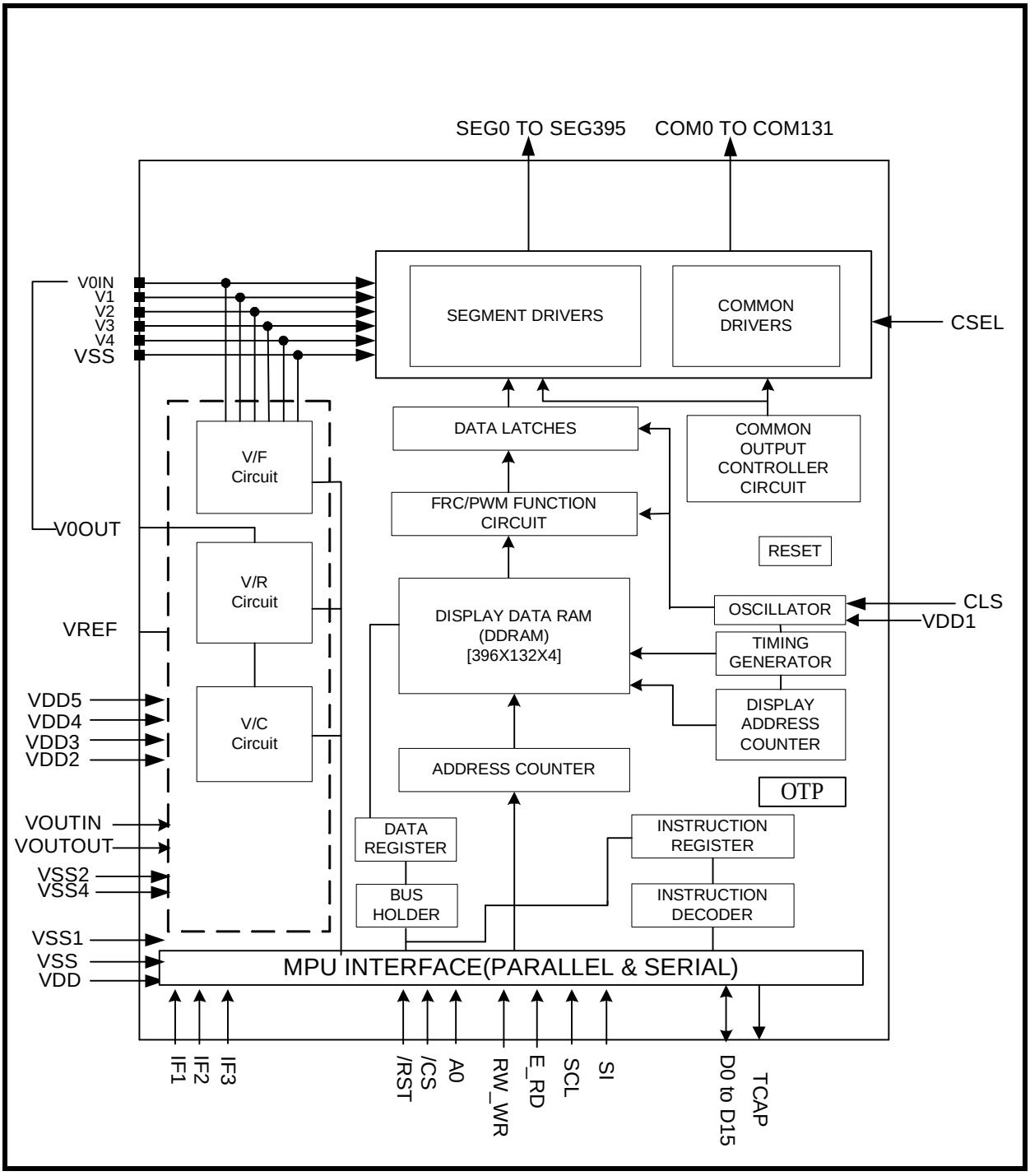
PAD No.	PIN Name	X	Y
575	VDD	3136	-660
576	VDD	3246	-660
577	VDD1	3356	-660
578	VDD1	3466	-660
579	VSS1	3576	-660
580	VSS1	3686	-660
581	VSS	3796	-660
582	VSS	3906	-660
583	VSS	4016	-660
584	VSS	4126	-660
585	VSS	4236	-660
586	VSS	4346	-660
587	VSS2	4456	-660
588	VSS2	4566	-660
589	VSS2	4676	-660
590	VSS2	4786	-660
591	VSS2	4896	-660
592	VSS2	5006	-660
593	VSS2	5116	-660
594	VSS2	5226	-660
595	VSS2	5336	-660
596	VSS2	5446	-660
597	VSS2	5556	-660
598	VSS2	5666	-660
599	VSS4	5776	-660
600	VSS4	5886	-660
601	VDD4	5996	-660
602	VDD4	6106	-660
603	VDD3	6216	-660
604	VDD3	6326	-660
605	VDD2	6436	-660
606	VDD2	6546	-660
607	VDD2	6656	-660
608	VDD2	6766	-660
609	VDD2	6876	-660
610	VDD2	6986	-660

PAD No.	PIN Name	X	Y
611	VDD2	7096	-660
612	VDD2	7206	-660
613	VDD2	7316	-660
614	VDD2	7426	-660
615	VDD5	7536	-660
616	VDD5	7646	-660
617	VDD5	7756	-660
618	VDD5	7866	-660
619	TCAP	7978	-660
620	VOUTIN	8090	-660
621	VOUTIN	8200	-660
622	VOUTIN	8310	-660
623	VOUTIN	8420	-660
624	VOUTIN	8530	-660
625	VOUTIN	8640	-660
626	VOUTOUT	8750	-660
627	VOUTOUT	8860	-660
628	VOUTOUT	8970	-660
629	VOUTOUT	9080	-660
630	VOUTOUT	9190	-660
631	VOUTOUT	9300	-660
632	COM[0]	9664	-634
633	COM[1]	9664	-594
634	COM[2]	9664	-554
635	COM[3]	9664	-514
636	COM[4]	9664	-474
637	COM[5]	9664	-434
638	COM[6]	9664	-394
639	COM[7]	9664	-354
640	COM[8]	9664	-314
641	COM[9]	9664	-274
642	COM[10]	9664	-234
643	COM[11]	9664	-194
644	COM[12]	9664	-154
645	COM[13]	9664	-114
646	COM[14]	9664	-74

PAD No.	PIN Name	X	Y
647	COM[15]	9664	-34
648	COM[16]	9664	6
649	COM[17]	9664	46
650	COM[18]	9664	86
651	COM[19]	9664	126
652	COM[20]	9664	166
653	COM[21]	9664	206
654	COM[22]	9664	246

PAD No.	PIN Name	X	Y
655	COM[23]	9664	286
656	COM[24]	9664	326
657	COM[25]	9664	366
658	COM[26]	9664	406
659	COM[27]	9664	446
660	COM[28]	9664	486
661	COM[29]	9664	526
662	COM[30]	9664	566
663	COM[31]	9664	606

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 POWER SUPPLY

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td>Power</td><td>Power supply for logic circuit</td></tr>
<tr><td>VDD1</td><td>Power</td><td>Power supply for OSC circuit</td></tr>
<tr><td>VDD2</td><td>Power</td><td>Power supply for Booster Circuit</td></tr>
<tr><td>VDD3</td><td>Power</td><td>Power supply for LCD.</td></tr>
<tr><td>VDD4</td><td>Power</td><td>Power supply for LCD.</td></tr>
<tr><td>VDD5</td><td>Power</td><td>Power supply for LCD.</td></tr>
<tr><td>VSS</td><td>Power</td><td>Ground. Ground system should be connected together.</td></tr>
<tr><td>VSS1</td><td>Power</td><td>Ground. Ground system should be connected together.</td></tr>
<tr><td>VSS2</td><td>Power</td><td>Ground. Ground system should be connected together.</td></tr>
<tr><td>VSS4</td><td>Power</td><td>Ground. Ground system should be connected together.</td></tr>
<tr><td>VOUTOUT</td><td>Power</td><td>If the internal voltage generator is used, the VOUTIN & VOUTOUT must be connected together.
If an external supply is used, this pin must be left open.</td></tr>
<tr><td>VOUTIN</td><td>Power</td><td>An external LCD supply voltage can be supplied using the V_{OUTIN} pad. In this case, VOUTOUT has to be left open, and the internal voltage generator has to be programmed to zero. (SET register VC=0)</td></tr>
<tr><td>V0IN
V0OUT
V1
V2
V3
V4</td><td>Power</td><td>LCD driver supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
V0IN & V0OUT should be connected together.
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.
<table>
<tr><th>LCD bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/N bias</td><td>(N-1) / N x V0</td><td>(N-2) / N x V0</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
NOTE: N = 5 to 12</td></tr>
<tr><td>VREF</td><td>O</td><td>Reference voltage output for monitor only. Left it opened.</td></tr>
</table>

6.2 LCD DRIVER SUPPLY

Name	I/O	Description
CLS	I	When using internal clock oscillator, connect CLS to VDD. When using external clock oscillator, connect CLS to VSS.
CL	I/O	When using internal clock oscillator, it's oscillator output. (when CLS="H") When using external clock oscillator, it's oscillator input. (when CLS="L")

6.3 SYSTEM CONTROL

Name	I/O	Description
CSEL	I	Must contact to VSS
TCAP	I	Test pin. Do not use. Let it open.

6.4 MICROPROCESSOR INTERFACE

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RST</td><td>I</td><td>Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td>IF[3:1]</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><th>IF1</th><th>IF2</th><th>IF3</th><th>MPU interface type</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>80 series 16-bit parallel</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>68 series 16-bit parallel</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>68 series 8-bit parallel</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>9-bit serial (3 line)</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>8-bit serial (4 line)</td></tr>
</table></td></tr>
<tr><td>/CS</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when /CS is "L". When chip select is non-active, D0 to D7 are high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
– A0 = "H": D0 to D15 or SI are display data
– A0 = "L": D0 to D15 or SI are control data
In 3-line interface not let it floating, contact it to VSS or VDD.</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>RW</td><td>Read / Write control input pin
RW = “H” : read
RW = “L” : write</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on D0 to D15 are latched at the rising edge of the /WR signal.</td></tr>
</table>
When not use, contact it to VDD.</td></tr>
</table>

<table>
<tr><td>E_RD</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Read / Write control input pin
– RW = “H”: When E is “H”, D0 to D15 are in an output status.
– RW = “L”: The data on D0 to D15 are latched at the falling edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, D0 to D15 are in an output status.</td></tr>
</table>
When not use, contact it to VDD</td></tr>
<tr><td>D15 to D0</td><td>I/O</td><td>They connect to the standard 8-bit or 16 bit MPU bus via the 8/16 –bit bi-directional bus.
When the following interface is selected and the CS pin is high, the following pins become high impedance.
1. 8-bit parallel: D15-D8 are in the state of high impedance, should contact to “H” level.
2. Serial interface: D15-D0 are in the state of high impedance, should contact to “H” level.</td></tr>
<tr><td>SI</td><td>I</td><td>This pin is used to input serial data when the serial interface is selected.(3 line and 4 line)
When not use contact it to VSS or VDD.</td></tr>
<tr><td>SCL</td><td>I</td><td>This pin is used to input serial clock when the serial interface is selected.
The data is converted in the rising edge. (3 line and 4 line)
When not use contact it to VSS or VDD.</td></tr>
</table>

NOTE: Microprocessor interface pins should not be floating in any operation mode.

6.5 LCD DRIVER OUTPUTS

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG395</td><td>O</td><td>LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">M (Internal)</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
</table>

<table>
<tr>
<td>COM0
to
COM131</td>
<td>O</td>
<td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>M (Internal)</th><th>Common driver output voltage</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td></tr>
</table>
</td>
</tr>
</table>

ST7632 I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
IF[2:0],CLS,CSEL	**No Limitation**
VREF, TCAP, CLP	**Floating**
VDD, VDD1~VDD5, VSS, VSS1, VSS2, VSS4, VOUTIN, VOUTOUT	**<100Ω**
V0IN, V0OUT, V1, V2, V3, V4	**<100Ω**
A0, RW_WR, E_RD, /CS, D0 …D15, SCL, SI	**<1KΩ**
RESB	**<10KΩ**

Suggest Vop range : 12v~14v

7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

There is /CS pin for chip selection. The ST7632 can interface with an MPU when /CS is "L". When these pins are set to any other combination, A0, E_RD, and RW_WR inputs are disabled and D0 to D15 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

7.1.1 Selecting Parallel / Serial Interface

ST7632 has six types of interface with an MPU, which are two serial and four parallel interfaces. This parallel or serial interface is determined by IF pin as shown in table 7.1.1.

Table 7.1.1 Parallel / Serial Interface Mode

IF1	IF2	IF3	Interface type	/CS	A0	E_RD	RW_WR	D15 to D8 D7 to D0	SI	SCL
H	H	H	80 serial 16-bit parallel	/CS	A0	/RD	/WR	D15 to D8 D7 to D0	VDD	VDD
H	H	L	80 serial 8-bit parallel	/CS	A0	/RD	/WR	fix to VDD D7 to D0	VDD	VDD
H	L	L	68 serial 16-bit parallel	/CS	A0	E	RW	D15 to D8 D7 to D0	VDD	VDD
L	H	H	68 serial 8-bit parallel	/CS	A0	E	RW	fix to VDD D7 to D0	VDD	VDD
L	L	H	9-bit SPI mode (3 line)	/CS	VDD	VDD	VDD	fix to VDD	SI	SCL
L	L	L	8-bit SPI mode (4 line)	/CS	A0	VDD	VDD	fix to VDD	SI	SCL

7.1.2 8- or 16-bit Parallel Interface

The ST7632 identifies type of the data bus signals according to combinations of A0, E_RD and RW_WR SIGNALS 8-bit as shown in table 7.1.2.

Table 7.1.2 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	RW	E	/RD	/WR	
H	H	H	L	H	Display data read out
H	L	H	H	L	Display data write
L	H	H	L	H	Register status read
L	L	H	H	L	Writes to internal register (instruction)

Relation between Data Bus and Gradation Data

ST7632 offers the 256-color display (8 gray scale) out of 4096, the 4096-color display (16 gray scale), the dithered 65K color display, dithered 262K color display, and dithered 16M color display.

When using 256-color display out of 4096 colors, you can specify color for each of R, G and B using the palette function.

When using 4096-color display, you can select the type A or B display mode depending on the data bus and RGB you use.

When using 65K, 262K, and 16M color, you can specify color for each of R, G, B using the palette function.

Use the command for switching between these modes.

(1) 256-color display out of 4096 colors

Using RGBSET8 command enables you to set color for each of R, G and B by turning on palette function prepared to convert 3-bit or 2-bit data to 4-bit data.

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0 : RRRGGGBB (8 bits) data is converted to RRRRGGGGBBBB (12 bits) and then stored on the display RAM.

(2) 4096-color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRR 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRRGGGGBBBB

A single pixel of data is read and written in the display RAM in a single write operation.

"XXXX" are dummy bits, and they are ignored for display.

(3) 65K color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGG 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGBBBBB 2nd write

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

2. 16-bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRGGGGGGBBBBB (16 bits)

Data is acquired through signal write operation and then written to the display RAM.

(4) 262K color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXX 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGXX 2nd write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXX 3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRXXGGGGGGXX

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBXXXXXXXXXXXX

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

"XXXX" are dummy bits, and they are ignored for display.

(5) 16M color display

1. 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRR 1st write

D7, D6, D5, D4, D3, D2, D1, D0: GGGGGGGG 2nd write

D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBB 3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

2. 16 bit mode

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRRRRRGGGGGGGG

D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: BBBBBBBBXXXXXXXX

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

7.1.3 8- and 9-bit Serial Interface

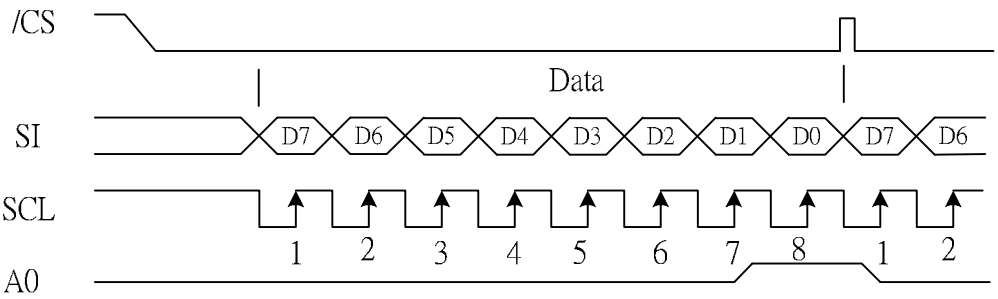
The 8-bit serial interface uses four pins /CS, SI, SCL, and A0 to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins /CS, SI and SCL for the same purpose.

Data read is not available with the serial interface. Data entered must be 8 bits. Refer to the following chart for entering commands, parameters or gray-scale data.

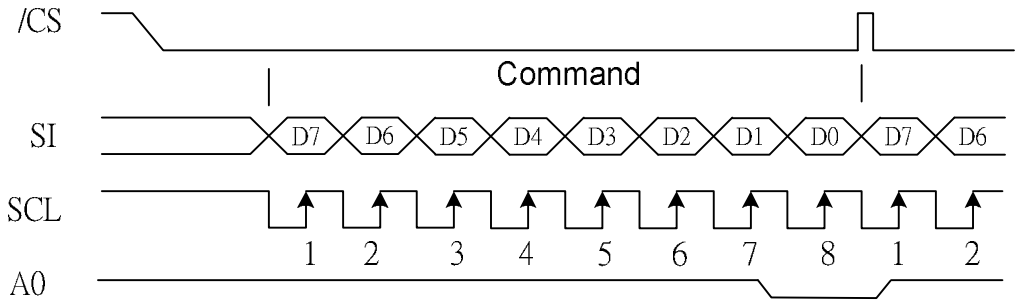
The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4 line)

When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.

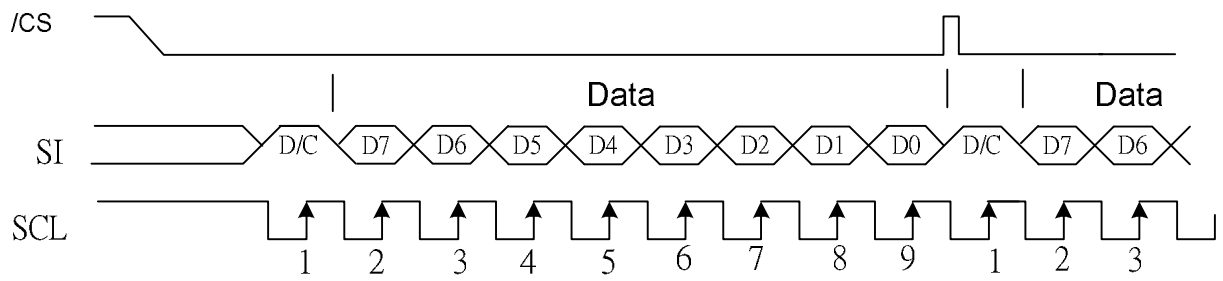


When entering command: A0= LOW at the rising edge of the 8th SCL

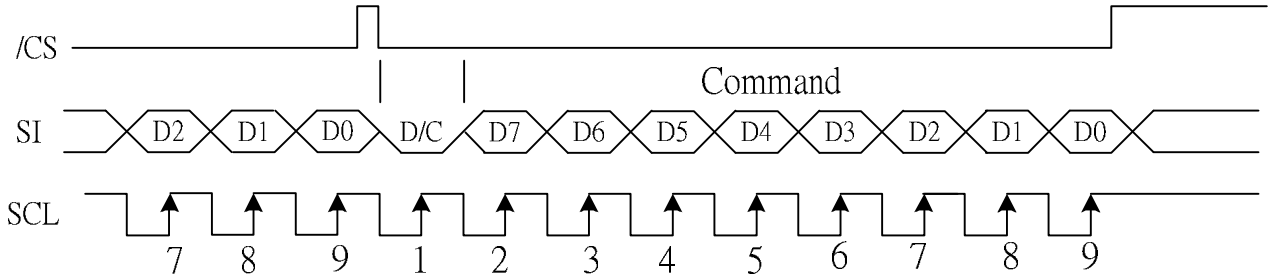


(2) 9-bit serial interface (3 line)

When entering data (parameters): SI= HIGH at the rising edge of the 1st SCL.



When entering command: SI= LOW at the rising edge of the 1st SCL.



- If /CS is caused to HIGH before 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set /CS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.
- When executing the command RAMWR, set /CS to HIGH after writing the last address (after starting the 9th pulse in case of 9-bit serial input or after starting the 8th pulse in case of 8-bit serial input).

7-2 ACCESS TO DDRAM AND INTERNAL REGISTERS

ST7632 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Fig. 7.2.1 illustrates these relations.

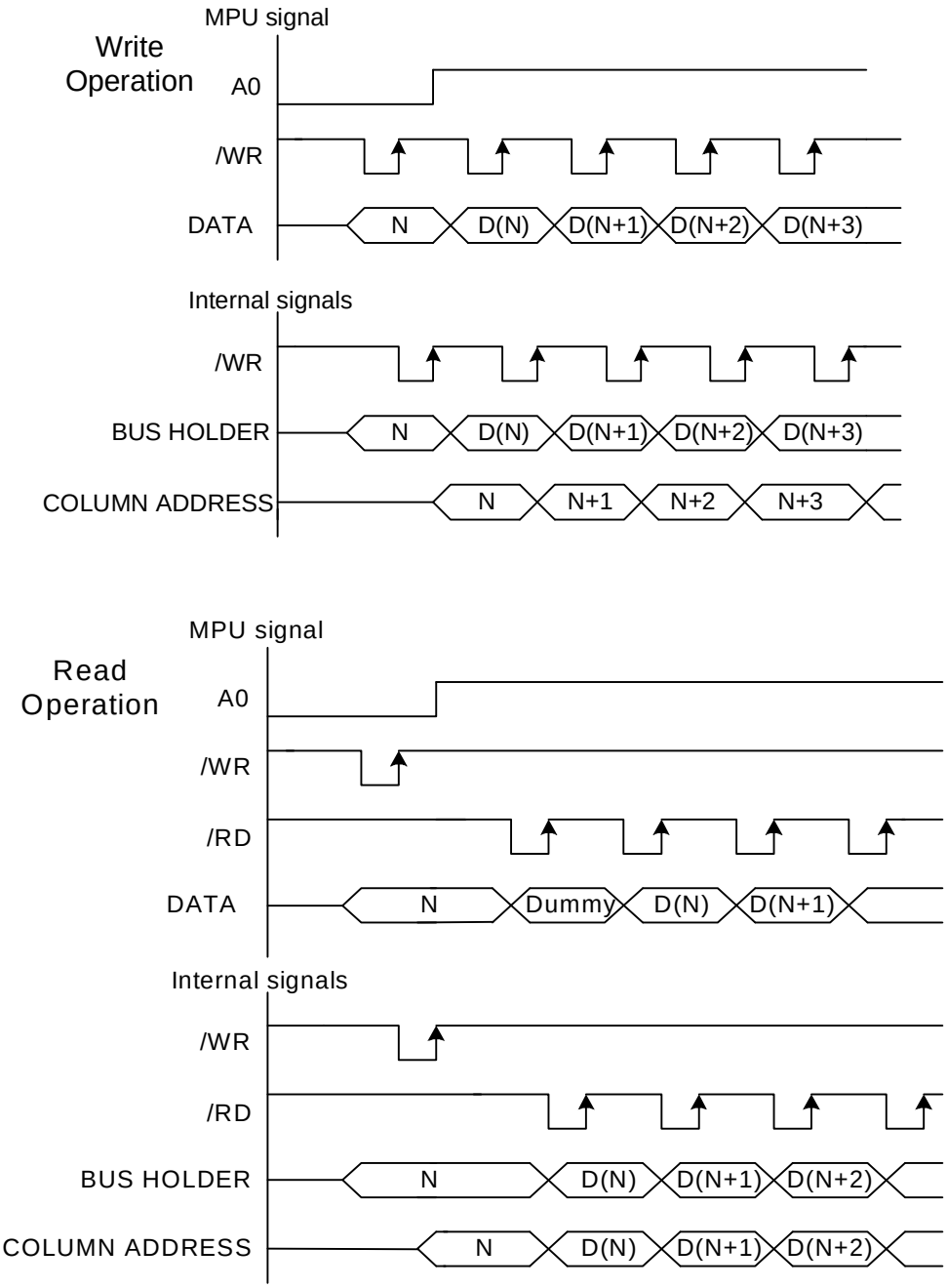


Fig 7.2.1

7-3 DISPLAY DATA RAM (DDRAM)

7.3.1 DDRAM

It is 396 X 132 X 4 bits capacity RAM prepared for storing dot data. You can access a desired bit by specifying the page address and column address. Since display data from MCU D7 to D0 and D15 to D8 correspond to one or two pixels of RGB, data transfer related restrictions are reduced, realizing the display flexing.

The RAM on ST7632 is separated to a block per 4 lines to allow the display system to process data on the block basis.

MPU's read and write operations to and from the RAM are performed via the I/O buffer circuit; Reading of the RAM for the liquid crystal drive is controlled from another separate circuit. Refer to the following memory map for the RAM configuration.

Memory Map (When using the 8 gray-scale. 8-bit mode)

RGB alignment (Command of data control parameter2=000)													
Data control command (BCH)			Column										
LCD read direction ↓	**P11:0**		0			1				131			
	P11:1		131			130				0			
	Color		**R**	**G**	**B**	**R**	**G**	**B**		**R**	**G**	**B**
	Data / Page		D7 D6 D5	D4 D3 D2	D1 D0	D7 D6 D5	D4 D3 D2	D1 D0		D7 D6 D5	D4 D3 D2	D1 D0
Block	**P10:0**	**P10:1**										
0	0	131										
	1	130										
	2	129										
	3	128										
1	4	127										
	5	126										
	6	125										
	7	124										
2	8	123										
	9	122										
31	124	7										
	125	6										
	126	5										
	127	4										
32	128	3										
	129	2										
	130	1										
	131	0										
SEGout			0	1	2	3	4	5		393	392	395

Memory Map (When using the 16 gray-scale Type B. 8-bit mode)

RGB alignment (Command of data control parameter2=000)														
Data control command (BCH)			Column											
LCD read direction	**P11:0**		0			1					131			
	Color		**R**	**G**	**B**	**R**	**G**	**B**			**R**	**G**	**B**	
	Page \ Data		D3	D7	D3	D3	D7	D3			D3	D7	D3	
			D2	D6	D2	D2	D6	D2			D2	D6	D2	
			D1	D5	D1	D1	D5	D1			D1	D5	D1	
			D0	D4	D0	D0	D4	D0			D0	D4	D0	
	P11:1		131			130					0			
	Color		**R**	**G**	**B**	**R**	**G**	**B**			**R**	**G**	**B**	
	Page \ Data		D3	D7	D3	D3	D7	D3			D3	D7	D3	
			D2	D6	D2	D2	D6	D2			D2	D6	D2	
			D1	D5	D1	D1	D5	D1			D1	D5	D1	
			D0	D4	D0	D0	D4	D0			D0	D4	D0	
Block	**P10:0**	**P10:1**												
0	0	131												
	1	130												
	2	129												
	3	128												
1	4	127												
	5	126												
	6	125												
	7	124												
2	8	123												
	9	122												
31	124	7												
	125	6												
	126	5												
	127	4												
32	128	3												
	129	2												
	130	1												
	131	0												
SEGout			0	1	2	3	4	5			393	394	395	

You can change position of R and B with DATACTL command.

Memory Map (When using the 16 gray-scale Type B. 16-bit mode, 16 gray-scale 65K (8bit/16bit), 16 gray-scale 262K(8bit/16bit), and 16 gray-scale 65M(8bit/16bit) mode.)

RGB alignment (Command of data control parameter2=000)														
Data control command (BCH)			Column											
LCD read direction ↓	**P11:0**		0			1					131			
	Color		**R**	**G**	**B**	**R**	**G**	**B**			**R**	**G**	**B**	
	Page \ Data		D11	D7	D3	D11	D7	D3			D11	D7	D3	
			D10	D6	D2	D10	D6	D2			D10	D6	D2	
			D9	D5	D1	D9	D5	D1			D9	D5	D1	
			D8	D4	D0	D8	D4	D0			D8	D4	D0	
	P11:1		131			130					0			
	Color		**R**	**G**	**B**	**R**	**G**	**B**			**R**	**G**	**B**	
	Page \ Data		D11	D7	D3	D11	D7	D3			D11	D7	D3	
			D10	D6	D2	D10	D6	D2			D10	D6	D2	
			D9	D5	D1	D9	D5	D1			D9	D5	D1	
			D8	D4	D0	D8	D4	D0			D8	D4	D0	
Block	**P10:0**	**P10:1**												
0	0	131												
	1	130												
	2	129												
	3	128												
1	4	127												
	5	126												
	6	125												
	7	124												
2	8	123												
	9	122												
31	124	7												
	125	6												
	126	5												
	127	4												
32	128	3												
	129	2												
	130	1												
	131	0												
SEGout			0	1	2	3	4	5			393	394	395	

You can change position of R and B with DATACTL command.

7.3.2 Page Address Control Circuit

This circuit is used to control the address in the page direction when MPU accesses the DDRAM or when reading the DDRAM to display image on the LCD.

You can specify a scope of the page address with page address set command. When the page-direction scan is specified with DATACTL command and the address are incremented from the start up to the end page, the column address is incremented by 1 and the page address returns to start page.

The DDRAM supports up to 132 lines, and thus the total page becomes 132.

In the read operation, as the end page is reached, the column address is automatically incremented by 1 and the page address is returned to start page.

Using the address normal/inverse parameter of DATACTL command allows you to inverse the correspondence between the DDRAM address and command output.

7.3.3 Column Address Control Circuit

This circuit is used to control the address in the column direction when MPU accesses the DDRAM. You can specify a scope of the column address using column address set command. When the column-direction scan is specified with DATACTL command and the address are incremented from the start up to the end page, the page address is incremented by 1 and the column address returns to start column.

In the read operation, too, the column address is automatically incremented by 1 and returned to start page as the end column is reached.

Just like the page address control circuit, using the column address Normal/Reverse parameter of DATACTL command enables to inverse the correspondence between the DDRAM column address and segment output. This arrangement relaxes restrictions in the chip layout on the LCD module.

7.3.4 I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM while the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.5 Block Address Circuit

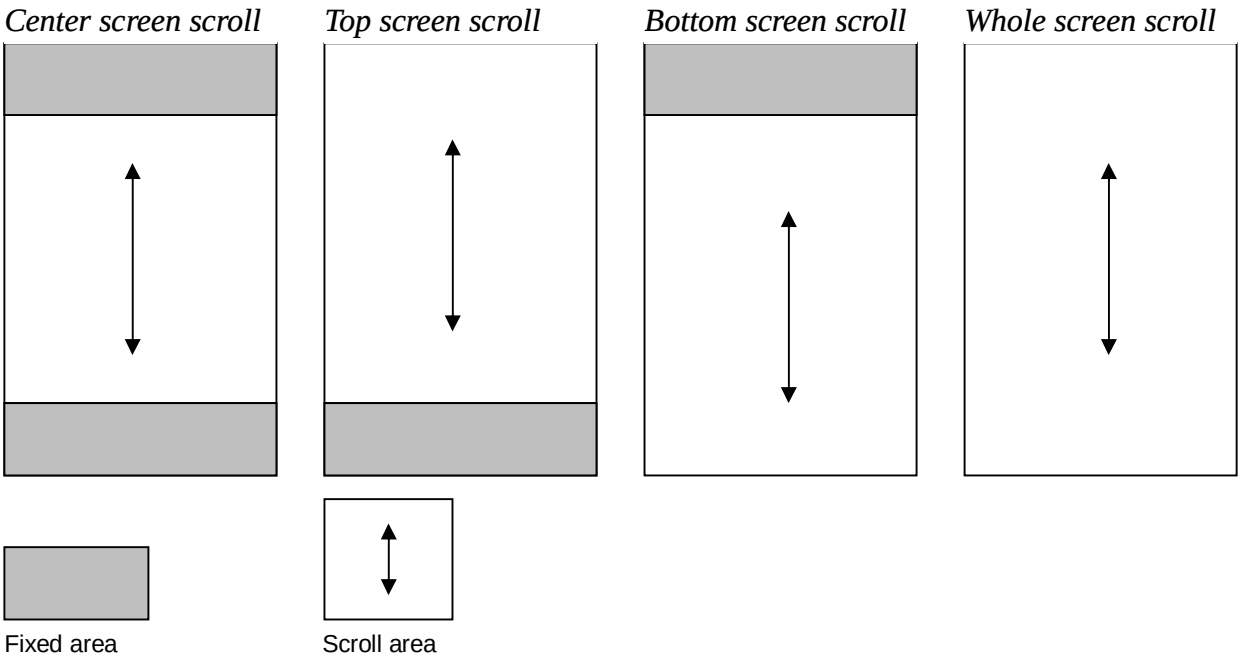
The circuit associates pages on DDRAM with COM output. ST7632 processes signals for the liquid crystal display on 4-page basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in block.

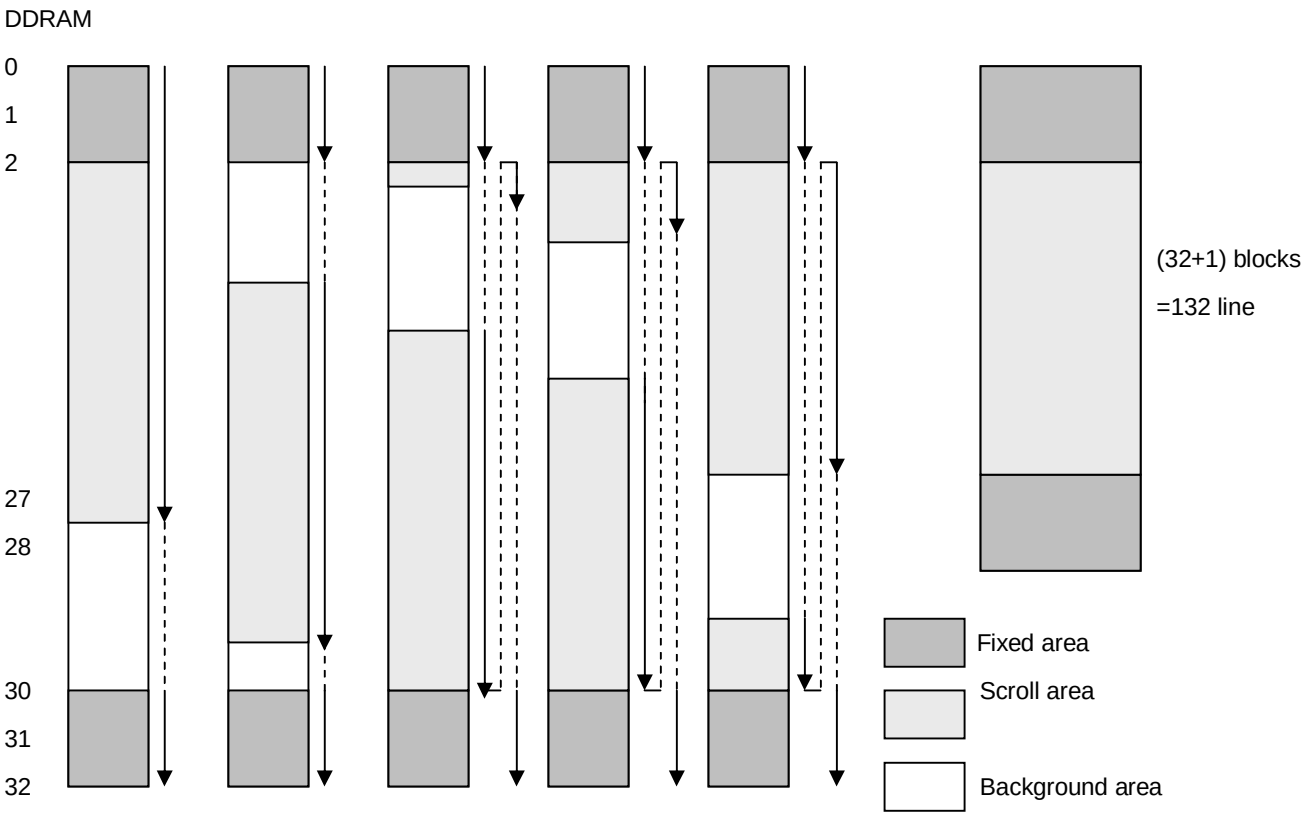
7.3.6 Display data Latch Circuit

This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.4 Area Scroll Display

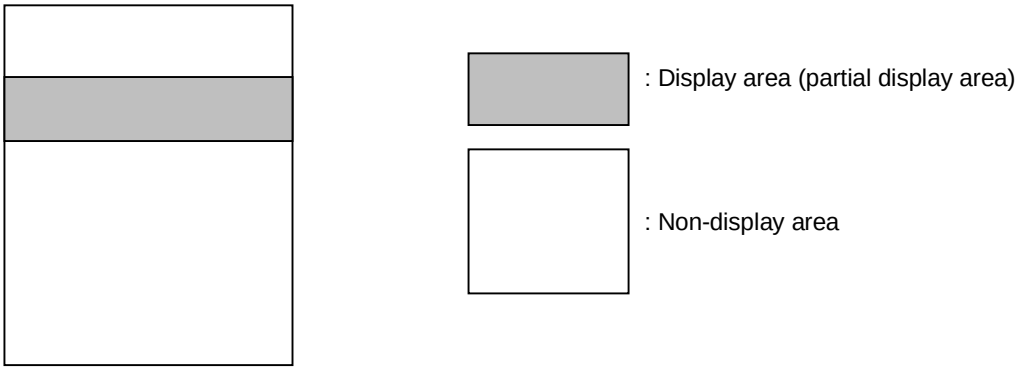
Using area scroll set and scroll start set commands allows you to scroll the display screen partially. You can select any one of the following four scroll patterns.





7.5 Partial Display

Using partial in command allows you turn on the partial display (division by line) of the screen. This mode requires less current consumption than the whole screen display, making it suitable for the equipment in the standby state.



If the partial display region is out of the Max. Display range, it would be no operation

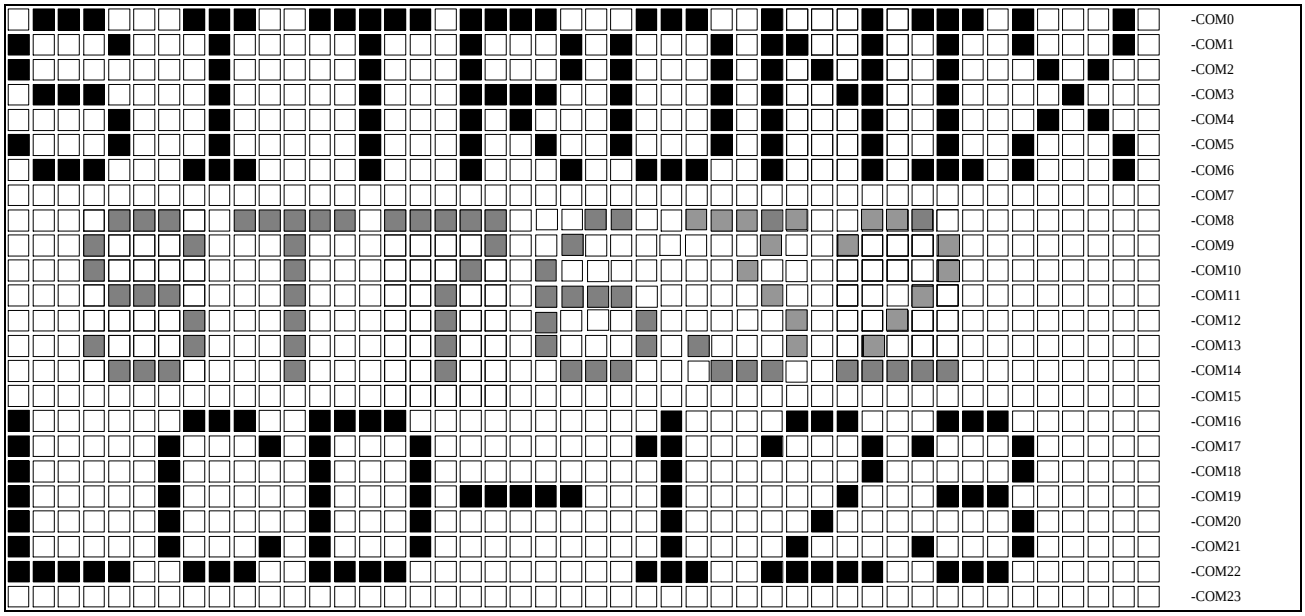


Figure 7.5.1.Reference Example for Partial Display

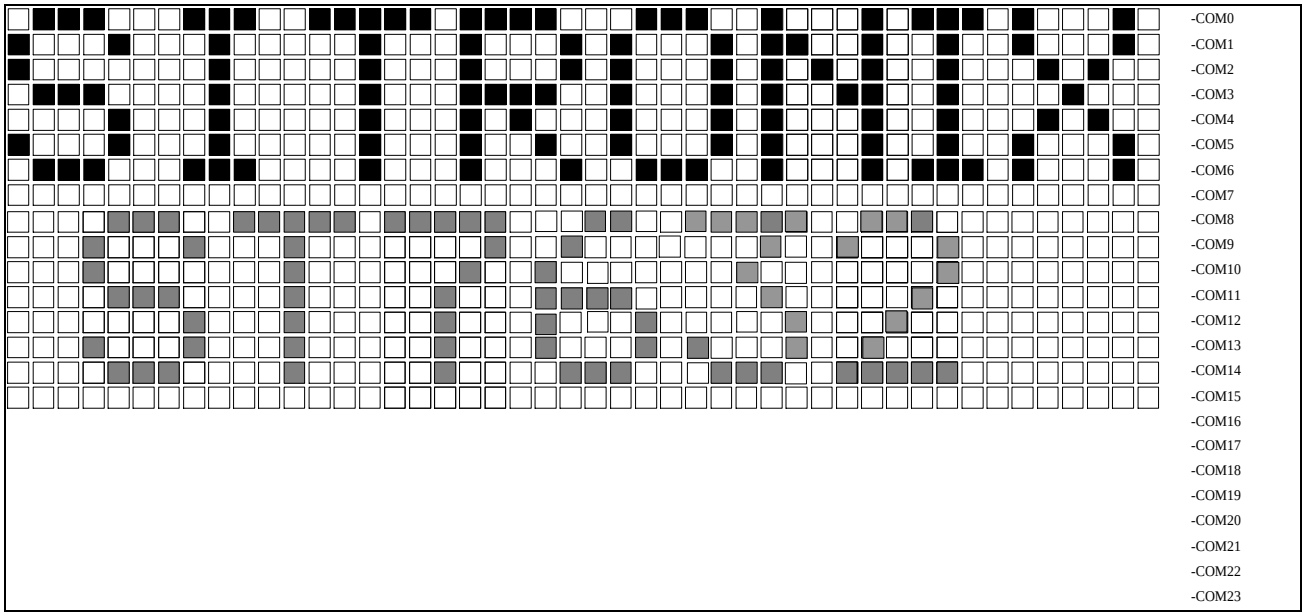


Figure 7.5.2.Partial Display (Partial Display Duty=16,initial COM0=0)

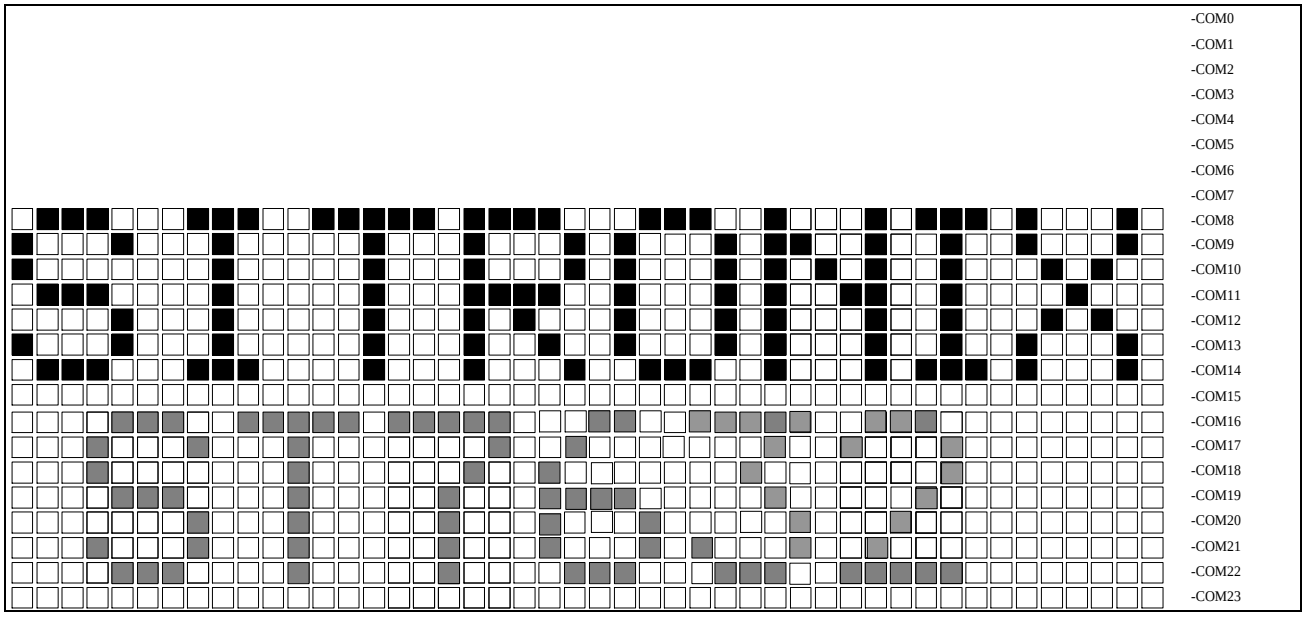


Figure 7.5.3.Moving Display (Partial Display Duty=16,Initial COM0=8)

7.6 Gray-Scale Display

ST7632 incorporates a 4FRC & 31 PWM function circuit to display a 16 gray-scale display.

7.7 Oscillation circuit

This is on-chip Oscillator without external resistor. When the internal oscillator is used, CLS must connect to VDD; when the external oscillator is used, CL could be input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.8 Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 132-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M), which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.8.1.

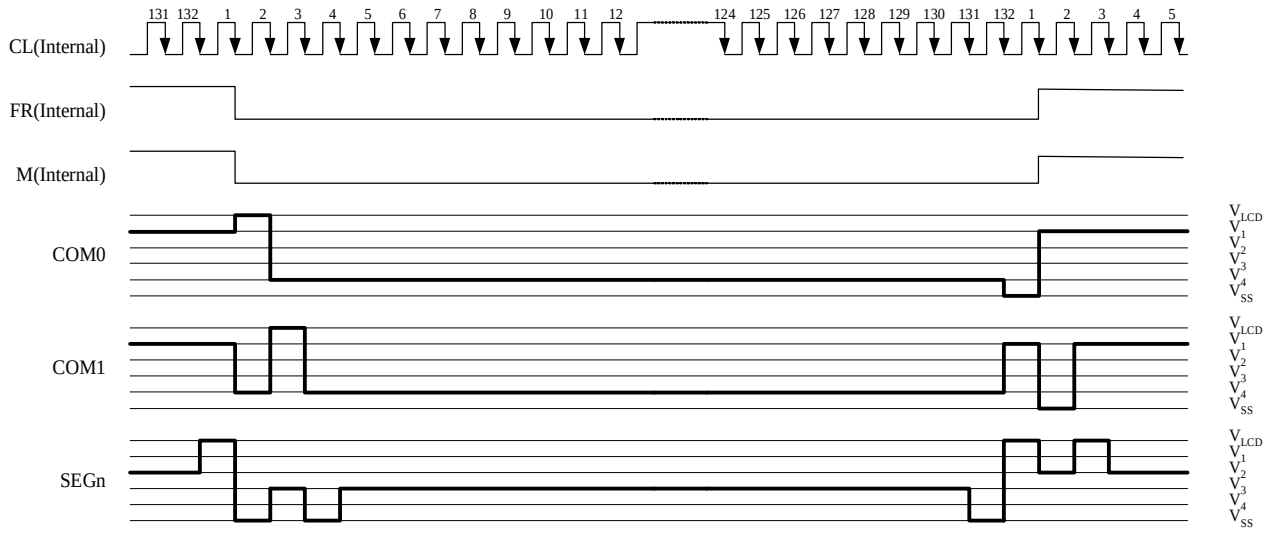


Figure 7.8.1 2-frame AC Driving Waveform (Duty Ratio: 1/132)

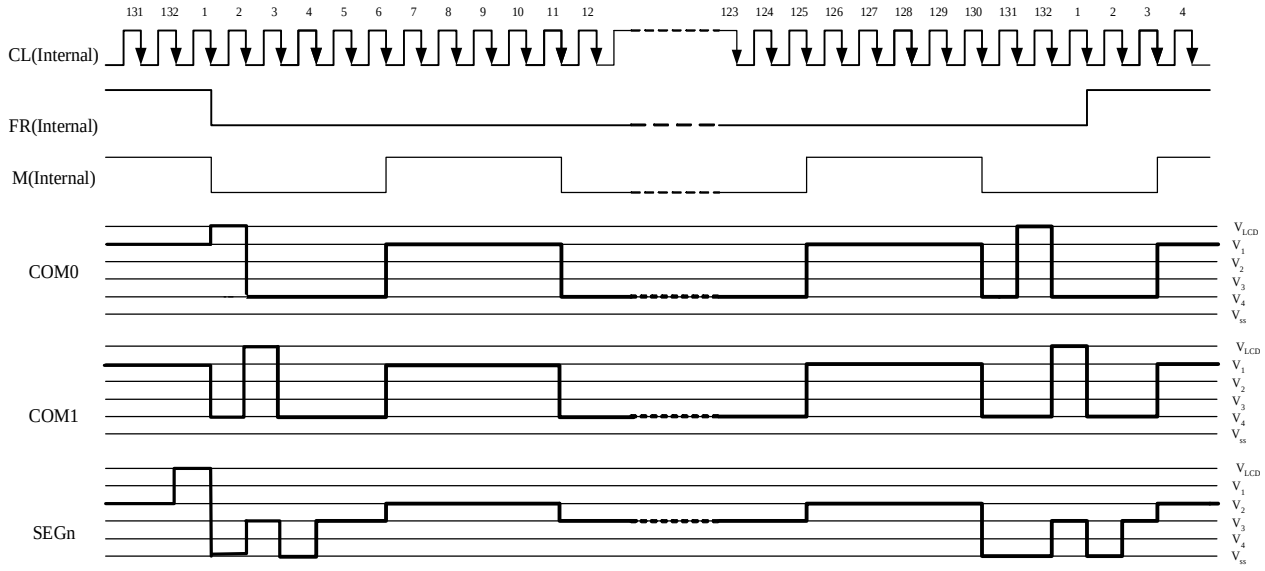
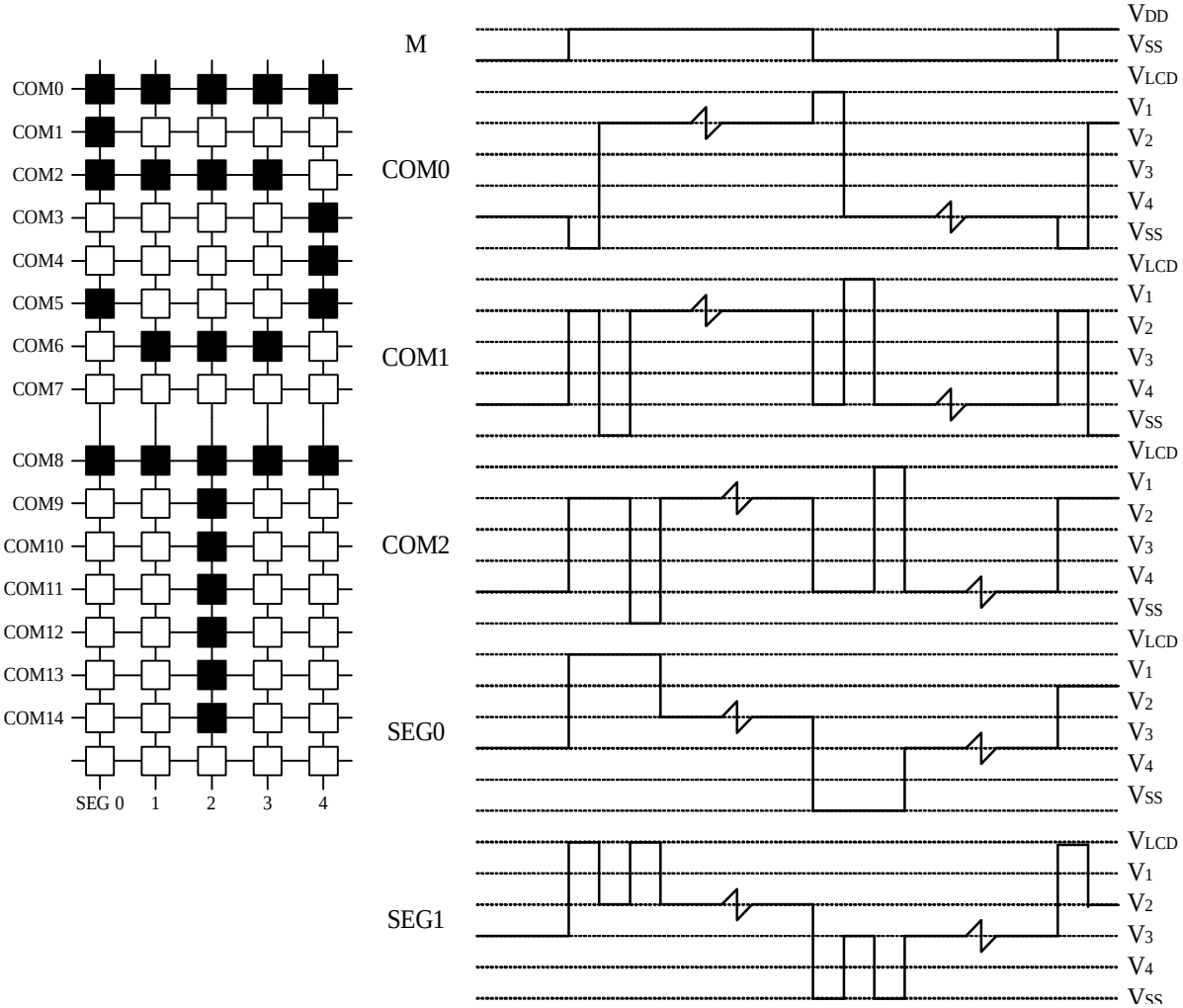


Figure 7.8.2 N-Line Inversion Driving Waveform (N=5,Duty Ratio=1/132)

7.9 Liquid Crystal drive Circuit

This driver circuit is configured by 132-channel common drivers and 396-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.



7.10 Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 7.10.1 shows the referenced combinations in using Power Supply circuits.

Table 7.10.1 Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

7.10.1 Voltage Converter Circuits

These circuits boost up the electric potential between VDD2 and Vss to 2, 3, 4, 5, 6, 7 or 8 times toward positive side and booster voltage is outputted from VOUOUT pin. It is possible to select the lower boosting level in any boosting circuit by “ANASET” instruction.

7.10.2 Voltage Regulator Circuits

SET VOP (SETVOP)

The set VOP function is used to program the optimum LCD supply voltage V0.

SETVOP

For example when Vop[8:0] is 257DEC = 13.88V.

The VOP value is programmed via the Vop[8:0] register.

V0=a+(Vop[8:6]Vop[5:0]) · b

Ex:Vop[5:0]=000001, Vop[8:6]=100

→ Vop [8:0]=100000001

→ 3.6+257x0.04=13.88

- a is a fixed constant value (see table 7.10.2).
- b is a fixed constant value (see table 7.10.2).
- Vop[8:0] is the programmed VOP value. The programming range for Vop[8:0] is 4 to 410 (05 to 19A hex).
- VOP[5:0] is the set contrast value which can be set via the interface and is in two’s complement format.(See command VOLUP & VOLDOWN)

Table 7.10.2

SYMBOL	VALUE	UNIT
a	3.6	V
b	0.04	V

The VOP[8:0] value must be in the V_{LCD} programming range as given in Fig.7.10.2. Evaluating equation (1), values outside the programming range indicated in Fig.7.10.2 may result. Calculated values below VOP[8:0]=4 will be mapped to VOP[8:0]=4, resulting V_{OP} values higher than VOP[8:0]=410 will be mapped to V_{OP}=410.

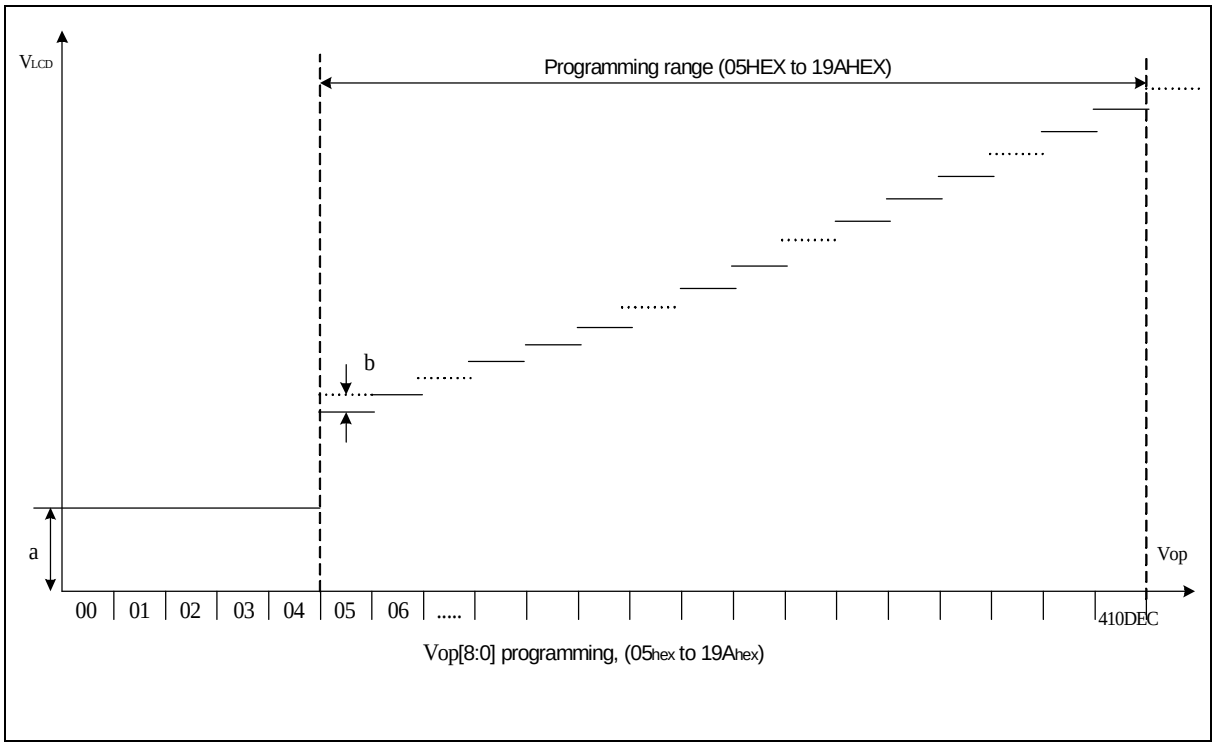


Fig. 7.10.2 VLCD programming range

As the programming range for the internally generated V_0 allows values above the max. Allowed V_0 (18V) the user has to ensure while setting the VOP register and the temperature compensation that under all conditions and including all tolerances the V_0 remains below 18V.

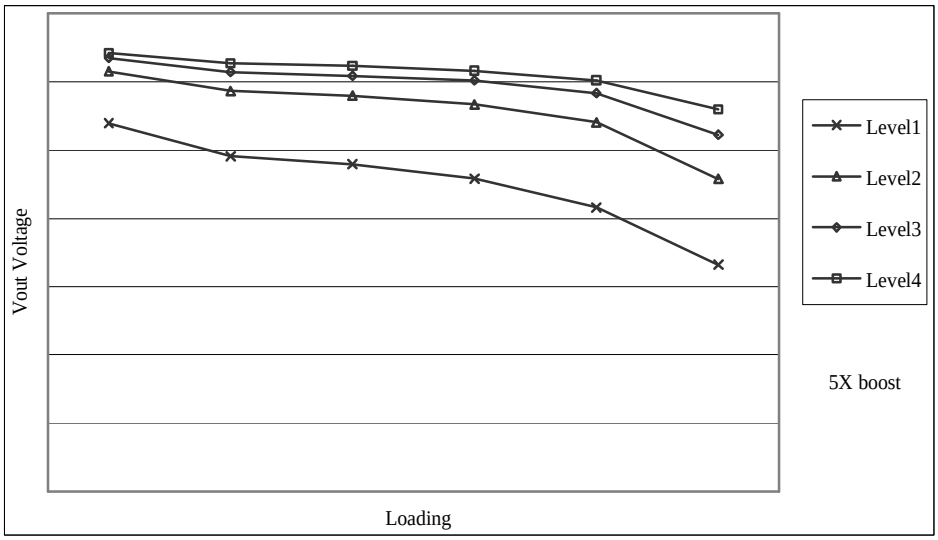
Par no.	Equipment Type	Thermal Gradient
ST7632	Internal Power Supply	-0.125(+-10%)%/℃

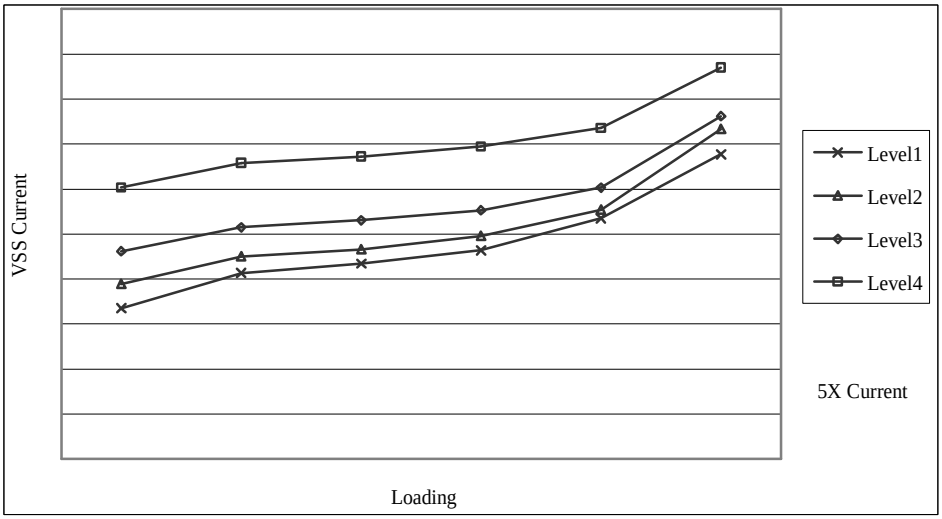
Booster Efficiency

By Booster Stages (2X, 3X, 4X, 5X, 6X, 7X, 8X) and Booster Efficiency (Level1~4) commands, we could easily set the best Booster performance with suitable current consumption. If the Booster Efficiency is set to higher level (level4 is higher than level1), The Boost Efficiency is better than lower level, and it just need few more power consumption current. It could be applied to each multiple voltage Condition.

When the LCD Panel loading is heavier, the performance of Booster will be not in a good working condition. User could set the BE level to be higher and just need few more current. Never consider to change to higher Booster Stage at beginning stage unless it really necessary.

The Booster Efficiency Command could be used together with Booster Stage Command to choose one best Boost output condition. Users could see the Booster Stage Command as a large scale operation, and see the Booster Efficiency Command as a small scale operation. These commands are very convenient for using.





RESET CIRCUIT

When Power is Turned On

Input power (VDD1~VDD5)

↓

Be sure to apply POWER-ON RESET (RES = LOW)

↓

<Display Setting>	**<<State after resetting>>**
Display control (DISCTL)	
Setting clock dividing ratio:	1 dividing
Duty setting:	1/4
Setting reverse rotation number of line:	11h reverse rotations
Common scan direction (COMSCN)	
Setting scan direction:	COM1 -> COM68, COM69 -> COM132
Oscillation ON (OSCON)	Oscillation OFF

↓

Sleep-out (SLIPOUT)	Sleep-in

↓

<Power Supply Setting>	**<<State after resetting>>**
Electronic volume control (VOLCTR)	
Setting volume value :	0
Setting built-in resistance value:	0 (3.76)
Power control (PWRCTR)	
Setting operation of power supply circuit:	All OFF

↓

<Display Setting 2>	**<<State after resetting>>**
Normal rotation of display (DISNOR)/Inversion of display (DISINV): Normal rotation of display	
Partial-in (PTLIN)/Partial-out (PTLOUT)	Partial-out
Setting fix area:	0
Area scroll set (ASSET)	
Setting area scroll region:	0
Setting area scroll type:	Full-screen scroll
Scroll start set (SCSTART)	
Setting scroll start address:	0

↓

<Display Setting 3>	**<<State after resetting>>**
Data control (DATCTL)	
Setting Normal/Reverse rotation of page address:	Normal rotation
Setting Normal/Reverse rotation of column address:	Normal rotation
Setting direction of address scanner:	Column direction

Setting RGB arrangement: RGB

Setting gradation: 8 gradations

256-color position set (RGBSET8)

Setting color position at 256-color All 0

↓

<RAM Setting> **<<State after resetting>>**

Page address set (PASET)

Setting start page address: 0

Setting end page address: 0

Column address set (CASET)

Setting start column address: 0

Setting end column address: 0

↓

<RAM Write> **<<State after resetting>>**

Memory write command (RAMWR)

Writing displayed data : Repeat as many as the number needed

and exit by entering other command.

↓

<Waiting (approximately 100ms)>

Wait until the power supply voltage has stabilized.

Enter the power supply control command first, then wait at least

100ms before entering the display ON command when the built-in

power supply circuit operates.

If you do not wait, an unwanted display may appear on the

liquid crystal panel.

↓

Display ON (DISON): Display OFF

8. COMMANDS

Ext=0															
Command	***A0***	***RD***	***WR***	***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0***	***Function***	***Hex***	***Parameter***	***Index***
DISON	0	1	0	1	0	1	0	1	1	1	1	Display On	AF	None	1
DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display Off	AE	None	2
DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal Display	A6	None	3
DISINV	0	1	0	1	0	1	0	0	1	1	1	Inverse Display	A7	None	4
COMSCN	0	1	0	1	0	1	1	1	0	1	1	Com Scan Direc.	BB	1 byte	5
DISCTR	0	1	0	1	1	0	0	1	0	1	0	Display Control	CA	3 byte	6
SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep In	95	None	7
SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep Out	94	None	8
PASET	0	1	0	0	1	1	1	0	1	0	1	Page Addr. Set	75	2 byte	9
CASET	0	1	0	0	0	0	1	0	1	0	1	Column Addr. Set	15	2 byte	10
DATCTL	0	1	0	1	0	1	1	1	1	0	0	Data Scan Direction	BC	3 byte	11
RGBSET8	0	1	0	1	1	0	0	1	1	1	0	256-color position set	CE	20 byte	12
RAMWR	0	1	0	0	1	0	1	1	1	0	0	Writing to Memory	5C	Data	13
RAMRD	0	1	0	0	1	0	1	1	1	0	1	Reading from Memory	5D	Data	14
PLTIN	0	1	0	1	0	1	0	1	0	0	0	Partial display in	A8	2 byte	15
PLTOUT	0	1	0	1	0	1	0	1	0	0	1	Partial display out	A9	None	16
RMWIN	0	1	0	1	1	1	0	0	0	0	0	Read and Modify Write	E0	None	17
RMWOUT	0	1	0	1	1	1	0	1	1	1	0	RMW end	EE	None	18
ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area Scroll Set	AA	4 byte	19
SCSTART	0	1	0	1	0	1	0	1	0	1	1	Scroll Start Set	AB	1 byte	20
OSCON	0	1	0	1	1	0	1	0	0	0	1	Internal OSC on	D1	None	21
OSCOFF	0	1	0	1	1	0	1	0	0	1	0	Internal OSC off	D2	None	22
PWRCTL	0	1	0	0	0	1	0	0	0	0	0	Power Control	20	1 byte	23
VOLCTR	0	1	0	1	0	0	0	0	0	0	1	EC control	81	2 byte	24
VOLUP	0	1	0	1	1	0	1	0	1	1	0	EC increase 1	D6	None	25
VOLDOWN	0	1	0	1	1	0	1	0	1	1	1	EC decrease 1	D7	None	26
RESERVED	0	1	0	1	0	0	0	0	0	1	0	Not Use	82		27
EPSRRD1	0	1	0	0	1	1	1	1	1	0	0	READ Register1	7C	None	28
EPSRRD2	0	1	0	0	1	1	1	1	1	0	1	READ Register2	7D	None	29
NOP	0	1	0	0	0	1	0	0	1	0	1	NOP Instruction	25	None	30
STREAD	0	0	1	Status Read								Status Read			31
MRW Set	0	1	0	0	0	0	0	0	0	0	1	Memory R/W Register Set	01	1 byte	32
CVV	0	1	0	0	0	0	0	0	1	0	0	Control Vout-V0	04	1 byte	33
CATR	0	1	0	0	0	0	0	0	1	1	0	Close Autoread	06	1 byte	34

EEOK	0	1	0	0	0	0	0	0	1	1	1	EEPROM Function Strat	07	1 byte	35

Ext=1															
Command	***A0***	***RD***	***WR***	***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0***	***Function***	***Hex***	***Parameter***	***Index***
Red1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 Red PWM Set	20	16 byte	1
Red2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 Red PWM Set	21	16 byte	2
Red3 Set	0	1	0	0	0	1	0	0	0	1	0	FRAME 3 Red PWM Set	22	16 byte	3
Red4 Set	0	1	0	0	0	1	0	0	0	1	1	FRAME 4 Red PWM Set	23	16 byte	4
Grn1 Set	0	1	0	0	0	1	0	0	1	0	0	FRAME 1 Grn PWM Set	24	16 byte	5
Grn2 Set	0	1	0	0	0	1	0	0	1	0	1	FRAME 2 Grn PWM Set	25	16 byte	6
Grn3 Set	0	1	0	0	0	1	0	0	1	1	0	FRAME 3 Grn PWM Set	26	16 byte	7
Grn4 Set	0	1	0	0	0	1	0	0	1	1	1	FRAME 4 Grn PWM Set	27	16 byte	8
Blu1 Set	0	1	0	0	0	1	0	1	0	0	0	FRAME 1 Blu PWM Set	28	16 byte	9
Blu2 Set	0	1	0	0	0	1	0	1	0	0	1	FRAME 2 Blu PWM Set	29	16 byte	10
Blu3 Set	0	1	0	0	0	1	0	1	0	1	0	FRAME 3 Blu PWM Set	2A	16 byte	11
Blu4 Set	0	1	0	0	0	1	0	1	0	1	1	FRAME 4 Blu PWM Set	2B	16 byte	12
ANASET	0	1	0	0	0	1	1	0	0	1	0	Analog	32	4 byte	13
DITHOFF	0	1	0	0	0	1	1	0	1	0	0	Dithering Circuit Off	34	None	14
DITHON	0	1	0	0	0	1	1	0	1	0	1	Dithering Circuit On	35	None	15
EPCTIN	0	1	0	1	1	0	0	1	1	0	1	Control EEPROM	CD	1 byte	17
EPCOUT	0	1	0	1	1	0	0	1	1	0	0	Cancel EEPROM	CC	None	18
EPMWR	0	1	0	1	1	1	1	1	1	0	0	Write to EEPROM	FC	None	19
EPMRD	0	1	0	1	1	1	1	1	1	0	1	Read from EEPROM	FD	None	20

Ext=1 or Ext=0															
Command	***A0***	***RD***	***WR***	***D7***	***D6***	***D5***	***D4***	***D3***	***D2***	***D1***	***D0***	***Function***	***Hex***	***Parameter***	***Index***
Ext In	0	1	0	0	0	1	1	0	0	0	0	Ext=0 Set	30	None	--
Ext Out	0	1	0	0	0	1	1	0	0	0	1	Ext=1 Set	31	None	--

EXT="0"

(1) Display ON (DISON) Command: 1; Parameter: None (AFH)

It is used to turn the display on. When the display is turned on, segment outputs and common outputs are generated at the level corresponding to the display data and display timing. You can't turn on the display as long as the sleep mode is selected. Thus, whenever using this command, you must cancel the sleep mode first.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	1

(2) Display OFF (DISOFF) Command: 1; Parameter: None (AEH)

It is used to forcibly turn the display off. As long as the display is turned off, every on segment and common outputs are forced to Vss level.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	0

(3) Normal display (DISNOR) Command: 1; Parameter: None (A6H)

It is used to normally highlight the display area without modifying contents of the display data RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	0

(4) Inverse display (DISINV) Command: 1; Parameter: None (A7)

It is used to inversely highlight the display area without modifying contents of the display data RAM. This command does not invert non-display areas in case of using partial display.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	1

(5) Common scan (COMSCAN) Command: 1; Parameter: 1 (BBH)

It is used to specify the direction the common output direction. This command helps increasing degrees of freedom of wiring on the LCD panel.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	0	1	1	–
Parameter1 (P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Command Scan direction

When 1/132 is selected for the display duty, pins and common output are scanned in the order shown below.

P12	P11	P10	Common scan direction				
			COM0 pin		COM65 pin	COM66 pin	COM131 pin
0	0	0	0	**à**	65	66 **à**	131
0	0	1	0	**à**	65	131 **à**	66
0	1	0	65	**à**	0	66 **à**	131
0	1	1	65	**à**	0	131 **à**	66

Common scan direction

Original graphic :

P12:P11:P10:0:0:0 (0 à 65,66 à 131)

P12:P11:P10:0:0:1 (0 à 65, 131 à 66)

P12:P11:P10:0:1:0 (65 à 0, 66 à 131)

P12:P11:P10:0:1:1 (65 à 0, 131 à 66)

(6) Display control (DISCTL) Command: 1; Parameter: 3 (CAH)

This command and succeeding parameters are used to perform the display timing-related setups. This command must be selected before using SLPOUT. Don't change this command while the display is turned on.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	0	0	1	0	1	0	—
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	*	*	CL dividing ratio,F1 and F2 drive pattern.
Parameter2(P2)	1	1	0	0	0	P25	P24	P23	P22	P21	P20	Drive duty
Parameter3(P3)	1	1	0	*	*	*	P34	P33	P32	P31	P30	FR inverse-set value

P1: it is used to specify the CL dividing ratio.

P10, P11: do not use

P14, P13, P12: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.

P14	P13	P12	CL dividing ratio
0	0	0	Not divide
0	0	1	2 divisions
0	1	0	Not divide
0	1	1	Not divide

P2: It is used to specify the duty of the module on block basis.

Duty	*	*	P25	P24	P23	P22	P21	P20	(Numbers of display lines)/4-1
Example: 1/128 duty	0	0	0	1	1	1	1	1	128/4-1=31

P3: It is used to specify number of lines to be inversely highlighted on LCD panel from P33 to P30 (lines can be inversely highlighted in the range of 2 to 16)

Inversely highlighted line	*	*	*	P34	P33	P32	P31	P30	Inversely highlighted lines-1
Example: 11H	0	0	0	0	1	0	1	0	11-1=10
Example: 13H	0	0	0	1	1	1	0	0	13-1=12

In the default, 11H inverse highlight is selected.

P34="0": Inversion occur every frame. P34="1": Independent from frames.

(7) Sleep in (SPLIN) Command: 1; Parameter: None (95H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	1

(8) Sleep out (SLPOUT) Command: 1;Parameter: None (94H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	0

(9) Page address set (PASET) Command: 1; Parameter: 2 (75H)

When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the page address area. As the addresses are incremented from the start to the end page in the page-direction scan, the column address is incremented by 1 and the page address is returned to the start page. Note that the start and end page must be specified as a pair. Also, the relation “start page <end page” must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	1	1	0	1	0	1	–
Parameter1(P1)	1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Start page
Parameter2(P2)	1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	End page

(10) Column address set (CASET) Command: 1; Parameter: 2 (15H)

When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the column address area. As the addresses are incremented from the start to the end column in the column-direction scan, the page address is incremented by 1 and the column address is returned to the start column. Note that the start and end page must be specified as a pair. Also, the relation “start column <end column” must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	1	0	1	0	1	–
Parameter1(P1)	1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Start address
Parameter2(P2)	1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	End address

(11) Data control (DATCTL) Command: 1;Parameter: 3 (BCH)

This command and succeeding parameters are used to perform various setups needed when MPU operates display data stored on the built-in RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	1	0	0	–
Parameter1(P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Normal/Reverse display of page address and page-address scan direction.
Parameter2(P2)	1	1	0	*	*	*	*	*	*	*	P20	RGB arrangement
Parameter3(P3)	1	1	0	*	*	P35	P34	P33	P32	P31	P30	Gray-scale setup

P1: It is used to specify the normal or inverse display of the page address and also to specify the page address scanning direction.

P10: Normal/Reverse display of the page address. P10=0: Normal and P10=1: Reverse

P11: Normal/Reverse turn of column address. P11=0: Normal rotation and P11=1: Reverse rotation.

P12: Address-scan direction. P12=0: In the column direction and P12=1: In the page direction.

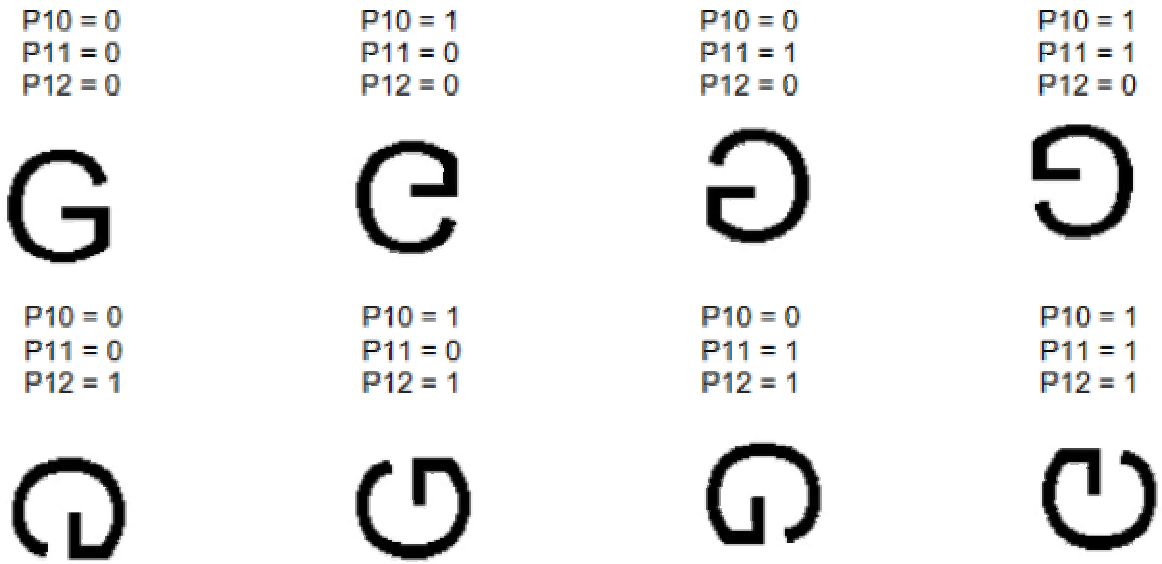
Page address and page-address scan direction.

P12=0 Column direction

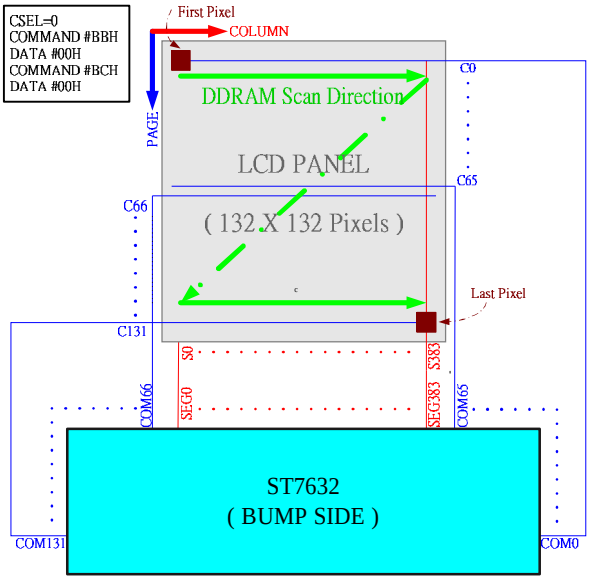
P11=0		0	1	2		129	130	131
P11=1		131	130	129		2	1	0
P10=0	P10=1							
0	131							
1	130							
2	129							
129	2							
130	1							
131	0							

P12=1 Page direction

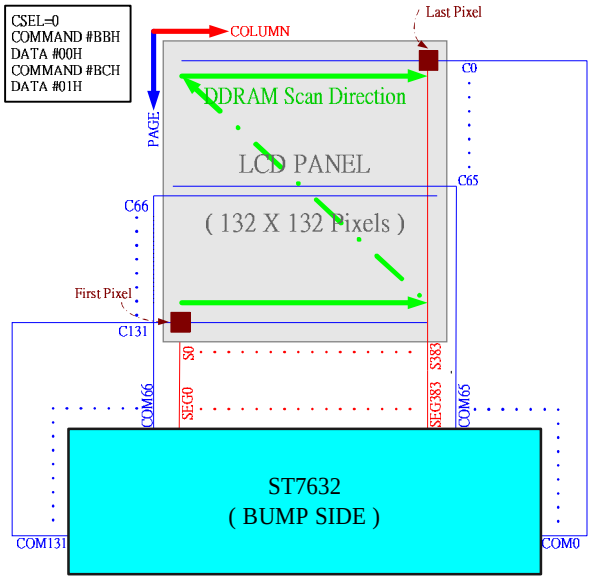
P11=0		0	1	2		129	130	131
P11=1		131	130	129		2	1	0
P10=0	P10=1							
0	131							
1	130							
2	129							
129	2							
130	1							
131	0							



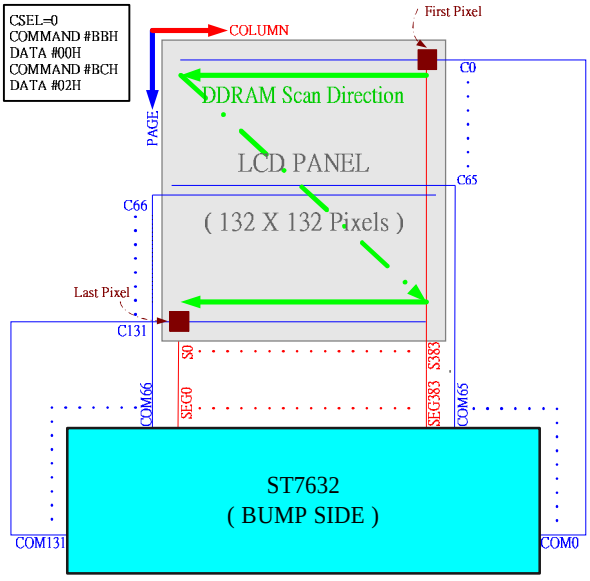
Examples of Normal or Inverse page/column scan direction



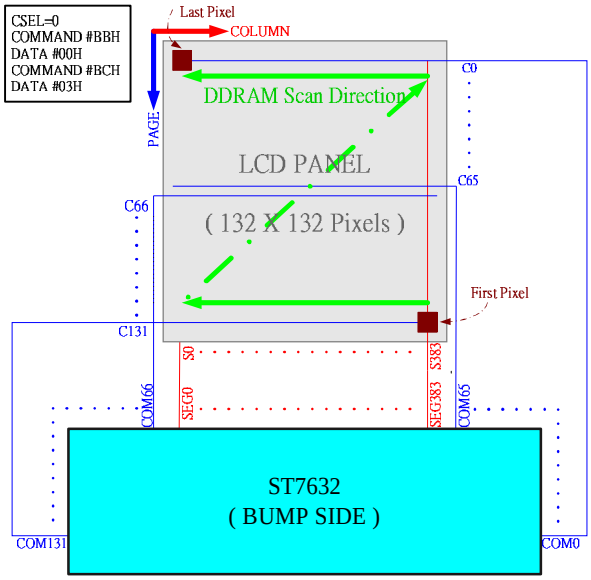
(a) COMMAND #BCH, DATA #00H



(b) COMMAND #BCH, DATA #01H

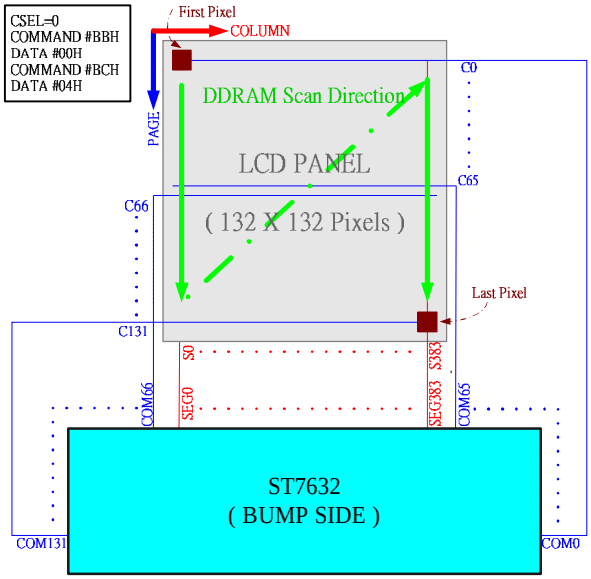


(c) COMMAND #BCH, DATA #02H

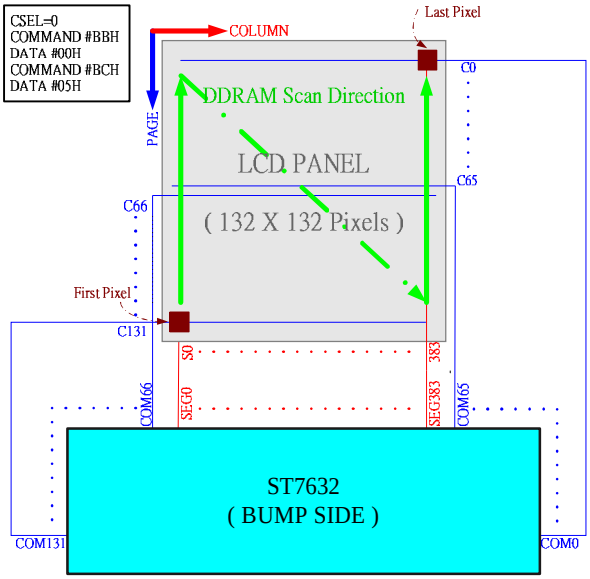


(d) COMMAND #BCH, DATA #03H

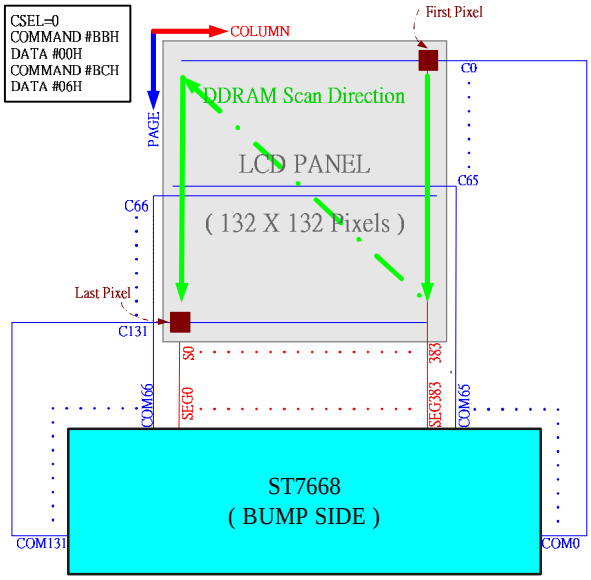
Different RAM accessing setupunder COMMAND #BBH, DATA #00H
(a) COMMAND #BCH, DATA #00H
(b) COMMAND #BCH, DATA #01H
(c) COMMAND #BCH, DATA #02H
(d) COMMAND #BCH, DATA #03H



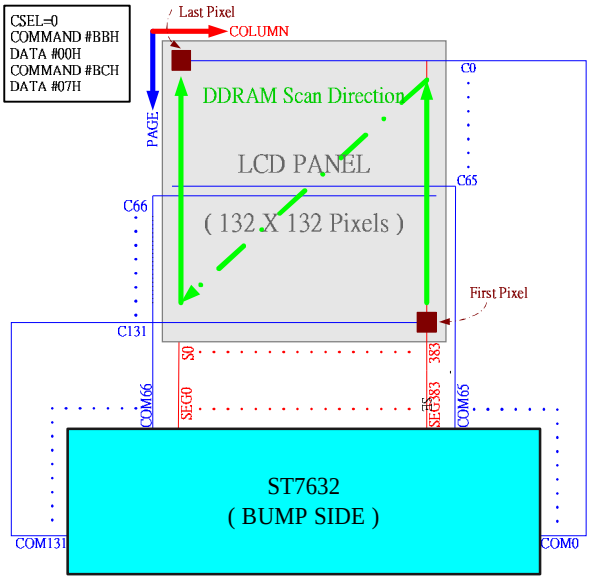
(e) COMMAND #BCH, DATA #04H



(f) COMMAND #BCH, DATA #05H



(g) COMMAND #BCH, DATA #06H



(h) COMMAND #BCH, DATA #07H

Figure 8.2.3 Different RAM accessing setup when CSEL=0 under COMMAND #BBH, DATA #00H (continue)
(e) COMMAND #BCH, DATA #04H
(f) COMMAND #BCH, DATA #05H
(g) COMMAND #BCH, DATA #06H

P2: RGB arrangement. This parameter allows you to change RGB arrangement of the segment output according to RGB arrangement on the LCD panel. In this case, writing position of data {R=(D7, D6, D5), G=(D4, D3, D2), B=(D1, D0)} on the display memory is changed.

P20	Line	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	…	SEG395
0	Even page	R	G	B	R	G	B	R	G	…	B
	Odd page	R	G	B	R	G	B	R	G	…	B
1	1	B	G	R	B	G	R	B	G	…	R
	2	B	G	R	B	G	R	B	G	…	R

P3: Gray scale setup. Using this parameter, you can a select desired display colors between the 256 colors (8 gray-scale) or 4096 colors (16 gray-scales) for the display color. For 16 gray-scale display, you can select the Type A, Type B, 65K, 262K, and 16M display mode depending on the difference in RGB data arrangement.

P35	P34	P33	P32	P31	P30	Numbers of gray-scale
0	0	0	0	0	1	8 gray-scale
0	0	0	1	0	0	16 gray-scale display 4K
0	0	1	0	0	0	16-gray 65K
0	1	0	0	0	0	16-gray 262K
1	0	0	0	0	0	16-gray 16M

(12) 256-color position set (RGBSET8) Command: 1;Parameter: 20 (CEH)

When turning on 256-color display (8 gray-scale), this command allows you to choose colors to represent each of red, green and blue from 4096 colors.

	A0	**RD**	**RW**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Function**
Command	0	1	0	1	1	0	0	1	1	1	0	--
Parameter(P1)	1	1	0	*	*	*	*	P13	P12	P11	P10	Intermediate red tone 000
Parameter(P8)	1	1	0	*	*	*	*	P83	P82	P81	P80	Intermediate red tone 111
Parameter(P9)	1	1	0	*	*	*	*	P93	P92	P91	P90	Intermediate green tone 000
Parameter(P16)	1	1	0	*	*	*	*	P163	P162	P161	P160	Intermediate green tone 111
Parameter(P17)	1	1	0	*	*	*	*	P173	P172	P171	P170	Intermediate blue tone 00
Parameter(P20)	1	1	0	*	*	*	*	P203	P202	P201	P200	Intermediate blue tone 11

Data (Red and Green: 3 bits and Blue: 2 bits) to be written from MPU to the DDRAM are converted to 4-bit data before the write operation takes place. When reading data from the DDRAM, data on red and green are converted to 3 bits and that on blue are converted 2 bits before the output.

(13) Memory write (RAMWR) Command: 1;Parameter: Numbers of data written (5CH)

When MPU writes data to the display memory, this command turns on the data entry mode. Entering this command always sets the page and column address at the start address. You can rewrite contents of the display data RAM by entering data succeeding to this command. At the same time, this operation increments the page or column address as applicable. The write mode is automatically cancelled if any other command is entered.

1. 8-bit bus

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	0	–
Parameter	1	1	0	Data to be written								Data to be written

2. 16-bit bus

	A0	RD	RW	D15	D14	…	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	…	*	*	0	1	0	1	1	1	0	0	Memory write
parameter	1	1	0	Data to be written													Write date

(14) Memory read (RAMRD) Command: 1; Parameter: Numbers of data read (5DH)

When MPU read data from the display memory, this command turns on the data read mode. Entering this command always sets the page and column address at the start address. After entering this command, you can read contents of the display data RAM. At the same time, this operation increments the page or column address as applicable. The data read mode is automatically cancelled if any other command is entered.

1. 8-bit bus

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	1	--
Parameter	1	0	1	Data to be read								Data to be read

2. 16-bit bus

	A0	RD	RW	D15	D14	….	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	*	*	*	0	1	0	1	1	1	0	1	Memory read
parameter	1	0	1	Data to be read													Read date

(15) Partial in (PTLIN) Command: 1; Parameter: 2 (A8H)

This command and succeeding parameters specify the partial display area. This command is used to turn on partial display of the screen (dividing screen by lines) in order to save power. Since ST7632 processes the liquid crystal display signal on 4-line basis (block basis), the display and non-display areas are also specified on 4-bit line (block basis).

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	0	0	--
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Start block address
Parameter(P2)	1	1	0	*	*	P25	P24	P23	P22	P21	P20	End block address

A block address that can be specified for the partial display must be the display one (don't try to specify an address not to be displayed when scrolled).

(16) Partial out (PTLOUT) Command: 1; Parameter: 0 (A9H)

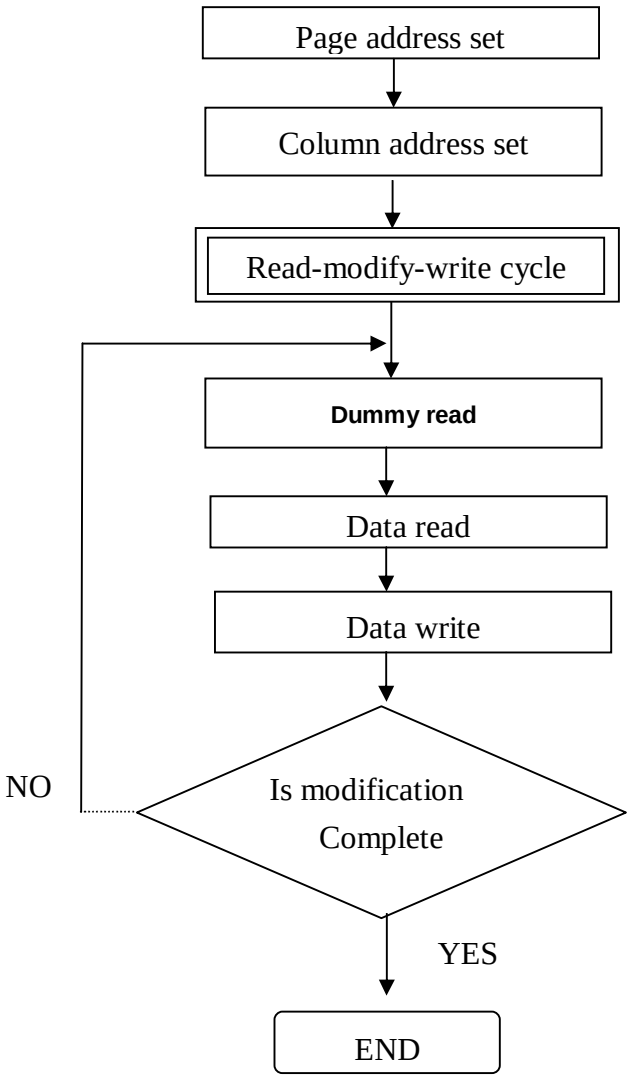
This command is used to exit from the partial display mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	0	0	1

(17) Read modify write in (RMWIN) Command: 1; Parameter: 0 (E0H)

This command is used along with the column address set command, page address set command and read modify write out command. This function is used when frequently modifying data to specify a specific display area such as blinking cursor. First set a specific display area using the column and page address commands. Then, enter this command to set the column and page addresses at the start address of the specific area. When this operation is complete, the column (page) address won't be modified by the display data read command. It is incremented only when the display data write command is used. You can cancel this mode by entering the read modify write out or any other command

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	0	0	0



(18) Read modify write out (RMWOUT) Command: 1; Parameter: 0 (EEH)

Enter this command cancels the read modify write mode

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	1	1	1	0

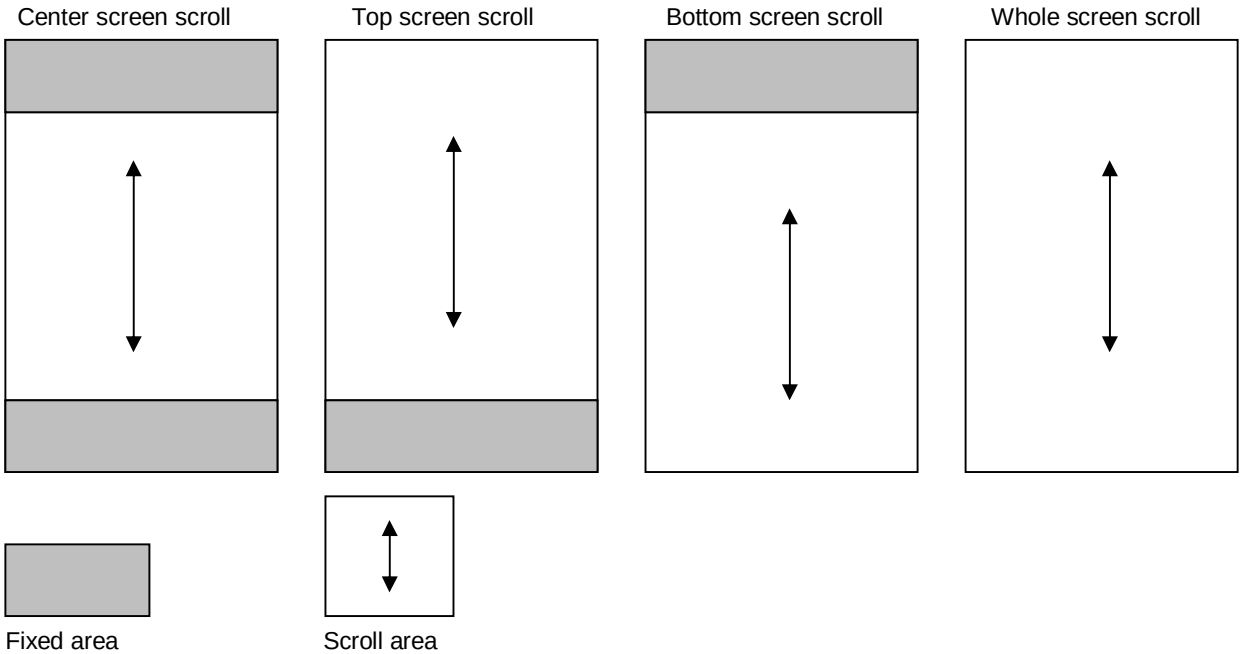
(19) Area scroll set (ASCSET) Command: 1; Parameter: 4 (AAH)

It is used when scrolling only the specified portion of the screen (dividing the screen by lines). This command and succeeding parameters specify the type of area scroll, FIX area and scroll area.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	0	--
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Top block address
Parameter(P2)	1	1	0	*	*	P25	P24	P23	P22	P21	P20	Bottom block address
Parameter(P3)	1	1	0	*	*	P35	P34	P33	P32	P31	P30	Number of specified blocks
Parameter(P4)	1	1	0	*	*	*	*	*	*	P41	P40	Area scroll mode

P4: It is used to specify an area scroll mode.

P41	P40	Type of area scroll
0	0	Center screen scroll
0	1	Top screen scroll
1	0	Bottom screen scroll
1	1	Whole screen scroll



Since ST7632 processes the liquid crystal display signals on the four-line basis (block basis), FIX and scroll areas are also specified on the four-line basis (block basis).

DDRAM address corresponding to the top FIX area is set in the block address incrementing direction starting with 0 block. DDRAM address corresponding to the bottom FIX area is set in the block address decreasing direction starting with 41st block. Other DDRAM blocks excluding the top and bottom FIX areas are assigned to the scroll + background areas.

P1: It is used to specify the top block address of the scroll+ background areas. Specify the 0th block for the top screen scroll or whole screen scroll.

P2: It specifies the bottom address of the scroll+ background areas. Specify the 32th block for the bottom or whole screen scroll.

Required relation between the start and end blocks (top block address<bottom block address) must be maintained.

P3: It specifies a specific number of blocks {Numbers of (Top FIX area +Scroll area) block-1}. When the bottom scroll or whole screen scroll, the value is identical with P2.

You can turn on the area scroll function by executing the area scroll set command first and then specifying the display start block of the scroll area with the scroll start set command.

[Area Scroll Setup Example]

In the center screen scroll of 1/120 duty (display range: 120 lines=30 blocks), if 8 lines=2 blocks and 8 lines=2 blocks are specified for the top and bottom FIX areas, 104 lines =26 blocks is specified for the scroll areas, respectively, 12 lines = 3 blocks on the DDRAM are usable as the background area. Value of each parameter at this time is as shown below.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	
P1	1	1	0	*	*	0	0	0	0	1	0	Top block address = 2
P2	1	1	0	*	*	0	1	1	1	1	0	Bottom block address = 30
P3	1	1	0	*	*	0	1	1	0	1	1	Number of specific blocks = 27
P4	1	1	0	*	*	*	*	*	*	0	0	Area scroll mode = center

(20) Scroll start address set (SCSTART) Command:1 Parameter: 1 (ABH)

This command and succeeding parameters are used to specify the start block address of the scroll area. Note that you must execute this command after executing the area scroll set command. Scroll becomes available by dynamically changing the start block address.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	1	--
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Start block address

(21) Internal oscillation on (OSCON) Command: 1; Parameter: 0 (D1H)

This command turns on the internal oscillation circuit. It is valid only when the internal oscillation circuit of CLS = HIGH is used.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	0	1

(22) Internal oscillation off (OSOFF) Command: 1; Parameter: 0 (D2H)

It turns off the internal oscillation circuit. This circuit is turned off in the reset mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	1	0

(23) Power control set (PWRCTR) Command: 1; Parameter: 1 (20H)

This command is used to turn on or off the Booster circuit, voltage regulator circuit, and follower voltage.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	1	0	0	0	1	0	0	0	0	--
Parameter(P1)	1	1	0	*	*	*	*	P13	*	P11	P10	LCD drive power

P10: It turns on or off the regulator circuit.

P10 = “1”: ON. P10 =” 0”: OFF

P11: It turns on or off the follower circuit.

P11 = “1”: ON. P11 =” 0”: OFF

P12: can not use

P13:It turns on or off the booster circuit.

P13 = “1”: ON. P13 =” 0”: OFF

(24) Electronic volume control (VOLCTR) Command: 1; Parameter: 2 (81H)

The command is used to program the optimum LCD supply voltage V_{LCD}. Reference to 7.10.2

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	0	0	0	0	0	1	--
Parameter(P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Set Vop[5:0]
Parameter(P2)	1	1	0	*	*	*	*	*	P18	P17	P16	Set Vop[8:6]

(25) Increment electronic control (VOLUP) Command: 1; Parameter: 0 (D6H)

With the VOLUP and VOLDOWN command the V_{LCD} voltage and therewith the contrast of the LCD can be adjusted.

This command increments electronic control value Vop[5:0]of voltage regulator circuit by 1.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	0

If you set the electronic control value to 111111, the control value is set to 000000 after this command has been executed.

(26) Decrement electronic control (VOLDOWN) Command: 1; Parameter: 0 (D7H)

With the VOLUP and VOLDOWN command the V_{LCD} voltage and therewith the contrast of the LCD can be adjusted.

This command decrements electronic control value Vop[5:0]of voltage regulator circuit by 1.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	1

If you set the electronic control value to 000000, the control value is set to 111111 after this command has been executed.

Table 8.1.1 Possible Vop[5:0] values

Electronic Control Value	Decimal Equivalent	VLCD Offset
111111	31	+1240 mV
111110	30	+1200 mV
111101	29	+1160 mV
…	…	…
000010	2	+80 mV
000001	1	+40 mV
000000	0	0 mV
111111	-1	-40 mV
111110	-2	-80 mV
…	…	…
100010	-30	-1200 mV
100001	-31	-1240 mV
100000	-32	-1280mV

(27) Reserved (82H)

Do not use this command

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	0	0	0	1	0

(28) Read Register 1 (EPSRRD1) Command: 1; Parameter: 0 (7CH)

Issue the EPSRRD1 and STREAD (Status Read) commands in succession to read the Electronic Control value.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	0

Issue the Status Read command immediately after this command. Also, always issue the NOP command after the STREAD (Status Read) command.

(29) Read Register 2 (EPSRRD2) Command: 1 ;Parameter: 0 (7DH)

Issue the EPSRRD1 and STREAD (Status Read) commands in succession to read the built-in resistance ratio.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	1

Issue the Status Read command immediately after this command. Also, always issue the NOP command after the STREAD (Status Read) command.

(30) Non-operating (NOP) Command: 1; Parameter: 0 (25H)

This command does not affect the operation.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	0	0	1	0	1

This command, however, has the function of canceling the IC test mode. Thus, it is recommended to enter it periodically to prevent malfunctioning due to noise and such.

(31) Status read (STREAD) Command: 1; Parameter: None

It is the command for reading the internal condition of the IC. One status can be displayed depending on the setting.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	0	1	Status data							

Status after reset or after NOP operation

D7: Area scroll mode	Refer to P41 (ASCSET)	
D6: Area scroll mode	Refer to P40 (ASCSET)	
D5: RMW on/off	0 : Out	1 : In
D4: Scan direction	0 : Column	1 : Page
D3: Display ON/OFF	0 : OFF	1 : ON
D2: EEPROM access	0: OutAccess	1: InAccess
D1: Display normal/inverse	0 : Inverse	1 : Normal
D0: Partial display	0 : OFF	1 : ON

(32) Memory R/W Register Set (MRW Set) Command: 1; Parameter: 1 (01H)

This command can set memory read/write register.It must be issued in the initial flow and set parameter =F0H.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	0	0	0	1	--
Parameter(P1)	1	1	0	1	1	1	1	0	0	0	0	F0H

(33) Control Vout V0(CVV) Command: 1; Parameter: 1 (04H)

Using this command can control the relationship of VOUT and V0. It must be issued in the initial flow and set parameter =04H.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	0	1	0	0	--
Parameter(P1)	1	1	0	0	0	0	0	0	1	1	0	06H

(34) Close Autoread (CATR) Command: 1; Parameter: 1 (06H)

This command is used for closing the autoread function of EEPROM. It must be issued in the initial flow and set parameter =41H.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	1	1	0	0	--
Parameter(P1)	1	1	0	0	1	0	0	0	0	0	1	41H

(35) EEPROM Function Strat(EEOK) Command:1;Parameter:1(07)

In the OTP read flow,this command can increase the clock of EEPROM.It must be issued in the initial flow and set parameter=1BH.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	0	0	1	1	1	--
Parameter(P1)	1	1	0	0	0	0	1	1	0	1	1	1BH

EXT="1"

(1)Set Red 1 value (Red1 set) Command: 1; Parameter: 16 (20H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set red level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 1st frame

(2)Set Red 2 value (Red2 set) Command: 1; Parameter: 16 (21H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 2nd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 2nd frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set red level 13 and 2nd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 2nd frame

(3) Set Red 3 value (Red3 set) Command: 1; Parameter: 16 (22H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red3 Set	0	1	0	0	0	1	0	0	0	1	0	FRAME 3 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 3rd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 3rdframe
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set red level 13 and 3rd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 3rd frame

(4) Set Red 4 value (Red4 set) Command: 1; Parameter: 16 (23H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Red4 Set	0	1	0	0	0	1	0	0	0	1	1	FRAME 4 Red PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set red level 0 and 4th frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set red level 1 and 4thframe
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set red level 13 and 4th frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set red level 15 and 4th frame

The default value of Red level set

	RED1SET	RED2SET	RED3SET	RED4SET
	FRAM1	FRAM2	FRAM3	FRAME4
red level0	00	00	00	00
red level1	03	03	03	03
red level2	06	06	06	06
red level3	08	08	08	09
red level4	0B	0B	0B	0C
red level5	0E	0E	0E	0D
red level6	10	11	10	11
red level7	12	13	12	13
red level8	14	15	14	15
red level9	17	17	17	16
red level10	19	19	19	18
red level11	1A	1B	1A	1B
red level12	1C	1C	1C	1B
red level13	1D	1D	1D	1E
red level14	1E	1E	1E	1F
red level15	1F	1F	1F	1F

(5) Set Green 1 value (Grn1 set) Command: 1; Parameter: 16 (24H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn 1 Set	0	1	0	0	0	1	0	0	1	0	0	FRAME 1 Grn PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set green level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 1st frame

(6) Set Green 2 value (Grn2 set) Command: 1;Parameter: 16 (25H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn2 Set	0	1	0	0	0	1	0	0	1	0	1	FRAME 2 Grn PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 2nd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 2nd frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set green level 13 and 2nd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 2nd frame

(7) Set Green 3 value (Grn3 set) Command: 1; Parameter: 16 (26H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn3 Set	0	1	0	0	0	1	0	0	1	0	1	FRAME 3 Grn PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 3rd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 3rdframe
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set green level 13 and 3rd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 3rd frame

(8) Set Green 4 value (Grn4 set) Command: 1;Parameter: 16 (27H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn4 Set	0	1	0	0	0	1	0	0	1	1	1	FRAME 4 Grn PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set green level 0 and 4th frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set green level 1 and 4thframe
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set green level 13 and 4th frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set green level 15 and 4th frame

The default value of Green level set

	GRN1SET	GRN2SET	GRN3SET	GRN4SET
	FRAM1	FRAM2	FRAM3	FRAME4
green level0	00	00	00	00
green level1	03	03	03	03
green level2	06	06	06	06
green level3	08	08	08	09
green level4	0B	0B	0B	0C
green level5	0E	0E	0E	0D
green level6	10	11	10	11
green level7	12	13	12	13
green level8	14	15	14	15
green level9	17	17	17	16
green level10	19	19	19	18
green level11	1A	1B	1A	1B
green level12	1C	1C	1C	1B
green level13	1D	1D	1D	1E
green level14	1E	1E	1E	1F
green level15	1F	1F	1F	1F

(9) Set Blue 1 value (Blu 1 set) Command: 1; Parameter: 16 (28H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn 1 Set	0	1	0	0	0	1	0	0	1	0	0	FRAME 1 Blu PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 1st frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 1st frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set blue level 13 and 1st frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 1st frame

(10) Set Blue 2 value (Blu2 set) Command: 1; Parameter: 16 (29H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn2 Set	0	1	0	0	0	1	0	0	1	0	1	FRAME 2 Blu PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 2nd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 2nd frame
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set blue level 13 and 2nd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 2nd frame

(11) Set Blue 3 value (Blu3 set) Command: 1; Parameter: 16 (2AH)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn3 Set	0	1	0	0	0	1	0	0	1	1	0	FRAME 3 Blu PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 3rd frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 3rdframe
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set blue level 13 and 3rd frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 3rd frame

(12) Set Blue 4 value (Blu4 set) Command: 1; Parameter: 16 (2BH)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Grn4 Set	0	1	0	0	0	1	0	0	1	1	1	FRAME 4 Blu PWM Set

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	–
Parameter1(P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	Set blue level 0 and 4th frame
Parameter2(P2)	1	1	0	*	*	*	P24	P23	P22	P21	P20	Set blue level 1 and 4thframe
Parameter14(P14)	1	1	0	*	*	*	P144	P143	P142	P141	P140	Set blue level 13 and 4th frame
Parameter16(P16)	1	1	0	*	*	*	P164	P163	P162	P161	P160	Set blue level 15 and 4th frame

The default value of Blue level set

	GRN1SET	GRN2SET	GRN3SET	GRN4SET
	FRAM1	FRAM2	FRAM3	FRAME4
blue level0	00	00	00	00
blue level1	03	03	03	03
blue level2	06	06	06	06
blue level3	08	08	08	09
blue level4	0B	0B	0B	0C
blue level5	0E	0E	0E	0D
blue level6	10	11	10	11
blue level7	12	13	12	13
blue level8	14	15	14	15
blue level9	17	17	17	16
blue level10	19	19	19	18
blue level11	1A	1B	1A	1B
blue level12	1C	1C	1C	1B
blue level13	1D	1D	1D	1E
blue level14	1E	1E	1E	1F
blue level15	1F	1F	1F	1F

(13) ANASET Command 1; Parameter: 4 (32H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	1	0	0	1	0	–
Parameter1(P1)	1	1	0	*	*	*	*	*	P12	P11	P10	OSC frequency Adjustment
Parameter2(P2)	1	1	0	*	*	*	*	*	*	P21	P20	Booster Efficiency Set
Parameter3(P3)	1	1	0	*	*	*	*	*	P32	P31	P30	Booster setting
Parameter4(P4)	1	1	0	*	*	*	*	*	P42	P41	P40	Bias setting

P1: Oscillator frequency adjustment (vdd=2.8V)

P12	P11	P10	CL(kHz)
0	0	0	10
0	0	1	10.5
0	1	0	11.5
0	1	1	13
1	0	0	15
1	0	1	17
1	1	0	20.5
1	1	1	25.5

FRAME=CL/(1/DUTY+1)

Ex:1/132 duty,(P12,P11,P10)=(0,0,0) , Frame=10k/(132+1)=75.19Hz

P2: Booster Efficiency set (vdd=2.8v)

P21	P20	Frequency(kHz)
0	0	1000
0	1	840
1	0	650
1	1	450

P3: Booster setting

P32	P31	P30	
0	0	0	Booster off
0	0	1	2 times boosting circuit
0	1	0	3 times boosting circuit
0	1	1	4 times boosting circuit
1	0	0	5 times boosting circuit
1	0	1	6 times boosting circuit
1	1	0	7 times boosting circuit
1	1	1	8 times boosting circuit

P4: Select LCD bias ratio of the voltage required for driving the LCD.

P42	P41	P40	LCD bias
0	0	0	1/12
0	0	1	1/11
0	1	0	1/10
0	1	1	1/9
1	0	0	1/8
1	0	1	1/7
1	1	0	1/6
1	1	1	1/5

(14) Color Dither OFF (DITHOFF) Command: 1; Parameter: None (34H)

Turn off the dithering circuit.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	1	0	0

(15) Color Dither ON (DITHON) Command: 1; Parameter: None (35H)

Turn on the dithering circuit.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	1	0	1

(16) Control EEPROM:1 Parameter: 1 (CDH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	1
Parameter (P1)	1	1	0	*	*	P15	*	*	*	*	*

P15: when setting “1” **è** The Write Enable of EEPROM will be opened.

P15: when setting “0” **è** The Read Enable of EEPROM will be opened.

(17) Cancel EEPROM Command: 1;Parameter : None (CCH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	0

(18) Write data to EEPROM (EPMWR) Command: 1; Parameter: None (FCH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	0

(19) Read data from EEPROM (EPMWR) Command: 1; Parameter: None (FDH)

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	1

EXT="1" or "0"

(1) Extension instruction disable (EXT IN) Command:1 Parameter: None (30H)

Use the "Ext=0" command table

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	0

(2) Extension instruction enable (EXT OUT) Command:1 Parameter: None (31H)

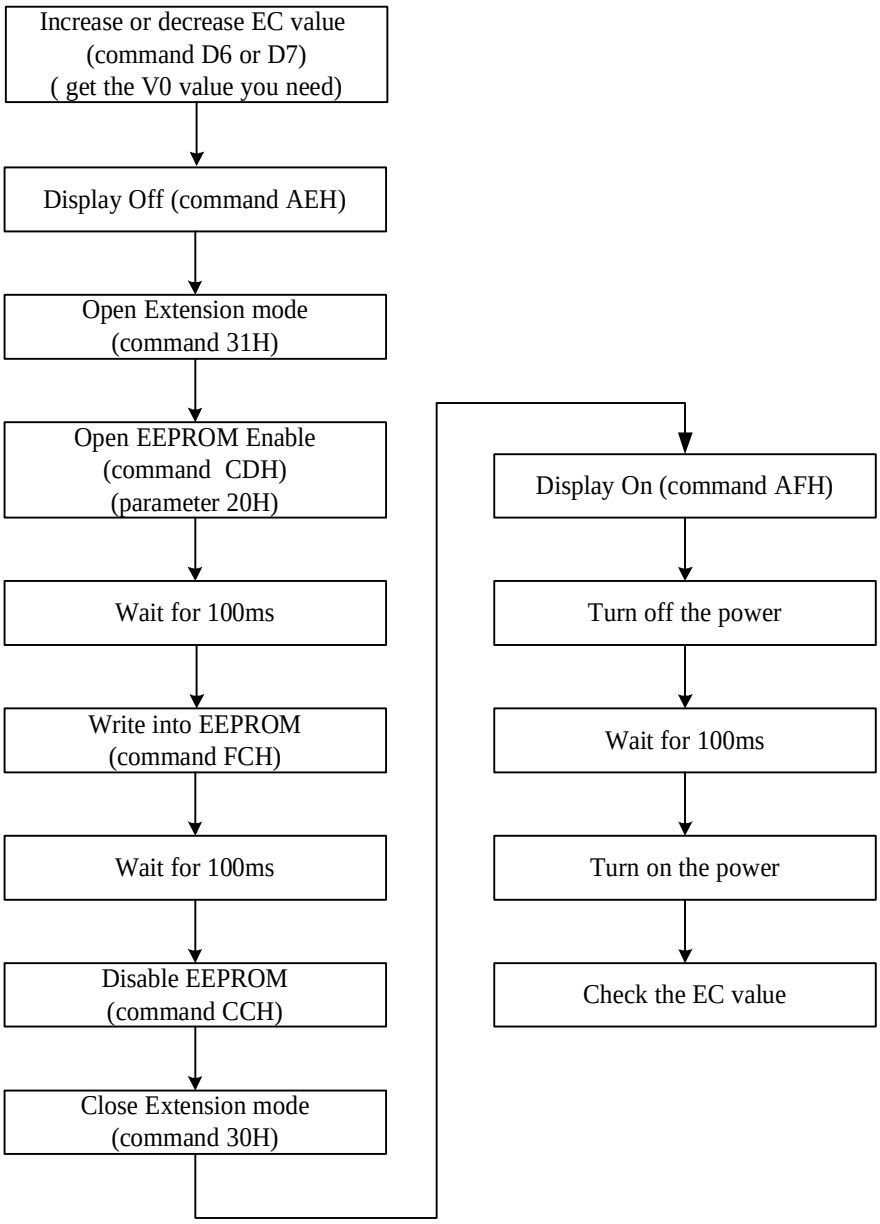
Use the extended command table (EXT="1")

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	1

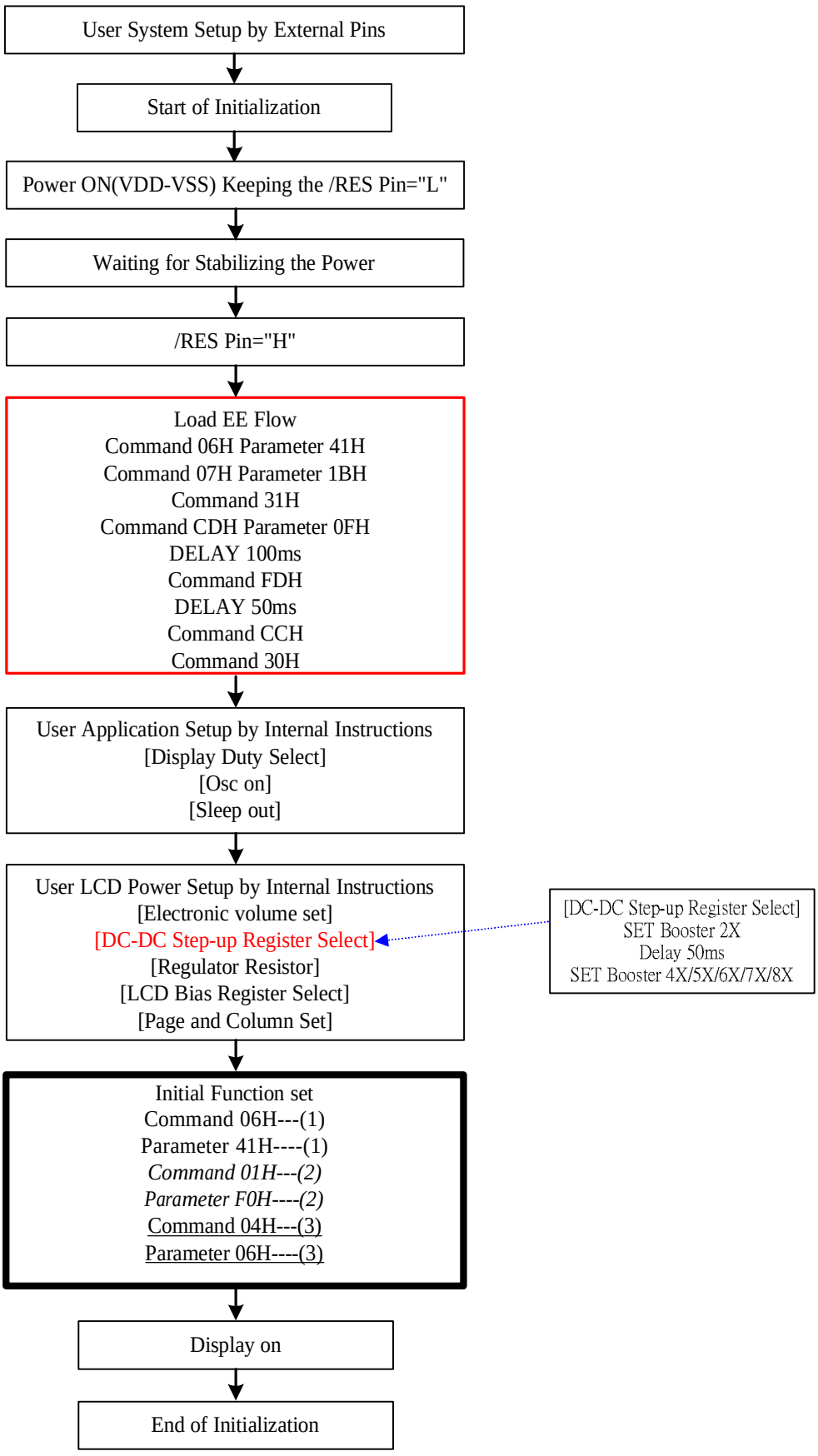
EEPROM Setting Following

The ST7632 chip provides the Write and Read function to write the Electronic Control value and Built-in resistance ratio into and read them from the built-in EEPROM. Using the Write and Read functions, you can store these values appropriate to each LCP panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.

Note: When writing value to EEPROM, the voltage of Voutin must be more than 16V.



Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits



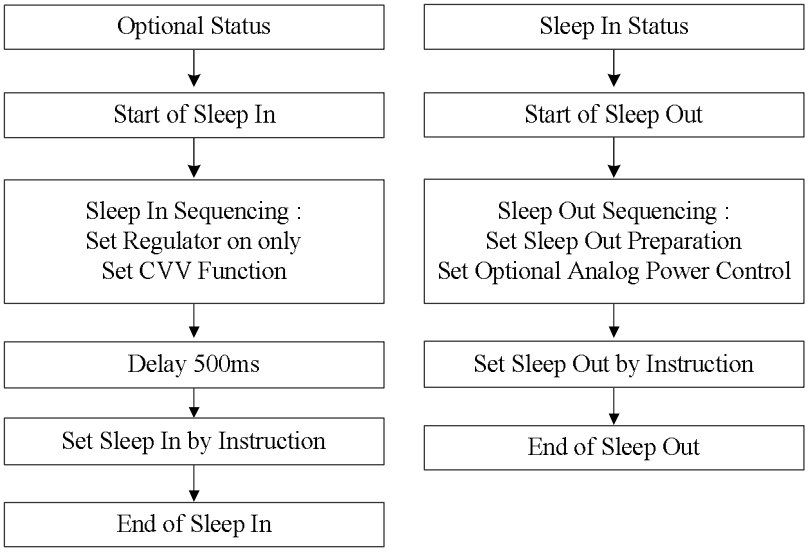
Initializing with the Built-in Power Supply Circuits

Example： 128X128 INITIAL FLOW

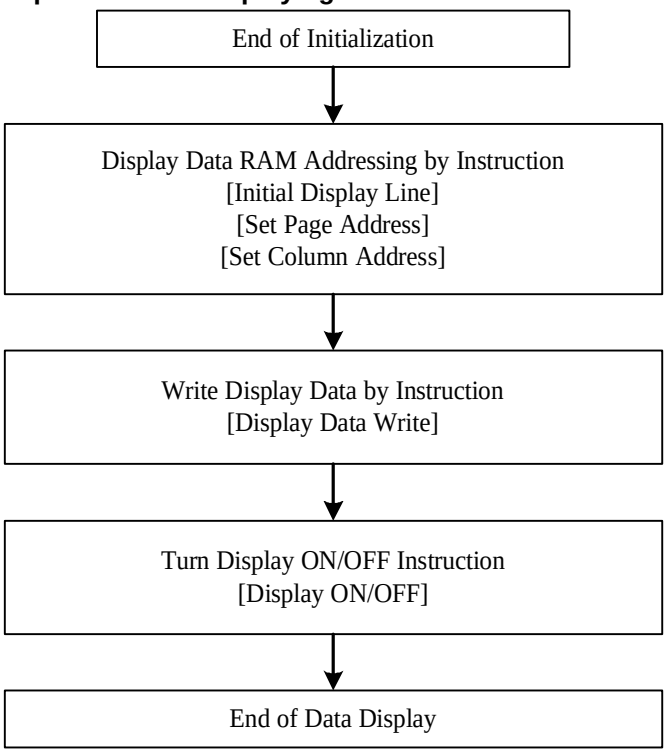
```
;;;;;;;;;;;;OTP READ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        COMMAND #06H                        ;INITIAL FUNCTION(1)
        PARA    #41H                        ;
                                            ;
        COMMAND #07H                        ;START OTP
        PARA    #1BH                        ;
                                            ;
        COMMAND #31H                        ;SET    EXT=1
        COMMAND #CDH                        ;CONTROL EEPROM ENABLE
        PARA    #0FH                        ;READ ENABLE
        CALL    DELAY_100MS                 ;
        COMMAND #FDH                        ;READ EEPROM
        CALL    DELAY_50MS                  ;
        COMMAND #CCH                        ;DISABLE EEPROM
        COMMAND #30H                        ;
;;;;;;;;;;;;;INITIAL LCD;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        COMMAND #CAH                        ;DISPLAY CONTROL (DISCTL)
        PARA    #00000000B                  ;CL DIVIDINB RATIO
        PARA    #00011111B                  ;DRIVE DUTY (DUTY)/4-1
        PARA    #00000000B                  ;
                                            ;
        COMMAND #D1H                        ;TURN ON OSC
                                            ;
        COMMAND #94H                        ;SLEEP OUT
                                            ;
        COMMAND #81H                        ;ELECTRONIC VOLUME CONTROL
        PARA    #00011111B                  ;B5~B0==>VPR8~VPR5
        PARA    #00000011B                  ;B2~B0==>RA/RB RATIO
                                            ;
        COMMAND #20H                        ;POWER CONTROL
        PARA    #00001111B                  ;B0:R,B1:F,B3:B,B2,B4:DON'T USE
                                            ;
        COMMAND #31H                        ;SET EXT=1 (OPEN EXT)
                                            ;
        COMMAND #32H                        ;ANALOG SET
        PARA    #00000000B                  ;B2~B0==> OSC FREQUENCY ADJUSTMENT
        PARA    #00000011B                  ;B1~B0==> BOOSTER EFFICIENY SET
        PARA    #00000001B                  ;B2~B0==>BOOSTER SET (2X)
        PARA    #00000000B                  ;B2~B0==>BIAS SET

        COMMAND #32H                        ;ANALOG SET
        PARA    #00000000B                  ;B2~B0==> OSC FREQUENCY ADJUSTMENT
        PARA    #00000011B                  ;B1~B0==> BOOSTER EFFICIENY SET
        PARA    #00000101B                  ;B2~B0==>BOOSTER SET (6X)
        PARA    #00000000B                  ;B2~B0==>BIAS SET
                                            ;
        COMMAND #30H                        ;SET EXT=0 (CLOSE EXT)
                                            ;
        COMMAND #BCH                        ;DATA CONTROL
        PARA    #00000011B                  ;USE B2~B0
        PARA    #00000000B                  ;USE B0==>0==>RGB,B0==>1==>BGR
        PARA    #00000100B                  ;16 GRAY-SCALE DISPLAY TYPE B,4096
                                            ;
        COMMAND #BBH                        ;COM DIRECTION
        PARA    #00000001B                  ;
                                            ;
```

```
        COMMAND #75H                            ;PAGE ADDRESS SET
        PARA    #00000000B                      ;B7~B0==>START PAGEPARA
        PARA    #128                            ;;B7~B0==>STOP PAGE
                                                ;
        COMMAND #15H                            ;COLUMN ADDRESS SET
        PARA    #00000000B                      ;B7~B0==>START COLUMN
        PARA    #128                            ;B7~B0==>STOP COLUMN(B)
        COMMAND #A7H                            ;INVERSE DISPLAY
;       COMMAND #A6H                            ;NORMAL DISPLAY
;;;
```

Sleep In/Out

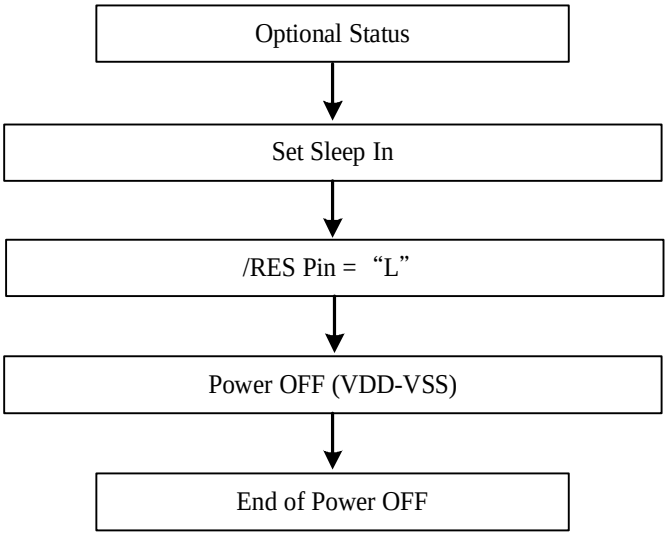


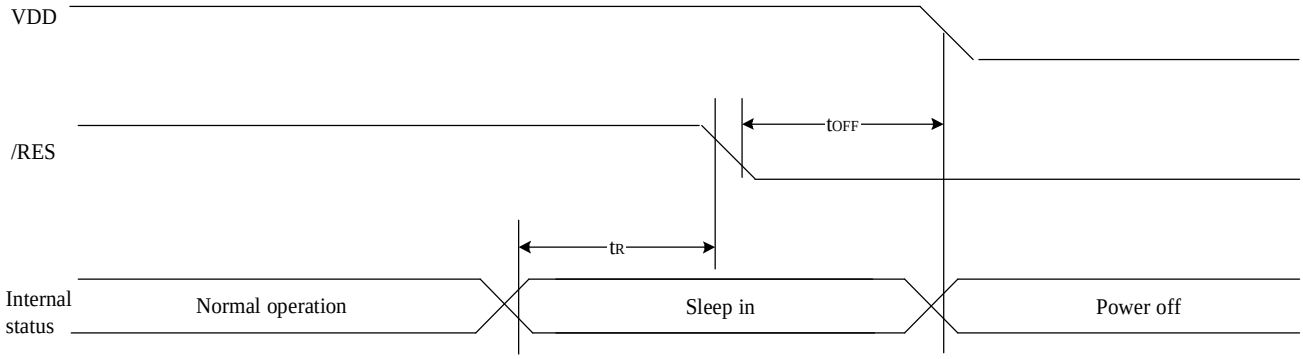
Referential Instruction Setup Flow: Data Displaying



Data Displaying

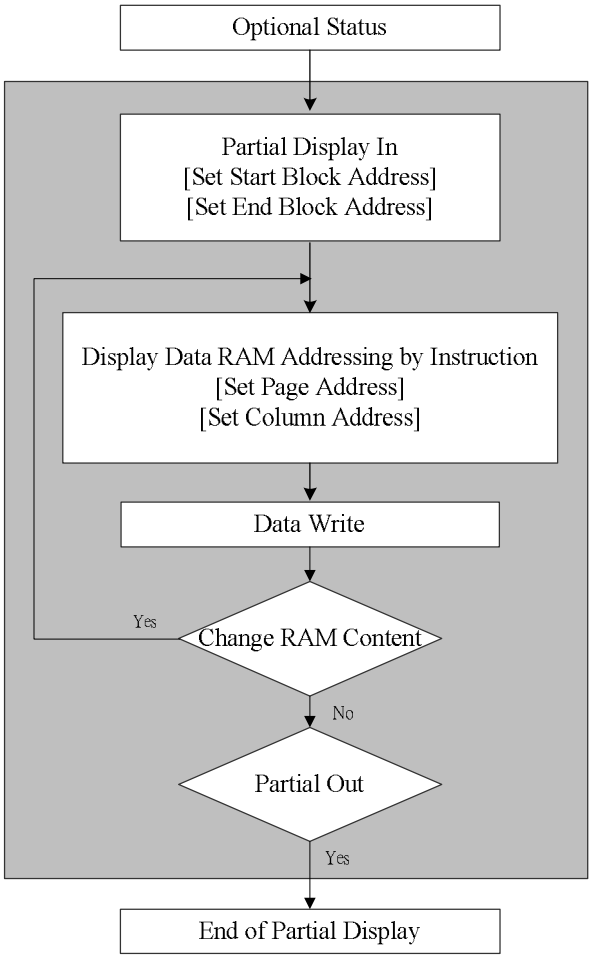
Referential Instruction Setup Flow: Power OFF





Power OFF

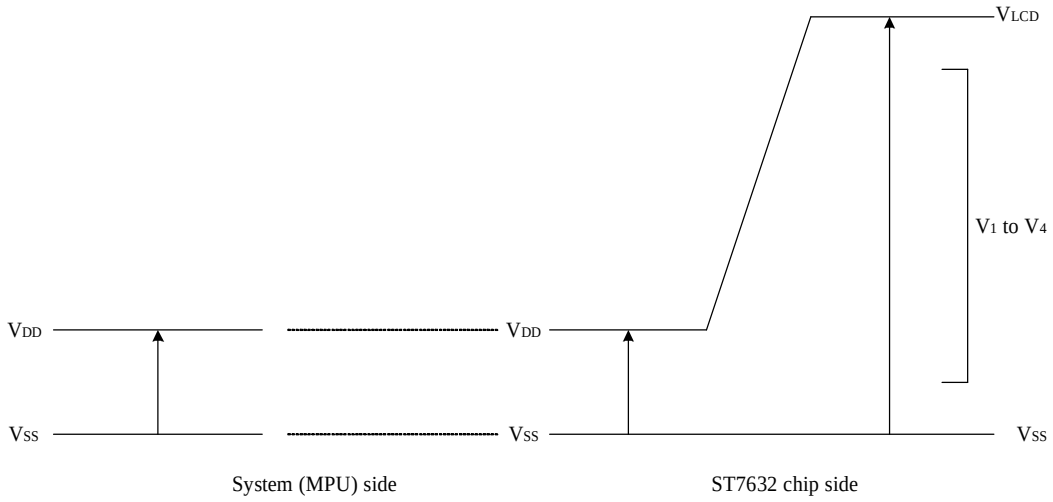
Partial Display In/Out



9. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDD,VDD1~5	–0.5 ~ 4.0	V
Power supply voltage (VDD standard)	VOUTIN	–0.5 ~ +20	V
Power supply voltage (VDD standard)	V1, V2, V3, V4	0.3 to VOUTIN	V
Input voltage	VIN	–0.5 to VDD+0.5	V
Output voltage	VO	–0.5 to VDD+0.5	V
Operating temperature (Die)	TOPR	–30 to +85	°C
Storage temperature (Die)	TSTR	–40 to +125	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure that the voltage levels of V1, V2, V3, and V4 are always such that

   VOUTIN ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ VSS

10. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS devices”).

11. DC CHARACTERISTICS

VDD = 2.6 V to 3.3V; VSS= 0 V; VLCD = 4.0 to 18.0V; Tamb = -30℃ to +85℃; unless otherwise specified.

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		VDD1			2.0	—	3.3(+10% Range)	V	VSS *1
Operating Voltage (2)		VDD2	(Relative to VSS)		2.6	—	3.3	V	VSS2
High-level Input Voltage		VIHC			0.8 x VDD	—	VDD	V	*2
Low-level Input Voltage		VILC			VSS	—	0.2 x VDD	V	*2
High-level Output Voltage		VOHC			0.8 x VDD	—	VDD	V	*3
Low-level Output Voltage		VOLC			VSS	—	0.2 x VDD	V	*3
Input leakage current		ILI	VIN = VDD or VSS		–1.0	—	1.0	μA	*4
Output leakage current		ILO	VIN = VDD or VSS		–3.0	—	3.0	μA	*5
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C (Relative To VSS)	VOUTIN = 15.0 V	—	2.0	3.5	KΩ	SEGn COMn *6
				VOUTIN = 8.0 V	—	3.2	5.4		
Oscillator Frequency	Internal Oscillator	fOSC	1/132 duty Ta = 25°C 31 PWM		10.2	--	10.3	kHz	*7
	Frame frequency	fFRAME			73.2	77	80.9	Hz	

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	VDD	(Relative To VSS)	2.0	—	3.3(+10% Range)	V	
	Supply Step-up output voltage Circuit	VOUOUT	(Relative To VSS)	—	—	18	V	VOUOUT
	Voltage regulator Circuit Operating Voltage	VOUTIN	(Relative To VSS)	—	—	18	V	VOUTIN

Dynamic Consumption Current : During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used .

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW (die)	ISS	VDD = 2.8 V, 1/12 bias ,6x V0 – VSS = 12.5 V	—	350	420	μA	*8
Sleep In	ISS	Ta = 25°C	—	—	10	μA	die

Notes to the DC characteristics

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load, Internal clock
2. Power-down mode. During power down all static currents are switched off.
3. If external V_{LCD}, the display load current is not transmitted to I_{DD}.
4. V_{LCD} external voltage applied to VOUTIN pin; VOUTIN disconnected from VOUOUT

References for items mark with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The A0, D0 to D5, D6 (SI), D7 (SCL), /RD (E), /WR ,/(R/W),CL, RESB ,and terminals.

*3 The D0 to D7 erminals.

*4 The A0,/RD (E), /WR ,/(R/W),/CS,RESB ,and terminals.

*5 Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.

*6 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range.
RON = 0.1 V /ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)

*7 The relationship between the oscillator frequency and the frame rate frequency.

*8,9 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.

12. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

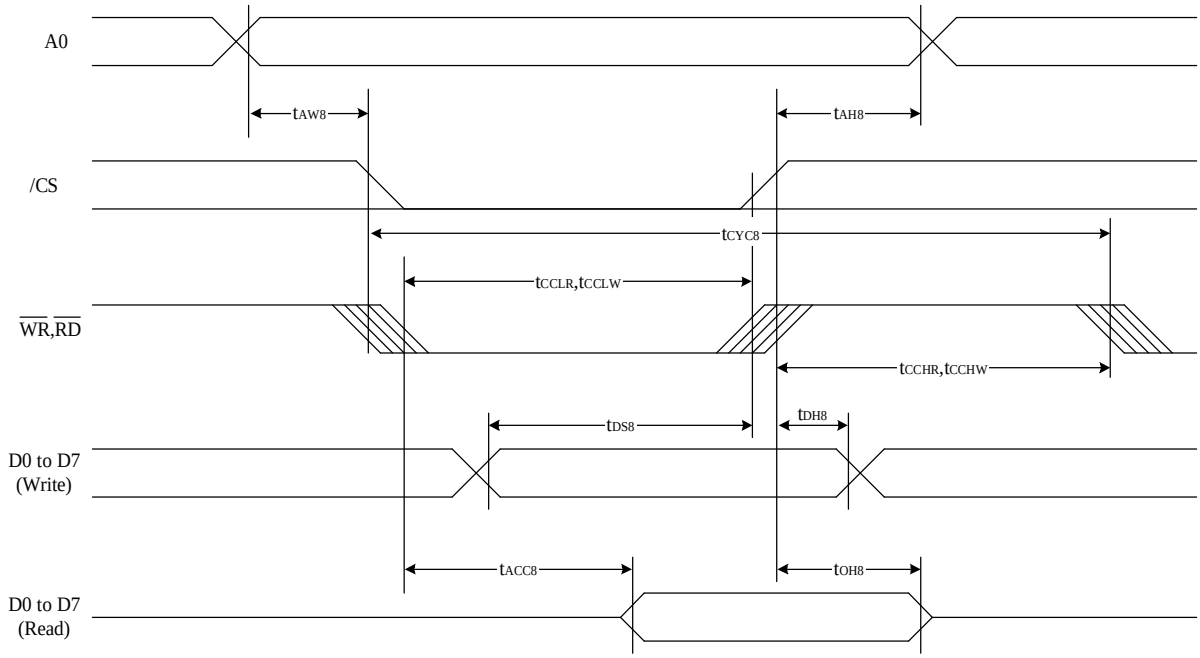


Figure 39.

(VDD = 3.3V , Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		30	—	ns
Address setup time		tAW8		30	—	
System cycle time		tCYC8		370	—	
Enable L pulse width (WRITE)	WR	tCCLW		120	—	
Enable H pulse width (WRITE)		tCCHW		250	—	
Enable L pulse width (READ)	RD	tCCLR		60	—	
Enable H pulse width (READ)		tCCHR		140		
WRITE Data setup time	D0 to D7	tDS8		200	—	
WRITE Address hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	—	50	

(VDD = 2.8 V , Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		30	—	ns
Address setup time		tAW8		30	—	
System cycle time		tCYC8		470	—	
Enable L pulse width (WRITE)	WR	tCCLW		200	—	
Enable H pulse width (WRITE)		tCCHW		280	—	
Enable L pulse width (READ)	RD	tCCLR		80	—	
Enable H pulse width (READ)		tCCHR		190	—	
WRITE Data setup time	D0 to D7	tDS8		280	—	
WRITE Address hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	—	100	

(VDD = 2.0V , Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		30	—	ns
Address setup time		tAW8		30	—	
System cycle time		tCYC8		880	—	
Enable L pulse width (WRITE)	WR	tCCLW		340	—	
Enable H pulse width (WRITE)		tCCHW		540	—	
Enable L pulse width (READ)	RD	tCCLR		170	—	
Enable H pulse width (READ)		tCCHR		360		
WRITE Data setup time	D0 to D7	tDS8		420	—	
WRITE Address hold time		tDH8		30	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	—	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) $\leqq$ (tCYC8 – tCCLW – tCCHW) for (tr + tf) $\leqq$ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between /CS being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

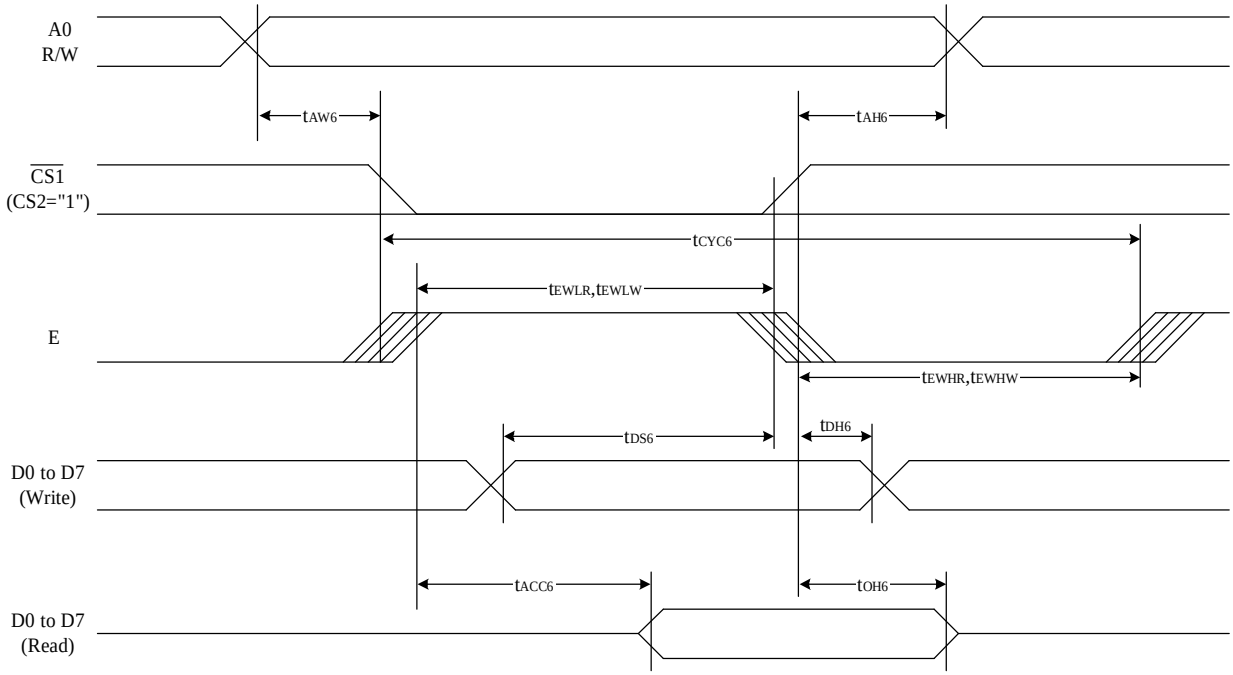


Figure 40.

(VDD = 3.3 V , Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		30	—	ns
Address setup time		tAW6		30	—	
System cycle time		tCYC6		380	—	
Enable L pulse width (WRITE)	WR	tEWLW		120	—	
Enable H pulse width (WRITE)		tEWHW		260	—	
Enable L pulse width (READ)	RD	tEWLR		60	—	
Enable H pulse width (READ)		tEWHR		130		
WRITE Data setup time	D0 to D7	tDS6		200	—	
WRITE Address hold time		tDH6		30	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	—	50	

(VDD = 2.8V , Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		30	—	ns
Address setup time		tAW6		30	—	
System cycle time		tCYC6		490	—	
Enable L pulse width (WRITE)	WR	tEWLW		200	—	
Enable H pulse width (WRITE)		tEWHW		290	—	
Enable L pulse width (READ)	RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		190	—	
WRITE Data setup time	D0 to D7	tDS6		290	—	
WRITE Address hold time		tDH6		40	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	—	100	

(VDD =2.0V , Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		30	—	ns
Address setup time		tAW6		30	—	
System cycle time		tCYC6		890	—	
Enable L pulse width (WRITE)	WR	tEWLW		340	—	
Enable H pulse width (WRITE)		tEWHW		550	—	
Enable L pulse width (READ)	RD	tEWLR		170	—	
Enable H pulse width (READ)		tEWHR		360	—	
WRITE Data setup time	D0 to D7	tDS6		420	—	
WRITE Address hold time		tDH6		30	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	—	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between /CS being “L” and E.

SERIAL INTERFACE(4-Line Interface)

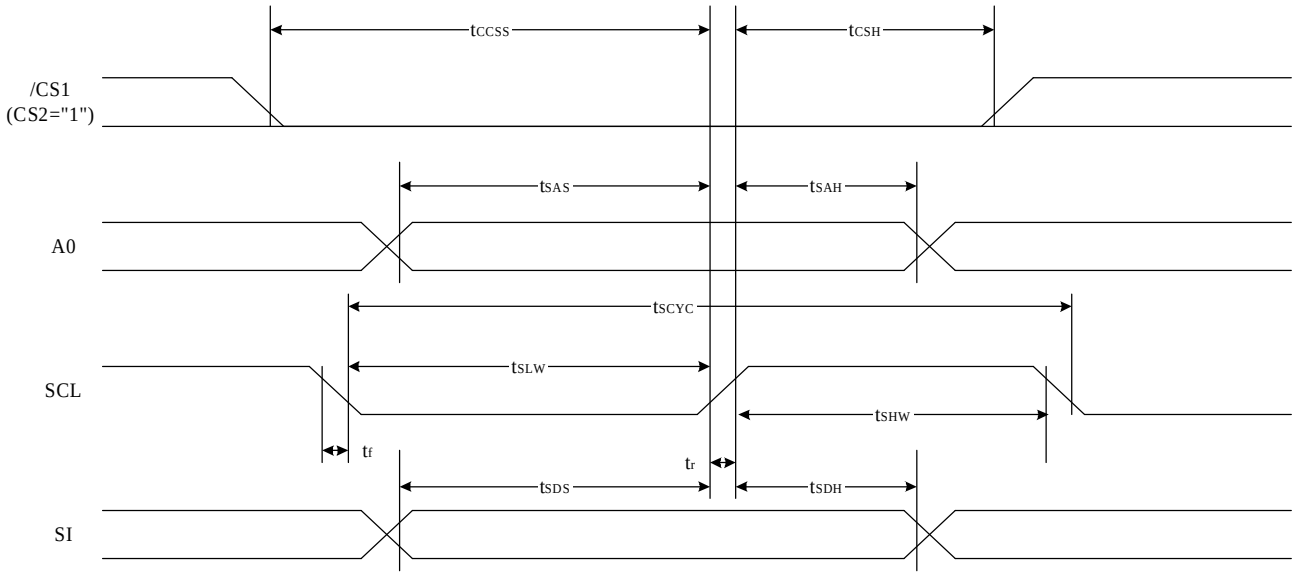


Fig 41.

(VDD=3.3V, Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		110	—	ns
SCL “H” pulse width		tSHW		60	—	
SCL “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		50	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		50	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		60	—	

(VDD=2.8V, Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		130	—	ns
SCL “H” pulse width		tSHW		70	—	
SCL “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		40	—	
Address hold time		tSAH		60	—	
Data setup time	SI	tSDS		40	—	
Data hold time		tSDH		50	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		90	—	

(VDD=2.0V, Ta =-30˚C ~85˚C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		240	—	ns
SCL “H” pulse width		tSHW		140	—	
SCL “L” pulse width		tSLW		110	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		90	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		90	—	
CS-SCL time	CSB	tCSS		60	—	
CS-SCL time		tCSH		140	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE(3-Line Interface)

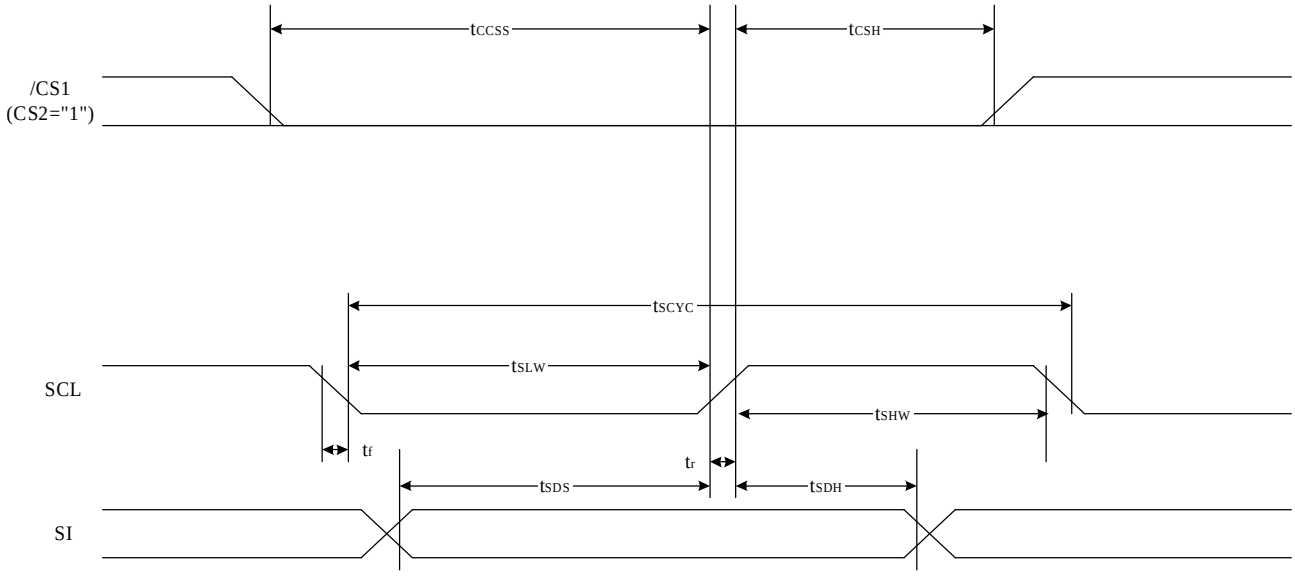


Fig 42.

(VDD=3.3V, Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		110	—	ns
SCL “H” pulse width		tSHW		60	—	
SCL “L” pulse width		tSLW		50	—	
Data setup time	SI	tSDS		30	—	
Data hold time		tSDH		50	—	
CS-SCL time	CSB	tCSS		30	—	
CS-SCL time		tCSH		60	—	

(V_{DD}=2.8V, Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		120	—	ns
SCL “H” pulse width		tSHW		70	—	
SCL “L” pulse width		tSLW		50	—	
Data setup time	SI	tSDS		40	—	
Data hold time		tSDH		50	—	
CS-SCL time	CSB	tCSS		40	—	
CS-SCL time		tCSH		90	—	

(V_{DD}=2.0V, Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC		260	—	ns
SCL “H” pulse width		tSHW		140	—	
SCL “L” pulse width		tSLW		120	—	
Data setup time	SI	tSDS		60	—	
Data hold time		tSDH		90	—	
CS-SCL time	CSB	tCSS		60	—	
CS-SCL time		tCSH		120	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

13. RESET TIMING

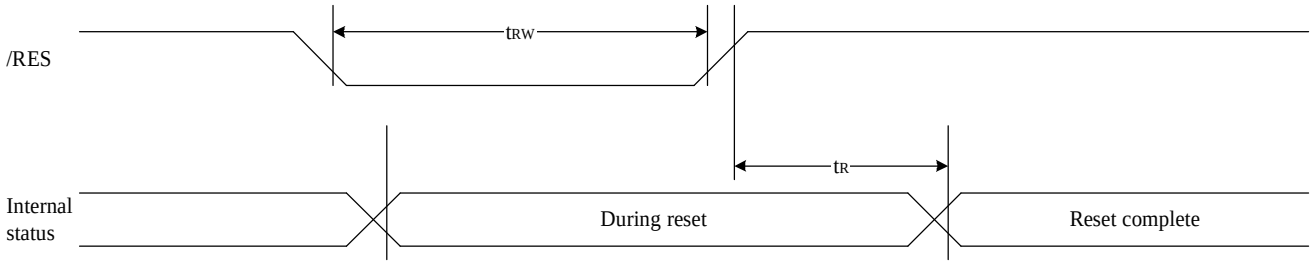


Fig 43.

(VDD = 3.3V , Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	us
Reset “L” pulse width	RESB	tRW		1	—	—	us

(VDD = 2.8V , Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	us
Reset “L” pulse width	RESB	tRW		1.5	—	—	us

(VDD = 2.0V , Ta =-30°C ~85°C, die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset “L” pulse width	RESB	tRW		2.0	—	—	us

The pinning of the ST7632 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size:

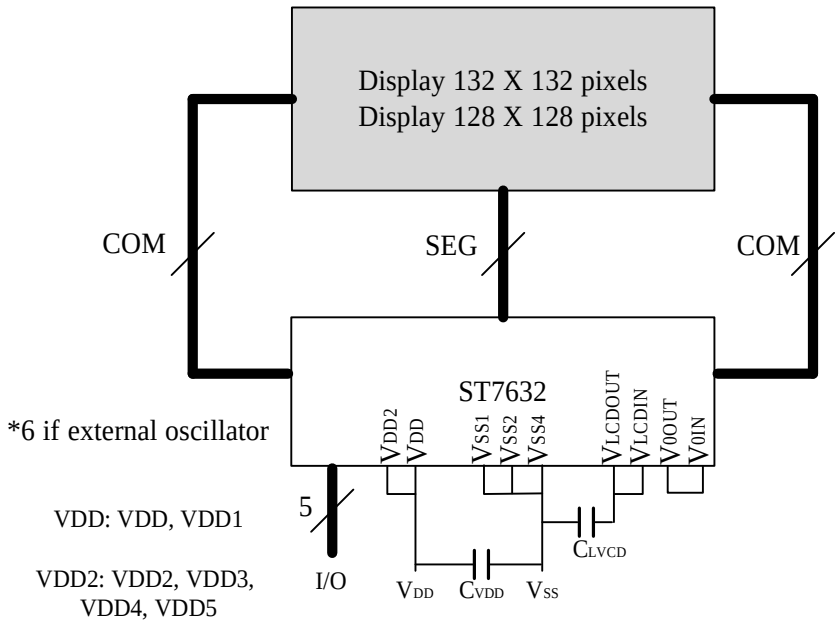


Fig 44. Application diagram: internal charge pump is used and s single V_{DD}

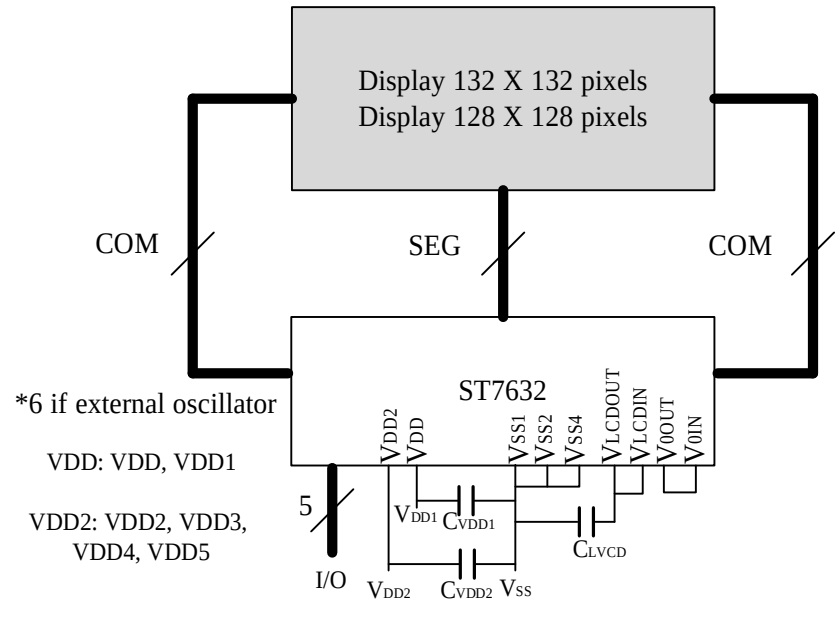


Fig 45. Application diagram: Internal charge pump is used and two separate V_{DD1}(V_{DD2})

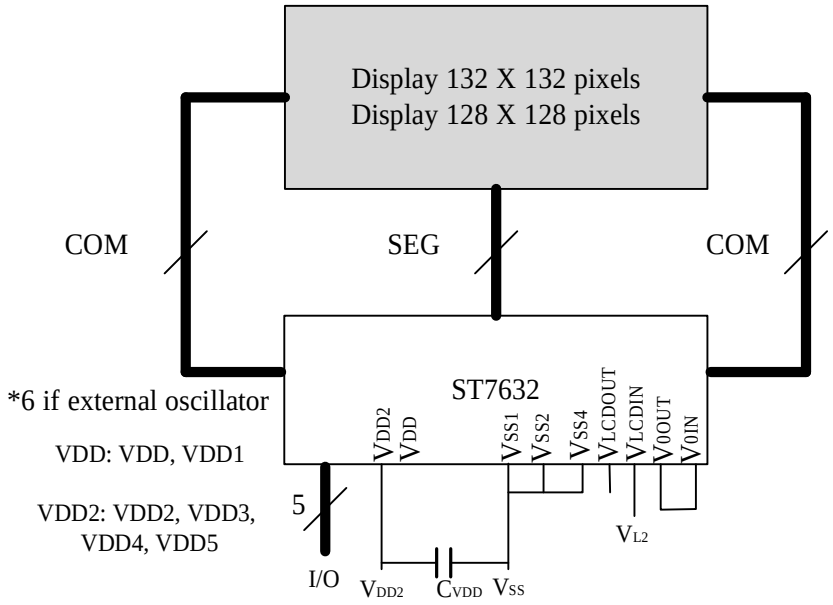


Fig 46. application diagram : External high voltage generation is used

The requiblue minimum value for the external capacitors in an application with the ST7632 are:

C_{VLCD} = min. 3.3uF $C_{VDD1,2}$= min. 1.0 μF

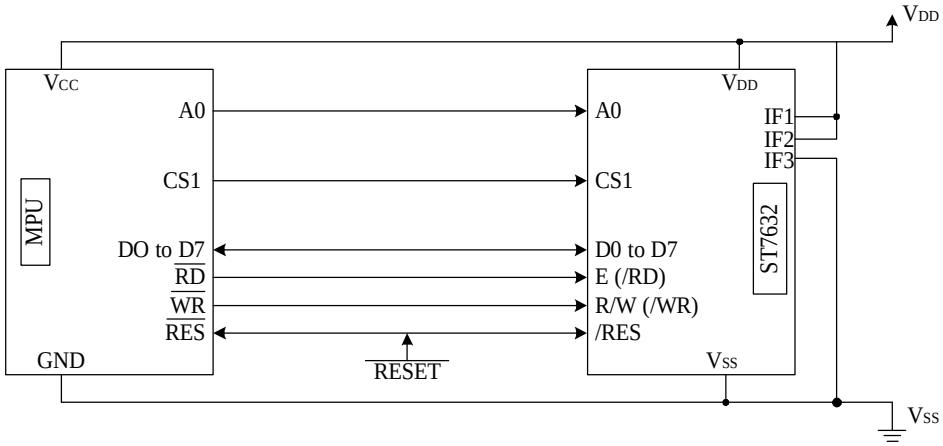
Higher capacitor values are recommended for ripple.

14. THE MPU INTERFACE (REFERENCE EXAMPLES)

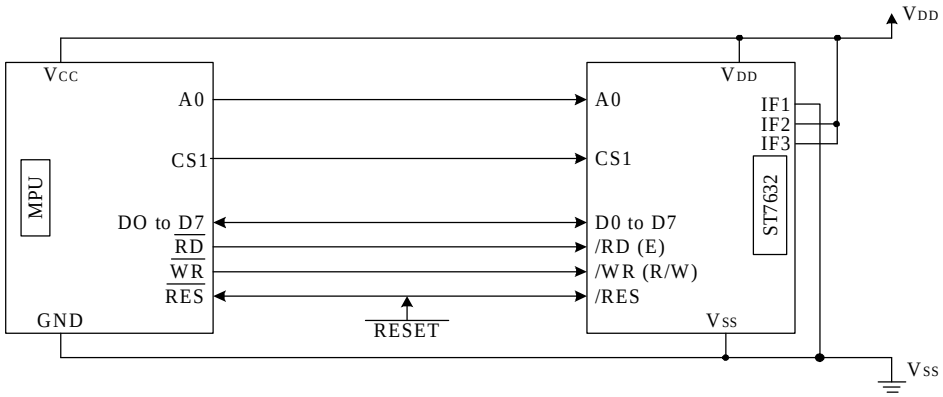
The ST7632 Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7632 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7632 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

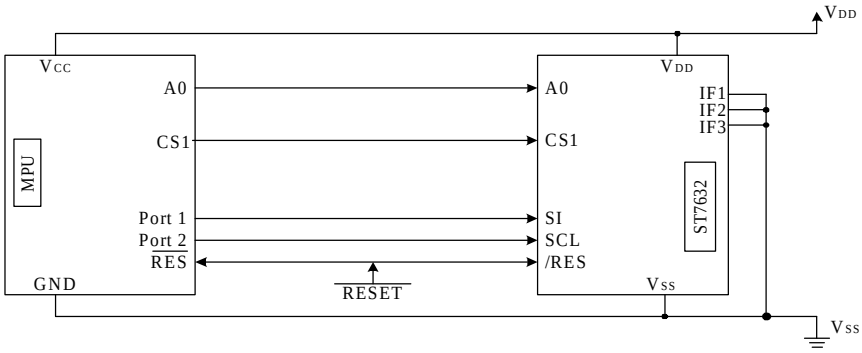
(1) 8080 Series MPUs



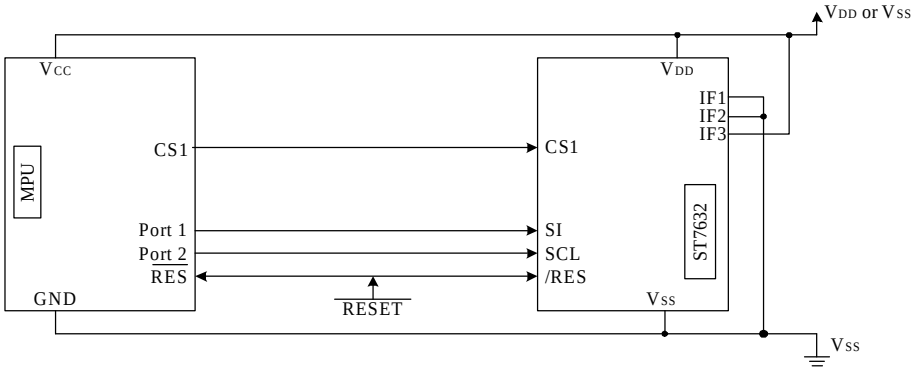
(2) 6800 Series MPUs



(3) Using the Serial Interface (4-line interface)

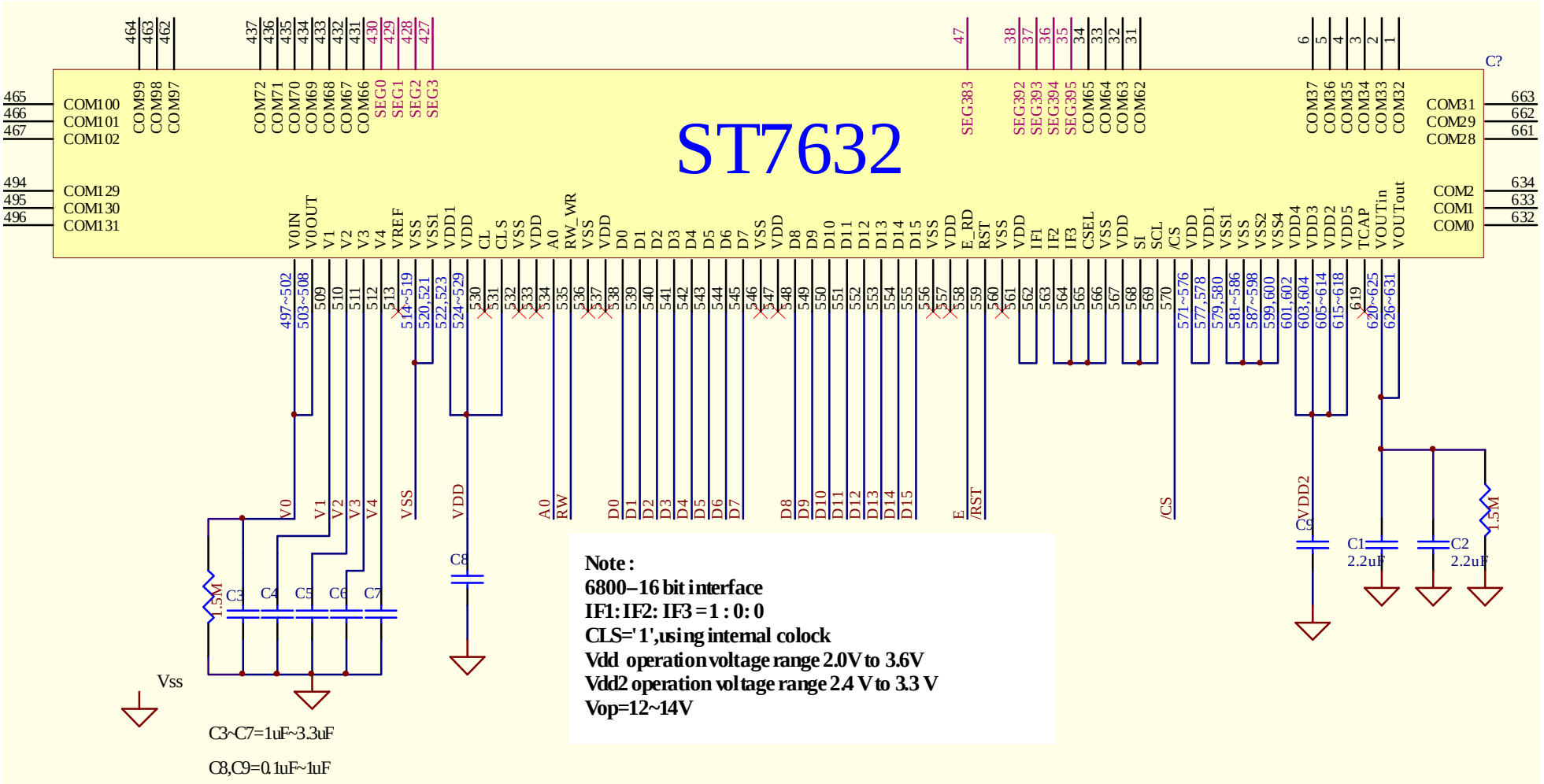


(4) Using the Serial Interface (3-line interface)

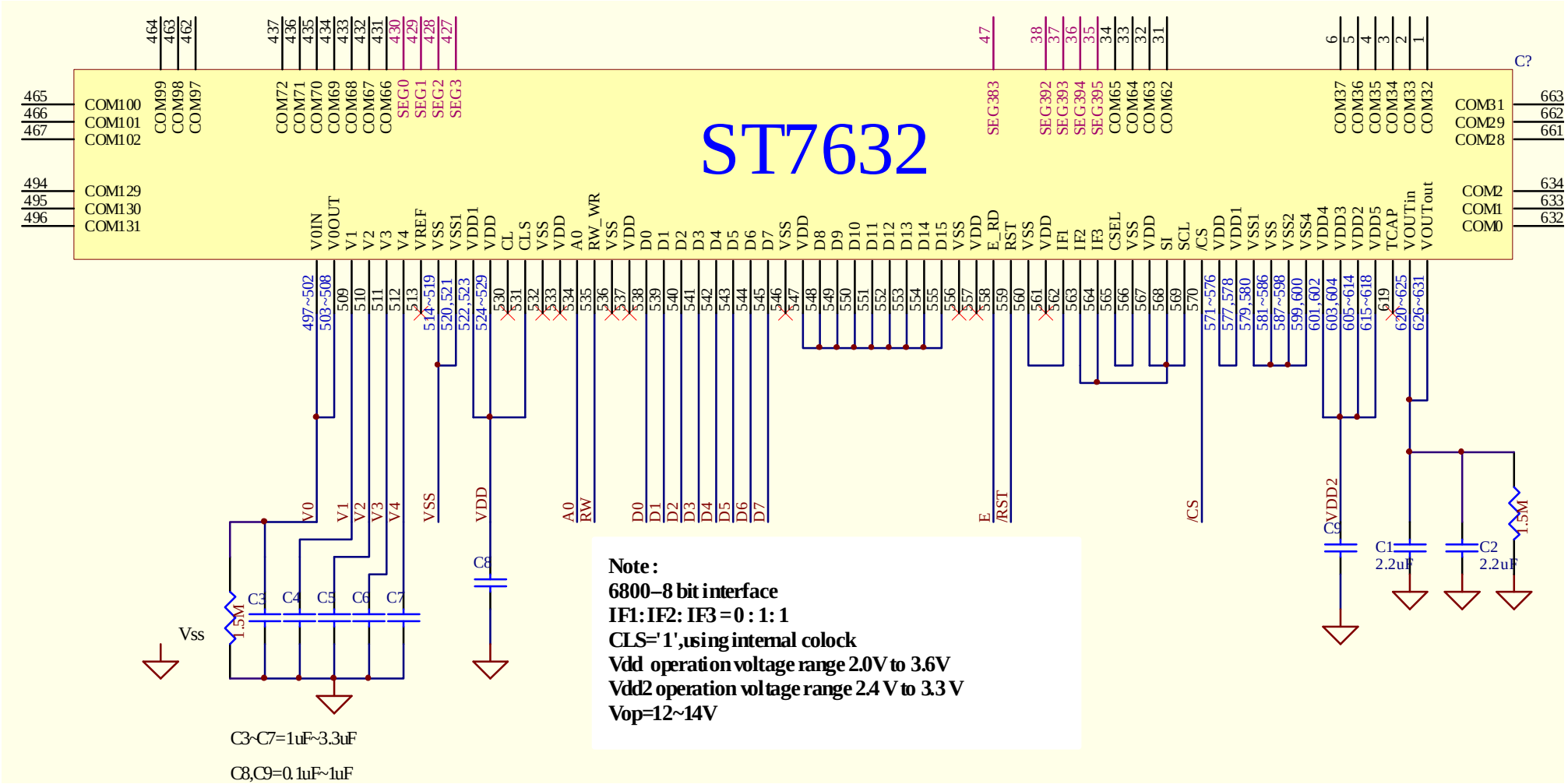


Application circuit :

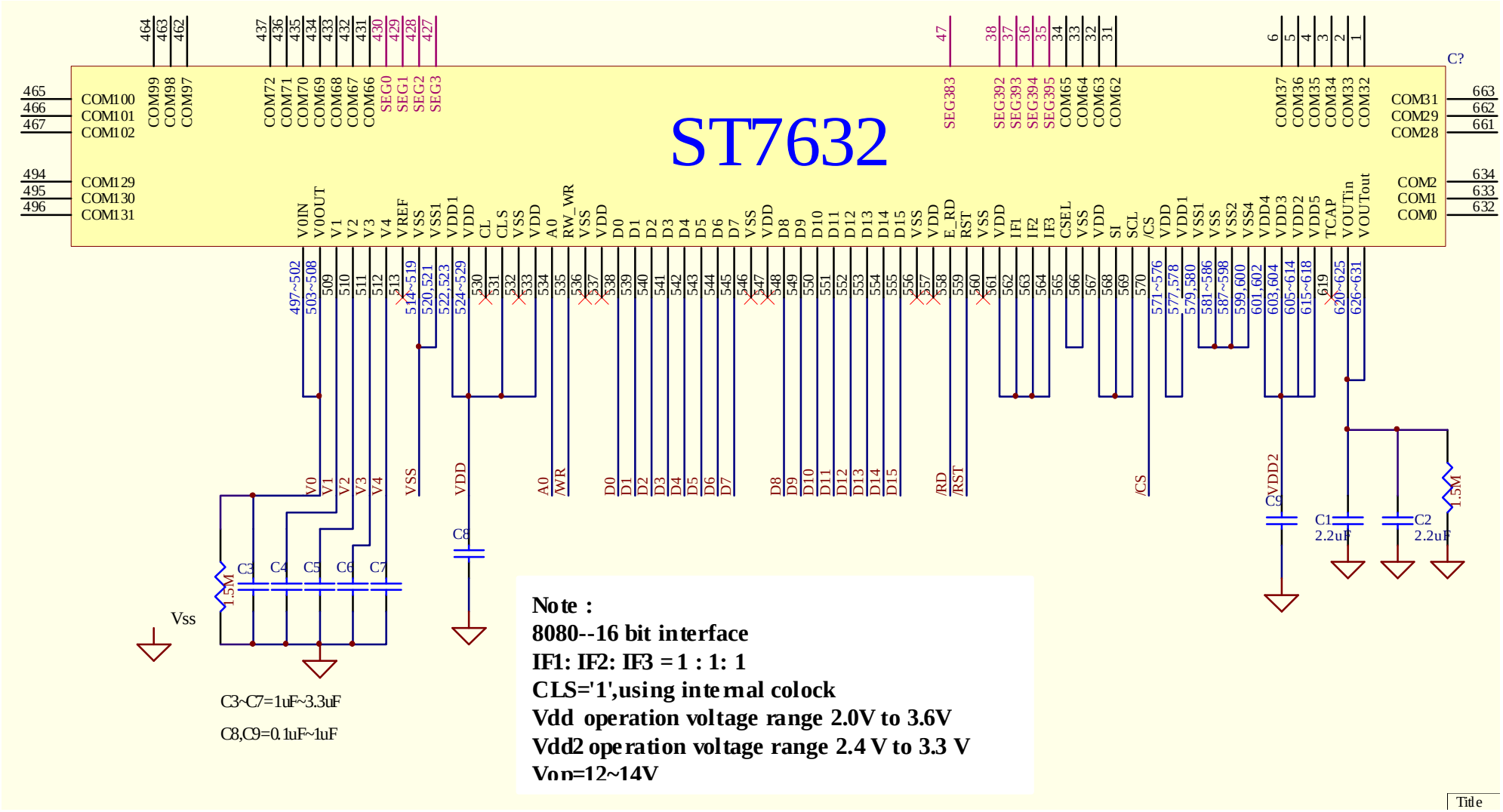
(A) 6800-16 bit interface (V0 and VLCD –internal)



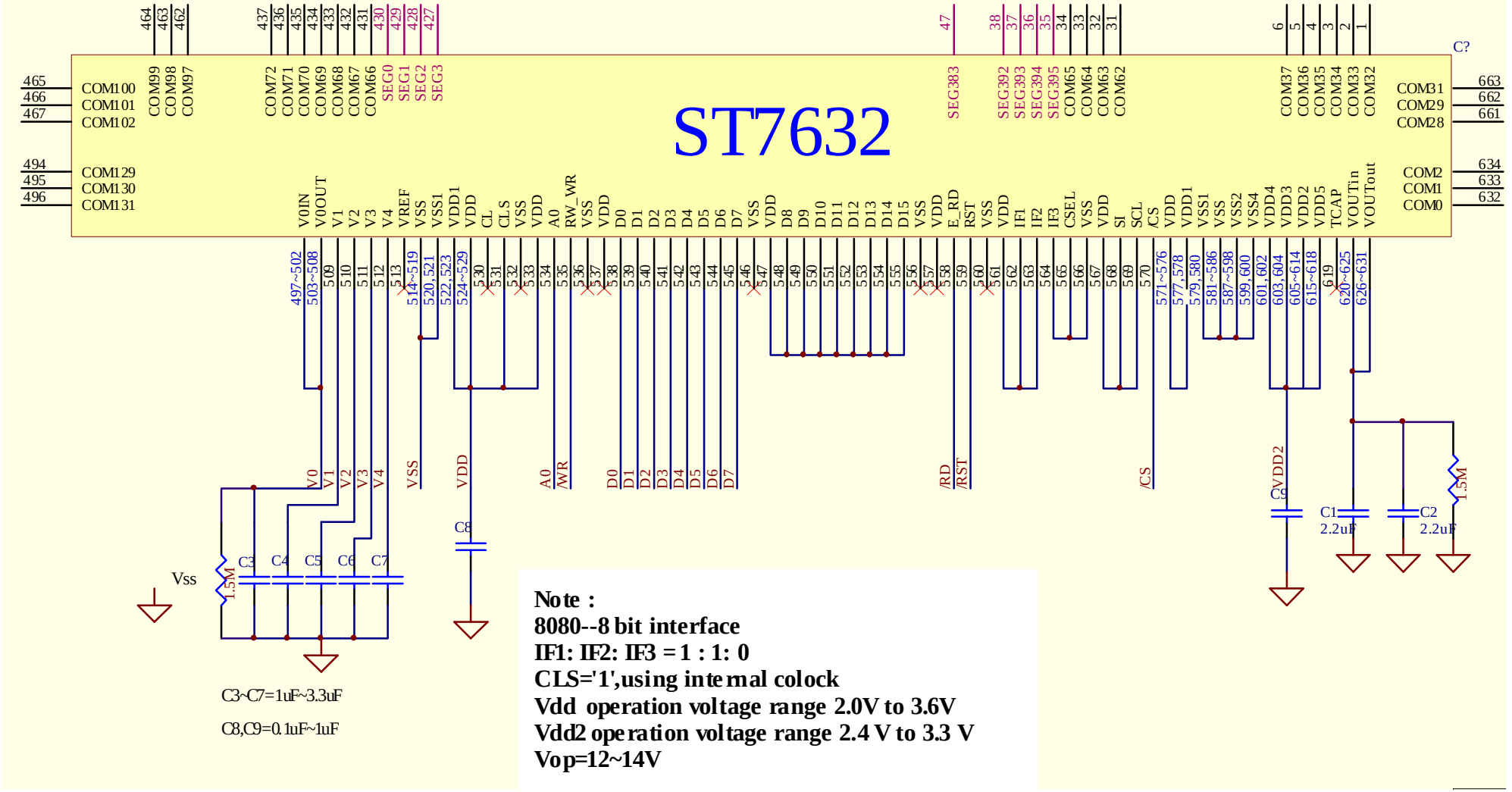
(B) 6800-8 bit interface (V0 and VLCD –internal)



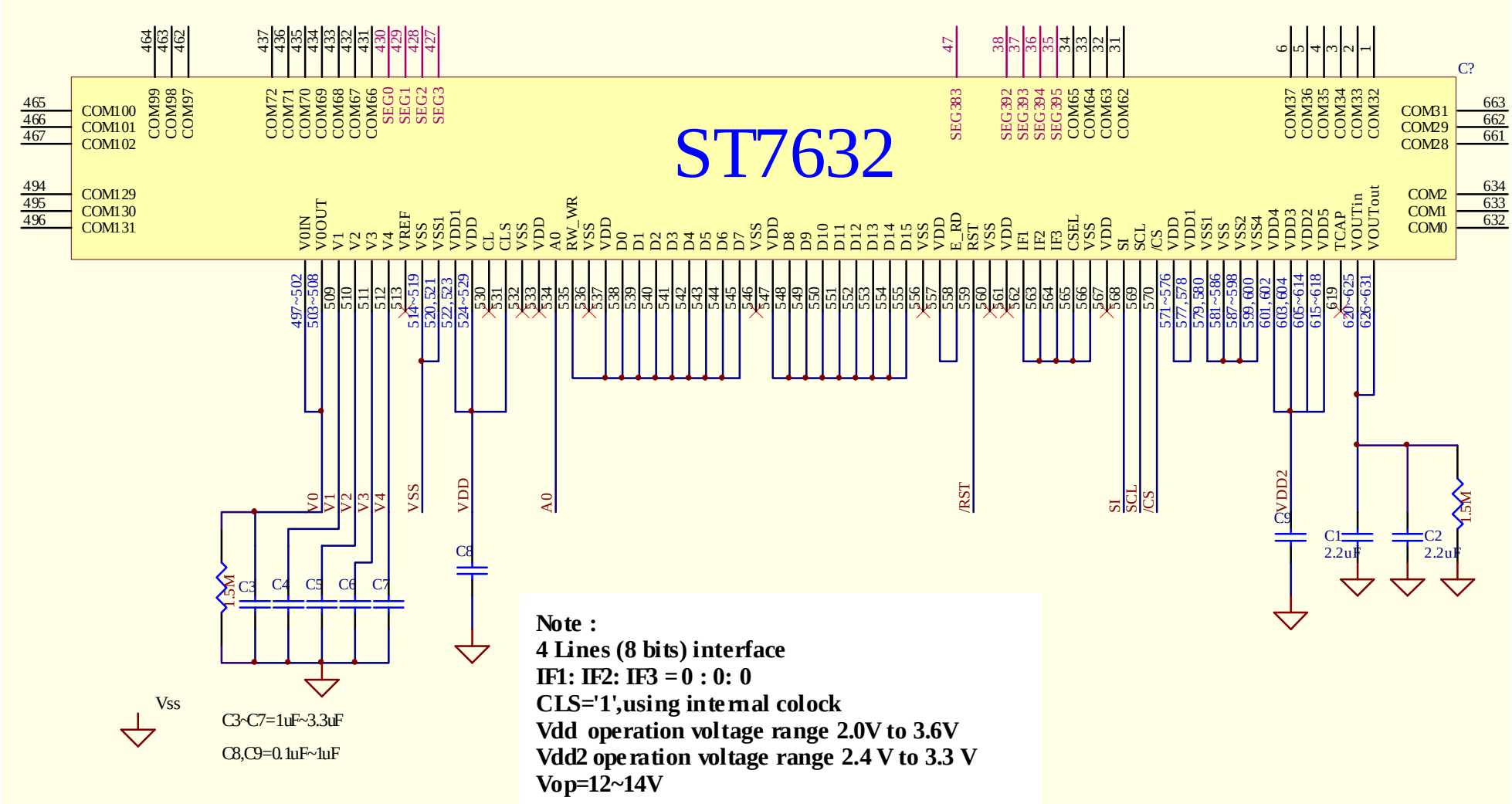
(C) 8080-16 bit interface (V0 and VLCD –internal)



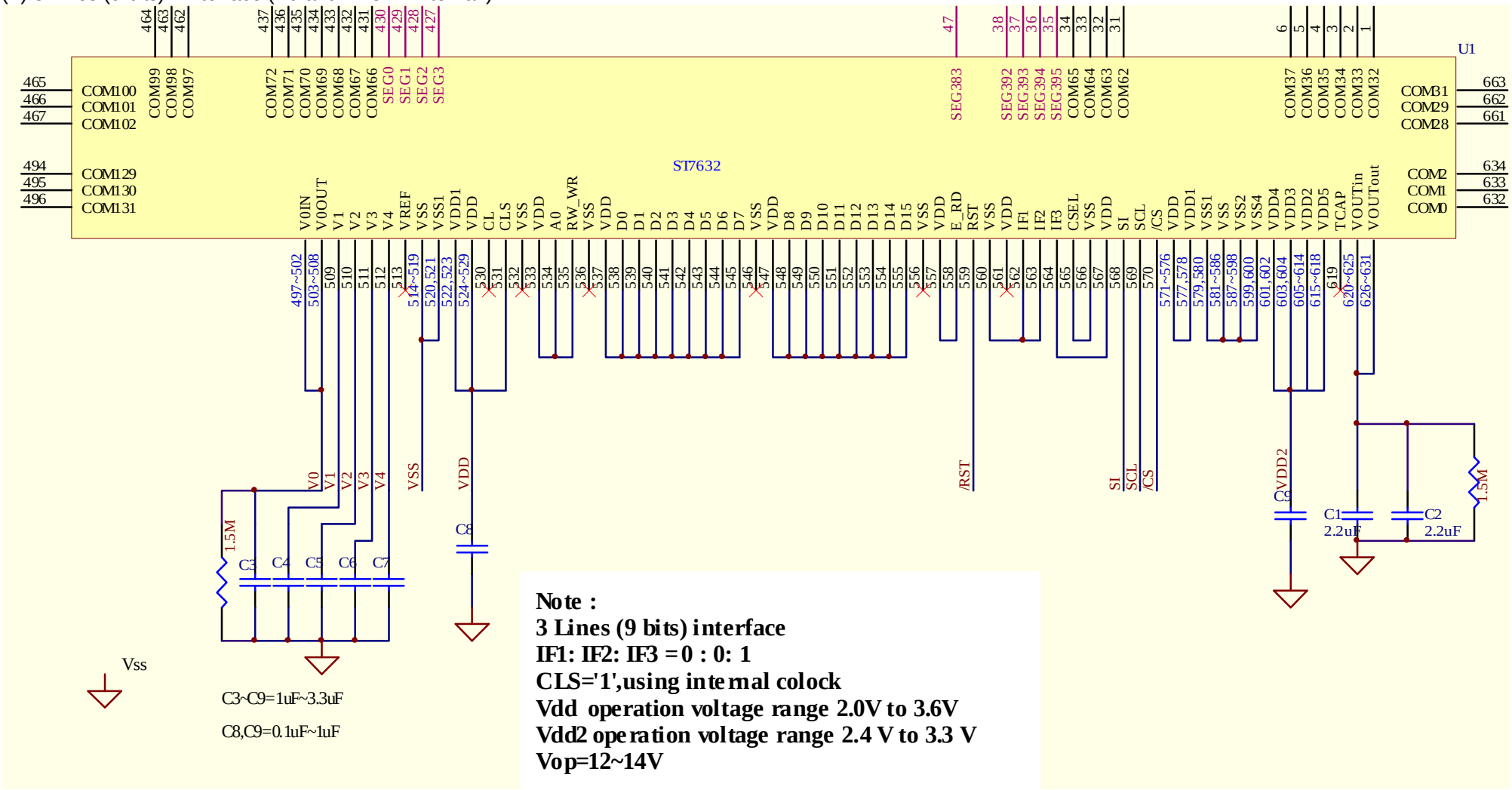
(D) 8080-8 bit interface (V0 and VLCD –internal)



(E) 4 Lines (8 bits) interface (V0 and VLCD –internal)

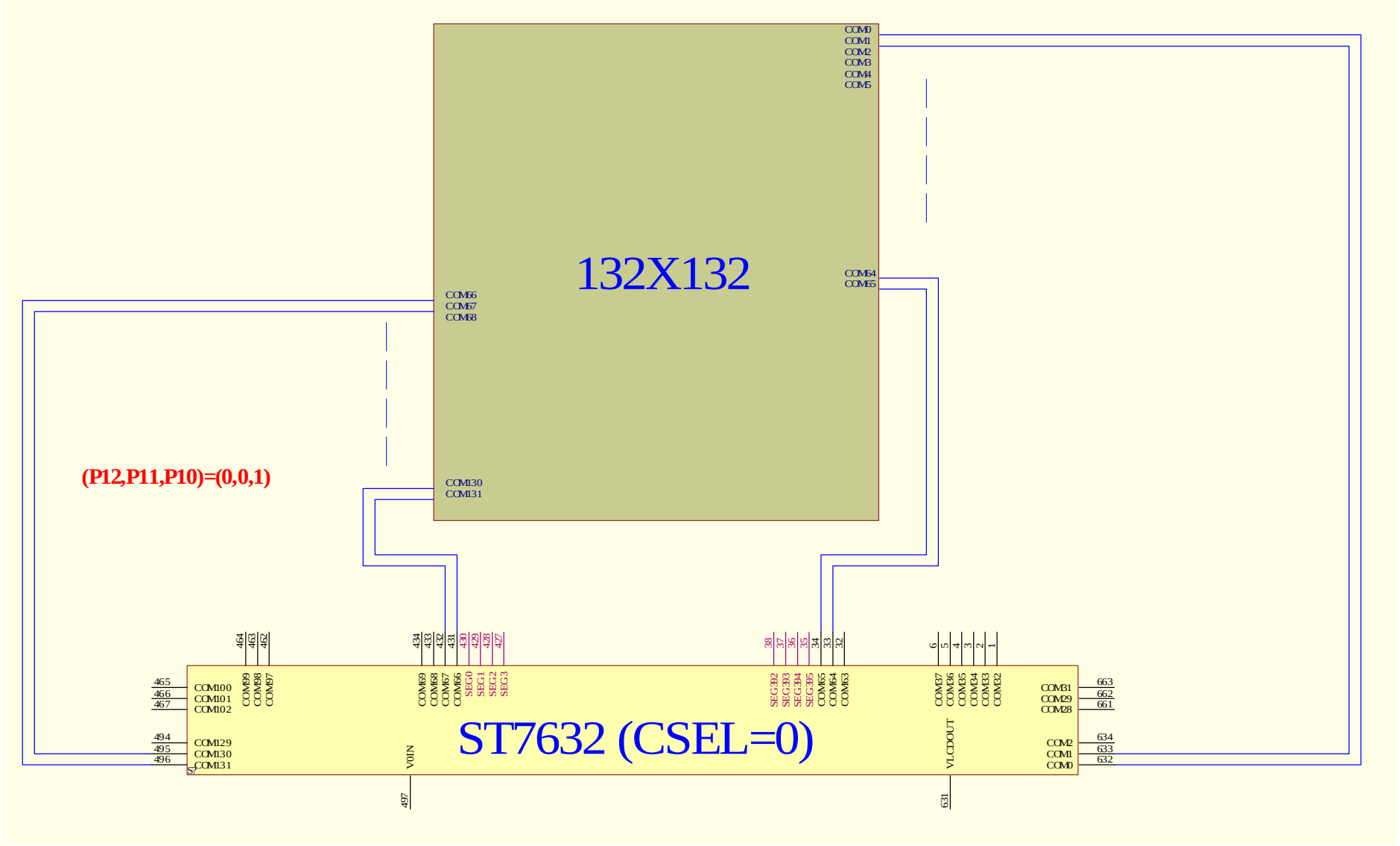


(F) 3 Lines (9 bits) interface (V0 and VLCD –internal)



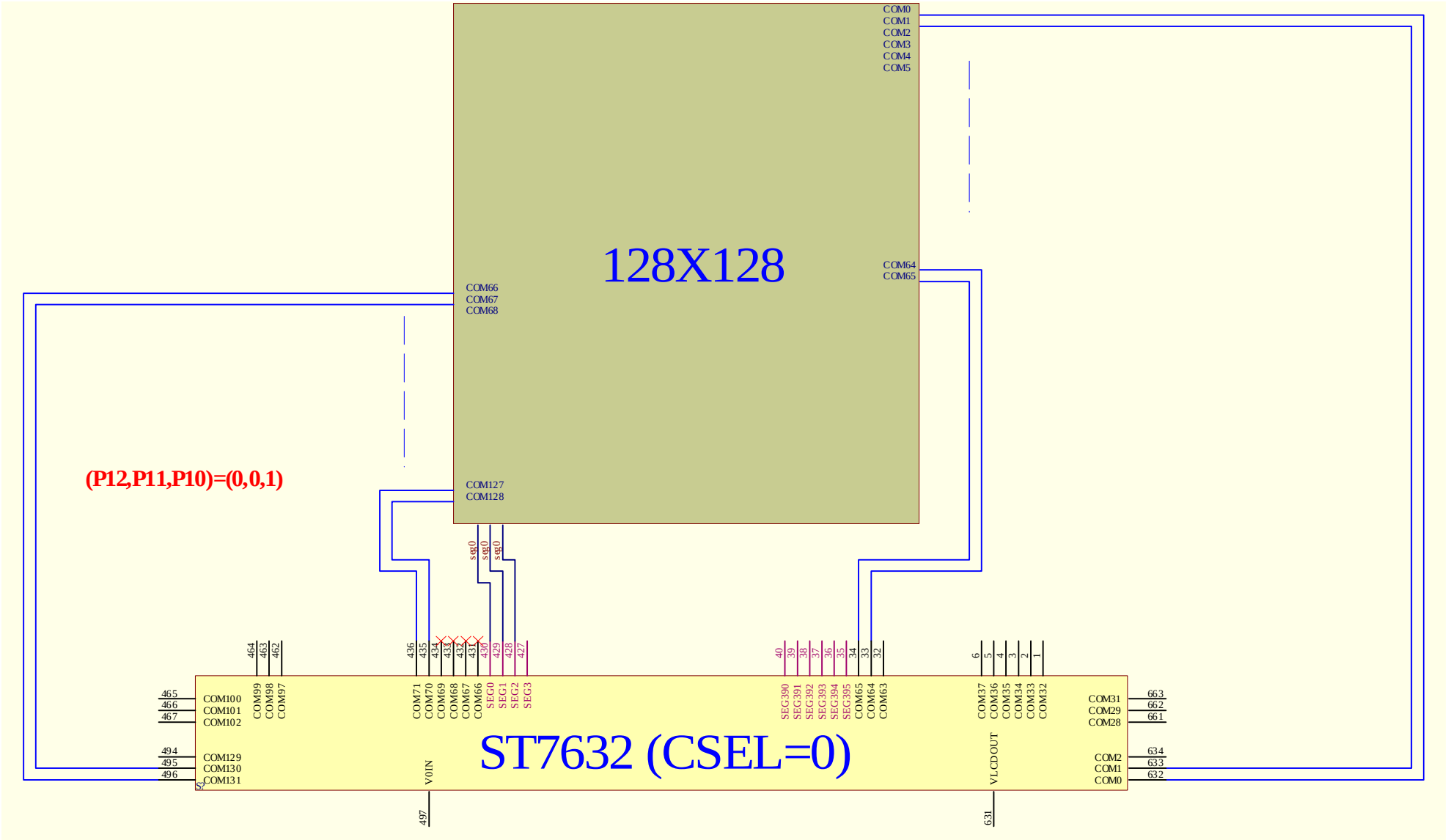
(G) Example 132X132 :

Duty=1/132 Vop=12~14V Bias=1/12 bias



(H) Example 128X128 :

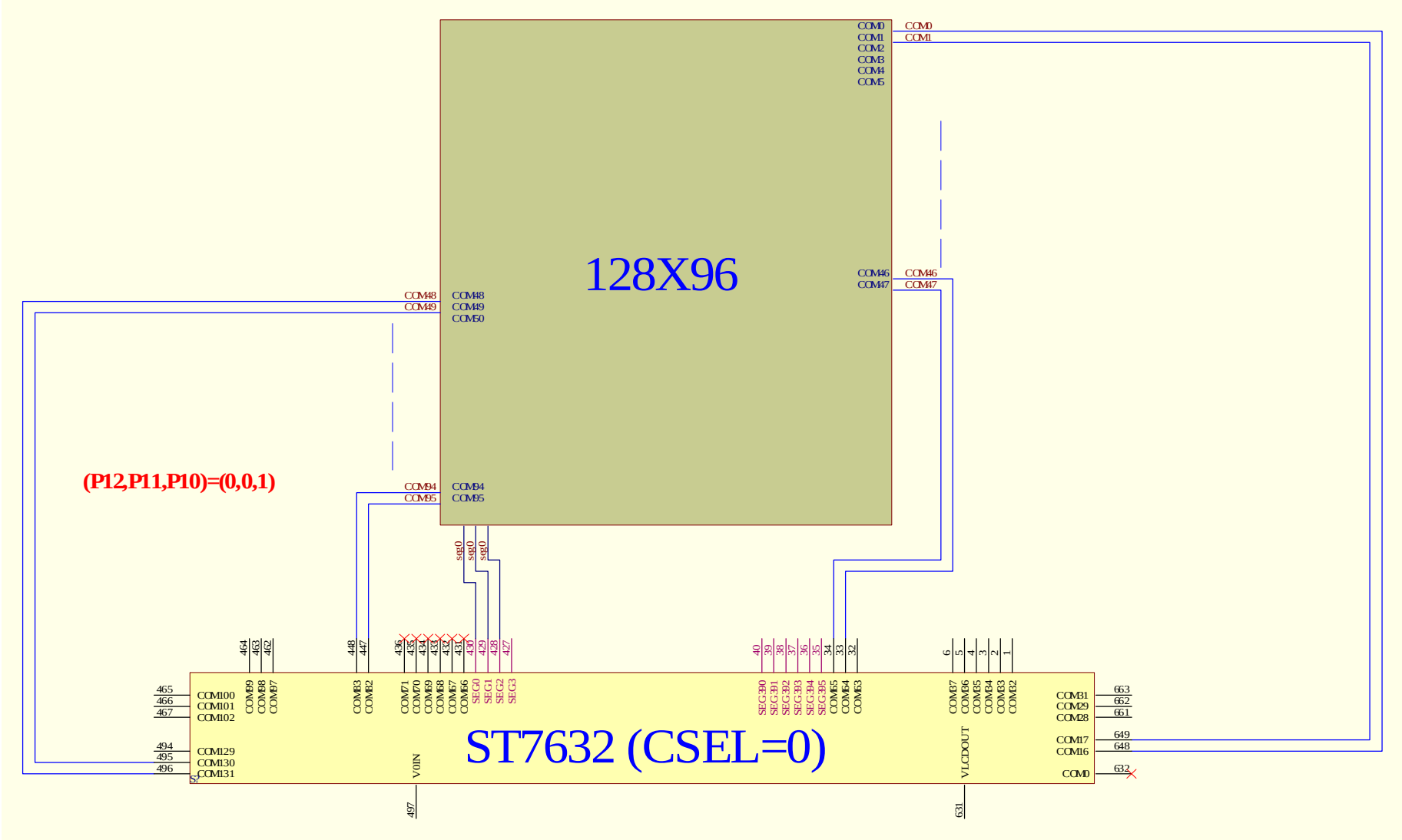
Duty=1/128 Vop=12~14V Bias=1/12 bias



(I)128X96

Duty=1/132 Vop=12~14V Bias=1/12 bias

Display window set: start page=16，end page=111



NOTE: Microprocessor interface pins should not be floating in any operation mode.

ST7632 Serial Specification Revision History		
Version	**Date**	**Description**
1.0	2004/8/31	Remove preliminary
1.1	2004/10/11	Correct errors in writting words & Modify Timing Characteristic
1.2	2004/12/07	Addition V3&V4 must <Vdd (p1), p48,p49 graphic diagram, and analog set flow p70,modify timing character
1.3	2005/02/01	Modify p75 LIMITING VALUES
1.4	2005/5/20	Remove the IIC Interface
1.5	2005/09/15	Addition DC/AC application range
1.6	2006/7/31	Modify Application Circuit P87~P92
1.7	2006/8/15	Add microprocessor notice item(p.16, p.95).