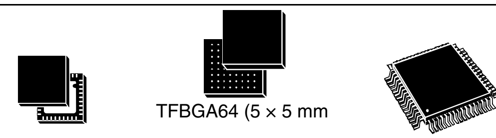
# STM32F103x4
# STM32F103x6

## Low-density performance line, ARM-based 32-bit MCU with 16 or 32 KB Flash, USB, CAN, 6 timers, 2 ADCs, 6 communication interfaces

### Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 72 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 16 or 32 Kbytes of Flash memory
  - 6 or 10 Kbytes of SRAM
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4-to-16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC
  - PLL for CPU clock
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - $V_{BAT}$ supply for RTC and backup registers
- 2 x 12-bit, 1 µs A/D converters (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Dual-sample and hold capability
  - Temperature sensor
- DMA
  - 7-channel DMA controller
  - Peripherals supported: timers, ADC, SPIs, $I^2C$s and USARTs
- Up to 51 fast I/O ports
  - 26/37/51 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant



TFBGA64 (5 × 5 mm
VFQFPN36 (6 × 6 mm)
LQFP64 (10 × 10 mm)
LQFP48 (7 × 7 mm)

- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- 6 timers
  - Two 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 16-bit, motor control PWM timer with dead-time generation and emergency stop
  - 2 watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
- 6 communication interfaces
  - 1 x $I^2C$ interface (SMBus/PMBus)
  - 2 × USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - 1 × SPI (18 Mbit/s)
  - CAN interface (2.0B Active)
  - USB 2.0 full-speed interface
- CRC calculation unit, 96-bit unique ID
- Packages are ECOPACK®

**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM32F103x4 | STM32F103C4, STM32F103R4, STM32F103T4 |
| STM32F103x6 | STM32F103C6, STM32F103R6, STM32F103T6 |

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103x4 and STM32F103x6 low-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The low-density STM32F103xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

# 2 Description

The STM32F103x4 and STM32F103x6 performance line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 32 Kbytes and SRAM up to 6 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two $I^2Cs$ and SPIs, three USARTs, an USB and a CAN.

The STM32F103xx low-density performance line family operates from a 2.0 to 3.6 V power supply. It is available in both the –40 to +85 °C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx low-density performance line family includes devices in four different package types: from 36 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx low-density performance line microcontroller family suitable for a wide range of applications:

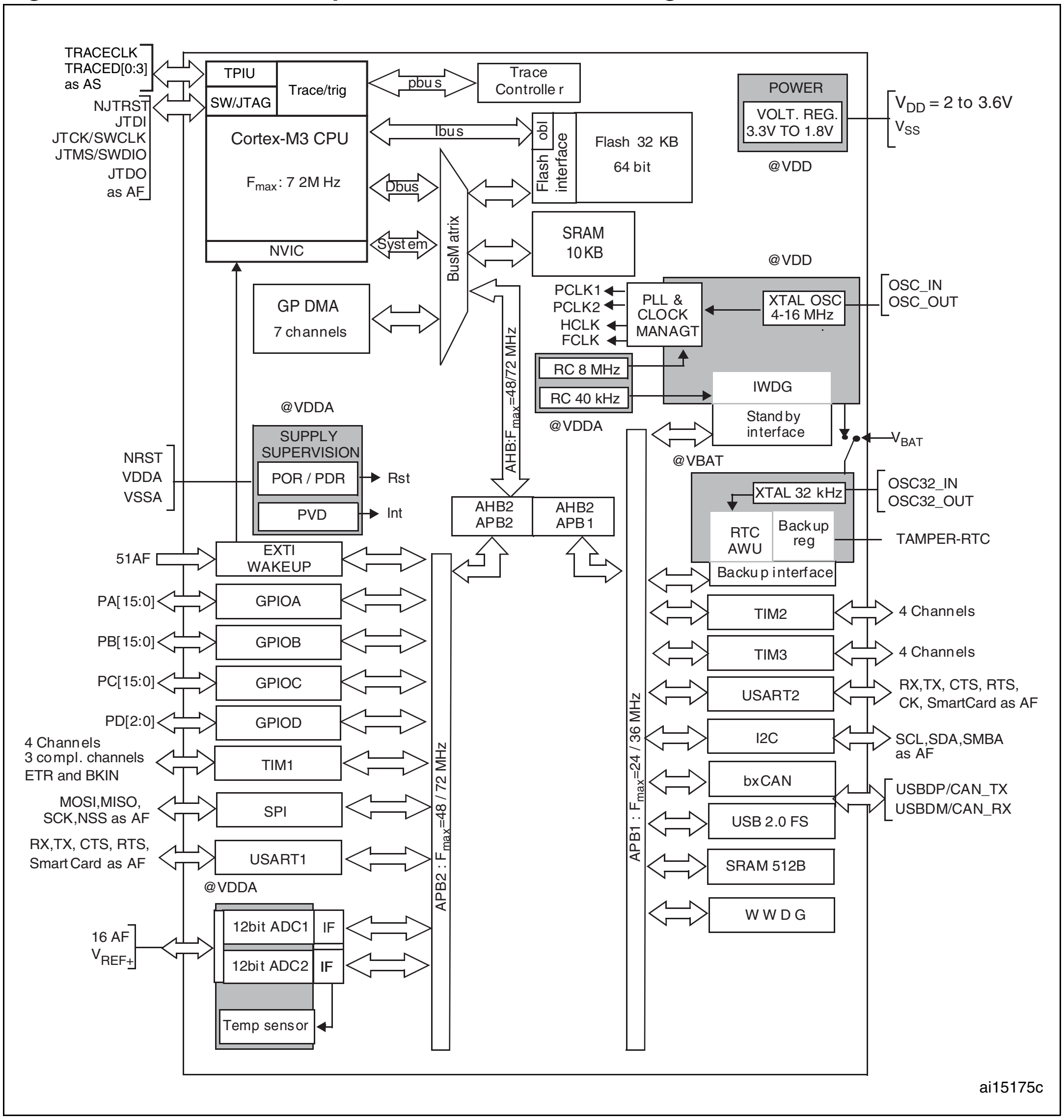
- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

## 2.1 Device overview

Table 2. STM32F103xx low-density device features and peripheral counts

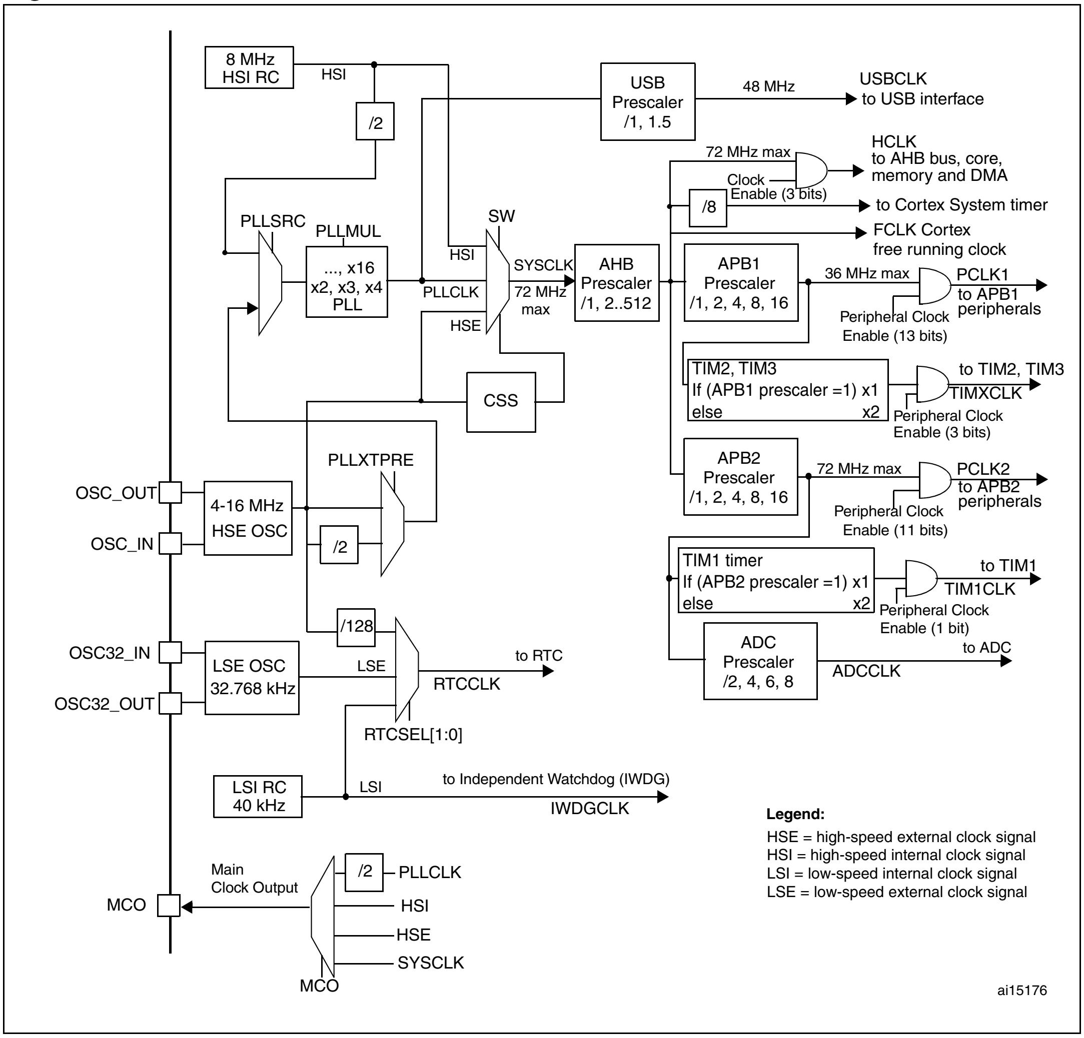
| Peripheral | | STM32F103Tx | | STM32F103Cx | | STM32F103Rx | |
|---|---|---|---|---|---|---|---|
| **Flash - Kbytes** | | 16 | 32 | 16 | 32 | 16 | 32 |
| **SRAM - Kbytes** | | 6 | 10 | 6 | 10 | 6 | 10 |
| **Timers** | **General-purpose** | 2 | 2 | 2 | 2 | 2 | 2 |
| | **Advanced-control** | 1 | | 1 | | 1 | |
| **Communication** | **SPI** | 1 | 1 | 1 | 1 | 1 | 1 |
| | **I²C** | 1 | 1 | 1 | 1 | 1 | 1 |
| | **USART** | 2 | 2 | 2 | 2 | 2 | 2 |
| | **USB** | 1 | 1 | 1 | 1 | 1 | 1 |
| | **CAN** | 1 | 1 | 1 | 1 | 1 | 1 |
| **GPIOs** | | 26 | | 37 | | 51 | |
| **12-bit synchronized ADC Number of channels** | | 2<br>10 channels | | 2<br>10 channels | | 2<br>16 channels | |
| **CPU frequency** | | 72 MHz | | | | | |
| **Operating voltage** | | 2.0 to 3.6 V | | | | | |
| **Operating temperatures** | | Ambient temperatures: –40 to +85 °C /–40 to +105 °C (see *Table 9*)<br>Junction temperature: –40 to + 125 °C (see *Table 9*) | | | | | |
| **Packages** | | VFQFPN36 | | LQFP48 | | LQFP64, TFBGA64 | |

**Figure 1. STM32F103xx performance line block diagram**




1. $T_A$ = –40 °C to +105 °C (junction temperature up to 125 °C).
2. AF = alternate function on I/O port pin.

## Figure 2. Clock tree




1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 48 MHz or 72 MHz.
3. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

## 2.2 Full compatibility throughout the family

The STM32F103xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F103x4 and STM32F103x6 are identified as low-density devices, the STM32F103x8 and STM32F103xB are referred to as medium-density devices, and the STM32F103xC, STM32F103xD and STM32F103xE are referred to as high-density devices.

Low- and high-density devices are an extension of the STM32F103x8/B devices, they are specified in the STM32F103x4/6 and STM32F103xC/D/E datasheets, respectively. Low-density devices feature lower Flash memory and RAM capacities, less timers and peripherals. High-density devices have higher Flash memory and RAM capacities, and additional peripherals like SDIO, FSMC, I$^2$S and DAC, while remaining fully compatible with the other members of the STM32F103xx family.

The STM32F103x4, STM32F103x6, STM32F103xC, STM32F103xD and STM32F103xE are a drop-in replacement for STM32F103x8/B medium-density devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F103xx performance line family is fully compatible with all existing STM32F101xx access line and STM32F102xx USB access line devices.

**Table 3. STM32F103xx family**

<table>
<tr><th rowspan="3">Pinout</th><th colspan="2">Low-density devices</th><th colspan="2">Medium-density devices</th><th colspan="3">High-density devices</th></tr>
<tr><th>16 KB Flash</th><th>32 KB Flash(1)</th><th>64 KB Flash</th><th>128 KB Flash</th><th>256 KB Flash</th><th>384 KB Flash</th><th>512 KB Flash</th></tr>
<tr><th>6 KB RAM</th><th>10 KB RAM</th><th>20 KB RAM</th><th>20 KB RAM</th><th>48 KB RAM</th><th>64 KB RAM</th><th>64 KB RAM</th></tr>
<tr><td>144</td><td></td><td></td><td></td><td></td><td colspan="3" rowspan="3">5 × USARTs<br>4 × 16-bit timers, 2 × basic timers<br>3 × SPIs, 2 × I$^2$Ss, 2 × I2Cs<br>USB, CAN, 2 × PWM timers<br>3 × ADCs, 2 × DACs, 1 × SDIO<br>FSMC (100 and 144 pins)</td></tr>
<tr><td>100</td><td></td><td></td><td colspan="2" rowspan="3">3 × USARTs<br>3 × 16-bit timers<br>2 × SPIs, 2 × I$^2$Cs, USB,<br>CAN, 1 × PWM timer<br>2 × ADCs</td></tr>
<tr><td>64</td><td colspan="2" rowspan="3">2 × USARTs<br>2 × 16-bit timers<br>1 × SPI, 1 × I$^2$C, USB,<br>CAN, 1 × PWM timer<br>2 × ADCs</td></tr>
<tr><td>48</td><td></td><td></td><td></td></tr>
<tr><td>36</td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

1. For orderable part numbers that do not show the A internal code after the temperature range code (6 or 7), the reference datasheet for electrical characteristics is that of the STM32F103x8/B medium-density devices.

## 2.3 Overview

### 2.3.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F103xx performance line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

*Figure 1* shows the general block diagram of the device family.

### 2.3.2 Embedded Flash memory

16 or 32 Kbytes of embedded Flash is available for storing programs and data.

### 2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### 2.3.4 Embedded SRAM

Six or ten Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

### 2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F103xx performance line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

### 2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 51 GPIOs can be connected to the 16 external interrupt lines.

### 2.3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 72 MHz. The maximum allowed frequency of the low-speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

### 2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

### 2.3.9 Power supply schemes

- $V_{DD}$ = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 2.0 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to $V_{DDA}$ is 2.4 V when the ADC is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

For more details on how to connect power pins, refer to *Figure 10: Power supply scheme*.

### 2.3.10 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Refer to *Table 11: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and $V_{PVD}$.

### 2.3.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

### 2.3.12 Low-power modes

The STM32F103xx performance line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** mode

  The Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.
- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

### 2.3.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, $I^2C$, USART, general-purpose and advanced-control timers TIMx and ADC.

### 2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on $V_{DD}$ supply when present or through the $V_{BAT}$ pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when $V_{DD}$ power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long-term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

### 2.3.15 Timers and watchdogs

The low-density STM32F101xx performance line devices include an advanced-control timer, two general-purpose timers, two watchdog timers and a SysTick timer.

*Table 4* compares the features of the advanced-control and general-purpose timers.

**Table 4. Timer feature comparison**

| Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|
| TIM1 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | Yes |
| TIM2, TIM3 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |

### Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### General-purpose timers (TIMx)

There are up to two synchronizable general-purpose timers embedded in the STM32F103xx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.
The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

### Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

### Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### SysTick timer

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

## 2.3.16 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

It can be served by DMA and they support SM Bus 2.0/PM Bus.

## 2.3.17 Universal synchronous/asynchronous receiver transmitter (USART)

One of the USART interfaces is able to communicate at speeds of up to 4.5 Mbit/s. The other available interface communicates at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, IrDA SIR ENDEC support, are ISO 7816 compliant and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

## 2.3.18 Serial peripheral interface (SPI)

The SPI interface is able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPI interface can be served by the DMA controller.

## 2.3.19 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

## 2.3.20 Universal serial bus (USB)

The STM32F103xx performance line embeds a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

### 2.3.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

### 2.3.22 ADC (analog-to-digital converter)

Two 12-bit analog-to-digital converters are embedded into STM32F103xx performance line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

### 2.3.23 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < $V_{DDA}$ < 3.6 V. The temperature sensor is internally connected to the ADC12_IN16 input channel which is used to convert the sensor output voltage into a digital value.

### 2.3.24 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded. and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

# 3 Pinouts and pin description

**Figure 3. STM32F103xx performance line LQFP64 pinout**

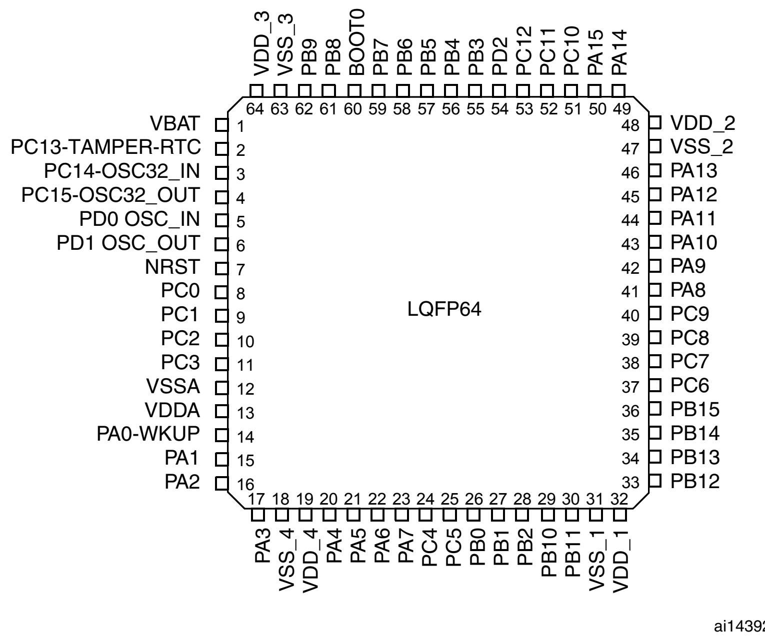


**Figure 4. STM32F103xx performance line TFBGA64 ballout**

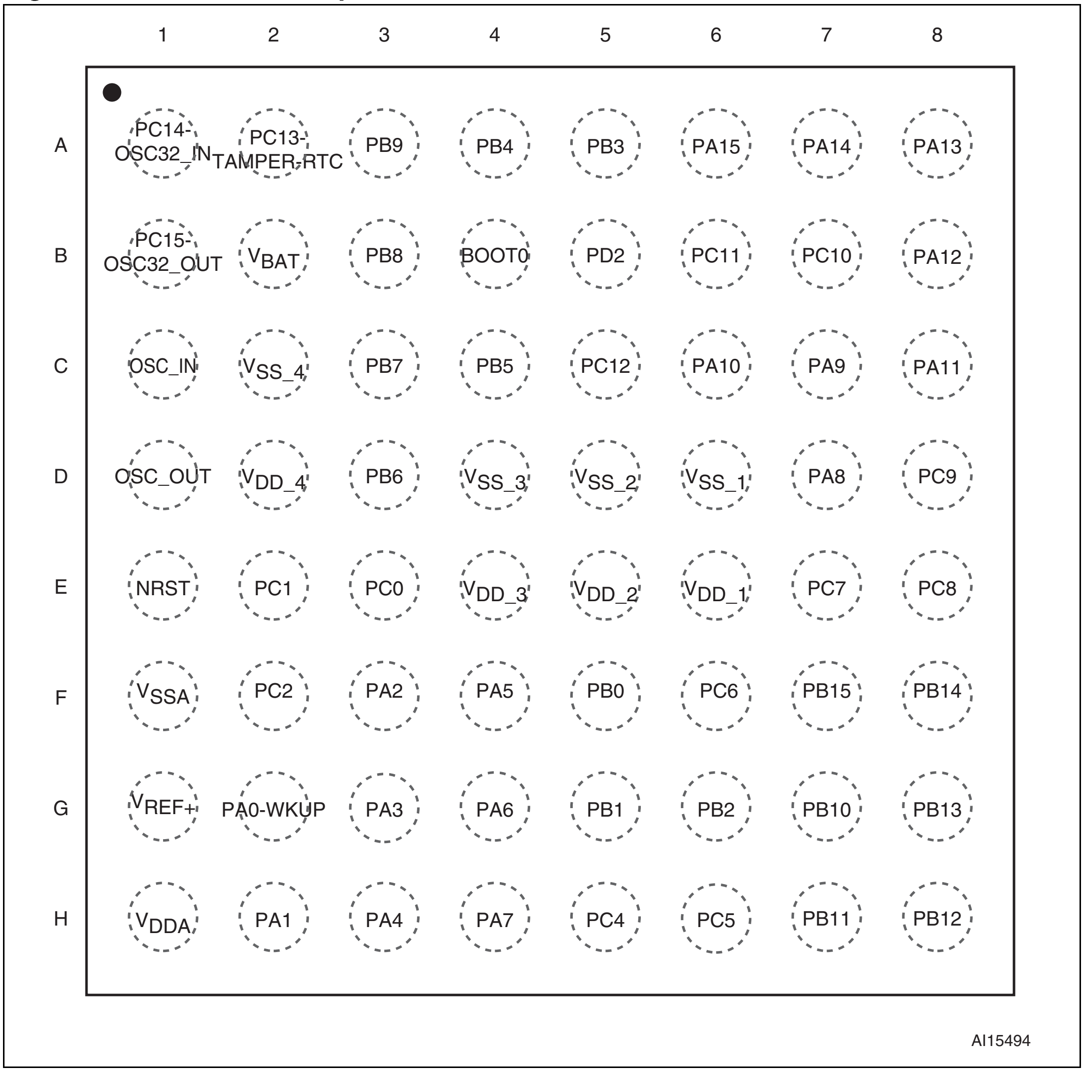


**Figure 5. STM32F103xx performance line LQFP48 pinout**

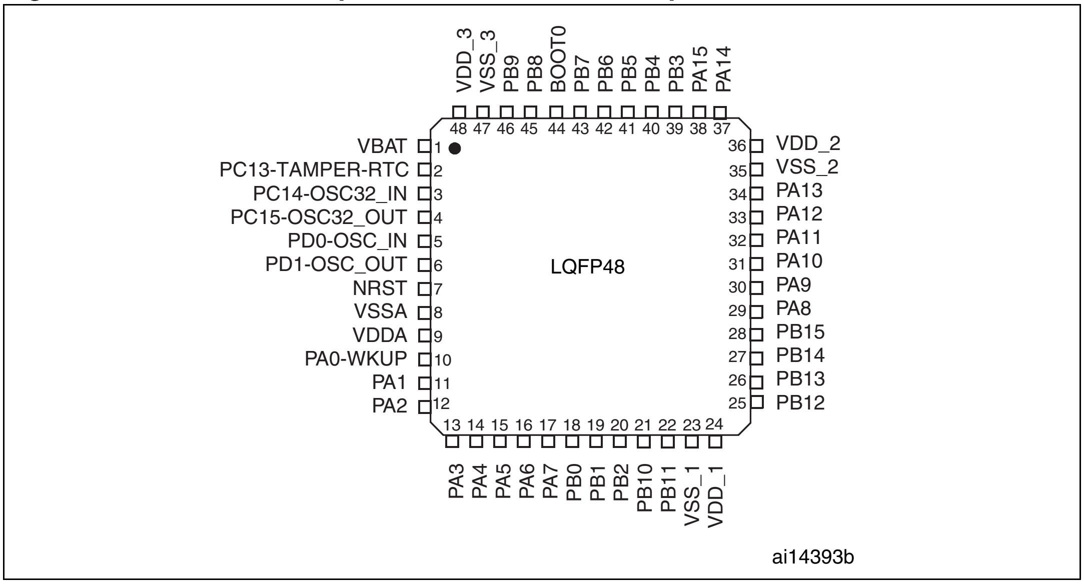



**Figure 6. STM32F101xx Medium-density access line VFQFPN36 pinout**

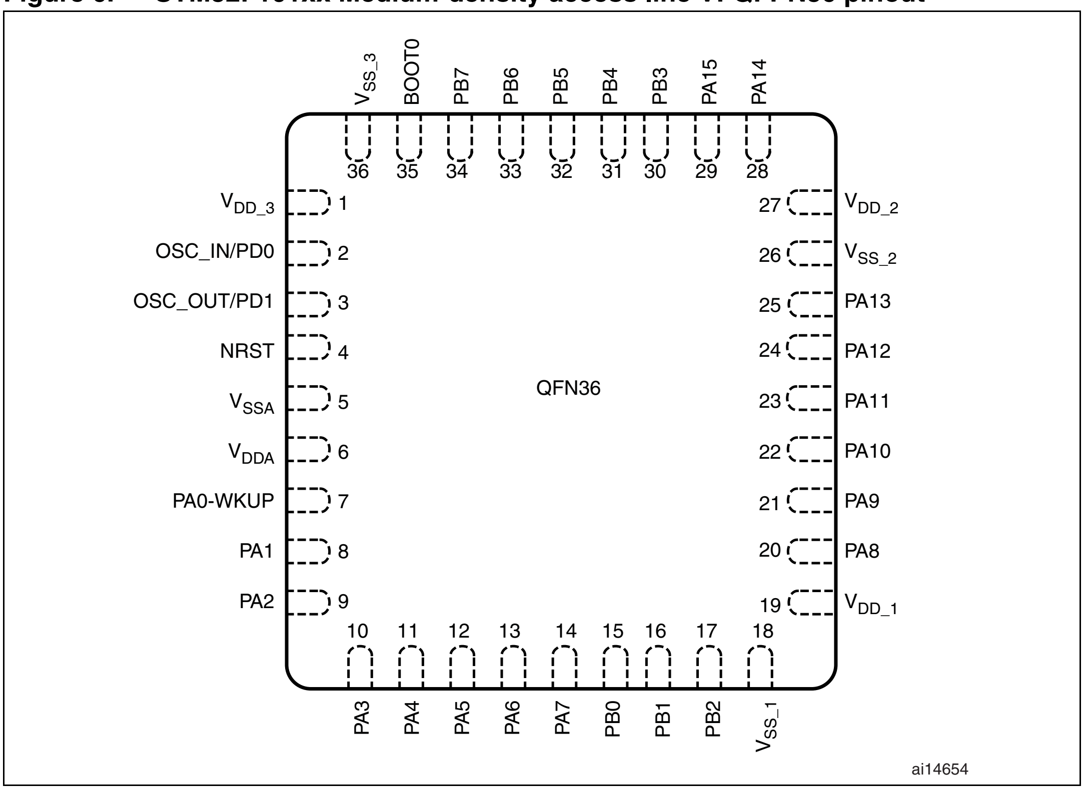


Table 5. Low-density STM32F103xx pin definitions

| Pins | | | | Pin name | Type(1) | I / O Level(2) | Main function(3) (after reset) | Alternate functions(4) | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | TFBGA64 | VFQFPN36 | | | | | Default | Remap |
| 1 | 1 | B2 | - | $V_{BAT}$ | S | | $V_{BAT}$ | | |
| 2 | 2 | A2 | - | PC13-TAMPER-RTC(5) | I/O | | PC13(6) | TAMPER-RTC | |
| 3 | 3 | A1 | - | PC14-OSC32_IN(5) | I/O | | PC14(6) | OSC32_IN | |
| 4 | 4 | B1 | - | PC15-OSC32_OUT(5) | I/O | | PC15(6) | OSC32_OUT | |
| 5 | 5 | C1 | 2 | OSC_IN | I | | OSC_IN | | |
| 6 | 6 | D1 | 3 | OSC_OUT | O | | OSC_OUT | | |
| 7 | 7 | E1 | 4 | NRST | I/O | | NRST | | |
| - | 8 | E3 | - | PC0 | I/O | | PC0 | ADC12_IN10 | |
| - | 9 | E2 | - | PC1 | I/O | | PC1 | ADC12_IN11 | |
| - | 10 | F2 | - | PC2 | I/O | | PC2 | ADC12_IN12 | |
| - | 11 | - | - | PC3 | I/O | | PC3 | ADC12_IN13 | |
| - | - | G1 | - | $V_{REF+}$(7) | S | | $V_{REF+}$ | | |
| 8 | 12 | F1 | 5 | $V_{SSA}$ | S | | $V_{SSA}$ | | |
| 9 | 13 | H1 | 6 | $V_{DDA}$ | S | | $V_{DDA}$ | | |
| 10 | 14 | G2 | 7 | PA0-WKUP | I/O | | PA0 | WKUP/USART2_CTS/ ADC12_IN0/ TIM2_CH1_ETR(8) | |
| 11 | 15 | H2 | 8 | PA1 | I/O | | PA1 | USART2_RTS/ ADC12_IN1/ TIM2_CH2(8) | |
| 12 | 16 | F3 | 9 | PA2 | I/O | | PA2 | USART2_TX/ ADC12_IN2/ TIM2_CH3(8) | |
| 13 | 17 | G3 | 10 | PA3 | I/O | | PA3 | USART2_RX/ ADC12_IN3/TIM2_CH4(8) | |
| - | 18 | C2 | - | $V_{SS\_4}$ | S | | $V_{SS\_4}$ | | |
| - | 19 | D2 | - | $V_{DD\_4}$ | S | | $V_{DD\_4}$ | | |
| 14 | 20 | H3 | 11 | PA4 | I/O | | PA4 | SPI1_NSS(8)/ USART2_CK/ADC12_IN4 | |
| 15 | 21 | F4 | 12 | PA5 | I/O | | PA5 | SPI1_SCK(8)/ ADC12_IN5 | |
| 16 | 22 | G4 | 13 | PA6 | I/O | | PA6 | SPI1_MISO(8)/ ADC12_IN6/TIM3_CH1(8) | TIM1_BKIN |
| 17 | 23 | H4 | 14 | PA7 | I/O | | PA7 | SPI1_MOSI(8)/ ADC12_IN7/TIM3_CH2(8) | TIM1_CH1N |
| - | 24 | H5 | | PC4 | I/O | | PC4 | ADC12_IN14 | |

Table 5. Low-density STM32F103xx pin definitions (continued)

| Pins | | | | Pin name | Type(1) | I / O Level(2) | Main function(3) (after reset) | Alternate functions(4) | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | TFBGA64 | VFQFPN36 | | | | | Default | Remap |
| - | 25 | H6 | | PC5 | I/O | | PC5 | ADC12_IN15 | |
| 18 | 26 | F5 | 15 | PB0 | I/O | | PB0 | ADC12_IN8/TIM3_CH3(8) | TIM1_CH2N |
| 19 | 27 | G5 | 16 | PB1 | I/O | | PB1 | ADC12_IN9/TIM3_CH4(8) | TIM1_CH3N |
| 20 | 28 | G6 | 17 | PB2 | I/O | FT | PB2/BOOT1 | | |
| 21 | 29 | G7 | - | PB10 | I/O | FT | PB10 | | TIM2_CH3 |
| 22 | 30 | H7 | - | PB11 | I/O | FT | PB11 | | TIM2_CH4 |
| 23 | 31 | D6 | 18 | $V_{SS\_1}$ | S | | $V_{SS\_1}$ | | |
| 24 | 32 | E6 | 19 | $V_{DD\_1}$ | S | | $V_{DD\_1}$ | | |
| 25 | 33 | H8 | - | PB12 | I/O | FT | PB12 | TIM1_BKIN(8) | |
| 26 | 34 | G8 | - | PB13 | I/O | FT | PB13 | TIM1_CH1N (8) | |
| 27 | 35 | F8 | - | PB14 | I/O | FT | PB14 | TIM1_CH2N (8) | |
| 28 | 36 | F7 | - | PB15 | I/O | FT | PB15 | TIM1_CH3N(8) | |
| - | 37 | F6 | - | PC6 | I/O | FT | PC6 | | TIM3_CH1 |
| | 38 | E7 | - | PC7 | I/O | FT | PC7 | | TIM3_CH2 |
| | 39 | E8 | - | PC8 | I/O | FT | PC8 | | TIM3_CH3 |
| - | 40 | D8 | - | PC9 | I/O | FT | PC9 | | TIM3_CH4 |
| 29 | 41 | D7 | 20 | PA8 | I/O | FT | PA8 | USART1_CK/ TIM1_CH1/MCO | |
| 30 | 42 | C7 | 21 | PA9 | I/O | FT | PA9 | USART1_TX(8)/ TIM1_CH2(8) | |
| 31 | 43 | C6 | 22 | PA10 | I/O | FT | PA10 | USART1_RX(8)/ TIM1_CH3 | |
| 32 | 44 | C8 | 23 | PA11 | I/O | FT | PA11 | USART1_CTS/ CAN_RX(8)/ TIM1_CH4 / USBDM | |
| 33 | 45 | B8 | 24 | PA12 | I/O | FT | PA12 | USART1_RTS/ CAN_TX(8) / TIM1_ETR / USBDP | |
| 34 | 46 | A8 | 25 | PA13 | I/O | FT | JTMS/SWDIO | | PA13 |
| 35 | 47 | D5 | 26 | $V_{SS\_2}$ | S | | $V_{SS\_2}$ | | |
| 36 | 48 | E5 | 27 | $V_{DD\_2}$ | S | | $V_{DD\_2}$ | | |
| 37 | 49 | A7 | 28 | PA14 | I/O | FT | JTCK/SWCLK | | PA14 |
| 38 | 50 | A6 | 29 | PA15 | I/O | FT | JTDI | | TIM2_CH1_ETR/ PA15 / SPI1_NSS |
| - | 51 | B7 | | PC10 | I/O | FT | PC10 | | |
| - | 52 | B6 | | PC11 | I/O | FT | PC11 | | |
| - | 53 | C5 | | PC12 | I/O | FT | PC12 | | |

**Table 5. Low-density STM32F103xx pin definitions (continued)**

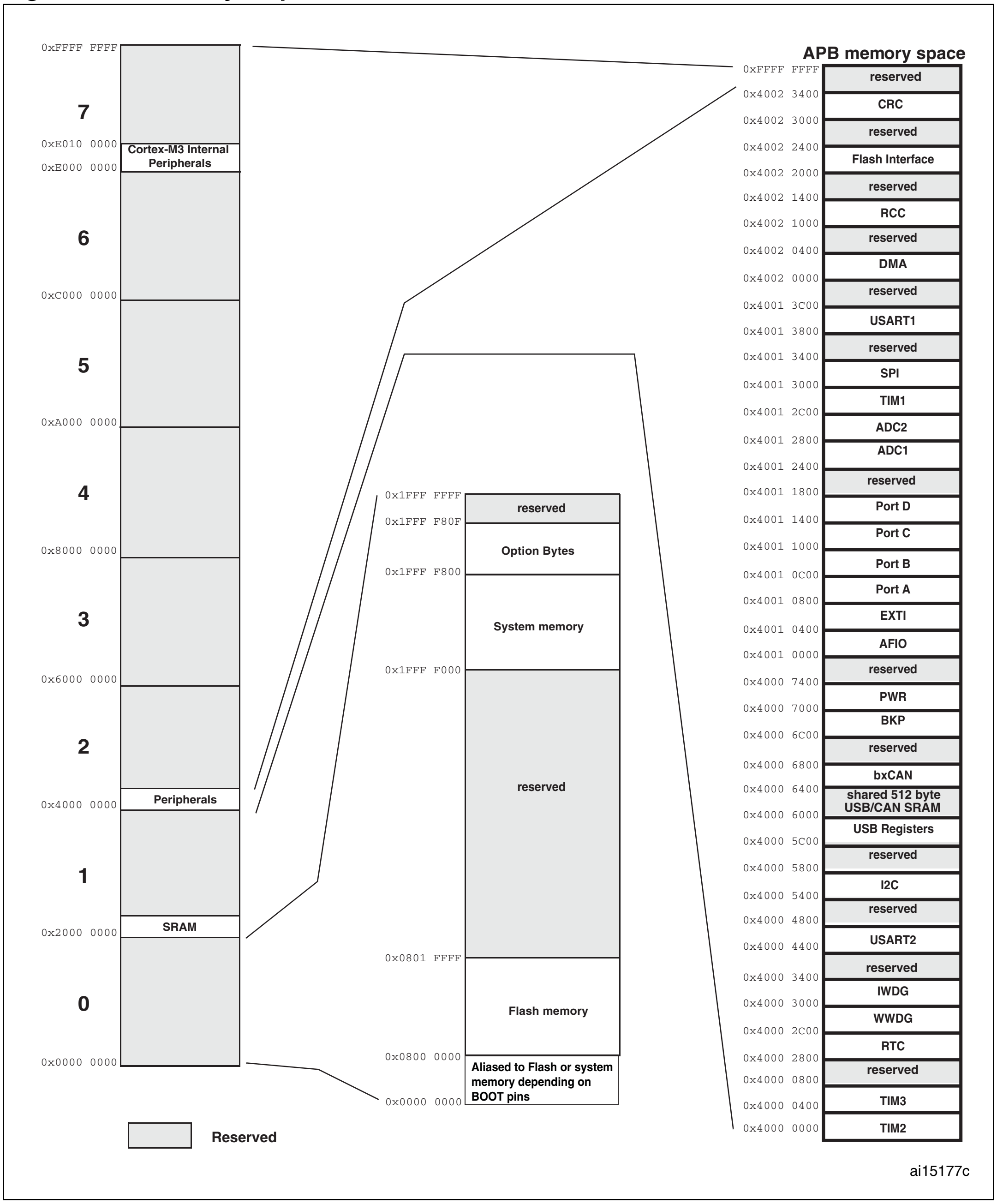
| Pins | | | | Pin name | Type[1] | I / O Level[2] | Main function[3] (after reset) | Alternate functions[4] | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | TFBGA64 | VFQFPN36 | | | | | Default | Remap |
| 5 | 5 | C1 | 2 | PD0 | I/O | FT | OSC_IN[9] | | |
| 6 | 6 | D1 | 3 | PD1 | I/O | FT | OSC_OUT[9] | | |
| | 54 | B5 | - | PD2 | I/O | FT | PD2 | TIM3_ETR | |
| 39 | 55 | A5 | 30 | PB3 | I/O | FT | JTDO | | TIM2_CH2 / PB3/ TRACESWO SPI1_SCK |
| 40 | 56 | A4 | 31 | PB4 | I/O | FT | NJTRST | | TIM3_CH1 /PB4 SPI1_MISO |
| 41 | 57 | C4 | 32 | PB5 | I/O | | PB5 | I2C1_SMBA | TIM3_CH2 / SPI1_MOSI |
| 42 | 58 | D3 | 33 | PB6 | I/O | FT | PB6 | I2C1_SCL[8]/ | USART1_TX |
| 43 | 59 | C3 | 34 | PB7 | I/O | FT | PB7 | I2C1_SDA[8] | USART1_RX |
| 44 | 60 | B4 | 35 | BOOT0 | I | | BOOT0 | | |
| 45 | 61 | B3 | - | PB8 | I/O | FT | PB8 | | I2C1_SCL /CAN_RX |
| 46 | 62 | A3 | - | PB9 | I/O | FT | PB9 | | I2C1_SDA / CAN_TX |
| 47 | 63 | D4 | 36 | $V_{SS\_3}$ | S | | $V_{SS\_3}$ | | |
| 48 | 64 | E4 | 1 | $V_{DD\_3}$ | S | | $V_{DD\_3}$ | | |

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 9*.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
7. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The $V_{REF+}$ functionality is provided instead.
8. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
9. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48 and LQFP64 packages and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.

# 4 Memory mapping

The memory map is shown in *Figure 7*.

Figure 7. Memory map



# 5 Electrical characteristics

## 5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

### 5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3.3 V (for the 2 V ≤ $V_{DD}$ ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

### 5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

### 5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

**Figure 8. Pin loading conditions**

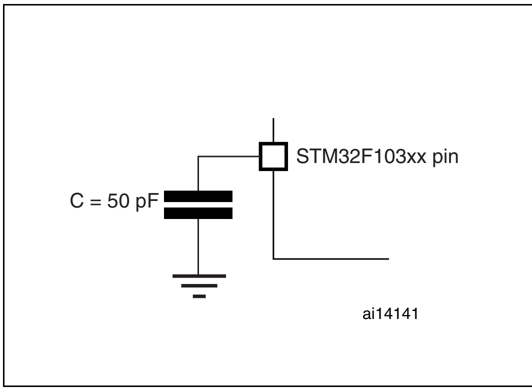
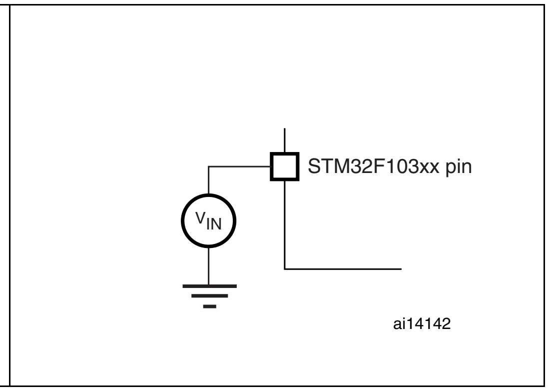
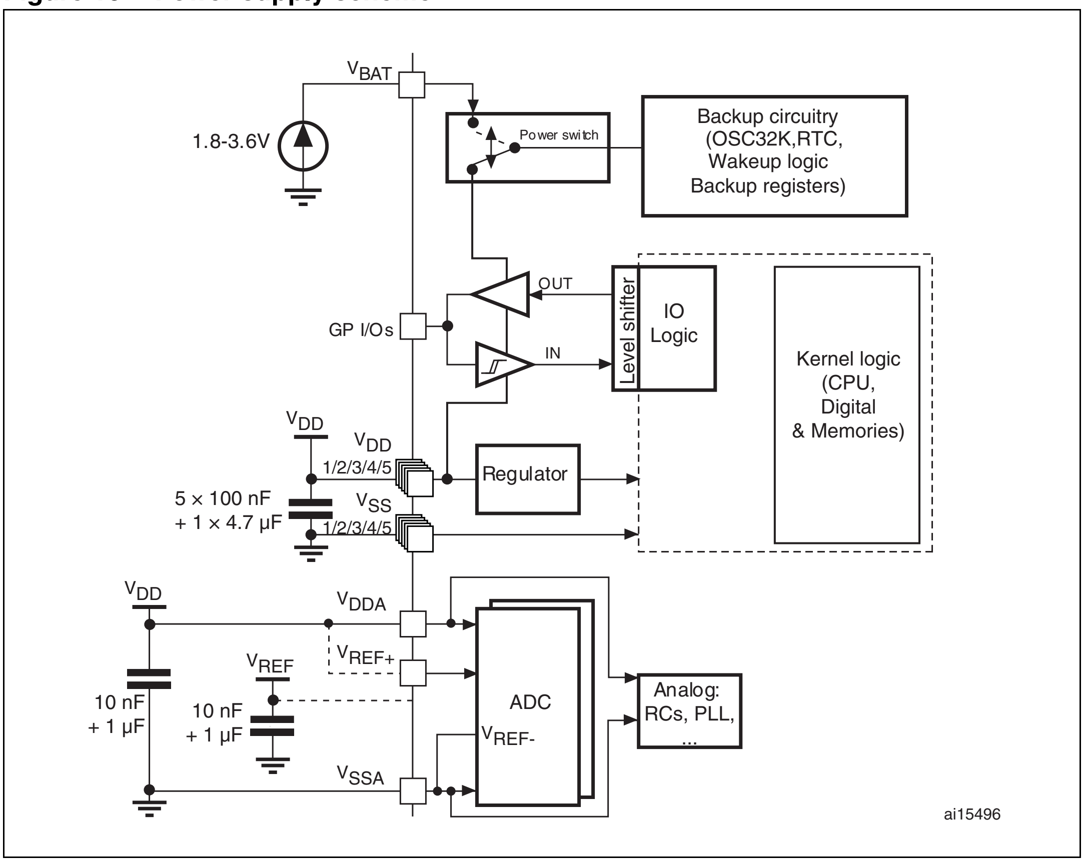



**Figure 9. Pin input voltage**




### 5.1.6 Power supply scheme

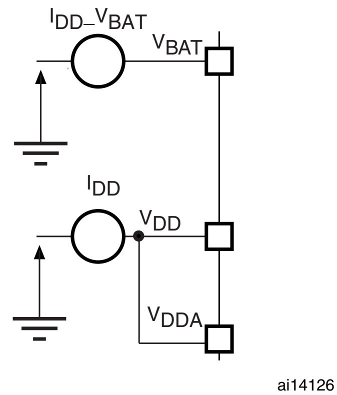
**Figure 10. Power supply scheme**




**Caution:** In *Figure 10*, the 4.7 μF capacitor must be connected to $V_{DD3}$.

### 5.1.7 Current consumption measurement

**Figure 11. Current consumption measurement scheme**




## 5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 6. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}–V_{SS}$ | External main supply voltage (including $V_{DDA}$ and $V_{DD}$)(1) | –0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on five volt tolerant pin(2) | $V_{SS} – 0.3$ | +5.5 | |
| | Input voltage on any other pin(2) | $V_{SS} – 0.3$ | $V_{DD}+0.3$ | |
| $\|\Delta V_{DDx}\|$ | Variations between different $V_{DD}$ power pins | | 50 | mV |
| $\|V_{SSX} – V_{SS}\|$ | Variations between all the different ground pins | | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)* | | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded (see *Table 7: Current characteristics*). This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}$> $V_{IN}$max while a negative injection is induced by $V_{IN} < V_{SS}$.

Table 7. Current characteristics

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}/V_{DDA}$ power lines (source)(1) | 150 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink)(1) | 150 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | – 25 | |
| $I_{INJ(PIN)}$ (2)(3) | Injected current on NRST pin | ± 5 | |
| | Injected current on HSE OSC_IN and LSE OSC_IN pins | ± 5 | |
| | Injected current on any other pin(4) | ± 5 | |
| $\Sigma I_{INJ(PIN)}$(2) | Total injected current (sum of all I/O and control pins)(4) | ± 25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.17: 12-bit ADC characteristics*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 8. Thermal characteristics

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

## 5.3 Operating conditions

### 5.3.1 General operating conditions

Table 9. General operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | | 0 | 72 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | | 0 | 36 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | | 0 | 72 | |
| $V_{DD}$ | Standard operating voltage | | 2 | 3.6 | V |
| $V_{DDA}$(1) | Analog operating voltage (ADC not used) | Must be the same potential as $V_{DD}$(2) | 2 | 3.6 | V |
| | Analog operating voltage (ADC used) | | 2.4 | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | | 1.8 | 3.6 | V |

**Table 9. General operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $P_D$ | Power dissipation at $T_A = 85$ °C for suffix 6 or $T_A = 105$ °C for suffix 7(3) | TFBGA64 | | 308 | mW |
| | | LQFP64 | | 444 | |
| | | LQFP48 | | 363 | |
| | | VFQFPN36 | | 1110 | |
| $T_A$ | Ambient temperature for 6 suffix version | Maximum power dissipation | –40 | 85 | °C |
| | | Low power dissipation(4) | –40 | 105 | |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | –40 | 105 | °C |
| | | Low power dissipation(4) | –40 | 125 | |
| $T_J$ | Junction temperature range | 6 suffix version | –40 | 105 | °C |
| | | 7 suffix version | –40 | 125 | |

1. When the ADC is used, refer to *Table 45: ADC characteristics*.
2. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and operation.
3. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 74*).
4. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 74*).

### 5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for $T_A$.

**Table 10. Operating conditions at power-up / power-down**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | | 0 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | | 20 | ∞ | |

### 5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 11. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$ | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.1 | 2.18 | 2.26 | V |
| | | PLS[2:0]=000 (falling edge) | 2 | 2.08 | 2.16 | V |
| | | PLS[2:0]=001 (rising edge) | 2.19 | 2.28 | 2.37 | V |
| | | PLS[2:0]=001 (falling edge) | 2.09 | 2.18 | 2.27 | V |
| | | PLS[2:0]=010 (rising edge) | 2.28 | 2.38 | 2.48 | V |
| | | PLS[2:0]=010 (falling edge) | 2.18 | 2.28 | 2.38 | V |
| | | PLS[2:0]=011 (rising edge) | 2.38 | 2.48 | 2.58 | V |
| | | PLS[2:0]=011 (falling edge) | 2.28 | 2.38 | 2.48 | V |
| | | PLS[2:0]=100 (rising edge) | 2.47 | 2.58 | 2.69 | V |
| | | PLS[2:0]=100 (falling edge) | 2.37 | 2.48 | 2.59 | V |
| | | PLS[2:0]=101 (rising edge) | 2.57 | 2.68 | 2.79 | V |
| | | PLS[2:0]=101 (falling edge) | 2.47 | 2.58 | 2.69 | V |
| | | PLS[2:0]=110 (rising edge) | 2.66 | 2.78 | 2.9 | V |
| | | PLS[2:0]=110 (falling edge) | 2.56 | 2.68 | 2.8 | V |
| | | PLS[2:0]=111 (rising edge) | 2.76 | 2.88 | 3 | V |
| | | PLS[2:0]=111 (falling edge) | 2.66 | 2.78 | 2.9 | V |
| $V_{PVDhyst}$(2) | PVD hysteresis | | | 100 | | mV |
| $V_{POR/PDR}$ | Power on/power down reset threshold | Falling edge | 1.8(1) | 1.88 | 1.96 | V |
| | | Rising edge | 1.84 | 1.92 | 2.0 | V |
| $V_{PDRhyst}$(2) | PDR hysteresis | | | 40 | | mV |
| $T_{RSTTEMPO}$(2) | Reset temporization | | 1 | 2.5 | 4.5 | ms |

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

### 5.3.4 Embedded reference voltage

The parameters given in *Table 12* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 12. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +105 °C | 1.16 | 1.20 | 1.26 | V |
| | | –40 °C < $T_A$ < +85 °C | 1.16 | 1.20 | 1.24 | V |
| $T_{S\_vrefint}$(1) | ADC sampling time when reading the internal reference voltage | | | 5.1 | 17.1(2) | µs |
| $V_{RERINT}$(2) | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3 V ±10 mV | | | 10 | mV |
| $T_{Coeff}$(2) | Temperature coefficient | | | | 100 | ppm/°C |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

### 5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

#### Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 13*, *Table 14* and *Table 15* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

Table 13. Maximum current consumption in Run mode, code with data processing running from Flash

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max[1] | | Unit |
|---|---|---|---|---|---|---|
| | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Run mode | External clock[2], all peripherals enabled | 72 MHz | 45 | 46 | mA |
| | | | 48 MHz | 32 | 33 | |
| | | | 36 MHz | 26 | 27 | |
| | | | 24 MHz | 18 | 19 | |
| | | | 16 MHz | 13 | 14 | |
| | | | 8 MHz | 7 | 8 | |
| | | External clock[2], all peripherals disabled | 72 MHz | 30 | 31 | |
| | | | 48 MHz | 23 | 24 | |
| | | | 36 MHz | 19 | 20 | |
| | | | 24 MHz | 13 | 14 | |
| | | | 16 MHz | 10 | 11 | |
| | | | 8 MHz | 6 | 7 | |

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

Table 14. Maximum current consumption in Run mode, code with data processing running from RAM

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max[1] | | Unit |
|---|---|---|---|---|---|---|
| | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Run mode | External clock[2], all peripherals enabled | 72 MHz | 41 | 42 | mA |
| | | | 48 MHz | 27 | 28 | |
| | | | 36 MHz | 20 | 21 | |
| | | | 24 MHz | 14 | 15 | |
| | | | 16 MHz | 10 | 11 | |
| | | | 8 MHz | 6 | 7 | |
| | | External clock[2], all peripherals disabled | 72 MHz | 27 | 28 | |
| | | | 48 MHz | 19 | 20 | |
| | | | 36 MHz | 15 | 16 | |
| | | | 24 MHz | 10 | 11 | |
| | | | 16 MHz | 7 | 8 | |
| | | | 8 MHz | 5 | 6 | |

1. Based on characterization, tested in production at $V_{DD}$ max, $f_{HCLK}$ max.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled**

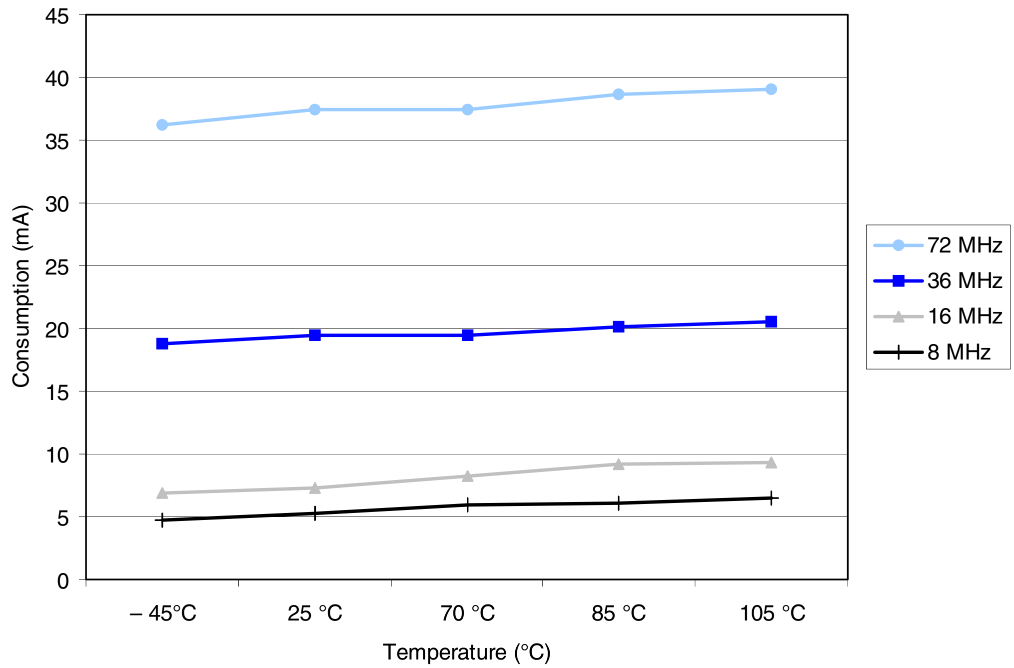



**Figure 13. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled**

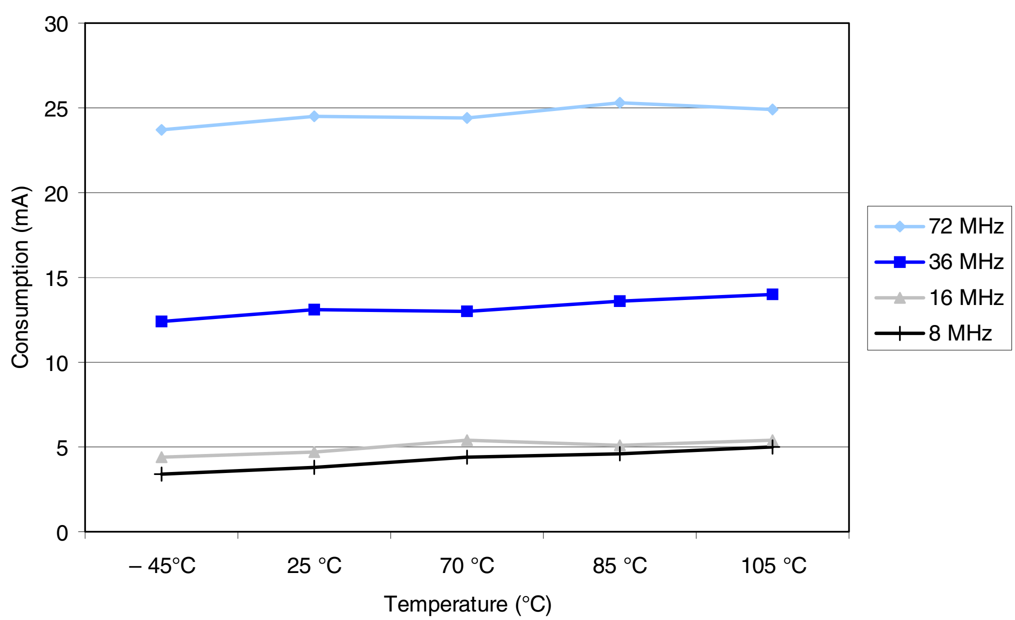


**Table 15. Maximum current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max[1] | | Unit |
|---|---|---|---|---|---|---|
| | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | External clock[2], all peripherals enabled | 72 MHz | 26 | 27 | mA |
| | | | 48 MHz | 17 | 18 | |
| | | | 36 MHz | 14 | 15 | |
| | | | 24 MHz | 10 | 11 | |
| | | | 16 MHz | 7 | 8 | |
| | | | 8 MHz | 4 | 5 | |
| | | External clock[2], all peripherals disabled | 72 MHz | 7.5 | 8 | |
| | | | 48 MHz | 6 | 6.5 | |
| | | | 36 MHz | 5 | 5.5 | |
| | | | 24 MHz | 4.5 | 5 | |
| | | | 16 MHz | 4 | 4.5 | |
| | | | 8 MHz | 3 | 4 | |

1. based on characterization, tested in production at $V_{DD\ max}$, $f_{HCLK}$ max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 16. Typical and maximum current consumptions in Stop and Standby modes**

| Symbol | Parameter | Conditions | Typ(1) | | | Max | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{DD}/V_{BAT}$ = 2.0 V | $V_{DD}/V_{BAT}$ = 2.4 V | $V_{DD}/V_{BAT}$ = 3.3 V | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Stop mode | Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | - | 21.3 | 21.7 | 160 | 200 | µA |
| | | Regulator in Low Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | - | 11.3 | 11.7 | 145 | 185 | |
| | Supply current in Standby mode | Low-speed internal RC oscillator and independent watchdog ON | - | 2.75 | 3.4 | - | - | |
| | | Low-speed internal RC oscillator ON, independent watchdog OFF | - | 2.55 | 3.2 | - | - | |
| | | Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF | - | 1.55 | 1.9 | 3.2 | 4.5 | |
| $I_{DD\_VBAT}$ | Backup domain supply current | Low-speed oscillator and RTC ON | 0.9 | 1.1 | 1.4 | 1.9(2) | 2.2 | |

1. Typical values are measured at $T_A$ = 25 °C.
2. Based on characterization, not tested in production.

**Figure 14. Typical current consumption on $V_{BAT}$ with RTC on versus temperature at different $V_{BAT}$ values**

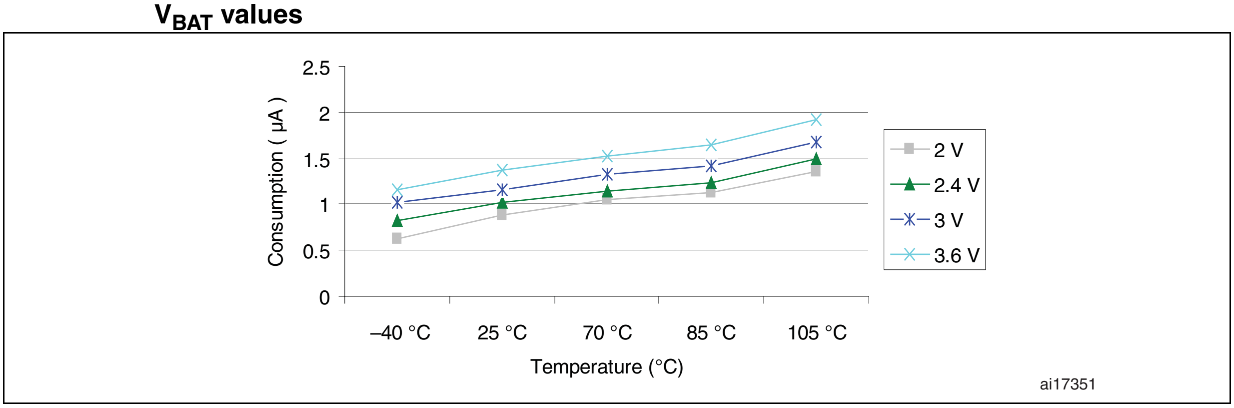


**Figure 15. Typical current consumption in Stop mode with regulator in Run mode versus temperature at $V_{DD}$ = 3.3 V and 3.6 V**

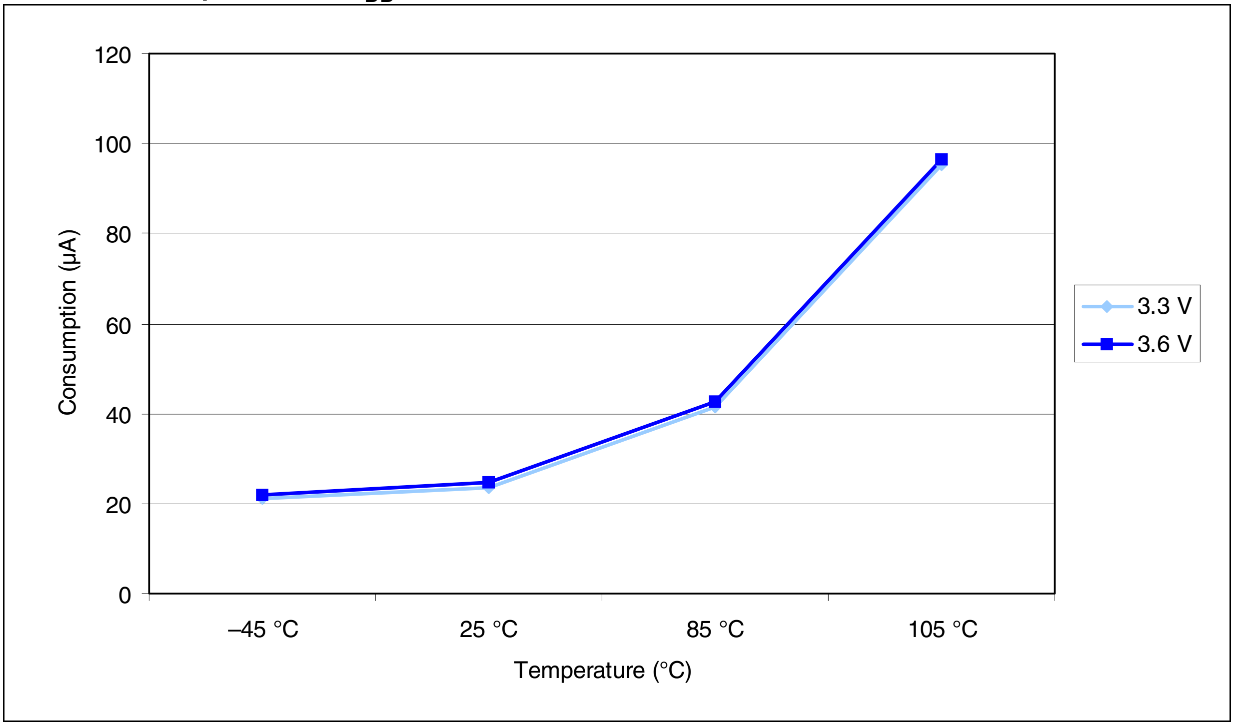



**Figure 16. Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at $V_{DD}$ = 3.3 V and 3.6 V**

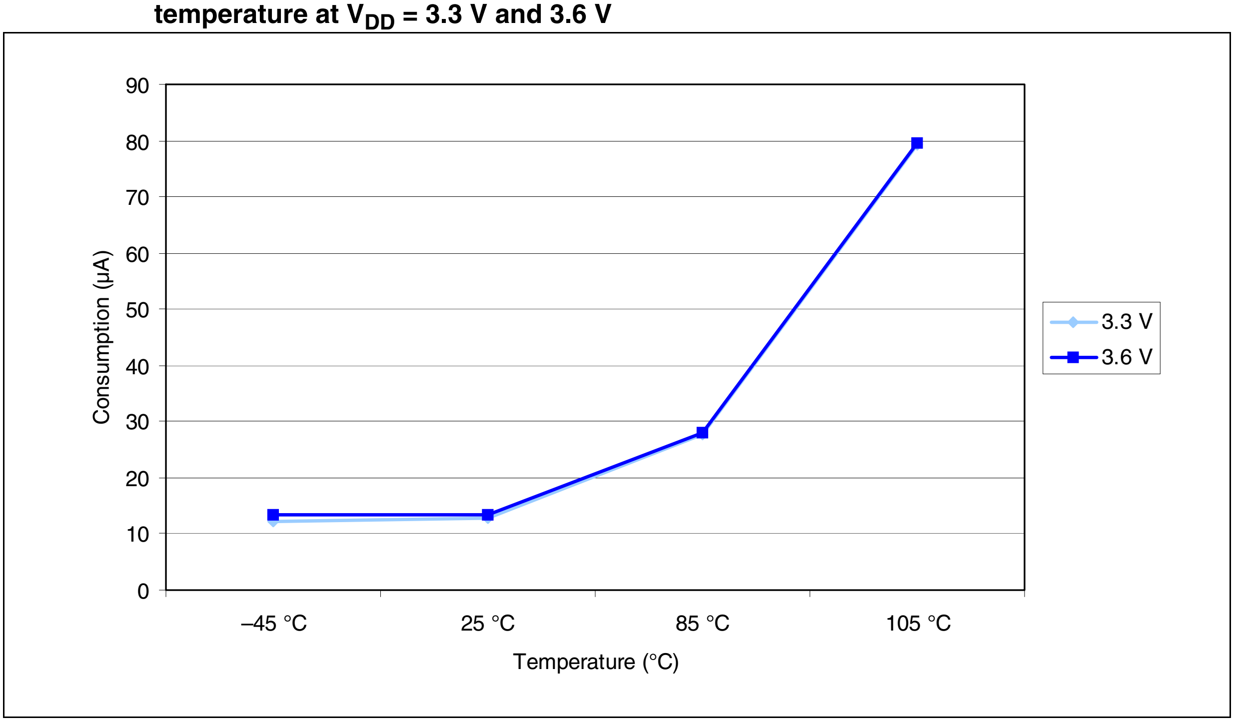
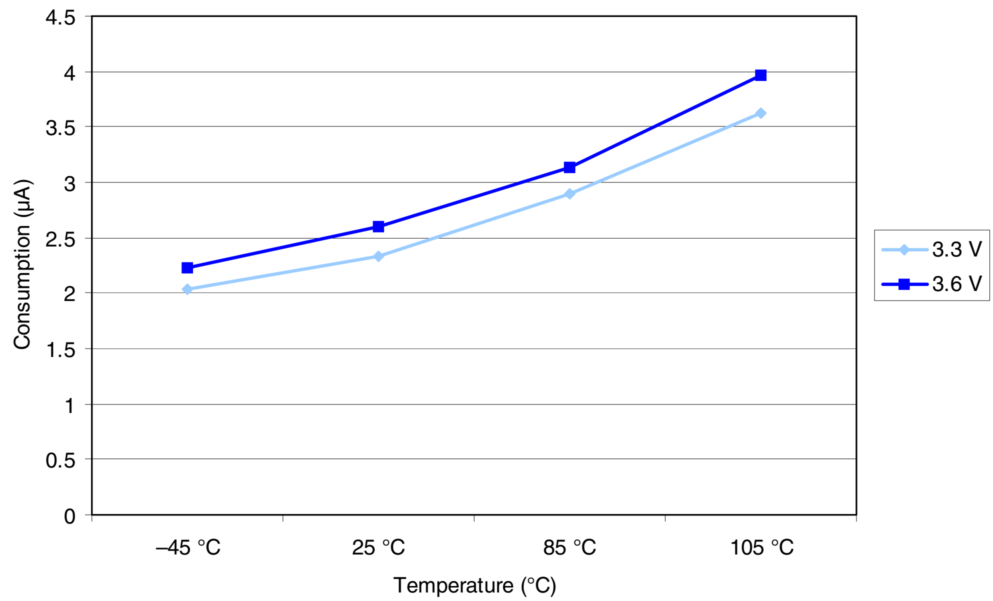


**Figure 17. Typical current consumption in Standby mode versus temperature at $V_{DD}$ = 3.3 V and 3.6 V**




### Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK}2 = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

**Table 17. Typical current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ[1] All peripherals enabled[2] | Typ[1] All peripherals disabled | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Run mode | External clock[3] | 72 MHz | 31.3 | 24.5 | mA |
| | | | 48 MHz | 21.9 | 17.4 | |
| | | | 36 MHz | 17.2 | 13.8 | |
| | | | 24 MHz | 11.2 | 8.9 | |
| | | | 16 MHz | 8.1 | 6.6 | |
| | | | 8 MHz | 5 | 4.2 | |
| | | | 4 MHz | 3 | 2.6 | |
| | | | 2 MHz | 2 | 1.8 | |
| | | | 1 MHz | 1.5 | 1.4 | |
| | | | 500 kHz | 1.2 | 1.2 | |
| | | | 125 kHz | 1.05 | 1 | |
| | | Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency | 64 MHz | 27.6 | 21.6 | mA |
| | | | 48 MHz | 21.2 | 16.7 | |
| | | | 36 MHz | 16.5 | 13.1 | |
| | | | 24 MHz | 10.5 | 8.2 | |
| | | | 16 MHz | 7.4 | 5.9 | |
| | | | 8 MHz | 4.3 | 3.6 | |
| | | | 4 MHz | 2.4 | 2 | |
| | | | 2 MHz | 1.5 | 1.3 | |
| | | | 1 MHz | 1 | 0.9 | |
| | | | 500 kHz | 0.7 | 0.65 | |
| | | | 125 kHz | 0.5 | 0.45 | |

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

**Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ(1) All peripherals enabled(2) | Typ(1) All peripherals disabled | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Sleep mode | External clock(3) | 72 MHz | 12.6 | 5.3 | mA |
| | | | 48 MHz | 8.7 | 3.8 | |
| | | | 36 MHz | 6.7 | 3.1 | |
| | | | 24 MHz | 4.8 | 2.3 | |
| | | | 16 MHz | 3.4 | 1.8 | |
| | | | 8 MHz | 2 | 1.2 | |
| | | | 4 MHz | 1.5 | 1.1 | |
| | | | 2 MHz | 1.25 | 1 | |
| | | | 1 MHz | 1.1 | 0.98 | |
| | | | 500 kHz | 1.05 | 0.96 | |
| | | | 125 kHz | 1 | 0.95 | |
| | | Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency | 64 MHz | 10.6 | 4.2 | |
| | | | 48 MHz | 8.1 | 3.2 | |
| | | | 36 MHz | 6.1 | 2.5 | |
| | | | 24 MHz | 4.2 | 1.7 | |
| | | | 16 MHz | 2.8 | 1.2 | |
| | | | 8 MHz | 1.4 | 0.55 | |
| | | | 4 MHz | 0.9 | 0.5 | |
| | | | 2 MHz | 0.7 | 0.45 | |
| | | | 1 MHz | 0.55 | 0.42 | |
| | | | 500 kHz | 0.48 | 0.4 | |
| | | | 125 kHz | 0.4 | 0.38 | |

1. Typical values are measures at $T_A$ = 25 °C, $V_{DD}$ = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and $V_{DD}$ supply voltage conditions summarized in *Table 6*

**Table 19. Peripheral current consumption(1)**

| Peripheral | | Typical consumption at 25 °C | Unit |
|---|---|---|---|
| APB1 | TIM2 | 1.2 | mA |
| | TIM3 | 1.2 | |
| | USART2 | 0.35 | |
| | I2C | 0.39 | |
| | USB | 0.65 | |
| | CAN | 0.72 | |
| APB2 | GPIO A | 0.47 | mA |
| | GPIO B | 0.47 | |
| | GPIO C | 0.47 | |
| | GPIO D | 0.47 | |
| | ADC1(2) | 1.81 | |
| | ADC2 | 1.78 | |
| | TIM1 | 1.6 | |
| | SPI | 0.43 | |
| | USART1 | 0.85 | |

1. $f_{HCLK}$ = 72 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. Specific conditions for ADC: $f_{HCLK}$ = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2/4}$, ADON bit in the ADC_CR2 register is set to 1.

## 5.3.6 External clock source characteristics

### High-speed external user clock generated from an external source

The characteristics given in *Table 20* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

**Table 20. High-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | User external clock source frequency(1) | | 1 | 8 | 25 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | | $0.3V_{DD}$ | V |
| $t_{w(HSE)}$<br>$t_{w(HSE)}$ | OSC_IN high or low time(1) | | 16 | | | ns |
| $t_{r(HSE)}$<br>$t_{f(HSE)}$ | OSC_IN rise or fall time(1) | | | | 20 | ns |
| $C_{in(HSE)}$ | OSC_IN input capacitance(1) | | | 5 | | pF |
| $DuCy_{(HSE)}$ | Duty cycle | | 45 | | 55 | % |
| $I_L$ | OSC_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | | | ±1 | µA |

1. Guaranteed by design, not tested in production.

## Low-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

**Table 21. Low-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | User External clock source frequency(1) | | | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | | $0.3V_{DD}$ | V |
| $t_{w(LSE)}$<br>$t_{w(LSE)}$ | OSC32_IN high or low time(1) | | 450 | | | ns |
| $t_{r(LSE)}$<br>$t_{f(LSE)}$ | OSC32_IN rise or fall time(1) | | | | 50 | ns |
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | | | 5 | | pF |
| $DuCy_{(LSE)}$ | Duty cycle | | 30 | | 70 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | | | ±1 | µA |

1. Guaranteed by design, not tested in production.

Figure 18. High-speed external clock source AC timing diagram

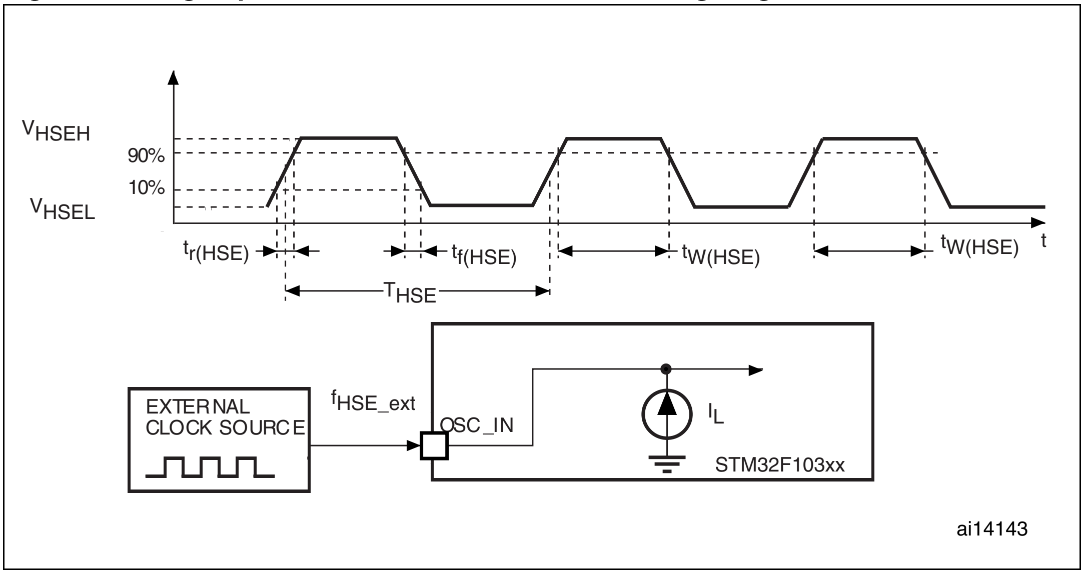
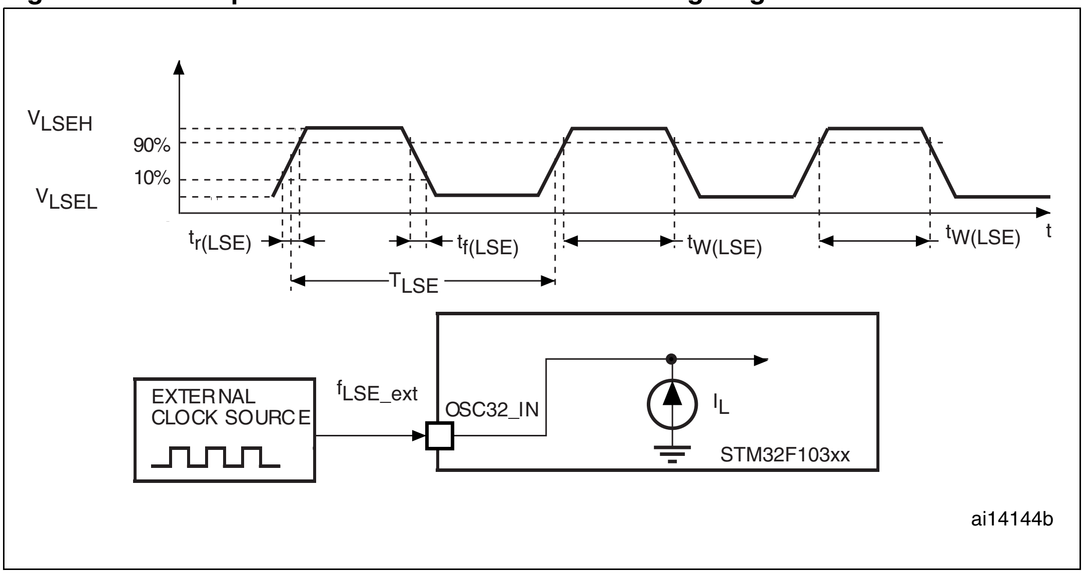



Figure 19. Low-speed external clock source AC timing diagram




## High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

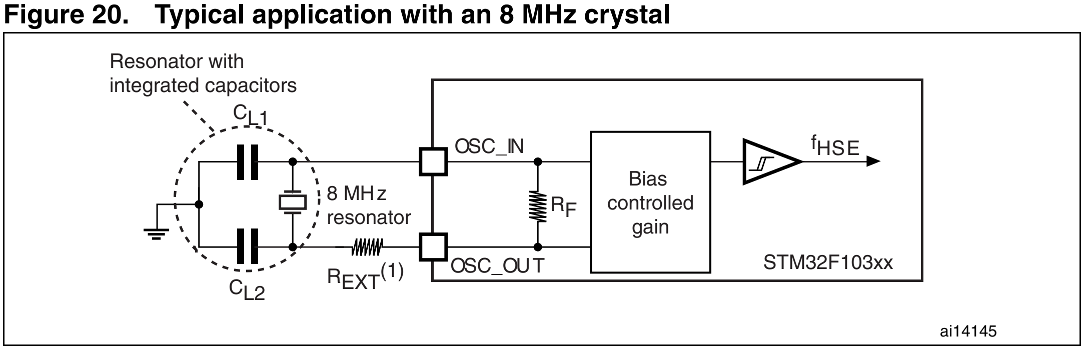
**Table 22. HSE 4-16 MHz oscillator characteristics(1) (2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | | 4 | 8 | 16 | MHz |
| $R_F$ | Feedback resistor | | | 200 | | kΩ |
| C | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)(3) | $R_S$ = 30 Ω | | 30 | | pF |
| $i_2$ | HSE driving current | $V_{DD}$ = 3.3 V, $V_{IN}$ = $V_{SS}$ with 30 pF load | | | 1 | mA |
| $g_m$ | Oscillator transconductance | Startup | 25 | | | mA/V |
| $t_{SU(HSE)}$(4) | startup time | $V_{DD}$ is stabilized | | 2 | | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 20*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$. Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

**Figure 20. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

## Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 23. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz) (1)**

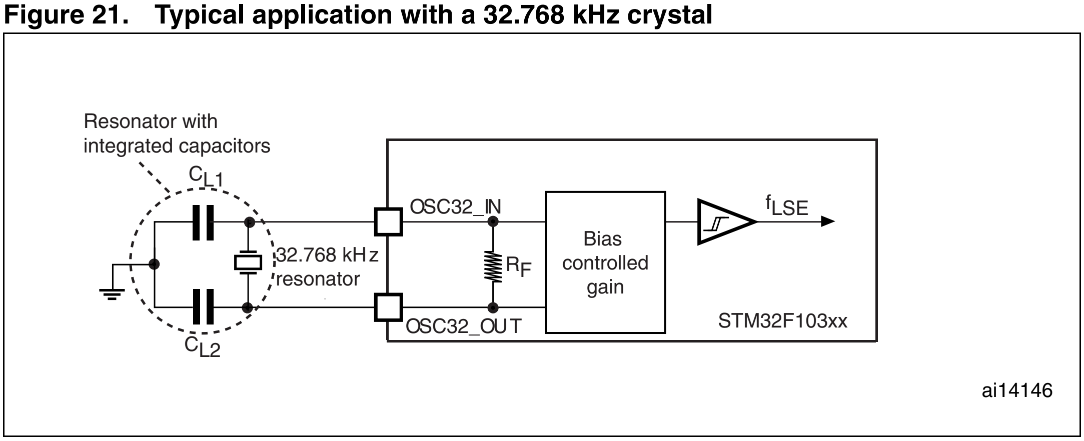
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor | | | 5 | | MΩ |
| C(2) | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)(3) | $R_S$ = 30 kΩ | | | 15 | pF |
| $I_2$ | LSE driving current | $V_{DD}$ = 3.3 V, $V_{IN} = V_{SS}$ | | | 1.4 | µA |
| $g_m$ | Oscillator Transconductance | | 5 | | | µA/V |
| $t_{SU(LSE)}$(4) | startup time | $V_{DD}$ is stabilized | | 3 | | s |

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small $R_S$ value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

*Note:* *For $C_{L1}$ and $C_{L2}$ it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. $C_{L1}$ and $C_{L2}$, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$.*
*Load capacitance $C_L$ has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where $C_{stray}$ is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.*

**Caution:** To avoid exceeding the maximum value of $C_{L1}$ and $C_{L2}$ (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq$ 7 pF. Never use a resonator with a load capacitance of 12.5 pF.
**Example:** if you choose a resonator with a load capacitance of $C_L$ = 6 pF, and $C_{stray}$ = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

**Figure 21. Typical application with a 32.768 kHz crystal**




## 5.3.7 Internal clock source characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

## High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics(1)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | | | | 8 | | MHz |
| $ACC_{HSI}$ | Accuracy of the HSI oscillator | User-trimmed with the RCC_CR register(2) | | | | 1(3) | % |
| | | Factory-calibrated(4) | $T_A$ = –40 to 105 °C | –2 | | 2.5 | % |
| | | | $T_A$ = –10 to 85 °C | –1.5 | | 2.2 | % |
| | | | $T_A$ = 0 to 70 °C | –1.3 | | 2 | % |
| | | | $T_A$ = 25 °C | –1.1 | | 1.8 | % |
| $t_{su(HSI)}$(4) | HSI oscillator startup time | | | 1 | | 2 | µs |
| $I_{DD(HSI)}$(4) | HSI oscillator power consumption | | | | 80 | 100 | µA |

1. $V_{DD}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website www.st.com.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.

## Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$(2) | Frequency | 30 | 40 | 60 | kHz |
| $t_{su(LSI)}$(3) | LSI oscillator startup time | | | 85 | µs |
| $I_{DD(LSI)}$(3) | LSI oscillator power consumption | | 0.65 | 1.2 | µA |

1. $V_{DD}$ = 3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

## Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

Table 26. Low-power mode wakeup timings

| Symbol | Parameter | Typ | Unit |
|---|---|---|---|
| $t_{WUSLEEP}$(1) | Wakeup from Sleep mode | 1.8 | µs |
| $t_{WUSTOP}$(1) | Wakeup from Stop mode (regulator in run mode) | 3.6 | µs |
| | Wakeup from Stop mode (regulator in low power mode) | 5.4 | |
| $t_{WUSTDBY}$(1) | Wakeup from Standby mode | 50 | µs |

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

### 5.3.8 PLL characteristics

The parameters given in *Table 27* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

Table 27. PLL characteristics

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min(1) | Typ | Max(1) | |
| $f_{PLL\_IN}$ | PLL input clock(2) | 1 | 8.0 | 25 | MHz |
| | PLL input clock duty cycle | 40 | | 60 | % |
| $f_{PLL\_OUT}$ | PLL multiplier output clock | 16 | | 72 | MHz |
| $t_{LOCK}$ | PLL lock time | | | 200 | µs |
| Jitter | Cycle-to-cycle jitter | | | 300 | ps |

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{PLL\_OUT}$.

### 5.3.9 Memory characteristics

#### Flash memory

The characteristics are given at $T_A$ = –40 to 105 °C unless otherwise specified.

Table 28. Flash memory characteristics

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | 16-bit programming time | $T_A$ = –40 to +105 °C | 40 | 52.5 | 70 | µs |
| $t_{ERASE}$ | Page (1 KB) erase time | $T_A$ = –40 to +105 °C | 20 | | 40 | ms |
| $t_{ME}$ | Mass erase time | $T_A$ = –40 to +105 °C | 20 | | 40 | ms |

**Table 28. Flash memory characteristics (continued)**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | Read mode<br>$f_{HCLK}$ = 72 MHz with 2 wait states, $V_{DD}$ = 3.3 V | | | 20 | mA |
| | | Write / Erase modes<br>$f_{HCLK}$ = 72 MHz, $V_{DD}$ = 3.3 V | | | 5 | mA |
| | | Power-down mode / Halt,<br>$V_{DD}$ = 3.0 to 3.6 V | | | 50 | µA |
| $V_{prog}$ | Programming voltage | | 2 | | 3.6 | V |

1. Guaranteed by design, not tested in production.

**Table 29. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min(1) | Typ | Max | |
| $N_{END}$ | Endurance | $T_A$ = –40 to +85 °C (6 suffix versions)<br>$T_A$ = –40 to +105 °C (7 suffix versions) | 10 | | | kcycles |
| $t_{RET}$ | Data retention | 1 kcycle(2) at $T_A$ = 85 °C | 30 | | | Years |
| | | 1 kcycle(2) at $T_A$ = 105 °C | 10 | | | |
| | | 10 kcycles(2) at $T_A$ = 55 °C | 20 | | | |

1. Based on characterization, not tested in production.
2. Cycling performed over the whole temperature range.

### 5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 30*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 30. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD} = 3.3$ V, $T_A = +25$ °C, $f_{HCLK} = 72$ MHz conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD} = 3.3$ V, $T_A = +25$ °C, $f_{HCLK} = 72$ MHz conforms to IEC 61000-4-4 | 4A |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

**Table 31. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] | | Unit |
|---|---|---|---|---|---|---|
| | | | | 8/48 MHz | 8/72 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD} = 3.3$ V, $T_A = 25$ °C | 0.1 to 30 MHz | 12 | 12 | dBµV |
| | | | 30 to 130 MHz | 22 | 19 | |
| | | | 130 MHz to 1GHz | 23 | 29 | |
| | | | SAE EMI Level | 4 | 4 | - |

## 5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 32. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value[1] | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C conforming to JESD22-C101 | II | 500 | |

1. Based on characterization results, not tested in production.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 33. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 5.3.12 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 34* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

**Table 34. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | TTL ports | –0.5 | | 0.8 | V |
| $V_{IH}$ | Standard IO input high level voltage | | 2 | | $V_{DD}$+0.5 | |
| | IO FT[1] input high level voltage | | 2 | | 5.5V | |
| $V_{IL}$ | Input low level voltage | CMOS ports | –0.5 | | 0.35 $V_{DD}$ | V |
| $V_{IH}$ | Input high level voltage | | 0.65 $V_{DD}$ | | $V_{DD}$+0.5 | |
| $V_{hys}$ | Standard IO Schmitt trigger voltage hysteresis[2] | | 200 | | | mV |
| | IO FT Schmitt trigger voltage hysteresis[2] | | 5% $V_{DD}$[3] | | | mV |
| $I_{lkg}$ | Input leakage current [4] | $V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os | | | ±1 | µA |
| | | $V_{IN}$= 5 V I/O FT | | | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistor[5] | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor[5] | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | kΩ |
| $C_{IO}$ | I/O pin capacitance | | | 5 | | pF |

1. FT = Five-volt tolerant.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required), their characteristics consider the most strict CMOS-technology or TTL parameters:

- For $V_{IH}$:
  - if $V_{DD}$ is in the [2.00 V - 3.08 V] range: CMOS characteristics but TTL included
  - if $V_{DD}$ is in the [3.08 V - 3.60 V] range: TTL characteristics but CMOS included
- For $V_{IL}$:
  - if $V_{DD}$ is in the [2.00 V - 2.28 V] range: TTL characteristics but CMOS included
  - if $V_{DD}$ is in the [2.28 V - 3.60 V] range: CMOS characteristics but TTL included

### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed $V_{OL}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD}$ (see *Table 7*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS}$ (see *Table 7*).

### Output voltage levels

Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

**Table 35. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | TTL port<br>$I_{IO}$ = +8 mA<br>2.7 V < $V_{DD}$ < 3.6 V | | 0.4 | V |
| $V_{OH}$(2) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}$–0.4 | | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | CMOS port<br>$I_{IO}$ =+ 8mA<br>2.7 V < $V_{DD}$ < 3.6 V | | 0.4 | V |
| $V_{OH}$(2) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | 2.4 | | |
| $V_{OL}$(1)(3) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO}$ = +20 mA<br>2.7 V < $V_{DD}$ < 3.6 V | | 1.3 | V |
| $V_{OH}$(2)(3) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}$–1.3 | | |
| $V_{OL}$(1)(3) | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO}$ = +6 mA<br>2 V < $V_{DD}$ < 2.7 V | | 0.4 | V |
| $V_{OH}$(2)(3) | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}$–0.4 | | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
3. Based on characterization data, not tested in production.

## Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 22* and *Table 36*, respectively.

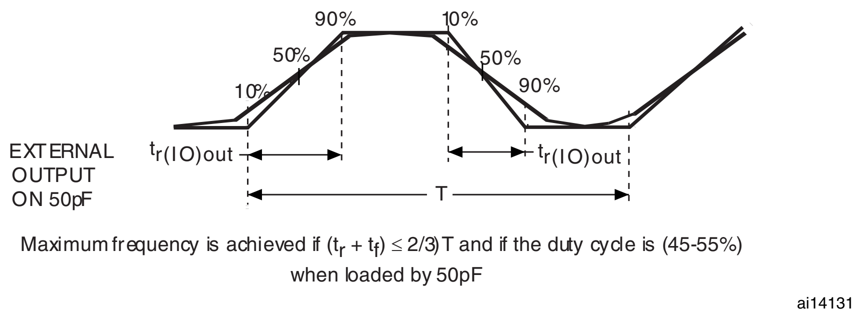
Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 36. I/O AC characteristics(1)**

| MODEx[1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 10 | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 2 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 125(3) | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | | 125(3) | |
| 01 | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 10 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | | 25(3) | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | | 25(3) | |
| 11 | $F_{max(IO)out}$ | Maximum frequency(2) | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 50 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 30 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 20 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 5(3) | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 8(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 12(3) | |
| | $t_{r(IO)out}$ | Output low to high level rise time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 5(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | | 8(3) | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | | 12(3) | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | | 10 | | ns |

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 22*.
3. Guaranteed by design, not tested in production.

**Figure 22. I/O AC characteristics definition**




### 5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 34*).

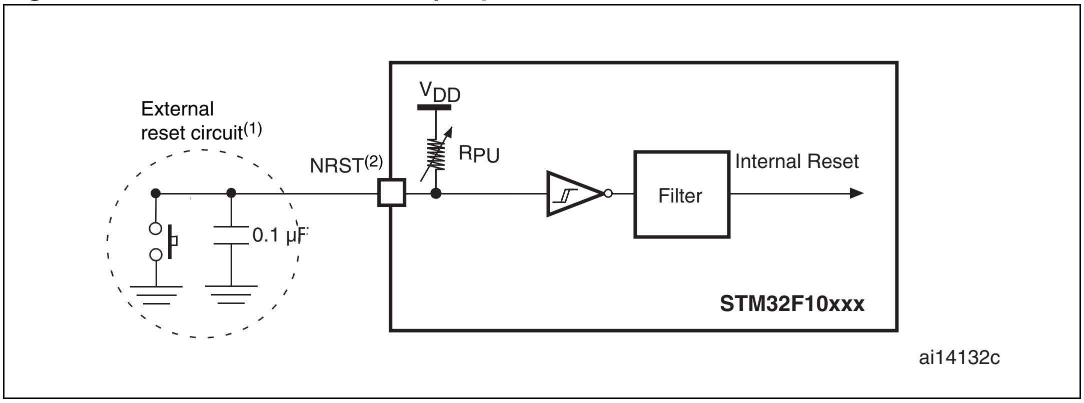
Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 37. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ (1) | NRST Input low level voltage | | –0.5 | | 0.8 | V |
| $V_{IH(NRST)}$ (1) | NRST Input high level voltage | | 2 | | $V_{DD}$+0.5 | V |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | | | 200 | | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor(2) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$ (1) | NRST Input filtered pulse | | | | 100 | ns |
| $V_{NF(NRST)}$ (1) | NRST Input not filtered pulse | | 300 | | | ns |

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

**Figure 23. Recommended NRST pin protection**




2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 37*. Otherwise the reset will not be taken into account by the device.

## 5.3.14 TIM timer characteristics

The parameters given in *Table 38* are guaranteed by design.

Refer to *Section 5.3.12: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 38. TIMx(1) characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | 13.9 | | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 72 MHz | 0 | 36 | MHz |
| $Res_{TIM}$ | Timer resolution | | | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | 0.0139 | 910 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count | | | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | | 59.6 | s |

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

## 5.3.15 Communications interfaces

### I²C interface characteristics

Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under the ambient temperature, $f_{PCLK1}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

The STM32F103xx performance line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

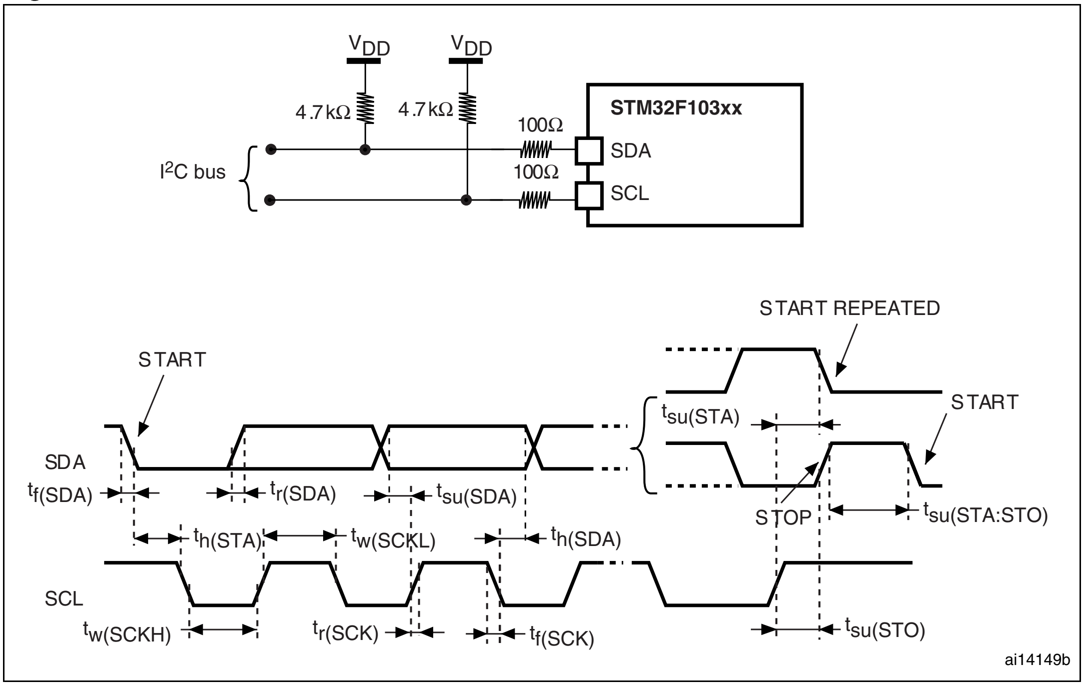
The I²C characteristics are described in *Table 39*. Refer also to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

**Table 39. I²C characteristics**

| Symbol | Parameter | Standard mode I²C(1) | | Fast mode I²C(1)(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0(3) | | 0(4) | 900(3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | $20 + 0.1C_b$ | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | | 300 | | 300 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | µs |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | | 0.6 | | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | µs |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | | 1.3 | | µs |
| $C_b$ | Capacitive load for each bus line | | 400 | | 400 | pF |

1. Guaranteed by design, not tested in production.
2. $f_{PCLK1}$ must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 4 MHz to achieve the maximum fast mode I²C frequency.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

**Figure 24. I²C bus AC waveforms and measurement circuit**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Table 40. SCL frequency ($f_{PCLK1}$= 36 MHz.,$V_{DD}$ = 3.3 V)(1)(2)**

| $f_{SCL}$ (kHz) | I2C_CCR value |
|---|---|
| | $R_P$ = 4.7 kΩ |
| 400 | 0x801E |
| 300 | 0x8028 |
| 200 | 0x803C |
| 100 | 0x00B4 |
| 50 | 0x0168 |
| 20 | 0x0384 |

1. $R_P$ = External pull-up resistance, $f_{SCL}$ = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

## SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 41. SPI characteristics[1]**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | | 18 | MHz |
| | | Slave mode | | 18 | |
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | | 8 | ns |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$[2] | NSS setup time | Slave mode | $4t_{PCLK}$ | | ns |
| $t_{h(NSS)}$[2] | NSS hold time | Slave mode | $2t_{PCLK}$ | | |
| $t_{w(SCKH)}$[2] $t_{w(SCKL)}$[2] | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 50 | 60 | |
| $t_{su(MI)}$[2] $t_{su(SI)}$[2] | Data input setup time | Master mode | 5 | | |
| | | Slave mode | 5 | | |
| $t_{h(MI)}$[2] | Data input hold time | Master mode | 5 | | |
| $t_{h(SI)}$[2] | | Slave mode | 4 | | |
| $t_{a(SO)}$[2][3] | Data output access time | Slave mode, $f_{PCLK}$ = 20 MHz | 0 | $3t_{PCLK}$ | |
| $t_{dis(SO)}$[2][4] | Data output disable time | Slave mode | 2 | 10 | |
| $t_{v(SO)}$[2][1] | Data output valid time | Slave mode (after enable edge) | | 25 | |
| $t_{v(MO)}$[2][1] | Data output valid time | Master mode (after enable edge) | | 5 | |
| $t_{h(SO)}$[2] | Data output hold time | Slave mode (after enable edge) | 15 | | |
| $t_{h(MO)}$[2] | | Master mode (after enable edge) | 2 | | |

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

**Figure 25. SPI timing diagram - slave mode and CPHA = 0**

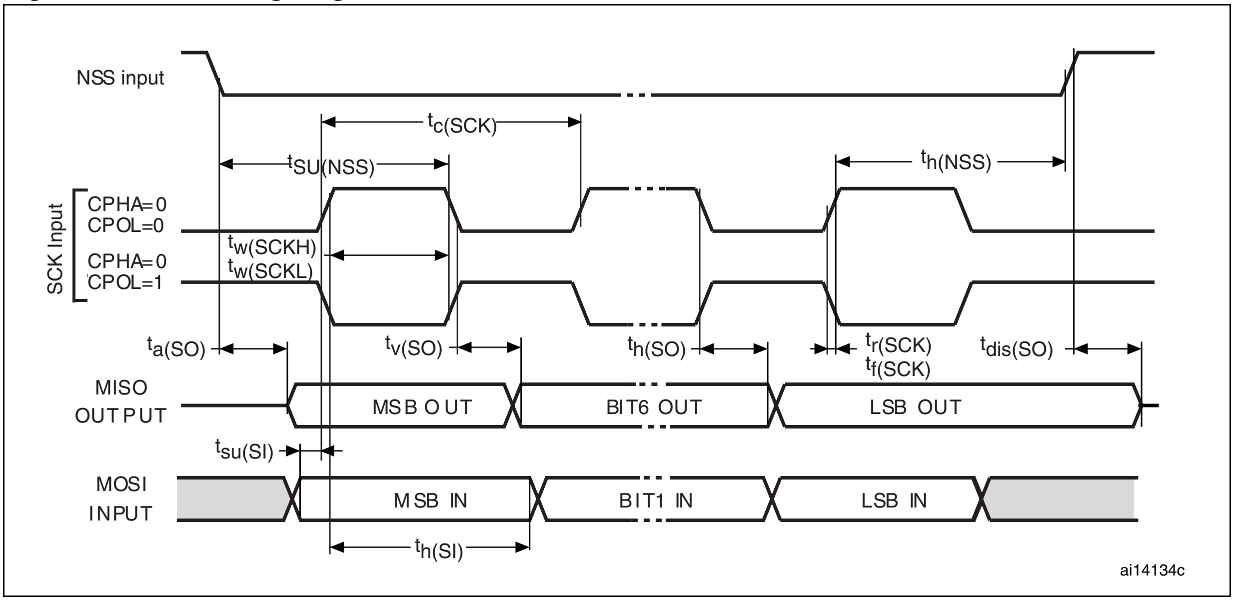
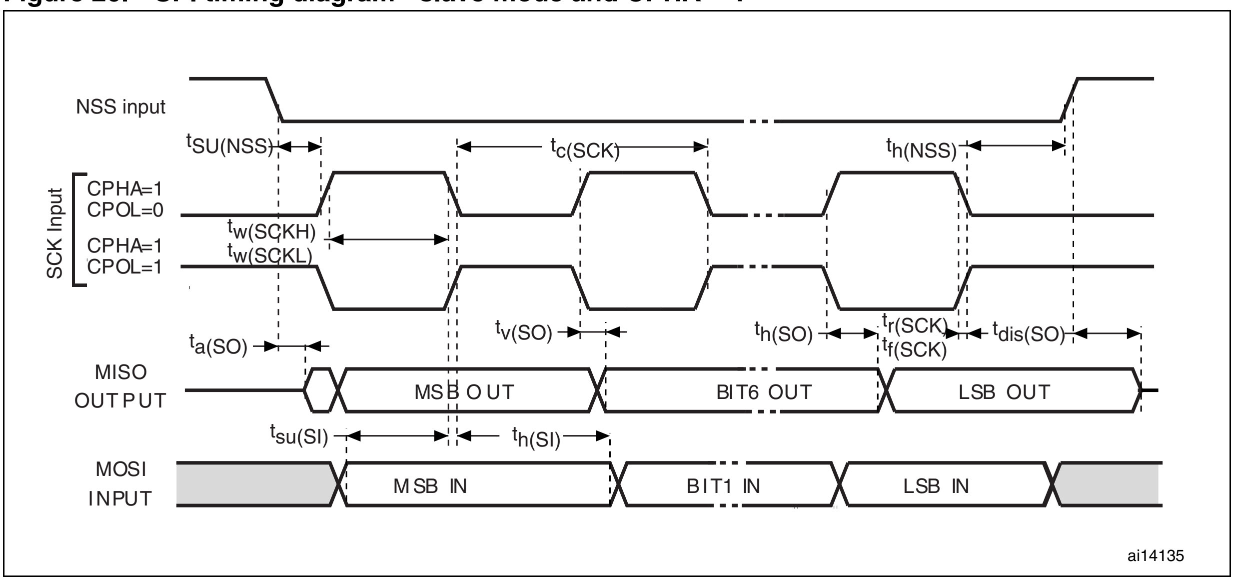
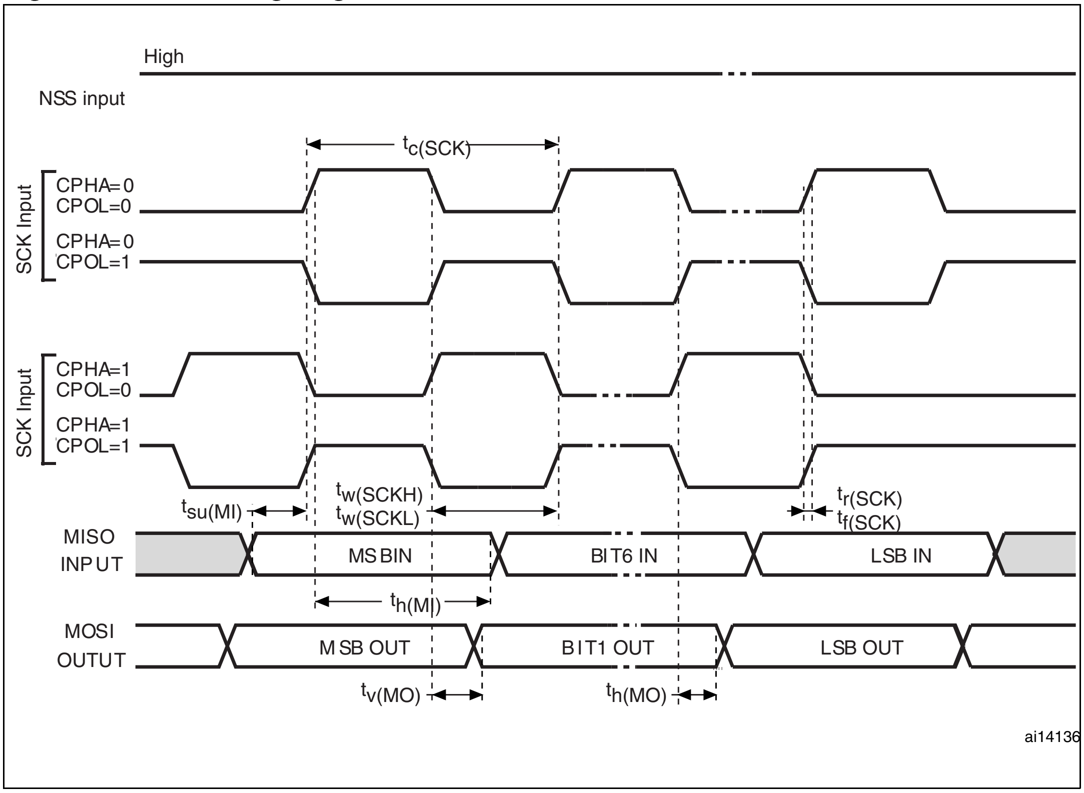



**Figure 26. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 27. SPI timing diagram - master mode(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

## USB characteristics

The USB interface is USB-IF certified (Full Speed).

**Table 42. USB startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USB transceiver startup time | 1 | µs |

1. Guaranteed by design, not tested in production.

Table 43. USB DC electrical characteristics

| Symbol | Parameter | Conditions | Min.[1] | Max.[1] | Unit |
|---|---|---|---|---|---|
| **Input levels** | | | | | |
| $V_{DD}$ | USB operating voltage[2] | | 3.0[3] | 3.6 | V |
| $V_{DI}$[4] | Differential input sensitivity | I(USBDP, USBDM) | 0.2 | | V |
| $V_{CM}$[4] | Differential common mode range | Includes $V_{DI}$ range | 0.8 | 2.5 | |
| $V_{SE}$[4] | Single ended receiver threshold | | 1.3 | 2.0 | |
| **Output levels** | | | | | |
| $V_{OL}$ | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V[5] | | 0.3 | V |
| $V_{OH}$ | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$[5] | 2.8 | 3.6 | |

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F103xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V $V_{DD}$ voltage range.
4. Guaranteed by design, not tested in production.
5. $R_L$ is the load connected on the USB drivers

Figure 28. USB timings: definition of data signal rise and fall time

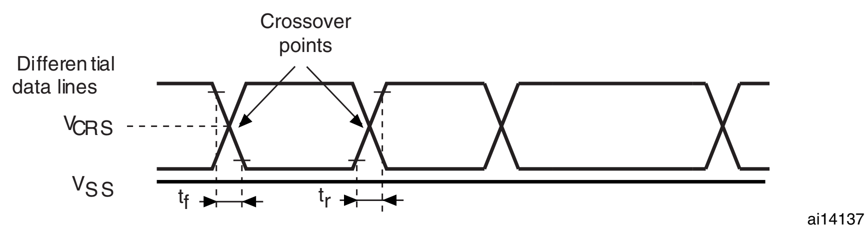



Table 44. USB: Full-speed electrical characteristics[1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **Driver characteristics** | | | | | |
| $t_r$ | Rise time[2] | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall time[2] | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | | 1.3 | 2.0 | V |

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

### 5.3.16 CAN (controller area network) interface

Refer to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

### 5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 9*.

*Note: It is recommended to perform a calibration after each power-up.*

**Table 45. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | | 2.4 | | 3.6 | V |
| $V_{REF+}$(3) | Positive reference voltage | | 2.4 | | $V_{DDA}$ | V |
| $I_{VREF}$(3) | Current on the $V_{REF}$ input pin | | | 160(1) | 220(1) | µA |
| $f_{ADC}$ | ADC clock frequency | | 0.6 | | 14 | MHz |
| $f_S$(2) | Sampling rate | | 0.05 | | 1 | MHz |
| $f_{TRIG}$(2) | External trigger frequency | $f_{ADC}$ = 14 MHz | | | 823 | kHz |
| | | | | | 17 | $1/f_{ADC}$ |
| $V_{AIN}$(3) | Conversion voltage range | | 0 ($V_{SSA}$ tied to ground) | | $V_{REF+}$ | V |
| $R_{AIN}$(2) | External input impedance | See *Equation 1* and *Table 46* for details | | | 50 | kΩ |
| $R_{ADC}$(2) | Sampling switch resistance | | | | 1 | kΩ |
| $C_{ADC}$(2) | Internal sample and hold capacitor | | | | 8 | pF |
| $t_{CAL}$(2) | Calibration time | $f_{ADC}$ = 14 MHz | 5.9 | | | µs |
| | | | 83 | | | $1/f_{ADC}$ |
| $t_{lat}$(2) | Injection trigger conversion latency | $f_{ADC}$ = 14 MHz | | | 0.214 | µs |
| | | | | | 3(4) | $1/f_{ADC}$ |
| $t_{latr}$(2) | Regular trigger conversion latency | $f_{ADC}$ = 14 MHz | | | 0.143 | µs |
| | | | | | 2(4) | $1/f_{ADC}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$ = 14 MHz | 0.107 | | 17.1 | µs |
| | | | 1.5 | | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Power-up time | | 0 | 0 | 1 | µs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 14 MHz | 1 | | 18 | µs |
| | | | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. In devices delivered in VFQFPN and LQFP packages, $V_{REF+}$ is internally connected to $V_{DDA}$ and $V_{REF-}$ is internally connected to $V_{SSA}$. Devices that come in the TFBGA64 package have a $V_{REF+}$ pin but no $V_{REF-}$ pin ($V_{REF-}$ is internally connected to $V_{SSA}$), see *Table 5* and *Figure 4*.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 45*.

**Equation 1: $R_{AIN}$ max formula:**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 46. $R_{AIN}$ max for $f_{ADC}$ = 14 MHz(1)**

| $T_s$ (cycles) | $t_S$ (µs) | $R_{AIN}$ max (kΩ) |
|---|---|---|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |
| 28.5 | 2.04 | 25.2 |
| 41.5 | 2.96 | 37.2 |
| 55.5 | 3.96 | 50 |
| 71.5 | 5.11 | NA |
| 239.5 | 17.1 | NA |

1. Based on characterization, not tested in production.

**Table 47. ADC accuracy - limited test conditions(1) (2)**

| Symbol | Parameter | Test conditions | Typ | Max(3) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{PCLK2}$ = 56 MHz, $f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 3 V to 3.6 V $T_A$ = 25 °C Measurements made after ADC calibration | ±1.3 | ±2 | LSB |
| EO | Offset error | | ±1 | ±1.5 | |
| EG | Gain error | | ±0.5 | ±1.5 | |
| ED | Differential linearity error | | ±0.7 | ±1 | |
| EL | Integral linearity error | | ±0.8 | ±1.5 | |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

Table 48. ADC accuracy(1) (2) (3)

| Symbol | Parameter | Test conditions | Typ | Max(4) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{PCLK2}$ = 56 MHz, $f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 2.4 V to 3.6 V Measurements made after ADC calibration | ±2 | ±5 | LSB |
| EO | Offset error | | ±1.5 | ±2.5 | |
| EG | Gain error | | ±1.5 | ±3 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±1.5 | ±3 | |

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted $V_{DD}$, frequency and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
4. Based on characterization, not tested in production.

Figure 29. ADC accuracy characteristics

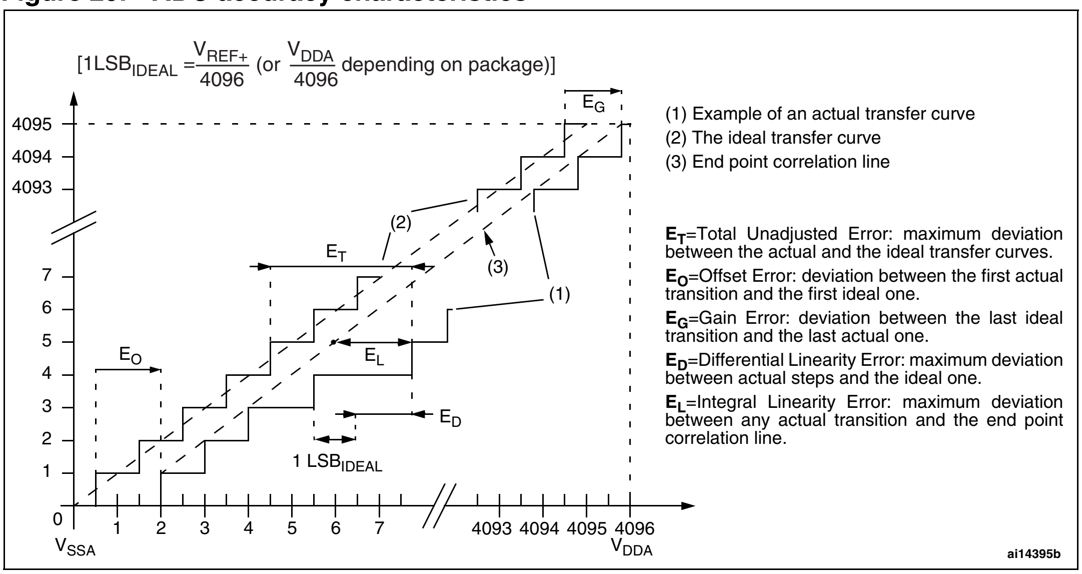
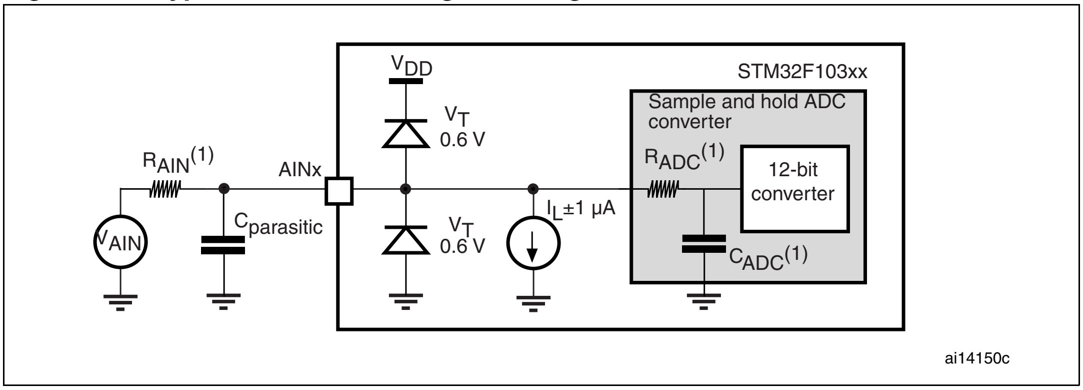


**Figure 30. Typical connection diagram using the ADC**

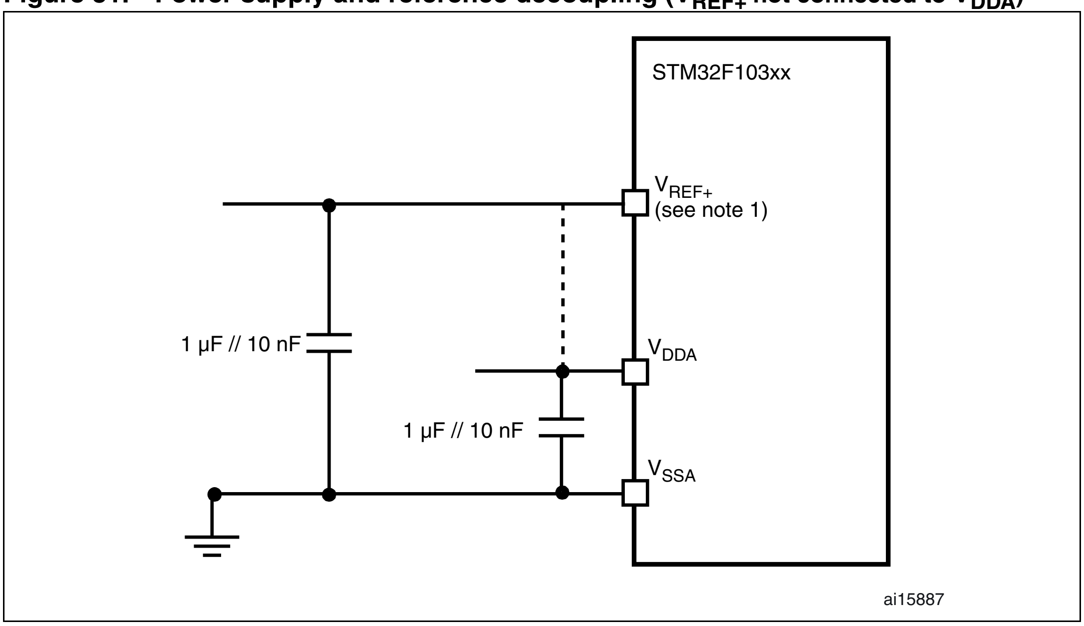



1. Refer to *Table 45* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## General PCB design guidelines

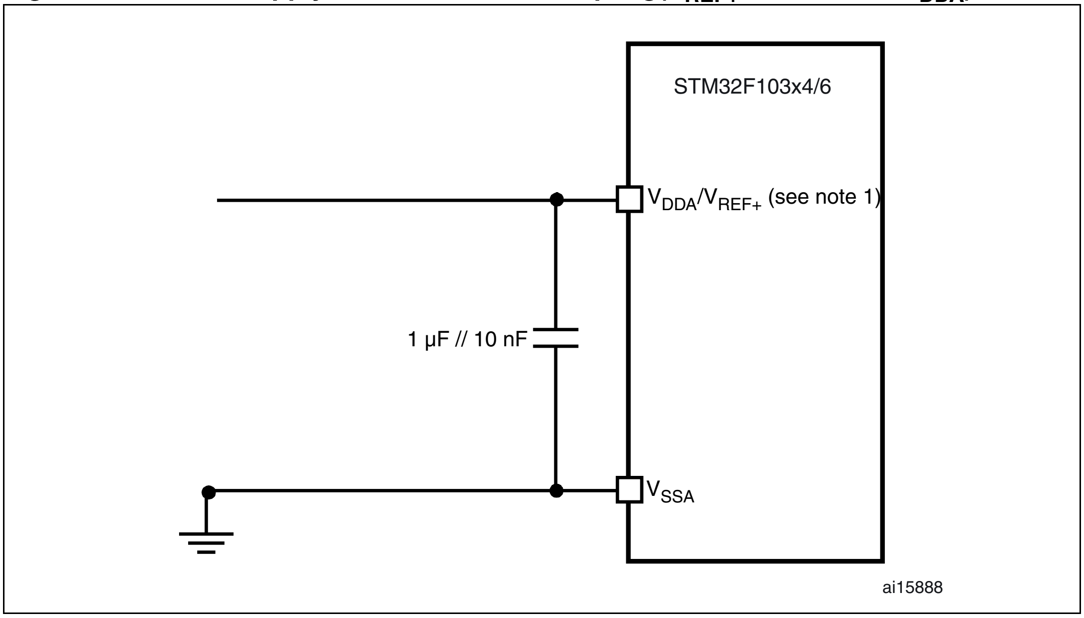
Power supply decoupling should be performed as shown in *Figure 31* or *Figure 32*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 31. Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)**




1. The $V_{REF+}$ input is available only on the TFBGA64 package.

**Figure 32. Power supply and reference decoupling($V_{REF+}$ connected to $V_{DDA}$)**




1. The $V_{REF+}$ input is available only on the TFBGA64 package.

### 5.3.18 Temperature sensor characteristics

**Table 49. TS characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$ (1) | $V_{SENSE}$ linearity with temperature | | ±1 | ±2 | °C |
| Avg_Slope(1) | Average slope | 4.0 | 4.3 | 4.6 | mV/°C |
| $V_{25}$ (1) | Voltage at 25 °C | 1.34 | 1.43 | 1.52 | V |
| $t_{START}$ (2) | Startup time | 4 | | 10 | µs |
| $T_{S\_temp}$ (3)(2) | ADC sampling time when reading the temperature | | | 17.1 | µs |

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

# 6 Package characteristics

## 6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Figure 33. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package outline(1)**

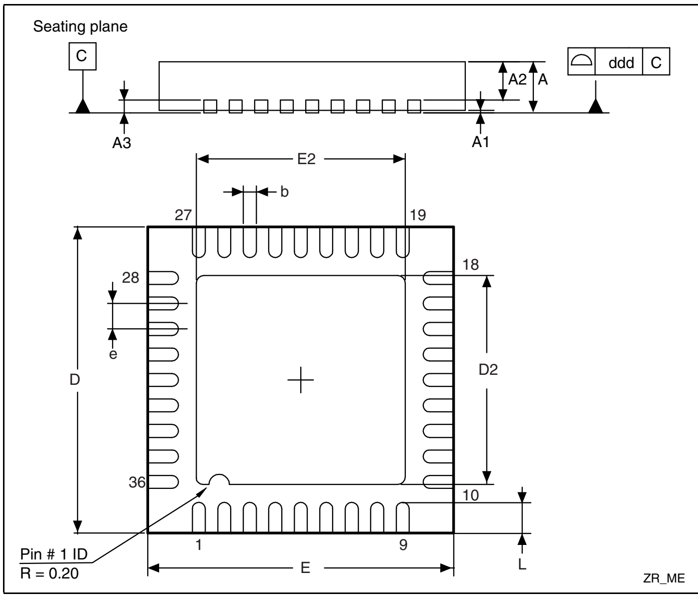
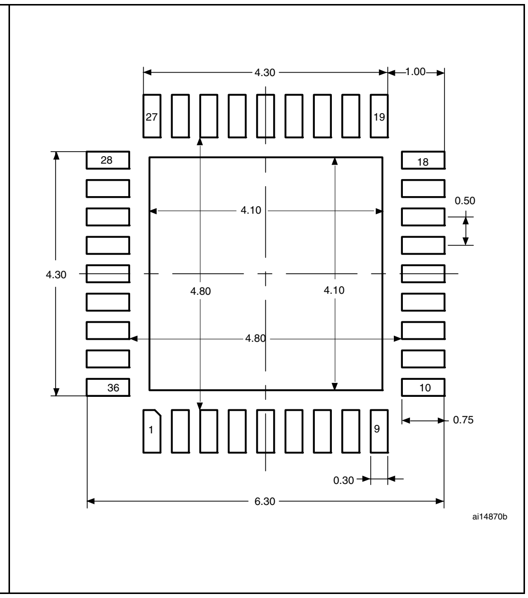



**Figure 34. Recommended footprint (dimensions in mm)(1)(2)(3)**




1. Drawing is not to scale.
2. The back-side pad is not internally connected to the $V_{SS}$ or $V_{DD}$ power pads.
3. There is an exposed die pad on the underside of the VFQFPN package. It should be soldered to the PCB. All leads should also be soldered to the PCB. It is recommended to connect it to $V_{SS}$.

**Table 50. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.800 | 0.900 | 1.000 | 0.0315 | 0.0354 | 0.0394 |
| A1 | | 0.020 | 0.050 | | 0.0008 | 0.0020 |
| A2 | | 0.650 | 1.000 | | 0.0256 | 0.0394 |
| A3 | | 0.250 | | | 0.0098 | |
| b | 0.180 | 0.230 | 0.300 | 0.0071 | 0.0091 | 0.0118 |
| D | 5.875 | 6.000 | 6.125 | 0.2313 | 0.2362 | 0.2411 |
| D2 | 1.750 | 3.700 | 4.250 | 0.0689 | 0.1457 | 0.1673 |
| E | 5.875 | 6.000 | 6.125 | 0.2313 | 0.2362 | 0.2411 |
| E2 | 1.750 | 3.700 | 4.250 | 0.0689 | 0.1457 | 0.1673 |
| e | 0.450 | 0.500 | 0.550 | 0.0177 | 0.0197 | 0.0217 |
| L | 0.350 | 0.550 | 0.750 | 0.0138 | 0.0217 | 0.0295 |
| ddd | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

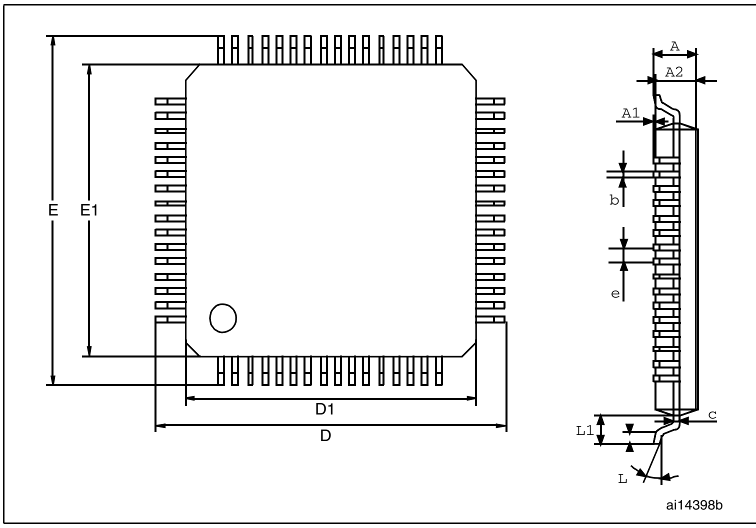



Figure 35. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline[1]

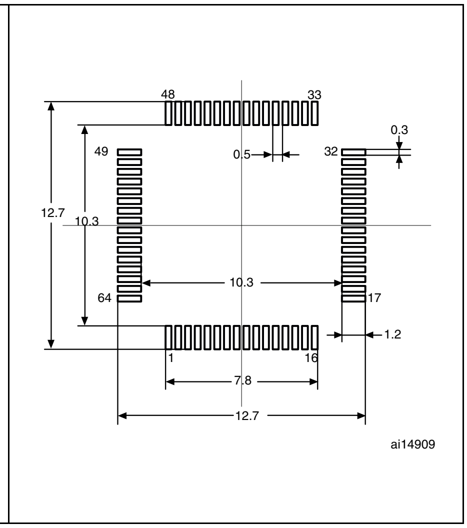



Figure 36. Recommended footprint[1][2]

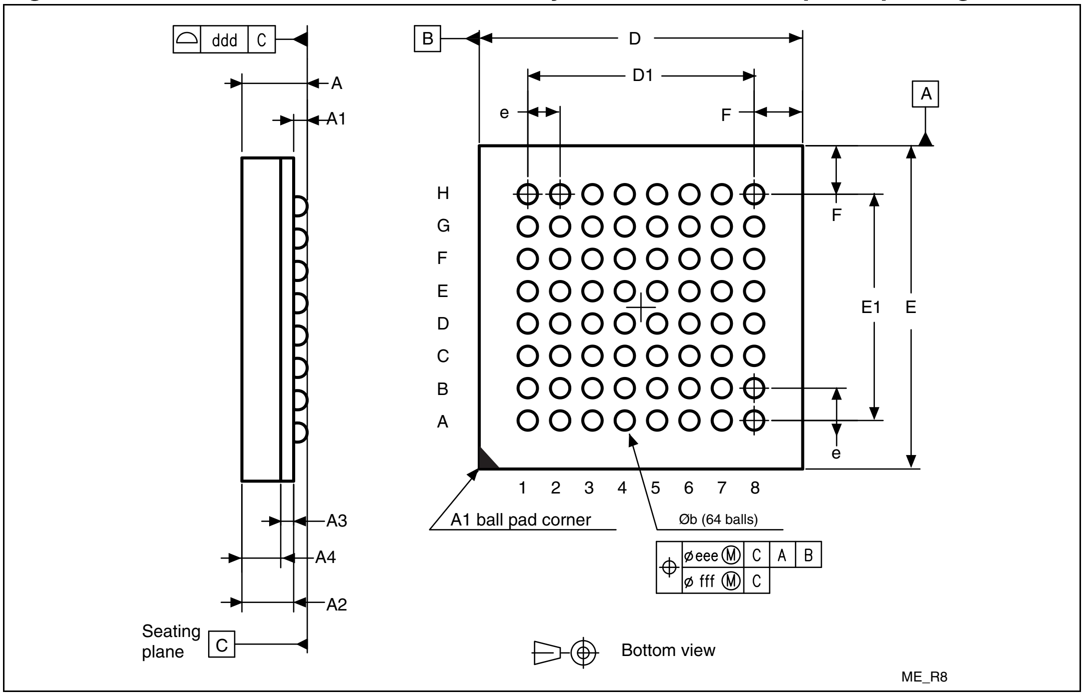
1. Drawing is not to scale.
2. Dimensions are in millimeters.

### Table 51. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.60 | | | 0.0630 |
| A1 | 0.05 | | 0.15 | 0.0020 | | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.0079 |
| D | | 12.00 | | | 0.4724 | |
| D1 | | 10.00 | | | 0.3937 | |
| E | | 12.00 | | | 0.4724 | |
| E1 | | 10.00 | | | 0.3937 | |
| e | | 0.50 | | | 0.0197 | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.00 | | | 0.0394 | |
| N | Number of pins | | | | | |
| | 64 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 37. TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package outline**



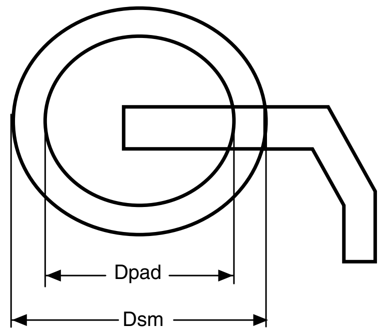

1. Drawing is not to scale.

**Table 52. TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.200 | | | 0.0472 |
| A1 | 0.150 | | | 0.0059 | | |
| A2 | | 0.785 | | | 0.0309 | |
| A3 | | 0.200 | | | 0.0079 | |
| A4 | | | 0.600 | | | 0.0236 |
| b | 0.250 | 0.300 | 0.350 | 0.0098 | 0.0118 | 0.0138 |
| D | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| D1 | | 3.500 | | | 0.1378 | |
| E | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| E1 | | 3.500 | | | 0.1378 | |
| e | | 0.500 | | | 0.0197 | |
| F | | 0.750 | | | 0.0295 | |
| ddd | | 0.080 | | | 0.0031 | |
| eee | | 0.150 | | | 0.0059 | |
| fff | | 0.050 | | | 0.0020 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

### Figure 38. Recommended PCB design rules for pads (0.5 mm pitch BGA)




| | |
|---|---|
| Pitch | 0.5 mm |
| D pad | 0.27 mm |
| Dsm | 0.35 mm typ (depends on the soldermask registration tolerance) |
| Solder paste | 0.27 mm aperture diameter |

ai15495

1. Non solder mask defined (NSMD) pads are recommended
2. 4 to 6 mils solder paste screen printing process

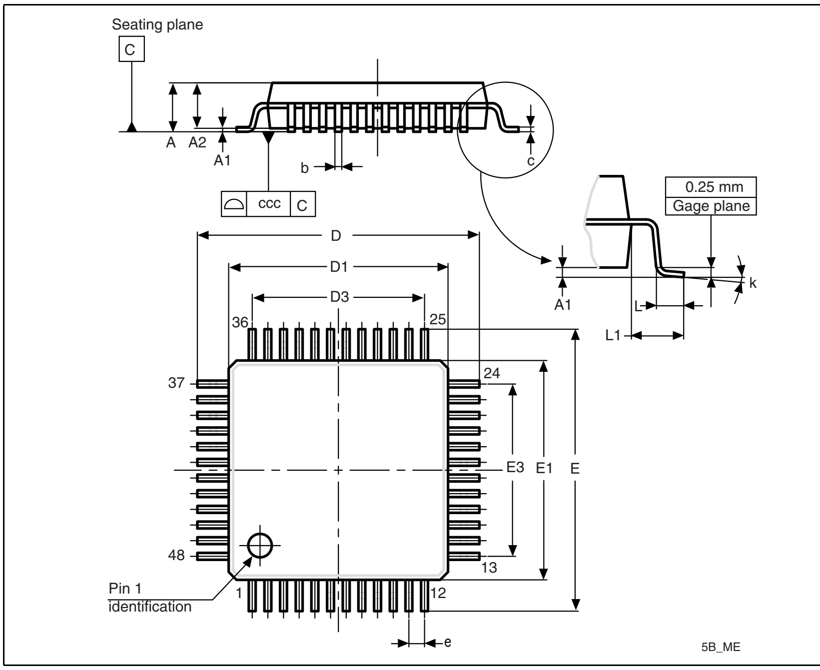



Figure 39. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package outline(1)

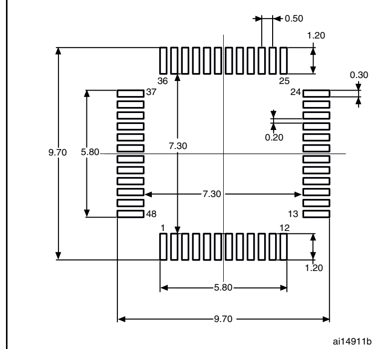



Figure 40. Recommended footprint(1)(2)

1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 53. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.600 | | | 0.0630 |
| A1 | 0.050 | | 0.150 | 0.0020 | | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | | 0.200 | 0.0035 | | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | | 5.500 | | | 0.2165 | |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | | 5.500 | | | 0.2165 | |
| e | | 0.500 | | | 0.0197 | |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.000 | | | 0.0394 | |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 6.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 9: General operating conditions on page 30*.

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J \max = T_A \max + (P_D \max \times \Theta_{JA})$$

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O} \max = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$,

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 54. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient**<br>TFBGA64 - 5 × 5 mm / 0.5 mm pitch | 65 | °C/W |
| | **Thermal resistance junction-ambient**<br>LQFP64 - 10 × 10 mm / 0.5 mm pitch | 45 | |
| | **Thermal resistance junction-ambient**<br>LQFP48 - 7 × 7 mm / 0.5 mm pitch | 55 | |
| | **Thermal resistance junction-ambient**<br>VFQFPN 36 - 6 × 6 mm / 0.5 mm pitch | 18 | |

### 6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

### 6.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 55: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

#### Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V and maximum 8 I/Os used at the same time in output at low level with $I_{OL}$ = 20 mA, $V_{OL}$= 1.3 V

$P_{INTmax}$ = 50 mA × 3.5 V= 175 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: $P_{INTmax}$ = 175 mW and $P_{IOmax}$ = 272 mW:

$P_{Dmax}$ = 175 + 272 = 447 mW

Thus: $P_{Dmax}$ = 447 mW

Using the values obtained in *Table 54* $T_{Jmax}$ is calculated as follows:

– For LQFP64, 45 °C/W

$T_{Jmax}$ = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts (–40 < $T_J$ < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 55: Ordering information scheme*).

#### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature $T_J$ remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 115 °C (measured according to JESD51-2), $I_{DDmax}$ = 20 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V

$P_{INTmax}$ = 20 mA × 3.5 V= 70 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V = 64 mW

This gives: $P_{INTmax}$ = 70 mW and $P_{IOmax}$ = 64 mW:

$P_{Dmax}$ = 70 + 64 = 134 mW

Thus: $P_{Dmax}$ = 134 mW

Using the values obtained in *Table 54* $T_{Jmax}$ is calculated as follows:

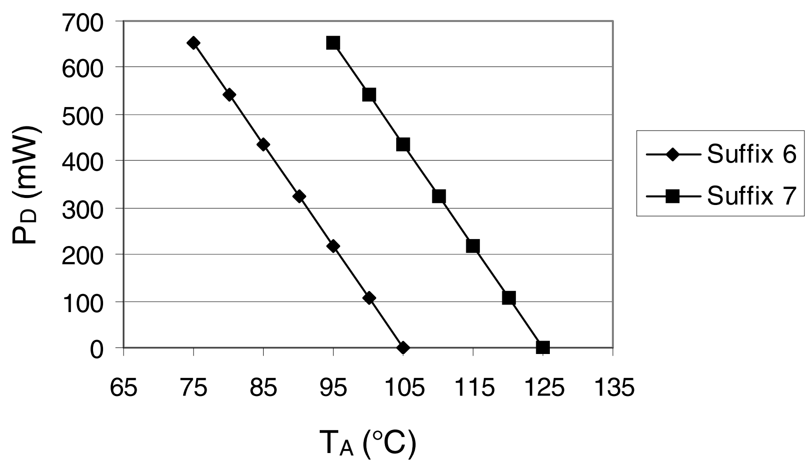
– For LQFP64, 45 °C/W

$T_{Jmax}$ = 115 °C + (45 °C/W × 134 mW) = 115 °C + 6.03 °C = 121.03 °C

This is within the range of the suffix 7 version parts (–40 < $T_J$ < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 55: Ordering information scheme*).

**Figure 41. LQFP64 $P_D$ max vs. $T_A$**



# 7 Ordering information scheme

**Table 55. Ordering information scheme**

Example: STM32 F 103 C 4 T 7 A xxx

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

F = general-purpose

**Device subfamily**

103 = performance line

**Pin count**

T = 36 pins
C = 48 pins
R = 64 pins

**Flash memory size**

4 = 16 Kbytes of Flash memory
6 = 32 Kbytes of Flash memory

**Package**

H = BGA
T = LQFP
U = VFQFPN

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

**Internal code**

“A” or blank[1]

**Options**

xxx = programmed parts
TR = tape and real

1. For STM32F103x6 devices with a **blank** Internal code, please refer to the STM32F103x8/B datasheet available from the ST website: www.st.com.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

# 8 Revision history

Table 56. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 22-Sep-2008 | 1 | Initial release. |
| 30-Mar-2009 | 2 | "96-bit unique ID" feature added and I/O information clarified *on page 1*.<br>Timers specified *on page 1* (Motor control capability mentioned).<br>*Table 4: Timer feature comparison* added.<br>PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column, plus small additional changes in *Table 5: Low-density STM32F103xx pin definitions*.<br>*Figure 7: Memory map* modified.<br>References to $V_{REF-}$ removed:<br>– *Figure 1: STM32F103xx performance line block diagram* modified,<br>– *Figure 10: Power supply scheme* modified<br>– *Figure 29: ADC accuracy characteristics* modified<br>– Note modified in *Table 48: ADC accuracy*.<br>*Table 20: High-speed external user clock characteristics* and *Table 21: Low-speed external user clock characteristics* modified.<br>Note modified in *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*.<br>*Figure 16* shows a typical curve (title modified). $ACC_{HSI}$ max values modified in *Table 24: HSI oscillator characteristics*.<br>TFBGA64 package added (see *Table 52* and *Table 37*).<br>Small text changes. |

**Table 56. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 24-Sep-2009 | 3 | *Note 5* updated and *Note 4* added in *Table 5: Low-density STM32F103xx pin definitions*.<br>$V_{RERINT}$ and $T_{Coeff}$ added to *Table 12: Embedded internal reference voltage*. Typical $I_{DD\_VBAT}$ value added in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 14: Typical current consumption on VBAT with RTC on versus temperature at different VBAT values* added.<br>$f_{HSE\_ext}$ min modified in *Table 20: High-speed external user clock characteristics*.<br>$C_{L1}$ and $C_{L2}$ replaced by C in *Table 22: HSE 4-16 MHz oscillator characteristics* and *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Table 24: HSI oscillator characteristics* modified. Conditions removed from *Table 26: Low-power mode wakeup timings*.<br>*Note 1* modified below *Figure 20: Typical application with an 8 MHz crystal*.<br>*Figure 23: Recommended NRST pin protection* modified.<br>Jitter added to *Table 27: PLL characteristics on page 48*.<br>IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.10: EMC characteristics on page 49*.<br>$C_{ADC}$ and $R_{AIN}$ parameters modified in *Table 45: ADC characteristics*. $R_{AIN}$ max values modified in *Table 46: RAIN max for fADC = 14 MHz*.<br>Small text changes. |

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