

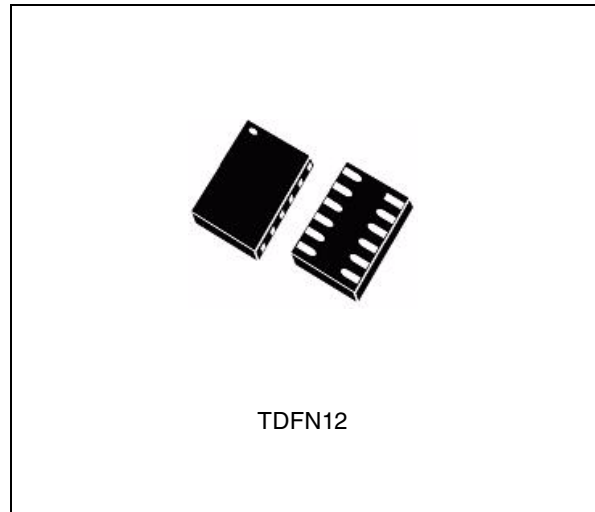


# STM6600 STM6601

## Smart push-button on/off controller with Smart Reset™ and power-on lockout

### Features

- Operating voltage 1.6 V to 5.5 V
- Low standby current of 1  $\mu$ A
- Adjustable Smart Reset™ assertion delay time driven by external  $C_{SRD}$
- Power-up duration determined primarily by push-button press (STM6600) or by fixed time period,  $t_{ON\_BLANK}$  (STM6601)
- Debounced  $\overline{PB}$  and  $\overline{SR}$  inputs
- $\overline{PB}$  and  $\overline{SR}$  ESD inputs withstand voltage up to  $\pm 15$  kV (air discharge)  $\pm 8$  kV (contact discharge)
- Active high or active low enable output option ( $\overline{EN}$  or  $EN$ ) provides control of MOSFET, DC-DC converter, regulator, etc.
- Secure startup, interrupt, Smart Reset™ or power down driven by push-button
- Precise 1.5 V voltage reference with 1% accuracy
- Industrial operating temperature  $-40$  to  $+85$  °C
- Available in TDFN12 2 x 3 mm package



### Applications

- Portable devices
- Terminals
- Audio and video players
- Cell phones and smart phones
- PDAs, palmtops, organizers

**Table 1. Device summary**

Device	$\overline{RST}$	$C_{SRD}$	$\overline{PB} / \overline{SR}$	$EN$ or $\overline{EN}$	$\overline{INT}$	Startup process
STM6600	open drain <sup>(1)</sup>	✓	✓	push-pull	open drain <sup>(1)</sup>	$\overline{PB}$ must be held low until the $PS_{HOLD}$ <sup>(2)</sup> confirmation
STM6601	open drain <sup>(1)</sup>	✓	✓	push-pull	open drain <sup>(1)</sup>	PB can be released before the $PS_{HOLD}$ <sup>(2)</sup> confirmation

1. External pull-up resistor needs to be connected to open drain outputs.

2. For a successful startup, the  $PS_{HOLD}$  (Power Supply Hold) needs to be pulled high within specific time,  $t_{ON\_BLANK}$ .

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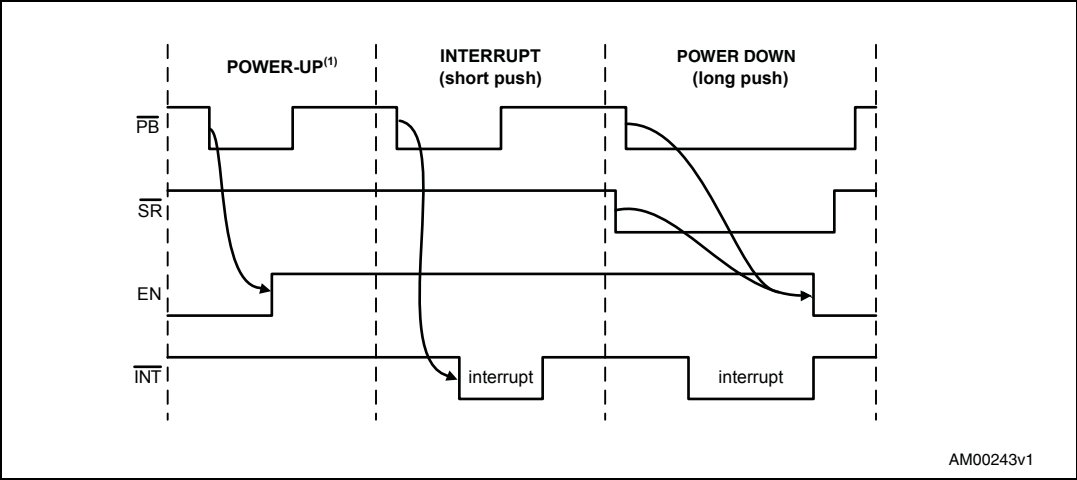
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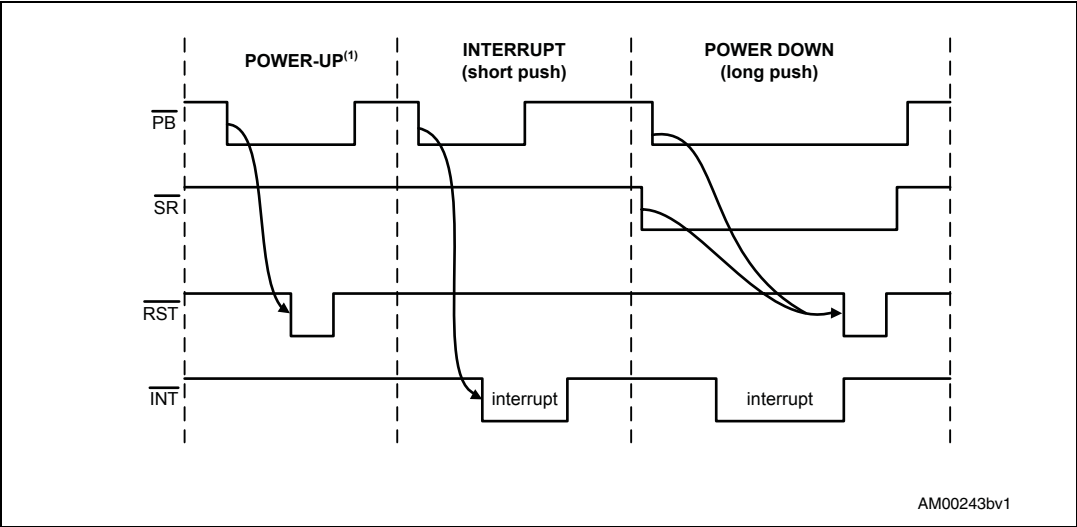


Figure 2. Basic functionality (option with enable deassertion after long push)



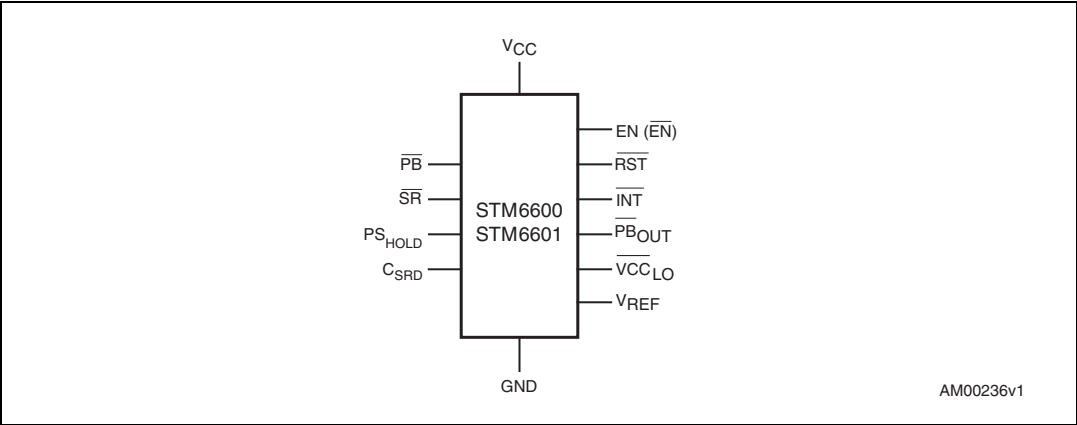
1. For power-up the battery voltage has to be above  $V_{TH+}$  threshold.

Figure 3. Basic functionality (option with  $\overline{RST}$  assertion after long push)



1. For power-up the battery voltage has to be above  $V_{TH+}$  threshold.

Figure 4. Logic diagram



**Table 2. Pin descriptions**

Pin number	Symbol	Function
1	$V_{CC}$	Power supply input
2	$\overline{SR}$	Smart Reset™ button input
3	$V_{REF}$	Precise 1.5 V voltage reference
4	$PS_{HOLD}$	$PS_{HOLD}$ input
5	$C_{SRD}$	Adjustable Smart Reset™ delay time input
6	$\overline{PB}$	Push-button input
7	$\overline{VCC}_{LO}$	Output for high threshold comparator output ( $V_{TH+}$ )
8	$\overline{PB}_{OUT}$	Status of $\overline{PB}$ push-button input
9	EN or $\overline{EN}$	Enable output
10	$\overline{RST}$	Reset output
11	$\overline{INT}$	Interrupt output
12	GND	Ground

**Figure 5. TDFN12 pin connections**

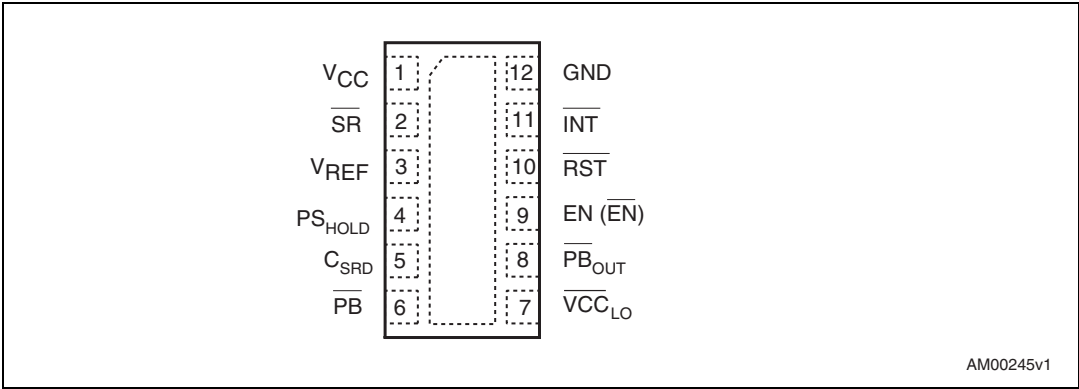
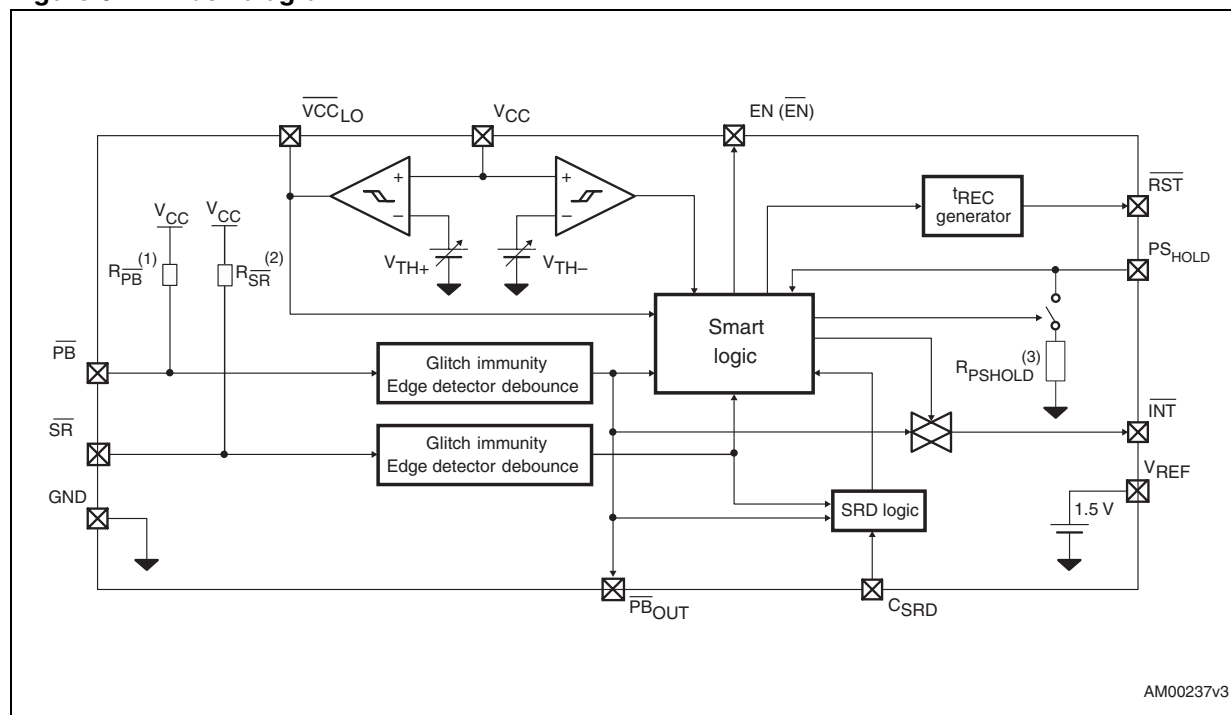


Figure 6. Block diagram



1. Internal pull-up resistor connected to  $\overline{PB}$  input (see [Table 5](#) for precise specifications).
2. Optional internal pull-up resistor connected to  $\overline{SR}$  input (see [Table 5](#) for precise specifications and [Table 10](#) for detailed device options).
3. Internal pull-down resistor is connected to  $PS_{HOLD}$  input only during startup (see [Figure 7](#), [8](#), [9](#), [10](#), [11](#), [12](#), [13](#), and [18](#)).



## 2 Pin descriptions

### **V<sub>CC</sub> - power supply input**

V<sub>CC</sub> is monitored during startup and normal operation for sufficient voltage level. Decouple the V<sub>CC</sub> pin from ground by placing a 0.1 µF capacitor as close to the device as possible.

### **$\overline{\text{SR}}$ - Smart Reset™ button input**

This input is equipped with voltage detector with a factory-trimmed threshold and has ±8 kV HBM ESD protection.

Both  $\overline{\text{PB}}$  and  $\overline{\text{SR}}$  buttons have to be pressed and held for t<sub>SRD</sub> period so the long push is recognized and the reset is asserted (or the enable output is deasserted depending on the option) - see [Figure 15](#), [16](#), and [17](#).

Active low  $\overline{\text{SR}}$  input is usually connected to GND through the momentary push-button (see [Figure 1](#)) and it has an optional 100 kΩ pull-up resistor. It is also possible to drive this input using an external device with either open drain (recommended) or push-pull output. Open drain output can be connected in parallel with push-button or other open drain outputs, which is not possible with push-pull output.

### **V<sub>REF</sub> - external precise 1.5 V voltage reference**

This 1.5 V voltage reference is specified with very tight accuracy of 1% (see [Table 5](#)). It has proper output voltage as soon as the reset output is deasserted (i.e. after t<sub>REC</sub> expires) and it is disabled when the device enters standby mode. A mandatory capacitor needs to be connected to V<sub>REF</sub> output (even if V<sub>REF</sub> is not used). Capacitor value of 1 µF is recommended.

### **PS<sub>HOLD</sub> input**

This input is equipped with a voltage detector with a factory-trimmed threshold. It is used to confirm correct power-up of the device (if EN or  $\overline{\text{EN}}$  is not asserted) or to initiate a shutdown (if EN or  $\overline{\text{EN}}$  is asserted).

Forcing PS<sub>HOLD</sub> high during power-up confirms the proper start of the application and keeps enable output asserted. Because most processors have outputs in high-Z state before initialization, an internal pull-down resistor is connected to PS<sub>HOLD</sub> input during startup (see [Figure 7](#), [8](#), [9](#), [10](#), [11](#), [12](#), [13](#), and [18](#)).

Forcing the PS<sub>HOLD</sub> signal low during normal operation deasserts the enable output (see [Figure 14](#)). Input voltage on this pin is compared to an accurate voltage reference.

### **C<sub>SRD</sub> - Smart Reset™ delay time input**

A capacitor to ground determines the additional time (t<sub>SRD</sub>) that  $\overline{\text{PB}}$  with  $\overline{\text{SR}}$  must be pressed and held before a long push is recognized. The connected C<sub>SRD</sub> capacitor is charged with I<sub>SRD</sub> current. Additional Smart Reset™ delay time t<sub>SRD</sub> ends when voltage on the C<sub>SRD</sub> capacitor reaches the V<sub>SRD</sub> voltage threshold. It is recommended to use a low ESR capacitor (e.g. ceramic). If the capacitor is not used, leave the C<sub>SRD</sub> pin open. If no capacitor is connected, there is no t<sub>SRD</sub> and a long push is recognized right after t<sub>INT\_Min</sub> expires (see [Figure 18](#) and [19](#)).

**$\overline{\text{PB}}$  - power ON switch**

This input is equipped with a voltage detector with a factory-trimmed threshold and has  $\pm 8$  kV HBM ESD protection.

When the  $\overline{\text{PB}}$  button is pressed and held, the battery voltage is detected and EN (or  $\overline{\text{EN}}$ ) is asserted if the battery voltage is above the threshold  $V_{\text{TH+}}$  during the whole  $t_{\text{DEBOUNCE}}$  period (see [Figure 13](#)).

A short push of the push-button during normal operation can initiate an interrupt through debounced  $\overline{\text{INT}}$  output (see [Figure 14](#)) and a long push of  $\overline{\text{PB}}$  and  $\overline{\text{SR}}$  simultaneously can either assert reset output  $\overline{\text{RST}}$  (see [Figure 18](#)) or deassert the EN or  $\overline{\text{EN}}$  output (see [Figure 19](#)) based on the option used.

*Note: A switch to GND must be connected to this input (e.g. mechanical push-button, open drain output of external circuitry, etc.), see [Figure 1](#). This ensures a proper startup signal on  $\overline{\text{PB}}$  (i.e. a transition from full  $V_{\text{CC}}$  below specified  $V_{\text{IL}}$ ).  $\overline{\text{PB}}$  input has an internal 100 k $\Omega$  pull-up resistor connected.*

 **$\overline{\text{VCC}}_{\text{LO}}$  - high threshold detection output**

During power-up,  $\overline{\text{VCC}}_{\text{LO}}$  is low when  $V_{\text{CC}}$  supply voltage is below the  $V_{\text{TH+}}$  threshold. After successful power-up (i.e. during normal operation)  $\overline{\text{VCC}}_{\text{LO}}$  is low anytime undervoltage is detected (see [Figure 13](#)).

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 k $\Omega$  is sufficient in most applications.

$\overline{\text{VCC}}_{\text{LO}}$  is floating when STM660x is in standby mode.

 **$\overline{\text{PB}}_{\text{OUT}}$  -  $\overline{\text{PB}}$  input state**

If the push-button  $\overline{\text{PB}}$  is pressed, the pin stays low during the  $t_{\text{DEBOUNCE}}$  time period.

If  $\overline{\text{PB}}$  is asserted for the entire  $t_{\text{DEBOUNCE}}$  period,  $\overline{\text{PB}}_{\text{OUT}}$  will then stay low for at least  $t_{\text{INT\_Min}}$ . If  $\overline{\text{PB}}$  is asserted after  $t_{\text{INT\_Min}}$  expires,  $\overline{\text{PB}}_{\text{OUT}}$  will return high as soon as  $\overline{\text{PB}}$  is deasserted (see [Figure 22](#)).  $\overline{\text{PB}}_{\text{OUT}}$  ignores  $\overline{\text{PB}}$  assertion during an undervoltage condition. At startup on the STM6601  $\overline{\text{PB}}_{\text{OUT}}$  will respond only to the first  $\overline{\text{PB}}$  assertion and any other assertion will be ignored until  $t_{\text{ON\_BLANK}}$  expires. This output is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 k $\Omega$  is sufficient in most applications.

**EN or  $\overline{\text{EN}}$  - enable output**

This output is intended to enable system power (see [Figure 1](#)). EN is asserted **high** after a valid turn-on event has been detected and confirmed (i.e. push-button has been pressed and held for  $t_{\text{DEBOUNCE}}$  or more and  $V_{\text{CC}} > V_{\text{TH+}}$  voltage level has been detected - see [Figure 13](#)). EN is released **low** if any of the conditions below occur:

- the push-button is released before  $\text{PS}_{\text{HOLD}}$  is driven high (valid for STM6600, see [Figure 9](#)) or  $t_{\text{ON\_BLANK}}$  expires before  $\text{PS}_{\text{HOLD}}$  is driven high during startup (valid for both STM6600 and STM6601, see [Figure 10](#) and [12](#)).
- $\text{PS}_{\text{HOLD}}$  is driven low during normal operation (see [Figure 14](#)).
- an undervoltage condition is detected for more than  $t_{\text{SRD}} + t_{\text{INT\_Min}} + t_{\text{DEBOUNCE}}$  (see [Figure 21](#)).
- a long push of the buttons is detected (only for the device with option “EN deasserted by long push” - see [Figure 19](#)) or  $\text{PS}_{\text{HOLD}}$  is not driven high during  $t_{\text{ON\_BLANK}}$  after a long push of the buttons (only for the device with option “RST asserted by long push” - see [Figure 18](#)).

Described logic levels are inverted in case of  $\overline{\text{EN}}$  output. Output type is push-pull by default.

 **$\overline{\text{RST}}$  - reset output**

This output pulls low for  $t_{\text{REC}}$ :

- during startup.  $\overline{\text{PB}}$  has been pressed (falling edge on the  $\overline{\text{PB}}$  detected) and held for at least  $t_{\text{DEBOUNCE}}$  and  $V_{\text{CC}} > V_{\text{TH+}}$  (see [Figure 7, 8, 9, 10, 11, 12](#) and [13](#) for more details).
- after long push detection (valid only for the device with option “ $\overline{\text{RST}}$  asserted by long push”).  $\overline{\text{PB}}$  has been pressed (falling edge on the  $\overline{\text{PB}}$  detected) and held for more than  $t_{\text{DEBOUNCE}} + t_{\text{SRD}}$  (additional Smart Reset™ delay time can be adjusted by the external capacitor  $C_{\text{SRD}}$ ) - see [Figure 18](#).

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 k $\Omega$  is sufficient in most applications.

 **$\overline{\text{INT}}$  - interrupt output**

While the system is under normal operation ( $\text{PS}_{\text{HOLD}}$  is driven high, power for application is asserted), the  $\overline{\text{INT}}$  is driven **low** if:

- $V_{\text{CC}}$  falls below  $V_{\text{TH-}}$  threshold (i.e. undervoltage is detected - see [Figure 20](#) and [21](#)).
- the falling edge on the  $\overline{\text{PB}}$  is detected and the push-button is held for  $t_{\text{DEBOUNCE}}$  or more.  $\overline{\text{INT}}$  is driven low after  $t_{\text{DEBOUNCE}}$  and stays low as long as  $\overline{\text{PB}}$  is held. The  $\overline{\text{INT}}$  signal is held high during power-up.

The state of the  $\overline{\text{PB}}_{\text{OUT}}$  output can be used to determine if the interrupt was caused by either the assertion of the  $\overline{\text{PB}}$  input, or was due to the detection of an undervoltage condition on  $V_{\text{CC}}$ .

$\overline{\text{INT}}$  output is asserted low for at least  $t_{\text{INT\_Min}}$ .

Output type is active low and open drain by default. Open drain output type requires a pull-up resistor. A 10 k $\Omega$  is sufficient in most applications.

**GND - ground**

### 3 Operation

The STM6600-STM6601 simplified smart push-button on/off controller with Smart Reset™ and power-on lockout enables and disables power for the application depending on push-button states, signals from the processor, and battery voltage.

#### Power-on

Because most of the processors have outputs in high-Z state before initialization, an internal pull-down resistor is connected to PS<sub>HOLD</sub> input during startup (see [Figure 7, 8, 9, 10, 11, 12, 13](#), and [18](#)).

To power up the device the push-button  $\overline{\text{PB}}$  has to be pressed for at least  $t_{\text{DEBOUNCE}}$  and  $V_{\text{CC}}$  has to be above  $V_{\text{TH+}}$  for the whole  $t_{\text{DEBOUNCE}}$  period. If the battery voltage drops below  $V_{\text{TH+}}$  during the  $t_{\text{DEBOUNCE}}$ , the counter is reset and starts to count again when  $V_{\text{CC}} > V_{\text{TH+}}$  (see [Figure 13](#)). After  $t_{\text{DEBOUNCE}}$  the enable signal is asserted (EN goes high,  $\overline{\text{EN}}$  goes low), reset output  $\overline{\text{RST}}$  is asserted for  $t_{\text{REC}}$  and then the startup routine is performed by the processor. During initialization, the processor sets the PS<sub>HOLD</sub> signal high.

On the STM6600 the PS<sub>HOLD</sub> signal has to be set high prior to push-button release and  $t_{\text{ON\_BLANK}}$  expiration, otherwise the enable signal is deasserted (EN goes low,  $\overline{\text{EN}}$  goes high) - see [Figure 7, 8, 9](#), and [10](#). The time up to push-button release represents the maximum time allowed for the system to power up and initialize the circuits driving the PS<sub>HOLD</sub> input. If the PS<sub>HOLD</sub> signal is low at push-button release, the enable output is deasserted immediately, thus turning off the system power. If  $t_{\text{ON\_BLANK}}$  expires prior to push-button release, the PS<sub>HOLD</sub> state is checked at its expiration. This safety feature disables the power and prevents discharging the battery if the push-button is stuck or it is held for an unreasonable period of time and the application is not responding (see [Figure 8](#) and [10](#)).  $\overline{\text{PB}}$  status,  $\overline{\text{INT}}$  status and  $V_{\text{CC}}$  undervoltage detection are not monitored until power-up is completed.

On the STM6601 the PS<sub>HOLD</sub> signal has to be set high before  $t_{\text{ON\_BLANK}}$  expires, otherwise the enable signal is deasserted - see [Figure 11](#) and [12](#). In this case the  $t_{\text{ON\_BLANK}}$  period is the maximum time allowed for the power switch and processor to perform the proper power-on. If the PS<sub>HOLD</sub> signal is low at the end of the blanking period, the enable output is released immediately, thus turning off the system power.  $\overline{\text{PB}}$  status,  $\overline{\text{INT}}$  status and  $V_{\text{CC}}$  undervoltage detection are not monitored during the entire  $t_{\text{ON\_BLANK}}$  period. This failsafe feature prevents the user from turning on the system when there is a faulty power switch or an unresponsive microprocessor.

#### Push-button interrupt

If the device works under normal operation (i.e. PS<sub>HOLD</sub> is high) and the push-button  $\overline{\text{PB}}$  is pressed for more than  $t_{\text{DEBOUNCE}}$ , a negative pulse with minimum  $t_{\text{INT\_Min}}$  width is generated on the  $\overline{\text{INT}}$  output. By connecting  $\overline{\text{INT}}$  to the processor interrupt input ( $\overline{\text{INT}}$  or NMI) a safeguard routine can be performed and the power can be shut down by setting PS<sub>HOLD</sub> low - see [Figure 14](#).

#### Forced power-down mode

The PS<sub>HOLD</sub> output can be forced low anytime during normal operation by the processor and can deassert the enable signal - see [Figure 14](#).

**Undervoltage detection**

If  $V_{CC}$  voltage drops below  $V_{TH}$  voltage threshold during normal operation, the  $\overline{INT}$  output is driven low (see [Figure 20](#) and [Figure 21](#)).

If an undervoltage condition is detected for  $t_{DEBOUNCE} + t_{\overline{INT\_Min}} + t_{SRD}$ , the enable output is deasserted (see [Figure 21](#)).

**Hardware reset or power-down while system not responding**

If the system is not responding and the system hangs, the  $\overline{PB}$  and  $\overline{SR}$  push-buttons can be pressed simultaneously longer than  $t_{DEBOUNCE} + t_{\overline{INT\_Min}} + t_{SRD}$ , and then

- a) either the reset output  $\overline{RST}$  is asserted for  $t_{REC}$  and the processor is reset (valid only for the device with option “ $\overline{RST}$  asserted by long push”) – see [Figure 18](#)
- b) or the power is disabled by EN or  $\overline{EN}$  signal (valid only for the device with option “EN deasserted by long push”) – see [Figure 19](#)

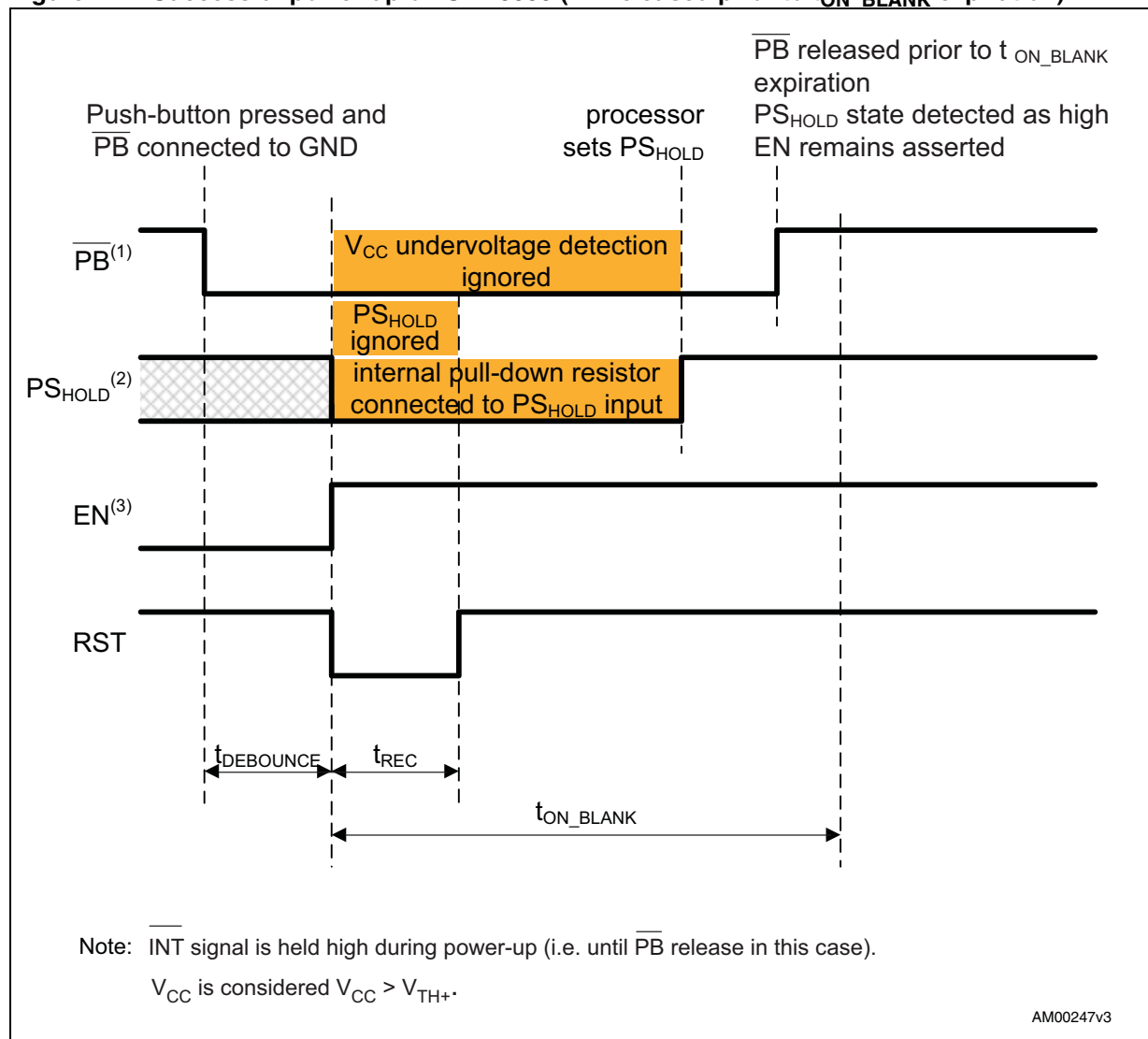
The  $t_{SRD}$  is set by the external capacitor connected to the  $C_{SRD}$  pin.

**Standby**

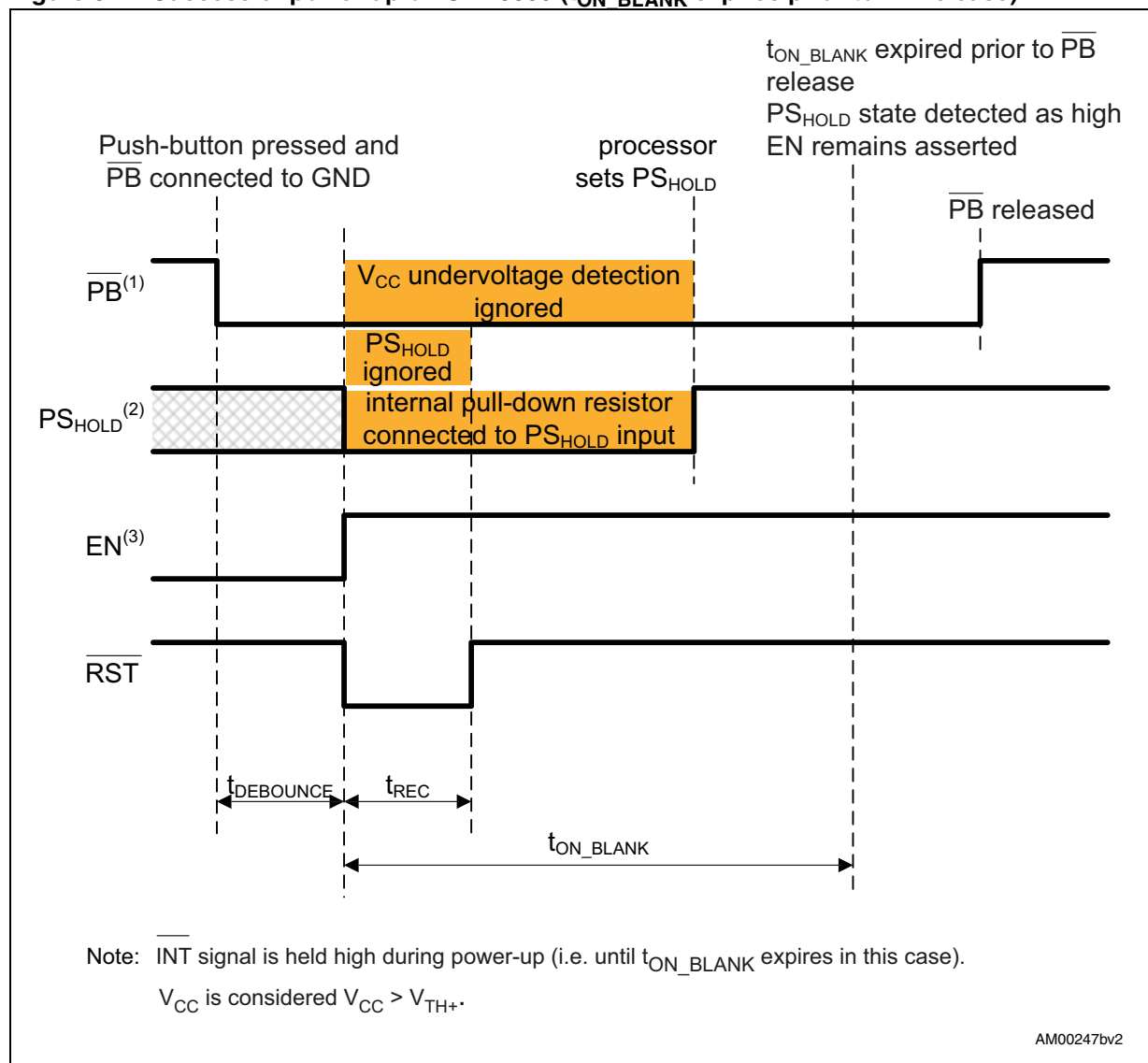
If the enable output is deasserted (i.e. EN is low or  $\overline{EN}$  is high), the STM660x device enters standby mode with low current consumption (see [Table 5](#)). In standby mode  $\overline{PB}$  input is only monitored for the falling edge. The external 1.5 V voltage reference is also disabled in standby mode.

## 4 Waveforms

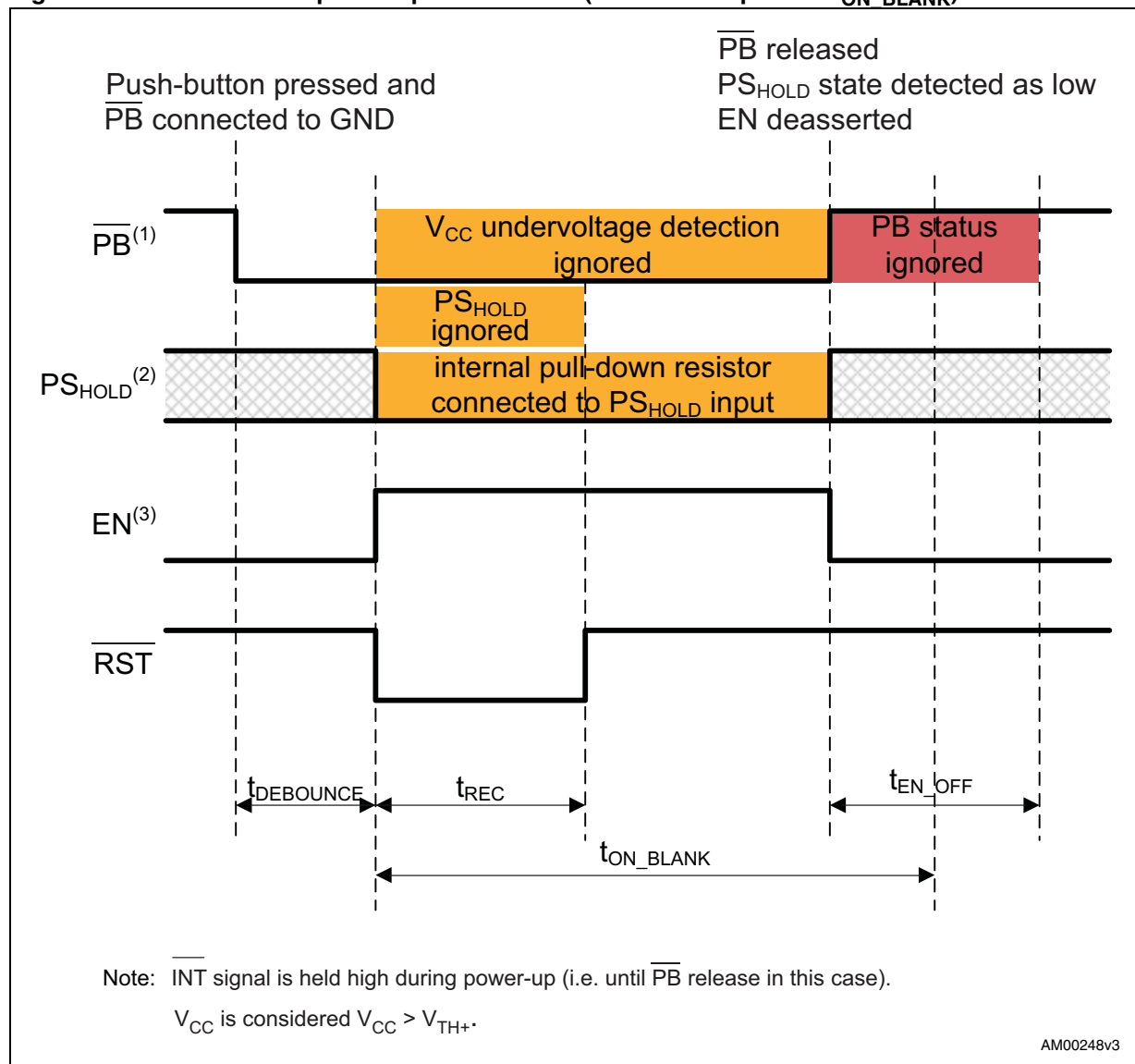
Figure 7. Successful power-up on STM6600 ( $\overline{\text{PB}}$  released prior to  $t_{\text{ON\_BLANK}}$  expiration)



1.  $\overline{\text{PB}}$  detection on falling and rising edges.
2. Internal pull-down resistor 300 k $\Omega$  is connected to  $\text{PS}_{\text{HOLD}}$  input during power-up.
3. EN signal is high even after  $\overline{\text{PB}}$  release, because processor sets  $\text{PS}_{\text{HOLD}}$  signal high before  $\overline{\text{PB}}$  is released.

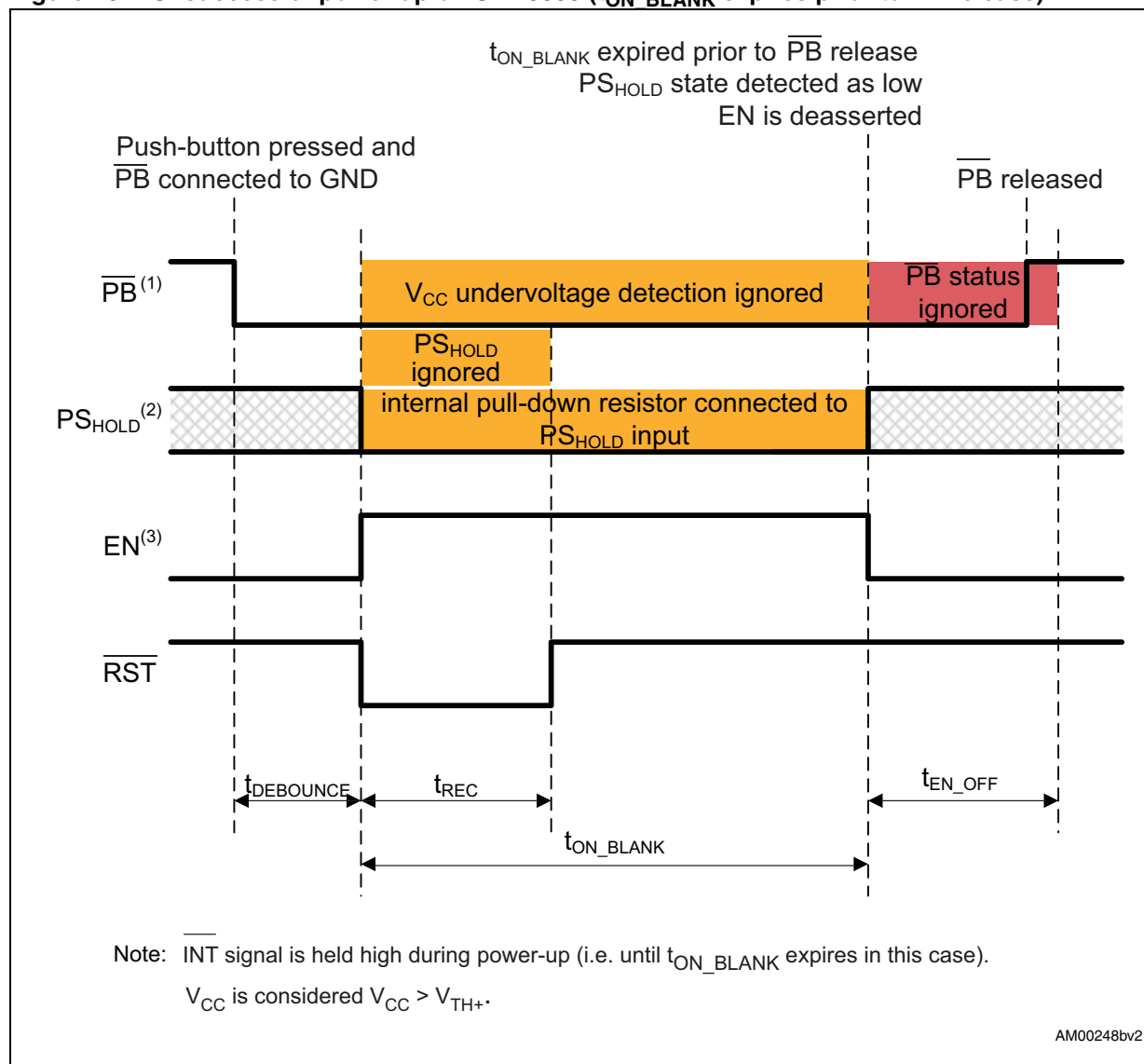
**Figure 8. Successful power-up on STM6600 ( $t_{ON\_BLANK}$  expires prior to  $\overline{PB}$  release)**

1.  $\overline{PB}$  detection on falling and rising edges.
2. Internal pull-down resistor 300 k $\Omega$  is connected to  $PS_{HOLD}$  input during power-up.
3.  $t_{ON\_BLANK}$  expires prior to  $\overline{PB}$  release so  $PS_{HOLD}$  is checked at its expiration.

Figure 9. Unsuccessful power-up on STM6600 ( $\overline{\text{PB}}$  released prior to  $t_{\text{ON\_BLANK}}$ )

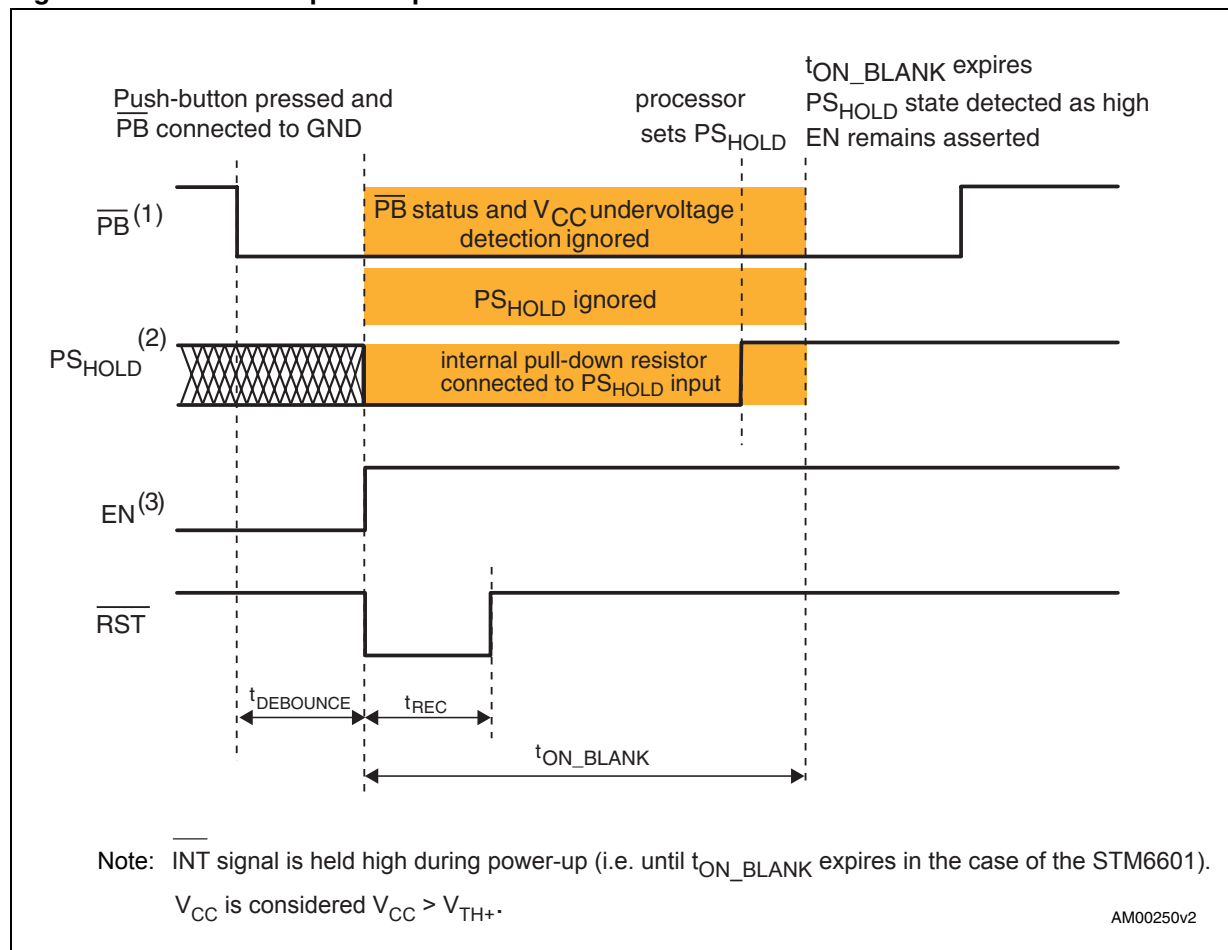
1.  $\overline{\text{PB}}$  detection on falling and rising edges.
2. Internal pull-down resistor 300 k $\Omega$  is connected to PS<sub>HOLD</sub> input during power-up.
3. EN signal goes low with  $\overline{\text{PB}}$  release, because processor did not force PS<sub>HOLD</sub> signal high.



**Figure 10. Unsuccessful power-up on STM6600 ( $t_{ON\_BLANK}$  expires prior to  $\overline{PB}$  release)**

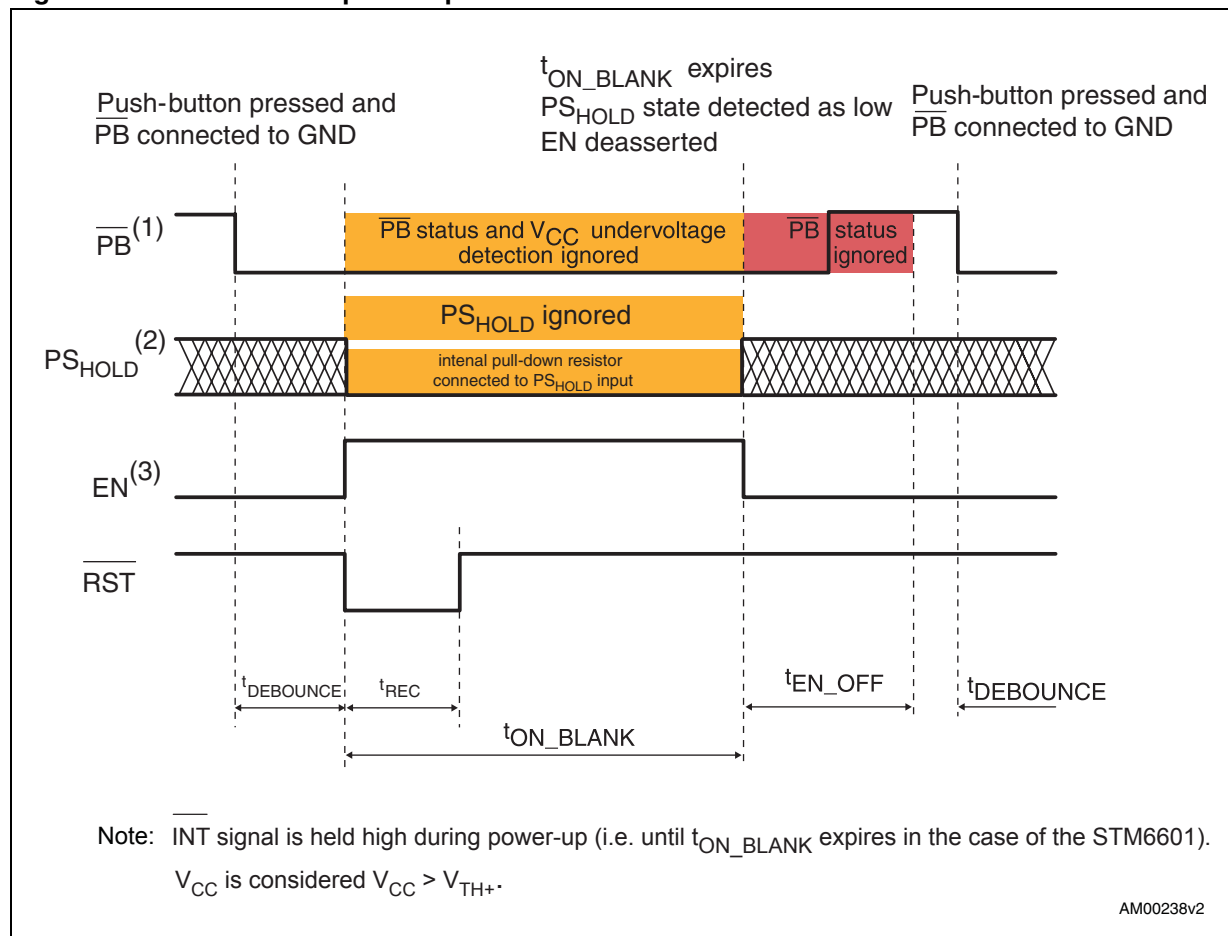
1.  $\overline{PB}$  detection on falling and rising edges.
2. Internal pull-down resistor 300 k $\Omega$  is connected to  $PS_{HOLD}$  input during power-up.
3.  $t_{ON\_BLANK}$  expires prior to  $\overline{PB}$  release so  $PS_{HOLD}$  is checked at its expiration.

Figure 11. Successful power-up on STM6601



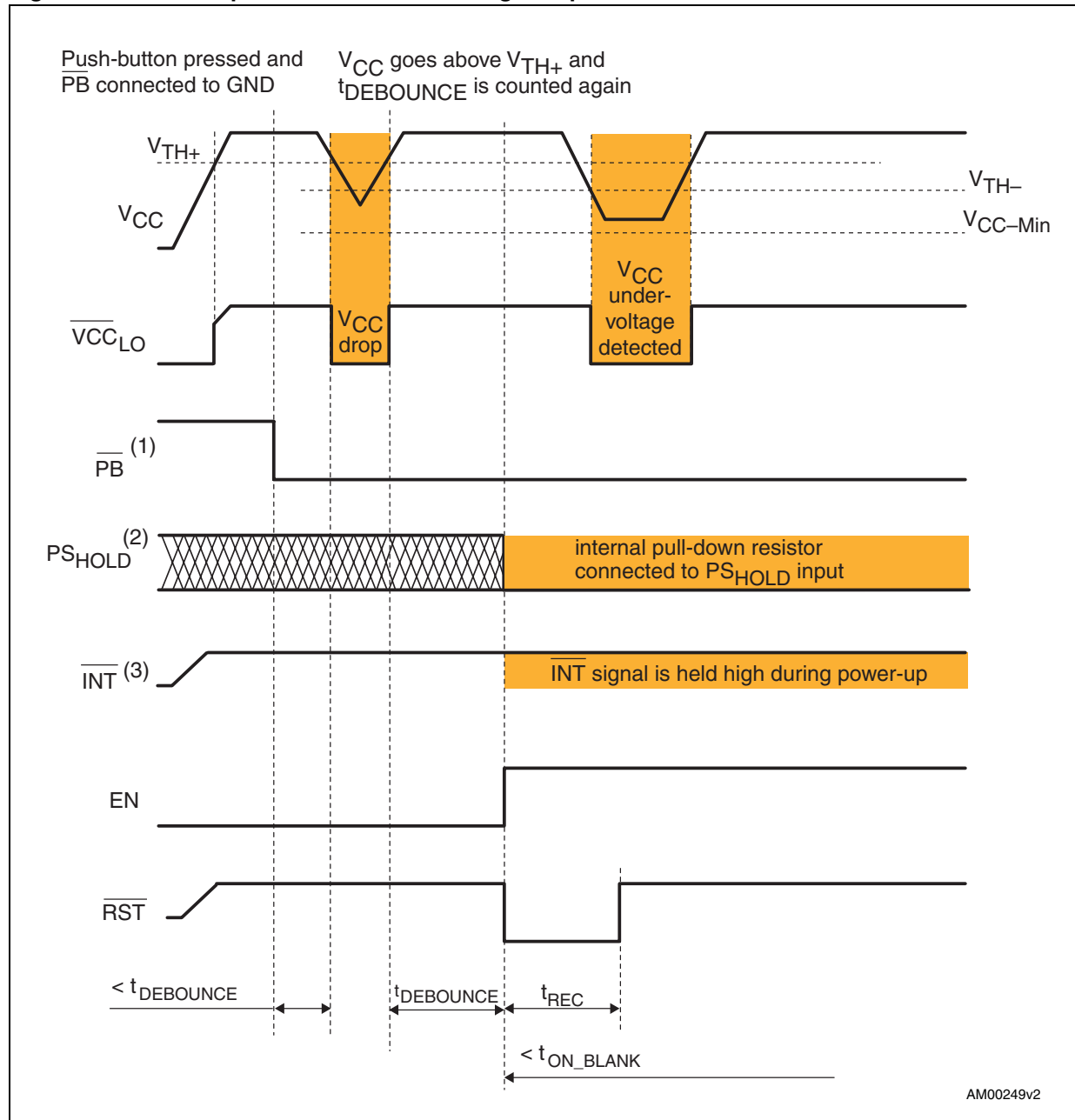
1.  $\overline{PB}$  detection on falling edge.
2. Internal pull-down resistor 300 k $\Omega$  is connected to  $PS_{HOLD}$  input during power-up.
3.  $PS_{HOLD}$  signal is ignored during  $t_{ON\_BLANK}$ . When  $t_{ON\_BLANK}$  expires, the level of the  $PS_{HOLD}$  signal is high therefore the  $EN$  signal remains asserted.

Figure 12. Unsuccessful power-up on STM6601



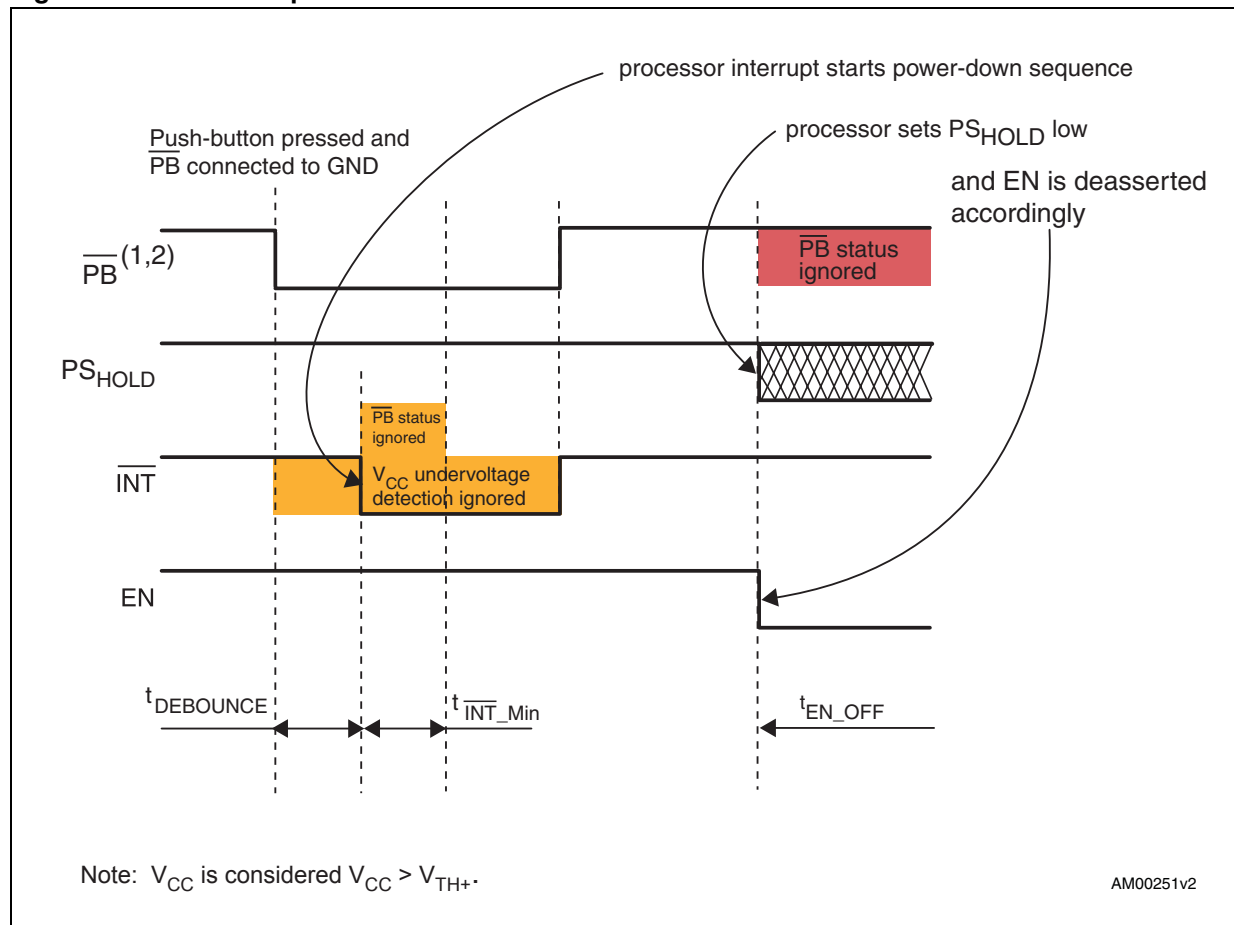
1.  $\overline{PB}$  detection on falling edge.
2. Internal pull-down resistor 300 k $\Omega$  is connected to PS\_HOLD input during power-up.
3. PS\_HOLD signal is ignored during  $t_{ON\_BLANK}$ . When  $t_{ON\_BLANK}$  expires, the level of the PS\_HOLD signal is not high therefore the EN signal goes low. Even releasing the PB button after the  $t_{ON\_BLANK}$  will not prevent this.

Figure 13. Power-up on STM660x with voltage dropout



1.  $\overline{\text{PB}}$  detection on falling and rising edges.
2. Internal pull-down resistor 300 k $\Omega$  is connected to  $\text{PS}_{\text{HOLD}}$  input during power-up.
3.  $\overline{\text{INT}}$  signal is held high during power-up.

**Figure 14.  $\overline{\text{PB}}$  interrupt**



1.  $\overline{\text{PB}}$  detection on falling edge.
2.  $\overline{\text{PB}}$  is released within  $t_{\text{SRD}}$  and that is why NO reset is asserted and EN is NOT deasserted immediately.

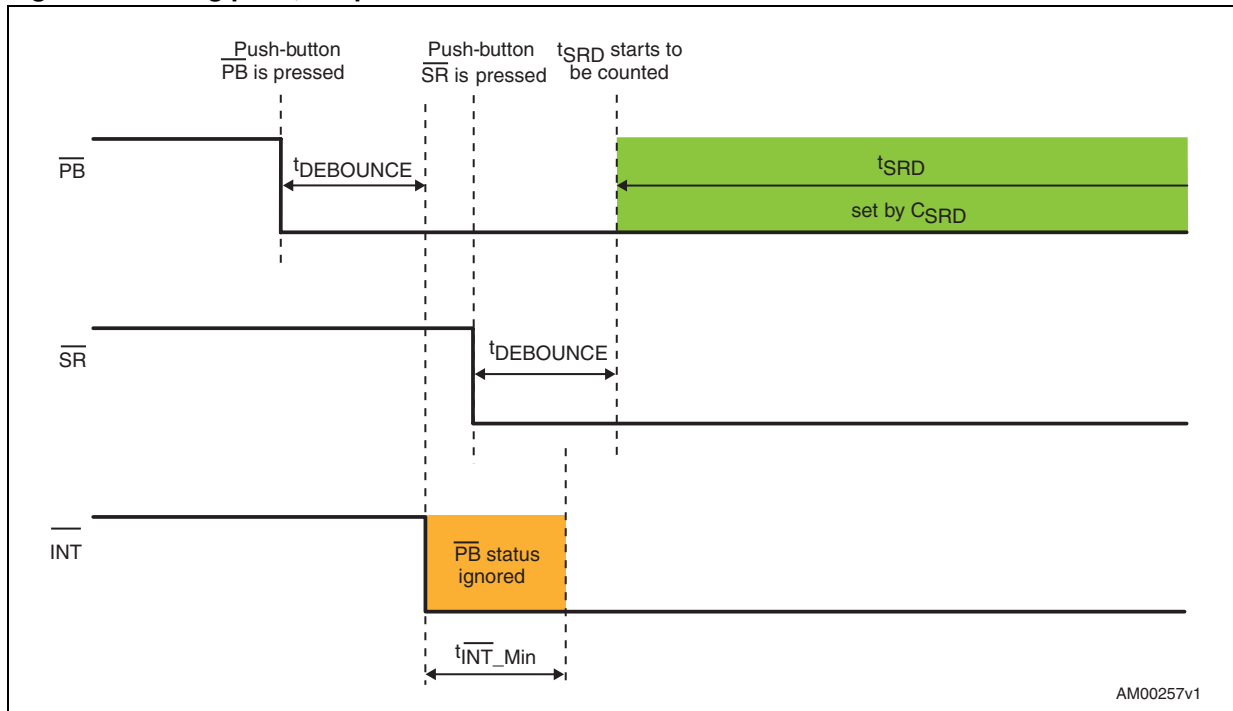
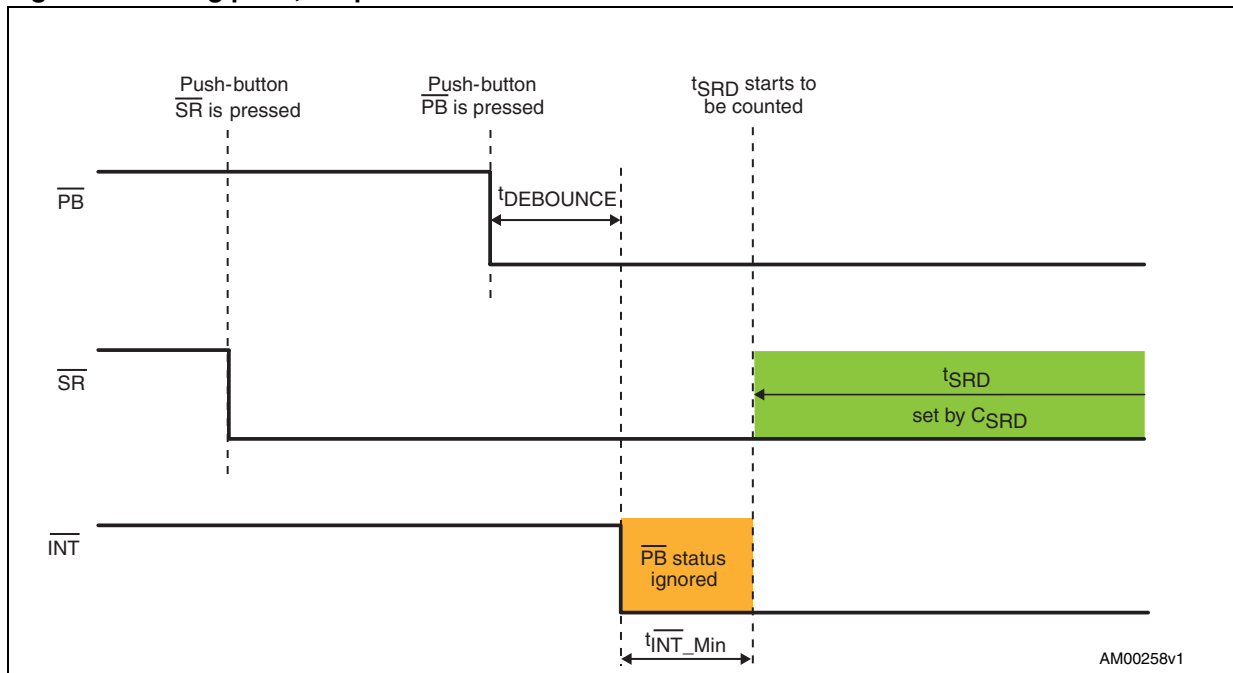
Figure 15. Long push,  $\overline{\text{PB}}$  pressed firstFigure 16. Long push,  $\overline{\text{SR}}$  pressed first

Figure 17. Invalid long push

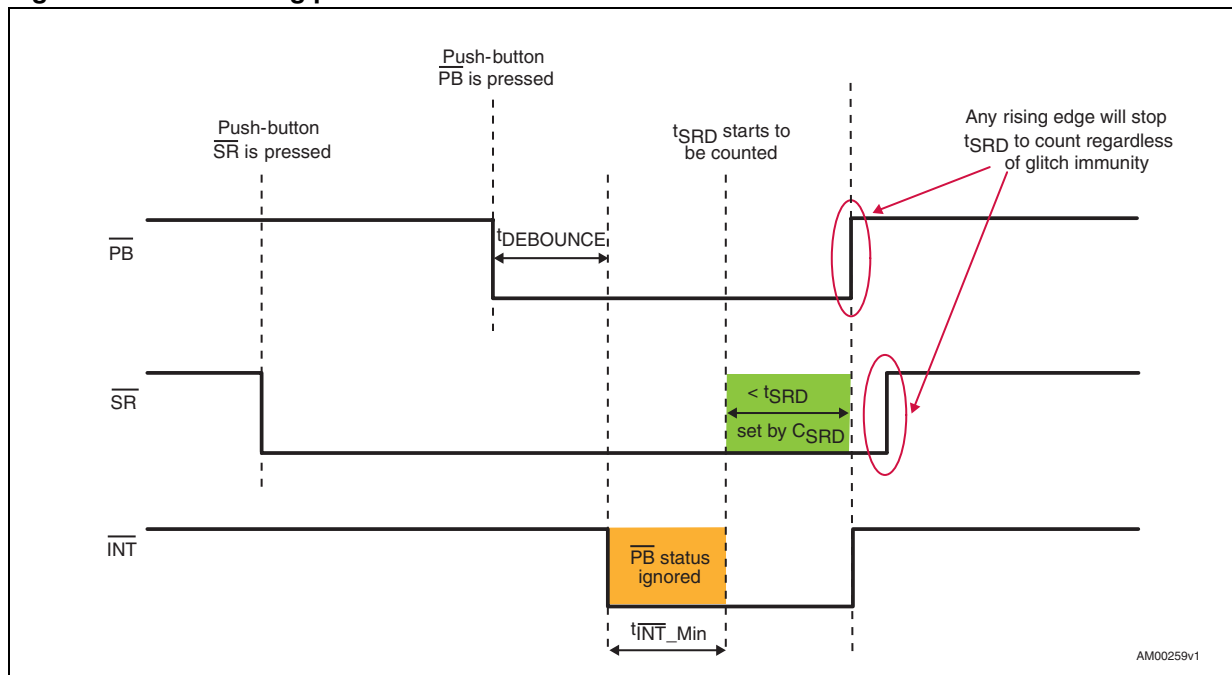
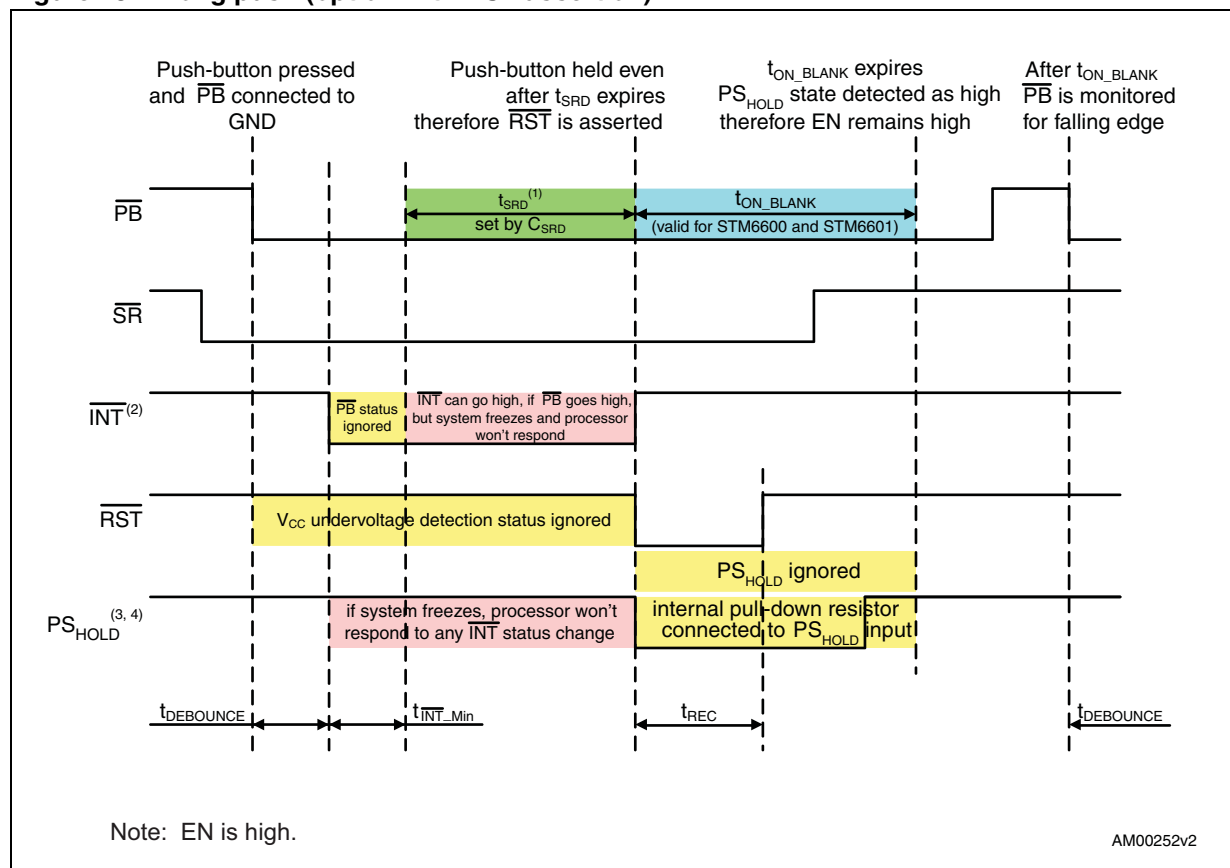
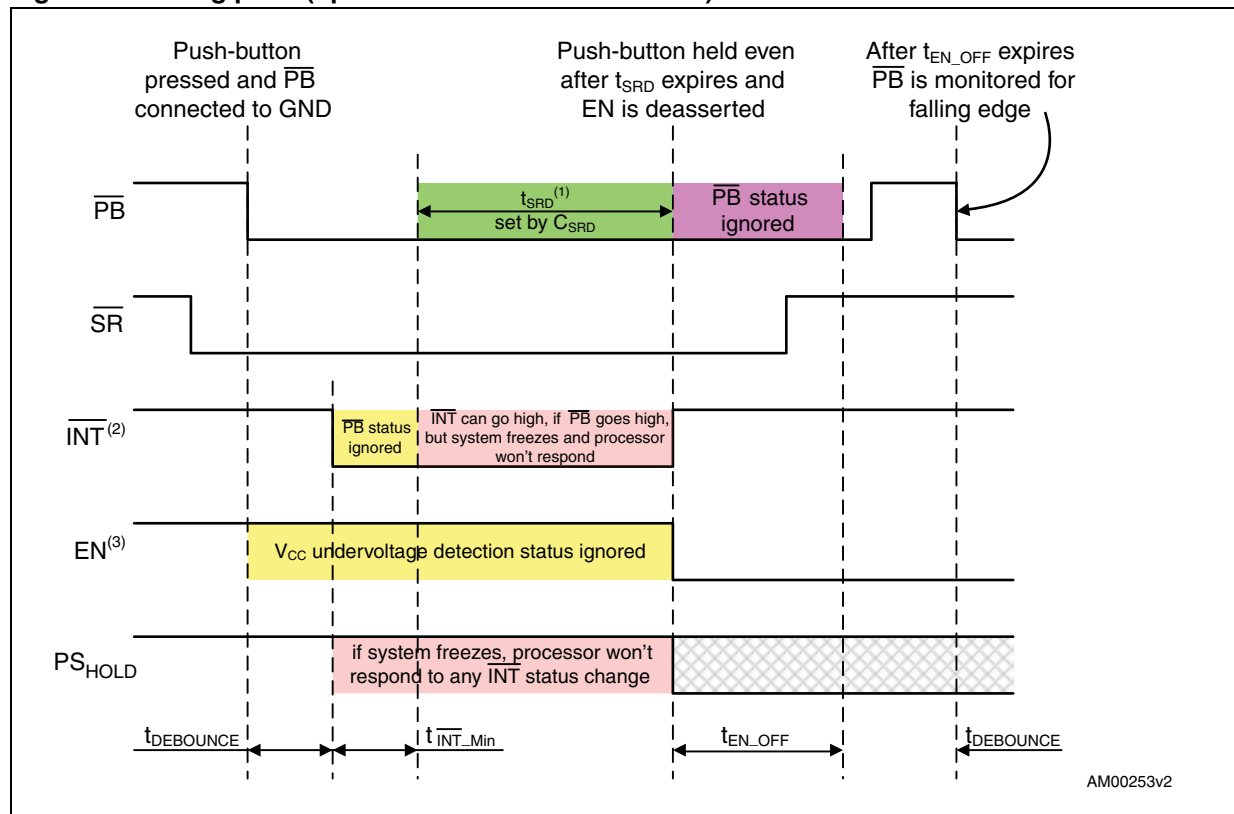


Figure 18. Long push (option with  $\overline{\text{RST}}$  assertion)

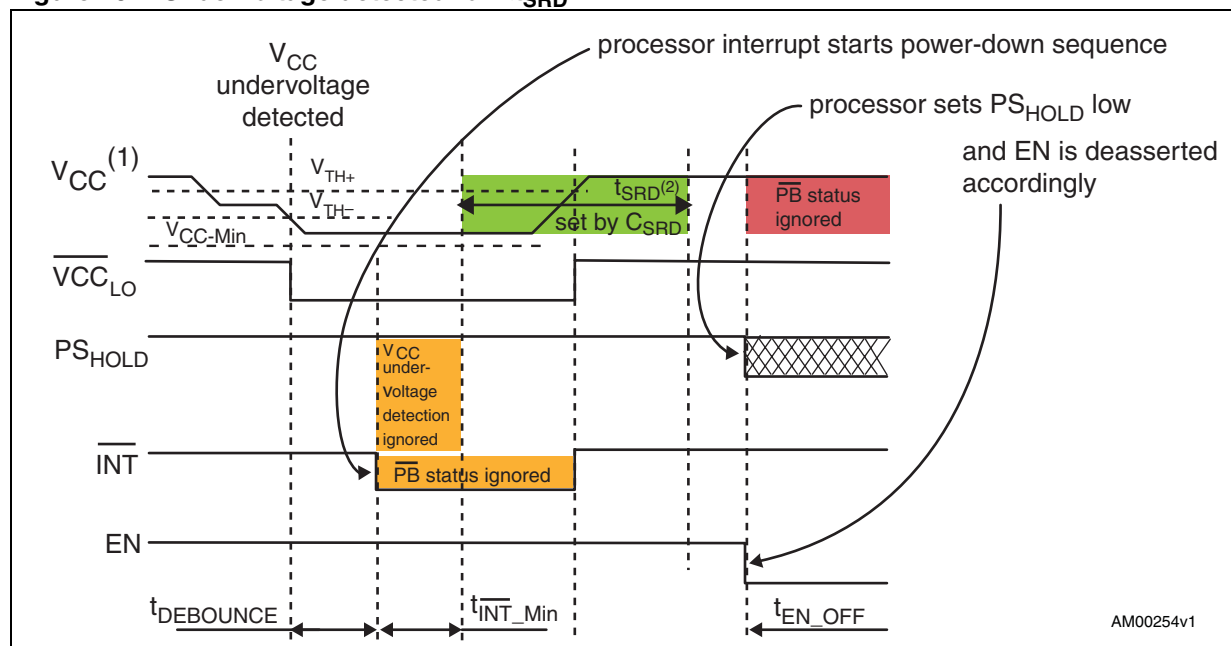
1.  $t_{\text{SRD}}$  period is set by external capacitor  $C_{\text{SRD}}$ .
2.  $\overline{\text{PB}}$  ignored during  $t_{\text{INT\_Min}}$ .
3.  $\text{PS}_{\text{HOLD}}$  signal is ignored during  $t_{\text{ON\_BLANK}}$ . Its level is checked after  $t_{\text{ON\_BLANK}}$  expires and if it is high the EN signal remains asserted, otherwise EN goes low.
4. Internal pull-down resistor 300 k $\Omega$  is connected to  $\text{PS}_{\text{HOLD}}$  input during startup when device is reset.



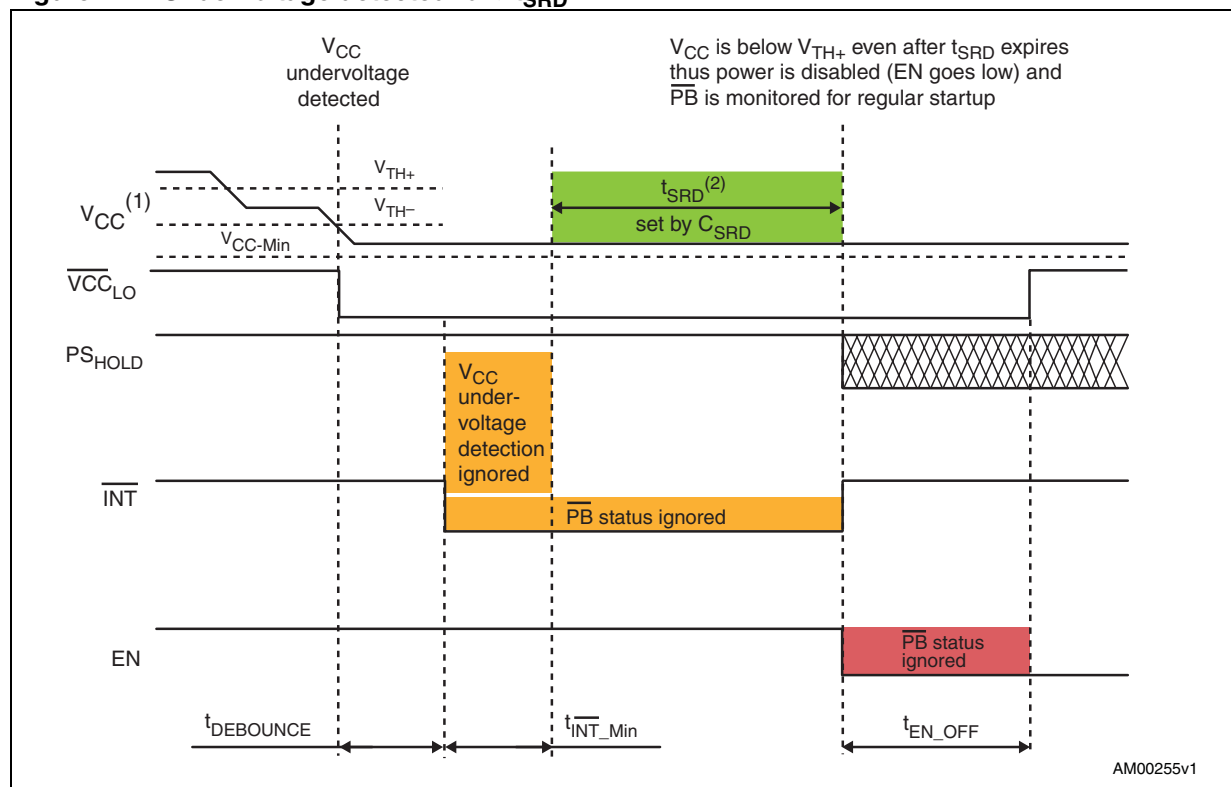
Figure 19. Long push (option with enable deassertion)



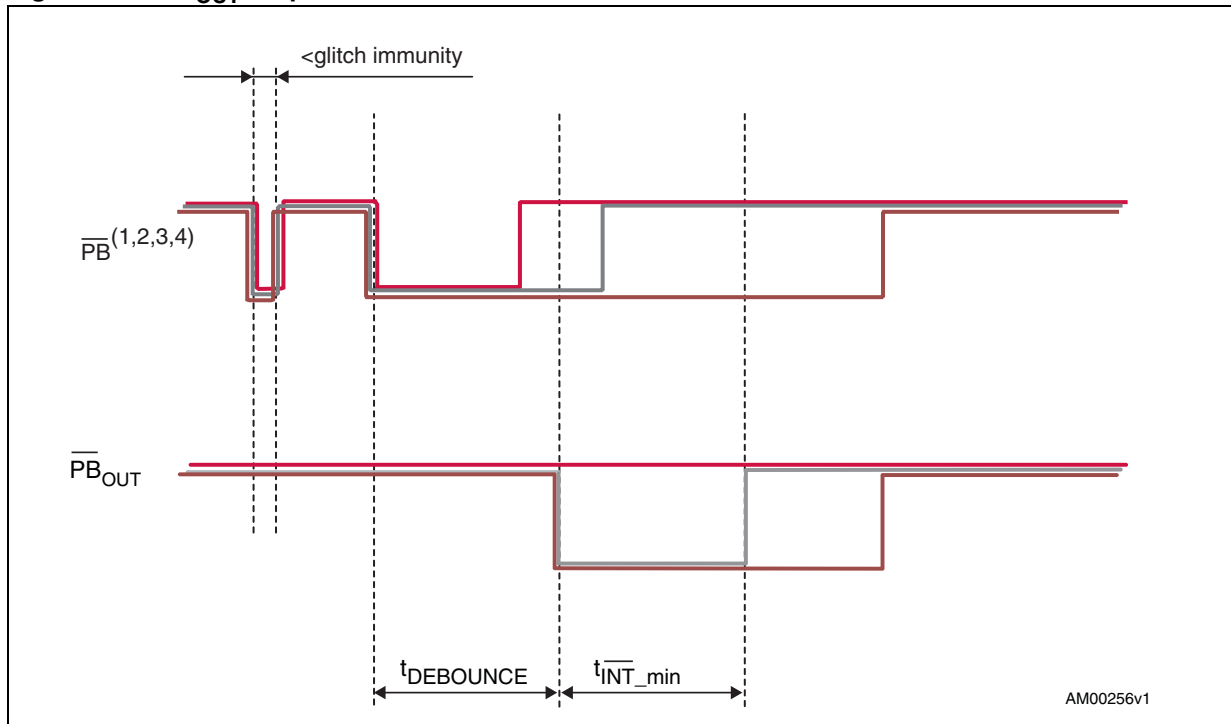
1.  $t_{SRD}$  period is set by external capacitor  $C_{SRD}$ .
2.  $\overline{PB}$  ignored during  $t_{INT\_Min}$ .
3. After  $t_{SRD}$  expires  $EN$  is forced low.

Figure 20. Undervoltage detected for  $<t_{SRD}$ 

1.  $V_{CC}$  goes above  $V_{TH+}$  within  $t_{SRD}$  thus power is not disabled after  $t_{SRD}$  expires.
2.  $t_{SRD}$  period is set by external capacitor  $C_{SRD}$ .

Figure 21. Undervoltage detected for  $>t_{SRD}$ 

1. After  $t_{SRD}$  expires  $V_{CC}$  is still insufficient (below  $V_{TH+}$ ) thus power is disabled ( $EN$  goes low or  $\overline{EN}$  goes high).
2.  $t_{SRD}$  period is set by external capacitor  $C_{SRD}$ .

Figure 22.  $\overline{PB}_{OUT}$  output waveform

1. Pulses on  $\overline{PB}$  shorter than glitch immunity are ignored.
2. Pulses on  $\overline{PB}$  shorter than  $t_{DEBOUNCE}$  are not recognized by  $\overline{PB}_{OUT}$ .
3. Minimum pulse width on  $\overline{PB}_{OUT}$  is  $t_{INT\_Min}$ .
4. If push-button is held longer than  $t_{DEBOUNCE} + t_{INT\_Min}$ ,  $\overline{PB}_{OUT}$  goes high when the push-button is released.

# 5 Typical operating characteristics

Figure 23. Supply current vs. temperature, normal state

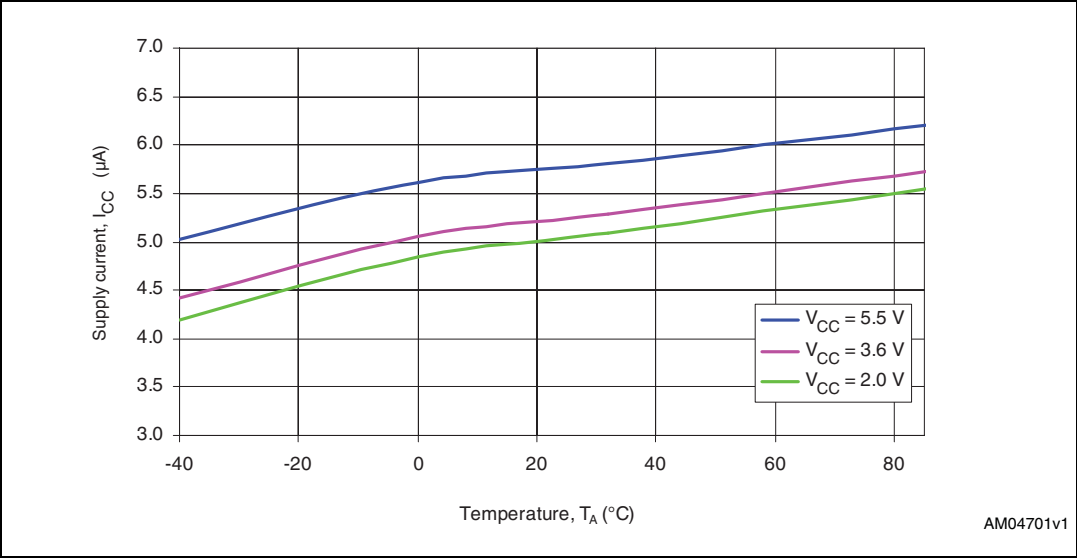


Figure 24. Supply current vs. temperature, standby state

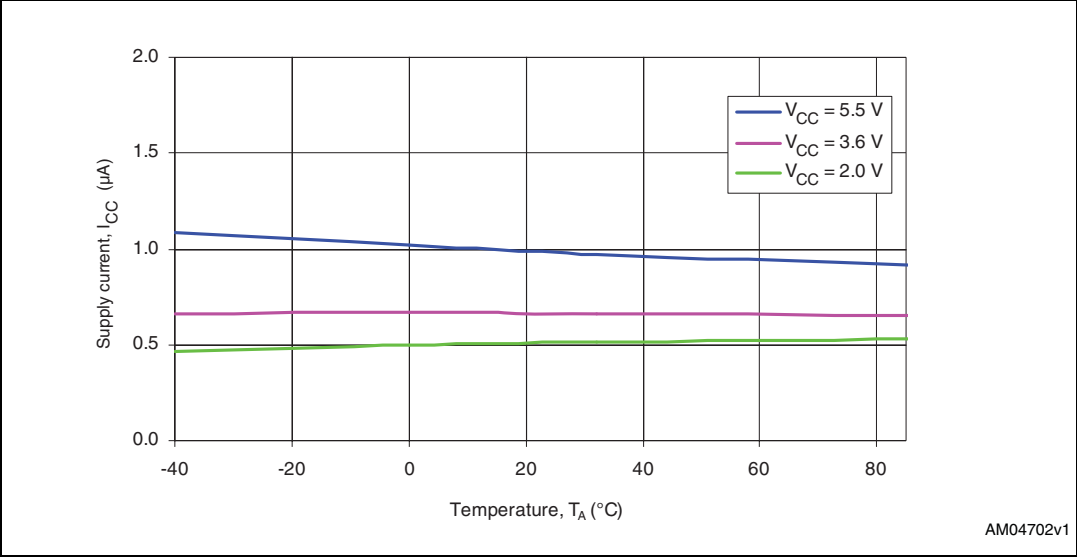


Figure 25. Supply current vs. supply voltage, normal state

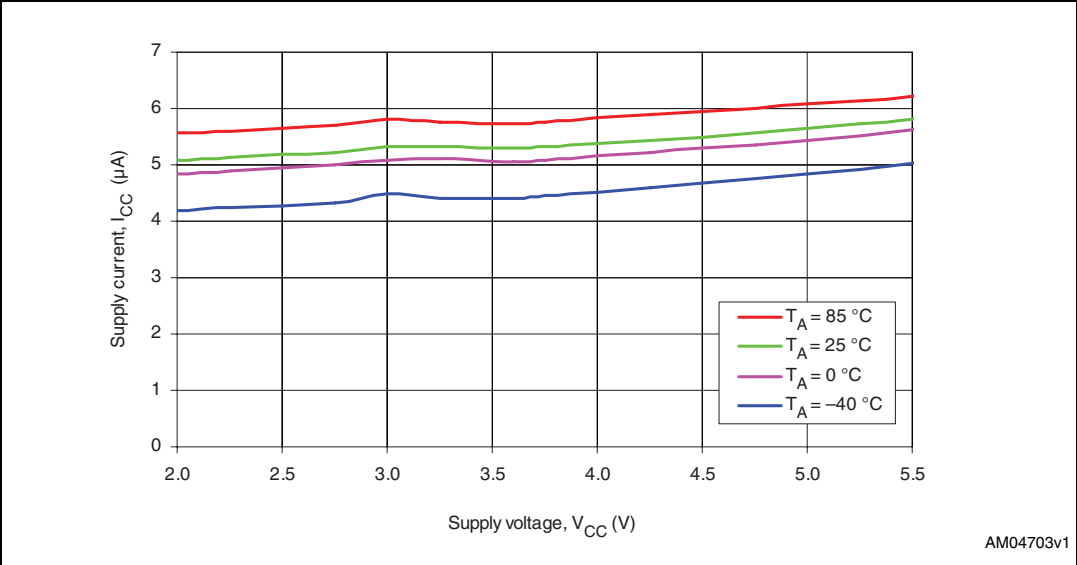
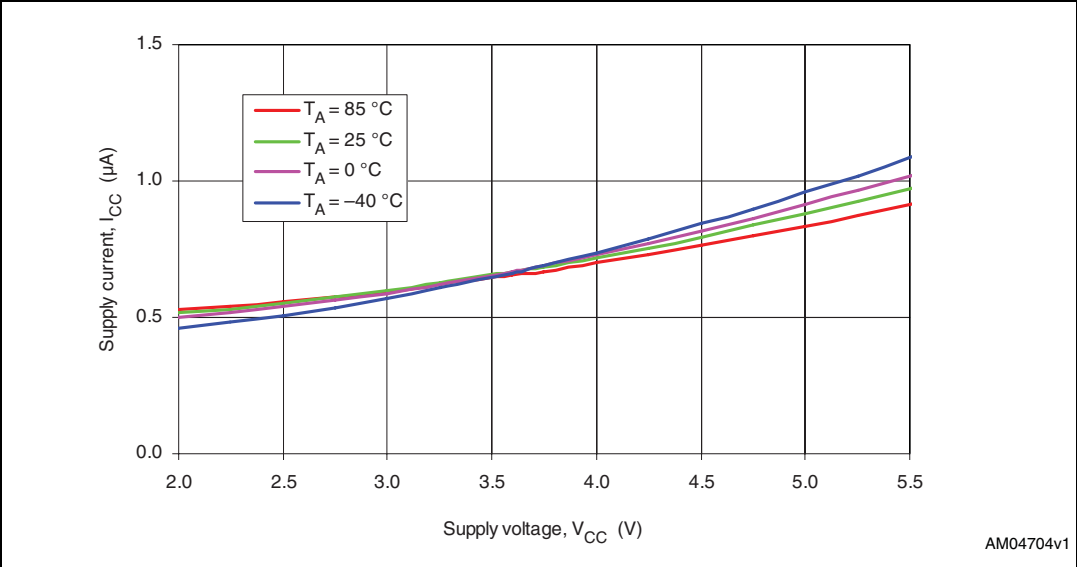


Figure 26. Supply current vs. supply voltage, standby state



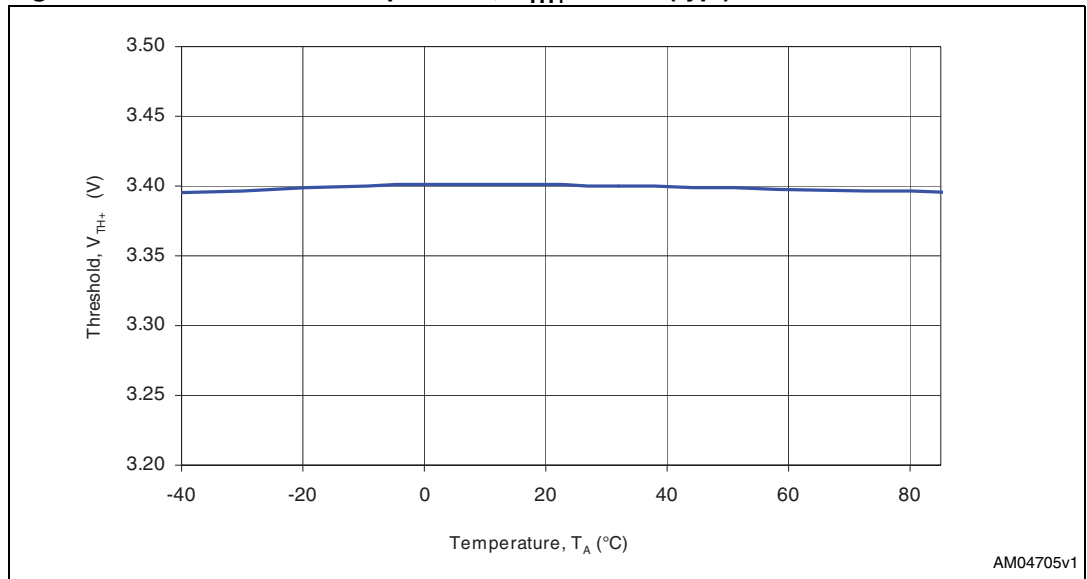
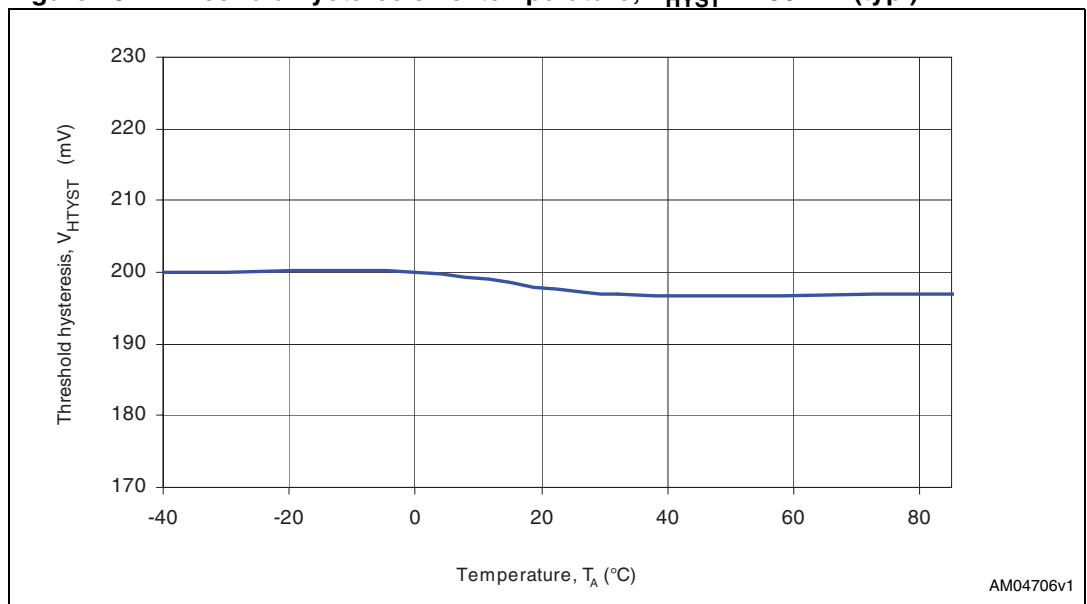
**Figure 27. Threshold vs. temperature,  $V_{TH+} = 3.4$  V (typ.)****Figure 28. Threshold hysteresis vs. temperature,  $V_{HYST} = 200$  mV (typ.)**

Figure 29. Debounce period vs. supply voltage

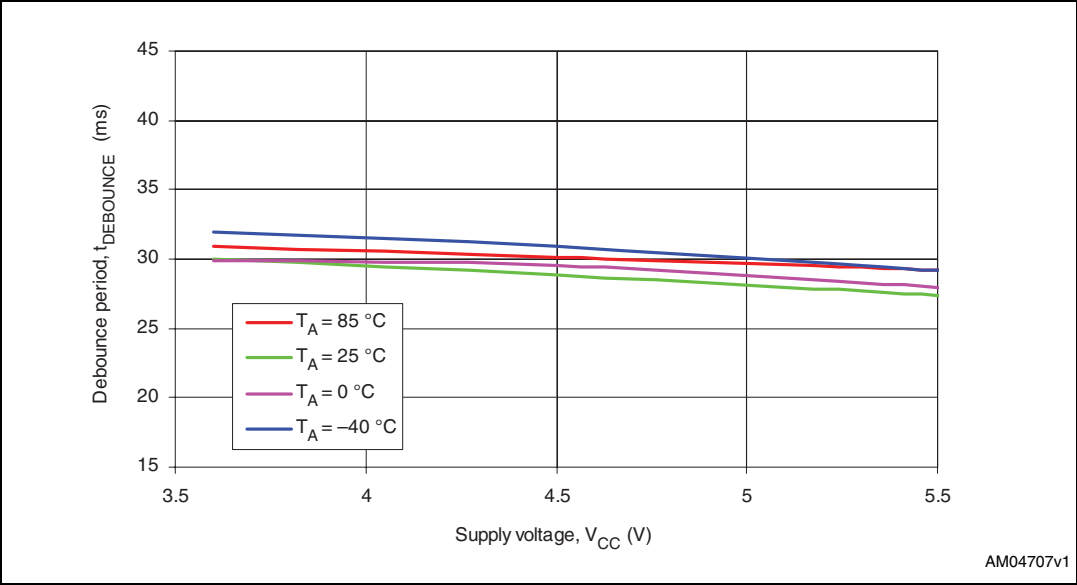
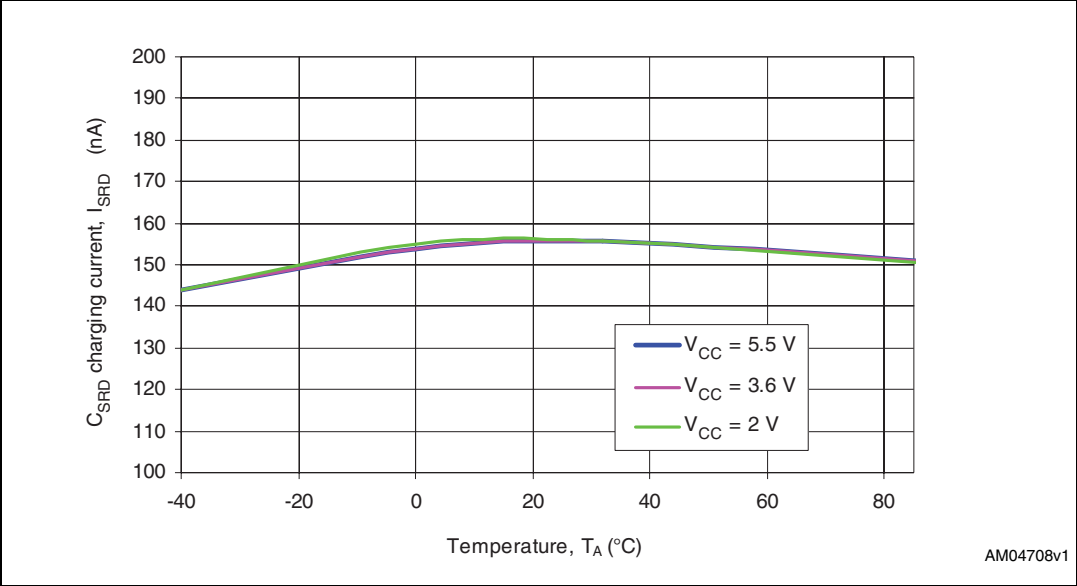
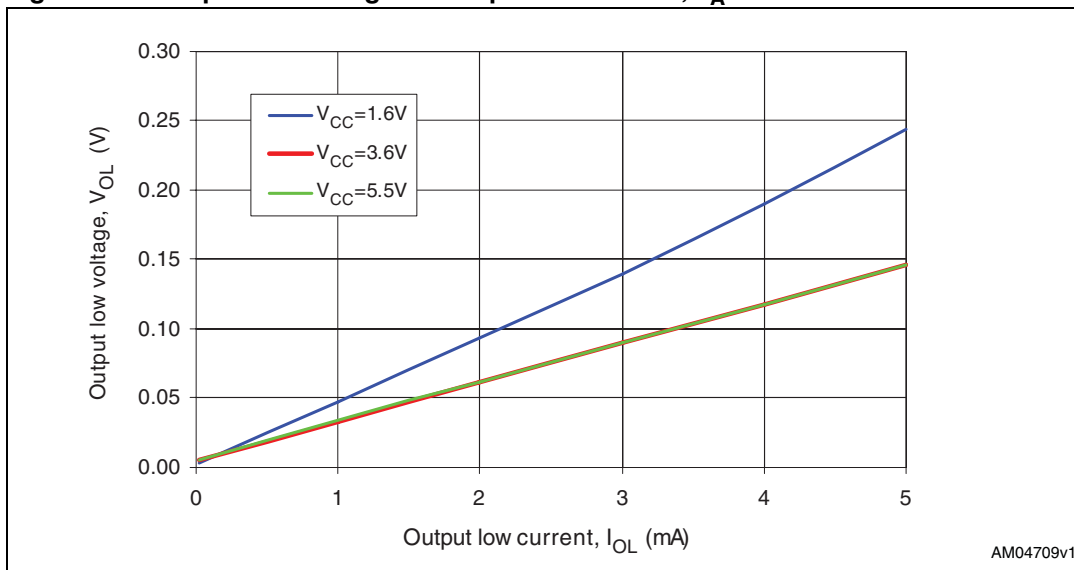
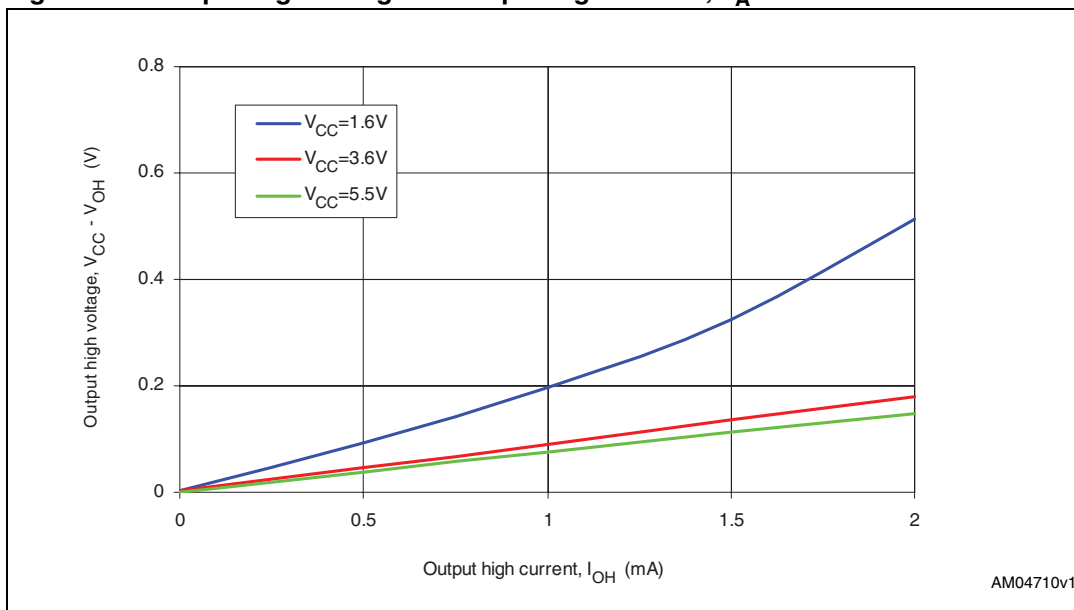


Figure 30.  $C_{SRD}$  charging current vs. temperature,  $V_{CC} = 3.6\text{ V}$



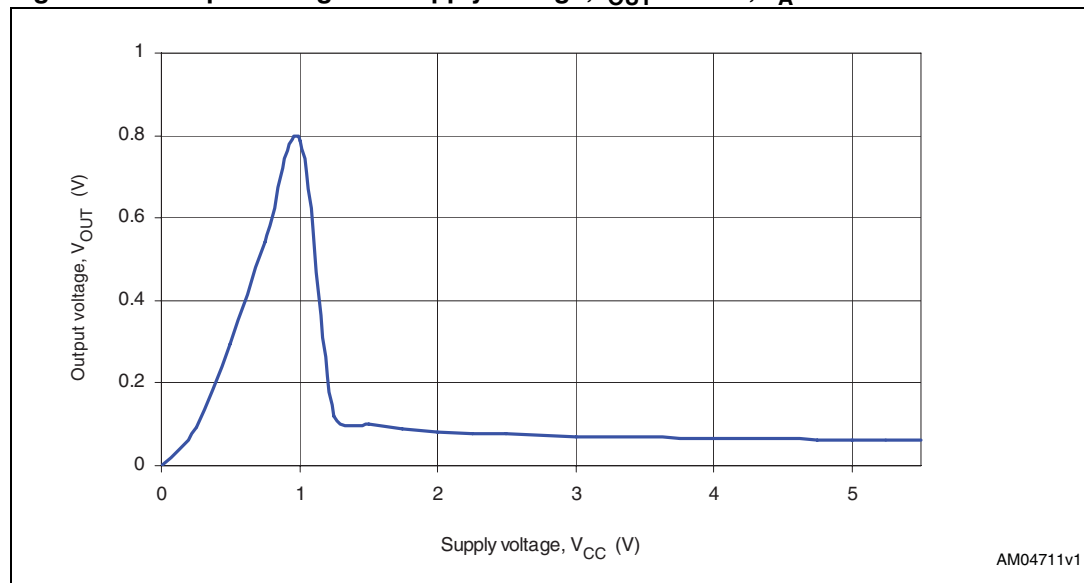
**Figure 31. Output low voltage vs. output low current,  $T_A = 25^\circ\text{C}$** 

Note: Characteristics valid for all the outputs ( $\overline{EN}$ ,  $\overline{EN}$ ,  $\overline{RST}$ ,  $\overline{INT}$ ,  $\overline{PB}_{OUT}$  and  $\overline{VCC}_{LO}$ ).

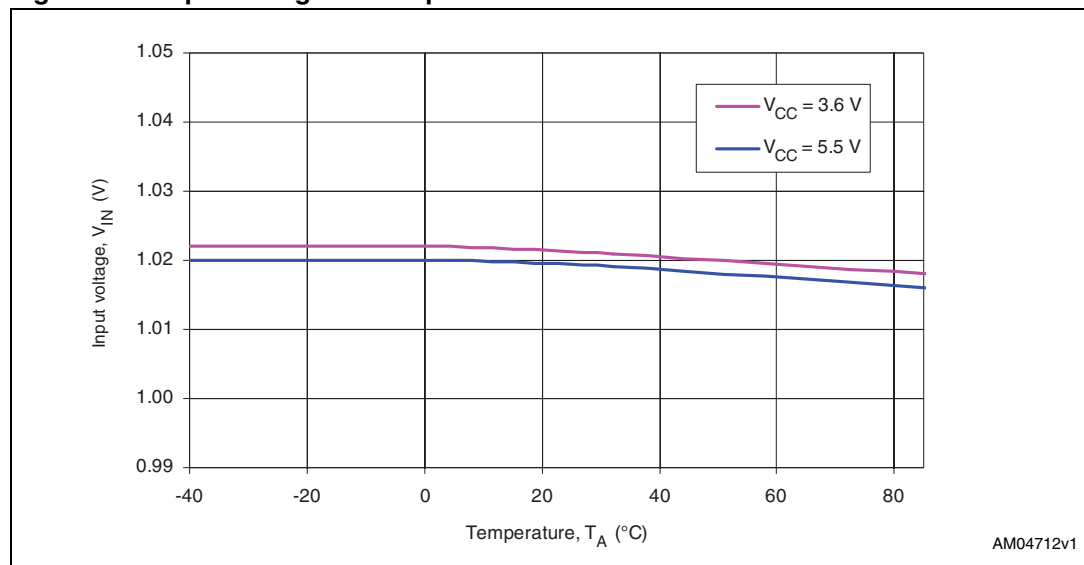
**Figure 32. Output high voltage vs. output high current,  $T_A = 25^\circ\text{C}$** 

Note: Characteristics valid for  $\overline{EN}$  and  $\overline{EN}$  outputs.

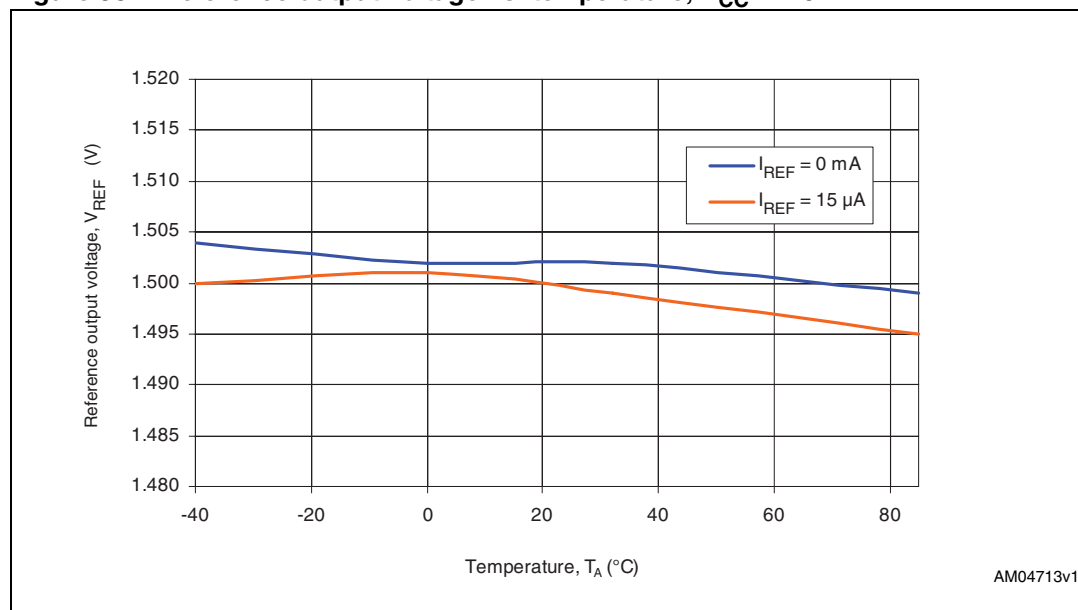


**Figure 33. Output voltage vs. supply voltage,  $I_{OUT} = 1\text{ mA}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$** 

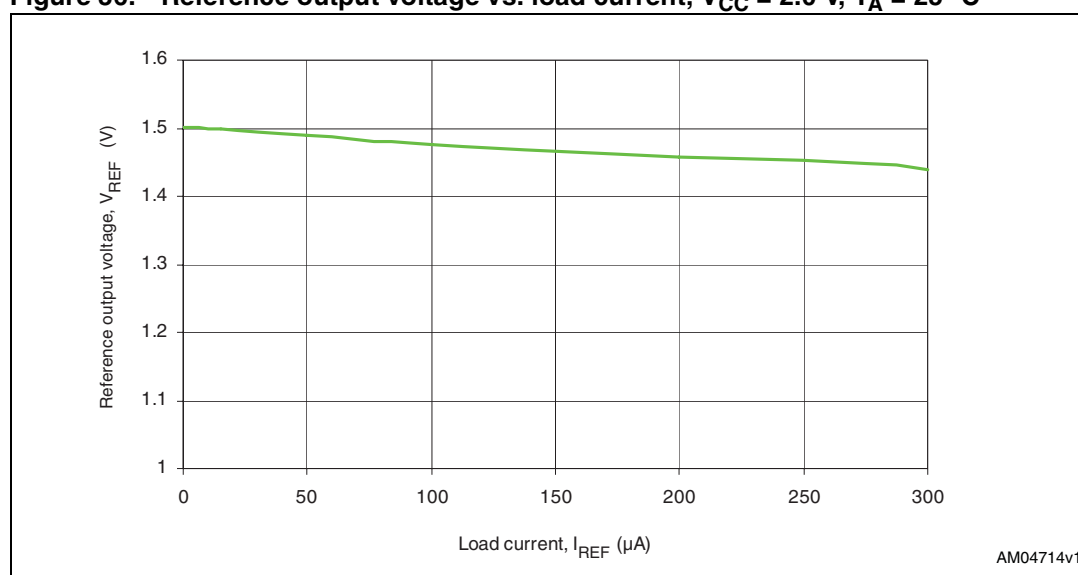
**Note:** Characteristics valid for all the outputs ( $\overline{EN}$ ,  $\overline{EN}$ ,  $\overline{RST}$ ,  $\overline{INT}$ ,  $\overline{PB}_{OUT}$  and  $\overline{VCC}_{LO}$ ).

**Figure 34. Input voltage vs. temperature**

**Note:** Characteristics valid for  $\overline{PB}$ ,  $\overline{SR}$  and  $PS_{HOLD}$  inputs.

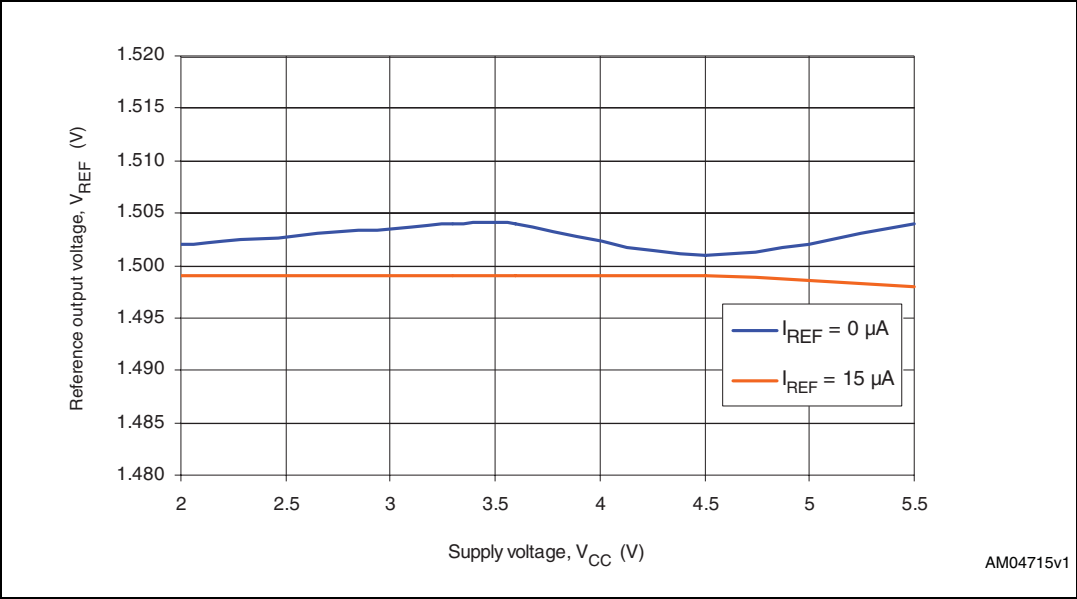
**Figure 35. Reference output voltage vs. temperature,  $V_{CC} = 2.0\text{ V}$** 

Note:  $1\text{ }\mu\text{F}$  capacitor is connected to the  $V_{REF}$  pin.

**Figure 36. Reference output voltage vs. load current,  $V_{CC} = 2.0\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$** 

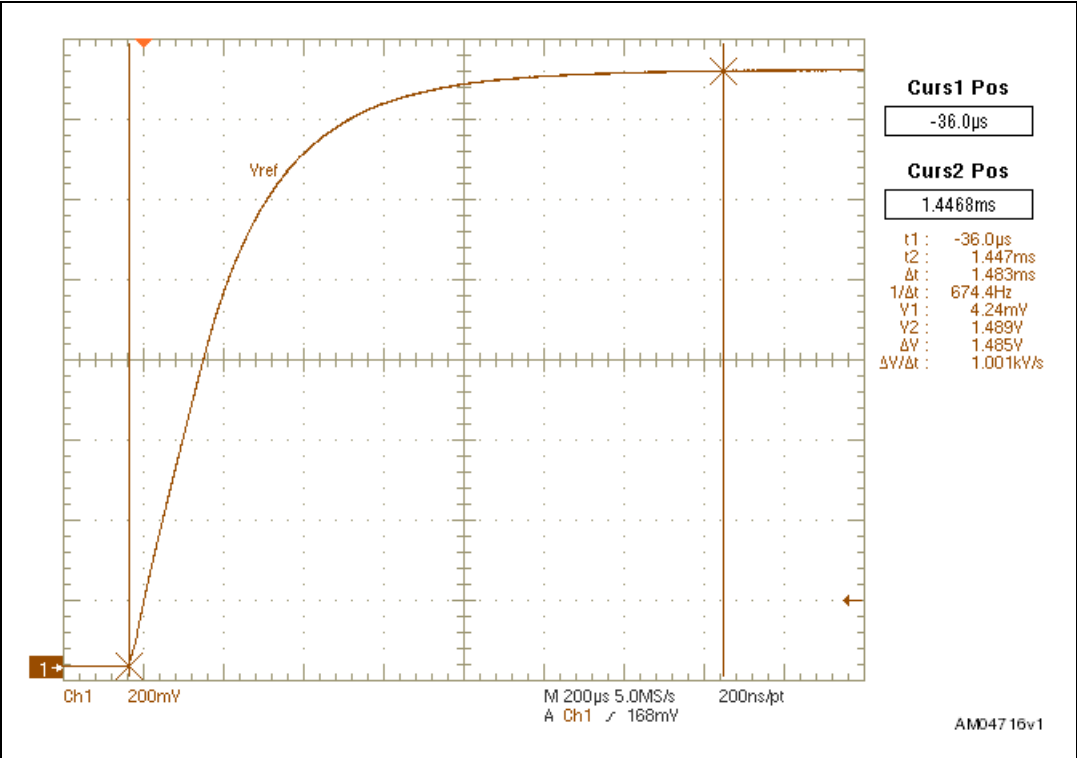
Note:  $1\text{ }\mu\text{F}$  capacitor is connected to the  $V_{REF}$  pin.

Figure 37. Reference output voltage vs. supply voltage,  $T_A = 25\text{ }^{\circ}\text{C}$

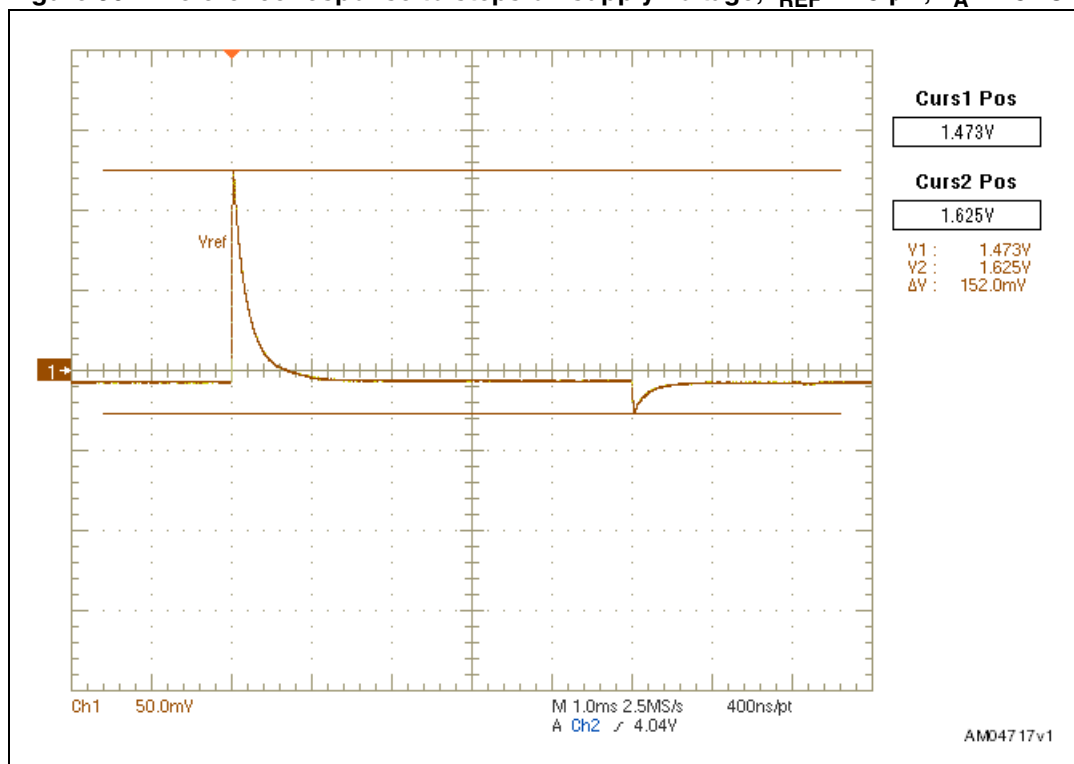


Note: 1  $\mu\text{F}$  capacitor is connected to the  $V_{REF}$  pin.

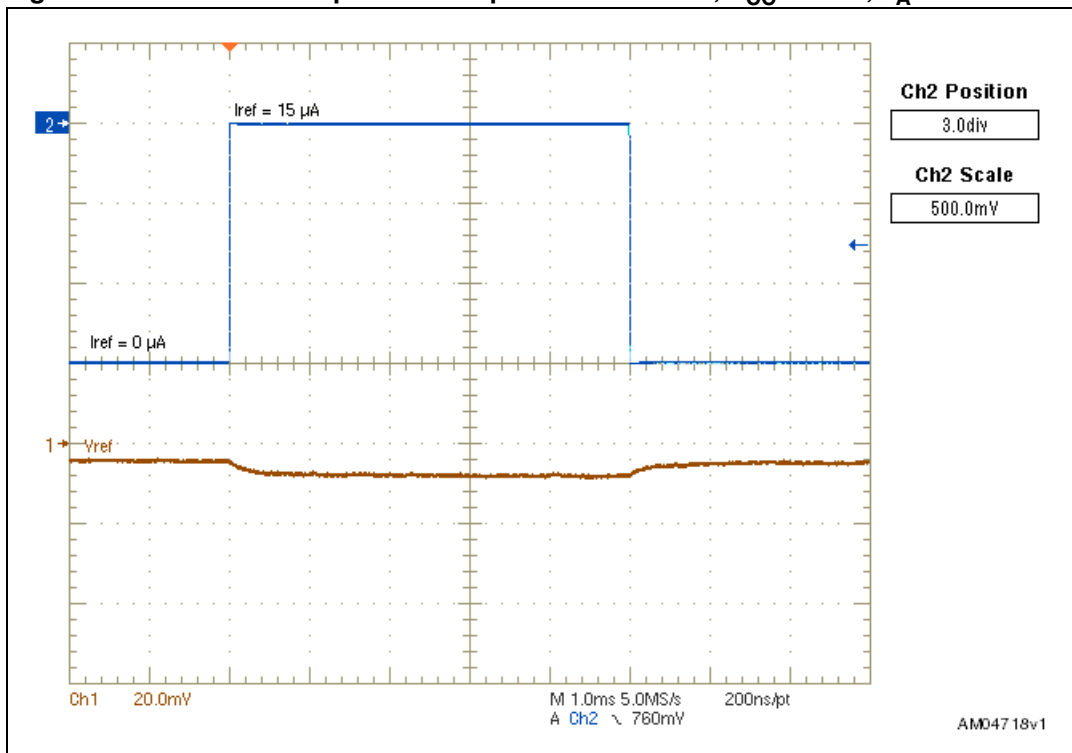
Figure 38. Reference startup,  $I_{REF} = 15\text{ }\mu\text{F}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$



Note: 1  $\mu\text{F}$  capacitor is connected to the  $V_{REF}$  pin.

**Figure 39. Reference response to steps on supply voltage,  $I_{REF} = 15 \mu A$ ,  $T_A = 25^\circ C$** 

- Note:
- 1 Supply voltage goes from 3.6 V to 5.5 V and back to 3.6 V, ramp 1 V / 100 ns.
  - 2 1  $\mu F$  capacitor is connected to the  $V_{REF}$  pin.

Figure 40. Reference response to steps in load current,  $V_{CC} = 3.6\text{ V}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ 

- Note:
- 1 Supply voltage goes from 0  $\mu\text{A}$  to 15  $\mu\text{A}$  and back to 0  $\mu\text{A}$ , ramp 1  $\mu\text{A}$  / 100 ns.
  - 2 1  $\mu\text{F}$  capacitor is connected to the  $V_{REF}$  pin.

## 6 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Min.	Max.	Unit	Remarks
$V_{CC}$	Input supply voltage	-0.3	+7.0	V	
	Input voltages on $\overline{PB}$ , $\overline{SR}$ , $PS_{HOLD}$ and $C_{SRD}$	-0.3	$V_{CC} + 0.3$	V	
	Output voltages on $\overline{EN}$ ( $\overline{EN}$ ), $\overline{RST}$ and $\overline{INT}$	-0.3	$V_{CC} + 0.3$	V	
$V_{ESD}$	Electrostatic protection	-2	+2	kV	Human body model (all pins)
		-8	+8	kV	Human body model ( $\overline{PB}$ and $\overline{SR}$ )
$V_{ESD}$	Electrostatic protection	-1000	+1000	V	Charged device model
$V_{ESD}$	Electrostatic protection	-200	+200	V	Machine model
$V_{ESD}$	Point discharge on $\overline{PB}$ and $\overline{SR}$ inputs	-8	+8	kV	IEC61000-4-2
$V_{ESD}$	Air discharge on $\overline{PB}$ and $\overline{SR}$ inputs	-15	+15	kV	IEC61000-4-2
$T_A$	Operating ambient temperature	-40	+85	°C	
$T_{STG}$	Storage temperature	-45	+150	°C	
$T_{SLD}^{(1)}$	Lead solder temperature for 10 seconds		+260	°C	
$\theta_{JA}$	Thermal resistance (junction to ambient)		+132.4	°C/W	

1. Reflow at peak temperature of 260°C. The time above 255°C must not exceed 30 seconds.

## 7 DC and AC characteristics

This section summarizes the operating measurement conditions and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the measurement conditions summarized in [Table 4](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 4. Operating and AC measurement conditions**

Parameter	Condition	Unit
V <sub>CC</sub> supply voltage	1.6 to 5.5	V
Ambient operating temperature (T <sub>A</sub> )	–40 to 85	°C
Input rise and fall times	≤ 5	ns

**Table 5. DC and AC characteristics**

Symbol	Parameter	Test condition <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
V <sub>CC</sub>	Supply voltage		1.6		5.5	V
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = 3.6 V, no load		6	8	μA
		Standby mode, enable deasserted, V <sub>CC</sub> = 3.6 V			1	μA
V <sub>TH+</sub>	Power-on lockout voltage (see <a href="#">Table 10</a> for detailed listing)		2.40	2.50	2.60	V
			3.00	3.10	3.20	
			3.20	3.30	3.40	
			3.29	3.40	3.51	
			3.39	3.50	3.61	
V <sub>HYST</sub>	Threshold hysteresis (see <a href="#">Table 10</a> for detailed listing)			200		mV
				500		
V <sub>TH–</sub>	Forced power-off voltage (see <a href="#">Table 10</a> for detailed listing)			V <sub>TH+</sub> – V <sub>HYST</sub>		V
t <sub>TH–</sub>	Undervoltage detection to INT̄ delay	V <sub>CC</sub> ≥ 2.0 V	20	32	44	ms
t <sub>ON_BLANK</sub>	Blanking period (see <a href="#">Table 10</a> for detailed listing) <sup>(3)</sup>		1.4	2.2	3.0	s
			5.6	8.8	12.0	
			11.2	17.6	24.0	
	RST̄ assertion to EN (EN) assertion delay during power-up	V <sub>CC</sub> = 3.6 V		100		ns

Table 5. DC and AC characteristics (continued)

Symbol	Parameter	Test condition <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
<b><math>\overline{\text{PB}}</math></b>						
$V_{\text{IL}}$	Input low voltage	$V_{\text{CC}} \geq 2.0 \text{ V}$ , enable asserted			0.99	V
$V_{\text{IH}}$	Input high voltage	$V_{\text{CC}} \geq 2.0 \text{ V}$ , enable asserted	1.05			V
$t_{\text{DEBOUNCE}}$	Debounce period	$V_{\text{CC}} \geq 2.0 \text{ V}$	20	32	44	ms
$R_{\overline{\text{PB}}}$	Internal pull-up resistor	$V_{\text{CC}} = 5.5 \text{ V}$ , input asserted	65	100	135	k $\Omega$
<b><math>\overline{\text{SR}}</math></b>						
$V_{\text{IL}}$	Input low voltage				0.99	V
$V_{\text{IH}}$	Input high voltage		1.05			V
$t_{\text{DEBOUNCE}}$	Debounce period		20	32	44	ms
$R_{\overline{\text{SR}}}^{(4)}$	Internal pull-up resistor	$V_{\text{CC}} = 5.5 \text{ V}$ , input asserted	65	100	135	k $\Omega$
<b><math>\overline{\text{PB}}_{\text{OUT}}</math></b>						
$V_{\text{OL}}$	Output low voltage	$V_{\text{CC}} = 2 \text{ V}$ , $I_{\text{SINK}} = 1 \text{ mA}$ , $\overline{\text{PB}}_{\text{OUT}}$ asserted			0.3	V
	$\overline{\text{PB}}_{\text{OUT}}$ leakage current	$V_{\overline{\text{PB}}_{\text{OUT}}} = 3 \text{ V}$ , $\overline{\text{PB}}_{\text{OUT}}$ open drain	-0.1		+0.1	$\mu\text{A}$
<b><math>\overline{\text{VCC}}_{\text{LO}}</math></b>						
$V_{\text{OL}}$	Output low voltage	$V_{\text{CC}} = 2 \text{ V}$ , $I_{\text{SINK}} = 1 \text{ mA}$ , $\overline{\text{VCC}}_{\text{LO}}$ asserted			0.3	V
	$\overline{\text{VCC}}_{\text{LO}}$ leakage current	$V_{\overline{\text{VCC}}_{\text{LO}}} = 3 \text{ V}$ , $\overline{\text{VCC}}_{\text{LO}}$ open drain	-0.1		+0.1	$\mu\text{A}$
<b><math>\text{PS}_{\text{HOLD}}</math></b>						
$V_{\text{IL}}$	Input low voltage	$V_{\text{CC}} \geq 2.0 \text{ V}$			0.99	V
$V_{\text{IH}}$	Input high voltage	$V_{\text{CC}} \geq 2.0 \text{ V}$	1.05			V
	Glitch immunity		1	80		$\mu\text{s}$
	$\text{PS}_{\text{HOLD}}$ leakage current	$V_{\text{PSHOLD}} = 0.6 \text{ V}$	-0.1		0.1	$\mu\text{A}$
	$\text{PS}_{\text{HOLD}}$ to enable propagation delay				30	$\mu\text{s}$
$R_{\text{PSHOLD}}$	Pull-down resistor connected internally during power-up	$V_{\text{PSHOLD}} = 5.5 \text{ V}$	195	300	405	k $\Omega$



Table 5. DC and AC characteristics (continued)

Symbol	Parameter	Test condition <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
<b>C<sub>SRD</sub></b>						
I <sub>SRD</sub>	C <sub>SRD</sub> charging current		100	150	200	nA
V <sub>SRD</sub>	C <sub>SRD</sub> voltage threshold	V <sub>CC</sub> = 3.6 V, load on V <sub>REF</sub> pin 100 kΩ and mandatory 1 μF capacitor, T <sub>A</sub> = 25 °C		1.5		V
t <sub>SRD</sub>	Additional Smart Reset™ delay time	External C <sub>SRD</sub> connected		10		s/μF
<b>EN, <math>\overline{\text{EN}}</math></b>						
V <sub>OL</sub>	Output low voltage	V <sub>CC</sub> = 2 V, I <sub>SINK</sub> = 1 mA, enable asserted			0.3	V
V <sub>OH</sub> <sup>(5)</sup>	Output high voltage	V <sub>CC</sub> = 2 V, I <sub>SOURCE</sub> = 1 mA, enable asserted	V <sub>CC</sub> – 0.3			V
t <sub>EN_OFF</sub> <sup>(6)</sup>	enable off to enable on	V <sub>CC</sub> ≥ 2.0 V	40	64	88	ms
	EN, $\overline{\text{EN}}$ leakage current	V <sub>EN</sub> = 2 V, enable open drain	–0.1		+0.1	μA
<b>RST</b>						
V <sub>OL</sub>	Output low voltage	V <sub>CC</sub> = 2 V, I <sub>SINK</sub> = 1 mA, RST asserted			0.3	V
t <sub>REC</sub>	RST pulse width	V <sub>CC</sub> ≥ 2.0 V	240	360	480	ms
	RST leakage current	V <sub>RST</sub> = 3 V	–0.1		+0.1	μA
<b><math>\overline{\text{INT}}</math></b>						
V <sub>OL</sub>	Output low voltage	V <sub>CC</sub> = 2 V, I <sub>SINK</sub> = 1 mA, $\overline{\text{INT}}$ asserted			0.3	V
t <sub>INT_Min</sub>	Minimum $\overline{\text{INT}}$ pulse width	V <sub>CC</sub> ≥ 2.0 V	20	32	44	ms
	$\overline{\text{INT}}$ leakage current	V <sub>INT</sub> = 3 V	–0.1		+0.1	μA
<b>V<sub>REF</sub></b>						
V <sub>REF</sub>	1.5 V voltage reference	V <sub>CC</sub> = 3.6 V, load on V <sub>REF</sub> pin 100 kΩ and mandatory 1 μF capacitor, T <sub>A</sub> = 25 °C	1.485 –1%	1.5	1.515 +1%	V

1. Valid for ambient operating temperature: T<sub>A</sub> = –40 to 85 °C; V<sub>CC</sub> = 1.6 V to 5.5 V (except where noted).
2. Typical values are at T<sub>A</sub> = +25 °C.
3. This blanking time allows the processor to start up correctly (see [Figure 7, 8, 9, 10, 11, 12](#)).
4. The internal pull-up resistor connected to the  $\overline{\text{SR}}$  input is optional (see [Table 10](#) for detailed device options).
5. Valid for push-pull only.
6. Minimal delay between enable off and enable on allows the application to power down properly.  $\overline{\text{PB}}$  is ignored during this period.

## 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 41. TDFN12 (2 x 3 mm) package outline

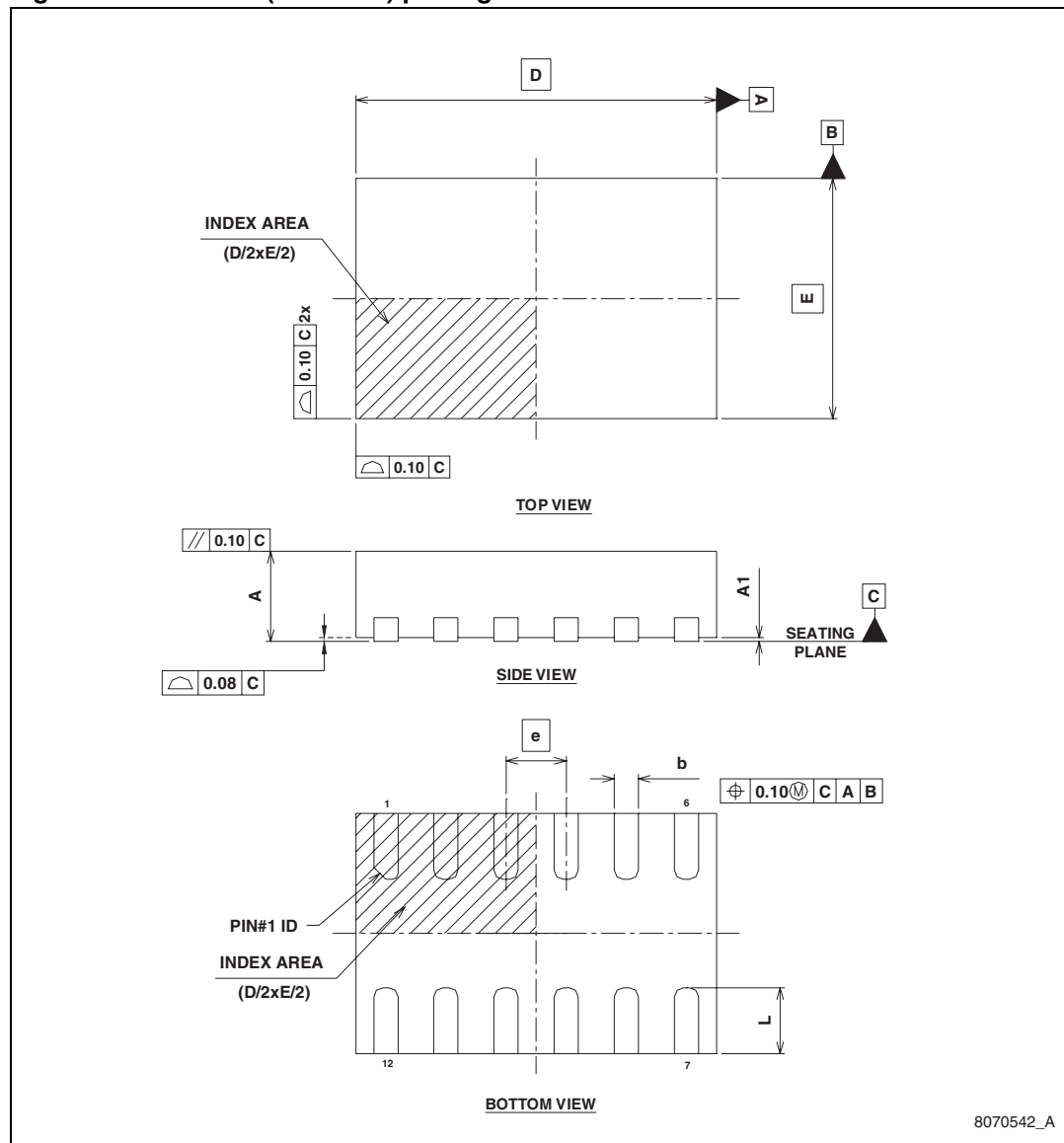
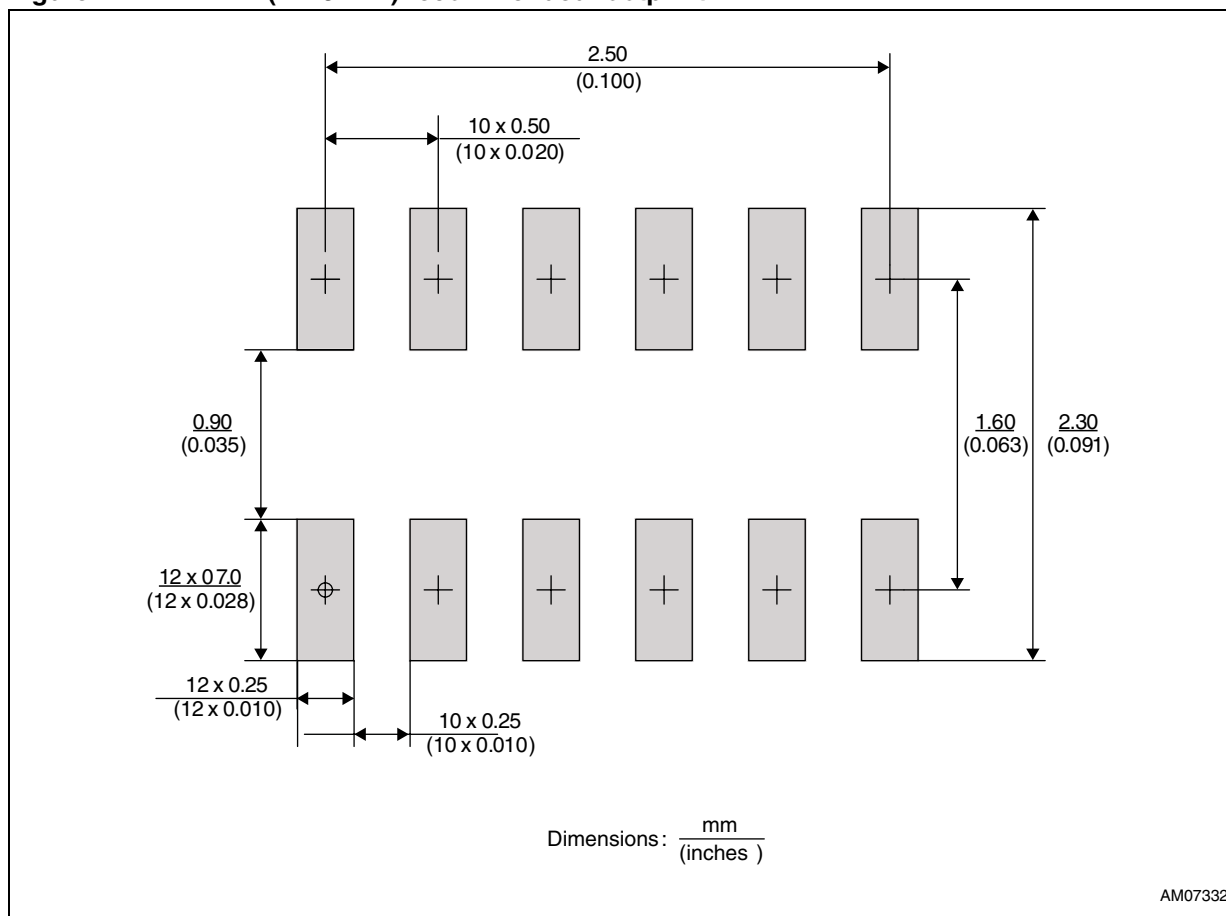


Table 6. TDFN12 (2 x 3 mm) package mechanical data

Symbol	mm			inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D		3.00 BSC			0.118	
E		2.00 BSC			0.079	
e		0.50			0.020	
L	0.45	0.55	0.65	0.018	0.022	0.026

**Figure 42. TDFN12 (2 x 3 mm) recommended footprint**

**Note:** Drawing not to scale.

Figure 43. Carrier tape for TDFN12 (2 mm x 3 mm) package

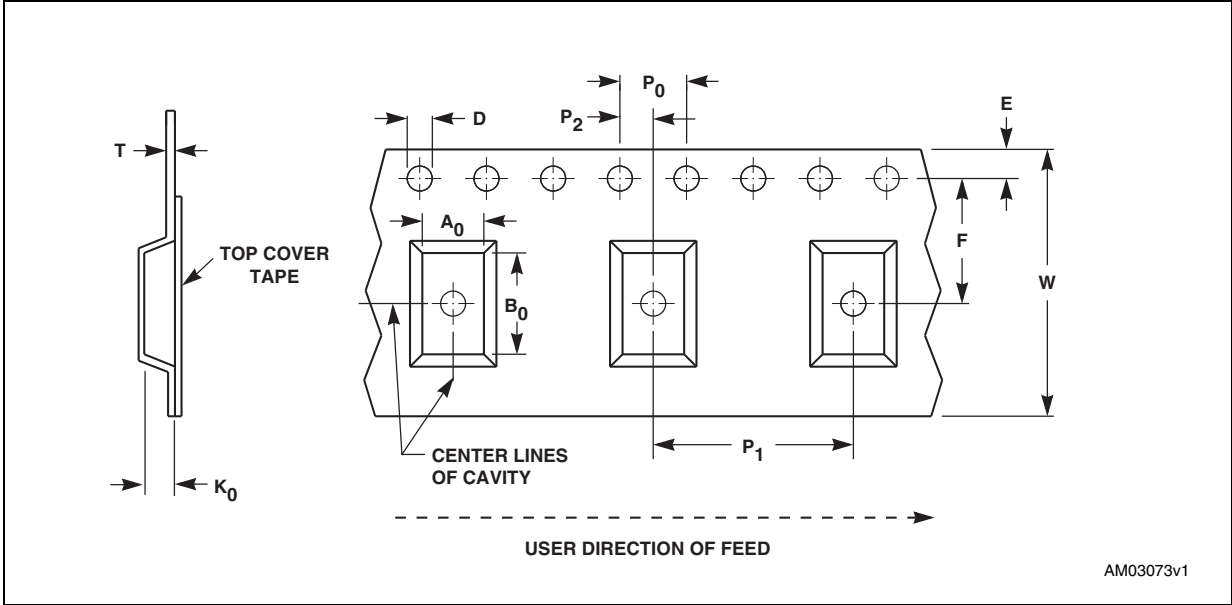


Table 7. Carrier tape dimensions for TDFN12 (2 mm x 3 mm) package

Package	W	D	E	P <sub>0</sub>	P <sub>2</sub>	F	A <sub>0</sub>	B <sub>0</sub>	K <sub>0</sub>	P <sub>1</sub>	T	Unit	Bulk Qty.
TDFN12	12.00 ±0.30	1.50 +0.10/ -0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	5.50 ±0.05	2.30 ±0.10	3.20 ±0.10	1.10 ±0.01	4.00 ±0.10	0.30 ±0.05	mm	3000

## 9 Part numbering

**Table 8. STM6600 ordering information scheme**

Example:	STM660	0	F	Q	2	4	DM	6	F
<b>Device type</b>									
STM660									
<b>Startup process</b>									
0: $\overline{PB}$ must be held low until the $PS_{HOLD}$ confirmation									
<b>Input and output types<sup>(1)</sup></b>									
A: active high EN output, long push asserts $\overline{RST}$ , pull-up on $\overline{SR}$									
E: active high EN output, long push asserts $\overline{RST}$ , no resistor on $\overline{SR}$									
F: active low $\overline{EN}$ output, long push asserts $\overline{RST}$ , no resistor on $\overline{SR}$									
G: active high EN output, long push deasserts EN, no resistor on $\overline{SR}$									
H: active low $\overline{EN}$ output, long push deasserts $\overline{EN}$ , no resistor on $\overline{SR}$									
<b><math>V_{TH+}</math> threshold voltage<sup>(1)</sup></b>									
A: 2.50 V									
Q: 3.30 V									
S: 3.40 V									
U: 3.50 V									
<b><math>V_{HYST}</math> voltage hysteresis<sup>(1)</sup></b>									
2: 200 mV									
5: 500 mV									
<b><math>t_{ON\_BLANK}</math> blanking period<sup>(1)</sup></b>									
2: 1.4 s (min.)									
4: 5.6 s (min.)									
5: 11.2 s (min.)									
<b>Package</b>									
DM: TDFN12									
<b>Temperature range</b>									
6: -40 °C to +85 °C									
<b>Shipping method</b>									
E: ECOPACK <sup>®</sup> package, tubes									
F: ECOPACK <sup>®</sup> package, tape and reel									

1. Other options are offered. Minimum order quantities may apply. Please contact local ST sales office for availability.

**Table 9. STM6601 ordering information scheme**

Example:	STM660	1	G	U	2	B	DM	6	F
<b>Device type</b>									
STM660									
<b>Startup process</b>									
1: $\overline{PB}$ can be released before the $PS_{HOLD}$ confirmation									
<b>Input and output types<sup>(1)</sup></b>									
A: active high EN output, long push asserts $\overline{RST}$ , pull-up on $\overline{SR}$									
B: active low $\overline{EN}$ output, long push asserts $\overline{RST}$ , pull-up on $\overline{SR}$									
C: active high EN output, long push deasserts EN, pull-up on $\overline{SR}$									
D: active low $\overline{EN}$ output, long push deasserts $\overline{EN}$ , pull-up on $\overline{SR}$									
G: active high EN output, long push deasserts EN, no resistor on $\overline{SR}$									
<b><math>V_{TH+}</math> threshold voltage<sup>(1)</sup></b>									
M: 3.10 V									
Q: 3.30 V									
S: 3.40 V									
U: 3.50 V									
<b><math>V_{HYST}</math> voltage hysteresis<sup>(1)</sup></b>									
2: 200 mV									
<b><math>t_{ON\_BLANK}</math> blanking period<sup>(1)</sup></b>									
B: 1.4 s (min.)									
D: 5.6 s (min.)									
<b>Package</b>									
DM: TDFN12									
<b>Temperature range</b>									
6: -40 °C to +85 °C									
<b>Shipping method</b>									
E: ECOPACK® package, tubes									
F: ECOPACK® package, tape and reel									

1. Other options are offered. Minimum order quantities may apply. Please contact local ST sales office for availability.

## 10 Product selector

Table 10. STM6600 product selector

Full part number	EN or $\overline{\text{EN}}$ <sup>(1)</sup>	After long push <sup>(2)</sup>	Internal resistor on $\overline{\text{SR}}$ input	Power-on lockout voltage $V_{\text{TH+}}$ (V)	Forced power-off voltage $V_{\text{TH-}}$ (V)	$t_{\text{ON\_BLANK}}$ (s) at startup (min.)	$t_{\text{ON\_BLANK}}$ (s) at reset (min.)	Top marking <sup>(3)</sup>
STM6600AS24DM6F	EN	$\overline{\text{RST}}$	pull-up	3.40	3.20	5.6	5.6	pyww AS24
STM6600ES24DM6F <sup>(4)</sup>	EN	$\overline{\text{RST}}$	—	3.40	3.20	5.6	5.6	pyww ES24
STM6600FQ24DM6F <sup>(4)</sup>	$\overline{\text{EN}}$	$\overline{\text{RST}}$	—	3.30	3.10	5.6	5.6	pyww FQ24
STM6600GS22DM6F <sup>(4)</sup>	EN	EN	—	3.40	3.20	1.4	—	pyww GS22
STM6600GS25DM6F <sup>(4)</sup>	EN	EN	—	3.40	3.20	11.2	—	pyww GS25
STM6600GU22DM6F <sup>(4)</sup>	EN	EN	—	3.50	3.30	1.4	—	pyww GU22
STM6600HA55DM6F <sup>(4)</sup>	$\overline{\text{EN}}$	$\overline{\text{EN}}$	—	2.50	2.00	11.2	—	pyww HA55
STM6600HQ25DM6F <sup>(4)</sup>	$\overline{\text{EN}}$	$\overline{\text{EN}}$	—	3.30	3.10	11.2	—	pyww HQ25
STM6600HU25DM6F <sup>(4)</sup>	$\overline{\text{EN}}$	$\overline{\text{EN}}$	—	3.50	3.30	11.2	—	pyww HU25

1. EN (or  $\overline{\text{EN}}$ ) output is push-pull.  $\overline{\text{RST}}$ ,  $\overline{\text{INT}}$ ,  $\overline{\text{PB}}_{\text{OUT}}$  and  $\overline{\text{VCC}}_{\text{LO}}$  outputs are open drain.

2. After  $t_{\text{SRD}}$  expires through long push, either device reset ( $\overline{\text{RST}}$ ) will be activated for  $t_{\text{REC}}$  (240 ms min.) or the EN (or  $\overline{\text{EN}}$ ) pin will be deasserted. The additional Smart Reset™ delay time,  $t_{\text{SRD}}$ , can be adjusted by the user at 10 s/μF (typ.) by connecting the external capacitor to the  $\text{C}_{\text{SRD}}$  pin.

3. Where “p” = assembly plant, “y” = assembly year (0 to 9) and “ww” = assembly work week (01 to 52).

4. Please contact local ST sales office for availability.



Table 11. STM6601 product selector

Full part number	EN or $\overline{\text{EN}}$ <sup>(1)</sup>	After long push <sup>(2)</sup>	Internal resistor on $\overline{\text{SR}}$ input	Power-on lockout voltage $V_{\text{TH}+}$ (V)	Forced power-off voltage $V_{\text{TH}-}$ (V)	$t_{\text{ON\_BLANK}}$ (s) at startup (min.)	$t_{\text{ON\_BLANK}}$ (s) at reset (min.)	Top marking <sup>(3)</sup>
STM6601AQ2BDM6F	EN	$\overline{\text{RST}}$	pull-up	3.30	3.10	1.4	1.4	pyww AQ2B
STM6601AU2DDM6F	EN	$\overline{\text{RST}}$	pull-up	3.50	3.30	5.6	5.6	pyww AU2D
STM6601BM2DDM6F	$\overline{\text{EN}}$	$\overline{\text{RST}}$	pull-up	3.10	2.90	5.6	5.6	pyww BM2D
STM6601BS2BDM6F	$\overline{\text{EN}}$	$\overline{\text{RST}}$	pull-up	3.40	3.20	1.4	1.4	pyww BS2B
STM6601CM2DDM6F	EN	EN	pull-up	3.10	2.90	5.6	—	pyww CM2D
STM6601CQ2BDM6F	EN	EN	pull-up	3.30	3.10	1.4	—	pyww CQ2B
STM6601DS2BDM6F	$\overline{\text{EN}}$	$\overline{\text{EN}}$	pull-up	3.40	3.20	1.4	—	pyww DS2B
STM6601GU2BDM6F <sup>(4)</sup>	EN	$\overline{\text{RST}}$	—	3.50	3.30	5.6	5.6	pyww GU2B

1. EN (or  $\overline{\text{EN}}$ ) output is push-pull.  $\overline{\text{RST}}$ ,  $\overline{\text{INT}}$ ,  $\overline{\text{PB}}_{\text{OUT}}$  and  $\overline{\text{VCC}}_{\text{LO}}$  outputs are open drain.
2. After  $t_{\text{SRD}}$  expires through long push, either device reset ( $\overline{\text{RST}}$ ) will be activated for  $t_{\text{REC}}$  (240 ms min.) or the EN (or  $\overline{\text{EN}}$ ) pin will be deasserted. The additional Smart Reset™ delay time,  $t_{\text{SRD}}$ , can be adjusted by the user at 10 s/μF (typ.) by connecting the external capacitor to the  $\text{C}_{\text{SRD}}$  pin.
3. Where “p” = assembly plant, “y” = assembly year (0 to 9) and “ww” = assembly work week (01 to 52).
4. Please contact local ST sales office for availability.

## 11 Revision history

**Table 12. Document revision history**

Date	Revision	Changes
04-Mar-2009	1	Initial release.
05-Jun-2009	2	Updated text in <a href="#">Section 2</a> , <a href="#">Section 3</a> , <a href="#">Figure 11</a> , <a href="#">12</a> ; updated <a href="#">Figure 1</a> , <a href="#">7</a> , <a href="#">9</a> , <a href="#">14</a> , <a href="#">18</a> , <a href="#">19</a> , <a href="#">43</a> , <a href="#">Table 3</a> , <a href="#">5</a> , <a href="#">8</a> , <a href="#">9</a> , <a href="#">10</a> ; added <a href="#">Figure 8</a> , <a href="#">10</a> , <a href="#">Table 7</a> ; reformatted document.
23-Jul-2009	3	Updated text in <a href="#">Features</a> , <a href="#">Table 1</a> , <a href="#">8</a> , <a href="#">9</a> , and <a href="#">10</a> ; reformatted document.
22-Oct-2009	4	Updated <a href="#">Section 2</a> , <a href="#">Table 5</a> , <a href="#">Table 10</a> , <a href="#">Figure 1</a> , <a href="#">7</a> , <a href="#">8</a> , <a href="#">9</a> , <a href="#">10</a> , <a href="#">11</a> , <a href="#">12</a> , <a href="#">14</a> , <a href="#">18</a> , title of <a href="#">Section 10</a> ; added <a href="#">Section 5: Typical operating characteristics</a> ( <a href="#">Figure 23</a> through <a href="#">40</a> ); document status upgraded to full datasheet.
25-Jan-2010	5	Updated <a href="#">Figure 6</a> , <a href="#">Section 2</a> , <a href="#">Table 5</a> ; textual update to “Smart Reset™”.
13-Apr-2010	6	Updated <a href="#">Figure 1</a> , <a href="#">6</a> , <a href="#">7</a> , <a href="#">8</a> , <a href="#">9</a> , <a href="#">10</a> , <a href="#">11</a> , <a href="#">12</a> , <a href="#">13</a> , <a href="#">Section 2</a> , <a href="#">Section 3</a> , <a href="#">Table 3</a> , <a href="#">5</a> , <a href="#">8</a> , <a href="#">9</a> , <a href="#">10</a> .
07-Jun-2010	7	Reformatted <a href="#">Figure 1</a> and <a href="#">Figure 42</a> , corrected typo in <a href="#">Section 3</a> , added option A to <a href="#">Table 8</a> , updated <a href="#">Table 10</a> and separated <a href="#">Table 10</a> to <a href="#">Table 10</a> and <a href="#">Table 11</a> .

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