

Silicon NPN Power Transistors

2SD546

DESCRIPTION

- With TO-66 package
- High breakdown voltage

APPLICATIONS

- Converters
- Inverters
- Switching regulators

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector



Fig.1 simplified outline (TO-66) and symbol

Absolute maximum ratings($T_a = \square$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	800	V
V_{CEO}	Collector-emitter voltage	Open base	500	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		1	A
P_C	Collector power dissipation	$T_C = 25 \square$	30	W
T_j	Junction temperature		150	$\square$
T_{stg}	Storage temperature		-55~150	$\square$

Silicon NPN Power Transistors

2SD546

CHARACTERISTICS

T_j=25℃ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEQ(SUS)}	Collector-emitter sustaining voltage	I _C =30mA ; I _B =0	500			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA ; I _C =0	6			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =500mA; I _B =100mA			1.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =500mA; I _B =100mA			1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =800V; I _E =0			0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =6V; I _C =0			0.1	mA
h _{FE}	DC current gain	I _C =20mA ; V _{CE} =10V	40		200	
f _T	Transition frequency	I _C =0.1A ; V _{CE} =10V		7		MHz

Silicon NPN Power Transistors

2SD546

PACKAGE OUTLINE

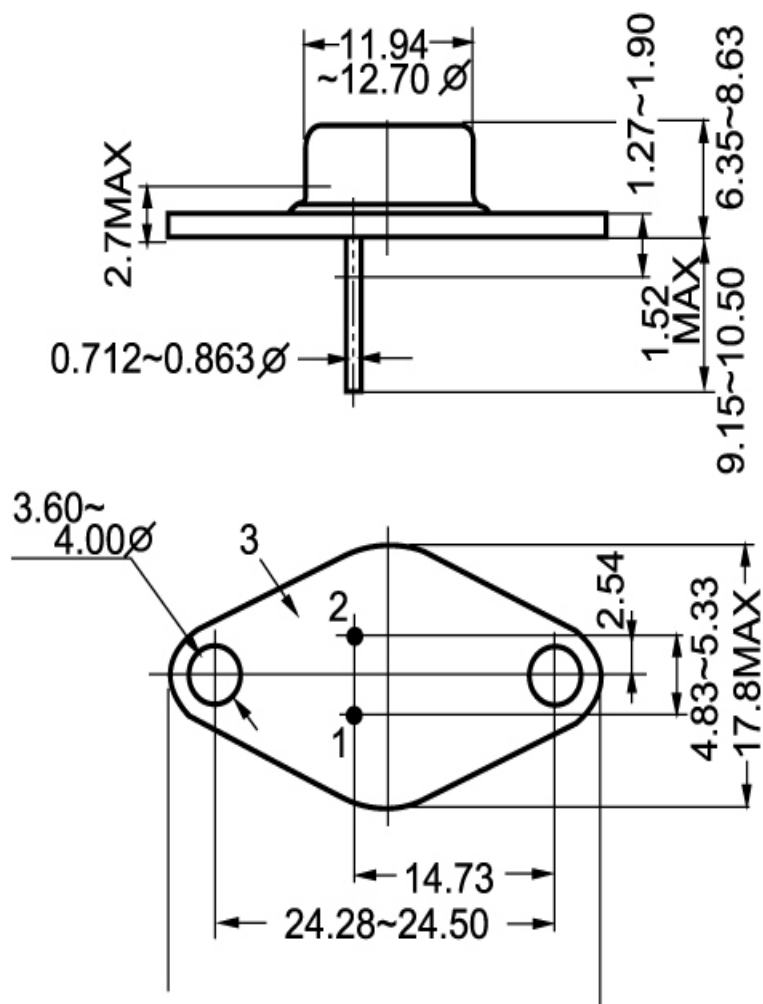


Fig.2 outline dimensions