ML87V2105 Preliminary

Video Signal Noise Reduction IC with a Built-in 5.6 Mbit Frame Memory

This document contains minimum specifications. For full specifications, please contact your nearest Oki office or representative.

GENERAL DESCRIPTION

The ML87V2105 comprises a 5.6 Mbit frame memory, a noise reduction filter, and a memory controller to reduce frame-recursive 3D noise in video signals.
The motion adaptive noise reduction is performed between frames, between fields, or between lines, to reduce the afterimage particular to 3D noise reduction as far as possible, while achieving effective noise reduction.
The ML87V2105 also features an automatic noise reduction mode that automatically detects the noise level in the input video data to set the optimum noise reduction.
Because it is possible to select the same format for output as for input, the ML87V2105 can be introduced into an existing system, making it easy to achieve noise reduction.

FEATURES

- Built-in memory:
  Frame memory (4:1:1 data equivalent) × 1 unit
- Maximum input and output operating frequencies (16 bits/8 bits, ITU-R BT.656):
  14.75/29.5 MHz
- Power supply voltage:
  3.3 V ± 0.3 V
- Input pin:
  LVTTL (3.3 V)
- Output pin:
  LVCMOS (3.3 V)
- Input data format:

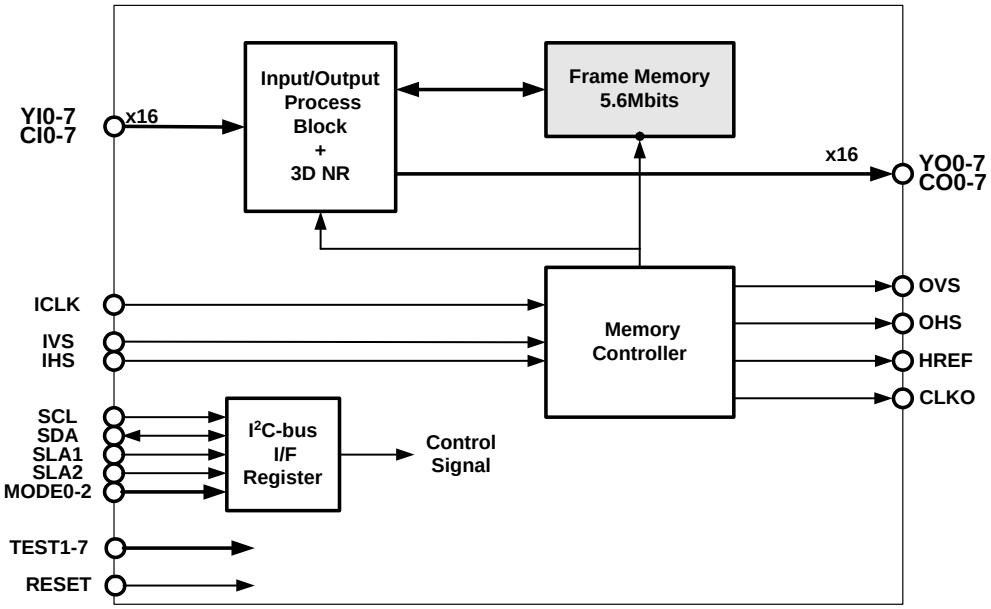
YCbCr (8 bits (Y) + 8 bits (CbCr) (4:2:2) + Sync.):	16-bit mode
YCbCr (8 bits (YCbCr) (4:2:2) + Sync.):	8-bit mode
ITU-R BT.656 (8 bits (YCbCr)):	ITU-R BT.656 mode

- Output data format:

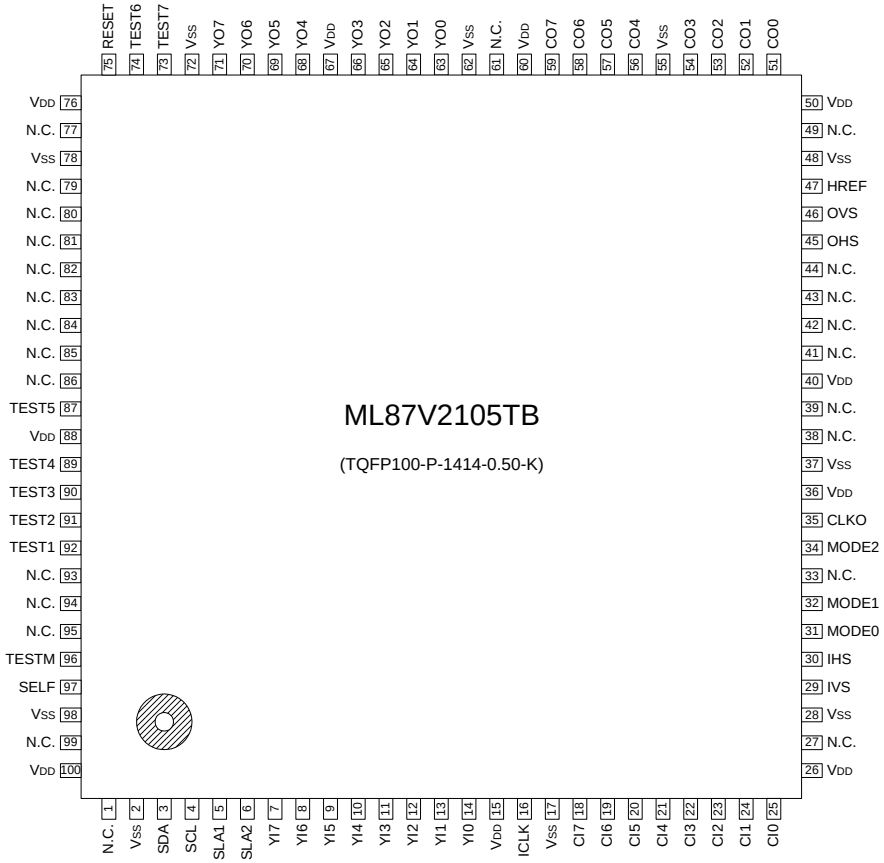
YCbCr (8 bits (Y) + 8 bits (CbCr) (4:2:2) + Sync.):	16-bit mode
YCbCr (8 bits (YCbCr) (4:2:2) + Sync.):	8-bit mode (Selectable in 8-bit input mode)
ITU-R BT.656 (8 bits (YCbCr)):	ITU-R BT.656 mode (Selectable in input ITU-R BT.656)

- Serial bus:
  I^2C-bus interface: (Standard mode: 100 kbps/Fast mode: 400 kbps)
- Internal memory controller:
  Compatible with 625/50 Hz 2:1, 525/60 Hz 2:1
  Compatible horizontal effective pixels: 640 (525 line mode only), 720, 768
- Frame-recursive noise reduction:
  Frame-recursive noise detection and subtraction
  Auto mode noise reduction
- Package:
  100 pin TQFP (TQFP100-P-1414-0.50-K)(ML87V2105TB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTIONS

No.	Symbol	I/O	Pad Remarks	Pin Description
1	N.C.	—		Unused pin
2	V_{SS}	—		Ground
3	SDA	I/O	Schmitt(IN)/ OpenDrain(OUT)	I^2C-bus data pin
4	SCL	I	Schmitt	I^2C-bus clock pin
5	SLA1	I	Internal pull-down 50k	Slave address setting pin
6	SLA2	I	Internal pull-down 50k	Slave address setting pin
7	YI7	I		Luminance signal input pin bit 7 (MSB)
8	YI6	I		Luminance signal input pin bit 6
9	YI5	I		Luminance signal input pin bit 5
10	YI4	I		Luminance signal input pin bit 4
11	YI3	I		Luminance signal input pin bit 3
12	YI2	I		Luminance signal input pin bit 2
13	YI1	I		Luminance signal input pin bit 1
14	YI0	I		Luminance signal input pin bit 0 (LSB)
15	V_{DD}	—		Power supply 3.3 V
16	ICLK	I		Input system clock pin
17	V_{SS}	—		Ground
18	CI7	I	Internal pull-down 50k	Color difference signal input pin bit 7 (MSB)
19	CI6	I	Internal pull-down 50k	Color difference signal input pin bit 6
20	CI5	I	Internal pull-down 50k	Color difference signal input pin bit 5
21	CI4	I	Internal pull-down 50k	Color difference signal input pin bit 4
22	CI3	I	Internal pull-down 50k	Color difference signal input pin bit 3
23	CI2	I	Internal pull-down 50k	Color difference signal input pin bit 2
24	CI1	I	Internal pull-down 50k	Color difference signal input pin bit 1
25	CI0	I	Internal pull-down 50k	Color difference signal input pin bit 0 (LSB)
26	V_{DD}	—		Power supply 3.3 V
27	N.C.	—		Unused pin
28	V_{SS}	—		Ground
29	IVS	I	Schmitt Internal pull-down 50k	Input system vertical sync signal input pin
30	IHS	I	Schmitt Internal pull-down 50k	Input system horizontal sync signal input pin
31	MODE0	I	Internal pull-down 50k	Mode setting pin – bit 0
32	MODE1	I	Internal pull-down 50k	Mode setting pin – bit 1
33	N.C.	—		Unused pin
34	MODE2	I	Internal pull-down 50k	Mode setting pin – bit 2
35	CLKO	O/(I)		Clock output (I^2C-bus control possible)
36	V_{DD}	—		Power supply 3.3 V
37	V_{SS}	—		Ground
38	N.C.	—		Unused pin
39	N.C.	—		Unused pin

No.	Symbol	I/O	Pad Remarks	Pin Description
40	V_{DD}	—		Power supply 3.3 V
41	N.C.	—		Unused pin
42	N.C.	—		Unused pin
43	N.C.	—		Unused pin
44	N.C.	—		Unused pin
45	OHS	O		Horizontal sync signal output pin
46	OVS	O		Vertical sync signal output pin
47	HREF	O		Data output horizontal reference signal output pin
48	V_{SS}	—		Ground
49	N.C.	—		Unused pin
50	V_{DD}	—		Power supply 3.3 V
51	CO0	O/(I)		Color difference signal output pin – bit 0 (LSB)
52	CO1	O/(I)		Color difference signal output pin – bit 1
53	CO2	O/(I)		Color difference signal output pin – bit 2
54	CO3	O/(I)		Color difference signal output pin – bit 3
55	V_{SS}	—		Ground
56	CO4	O/(I)		Color difference signal output pin – bit 4
57	CO5	O/(I)		Color difference signal output pin – bit 5
58	CO6	O/(I)		Color difference signal output pin – bit 6
59	CO7	O/(I)		Color difference signal output pin – bit 7(MSB)
60	V_{DD}	—		Power supply 3.3 V
61	N.C.	—		Unused pin
62	V_{SS}	—		Ground
63	YO0	O		Luminance signal output pin – bit 0 (LSB)
64	YO1	O		Luminance signal output pin – bit 1
65	YO2	O		Luminance signal output pin – bit 2
66	YO3	O		Luminance signal output pin – bit 3
67	V_{DD}	—		Power supply 3.3 V
68	YO4	O		Luminance signal output pin – bit 4
69	YO5	O		Luminance signal output pin – bit 5
70	YO6	O		Luminance signal output pin – bit 6
71	YO7	O		Luminance signal output pin – bit 7 (MSB)
72	V_{SS}	—		Ground
73	TEST7	I		Test input pin – bit 7 (1: test mode)
74	TEST6	I		Test input pin – bit 6 (1: test mode)
75	RESET	I	Schmitt	System reset/input pin 0: System reset 1: Operation

No.	Symbol	I/O	Pad Remarks	Pin Description
76	V_{DD}	—		Power supply 3.3 V
77	N.C.	—		Unused pin
78	V_{SS}	—		Ground
79	N.C.	—		Unused pin
80	N.C.	—		Unused pin
81	N.C.	—		Unused pin
82	N.C.	—		Unused pin
83	N.C.	—		Unused pin
84	N.C.	—		Unused pin
85	N.C.	—		Unused pin
86	N.C.	—		Unused pin
87	TEST5	I	Internal pull-down 50k	Test input pin – bit 5 (1: test mode)
88	V_{DD}	—		Power supply 3.3 V
89	TEST4	I	Internal pull-down 50k	Test input pin – bit 4 (1: test mode)
90	TEST3	I	Internal pull-down 50k	Test input pin – bit 3 (1: test mode)
91	TEST2	I	Internal pull-down 50k	Test input pin – bit 2 (1: test mode)
92	TEST1	I	Internal pull-down 50k	Test input pin – bit 1 (1: test mode)
93	N.C.	—		Unused pin
94	N.C.	—		Unused pin
95	N.C.	—		Unused pin
96	TESTM	I	Internal pull-down 50k	Memory test input pin (1: test mode)
97	SELF	I	Internal pull-down 50k	Self refresh setting pin (0: Self refresh stopped, 1: Self refresh operated)
98	V_{SS}	—		Ground

Notes: Keep the test mode pins fixed to 0 or leave them open.
CL0 to CL7 and CLK0 are configured as inputs only in the test mode.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to + 4.6	V
Input pin voltage	V_I	Ta = 25°C	–0.3 to + 7.0	V
Output pin short-circuit current	I_{OS}	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	T_{opr}	—	0 to 70	°C
Storage temperature	T_{stg}	—	–50 to + 150	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.0	3.3	3.6	V
Power supply voltage	V_{SS}	0	0	0	V
Operating temperature	Ta	0	—	70	°C

Pin Capacitance

(V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz, Ta = 25°C)

Parameter	Symbol	Min.	Max.	Unit
Input capacitance	C_i	—	5	pF
Input/output capacitance (CO0 to CO7, CLK0)	C_{io1}	—	10	pF
Input/output capacitance (SDA)	C_{io2}	—	10	pF
Output capacitance (YO0 to YO7, OVS, OHS, HREF)	C_o	—	10	pF

DC Characteristics

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
H level input voltage	V_{IH}	—	2.0	V_{DD}+0.3	V
L level input voltage	V_{IL}	—	–0.3	0.8	V
Schmitt trigger threshold voltage (SDA, SCL, IVS, IHS, RESET)	V_{t+}	—	—	2.0	V
Schmitt trigger threshold voltage (SDA, SCL, IVS, IHS, RESET)	V_{t-}	—	0.8	—	V
Hysteresis voltage width	V_h	—	0.1	—	V
H level input current (pull-down)	I_{IH}	50 kΩ Pull Down	20	200	μA
Input leakage current	I_{IL}	TTL	–10	10	μA
H level output voltage (other than SDA)	V_{OH}	I_{OH} = –4 mA	2.4	V_{DD}	V
L level output voltage (other than SDA)	V_{OL}	I_{OL} = 4 mA	0	0.4	V
L level output voltage (N-Ch.OD) (SDA)	V_{OOL}	I_{OL} = 4 mA	0	0.4	V
Output leakage current	I_{OL}	$0 \le V_{out} \le V_{DD}$ Output disabled	–10	10	μA
Supply current (during operation)	I_{DD1}	ICLK: 29.5 MHz Output disabled	—	80	mA
Supply current (during standby)	I_{DD2}	Input pin = V_{IL}	—	5	mA

AC Characteristics

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
ICLK clock cycle time	t_{ICLK}	16-bit input mode	66	—	ns
ICLK clock cycle time	t_{ICLK}	8-bit input mode ITU-R BT.656 mode	33	—	ns
ICLK clock duty ratio	dt_{ICLK}	—	40	60	%
ICLK input set-up time	t_{IISU}	—	5	—	ns
ICLK input hold time	t_{IIH}	—	3	—	ns
ICLK output delay time	t_{IOD}	C_L = 30 pF	5	25	ns
CLKO delay time	t_{CKD}	C_L = 30 pF (IICLK output)	2	25	ns
		C_L = 30 pF (ICLK output)	2	25	ns
Data through time	t_{DIDO}	C_L = 30 pF	5	20	ns

*1: ( ) indicates the input internal system clock cycle.

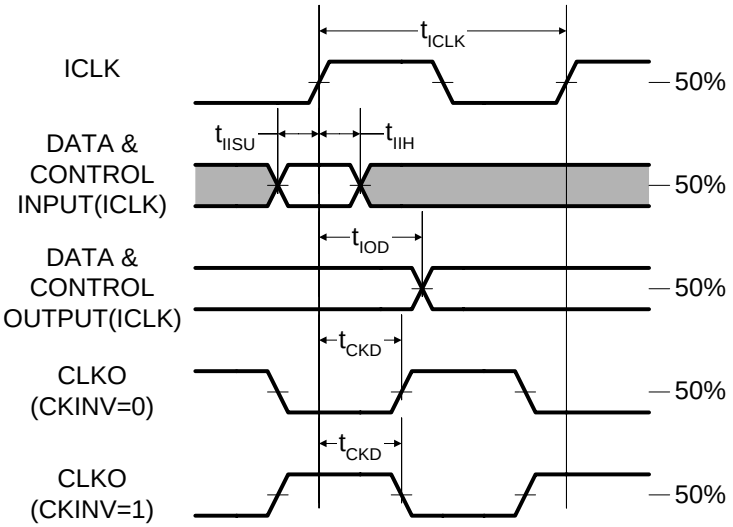
Note 1: Measurement conditions
Output comparison level: V_{OH} = 1.5 V, V_{OL} = 1.5 V
Input voltage level: V_{IH} = 3.0 V, V_{IL} = 0.0 V

Note 2: .When writing input data to the memory, compensation is applied from the second input system vertical synchronization signal when V_{DD} reaches 3.0 V after the power is turned on, and when RESET = 1. (Due to memory initialization, the first data for the first field is not compensated.)

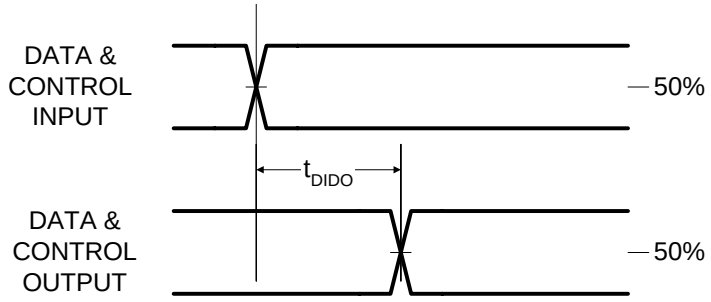
Note 3: .When reading output data from the memory, compensation is applied from the second output system vertical synchronization signal when V_{DD} reaches 3.0 V after the power is turned on, and when RESET = 1. (Due to memory initialization, the first data for the first field is not compensated.)

INPUT/OUTPUT TIMING

1. ICLK input/output timing



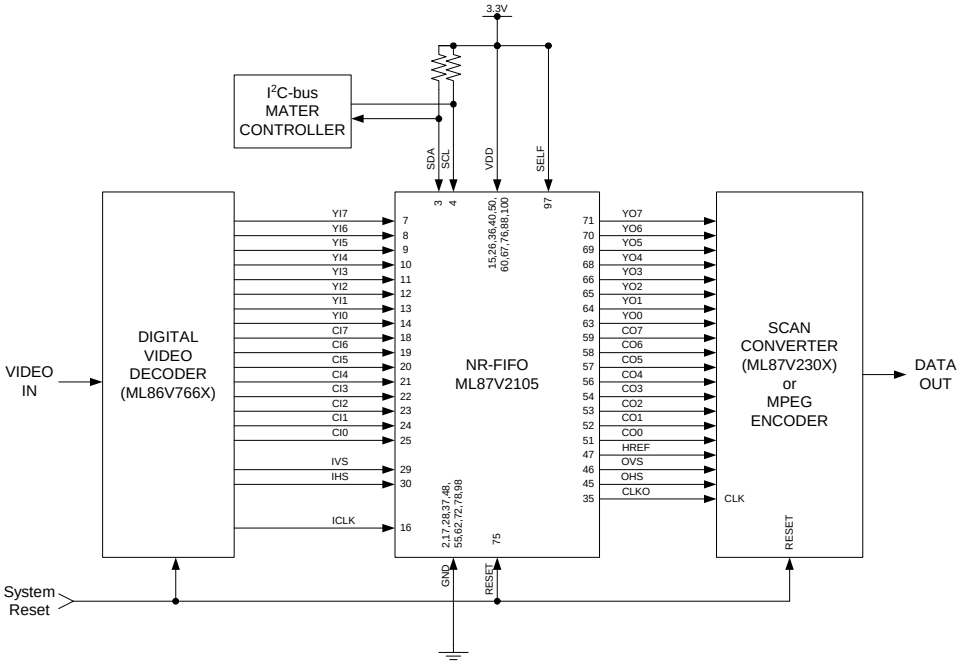
2. Data through mode input/output timing



CIRCUIT APPLICATION EXAMPLES

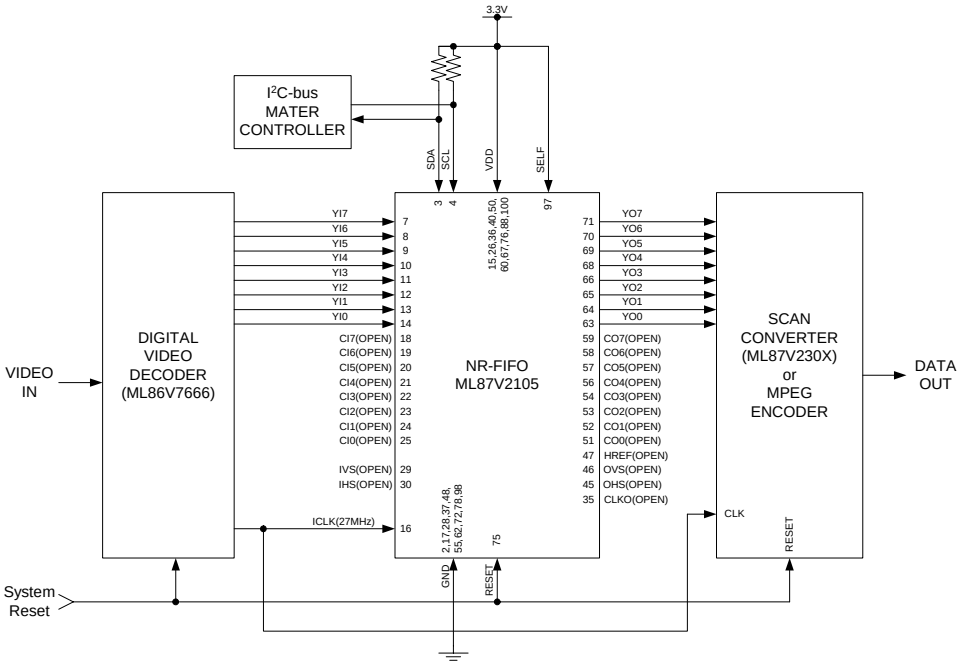
Application Example 1

Mode setting: Open
Slave address: 1011100
Input format: 16-bit YCbCr (Register setting: DISEL = 0, R656 = 0)



Application Example 2

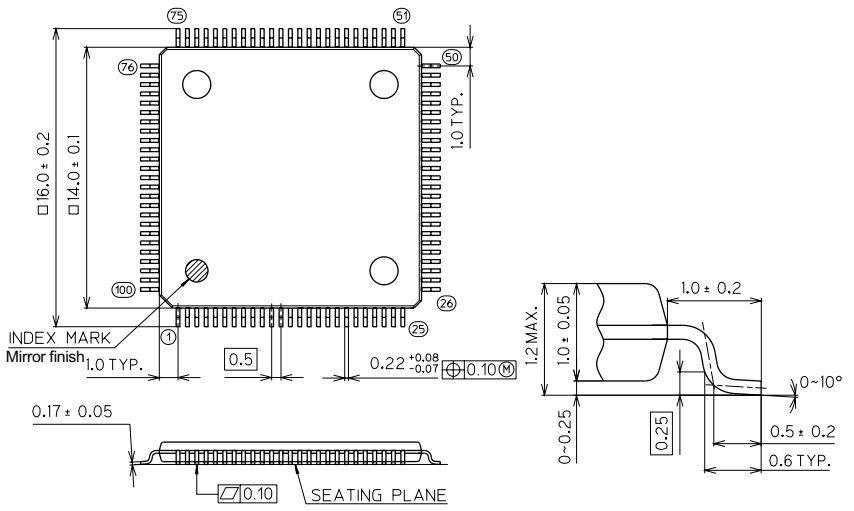
Mode setting: Open
Slave address: 1011100
Input format: ITU-R BT656 (Register setting: DISEL = 0, R656 = 1)



PACKAGE DIMENSIONS

(Unit: mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

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Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL87V2105DIGEST-01	Oct.20,2003	–	14	Preliminary edition 1
PEDL87V2105DIGEST-02	Dec.20,2003	14	14	Internal pull down, application schematic

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