

**12P10**

Preliminary

Power MOSFET**100V P-CHANNEL MOSFET**

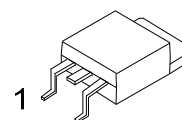
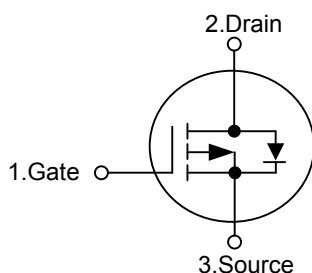
■ DESCRIPTION

The **12P10** uses advanced proprietary, planar stripe, DMOS technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable to be used in low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

■ FEATURES

- * $R_{DS(ON)} = 0.29\Omega @ V_{GS} = -10V$
- * Low capacitance
- * Low gate charge
- * Fast switching capability
- * Avalanche energy specified

■ SYMBOL



TO-252

Lead-free: 12P10L
Halogen-free: 12P10G

■ ORDERING INFORMATION

Ordering Number			Package	Pin Assignment			Packing
Normal	Lead Free	Halogen Free		1	2	3	
12P10-TN3-R	12P10L-TN3-R	12P10G-TN3-R	TO-252	G	D	S	Tape Reel
12P10-TN3-T	12P10L-TN3-T	12P10G-TN3-T	TO-252	G	D	S	Tube

12P10L-TN3-R (1)Packing Type (2)Package Type (3)Lead Plating	(1) R: Tape Reel, T: Tube (2) TN3: TO-252 (3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn
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■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	-100	V
Gate-Source Voltage	V_{GSS}	± 30	V
Continuous Drain Current	I_{D}	-9.4	A
Pulsed Drain Current (Note 2)	I_{DM}	-37.6	A
Avalanche Current (Note 2)	I_{AR}	-9.4	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	370	mJ
Repetitive Avalanche Energy (Note 2)	E_{AR}	5.0	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	-6.0	V/ns
Power Dissipation	P_{D}	50	W
Derate above 25°C		0.4	W/ $^{\circ}\text{C}$
Junction Temperature	T_{J}	+150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by $T_{\text{J(MAX)}}$
3. $L=6.3\text{mH}$, $I_{\text{AS}}=-9.4\text{A}$, $V_{\text{DD}}=-25\text{V}$, $R_{\text{G}}=25\Omega$, Starting $T_{\text{J}}=25^{\circ}\text{C}$
4. $I_{\text{SD}}\leq 11.5\text{A}$, $di/dt\leq 300\mu\text{A/s}$, $V_{\text{DD}}\leq BV_{\text{DSS}}$, Starting $T_{\text{J}}=25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction-to-Ambient	θ_{JA}			110	$^{\circ}\text{C/W}$
Junction-to-Case	θ_{JC}			2.5	$^{\circ}\text{C/W}$

■ ELECTRICAL CHARACTERISTICS ($T_c=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0 V, I _D =-250μA	-100			V
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _p =-250μA, Referenced to 25°C		-0.1		V/°C
Drain-Source Leakage Current	I _{DSS}	V _{DS} =-100V, V _{GS} =0V			-1	μA
Gate-Source Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±30V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-2.0		-4.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-4.7A		0.24	0.29	Ω
Forward Transconductance	g _{FS}	V _{DS} =-40V, I _D =-4.7A (Note 1)		6.3		S
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{DS} =-25V, V _{GS} =0V, f=1.0MHZ		620	800	pF
Output Capacitance	C _{OSS}			220	290	pF
Reverse Transfer Capacitance	C _{RSS}			65	85	pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =-80V, I _D =-11.5A, V _{GS} =-10V(Note 1, 2)		21	27	nC
Gate Source Charge	Q _{GS}			4.6		nC
Gate Drain Charge	Q _{GD}			11.5		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =-50V, I _D =-11.5A, R _G =25Ω(Note 1, 2)		15	40	ns
Turn-ON Rise Time	t _R			160	330	ns
Turn-OFF Delay Time	t _{D(OFF)}			35	80	ns
Turn-OFF Fall-Time	t _F			60	130	ns

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V$, $I_S=-9.4A$			-4.0	V
Maximum Body-Diode Continuous Current	I_S				-9.4	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				-37.6	A
Body Diode Reverse Recovery Time	t_{RR}	$V_{GS}=0V$, $I_S=-11.5A$,		110		ns
Body Diode Reverse Recovery Charge	Q_{RR}	$dI_F/dt=100A/s$ (Note 4)		0.47		nC

Note: 1. Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

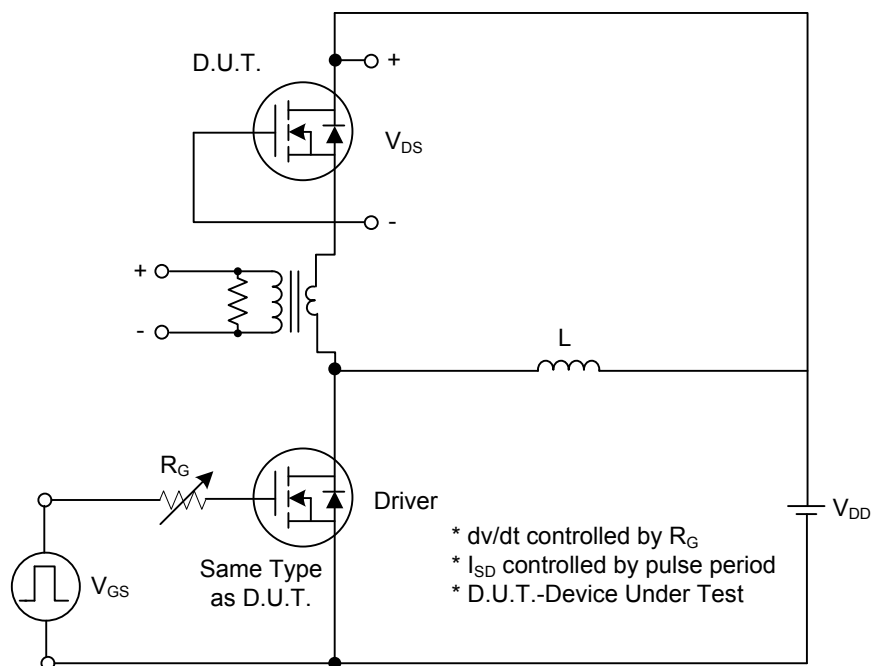


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

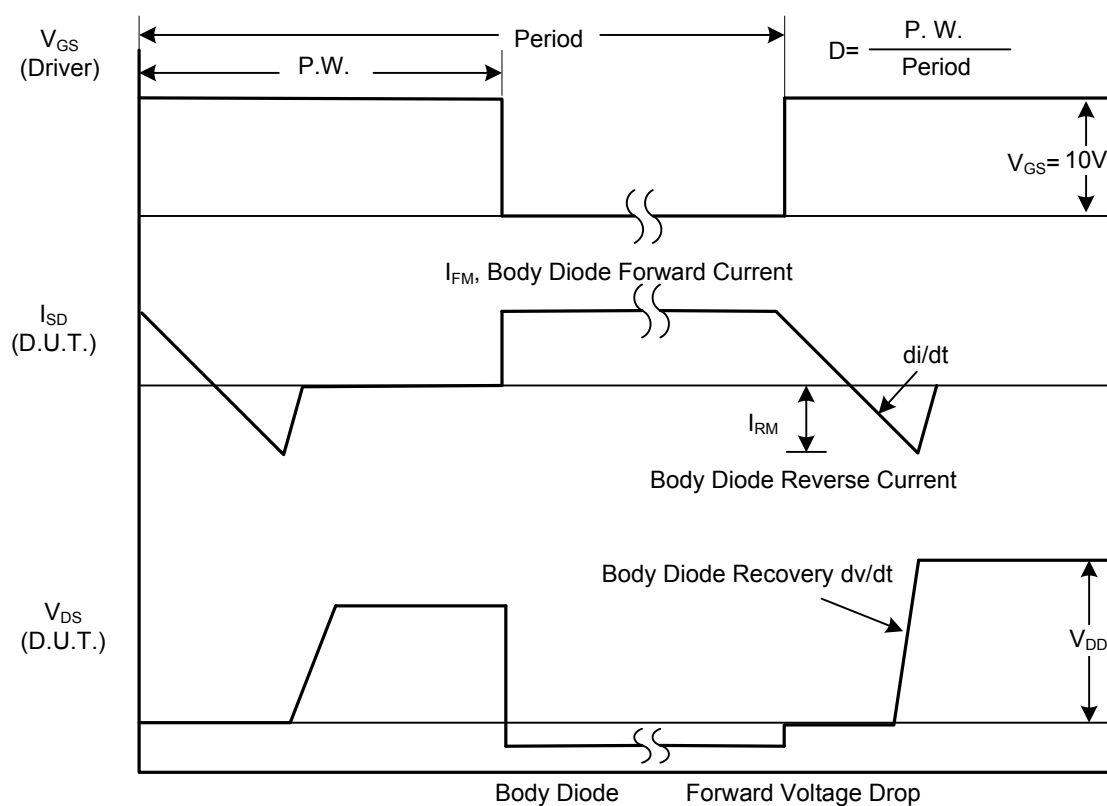


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

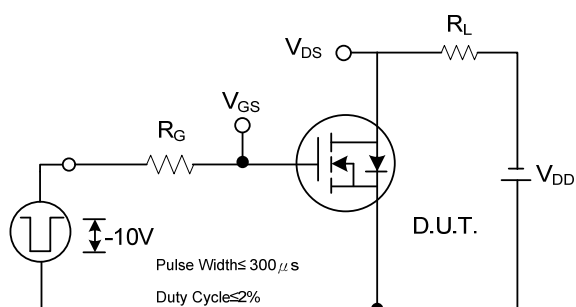


Fig. 2A Switching Test Circuit

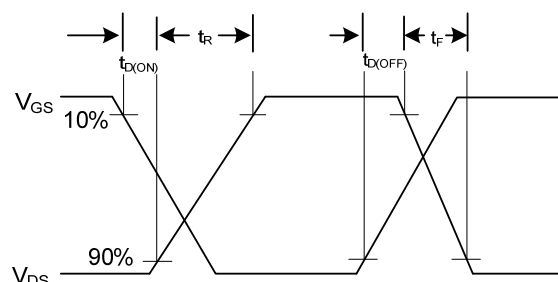


Fig. 2B Switching Waveforms

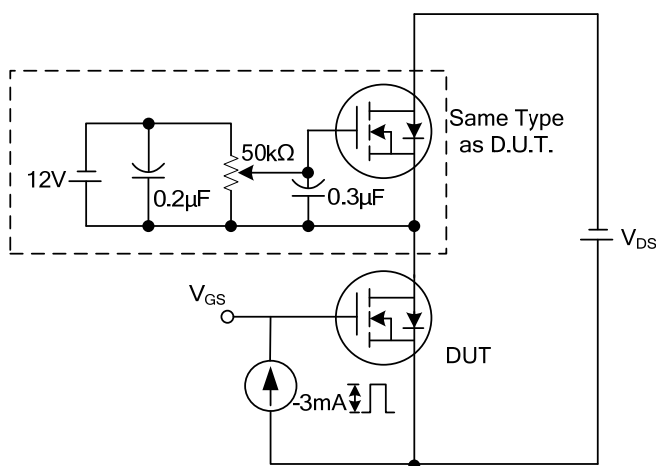


Fig. 3A Gate Charge Test Circuit

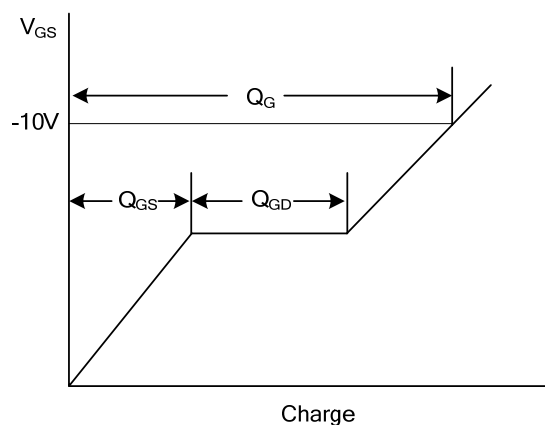


Fig. 3B Gate Charge Waveform

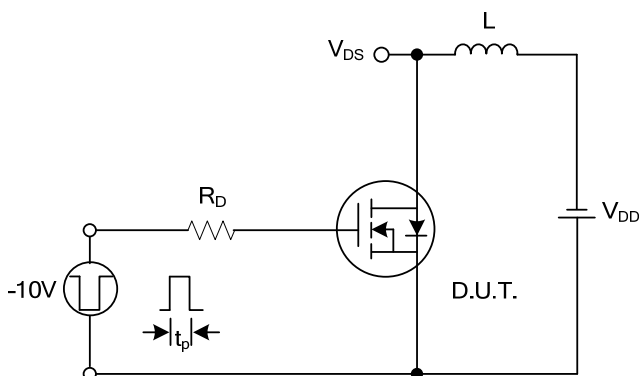


Fig. 4A Unclamped Inductive Switching Test Circuit

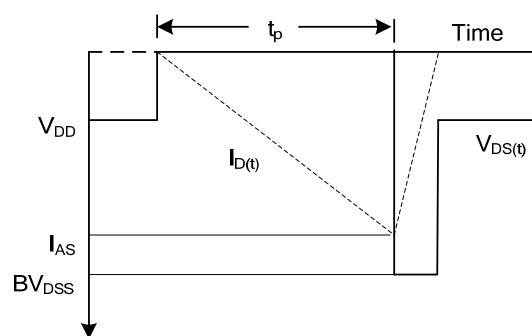
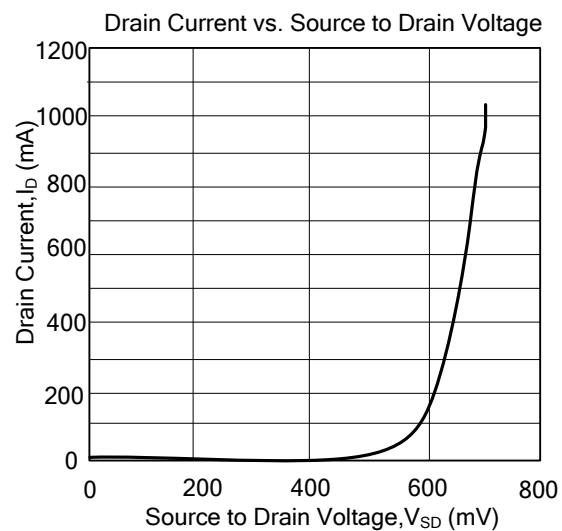


Fig. 4B Unclamped Inductive Switching Waveforms

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TYPICAL CHARACTERISTICS



Switching Time Waveforms

