

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.)

Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

MITSUBISHI 8-BIT SINGLE-CHIP MICROCOMPUTER
740 FAMILY / 38000 SERIES

38B5
Group

User's Manual

— keep safety first in your circuit designs ! —

- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

— Notes regarding these materials —

- These materials are intended as a reference to assist our customers in the selection of the Mitsubishi semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.
- Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts or circuit application examples contained in these materials.
- All information contained in these materials, including product data, diagrams and charts, represent information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for the latest product information before purchasing a product listed herein.
- Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
- The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.
- If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination. Any diversion or reexport contrary to the export control laws and regulations of JAPAN and/or the country of destination is prohibited.
- Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for further details on these materials or the products contained therein.

Preface

This user's manual describes Mitsubishi's CMOS 8-bit microcomputers 38B5 Group.

After reading this manual, the user should have a thorough knowledge of the functions and features of the 38B5 Group, and should be able to fully utilize the product. The manual starts with specifications and ends with application examples.

For details of software, refer to the "740 Family Software Manual."

For details of development support tools, refer to the "DEVELOPMENT SUPPORT TOOLS FOR MICROCOMPUTERS" data book.

BEFORE USING THIS USER'S MANUAL

This user's manual consists of the following three chapters. Refer to the chapter appropriate to your conditions, such as hardware design or software development.

1. Organization

● CHAPTER 1 HARDWARE

This chapter describes features of the microcomputer and operation of each peripheral function.

● CHAPTER 2 APPLICATION

This chapter describes usage and application examples of peripheral functions, based mainly on setting examples of relevant registers.

● CHAPTER 3 APPENDIX

This chapter includes a list of registers, and necessary information for systems development using the microcomputer, the mask ROM confirmation (for mask ROM version), ROM programming confirmation, and the mark specifications which are to be submitted when ordering.

2. Structure of Register

The figure of each register structure describes its functions, contents at reset, and attributes as follows:

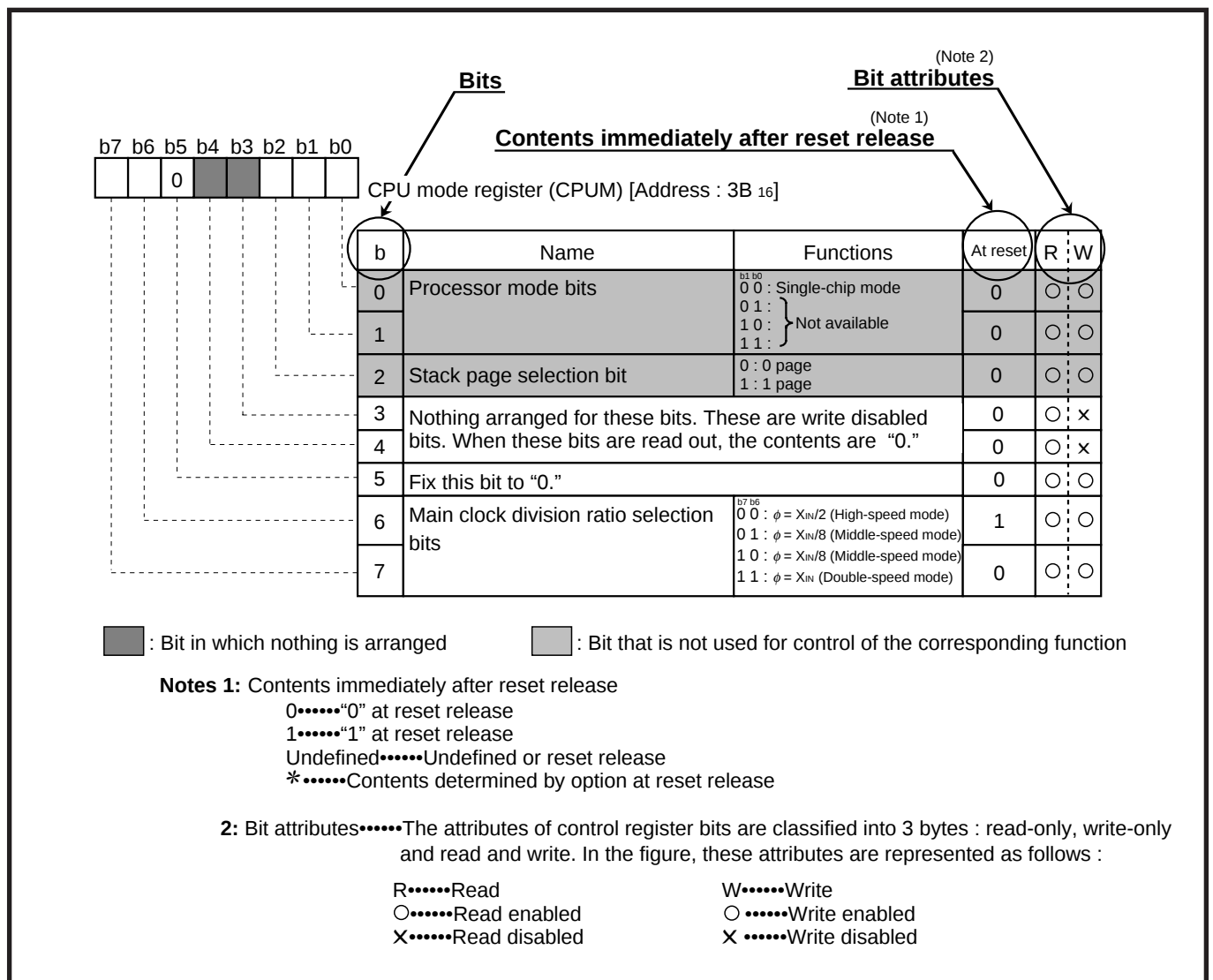


Table of contents

CHAPTER 1 HARDWARE

DESCRIPTION	1-2
FEATURES	1-2
APPLICATION	1-2
PIN CONFIGURATION	1-2
FUNCTIONAL BLOCK	1-3
PIN DESCRIPTION	1-4
PART NUMBERING	1-6
GROUP EXPANSION	1-7
Memory Type	1-7
Memory Size	1-7
Package	1-7
FUNCTIONAL DESCRIPTION	1-8
Central Processing Unit (CPU)	1-8
Memory	1-12
I/O Ports	1-14
Interrupts	1-20
Timers	1-23
Serial I/O	1-28
FLD Controller	1-40
A-D Converter	1-52
Pulse Width Modulation (PWM)	1-53
Interrupt Interval Determination Function	1-56
Watchdog Timer	1-58
Buzzer Output Circuit	1-59
Reset Circuit	1-60
Clock Generating Circuit	1-62
NOTES ON PROGRAMMING	1-65
NOTES ON USE	1-65
DATA REQUIRED FOR MASK ORDERS	1-66
DATA REQUIRED FOR ROM WRITING ORDERS	1-66
ROM PROGRAMMING METHOD	1-66
MASK OPTION OF PULL-DOWN RESISTOR	1-67
FUNCTIONAL DESCRIPTION SUPPLEMENT	1-69

CHAPTER 2 APPLICATION

2.1 I/O port	2-2
2.1.1 Memory assignment	2-2
2.1.2 Relevant registers	2-3
2.1.3 Terminate unused pins	2-6
2.1.4 Notes on use	2-7
2.1.5 Termination of unused pins	2-8
2.2 Timer	2-10
2.2.1 Memory map	2-10
2.2.2 Relevant registers	2-11

Table of contents

2.2.3 Timer application examples	2-19
2.3 Serial I/O	2-35
2.3.1 Memory map	2-35
2.3.2 Relevant registers	2-36
2.3.3 Serial I/O1 connection examples	2-47
2.3.4 Serial I/O1's modes	2-49
2.3.5 Serial I/O1 application examples	2-50
2.3.6 Serial I/O2 connection examples	2-56
2.3.7 Serial I/O2's modes	2-58
2.3.8 Serial I/O2 application examples	2-59
2.3.9 Notes on serial I/O1	2-78
2.3.10 Notes on serial I/O2	2-80
2.4 FLD controller	2-83
2.4.1 Memory assignment	2-83
2.4.2 Relevant registers	2-84
2.4.3 FLD controller application examples	2-93
2.4.4 Notes on use	2-124
2.5 A-D converter	2-125
2.5.1 Memory assignment	2-125
2.5.2 Relevant registers	2-125
2.5.3 A-D converter application examples	2-129
2.5.4 Notes on use	2-131
2.6 PWM	2-132
2.6.1 Memory assignment	2-132
2.6.2 Relevant registers	2-132
2.6.3 PWM application example	2-134
2.6.4 Notes on use	2-135
2.7 Interrupt interval determination function	2-136
2.7.1 Memory assignment	2-136
2.7.2 Relevant registers	2-136
2.7.3 Interrupt interval determination function application examples	2-140
2.8 Watchdog timer	2-144
2.8.1 Memory assignment	2-144
2.8.2 Relevant register	2-144
2.8.3 Watchdog timer application examples	2-145
2.8.4 Notes on use	2-146
2.9 Buzzer output circuit	2-147
2.9.1 Memory assignment	2-147
2.9.2 Relevant register	2-147
2.9.3 Buzzer output circuit application examples	2-148
2.10 Reset circuit	2-149
2.10.1 Connection example of reset IC	2-149
2.10.2 Notes on use	2-150
2.11 Clock generating circuit	2-151
2.11.1 Relevant register	2-151
2.11.2 Clock generating circuit application examples	2-152

CHAPTER 3 APPENDIX

3.1 Electrical characteristics	3-2
3.1.1 Absolute maximum ratings.....	3-2
3.1.2 Recommended operating conditions.....	3-3
3.1.3 Electrical characteristics	3-4
3.1.4 A-D converter characteristics	3-5
3.1.5 Timing requirements and switching characteristics	3-6
3.2 Standard characteristics	3-8
3.2.1 Power source current standard characteristics.....	3-8
3.2.2 Port standard characteristics	3-9
3.2.3 A-D conversion standard characteristics.....	3-13
3.3 Notes on use	3-14
3.3.1 Notes on interrupts	3-14
3.3.2 Notes on serial I/O1	3-15
3.3.3 Notes on serial I/O2	3-16
3.3.4 Notes on FLD controller	3-19
3.3.5 Notes on A-D converter	3-19
3.3.6 Notes on PWM	3-19
3.3.7 Notes on watchdog timer	3-20
3.3.8 Notes on reset circuit	3-20
3.3.9 Notes on input and output pins	3-20
3.3.10 Notes on programming	3-22
3.3.11 Programming and test of built-in PROM version.....	3-23
3.3.12 Notes on built-in PROM version	3-24
3.3.13 Termination of unused pins.....	3-25
3.4 Countermeasures against noise	3-26
3.4.1 Shortest wiring length.....	3-26
3.4.2 Connection of bypass capacitor across V_{SS} line and V_{CC} line.....	3-28
3.4.3 Wiring to analog input pins	3-29
3.4.4 Oscillator concerns.....	3-29
3.4.5 Setup for I/O ports.....	3-31
3.4.6 Providing of watchdog timer function by software	3-32
3.5 Control registers.....	3-33
3.6 Mask ROM confirmation form.....	3-67
3.7 ROM programming confirmation form.....	3-75
3.8 Mark specification form	3-77
3.9 Package outline	3-78
3.10 List of instruction code	3-79
3.11 Machine instructions	3-80
3.12 M35501FP	3-91
3.13 SFR memory map.....	3-103
3.14 Pin configuration	3-104

List of figures

CHAPTER 1 HARDWARE

Fig. 1 Pin configuration of M38B5xMxH-XXXXFP	1-2
Fig. 2 Functional block diagram.....	1-3
Fig. 3 Part numbering.....	1-6
Fig. 4 Memory expansion plan.....	1-7
Fig. 5 740 Family CPU register structure.....	1-8
Fig. 6 Register push and pop at interrupt generation and subroutine call	1-9
Fig. 7 Structure of CPU mode register	1-11
Fig. 8 Memory map diagram	1-12
Fig. 9 Memory map of special function register (SFR)	1-13
Fig. 10 Structure of pull-up control registers (PULL1 and PULL2)	1-14
Fig. 11 Port block diagram (1).....	1-17
Fig. 12 Port block diagram (2).....	1-18
Fig. 13 Port block diagram (3).....	1-19
Fig. 14 Interrupt control.....	1-22
Fig. 15 Structure of interrupt related registers	1-22
Fig. 16 Structure of timer related register	1-23
Fig. 17 Block diagram of timer	1-24
Fig. 18 Timing chart of timer 6 PWM ₁ mode	1-25
Fig. 19 Block diagram of timer X	1-27
Fig. 20 Structure of timer X related registers	1-27
Fig. 21 Block diagram of serial I/O1	1-28
Fig. 22 Structure of serial I/O1 control registers 1, 2	1-29
Fig. 23 Structure of serial I/O1 control register 3.....	1-30
Fig. 24 Structure of serial I/O1 automatic transfer data pointer	1-31
Fig. 25 Automatic transfer serial I/O operation	1-32
Fig. 26 S _{STB1} output operation	1-33
Fig. 27 S _{BUSY1} input operation (internal synchronous clock).....	1-33
Fig. 28 S _{BUSY1} input operation (external synchronous clock).....	1-33
Fig. 29 S _{BUSY1} output operation (internal synchronous clock, 8-bits serial I/O).....	1-34
Fig. 30 S _{BUSY1} output operation (external synchronous clock, 8-bits serial I/O)	1-34
Fig. 31 S _{BUSY1} output operation in automatic transfer serial I/O mode (internal synchronous clock, S _{BUSY1} output function outputs each 1-byte)	1-34
Fig. 32 S _{RDY1} output operation	1-35
Fig. 33 S _{RDY1} input operation (internal synchronous clock)	1-35
Fig. 34 Handshake operation at serial I/O1 mutual connecting (1).....	1-36
Fig. 35 Handshake operation at serial I/O1 mutual connecting (2).....	1-36
Fig. 36 Block diagram of clock synchronous serial I/O2	1-37
Fig. 37 Operation of clock synchronous serial I/O2 function	1-37
Fig. 38 Block diagram of UART serial I/O2	1-38
Fig. 39 Operation of UART serial I/O2 function	1-38
Fig. 40 Structure of serial I/O2 related register	1-39
Fig. 41 Block diagram for FLD control circuit.....	1-40
Fig. 42 Structure of FLDC mode register	1-41
Fig. 43 Segment/Digit setting example	1-42
Fig. 44 FLD automatic display RAM assignment	1-43
Fig. 45 Example of using FLD automatic display RAM in 16-timing•ordinary mode	1-44

List of figures

Fig. 46 Example of using FLD automatic display RAM in 16-timing•gradation display mode	1-45
Fig. 47 Example of using FLD automatic display RAM in 32-timing mode.....	1-46
Fig. 48 Structure of FLDRAM write disable register	1-47
Fig. 49 Example of digit timing using grid scan type	1-48
Fig. 50 Example of using FLD automatic display RAM using grid scan type	1-48
Fig. 51 FLDC timing	1-50
Fig. 52 P8 ₄ to P8 ₇ FLD output waveform	1-51
Fig. 53 Structure of port P8 FLD output control register	1-51
Fig. 54 Structure of A-D control register	1-52
Fig. 55 Block diagram of A-D converter	1-52
Fig. 56 PWM block diagram	1-53
Fig. 57 PWM timing	1-54
Fig. 58 Structure of PWM control register	1-55
Fig. 59 14-bit PWM timing	1-55
Fig. 60 Interrupt interval determination circuit block diagram	1-56
Fig. 61 Structure of iterrupt interval determination control register	1-57
Fig. 62 Interrupt interval determination operation example (at rising edge active)	1-57
Fig. 63 Interrupt interval determination operation example (at both-sided edge active) ...	1-57
Fig. 64 Block diagram of watchdog timer	1-58
Fig. 65 Structure of watchdog timer control register	1-58
Fig. 66 Block diagram of buzzer output circuit.....	1-59
Fig. 67 Structure of buzzer output control register	1-59
Fig. 68 Reset circuit example	1-60
Fig. 69 Reset sequence	1-60
Fig. 70 Internal status at reset	1-61
Fig. 71 Ceramic resonator circuit	1-62
Fig. 72 External clock input circuit	1-62
Fig. 73 Clock generating circuit block diagram	1-63
Fig. 74 State transitions of system clock	1-64
Fig. 75 Programming and testing of One Time PROM version	1-66
Fig. 76 Digit timing waveform (1)	1-67
Fig. 77 Digit timing waveform (2)	1-68
Fig. 78 Timing chart after interrupt occurs.....	1-70
Fig. 79 Tlme up to execution of interrupt processing routine	1-70
Fig. 80 A-D conversion equivalent circuit.....	1-72
Fig. 81 A-D conversion timing chart.....	1-72

CHAPTER 2 APPLICATION

Fig. 2.1.1 Memory assignment of I/O port relevant registers.....	2-2
Fig. 2.1.2 Structure of port P _i (i = 0, 1, 2, 3, 4, 5, 7, 8)	2-3
Fig. 2.1.3 Structure of port P6	2-3
Fig. 2.1.4 Structure of port P9	2-3
Fig. 2.1.5 Structure of port P _i (i = 0, 2, 4, 5, 7, 8) direction register	2-4
Fig. 2.1.6 Structure of port P6 direction register	2-4
Fig. 2.1.7 Structure of port P9 direction register	2-5
Fig. 2.1.8 Structure of pull-up control register 1	2-5
Fig. 2.1.9 Structure of pull-up control register 2	2-6
Fig. 2.2.1 Memory map of registers relevant to timers	2-10

Fig. 2.2.2 Structure of Timer i (i=1, 3, 4, 5, 6)	2-11
Fig. 2.2.3 Structure of Timer 2	2-11
Fig. 2.2.4 Structure of Timer 6 PWM register	2-11
Fig. 2.2.5 Structure of Timer 12 mode register	2-12
Fig. 2.2.6 Structure of Timer 34 mode register	2-12
Fig. 2.2.7 Structure of Timer 56 mode register	2-13
Fig. 2.2.8 Structure of Timer X (low-order, high-order)	2-13
Fig. 2.2.9 Structure of Timer X mode register 1	2-14
Fig. 2.2.10 Structure of Timer X mode register 2	2-15
Fig. 2.2.11 Structure of Interrupt request register 1	2-16
Fig. 2.2.12 Structure of Interrupt request register 2	2-17
Fig. 2.2.13 Structure of Interrupt control register 1	2-18
Fig. 2.2.14 Structure of Interrupt control register 2	2-18
Fig. 2.2.15 Timers connection and setting of division ratios	2-20
Fig. 2.2.16 Relevant registers setting	2-21
Fig. 2.2.17 Control procedure	2-22
Fig. 2.2.18 Peripheral circuit example	2-23
Fig. 2.2.19 Timers connection and setting of division ratios	2-23
Fig. 2.2.20 Relevant registers setting	2-24
Fig. 2.2.21 Control procedure	2-24
Fig. 2.2.22 Judgment method of valid/invalid of input pulses	2-25
Fig. 2.2.23 Relevant registers setting	2-26
Fig. 2.2.24 Control procedure	2-27
Fig. 2.2.25 Timers connection and setting of division ratios	2-28
Fig. 2.2.26 Relevant registers setting	2-29
Fig. 2.2.27 Control procedure	2-30
Fig. 2.2.28 Timers connection and table example of timer X/RTP setting values	2-32
Fig. 2.2.29 RTP output example	2-32
Fig. 2.2.30 Relevant registers setting	2-33
Fig. 2.2.31 Control procedure	2-34
Fig. 2.3.1 Memory map of registers relevant to Serial I/O	2-35
Fig. 2.3.2 Structure of Serial I/O1 automatic transfer data pointer	2-36
Fig. 2.3.3 Structure of Serial I/O1 control register 1	2-37
Fig. 2.3.4 Structure of Serial I/O1 control register 2	2-38
Fig. 2.3.5 Structure of Serial I/O1 register/Transfer counter	2-39
Fig. 2.3.6 Structure of Serial I/O1 control register 3	2-40
Fig. 2.3.7 Structure of Baud rate generator	2-41
Fig. 2.3.8 Structure of UART control register	2-41
Fig. 2.3.9 Structure of Serial I/O2 control register	2-42
Fig. 2.3.10 Structure of Serial I/O2 status register	2-43
Fig. 2.3.11 Structure of Serial I/O2 transmit/receive buffer register	2-43
Fig. 2.3.12 Structure of Interrupt source switch register	2-44
Fig. 2.3.13 Structure of Interrupt request register 1	2-44
Fig. 2.3.14 Structure of Interrupt request register 2	2-45
Fig. 2.3.15 Structure of Interrupt control register 1	2-46
Fig. 2.3.16 Structure of Interrupt control register 2	2-46
Fig. 2.3.17 Serial I/O1 connection examples (1)	2-47
Fig. 2.3.18 Serial I/O1 connection examples (2)	2-48
Fig. 2.3.19 Serial I/O1's modes	2-49
Fig. 2.3.20 Connection diagram	2-50
Fig. 2.3.21 Timing chart	2-50

List of figures

Fig. 2.3.22 Registers setting relevant to transmission side	2-51
Fig. 2.3.23 Setting of transmission data	2-51
Fig. 2.3.24 Control procedure.....	2-52
Fig. 2.3.25 Connection diagram	2-53
Fig. 2.3.26 Timing chart of serial data transmission/reception	2-53
Fig. 2.3.27 Relevant registers setting	2-54
Fig. 2.3.28 Control procedure.....	2-55
Fig. 2.3.29 Serial I/O2 connection examples (1)	2-56
Fig. 2.3.30 Serial I/O2 connection examples (2)	2-57
Fig. 2.3.31 Serial I/O2's modes	2-58
Fig. 2.3.32 Serial I/O2 transfer data format	2-58
Fig. 2.3.33 Connection diagram	2-59
Fig. 2.3.34 Timing chart	2-59
Fig. 2.3.35 Registers setting relevant to transmission side	2-60
Fig. 2.3.36 Registers setting relevant to reception side	2-61
Fig. 2.3.37 Control procedure of transmission side	2-62
Fig. 2.3.38 Control procedure of reception side	2-63
Fig. 2.3.39 Connection diagram	2-64
Fig. 2.3.40 Timing chart	2-64
Fig. 2.3.41 Relevant registers setting	2-65
Fig. 2.3.42 Setting of transmission data	2-65
Fig. 2.3.43 Control procedure.....	2-66
Fig. 2.3.44 Connection diagram	2-67
Fig. 2.3.45 Timing chart	2-68
Fig. 2.3.46 Relevant registers setting in master unit	2-68
Fig. 2.3.47 Relevant registers setting in slave unit	2-69
Fig. 2.3.48 Control procedure of master unit.....	2-70
Fig. 2.3.49 Control procedure of slave unit	2-71
Fig. 2.3.50 Connection diagram	2-72
Fig. 2.3.51 Timing chart	2-72
Fig. 2.3.52 Registers setting relevant to transmission side	2-74
Fig. 2.3.53 Registers setting relevant to reception side.....	2-75
Fig. 2.3.54 Control procedure of transmission side	2-76
Fig. 2.3.55 Control procedure of reception side	2-77
Fig. 2.3.56 Sequence of setting serial I/O2 control register again.....	2-81
Fig. 2.4.1 Memory assignment of FLD controller relevant registers.....	2-83
Fig. 2.4.2 Structure of P1FLDRAM write disable register	2-84
Fig. 2.4.3 Structure of P3FLDRAM write disable register	2-85
Fig. 2.4.4 Structure of FLD mode register	2-86
Fig. 2.4.5 Structure of Tdisp time set register.....	2-87
Fig. 2.4.6 Structure of Toff1 time set register	2-88
Fig. 2.4.7 Structure of Toff2 time set register	2-88
Fig. 2.4.8 Structure of FLD data pointer/FLD data pointer reload register	2-89
Fig. 2.4.9 Structure of port P0FLD/port switch register.....	2-89
Fig. 2.4.10 Structure of port P2FLD/port switch register	2-90
Fig. 2.4.11 Structure of port P8FLD/port switch register	2-90
Fig. 2.4.12 Structure of port P8FLD output control register	2-91
Fig. 2.4.13 Structure of interrupt request register 2	2-91
Fig. 2.4.14 Structure of interrupt control register 2	2-92
Fig. 2.4.15 Connection diagram	2-93
Fig. 2.4.16 Timing chart of key-scan using FLD automatic display mode and segments.....	2-93

Fig. 2.4.17 Enlarged view of FLD ₀ (P2 ₀) to FLD ₇ (P2 ₇) Tscan	2-93
Fig. 2.4.18 Setting of relevant registers	2-94
Fig. 2.4.19 FLD digit allocation example	2-97
Fig. 2.4.20 Control procedure.....	2-98
Fig. 2.4.21 Connection diagram	2-100
Fig. 2.4.22 Timing chart of key-scan using FLD automatic display mode and digits	2-101
Fig. 2.4.23 Setting of relevant registers	2-102
Fig. 2.4.24 FLD digit allocation example	2-105
Fig. 2.4.25 Control procedure.....	2-106
Fig. 2.4.26 Connection diagram	2-108
Fig. 2.4.27 Timing chart of FLD display by software	2-108
Fig. 2.4.28 Enlarged view of P2 ₀ to P2 ₇ key-scan	2-108
Fig. 2.4.29 Setting of relevant registers	2-109
Fig. 2.4.30 FLD digit allocation example	2-110
Fig. 2.4.31 Control procedure.....	2-111
Fig. 2.4.32 Connection diagram	2-112
Fig. 2.4.33 Timing chart of 38B5 Group and M35501FP	2-113
Fig. 2.4.34 Timing chart (enlarged view) of digit and segment output	2-113
Fig. 2.4.35 Setting of relevant registers	2-114
Fig. 2.4.36 FLD digit allocation example	2-117
Fig. 2.4.37 Control procedure.....	2-117
Fig. 2.4.38 Connection diagram	2-118
Fig. 2.4.39 Timing chart (at correct state) of 38B5 Group and M35501FP	2-119
Fig. 2.4.40 Timing chart (at incorrect state) of 38B5 Group and M35501FP	2-119
Fig. 2.4.41 Setting of relevant registers	2-120
Fig. 2.4.42 Control procedure.....	2-122
Fig. 2.5.1 Memory assignment of A-D converter relevant registers	2-125
Fig. 2.5.2 Structure of A-D control register	2-125
Fig. 2.5.3 Structure of A-D conversion register (low-order)	2-126
Fig. 2.5.4 Structure of A-D conversion register (high-order)	2-126
Fig. 2.5.5 Structure of interrupt request register 2	2-127
Fig. 2.5.6 Structure of interrupt control register 2	2-128
Fig. 2.5.7 Connection diagram	2-129
Fig. 2.5.8 Setting of relevant registers	2-129
Fig. 2.5.9 Control procedure.....	2-130
Fig. 2.6.1 Memory assignment of PWM relevant registers	2-132
Fig. 2.6.2 Structure of PWM register (high-order).....	2-132
Fig. 2.6.3 Structure of PWM register (low-order)	2-133
Fig. 2.6.4 Structure of PWM control register	2-133
Fig. 2.6.5 Connection diagram	2-134
Fig. 2.6.6 Setting of relevant registers	2-134
Fig. 2.6.7 Control procedure.....	2-135
Fig. 2.6.8 PWM ₀ output	2-135
Fig. 2.7.1 Memory assignment of interrupt interval determination function relevant registers	2-136
Fig. 2.7.2 Structure of interrupt interval determination register.....	2-136
Fig. 2.7.3 Structure of interrupt interval determination control register	2-137
Fig. 2.7.4 Structure of interrupt edge selection register.....	2-137
Fig. 2.7.5 Structure of interrupt request register 1	2-138
Fig. 2.7.6 Structure of interrupt control register 1	2-139
Fig. 2.7.7 Connection diagram	2-140

List of figures

Fig. 2.7.8 Function block diagram	2-140
Fig. 2.7.9 Timing chart of data determination	2-140
Fig. 2.7.10 Setting of relevant registers	2-141
Fig. 2.7.11 Control procedure.....	2-142
Fig. 2.7.12 Reception of remote-control data (timer 2 interrupt)	2-143
Fig. 2.8.1 Memory assignment of watchdog timer relevant register	2-144
Fig. 2.8.2 Structure of watchdog timer control register	2-144
Fig. 2.8.3 Connection of watchdog timer and setting of division ratio	2-145
Fig. 2.8.4 Setting of relevant registers	2-145
Fig. 2.8.5 Control procedure.....	2-146
Fig. 2.9.1 Memory assignment of buzzer output circuit relevant register	2-147
Fig. 2.9.2 Structure of buzzer output control register	2-147
Fig. 2.9.3 Connection of buzzer output circuit and setting of division ratio.....	2-148
Fig. 2.9.4 Setting of relevant register	2-148
Fig. 2.9.5 Control procedure.....	2-148
Fig. 2.10.1 Example of power-on reset circuit.....	2-149
Fig. 2.10.2 RAM backup system example	2-149
Fig. 2.11.1 Structure of CPU mode register	2-151
Fig. 2.11.2 Connection diagram	2-152
Fig. 2.11.3 Status transition diagram during power failure	2-152
Fig. 2.11.4 Setting of relevant registers	2-153
Fig. 2.11.5 Control procedure.....	2-154
Fig. 2.11.6 Structure of clock counter	2-155
Fig. 2.11.7 Initial setting of relevant registers	2-156
Fig. 2.11.8 Setting of relevant registers after detecting power failure	2-157
Fig. 2.11.9 Control procedure.....	2-158

CHAPTER 3 APPENDIX

Fig. 3.1.1 Circuit for measuring output switching characteristics	3-6
Fig. 3.1.2 Timing diagram	3-7
Fig. 3.2.1 Power source current standard characteristics	3-8
Fig. 3.2.2 Power source current standard characteristics (in wait mode)	3-8
Fig. 3.2.3 High-breakdown P-channel open-drain output port characteristics (25 °C)	3-9
Fig. 3.2.4 High-breakdown P-channel open-drain output port characteristics (90 °C)	3-9
Fig. 3.2.5 CMOS output port P-channel side characteristics (25 °C)	3-10
Fig. 3.2.6 CMOS output port P-channel side characteristics (90 °C)	3-10
Fig. 3.2.7 CMOS output port N-channel side characteristics (25 °C)	3-11
Fig. 3.2.8 CMOS output port N-channel side characteristics (90 °C)	3-11
Fig. 3.2.9 N-channel open-drain output port characteristics (25 °C)	3-12
Fig. 3.2.10 N-channel open-drain output port characteristics (90 °C)	3-12
Fig. 3.2.11 A-D conversion standard characteristics.....	3-13
Fig. 3.3.1 Sequence of switch detection edge	3-14
Fig. 3.3.2 Sequence of check of interrupt request bit	3-14
Fig. 3.3.3 Structure of interrupt control register 2	3-15
Fig. 3.3.4 Sequence of setting serial I/O2 control register again	3-18
Fig. 3.3.5 PWM output	3-19
Fig. 3.3.6 Initialization of processor status register	3-22
Fig. 3.3.7 Sequence of PLP instruction execution	3-22
Fig. 3.3.8 Stack memory contents after PHP instruction execution	3-22

Fig. 3.3.9 Status flag at decimal calculations	3-23
Fig. 3.3.10 Programming and testing of One Time PROM version	3-23
Fig. 3.4.1 Selection of packages	3-26
Fig. 3.4.2 Wiring for the RESET pin	3-26
Fig. 3.4.3 Wiring for clock I/O pins	3-27
Fig. 3.4.4 Wiring for the V _{PP} pin of the One Time PROM and the EPROM version	3-28
Fig. 3.4.5 Bypass capacitor across the V _{SS} line and the V _{CC} line	3-28
Fig. 3.4.6 Analog signal line and a resistor and a capacitor	3-29
Fig. 3.4.7 Wiring for a large current signal line	3-29
Fig. 3.4.8 Wiring of signal lines where potential levels change frequently	3-30
Fig. 3.4.9 V _{SS} pattern on the underside of an oscillator	3-30
Fig. 3.4.10 Setup for I/O ports	3-31
Fig. 3.4.11 Watchdog timer by software	3-32
Fig. 3.5.1 Structure of port Pi	3-33
Fig. 3.5.2 Structure of port Pi direction register	3-33
Fig. 3.5.3 Structure of port P6	3-34
Fig. 3.5.4 Structure of port P6 direction register	3-34
Fig. 3.5.5 Structure of port P9	3-35
Fig. 3.5.6 Structure of port P9 direction register	3-35
Fig. 3.5.7 Structure of PWM register (high-order)	3-36
Fig. 3.5.8 Structure of PWM register (low-order)	3-36
Fig. 3.5.9 Structure of baud rate generator	3-37
Fig. 3.5.10 Structure of UART control register	3-37
Fig. 3.5.11 Structure of serial I/O1 automatic transfer data pointer	3-38
Fig. 3.5.12 Structure of serial I/O1 control register 1	3-38
Fig. 3.5.13 Structure of serial I/O1 control register 2	3-39
Fig. 3.5.14 Structure of serial I/O1 register/Transfer counter	3-40
Fig. 3.5.15 Structure of serial I/O1 control register 3	3-41
Fig. 3.5.16 Structure of serial I/O2 control register	3-42
Fig. 3.5.17 Structure of serial I/O2 status register	3-43
Fig. 3.5.18 Structure of serial I/O2 transmit/receive buffer register	3-43
Fig. 3.5.19 Structure of timer i	3-44
Fig. 3.5.20 Structure of timer 2	3-44
Fig. 3.5.21 Structure of PWM control register	3-44
Fig. 3.5.22 Structure of timer 6 PWM register	3-45
Fig. 3.5.23 Structure of timer 12 mode register	3-45
Fig. 3.5.24 Structure of timer 34 mode register	3-46
Fig. 3.5.25 Structure of timer 56 mode register	3-46
Fig. 3.5.26 Structure of watchdog timer control register	3-47
Fig. 3.5.27 Structure of timer X (low-order, high-order)	3-47
Fig. 3.5.28 Structure of timer X mode register 1	3-48
Fig. 3.5.29 Structure of timer X mode register 2	3-49
Fig. 3.5.30 Structure of interrupt interval determination register	3-49
Fig. 3.5.31 Structure of interrupt interval determination control register	3-50
Fig. 3.5.32 Structure of A-D control register	3-50
Fig. 3.5.33 Structure of A-D conversion register (low-order)	3-51
Fig. 3.5.34 Structure of A-D conversion register (high-order)	3-51
Fig. 3.5.35 Structure of interrupt source switch register	3-52
Fig. 3.5.36 Structure of interrupt edge selection register	3-52
Fig. 3.5.37 Structure of CPU mode register	3-53
Fig. 3.5.38 Structure of interrupt request register 1	3-54

List of figures

Fig. 3.5.39 Structure of interrupt request register 2	3-55
Fig. 3.5.40 Structure of interrupt control register 1	3-56
Fig. 3.5.41 Structure of interrupt control register 2	3-57
Fig. 3.5.42 Structure of pull-up control register 1	3-58
Fig. 3.5.43 Structure of pull-up control register 2	3-58
Fig. 3.5.44 Structure of P1FLDRAM write disable register	3-59
Fig. 3.5.45 Structure of P3FLDRAM write disable register	3-60
Fig. 3.5.46 Structure of FLDC mode register	3-61
Fig. 3.5.47 Structure of Tdisp time set register	3-62
Fig. 3.5.48 Structure of Toff1 time set register	3-63
Fig. 3.5.49 Structure of Toff2 time set register	3-63
Fig. 3.5.50 Structure of FLD data pointer/FLD data pointer reload register	3-64
Fig. 3.5.51 Structure of port P0FLD/Port switch register	3-64
Fig. 3.5.52 Structure of port P2FLD/port switch register	3-65
Fig. 3.5.53 Structure of port P8FLD/port switch register	3-65
Fig. 3.5.54 Structure of port P8FLD output control register	3-66
Fig. 3.5.55 Structure of buzzer output control register	3-66
Fig. 3.12.1 Pin configuration of M35501FP	3-91
Fig. 3.12.2 Functional block diagram	3-92
Fig. 3.12.3 Port block diagram	3-93
Fig. 3.12.4 Digit setting	3-94
Fig. 3.12.5 16-digit mode output waveform	3-95
Fig. 3.12.6 Optional digit mode output waveform	3-95
Fig. 3.12.7 Cascade mode connection example: 17 digits or more selected	3-96
Fig. 3.12.8 Cascade mode output waveform	3-96
Fig. 3.12.9 Connection example with 38B5 Group microcomputer (1 to 16 digits)	3-97
Fig. 3.12.10 Connection example with 38B5 Group microcomputer (17 to 32 digits)	3-97
Fig. 3.12.11 Digit output waveform when reset signal is input	3-98
Fig. 3.12.12 Power-on reset circuit	3-99
Fig. 3.12.13 Timing diagram	3-102

List of tables

CHAPTER 1 HARDWARE

Table 1 Pin description (1)	1-4
Table 2 Pin description (2)	1-5
Table 3 List of supported products	1-7
Table 4 Push and pop instructions of accumulator or processor status register	1-9
Table 5 Set and clear instructions of each bit of processor status register	1-10
Table 6 List of I/O port functions (1)	1-15
Table 7 List of I/O port functions (2)	1-16
Table 8 Interrupt vector addresses and priority	1-21
Table 9 Pins in FLD automatic display mode	1-42
Table 10 Relationship between low-order 6-bit data and setting period of ADD bit	1-54
Table 11 Special programming adapter	1-66
Table 12 Mask option type of pull-down resistor	1-67
Table 13 Interrupt sources, vector addresses and interrupt priority	1-69
Table 14 Relative formula for a reference voltage V_{REF} of A-D converter and V_{ref}	1-71
Table 15 Change of A-D conversion register during A-D conversion	1-71

CHAPTER 2 APPLICATION

Table 2.1.1 Termination of unused pins	2-6
Table 2.3.1 Setting examples of baud rate generator values and transfer bit rate values	2-73
Table 2.4.1 FLD automatic display RAM map	2-96
Table 2.4.2 FLD automatic display RAM map example	2-97
Table 2.4.3 FLD automatic display RAM map	2-104
Table 2.4.4 FLD automatic display RAM map example	2-105
Table 2.4.5 FLD automatic display RAM map example	2-110
Table 2.4.6 FLD automatic display RAM map	2-116

CHAPTER 3 APPENDIX

Table 3.1.1 Absolute maximum ratings	3-2
Table 3.1.2 Recommended operating conditions (1)	3-3
Table 3.1.3 Recommended operating conditions (2)	3-4
Table 3.1.4 Electrical characteristics (1)	3-4
Table 3.1.5 Electrical characteristics (2)	3-5
Table 3.1.6 A-D converter characteristics	3-5
Table 3.1.7 Timing requirements	3-6
Table 3.1.8 Switching characteristics	3-6
Table 3.3.1 Programming adapter	3-24
Table 3.3.2 PROM programmer address setting	3-24
Table 3.12.1 Pin description	3-92
Table 3.12.2 Absolute maximum ratings	3-100
Table 3.12.3 Recommended operating conditions	3-100
Table 3.12.4 Recommended operating conditions	3-100
Table 3.12.5 Electrical characteristics	3-101
Table 3.12.6 Timing requirements	3-102

CHAPTER 1

HARDWARE

DESCRIPTION
FEATURES
APPLICATION
PIN CONFIGURATION
FUNCTIONAL BLOCK
PIN DESCRIPTION
PART NUMBERING
GROUP EXPANSION
FUNCTIONAL DESCRIPTION
NOTES ON PROGRAMMING
NOTES ON USE
DATA REQUIRED FOR MASK
ORDERS
DATA REQUIRED FOR ROM WRITING
ORDERS
ROM PROGRAMMING METHOD
MASK OPTION OF PULL-DOWN
RESISTOR
FUNCTIONAL DESCRIPTION
SUPPLEMENT

HARDWARE

DESCRIPTION/FEATURES/APPLICATION/PIN CONFIGURATION

DESCRIPTION

The 38B5 group is the 8-bit microcomputer based on the 740 family core technology.

The 38B5 group has six 8-bit timers, a 16-bit timer, a fluorescent display automatic display circuit, 12-channel 10-bit A-D converter, a serial I/O with automatic transfer function, which are available for controlling musical instruments and household appliances. The 38B5 group has variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 38B5 group, refer to the section on group expansion.

Built-in pull-down resistors connected to high-breakdown voltage ports are available by specifying with the mask option in some products. For the details, refer to the section on the mask option of pull-down resistor.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time 0.48 μ s (at 4.19 MHz oscillation frequency)
- Memory size
 - ROM 24K to 60K bytes
 - RAM 1024 to 2048 bytes
- Programmable input/output ports 55
- High-breakdown-voltage output ports 36
- Software pull-up resistors (Ports P5, P6₁ to P6₅, P7, P8₄ to P8₇, P9)
- Interrupts 21 sources, 16 vectors
- Timers 8-bit X 6, 16-bit X 1
- Serial I/O1 (Clock-synchronized) 8-bit X 1 (max. 256-byte automatic transfer function)

- Serial I/O2 (UART or Clock-synchronized) 8-bit X 1
- PWM 14-bit X 1 8-bit X 1 (also functions as timer 6)
- A-D converter 10-bit X 12 channels
- Fluorescent display function Total 40 control pins
- Interrupt interval determination function 1
- Watchdog timer 20-bit X 1
- Buzzer output 1
- 2 Clock generating circuit
 - Main clock (X_{IN}–X_{OUT}) Internal feedback resistor
 - Sub-clock (X_{CIN}–X_{COU}T) Without internal feedback resistor (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
 - In high-speed mode 4.0 to 5.5 V (at 4.19 MHz oscillation frequency and high-speed selected)
 - In middle-speed mode 2.7 to 5.5 V (at 4.19 MHz oscillation frequency and middle-speed selected)
 - In low-speed mode 2.7 to 5.5 V (at 32 kHz oscillation frequency)
- Power dissipation
 - In high-speed mode 35 mW (at 4.19 MHz oscillation frequency)
 - In low-speed mode 60 μ W (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range –20 to 85 °C

APPLICATION

Musical instruments, VCR, household appliances, etc.

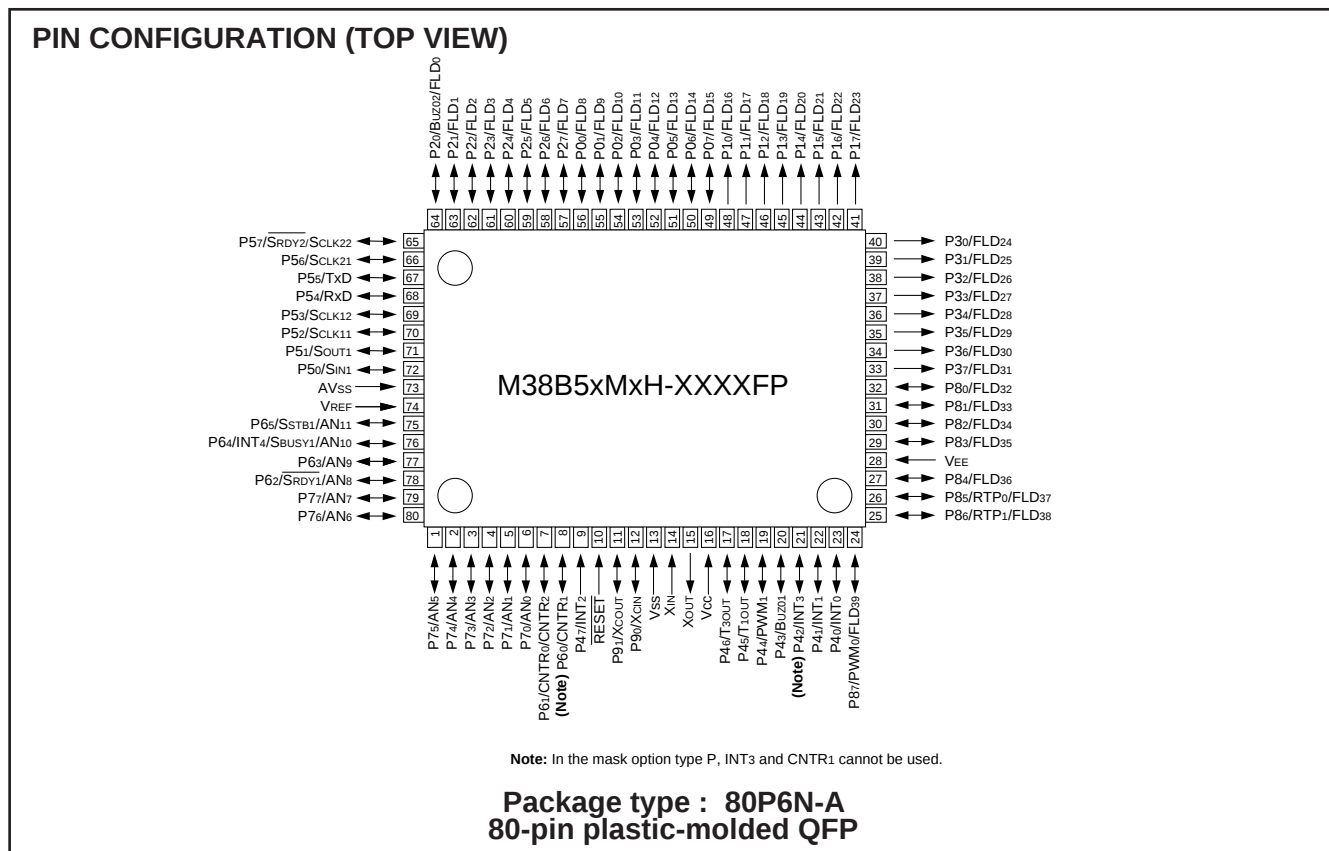


Fig. 1 Pin configuration of M38B5xMxH-XXXXFP

FUNCTIONAL BLOCK

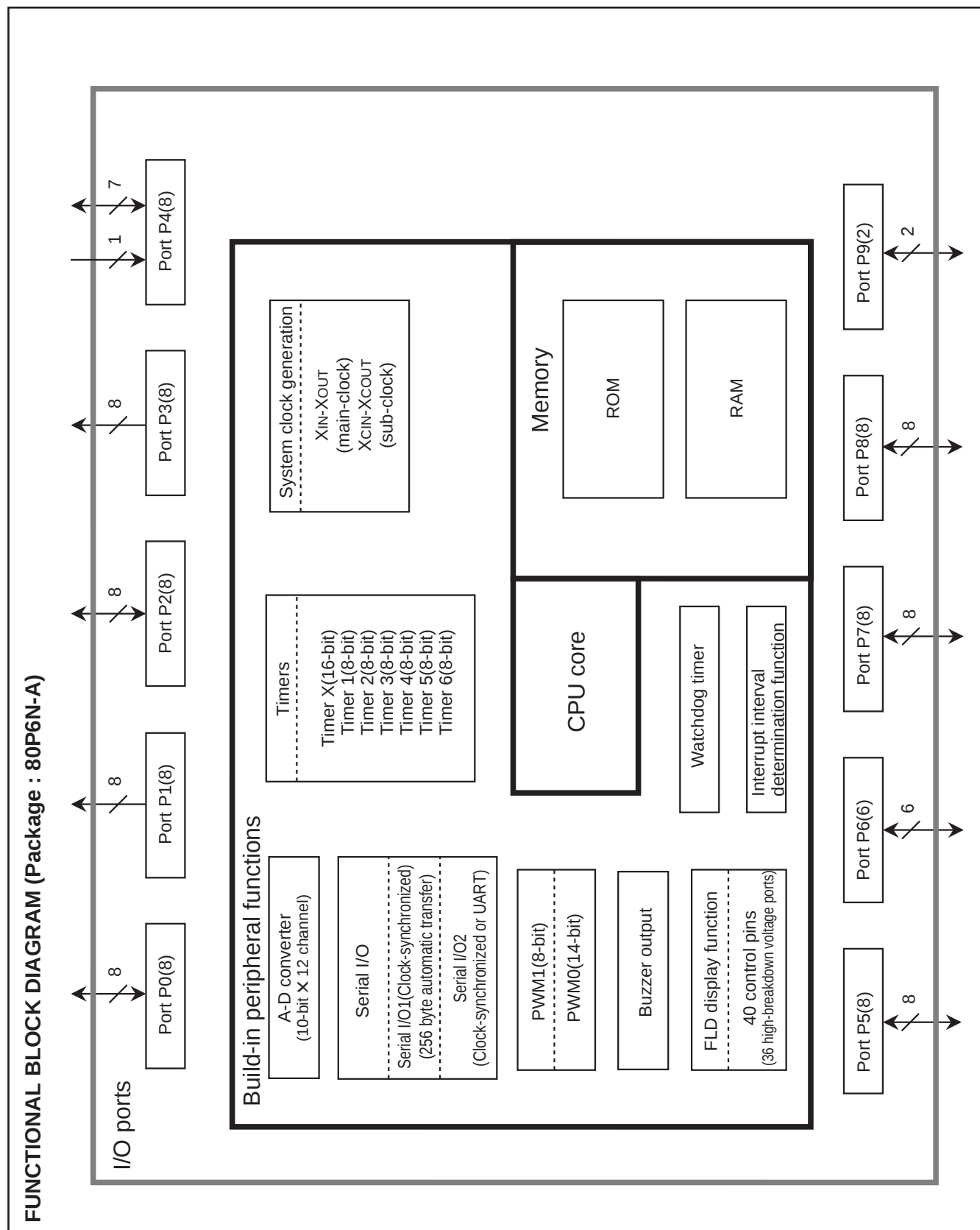


Fig. 2 Functional block diagram

HARDWARE

PIN DESCRIPTION

PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Function	Function except a port function
VCC, VSS	Power source	• Apply voltage of 4.0–5.5 V to VCC, and 0 V to VSS.	
VEE	Pull-down power source	• Apply voltage supplied to pull-down resistors of ports P0, P1, and P3.	
VREF	Reference voltage	• Reference voltage input pin for A-D converter.	
AVSS	Analog power source	• Analog power source input pin for A-D converter. • Connect to VSS.	
RESET	Reset input	• Reset input pin for active “L.”	
XIN	Clock input	• Input and output pins for the main clock generating circuit. • Feedback resistor is built in between XIN pin and XOUT pin.	
XOUT	Clock output	• Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. • When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. • The clock is used as the oscillating source of system clock.	
P00/FLD8– P07/FLD15	I/O port P0	• 8-bit I/O port. • I/O direction register allows each pin to be individually programmed as either input or output. • At reset, this port is set to input mode. • A pull-down resistor is built in between port P0 and the VEE pin. • CMOS compatible input level. • High-breakdown-voltage P-channel open-drain output structure. • At reset, this port is set to VEE level.	• FLD automatic display pins
P10/FLD16– P17/FLD23	Output port P1	• 8-bit output port. • A pull-down resistor is built in between port P1 and the VEE pin. • High-breakdown-voltage P-channel open-drain output structure. • At reset, this port is set to VEE level.	• FLD automatic display pins
P20/BUZ02/ FLD0– P27/FLD7	I/O port P2	• 8-bit I/O port with the same function as port P0. • Low-voltage input level. • High-breakdown-voltage P-channel open-drain output structure.	• FLD automatic display pins • Buzzer output pin (P20)
P30/FLD24– P37/FLD31	Output port P3	• 8-bit output port. • A pull-down resistor is built in between port P3 and the VEE pin. • High-breakdown-voltage P-channel open-drain output structure. • At reset, this port is set to VEE level.	• FLD automatic display pins
P40/INT0, P41/INT1, P42/INT3 P43/BUZ01 P44/PWM1	I/O port P4	• 7-bit I/O port with the same function as port P0. • CMOS compatible input level • N-channel open-drain output structure.	• Interrupt input pins In the mask option type P, INT3 cannot be used.
P45/T1OUT, P46/T3OUT			• Buzzer output pin • PWM output pin (Timer output pin)
P47/INT2	Input port P4	• 1-bit input port. • CMOS compatible input level.	• Interrupt input pin

Table 2 Pin description (2)

Pin	Name	Function	Function except a port function
P50/SIN1, P51/SOUT1, P52/SCLK11, P53/SCLK12	I/O port P5	8-bit CMOS I/O port with the same function as port P0. - CMOS compatible input level. - CMOS 3-state output structure.	Serial I/O1 function pins
P54/RxD, P55/TxD, P56/SCLK21, P57/SRDY2/ SCLK22			Serial I/O2 function pins
P60/CNTR1	I/O port P6	1-bit I/O port with the same function as port P0. - CMOS compatible input level. - N-channel open-drain output structure.	Timer input pin In the mask option type P, CNTR1 cannot be used.
P61/CNTR0/ CNTR2		5-bit CMOS I/O port with the same function as port P0. - CMOS compatible input level. - CMOS 3-state output structure.	Timer I/O pin
P62/SRDY1/ AN8			- Serial I/O1 function pin - A-D conversion input pin
P63/AN9			- A-D conversion input pin - Dimmer signal output pin
P64/INT4/ S8USY1/AN10, P65/SSTB1/ AN11			- Serial I/O1 function pin - A-D conversion input pin - Interrupt input pin (P64)
P70/AN0– P77/AN7	I/O port P7	8-bit CMOS I/O port with the same function as port P0. - CMOS compatible input level. - CMOS 3-state output structure.	A-D conversion input pin
P80/FLD32– P83/FLD35	I/O port P8	4-bit I/O port with the same function as port P0. - Low-voltage input level. - High-breakdown-voltage P-channel open-drain output structure.	FLD automatic display pins
P84/FLD36		4-bit CMOS I/O port with the same function as port P0. - Low-voltage input level. - CMOS 3-state output structure	- FLD automatic display pins - Real time port output
P85/RTP0/ FLD37, P86/RTP1/ FLD38			
P87/PWM0/ FLD39			- FLD automatic display pins 14-bit PWM output
P90/XCIN, P91/XCOUT	I/O port P9	2-bit CMOS I/O port with the same function as port P0. - CMOS compatible input level. - CMOS 3-state output structure.	I/O pins for sub-clock generating circuit (connect a ceramic resonator or a quartz-crystal oscillator)

HARDWARE

PART NUMBERING

PART NUMBERING

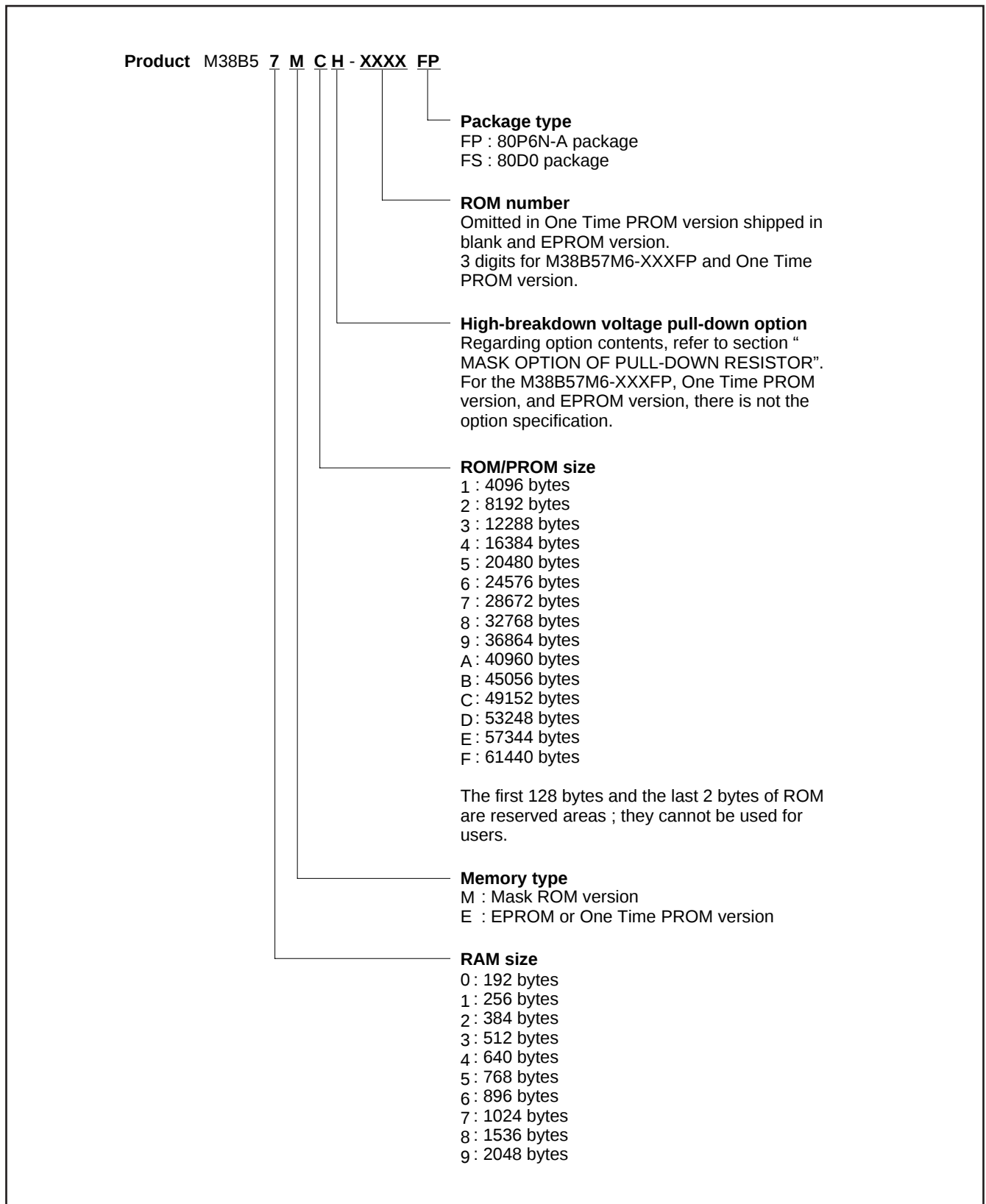


Fig. 3 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 38B5 group as follows:

Memory Type

Support for Mask ROM, One Time PROM and EPROM versions.

Memory Size

ROM/PROM size 24K to 60K bytes

RAM size 1024 to 2048 bytes

Package

80P6N-A 0.8 mm-pitch plastic molded QFP

80D0 0.8 mm-pitch ceramic LCC (EPROM version)

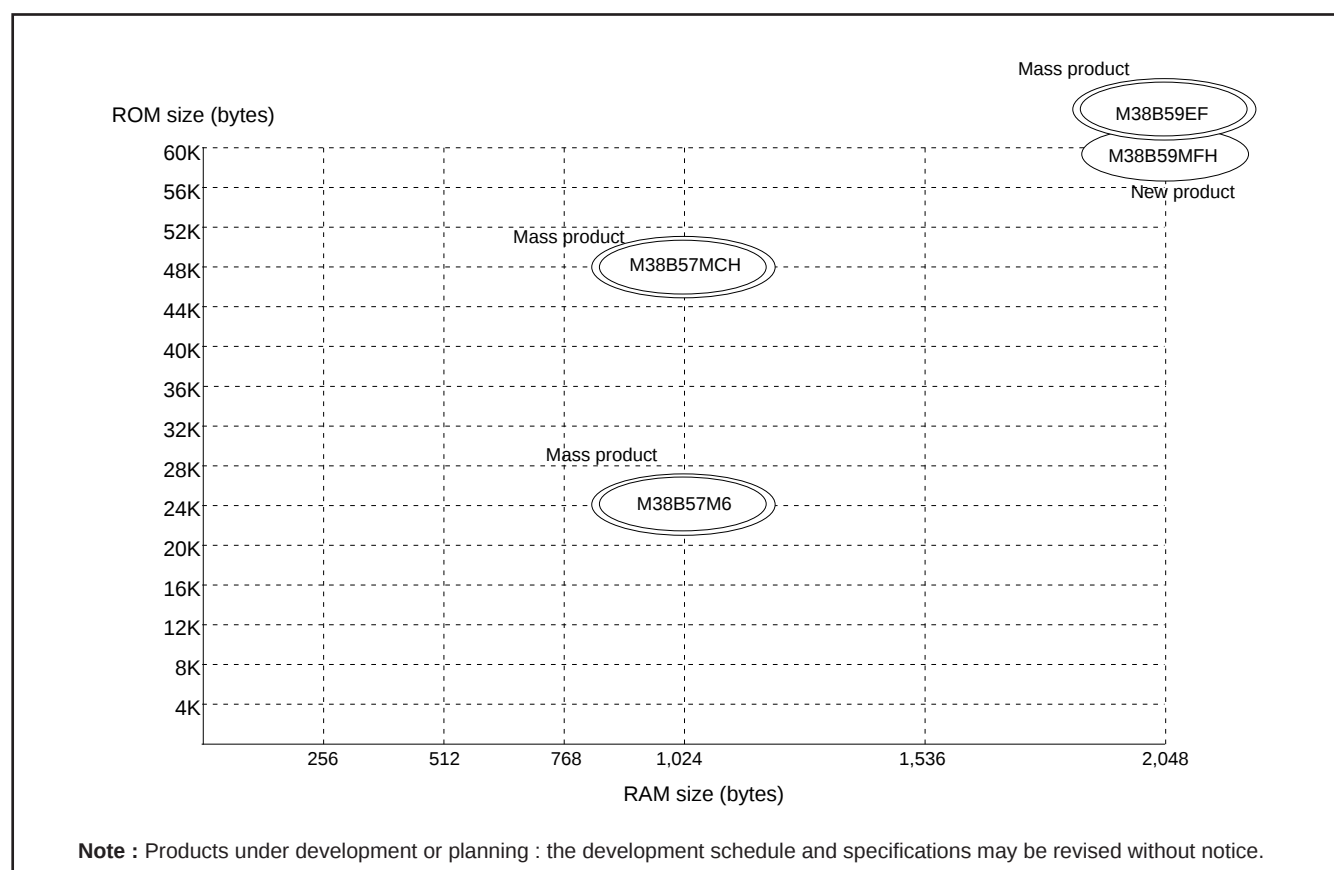


Fig. 4 Memory expansion plan

Currently supported products are listed below.

Table 3 List of supported products

As of Nov. 1998

Product	(P) ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M38B57M6-XXXXFP	24576 (24446)	1024	80P6N-A	Mask ROM version Corresponded to mask option
M38B57MCH-XXXXFP	49152 (49022)	1024	80P6N-A	Mask ROM version
M38B59MFH-XXXXFP	61440 (61310)	2048	80P6N-A	Mask ROM version Corresponded to mask option
M38B59EF-XXXXFP	61440 (61310)	2048	80P6N-A	One Time PROM version
M38B59EFFP	61440 (61310)	2048	80P6N-A	One Time PROM version (blank)
M38B59EFFS	61440 (61310)	2048	80D0	EPROM version

HARDWARE

FUNCTIONAL DESCRIPTION

FUNCTIONAL DESCRIPTION Central Processing Unit (CPU)

The 38B5 group uses the standard 740 Family instruction set. Refer to the table of 740 Series addressing modes and machine instructions or the 740 Series Software Manual for details on the instruction set.

Machine-resident 740 Series instructions are as follows:

- The FST and SLW instructions cannot be used.
- The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts. The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0”, the high-order 8 bits becomes “00₁₆”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01₁₆”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

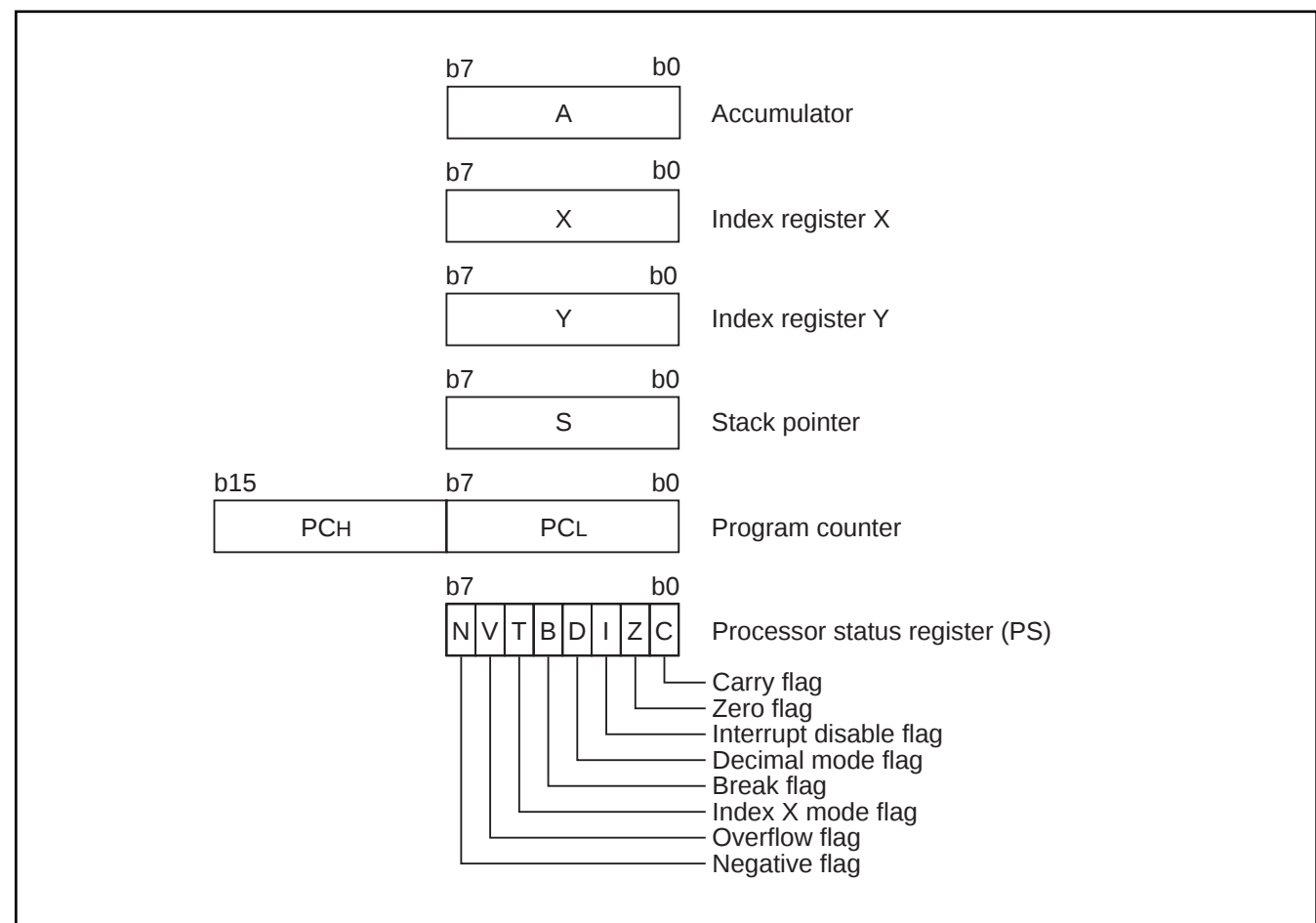


Fig. 5 740 Family CPU register structure

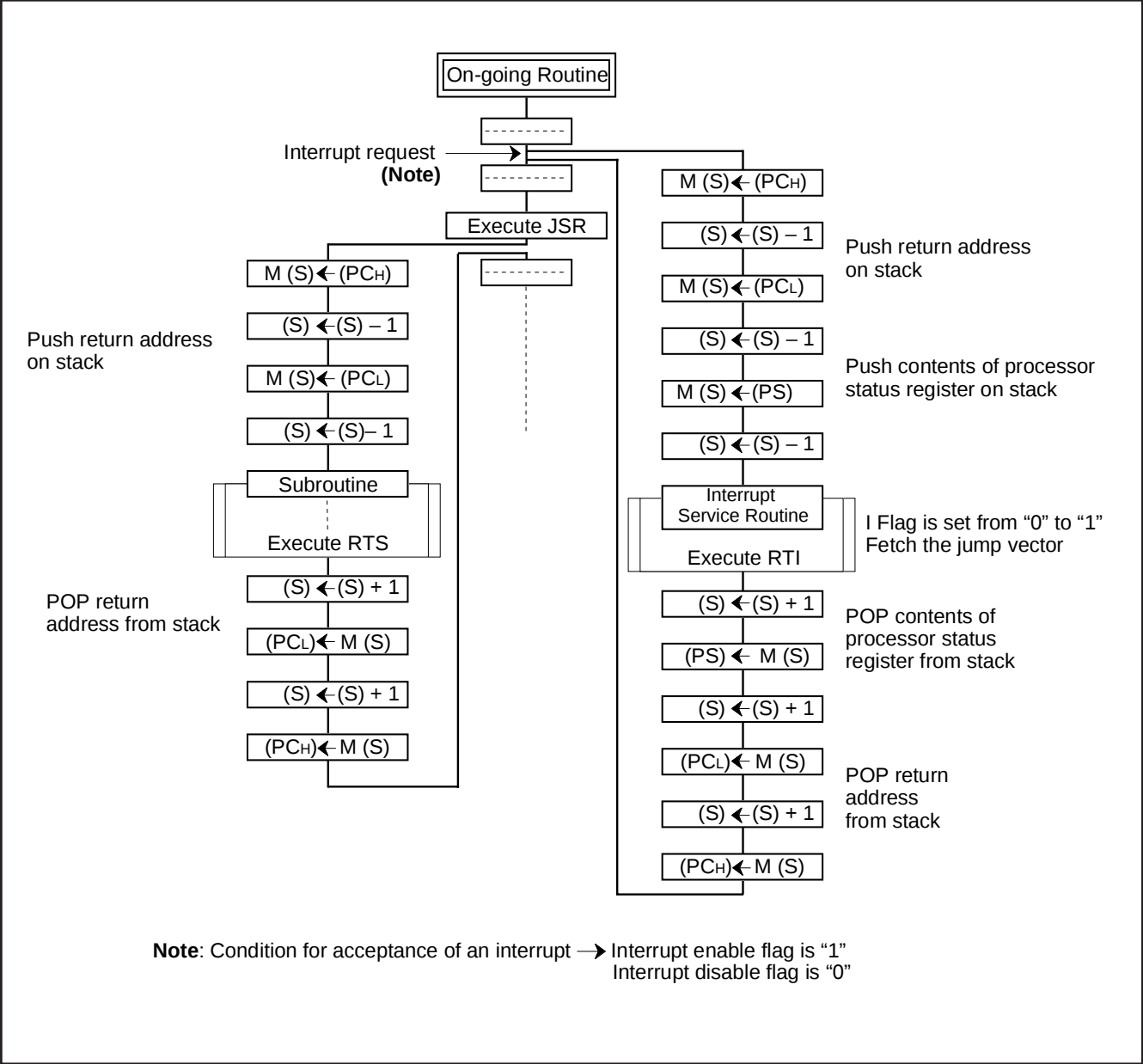


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

HARDWARE

FUNCTIONAL DESCRIPTION

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

•Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is "1".

•Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1". Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

•Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".

•Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	—	SEI	SED	—	SET	—	—
Clear instruction	CLC	—	CLI	CLD	—	CLT	CLV	—

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the internal system clock selection bit etc.

The CPU mode register is allocated at address 003B16.

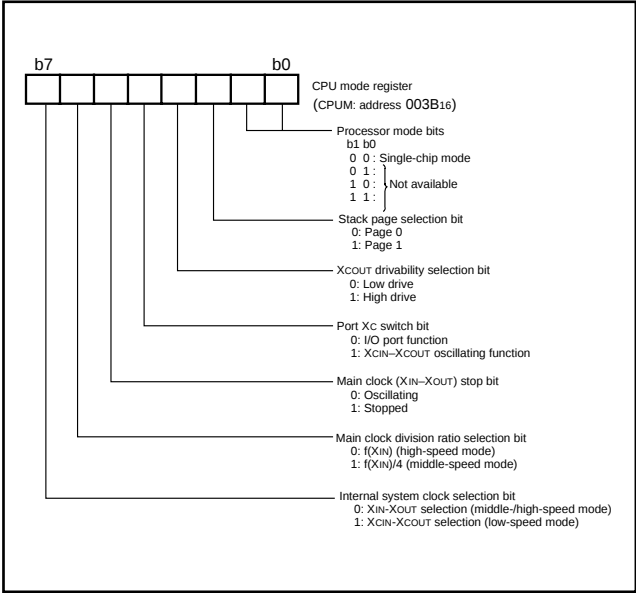


Fig. 7 Structure of CPU mode register

HARDWARE

FUNCTIONAL DESCRIPTION

Memory

Special function register (SFR) area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing, and the other areas are user areas for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

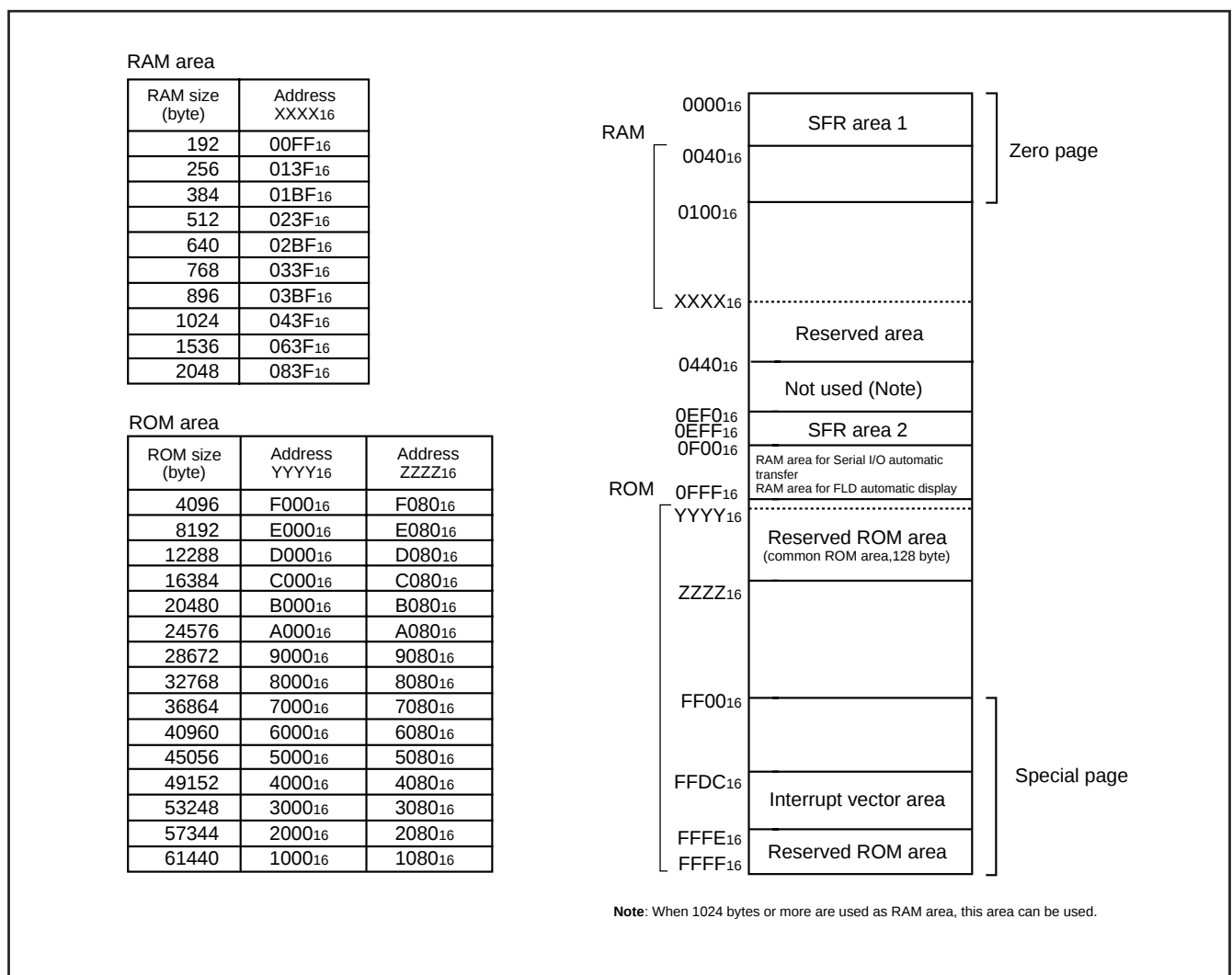


Fig. 8 Memory map diagram

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Timer 1 (T1)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	Timer 2 (T2)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 3 (T3)
0003 ₁₆		0023 ₁₆	Timer 4 (T4)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer 5 (T5)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer 6 (T6)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	PWM control register (PWMCON)
0007 ₁₆		0027 ₁₆	Timer 6 PWM register (T6PWM)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer 12 mode register (T12M)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Timer 34 mode register (T34M)
000A ₁₆	Port P5 (P5)	002A ₁₆	Timer 56 mode register (T56M)
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	Watchdog timer control register (WDTCON)
000C ₁₆	Port P6 (P6)	002C ₁₆	Timer X (low-order) (TXL)
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	Timer X (high-order) (TXH)
000E ₁₆	Port P7 (P7)	002E ₁₆	Timer X mode register 1 (TXM1)
000F ₁₆	Port P7 direction register (P7D)	002F ₁₆	Timer X mode register 2 (TXM2)
0010 ₁₆	Port P8 (P8)	0030 ₁₆	Interrupt interval determination register (IID)
0011 ₁₆	Port P8 direction register (P8D)	0031 ₁₆	Interrupt interval determination control register (IIDCON)
0012 ₁₆	Port P9 (P9)	0032 ₁₆	A-D control register (ADCON)
0013 ₁₆	Port P9 direction register (P9D)	0033 ₁₆	A-D conversion register (low-order) (ADL)
0014 ₁₆	PWM register (high-order) (PWMH)	0034 ₁₆	A-D conversion register (high-order) (ADH)
0015 ₁₆	PWM register (low-order) (PWM L)	0035 ₁₆	
0016 ₁₆	Baud rate generator (BRG)	0036 ₁₆	
0017 ₁₆	UART control register (UARTCON)	0037 ₁₆	
0018 ₁₆	Serial I/O1 automatic transfer data pointer (SIO1DP)	0038 ₁₆	
0019 ₁₆	Serial I/O1 control register 1 (SIO1CON1)	0039 ₁₆	Interrupt source switch register (IFR)
001A ₁₆	Serial I/O1 control register 2 (SIO1CON2)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	Serial I/O1 register/Transfer counter (SIO1)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Serial I/O1 control register 3 (SIO1CON3)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	Serial I/O2 control register (SIO2CON)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆	Serial I/O2 status register (SIO2STS)	003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	Serial I/O2 transmit/receive buffer register (TB/RB)	003F ₁₆	Interrupt control register 2 (ICON2)
0EF0 ₁₆	Pull-up control register 1 (PULL1)	0EF8 ₁₆	FLD data pointer (FLDDP)
0EF1 ₁₆	Pull-up control register 2 (PULL2)	0EF9 ₁₆	Port P0FLD/port switch register (P0FPR)
0EF2 ₁₆	P1FLDRAM write disable register (P1FLDRAM)	0EFA ₁₆	Port P2FLD/port switch register (P2FPR)
0EF3 ₁₆	P3FLDRAM write disable register (P3FLDRAM)	0EFB ₁₆	Port P8FLD/port switch register (P8FPR)
0EF4 ₁₆	FLDC mode register (FLDM)	0EFC ₁₆	Port P8FLD output control register (P8FLDCON)
0EF5 ₁₆	Tdisp time set register (TDISP)	0EFD ₁₆	Buzzer output control register (BUZCON)
0EF6 ₁₆	Toff1 time set register (TOFF1)	0EFE ₁₆	
0EF7 ₁₆	Toff2 time set register (TOFF2)	0EFF ₁₆	

Fig. 9 Memory map of special function register (SFR)

HARDWARE

FUNCTIONAL DESCRIPTION

I/O Ports

[Direction Registers] PiD

The 38B5 group has 55 programmable I/O pins arranged in eight individual I/O ports (P0, P2, P4₀–P4₆, and P5–P9). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port. When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that pin, that pin becomes an output pin. If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input (the bit corresponding to that pin must be set to “0”) are floating and the value of that pin can be read. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

[High-Breakdown-Voltage Output Ports]

The 38B5 group has 5 ports with high-breakdown-voltage pins (ports P0–P3 and P8₀–P8₃). The high-breakdown-voltage ports have P-channel open-drain output with V_{CC}- 45 V of breakdown voltage. Each pin in ports P0, P1, and P3 has an internal pull-down resistor connected to V_{EE}. At reset, the P-channel output transistor of each port latch is turned off, so that it goes to V_{EE} level (“L”) by the pull-down resistor.

Writing “1” (weak drivability) to bit 7 of the FLDC mode register (address 0EF4₁₆) shows the rising transition of the output transistors for reducing transient noise. At reset, bit 7 of the FLDC mode register is set to “0” (strong drivability).

[Pull-up Control Register] PULL

Ports P5, P6₁–P6₅, P7, P8₄–P8₇ and P9 have built-in programmable pull-up resistors. The pull-up resistors are valid only in the case that the each control bit is set to “1” and the corresponding port direction registers are set to input mode.

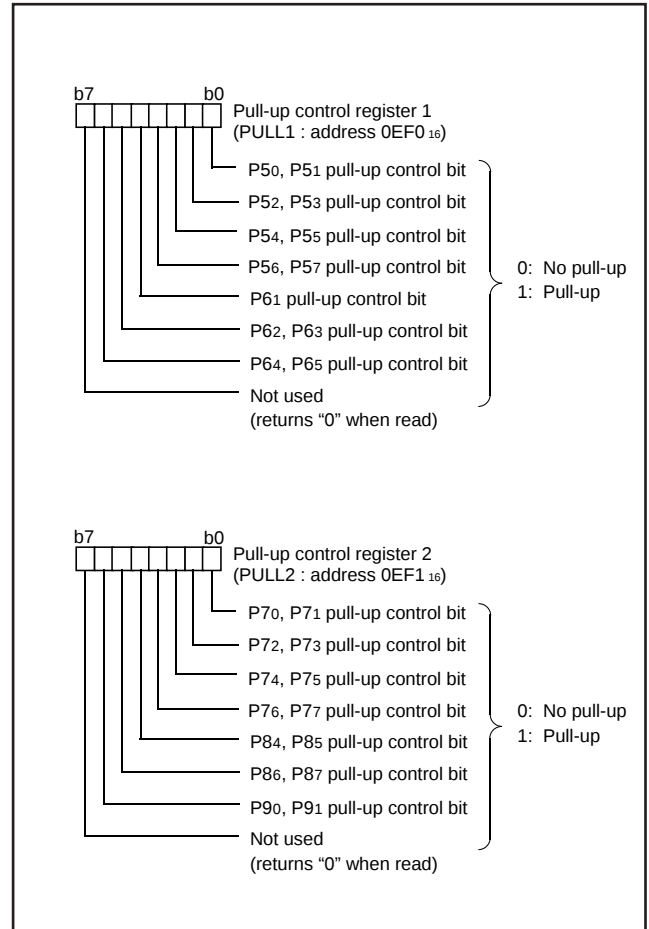


Fig. 10 Structure of pull-up control registers (PULL1 and PULL2)

Table 6 List of I/O port functions (1)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
P00/FLD8– P07/FLD15	Port P0	Input/output, individual bits	CMOS compatible input level High-breakdown voltage P- channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Port P0FLD/port switch register	(1)
P10/FLD16– P17/FLD23	Port P1	Output	High-breakdown voltage P- channel open-drain output with pull-down resistor		FLDC mode register	(2)
P20/BUZ02/ FLD0	Port P2	Input/output, individual bits	Low-voltage input level High-breakdown voltage P- channel open-drain output	Buzzer output (P20) FLD automatic display function	FLDC mode register Port P2FLD/port switch register	(3)
P21/FLD1– P27/FLD7				FLD automatic display function	Buzzer output control register	(1)
P30/FLD24– P37/FLD31	Port P3	Output	High-breakdown voltage P- channel open-drain output with pull-down resistor		FLDC mode register	(2)
P40/INT0, P41/INT1, P42/INT3	Port P4	Input/output, individual bits	CMOS compatible input level N-channel open-drain output	External interrupt input In the mask option type P, INT3 cannot be used.	Interrupt edge selection register	(5-1) (5-2)
P43/BUZ01				Buzzer output	Buzzer output control register	(4)
P44/PWM1				PWM output	Timer 56 mode register	(6)
P45/T1OUT				Timer output	Timer 12 mode register	(7)
P46/T3OUT				Timer output	Timer 34 mode register	(7)
P47/INT2		Input	CMOS compatible input level	External interrupt input	Interrupt edge selection register Interrupt interval determination control register	(8)
P50/SIN1 P51/SOUT1, P52/SCLK11, P53/SCLK12	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O1 function I/O	Serial I/O1 control register 1, 2	(9) (10)
P54/RxD, P55/TxD, P56/SCLK21 P57/SRDY2/ SCLK22				Serial I/O2 function I/O	Serial I/O2 control register UART control register	(9) (10) (11)
P60/CNTR1 P61/CNTR0/ CNTR2	Port P6		CMOS compatible input level N-channel open-drain output CMOS compatible input level CMOS 3-state output	External count input In the mask option type P, CNTR1 cannot be used.	Interrupt edge selection register	(5-1) (5-2) (12)
P62/SRDY1/ AN8 P63/AN9				Serial I/O1 function I/O A-D conversion input	Serial I/O1 control register 1, 2 A-D control register	(13)
P64/INT4/ SBUSY1/AN10				A-D conversion input Dimmer signal output	A-D control register P8FLD output control bit	(14)
P65/SSTB1/ AN11				Serial I/O1 function I/O A-D conversion input External interrupt input	Serial I/O1 control register 1, 2 A-D control register Interrupt edge selection register	(15)
P70/AN0– P77/AN7	Port P7			Serial I/O1 function I/O A-D conversion input	Serial I/O1 control register 1, 2 A-D control register	(16)
				A-D conversion input	A-D control register	(14)

HARDWARE

FUNCTIONAL DESCRIPTION

Table 7 List of I/O port functions (2)

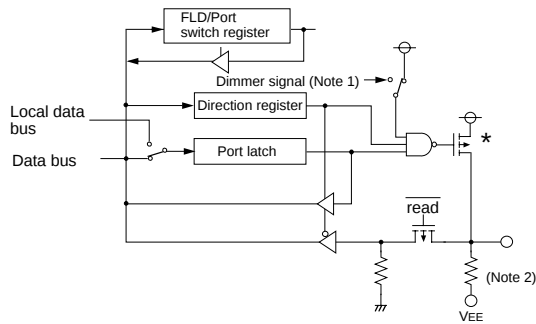
Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
P80/FLD32– P83/FLD35	Port P8	Input/output, individual bits	Low-voltage input level High-breakdown voltage P- channel open-drain output	FLD automatic display function	FLDC mode register Port P8FLD/port switch register	(1)
P84/FLD36			Low-voltage input level			(17)
P85/RTP0/ FLD37, P86/RTP1/ FLD38			CMOS 3-state output	FLD automatic display function Real time port output	FLDC mode register Port P8FLD/port switch register Timer X mode register 2	(18)
P87/PWM0/ FLD39				FLD automatic display function PWM output	FLDC mode register Port P8FLD/port switch register PWM control register	(19)
P90/XCIN			Port P9	CMOS compatible input level	Sub-clock generating circuit I/O	CPU mode register
P91/XCOUT	CMOS 3-state output	(21)				

Notes 1 : How to use double-function ports as function I/O ports, refer to the applicable sections.

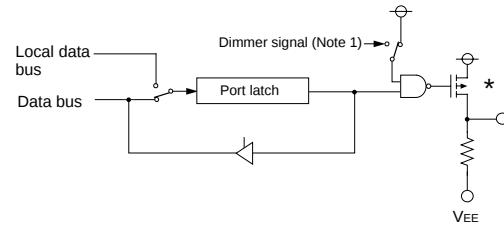
2 : Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction.

When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

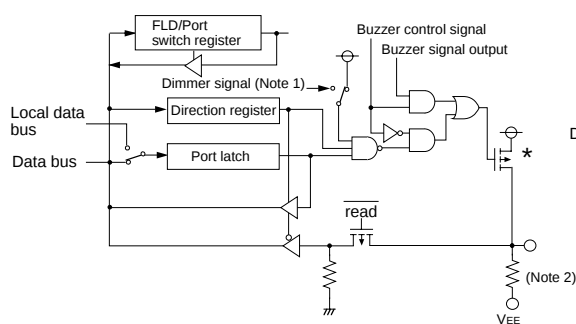
(1) Ports P0, P21–P27, P80–P83



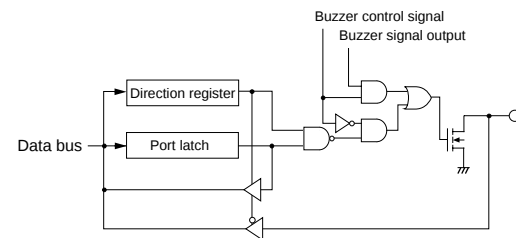
(2) Ports P1, P3



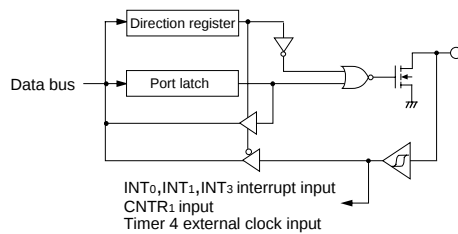
(3) Port P20



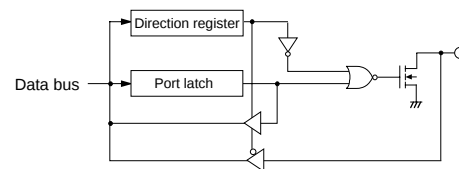
(4) Port P43



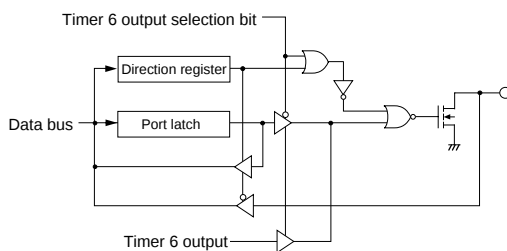
(5-1) Ports P40–P42, P60



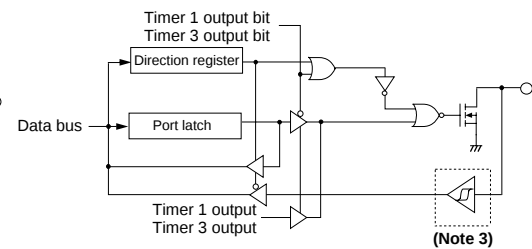
(5-2) Ports P42, P60 (in mask option type P)



(6) Port P44



(7) Ports P45, P46



* High-breakdown-voltage P-channel transistor

Notes 1: The dimmer signal sets the Toff timing.

2: A pull-down resistor is not built in to ports P2 and P8.

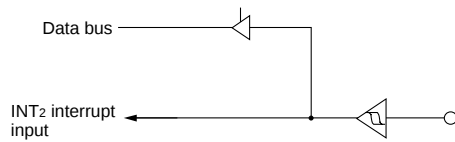
3: In the mask option type P, the hysteresis circuit of  part is not built-in.

Fig. 11 Port block diagram (1)

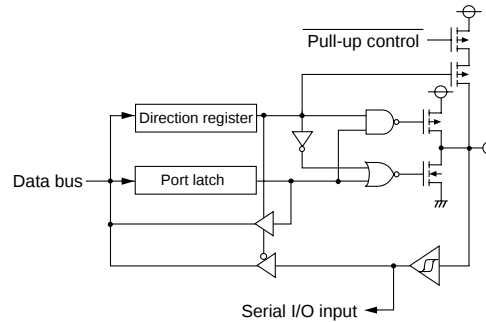
HARDWARE

FUNCTIONAL DESCRIPTION

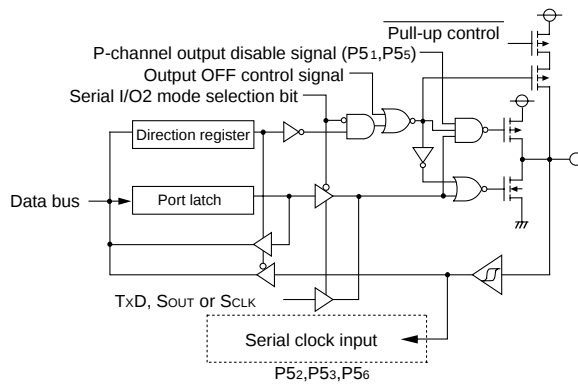
(8) Port P47



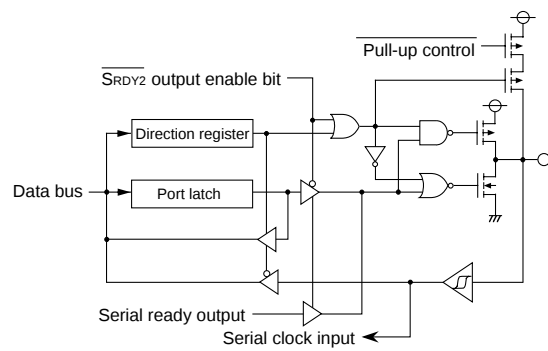
(9) Ports P50, P54



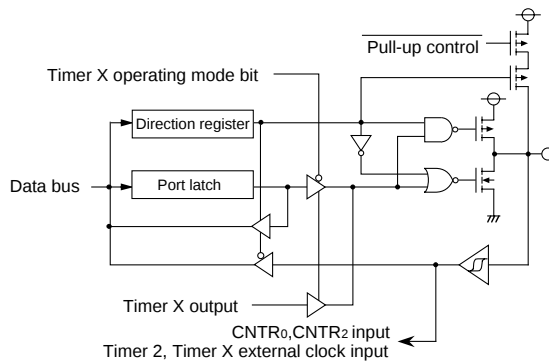
(10) Ports P51–P53, P55, P56



(11) Port P57



(12) Port P61



(13) Port P62

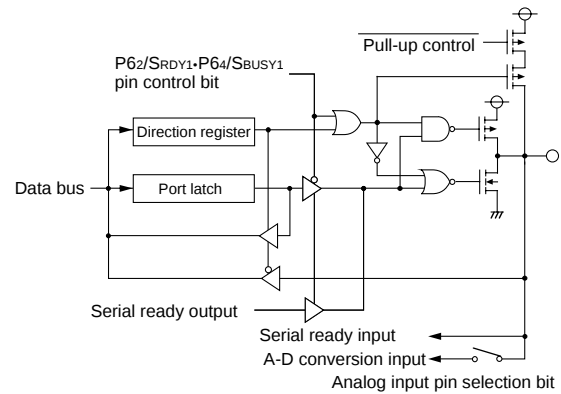
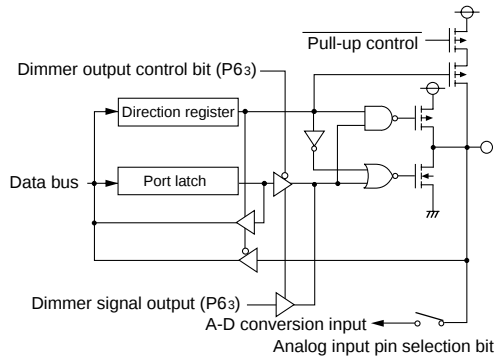
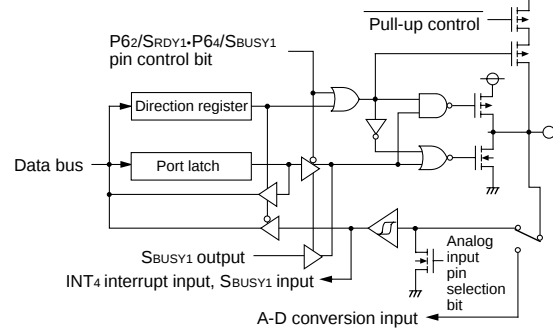


Fig. 12 Port block diagram (2)

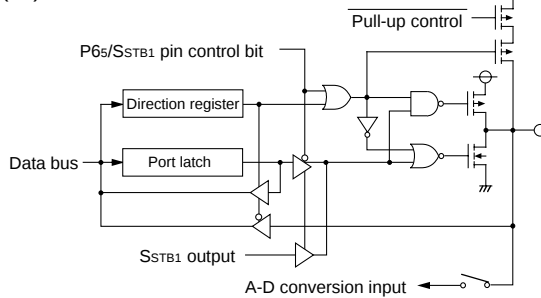
(14) Ports P63, P7



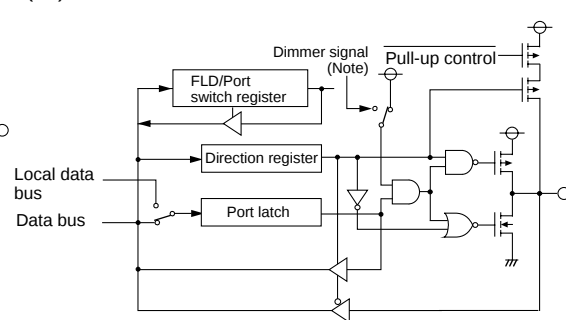
(15) Port P64



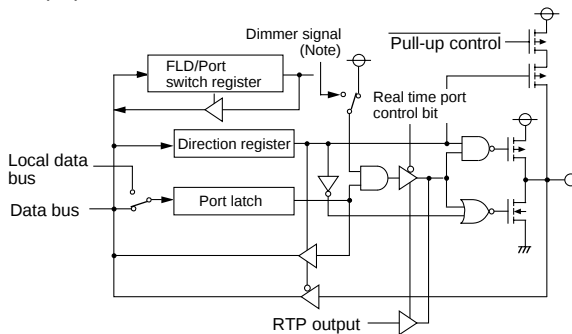
(16) Port P65



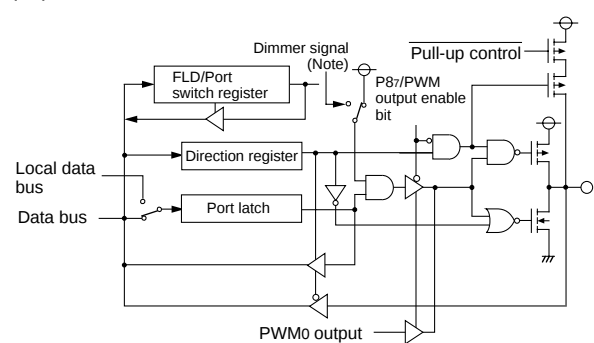
(17) Port P84



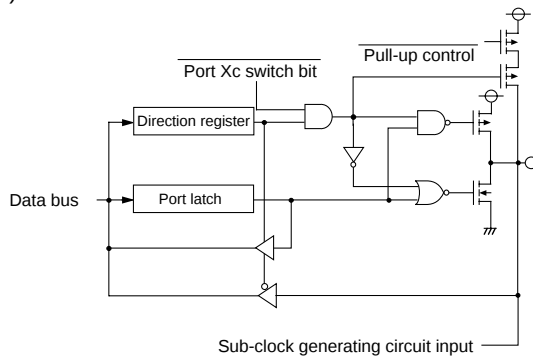
(18) Ports P85, P86



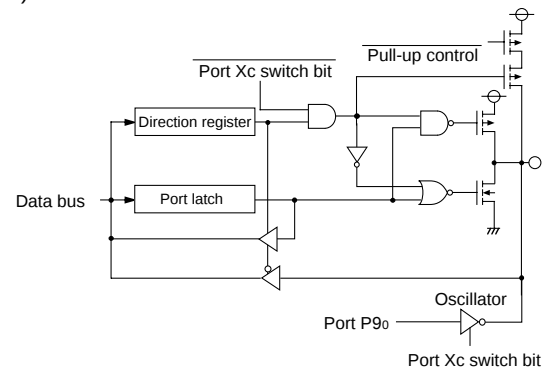
(19) Port P87



(20) Port P90



(21) Port P91



* High-breakdown-voltage P-channel transistor
Note: The dimmer signal sets the Toff timing.

Fig. 13 Port block diagram (3)

HARDWARE

FUNCTIONAL DESCRIPTION

Interrupts

Interrupts occur by twenty one sources: five external, fifteen internal, and one software.

(1) Interrupt Control

Each interrupt except the BRK instruction interrupt have both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0." Interrupt enable bits can be set or cleared by software. Interrupt request bits can be cleared by software, but cannot be set by software. The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupts requests occurs at the same time the interrupt with highest priority is accepted first.

(2) Interrupt Operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The contents of the program counter and processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■Notes on Use

When the active edge of an external interrupt (INT0–INT4) is set or when switching interrupt sources in the same vector address, the corresponding interrupt request bit may also be set. Therefore, please take following sequence:

- (1) Disable the external interrupt which is selected.
- (2) Change the active edge in interrupt edge selection register
- (3) Clear the set interrupt request bit to "0."
- (4) Enable the external interrupt which is selected.

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
INT ₀	2	FFFB ₁₆	FFFA ₁₆	At detection of either rising or falling edge of INT ₀ input	External interrupt (active edge selectable)
INT ₁	3	FFF9 ₁₆	FFF8 ₁₆	At detection of either rising or falling edge of INT ₁ input	External interrupt (active edge selectable)
INT ₂	4	FFF7 ₁₆	FFF6 ₁₆	At detection of either rising or falling edge of INT ₂ input	External interrupt (active edge selectable)
Remote control/counter overflow				At 8-bit counter overflow	Valid when interrupt interval determination is operating
Serial I/O1	5	FFF5 ₁₆	FFF4 ₁₆	At completion of data transfer	Valid when serial I/O ordinary mode is selected
Serial I/O automatic transfer				At completion of the last data transfer	Valid when serial I/O automatic transfer mode is selected
Timer X	6	FFF3 ₁₆	FFF2 ₁₆	At timer X underflow	
Timer 1	7	FFF1 ₁₆	FFF0 ₁₆	At timer 1 underflow	
Timer 2	8	FFEF ₁₆	FFEE ₁₆	At timer 2 underflow	STP release timer underflow
Timer 3	9	FFED ₁₆	FFEC ₁₆	At timer 3 underflow	
Timer 4	10	FFEB ₁₆	FFEA ₁₆	At timer 4 underflow	(Note 3)
Timer 5	11	FFE9 ₁₆	FFE8 ₁₆	At timer 5 underflow	
Timer 6	12	FFE7 ₁₆	FFE6 ₁₆	At timer 6 underflow	
Serial I/O2 receive	13	FFE5 ₁₆	FFE4 ₁₆	At completion of serial I/O2 data receive	
INT ₃	14	FFE3 ₁₆	FFE2 ₁₆	At detection of either rising or falling edge of INT ₃ input	External interrupt (Note 4) (active edge selectable)
Serial I/O2 transmit				At completion of serial I/O2 data transmit	
INT ₄	15	FFE1 ₁₆	FFE0 ₁₆	At detection of either rising or falling edge of INT ₄ input	External interrupt (active edge selectable) Valid when INT ₄ interrupt is selected
A-D conversion				At completion of A-D conversion	Valid when A-D conversion is selected
FLD blanking	16	FFDF ₁₆	FFDE ₁₆	At falling edge of the last timing immediately before blanking period starts	Valid when FLD blanking interrupt is selected
FLD digit				At rising edge of digit (each timing)	Valid when FLD digit interrupt is selected
BRK instruction	17	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Notes 1 : Vector addresses contain interrupt jump destination addresses.

2 : Reset function in the same way as an interrupt with the highest priority.

3 : In the mask option type P, timer 4 interrupt whose count source is CNTR₁ input cannot be used.

4 : In the mask option type P, INT₃ interrupt cannot be used.

HARDWARE

FUNCTIONAL DESCRIPTION

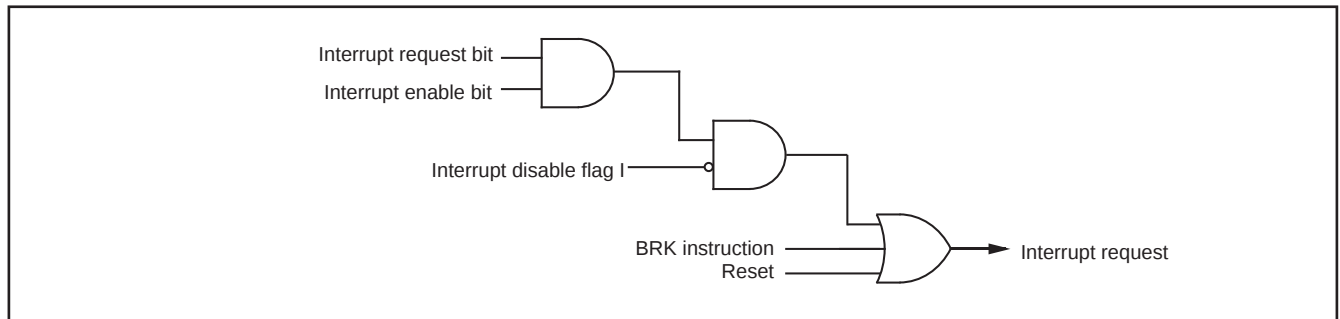


Fig. 14 Interrupt control

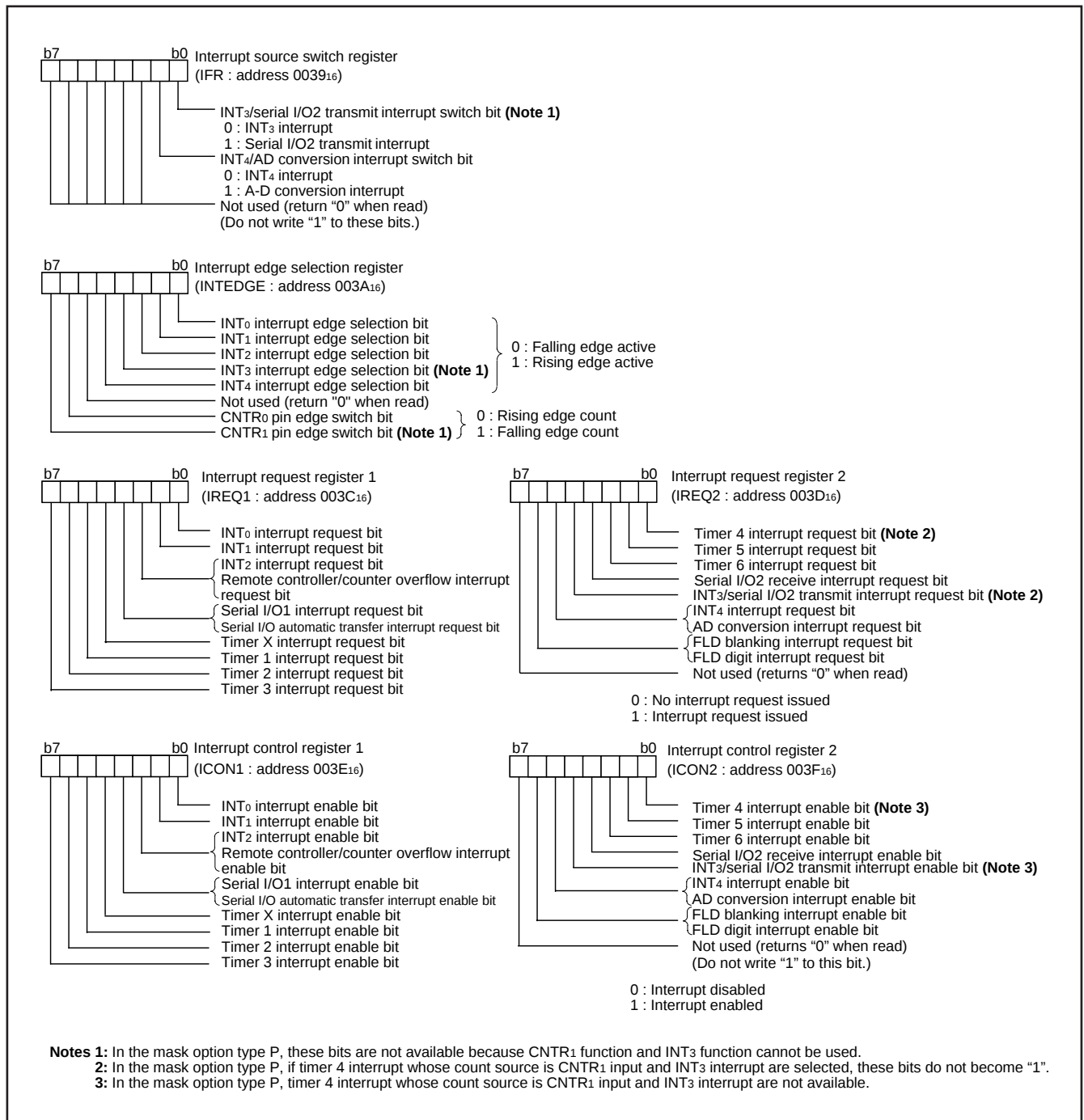


Fig. 15 Structure of interrupt related registers

Timers

8-Bit Timer

The 38B5 group has six built-in timers : Timer 1, Timer 2, Timer 3, Timer 4, Timer 5, and Timer 6.

Each timer has the 8-bit timer latch. All timers are down-counters. When the timer reaches "00₁₆," an underflow occurs with the next count pulse. Then the contents of the timer latch is reloaded into the timer and the timer continues down-counting. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1."

The count can be stopped by setting the stop bit of each timer to "1." The internal system clock can be set to either the high-speed mode or low-speed mode with the CPU mode register. At the same time, timer internal count source is switched to either $f(X_{IN})$ or $f(X_{CIN})$.

●Timer 1, Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register. A rectangular waveform of timer 1 underflow signal divided by 2 can be output from the P4₅/T1_{OUT} pin. The active edge of the external clock CNTR₀ can be switched with the bit 6 of the interrupt edge selection register.

At reset or when executing the STP instruction, all bits of the timer 12 mode register are cleared to "0," timer 1 is set to "FF₁₆," and timer 2 is set to "01₁₆."

●Timer 3, Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. A rectangular waveform of timer 3 underflow signal divided by 2 can be output from the P4₆/T3_{OUT} pin. The active edge of the external clock CNTR₁ (**Note**) can be switched with the bit 7 of the interrupt edge selection register.

Note: In the mask option type P, CNTR₁ function cannot be used.

●Timer 5, Timer 6

The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register. A rectangular waveform of timer 6 underflow signal divided by 2 can be output from the P4₄/PWM₁ pin.

●Timer 6 PWM1 Mode

Timer 6 can output a PWM rectangular waveform with "H" duty cycle $n/(n+m)$ from the P4₄/PWM₁ pin by setting the timer 56 mode register (refer to Figure 18). The n is the value set in timer 6 latch (address 0025₁₆) and m is the value in the timer 6 PWM register (address 0027₁₆). If n is "0," the PWM output is "L," if m is "0," the PWM output is "H" ($n = 0$ is prior than $m = 0$). In the PWM mode, interrupts occur at the rising edge of the PWM output.

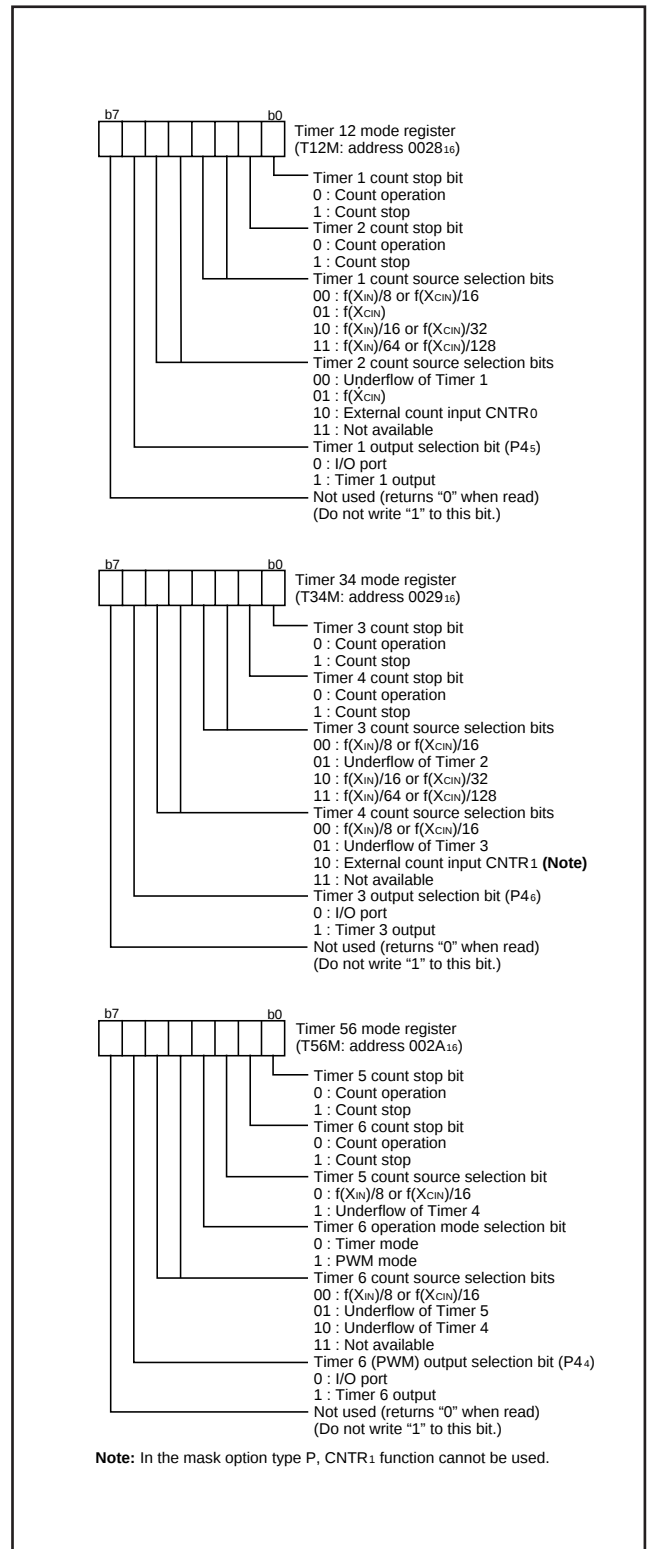


Fig. 16 Structure of timer related register

HARDWARE

FUNCTIONAL DESCRIPTION

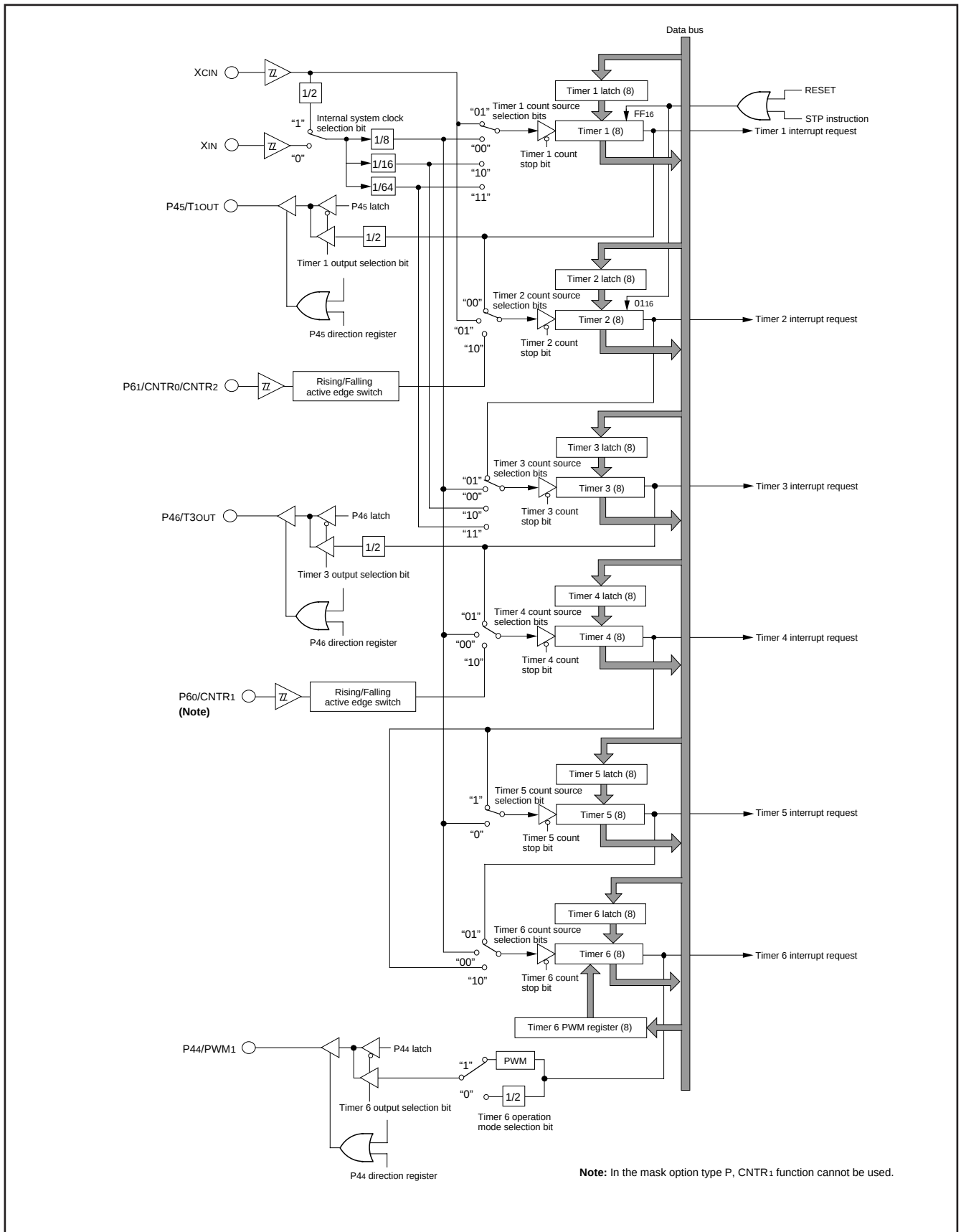
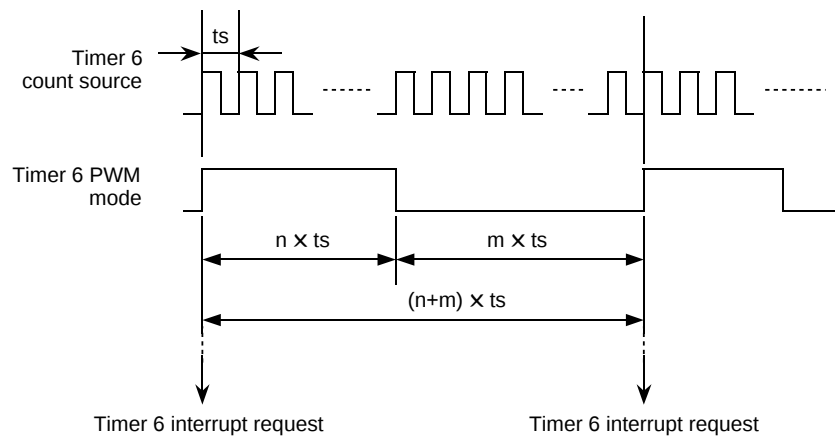


Fig. 17 Block diagram of timer



Note: PWM waveform (duty : $n/(n + m)$ and period: $(n + m) \times ts$) is output.
 n : setting value of Timer 6
 m : setting value of Timer 6 PWM register
 ts : period of Timer 6 count source

Fig. 18 Timing chart of timer 6 PWM1 mode

HARDWARE

FUNCTIONAL DESCRIPTION

16-Bit Timer

Timer X is a 16-bit timer that can be selected in one of four modes by the Timer X mode registers 1, 2 and can be controlled the timer X write and the real time port by setting the timer X mode registers.

Read and write operation on 16-bit timer must be performed for both high- and low-order bytes. When reading a 16-bit timer, read from the high-order byte first. When writing to 16-bit timer, write to the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during write operation, or when writing during read operation.

●Timer X

Timer X is a down-counter. When the timer reaches “0000₁₆,” an underflow occurs with the next count pulse. Then the contents of the timer latch is reloaded into the timer and the timer continues down-counting. When a timer underflows, the interrupt request bit corresponding to that timer is set to “1.”

(1) Timer mode

A count source can be selected by setting the Timer X count source selection bits (bits 1 and 2) of the Timer X mode register 1.

(2) Pulse output mode

Each time the timer underflows, a signal output from the CNTR₂ pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the port shared with the CNTR₂ pin to output.

(3) Event counter mode

The timer counts signals input through the CNTR₂ pin. Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the port shared with the CNTR₂ pin to input.

(4) Pulse width measurement mode

A count source can be selected by setting the Timer X count source selection bits (bits 1 and 2) of the Timer X mode register 1. When CNTR₂ active edge switch bit is “0,” the timer counts while the input signal of the CNTR₂ pin is at “H.” When it is “1,” the timer counts while the input signal of the CNTR₂ pin is at “L.” When using a timer in this mode, set the port shared with the CNTR₂ pin to input.

■ Note

•Timer X Write Control

If the timer X write control bit is “0,” when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.

If the timer X write control bit is “1,” when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.

When the value is written in latch only, unexpected value may be set in the high-order counter if the writing in high-order latch and the underflow of timer X are performed at the same timing.

•Real Time Port Control

While the real time port function is valid, data for the real time port are output from ports P8₅ and P8₆ each time the timer X underflows. (However, if the real time port control bit is changed from “0” to “1,” data are output without the timer X.) When the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.

Before using this function, set the corresponding port direction registers to output mode.

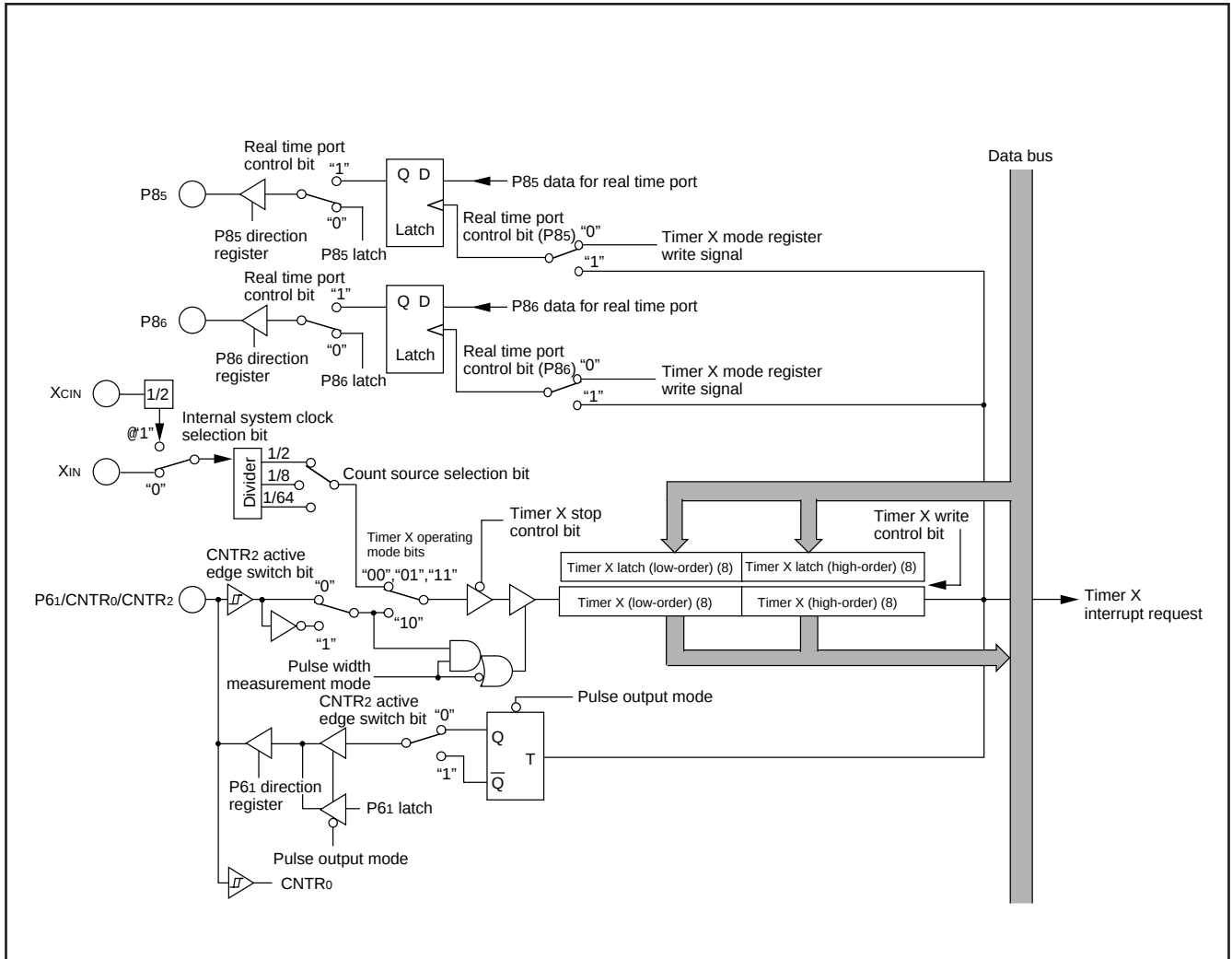


Fig. 19 Block diagram of timer X

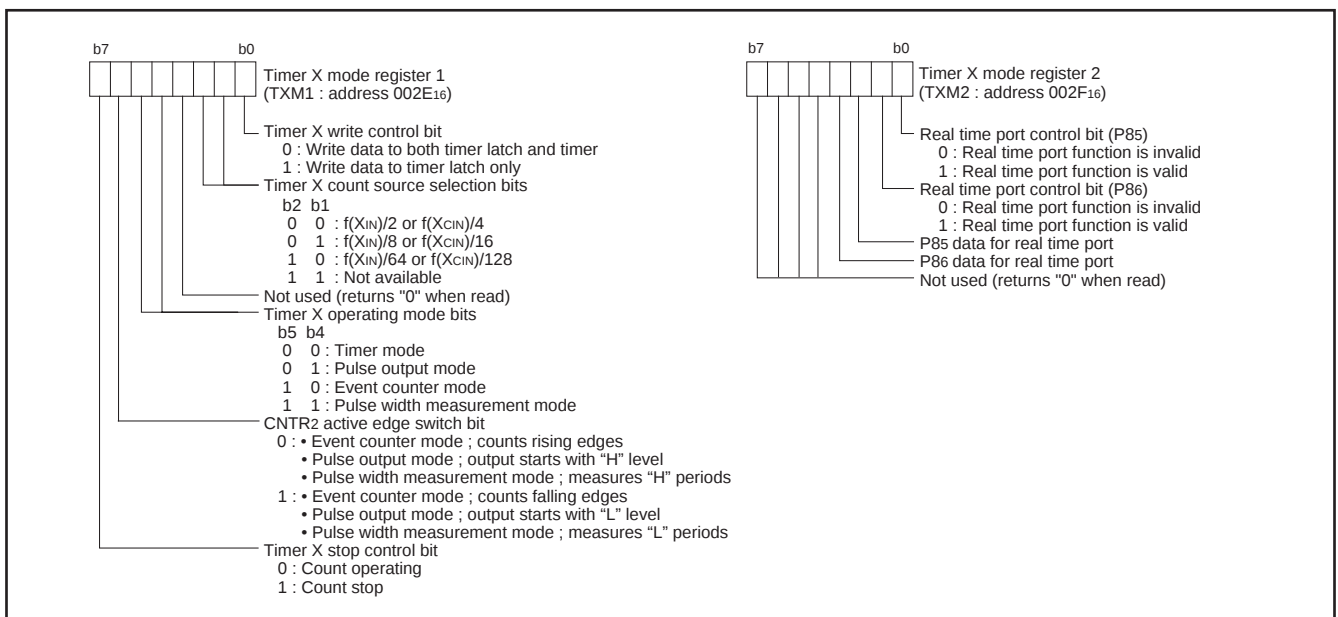


Fig. 20 Structure of timer X related registers

FUNCTIONAL DESCRIPTION

●Serial I/O1

FLD automatic display RAM).

The P62/SRDY1/AN8, P64/INT4/SBUSY1/AN10, and P65/SSTB1/AN11 pins each have a handshake I/O signal function and can select either “H” active or “L” active for active logic.



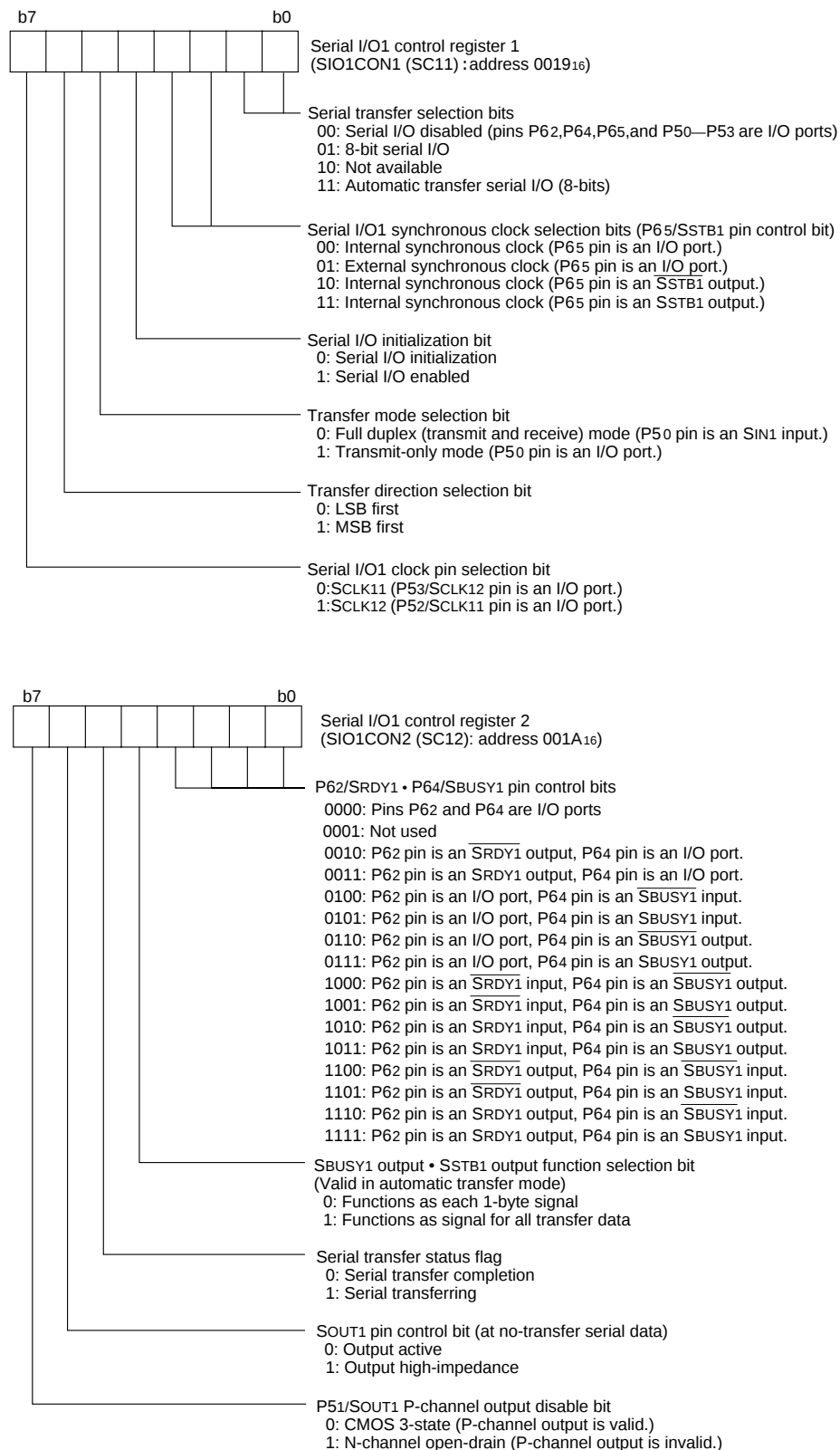


Fig. 22 Structure of serial I/O1 control registers 1, 2

HARDWARE

FUNCTIONAL DESCRIPTION

(1) Serial I/O1 Operation

Either the internal synchronous clock or external synchronous clock can be selected by the serial I/O1 synchronous clock selection bits (b2 and b3 of address 0019₁₆) of serial I/O1 control register 1 as synchronous clock for serial transfer.

The internal synchronous clock has a built-in dedicated divider where 7 different clocks are selected by the internal synchronous clock selection bits (b5, b6 and b7 of address 001C₁₆) of serial I/O1 control register 3.

The P62/SRDY1/AN8, P64/INT4/SBUSY1/AN10, and P65/SSTB1/AN11 pins each select either I/O port or handshake I/O signal by the serial I/O1 synchronous clock selection bits (b2 and b3 of address 0019₁₆) of serial I/O1 control register 1 as well as the P62/SRDY1 • P64/SBUSY1 pin control bits (b0 to b3 of address 001A₁₆) of serial I/O1 control register 2.

For the SOUT1 being used as an output pin, either CMOS output or N-channel open-drain output is selected by the P51/SOUT1 P-channel output disable bit (b7 of address 001A₁₆) of serial I/O1 control register 2.

Either output active or high-impedance can be selected as a SOUT1 pin state at serial non-transfer by the SOUT1 pin control bit (b6 of address 001A₁₆) of serial I/O1 control register 2. However, when the external synchronous clock is selected, perform the following setup to put the SOUT1 pin into a high-impedance state.

When the SCLK1 input is “H” after completion of transfer, set the SOUT1 pin control bit to “1.”

When the SCLK1 input goes to “L” after the start of the next serial transfer, the SOUT1 pin control bit is automatically reset to “0” and put into an output active state.

Regardless of whether the internal synchronous clock or external synchronous clock is selected, the full duplex mode and the transmit-only mode are available for serial transfer, one of which is selected by the transfer mode selection bit (b5 of address 0019₁₆) of serial I/O1 control register 1.

Either LSB first or MSB first is selected for the I/O sequence of the serial transfer bit strings by the transfer direction selection bit (b6 of address 0019₁₆) of serial I/O1 control register 1.

When using serial I/O1, first select either 8-bit serial I/O or automatic transfer serial I/O by the serial transfer selection bits (b0 and b1 of address 0019₁₆) of serial I/O1 control register 1, after completion of the above bit setup. Next, set the serial I/O initialization bit (b4 of address 0019₁₆) of serial I/O1 control register 1 to “1” (Serial I/O enable) .

When stopping serial transfer while data is being transferred, regardless of whether the internal or external synchronous clock is selected, reset the serial I/O initialization bit (b4) to “0.”

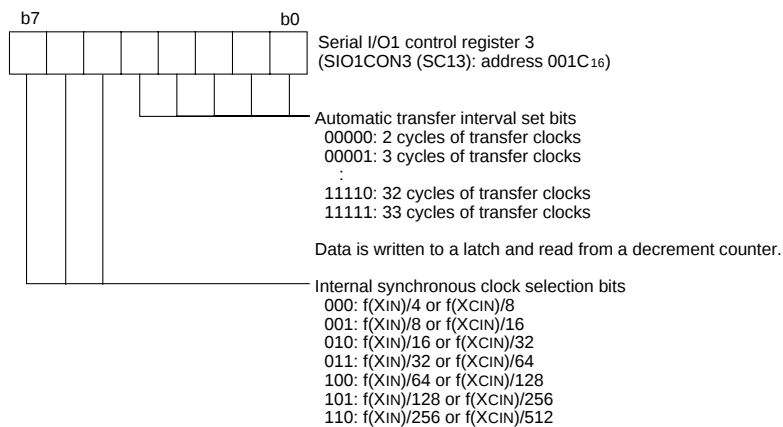


Fig. 23 Structure of serial I/O1 control register 3

HARDWARE

FUNCTIONAL DESCRIPTION

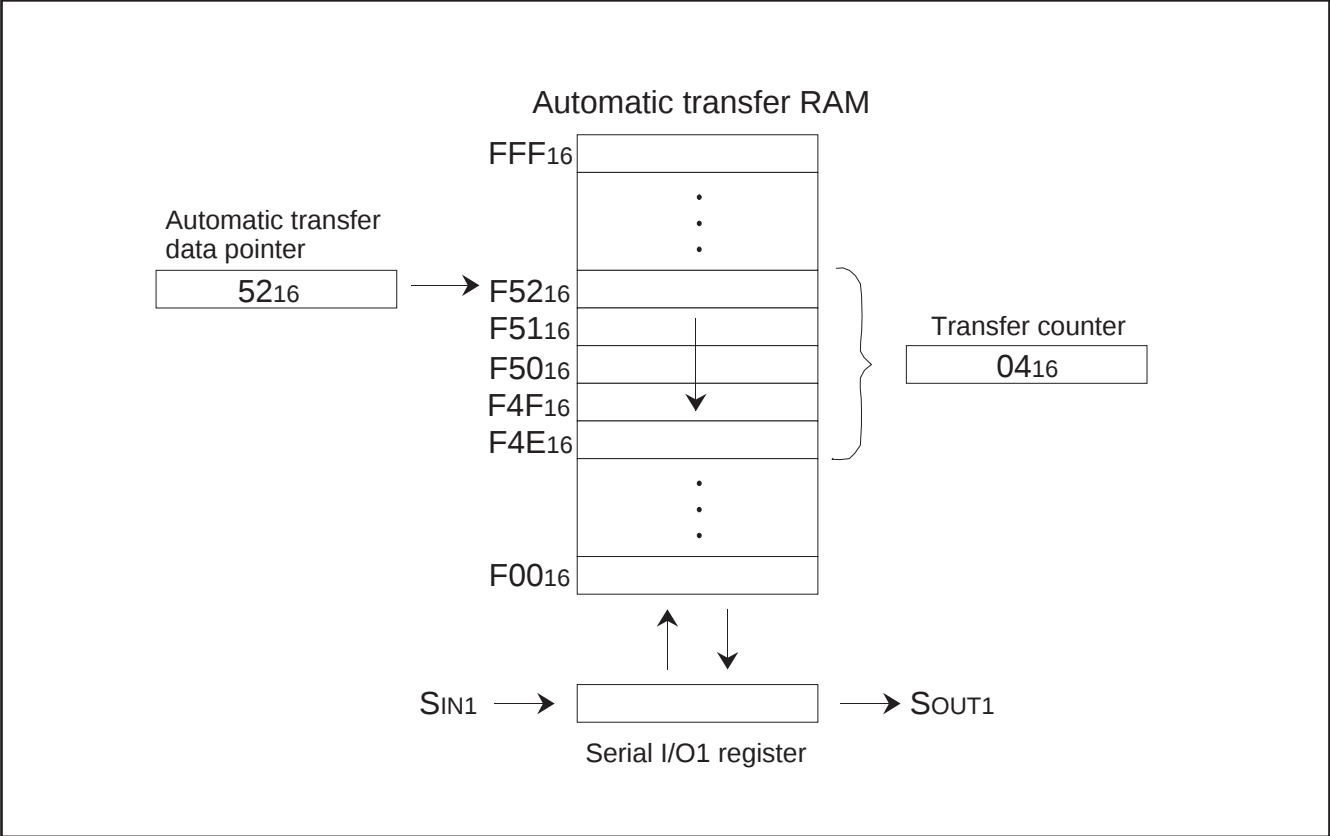


Fig. 25 Automatic transfer serial I/O operation

(4) Handshake Signal

1. S_{STB1} output signal

The S_{STB1} output is a signal to inform an end of transmission/reception to the serial transfer destination. The S_{STB1} output signal can be used only when the internal synchronous clock is selected. In the initial status, namely, in the status in which the serial I/O initialization bit (b4) is reset to "0," the S_{STB1} output goes to "L," or the S_{STB1} output goes to "H."

At the end of transmit/receive operation, when the data of the serial I/O1 register is all output from S_{OUT1}, pulses are output in the period of 1 cycle of the transfer clock so as to cause the S_{STB1} output to go "H" or the S_{STB1} output to go "L." After that, each pulse is returned to the initial status in which S_{STB1} output goes to "L" or the S_{STB1} output goes to "H."

Furthermore, after 1 cycle, the serial transfer status flag (b5) is reset to "0."

In the automatic transfer serial I/O mode, whether the S_{STB1} output is to be active at an end of each 1-byte data or after completion of transfer of all data can be selected by the S_{BUSY1} output • S_{STB1} output function selection bit (b4 of address 001A16) of serial I/O1 control register 2.

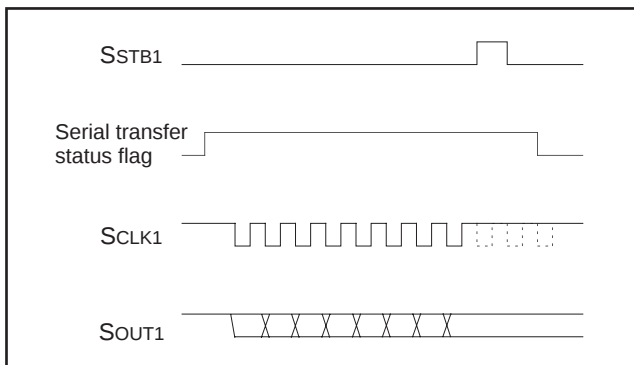


Fig. 26 S_{STB1} output operation

2. S_{BUSY1} input signal

The S_{BUSY1} input is a signal which receives a request for a stop of transmission/reception from the serial transfer destination.

When the internal synchronous clock is selected, input an "H" level signal into the S_{BUSY1} input and an "L" level signal into the S_{BUSY1} input in the initial status in which transfer is stopped.

When starting a transmit/receive operation, input an "L" level signal into the S_{BUSY1} input and an "H" level signal into the S_{BUSY1} input in the period of 1.5 cycles or more of the transfer clock. Then, transfer clocks are output from the S_{CLK1} output.

When an "H" level signal is input into the S_{BUSY1} input and an "L" level signal into the S_{BUSY1} input after a transmit/receive operation is started, this transmit/receive operation is not stopped immediately and the transfer clocks from the S_{CLK1} output is not stopped until the specified number of bits are transmitted and received.

The handshake unit of the 8-bit serial I/O is 8 bits and that of the automatic transfer serial I/O is 8 bits.

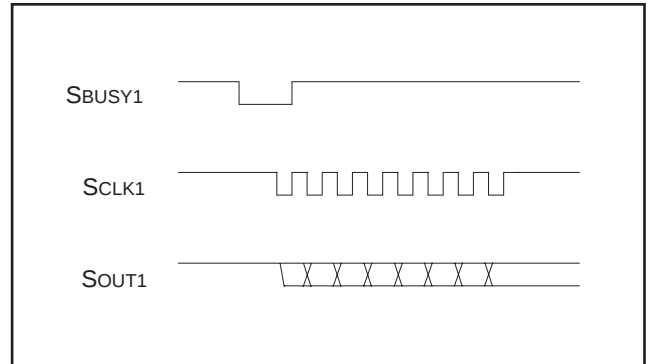


Fig. 27 S_{BUSY1} input operation (internal synchronous clock)

When the external synchronous clock is selected, input an "H" level signal into the S_{BUSY1} input and an "L" level signal into the S_{BUSY1} input in the initial status in which transfer is stopped. At this time, the transfer clocks to be input in S_{CLK1} become invalid.

During serial transfer, the transfer clocks to be input in S_{CLK1} become valid, enabling a transmit/receive operation, while an "L" level signal is input into the S_{BUSY1} input and an "H" level signal is input into the S_{BUSY1} input.

When changing the input values in the S_{BUSY1} input and the S_{BUSY1} input at these operations, change them when the S_{CLK1} input is in a high state.

When the high impedance of the S_{OUT1} output is selected by the S_{OUT1} pin control bit (b6), the S_{OUT1} output becomes active, enabling serial transfer by inputting a transfer clock to S_{CLK1}, while an "L" level signal is input into the S_{BUSY1} input and an "H" level signal is input into the S_{BUSY1} input.

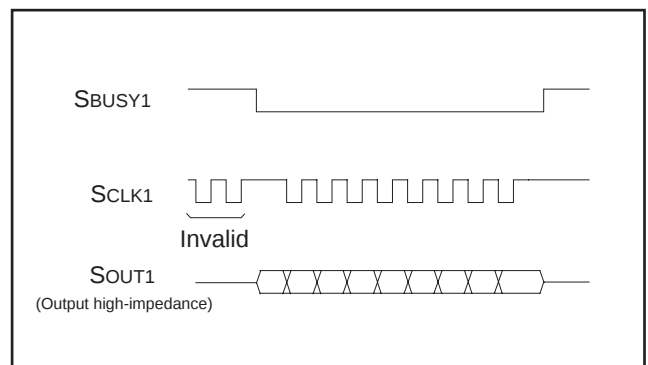


Fig. 28 S_{BUSY1} input operation (external synchronous clock)

3. S_{BUSY1} output signal

The S_{BUSY1} output is a signal which requests a stop of transmission/reception to the serial transfer destination. In the automatic transfer serial I/O mode, regardless of the internal or external synchronous clock, whether the S_{BUSY1} output is to be active at transfer of each 1-byte data or during transfer of all data can be selected by the S_{BUSY1} output • S_{STB1} output function selection bit (b4).

In the initial status, the status in which the serial I/O initialization bit (b4) is reset to "0," the S_{BUSY1} output goes to "H" and the S_{BUSY1} output goes to "L."

HARDWARE

FUNCTIONAL DESCRIPTION

When the internal synchronous clock is selected, in the 8-bit serial I/O mode and the automatic transfer serial I/O mode (S_{BUSY1} output function outputs in 1-byte units), the S_{BUSY1} output goes to “L” and the $\overline{\text{S}}_{\text{BUSY1}}$ output goes to “H” before 0.5 cycle (transfer clock) of the timing at which the transfer clock from the SCLK1 output goes to “L” at a start of transmit/receive operation.

In the automatic transfer serial I/O mode (the S_{BUSY1} output function outputs all transfer data), the S_{BUSY1} output goes to “L” and the $\overline{\text{S}}_{\text{BUSY1}}$ output goes to “H” when the first transmit data is written into the serial I/O1 register (address 001B16).

When the external synchronous clock is selected, the S_{BUSY1} output goes to “L” and the $\overline{\text{S}}_{\text{BUSY1}}$ output goes to “H” when transmit

data is written into the serial I/O1 register to start a transmit operation, regardless of the serial I/O transfer mode.

At termination of transmit/receive operation, the S_{BUSY1} output returns to “H” and the $\overline{\text{S}}_{\text{BUSY1}}$ output returns to “L”, the initial status, when the serial transfer status flag is set to “0”, regardless of whether the internal or external synchronous clock is selected.

Furthermore, in the automatic transfer serial I/O mode (S_{BUSY1} output function outputs in 1-byte units), the S_{BUSY1} output goes to “H” and the $\overline{\text{S}}_{\text{BUSY1}}$ output goes to “L” each time 1-byte of receive data is written into the automatic transfer RAM.

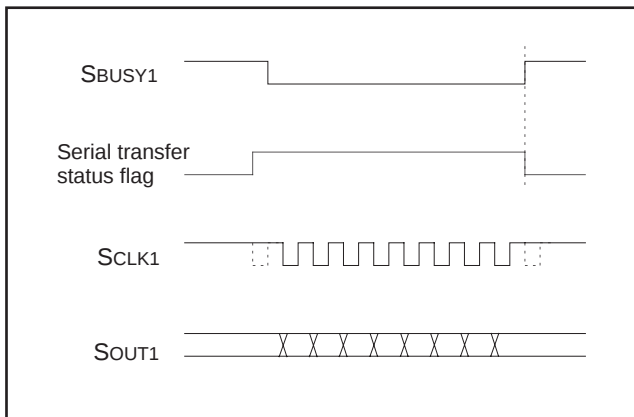


Fig. 29 S_{BUSY1} output operation
(internal synchronous clock, 8-bits serial I/O)

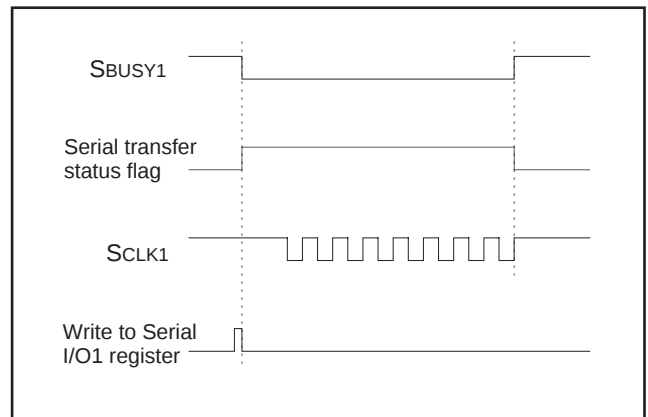


Fig. 30 S_{BUSY1} output operation
(external synchronous clock, 8-bits serial I/O)

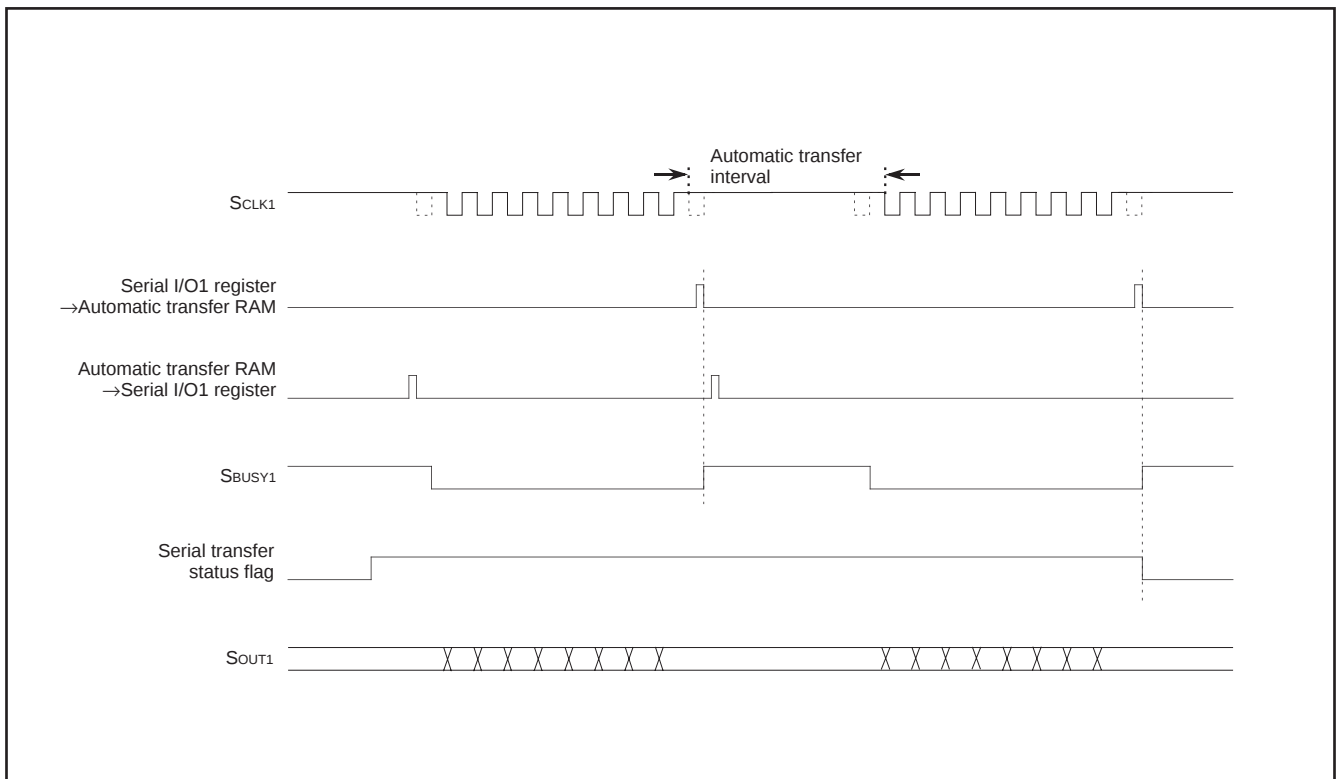


Fig. 31 S_{BUSY1} output operation in automatic transfer serial I/O mode
(internal synchronous clock, S_{BUSY1} output function outputs each 1-byte)

4. SRDY1 output signal

The SRDY1 output is a transmit/receive enable signal which informs the serial transfer destination that transmit/receive is ready. In the initial status, when the serial I/O initialization bit (b4) is reset to "0," the SRDY1 output goes to "L" and the $\overline{\text{SRDY1}}$ output goes to "H". After transmitted data is stored in the serial I/O1 register (address 001B16) and a transmit/receive operation becomes ready, the SRDY1 output goes to "H" and the $\overline{\text{SRDY1}}$ output goes to "L". When a transmit/receive operation is started and the transfer clock goes to "L", the SRDY1 output goes to "L" and the $\overline{\text{SRDY1}}$ output goes to "H".

5. SRDY1 input signal

The SRDY1 input signal becomes valid only when the SRDY1 input and the SBUSY1 output are used. The SRDY1 input is a signal for receiving a transmit/receive ready completion signal from the serial transfer destination.

When the internal synchronous clock is selected, input a low level signal into the SRDY1 input and a high level signal into the $\overline{\text{SRDY1}}$ input in the initial status in which the transfer is stopped.

When an "H" level signal is input into the SRDY1 input and an "L" level signal is input into the $\overline{\text{SRDY1}}$ input for a period of 1.5 cycles or more of transfer clock, transfer clocks are output from the SCLK1 output and a transmit/receive operation is started.

After the transmit/receive operation is started and an "L" level signal is input into the SRDY1 input and an "H" level signal into the $\overline{\text{SRDY1}}$ input, this operation cannot be immediately stopped.

After the specified number of bits are transmitted and received, the transfer clocks from the SCLK1 output is stopped. The handshake unit of the 8-bit serial I/O and that of the automatic transfer serial I/O are of 8 bits.

When the external synchronous clock is selected, the SRDY1 input becomes one of the triggers to output the SBUSY1 signal.

To start a transmit/receive operation (SBUSY1 output: "L," SBUSY1 output: "H"), input an "H" level signal into the SRDY1 input and an "L" level signal into the $\overline{\text{SRDY1}}$ input, and also write transmit data into the serial I/O1 register.

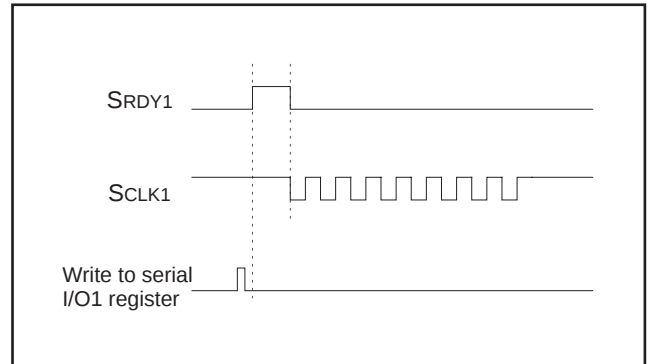


Fig. 32 SRDY1 output operation

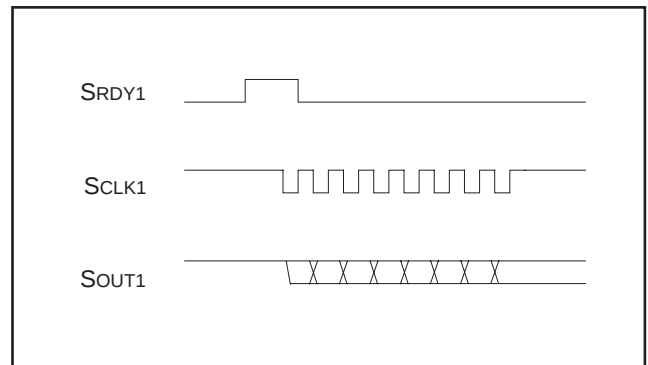


Fig. 33 SRDY1 input operation (internal synchronous clock)

HARDWARE

FUNCTIONAL DESCRIPTION

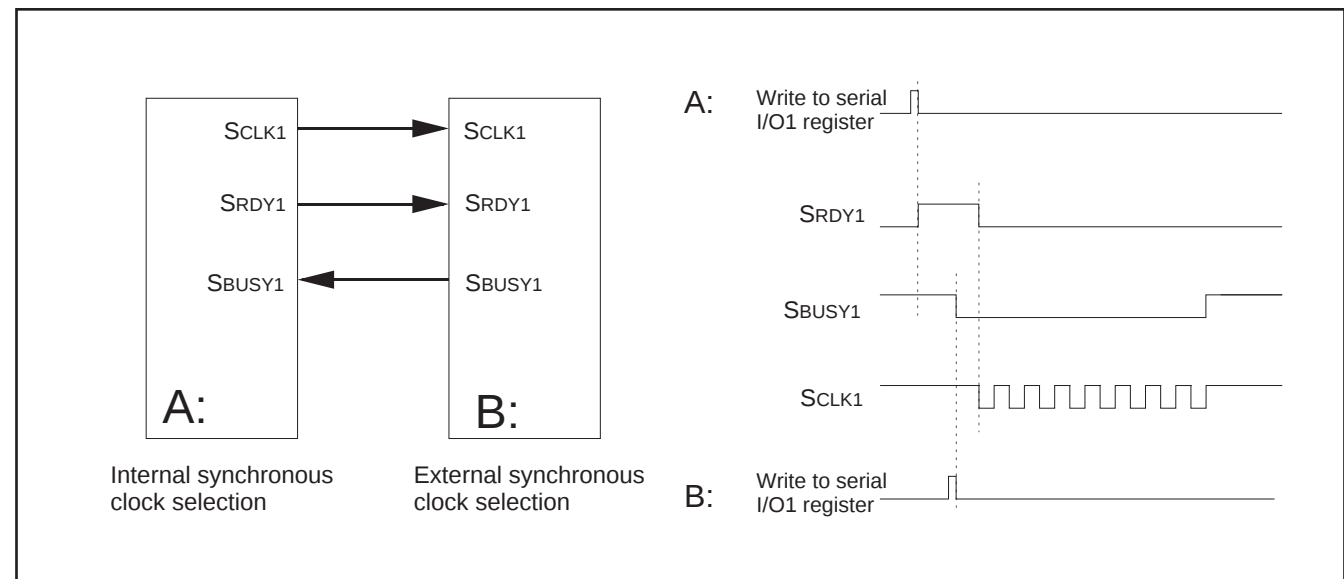


Fig. 34 Handshake operation at serial I/O1 mutual connecting (1)

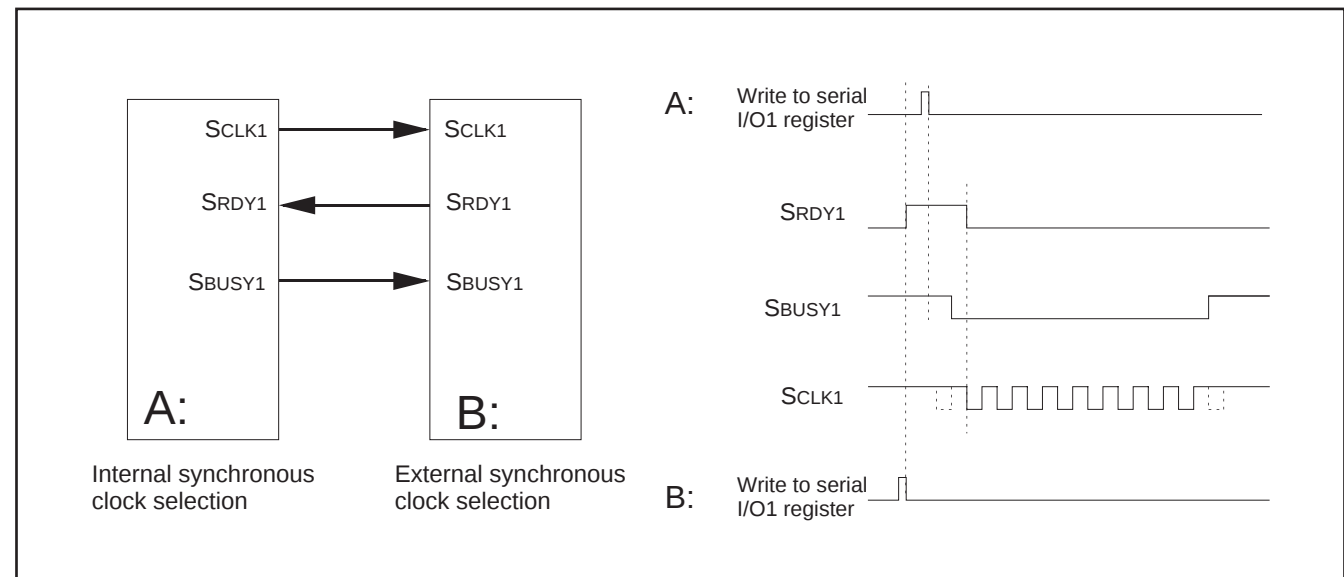


Fig. 35 Handshake operation at serial I/O1 mutual connecting (2)

Serial I/O2

Serial I/O2 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation during serial I/O2 operation.

(1) Clock Synchronous Serial I/O Mode

The clock synchronous serial I/O mode can be selected by setting the serial I/O2 mode selection bit (b6) of the serial I/O2 control reg-

ister (address 001D16) to "1." For clock synchronous serial I/O, the transmitter and the receiver must use the same clock for serial I/O2 operation. If an internal clock is used, transmit/receive is started by a write signal to the serial I/O2 transmit/receive buffer register (TB/RB) (address 001F16).

When P57 (SCLK22) is selected as a clock I/O pin, $\overline{\text{SRDY2}}$ output function is invalid, and P56 (SCLK21) is used as an I/O port.

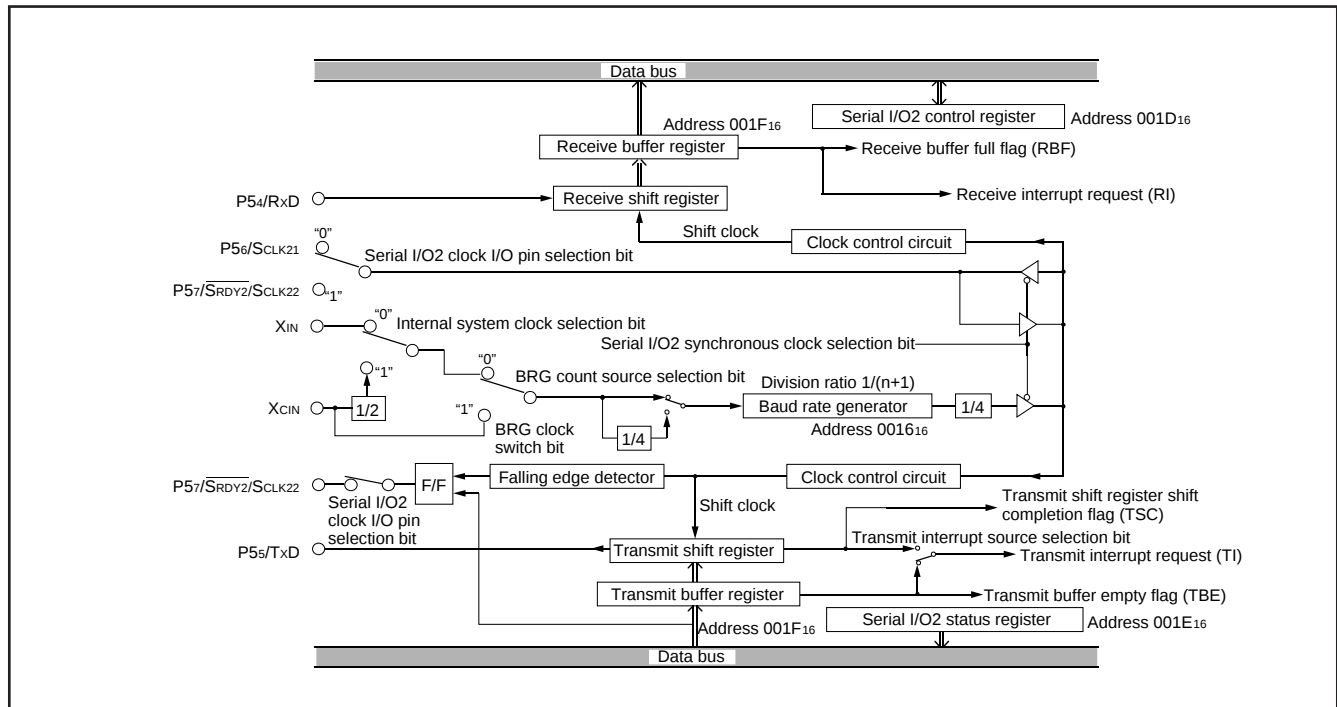


Fig. 36 Block diagram of clock synchronous serial I/O2

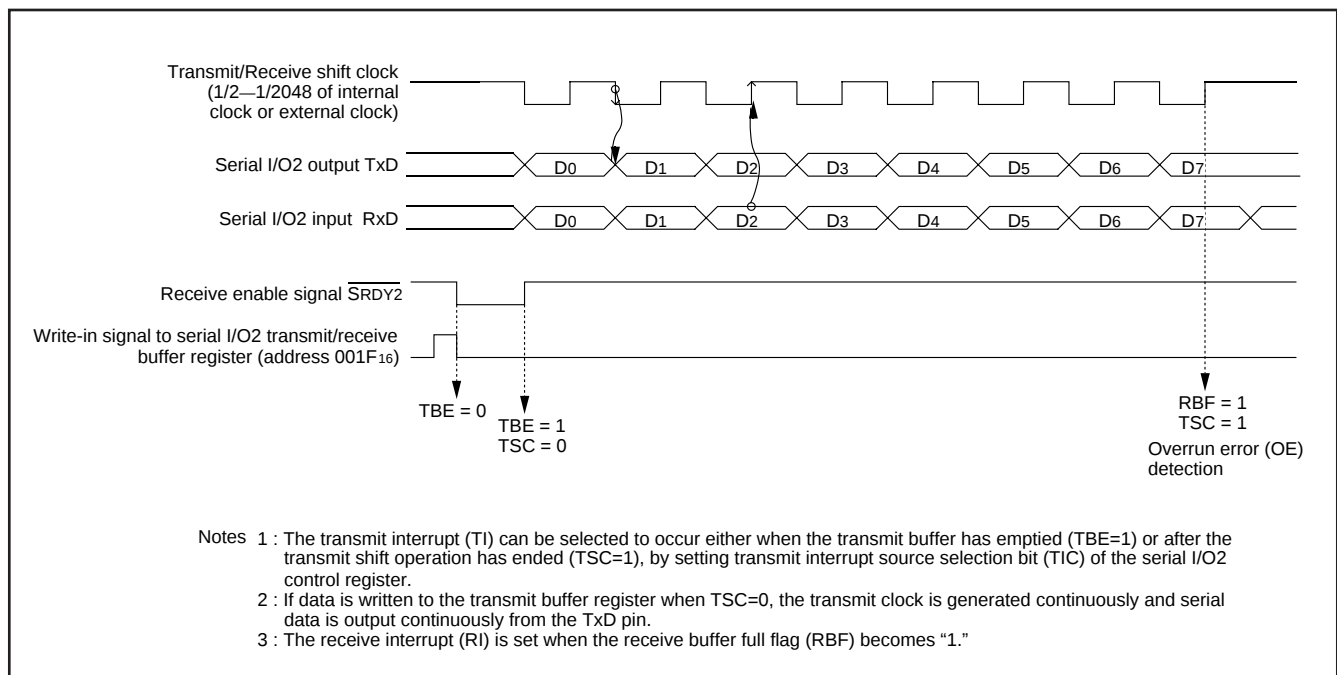


Fig. 37 Operation of clock synchronous serial I/O2 function

HARDWARE

FUNCTIONAL DESCRIPTION

(2) Asynchronous Serial I/O (UART) Mode

The asynchronous serial I/O (UART) mode can be selected by clearing the serial I/O2 mode selection bit (b6) of the serial I/O2 control register (address 001D₁₆) to "0." Eight serial data transfer formats can be selected and the transfer formats used by the transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer (the two buffers have the same address in memory). Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer. The transmit buffer can also hold the next data to be transmitted, and the receive buffer can receive 2-byte data continuously.

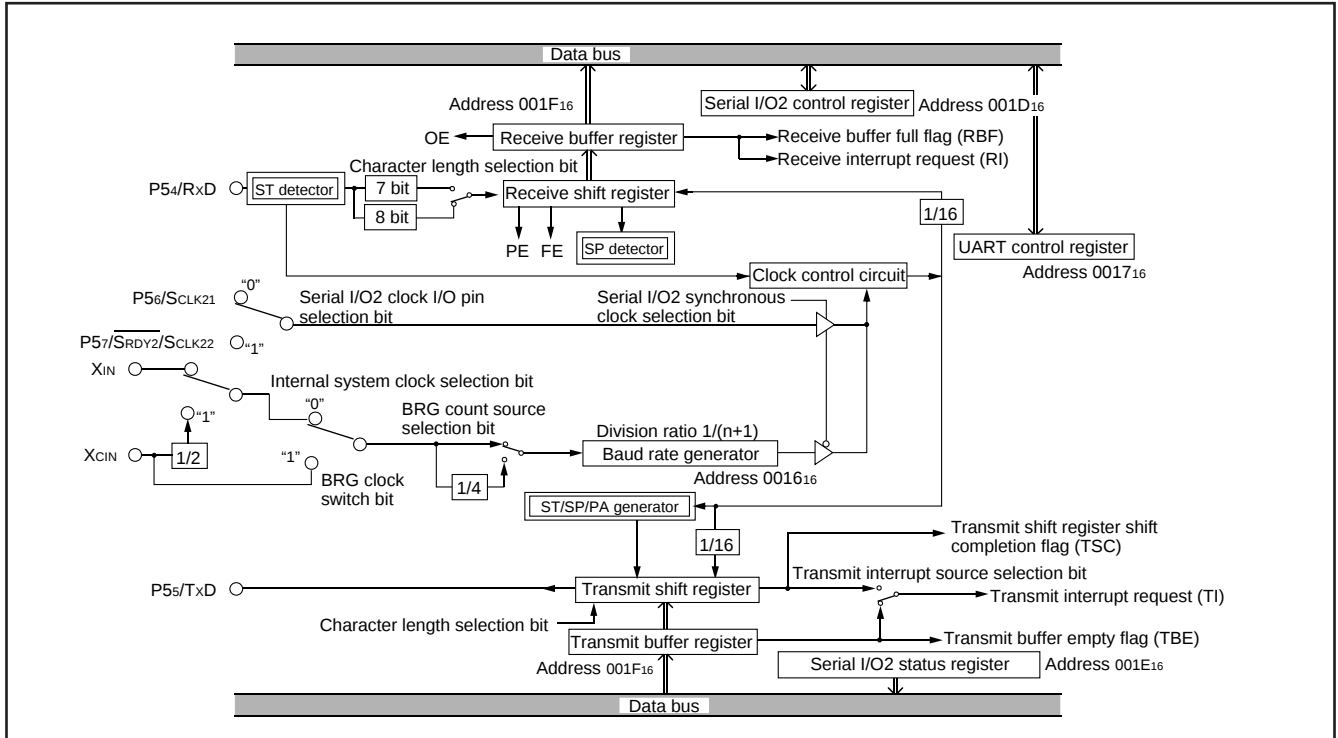


Fig. 38 Block diagram of UART serial I/O2

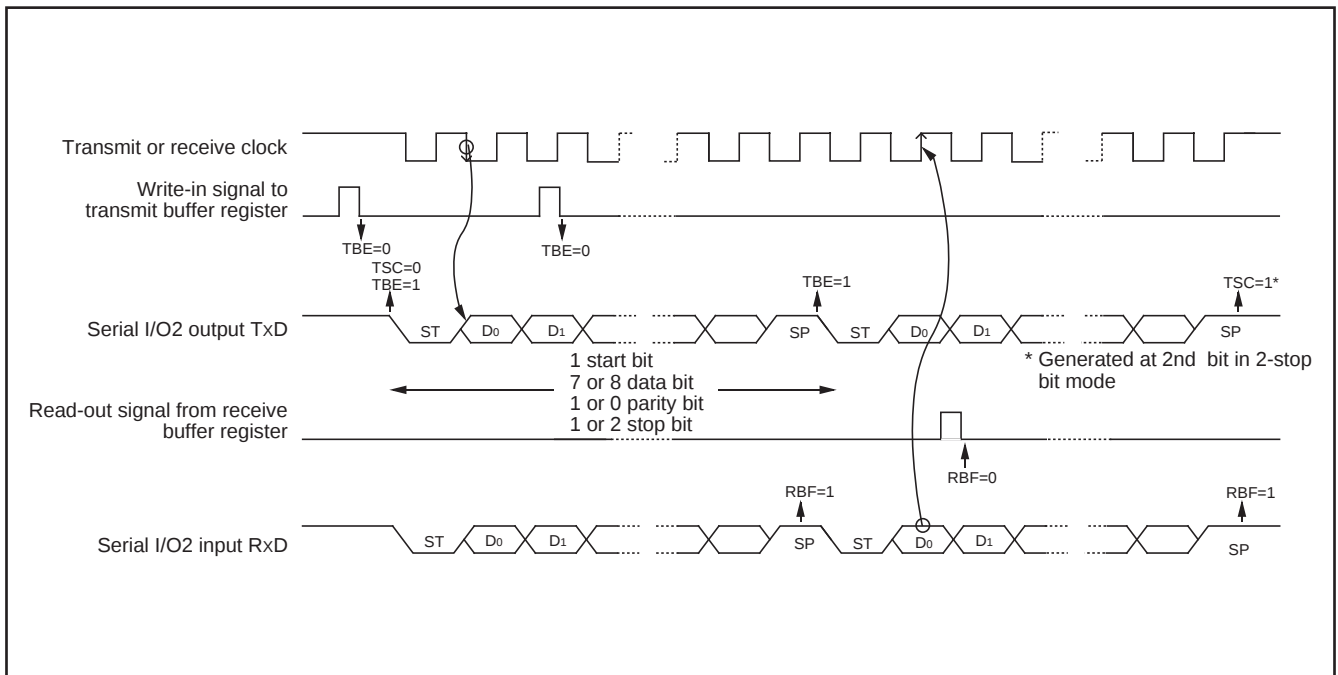


Fig. 39 Operation of UART serial I/O2 function

[Serial I/O2 Control Register] SIO2CON (001D16)

The serial I/O2 control register contains eight control bits for serial I/O2 functions.

[UART Control Register] UARTCON (001716)

This is a 7 bit register containing four control bits, which are valid when UART is selected, two control bits, which are valid when using serial I/O2, and one control bit, which is always valid.

Data format of serial data receive/transfer and the output structure of the P55/TxD pin, etc. are set by this register.

[Serial I/O2 Status Register] SIO2STS (001E16)

The read-only serial I/O2 status register consists of seven flags (b0 to b6) which indicate the operating status of the serial I/O2 function and various errors. Three of the flags (b4 to b6) are only valid in the UART mode. The receive buffer full flag (b1) is cleared to "0" when the receive buffer is read.

The error detection is performed at the same time data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A writing to the serial I/O2 status regis-

ter clears error flags OE, PE, FE, and SE (b3 to b6, respectively). Writing "0" to the serial I/O2 enable bit (SIOE : b7 of the serial I/O2 control register) also clears all the status flags, including the error flags.

All bits of the serial I/O2 status register are initialized to "0" at reset, but if the transmit enable bit (b4) of the serial I/O2 control register has been set to "1," the transmit shift register shift completion flag (b2) and the transmit buffer empty flag (b0) become "1."

[Serial I/O2 Transmit Buffer Register/Receive Buffer Register] TB/RB (001F16)

The transmit buffer and the receive buffer are located in the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Baud Rate Generator] BRG (001616)

The baud rate generator determines the baud rate for serial transfer. With the 8-bit counter having a reload register, the baud rate generator divides the frequency of the count source by $1/(n+1)$, where n is the value written to the baud rate generator.

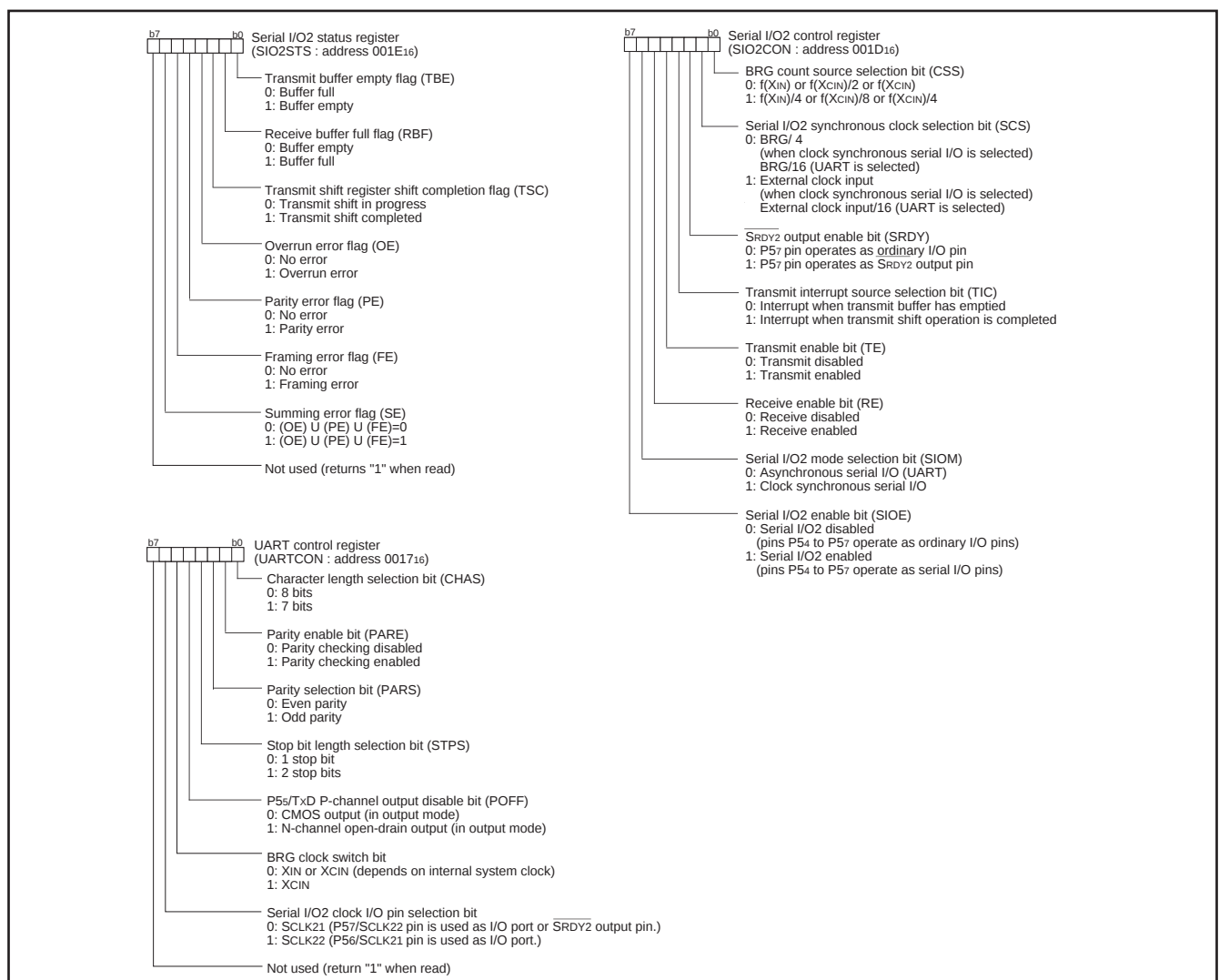


Fig. 40 Structure of serial I/O2 related register

HARDWARE

FUNCTIONAL DESCRIPTION

FLD Controller

The 38B5 group has fluorescent display (FLD) drive and control circuits.

The FLD controller consists of the following components:

- 40 pins for FLD control pins
- FLDC mode register
- FLD data pointer
- FLD data pointer reload register
- Tdisp time set register

- Toff1 time set register
- Toff2 time set register
- Port P0FLD/port switch register
- Port P2FLD/port switch register
- Port P8FLD/port switch register
- Port P8 FLD output control register
- FLD automatic display RAM (max. 160 bytes)

A gradation display mode can be used for bright/dark display as a display function.

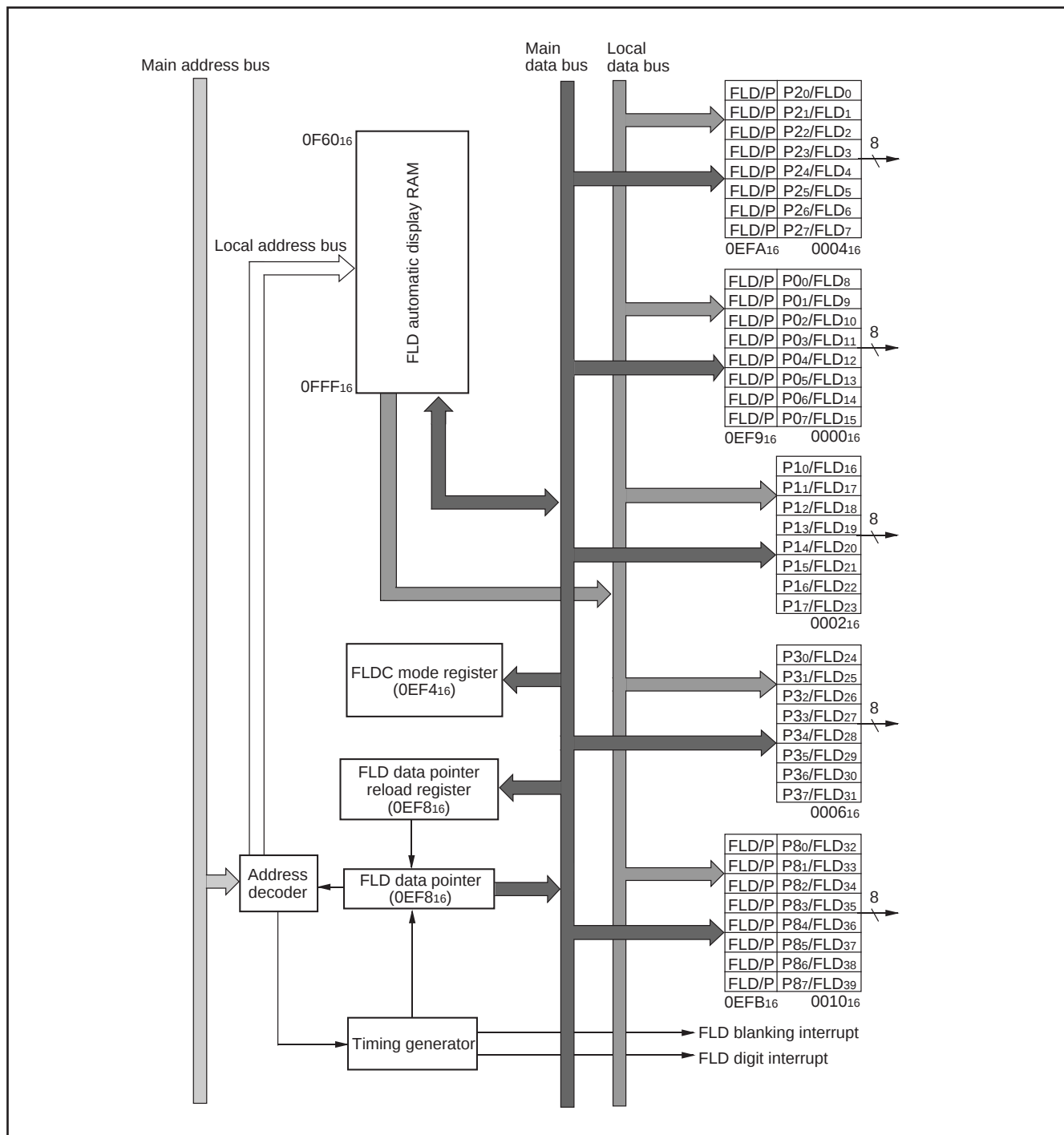
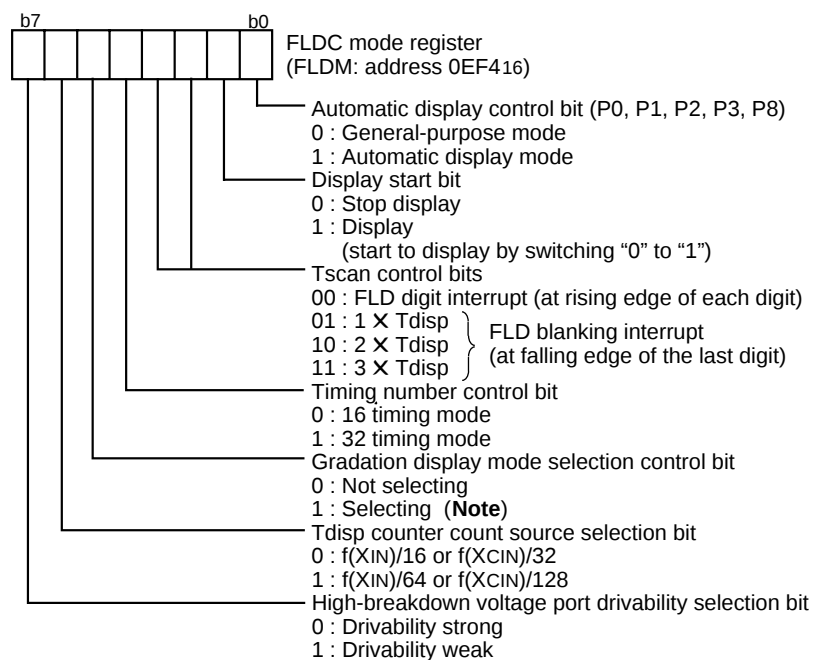


Fig. 41 Block diagram for FLD control circuit

[FLDC Mode Register] FLDM

The FLDC mode register is a 8-bit register respectively which is used to control the FLD automatic display and to set the blanking time Tscan for key-scan.



- Notes**
- 1: When a gradation display mode is selected, a number of timing is max. 16 timing. (Set the timing number control bit to "0".)
 - 2: When changing bit 4 (timing number control bit) or bit 5 (gradation display mode selection control bit), set "0" to bit 1 (display start bit) to perform at display stop state.

Fig. 42 Structure of FLDC mode register

HARDWARE

FUNCTIONAL DESCRIPTION

FLD automatic display pins

When the automatic display control bits of the FLDC mode register (address 0EF416) are set to "1," the ports of P0, P1, P2, P3 and P8 are used as FLD automatic display pins.

When using the FLD automatic display mode, set each port to the FLD pin or the general-purpose port using the respective switch register in accordance with the number of segments and the number of digits.

This setting is performed by writing a value into the FLD/port switch register (addresses 0EF916 to 0EFB16) of each port.

This setting can be performed in units of bit. When "0" is set, the port is set to the general-purpose port. When "1" is set, the port is set to the FLD pin. There is no restriction on whether the FLD pin is to be used as a segment pin or a digit pin.

Table 9 Pins in FLD automatic display mode

Port Name	Automatic Display Pins	Setting Method
P0, P2, P80–P83	FLD0–FLD15 FLD32–FLD35	The individual bits of the FLD/port switch register (addresses 0EF916–0EFB16) can be set each pin either FLD port ("1") or general-purpose port ("0").
P1, P3	FLD16–FLD31	None (FLD only)
P84–P87	FLD36–FLD39	The individual bits of the FLD/port switch register (address 0EFB16) can be set each pin to either FLD port ("1") or general-purpose port ("0"). The output can be reversed by the port P8 FLD output control register (address 0EFC16). The port output format is the CMOS output format. When using the port as a display pin, a driver must be installed externally.

	Setting example 1	Setting example 2	Setting example 3	Setting example 4																																																																
Number of segments	15	25	18	16																																																																
Number of digits	8	15	20	10																																																																
Port P2	<table><tr><td>0</td><td>P20</td></tr><tr><td>0</td><td>P21</td></tr><tr><td>0</td><td>P22</td></tr><tr><td>0</td><td>P23</td></tr><tr><td>0</td><td>P24</td></tr><tr><td>0</td><td>P25</td></tr><tr><td>0</td><td>P26</td></tr><tr><td>0</td><td>P27</td></tr></table>	0	P20	0	P21	0	P22	0	P23	0	P24	0	P25	0	P26	0	P27	<table><tr><td>1</td><td>FLD0(SEG1)</td></tr><tr><td>1</td><td>FLD1(SEG2)</td></tr><tr><td>1</td><td>FLD2(SEG3)</td></tr><tr><td>1</td><td>FLD3(SEG4)</td></tr><tr><td>1</td><td>FLD4(SEG5)</td></tr><tr><td>1</td><td>FLD5(SEG6)</td></tr><tr><td>1</td><td>FLD6(SEG7)</td></tr><tr><td>1</td><td>FLD7(SEG8)</td></tr></table>	1	FLD0(SEG1)	1	FLD1(SEG2)	1	FLD2(SEG3)	1	FLD3(SEG4)	1	FLD4(SEG5)	1	FLD5(SEG6)	1	FLD6(SEG7)	1	FLD7(SEG8)	<table><tr><td>0</td><td>P20</td></tr><tr><td>0</td><td>P21</td></tr><tr><td>1</td><td>FLD2(SEG1)</td></tr><tr><td>1</td><td>FLD3(SEG2)</td></tr><tr><td>1</td><td>FLD4(SEG3)</td></tr><tr><td>1</td><td>FLD5(SEG4)</td></tr><tr><td>1</td><td>FLD6(SEG5)</td></tr><tr><td>1</td><td>FLD7(SEG6)</td></tr></table>	0	P20	0	P21	1	FLD2(SEG1)	1	FLD3(SEG2)	1	FLD4(SEG3)	1	FLD5(SEG4)	1	FLD6(SEG5)	1	FLD7(SEG6)	<table><tr><td>0</td><td>P20</td></tr><tr><td>0</td><td>P21</td></tr><tr><td>0</td><td>P22</td></tr><tr><td>0</td><td>P23</td></tr><tr><td>0</td><td>P24</td></tr><tr><td>0</td><td>P25</td></tr><tr><td>1</td><td>FLD4(SEG1)</td></tr><tr><td>1</td><td>FLD5(SEG2)</td></tr></table>	0	P20	0	P21	0	P22	0	P23	0	P24	0	P25	1	FLD4(SEG1)	1	FLD5(SEG2)
0	P20																																																																			
0	P21																																																																			
0	P22																																																																			
0	P23																																																																			
0	P24																																																																			
0	P25																																																																			
0	P26																																																																			
0	P27																																																																			
1	FLD0(SEG1)																																																																			
1	FLD1(SEG2)																																																																			
1	FLD2(SEG3)																																																																			
1	FLD3(SEG4)																																																																			
1	FLD4(SEG5)																																																																			
1	FLD5(SEG6)																																																																			
1	FLD6(SEG7)																																																																			
1	FLD7(SEG8)																																																																			
0	P20																																																																			
0	P21																																																																			
1	FLD2(SEG1)																																																																			
1	FLD3(SEG2)																																																																			
1	FLD4(SEG3)																																																																			
1	FLD5(SEG4)																																																																			
1	FLD6(SEG5)																																																																			
1	FLD7(SEG6)																																																																			
0	P20																																																																			
0	P21																																																																			
0	P22																																																																			
0	P23																																																																			
0	P24																																																																			
0	P25																																																																			
1	FLD4(SEG1)																																																																			
1	FLD5(SEG2)																																																																			
Port P0	<table><tr><td>1</td><td>FLD8(SEG1)</td></tr><tr><td>0</td><td>P01</td></tr><tr><td>0</td><td>P02</td></tr><tr><td>0</td><td>P03</td></tr><tr><td>0</td><td>P04</td></tr><tr><td>0</td><td>P05</td></tr><tr><td>1</td><td>FLD14(SEG2)</td></tr><tr><td>1</td><td>FLD15(SEG3)</td></tr></table>	1	FLD8(SEG1)	0	P01	0	P02	0	P03	0	P04	0	P05	1	FLD14(SEG2)	1	FLD15(SEG3)	<table><tr><td>1</td><td>FLD8(SEG9)</td></tr><tr><td>1</td><td>FLD9(SEG10)</td></tr><tr><td>1</td><td>FLD10(SEG11)</td></tr><tr><td>1</td><td>FLD11(SEG12)</td></tr><tr><td>1</td><td>FLD12(SEG13)</td></tr><tr><td>1</td><td>FLD13(SEG14)</td></tr><tr><td>1</td><td>FLD14(SEG15)</td></tr><tr><td>1</td><td>FLD15(SEG16)</td></tr></table>	1	FLD8(SEG9)	1	FLD9(SEG10)	1	FLD10(SEG11)	1	FLD11(SEG12)	1	FLD12(SEG13)	1	FLD13(SEG14)	1	FLD14(SEG15)	1	FLD15(SEG16)	<table><tr><td>1</td><td>FLD8(DIG1)</td></tr><tr><td>1</td><td>FLD9(DIG2)</td></tr><tr><td>1</td><td>FLD10(DIG3)</td></tr><tr><td>1</td><td>FLD11(DIG4)</td></tr><tr><td>1</td><td>FLD12(DIG5)</td></tr><tr><td>1</td><td>FLD13(DIG6)</td></tr><tr><td>1</td><td>FLD14(DIG7)</td></tr><tr><td>1</td><td>FLD15(DIG8)</td></tr></table>	1	FLD8(DIG1)	1	FLD9(DIG2)	1	FLD10(DIG3)	1	FLD11(DIG4)	1	FLD12(DIG5)	1	FLD13(DIG6)	1	FLD14(DIG7)	1	FLD15(DIG8)	<table><tr><td>1</td><td>FLD6(SEG3)</td></tr><tr><td>1</td><td>FLD7(SEG4)</td></tr><tr><td>1</td><td>FLD8(SEG5)</td></tr><tr><td>1</td><td>FLD9(SEG6)</td></tr><tr><td>1</td><td>FLD10(SEG7)</td></tr><tr><td>1</td><td>FLD11(SEG8)</td></tr><tr><td>1</td><td>FLD12(SEG9)</td></tr><tr><td>1</td><td>FLD13(SEG10)</td></tr></table>	1	FLD6(SEG3)	1	FLD7(SEG4)	1	FLD8(SEG5)	1	FLD9(SEG6)	1	FLD10(SEG7)	1	FLD11(SEG8)	1	FLD12(SEG9)	1	FLD13(SEG10)
1	FLD8(SEG1)																																																																			
0	P01																																																																			
0	P02																																																																			
0	P03																																																																			
0	P04																																																																			
0	P05																																																																			
1	FLD14(SEG2)																																																																			
1	FLD15(SEG3)																																																																			
1	FLD8(SEG9)																																																																			
1	FLD9(SEG10)																																																																			
1	FLD10(SEG11)																																																																			
1	FLD11(SEG12)																																																																			
1	FLD12(SEG13)																																																																			
1	FLD13(SEG14)																																																																			
1	FLD14(SEG15)																																																																			
1	FLD15(SEG16)																																																																			
1	FLD8(DIG1)																																																																			
1	FLD9(DIG2)																																																																			
1	FLD10(DIG3)																																																																			
1	FLD11(DIG4)																																																																			
1	FLD12(DIG5)																																																																			
1	FLD13(DIG6)																																																																			
1	FLD14(DIG7)																																																																			
1	FLD15(DIG8)																																																																			
1	FLD6(SEG3)																																																																			
1	FLD7(SEG4)																																																																			
1	FLD8(SEG5)																																																																			
1	FLD9(SEG6)																																																																			
1	FLD10(SEG7)																																																																			
1	FLD11(SEG8)																																																																			
1	FLD12(SEG9)																																																																			
1	FLD13(SEG10)																																																																			
Port P1	<table><tr><td>FLD16(DIG1)</td><td>1</td></tr><tr><td>FLD17(DIG2)</td><td>1</td></tr><tr><td>FLD18(DIG3)</td><td>1</td></tr><tr><td>FLD19(DIG4)</td><td>1</td></tr><tr><td>FLD20(SEG4)</td><td>0</td></tr><tr><td>FLD21(SEG5)</td><td>0</td></tr><tr><td>FLD22(SEG6)</td><td>0</td></tr><tr><td>FLD23(SEG7)</td><td>0</td></tr></table>	FLD16(DIG1)	1	FLD17(DIG2)	1	FLD18(DIG3)	1	FLD19(DIG4)	1	FLD20(SEG4)	0	FLD21(SEG5)	0	FLD22(SEG6)	0	FLD23(SEG7)	0	<table><tr><td>FLD16(DIG1)</td><td>1</td></tr><tr><td>FLD17(DIG2)</td><td>1</td></tr><tr><td>FLD18(DIG3)</td><td>1</td></tr><tr><td>FLD19(DIG4)</td><td>1</td></tr><tr><td>FLD20(DIG5)</td><td>1</td></tr><tr><td>FLD21(DIG6)</td><td>1</td></tr><tr><td>FLD22(DIG7)</td><td>1</td></tr><tr><td>FLD23(DIG8)</td><td>1</td></tr></table>	FLD16(DIG1)	1	FLD17(DIG2)	1	FLD18(DIG3)	1	FLD19(DIG4)	1	FLD20(DIG5)	1	FLD21(DIG6)	1	FLD22(DIG7)	1	FLD23(DIG8)	1	<table><tr><td>FLD16(DIG9)</td><td>1</td></tr><tr><td>FLD17(DIG10)</td><td>1</td></tr><tr><td>FLD18(DIG11)</td><td>1</td></tr><tr><td>FLD19(DIG12)</td><td>1</td></tr><tr><td>FLD20(DIG13)</td><td>1</td></tr><tr><td>FLD21(DIG14)</td><td>1</td></tr><tr><td>FLD22(DIG15)</td><td>1</td></tr><tr><td>FLD23(DIG16)</td><td>1</td></tr></table>	FLD16(DIG9)	1	FLD17(DIG10)	1	FLD18(DIG11)	1	FLD19(DIG12)	1	FLD20(DIG13)	1	FLD21(DIG14)	1	FLD22(DIG15)	1	FLD23(DIG16)	1	<table><tr><td>FLD16(DIG1)</td><td>1</td></tr><tr><td>FLD17(DIG2)</td><td>1</td></tr><tr><td>FLD18(DIG3)</td><td>1</td></tr><tr><td>FLD19(DIG4)</td><td>1</td></tr><tr><td>FLD20(DIG5)</td><td>1</td></tr><tr><td>FLD21(DIG6)</td><td>1</td></tr><tr><td>FLD22(DIG7)</td><td>1</td></tr><tr><td>FLD23(DIG8)</td><td>1</td></tr></table>	FLD16(DIG1)	1	FLD17(DIG2)	1	FLD18(DIG3)	1	FLD19(DIG4)	1	FLD20(DIG5)	1	FLD21(DIG6)	1	FLD22(DIG7)	1	FLD23(DIG8)	1
FLD16(DIG1)	1																																																																			
FLD17(DIG2)	1																																																																			
FLD18(DIG3)	1																																																																			
FLD19(DIG4)	1																																																																			
FLD20(SEG4)	0																																																																			
FLD21(SEG5)	0																																																																			
FLD22(SEG6)	0																																																																			
FLD23(SEG7)	0																																																																			
FLD16(DIG1)	1																																																																			
FLD17(DIG2)	1																																																																			
FLD18(DIG3)	1																																																																			
FLD19(DIG4)	1																																																																			
FLD20(DIG5)	1																																																																			
FLD21(DIG6)	1																																																																			
FLD22(DIG7)	1																																																																			
FLD23(DIG8)	1																																																																			
FLD16(DIG9)	1																																																																			
FLD17(DIG10)	1																																																																			
FLD18(DIG11)	1																																																																			
FLD19(DIG12)	1																																																																			
FLD20(DIG13)	1																																																																			
FLD21(DIG14)	1																																																																			
FLD22(DIG15)	1																																																																			
FLD23(DIG16)	1																																																																			
FLD16(DIG1)	1																																																																			
FLD17(DIG2)	1																																																																			
FLD18(DIG3)	1																																																																			
FLD19(DIG4)	1																																																																			
FLD20(DIG5)	1																																																																			
FLD21(DIG6)	1																																																																			
FLD22(DIG7)	1																																																																			
FLD23(DIG8)	1																																																																			
Port P3	<table><tr><td>FLD24(SEG8)</td><td>0</td></tr><tr><td>FLD25(SEG9)</td><td>0</td></tr><tr><td>FLD26(SEG10)</td><td>0</td></tr><tr><td>FLD27(SEG11)</td><td>0</td></tr><tr><td>FLD28(DIG5)</td><td>1</td></tr><tr><td>FLD29(DIG6)</td><td>1</td></tr><tr><td>FLD30(DIG7)</td><td>1</td></tr><tr><td>FLD31(DIG8)</td><td>1</td></tr></table>	FLD24(SEG8)	0	FLD25(SEG9)	0	FLD26(SEG10)	0	FLD27(SEG11)	0	FLD28(DIG5)	1	FLD29(DIG6)	1	FLD30(DIG7)	1	FLD31(DIG8)	1	<table><tr><td>FLD24(DIG9)</td><td>1</td></tr><tr><td>FLD25(DIG10)</td><td>1</td></tr><tr><td>FLD26(DIG11)</td><td>1</td></tr><tr><td>FLD27(DIG12)</td><td>1</td></tr><tr><td>FLD28(DIG13)</td><td>1</td></tr><tr><td>FLD29(DIG14)</td><td>1</td></tr><tr><td>FLD30(DIG15)</td><td>1</td></tr><tr><td>FLD31(SEG17)</td><td>0</td></tr></table>	FLD24(DIG9)	1	FLD25(DIG10)	1	FLD26(DIG11)	1	FLD27(DIG12)	1	FLD28(DIG13)	1	FLD29(DIG14)	1	FLD30(DIG15)	1	FLD31(SEG17)	0	<table><tr><td>FLD24(DIG17)</td><td>1</td></tr><tr><td>FLD25(DIG18)</td><td>1</td></tr><tr><td>FLD26(DIG19)</td><td>1</td></tr><tr><td>FLD27(DIG20)</td><td>1</td></tr><tr><td>FLD28(SEG7)</td><td>0</td></tr><tr><td>FLD29(SEG8)</td><td>0</td></tr><tr><td>FLD30(SEG9)</td><td>0</td></tr><tr><td>FLD31(SEG10)</td><td>0</td></tr></table>	FLD24(DIG17)	1	FLD25(DIG18)	1	FLD26(DIG19)	1	FLD27(DIG20)	1	FLD28(SEG7)	0	FLD29(SEG8)	0	FLD30(SEG9)	0	FLD31(SEG10)	0	<table><tr><td>FLD24(DIG9)</td><td>1</td></tr><tr><td>FLD25(DIG10)</td><td>1</td></tr><tr><td>FLD14(SEG11)</td><td>1</td></tr><tr><td>FLD15(SEG12)</td><td>1</td></tr><tr><td>FLD26(SEG13)</td><td>0</td></tr><tr><td>FLD27(SEG14)</td><td>0</td></tr><tr><td>FLD28(SEG15)</td><td>0</td></tr><tr><td>FLD29(SEG16)</td><td>0</td></tr></table>	FLD24(DIG9)	1	FLD25(DIG10)	1	FLD14(SEG11)	1	FLD15(SEG12)	1	FLD26(SEG13)	0	FLD27(SEG14)	0	FLD28(SEG15)	0	FLD29(SEG16)	0
FLD24(SEG8)	0																																																																			
FLD25(SEG9)	0																																																																			
FLD26(SEG10)	0																																																																			
FLD27(SEG11)	0																																																																			
FLD28(DIG5)	1																																																																			
FLD29(DIG6)	1																																																																			
FLD30(DIG7)	1																																																																			
FLD31(DIG8)	1																																																																			
FLD24(DIG9)	1																																																																			
FLD25(DIG10)	1																																																																			
FLD26(DIG11)	1																																																																			
FLD27(DIG12)	1																																																																			
FLD28(DIG13)	1																																																																			
FLD29(DIG14)	1																																																																			
FLD30(DIG15)	1																																																																			
FLD31(SEG17)	0																																																																			
FLD24(DIG17)	1																																																																			
FLD25(DIG18)	1																																																																			
FLD26(DIG19)	1																																																																			
FLD27(DIG20)	1																																																																			
FLD28(SEG7)	0																																																																			
FLD29(SEG8)	0																																																																			
FLD30(SEG9)	0																																																																			
FLD31(SEG10)	0																																																																			
FLD24(DIG9)	1																																																																			
FLD25(DIG10)	1																																																																			
FLD14(SEG11)	1																																																																			
FLD15(SEG12)	1																																																																			
FLD26(SEG13)	0																																																																			
FLD27(SEG14)	0																																																																			
FLD28(SEG15)	0																																																																			
FLD29(SEG16)	0																																																																			
Port P8	<table><tr><td>1</td><td>FLD32(SEG12)</td></tr><tr><td>1</td><td>FLD33(SEG13)</td></tr><tr><td>1</td><td>FLD34(SEG14)</td></tr><tr><td>1</td><td>FLD35(SEG15)</td></tr><tr><td>0</td><td>P84</td></tr><tr><td>0</td><td>P85</td></tr><tr><td>0</td><td>P86</td></tr><tr><td>0</td><td>P87</td></tr></table>	1	FLD32(SEG12)	1	FLD33(SEG13)	1	FLD34(SEG14)	1	FLD35(SEG15)	0	P84	0	P85	0	P86	0	P87	<table><tr><td>1</td><td>FLD32(SEG18)</td></tr><tr><td>1</td><td>FLD33(SEG19)</td></tr><tr><td>1</td><td>FLD34(SEG20)</td></tr><tr><td>1</td><td>FLD35(SEG21)</td></tr><tr><td>1</td><td>FLD36(SEG22)</td></tr><tr><td>1</td><td>FLD37(SEG23)</td></tr><tr><td>1</td><td>FLD38(SEG24)</td></tr><tr><td>1</td><td>FLD39(SEG25)</td></tr></table>	1	FLD32(SEG18)	1	FLD33(SEG19)	1	FLD34(SEG20)	1	FLD35(SEG21)	1	FLD36(SEG22)	1	FLD37(SEG23)	1	FLD38(SEG24)	1	FLD39(SEG25)	<table><tr><td>1</td><td>FLD32(SEG11)</td></tr><tr><td>1</td><td>FLD33(SEG12)</td></tr><tr><td>1</td><td>FLD34(SEG13)</td></tr><tr><td>1</td><td>FLD35(SEG14)</td></tr><tr><td>1</td><td>FLD36(SEG15)</td></tr><tr><td>1</td><td>FLD37(SEG16)</td></tr><tr><td>1</td><td>FLD38(SEG17)</td></tr><tr><td>1</td><td>FLD39(SEG18)</td></tr></table>	1	FLD32(SEG11)	1	FLD33(SEG12)	1	FLD34(SEG13)	1	FLD35(SEG14)	1	FLD36(SEG15)	1	FLD37(SEG16)	1	FLD38(SEG17)	1	FLD39(SEG18)	<table><tr><td>0</td><td>P80</td></tr><tr><td>0</td><td>P81</td></tr><tr><td>0</td><td>P82</td></tr><tr><td>0</td><td>P83</td></tr><tr><td>0</td><td>P84</td></tr><tr><td>0</td><td>P85</td></tr><tr><td>0</td><td>P86</td></tr><tr><td>0</td><td>P87</td></tr></table>	0	P80	0	P81	0	P82	0	P83	0	P84	0	P85	0	P86	0	P87
1	FLD32(SEG12)																																																																			
1	FLD33(SEG13)																																																																			
1	FLD34(SEG14)																																																																			
1	FLD35(SEG15)																																																																			
0	P84																																																																			
0	P85																																																																			
0	P86																																																																			
0	P87																																																																			
1	FLD32(SEG18)																																																																			
1	FLD33(SEG19)																																																																			
1	FLD34(SEG20)																																																																			
1	FLD35(SEG21)																																																																			
1	FLD36(SEG22)																																																																			
1	FLD37(SEG23)																																																																			
1	FLD38(SEG24)																																																																			
1	FLD39(SEG25)																																																																			
1	FLD32(SEG11)																																																																			
1	FLD33(SEG12)																																																																			
1	FLD34(SEG13)																																																																			
1	FLD35(SEG14)																																																																			
1	FLD36(SEG15)																																																																			
1	FLD37(SEG16)																																																																			
1	FLD38(SEG17)																																																																			
1	FLD39(SEG18)																																																																			
0	P80																																																																			
0	P81																																																																			
0	P82																																																																			
0	P83																																																																			
0	P84																																																																			
0	P85																																																																			
0	P86																																																																			
0	P87																																																																			
	↑ Value of FLD/port switch register			↑ Value of FLDRAM write disable register If data is set to "1", data is protected. This setting does not decide the FLD port function (SEG/DIG).																																																																

Fig. 43 Segment/Digit setting example

FLD automatic display RAM

The FLD automatic display RAM uses the 160 bytes of addresses 0F60₁₆ to 0FFF₁₆. For FLD, the 3 modes of 16-timing ordinary mode, 16-timing•gradation display mode and 32-timing mode are available depending on the number of timings and the presence/absence of gradation display.

The automatic display RAM in each mode is as follows:

(1) 16-timing•Ordinary Mode

The 80 bytes of addresses 0FB0₁₆ to 0FFF₁₆ are used as a FLD display data store area. Because addresses 0F60₁₆ to 0FAF₁₆ are not used as the automatic display RAM, they can be the ordinary RAM or serial I/O automatic transfer RAM.

(2) 16-timing•Gradation Display Mode

The 160 bytes of addresses 0F60₁₆ to 0FFF₁₆ are used. The 80 bytes of addresses 0FB0₁₆ to 0FFF₁₆ are used as an FLD display data store area, while the 80 bytes of addresses 0F60₁₆ to 0FAF₁₆ are used as a gradation display control data store area.

(3) 32-timing Mode

The 160 bytes of addresses 0F60₁₆ to 0FFF₁₆ are used as an FLD display data store area.

[FLD Data Pointer and FLD Data Pointer Reload Register] FLDDP (0EF8₁₆)

Both the FLD data pointer and FLD data pointer reload register are 8-bit registers assigned at address 0EF8₁₆. When writing data to this address, the data is written to the FLD data pointer reload register; when reading data from this address, the value in the FLD data pointer is read.

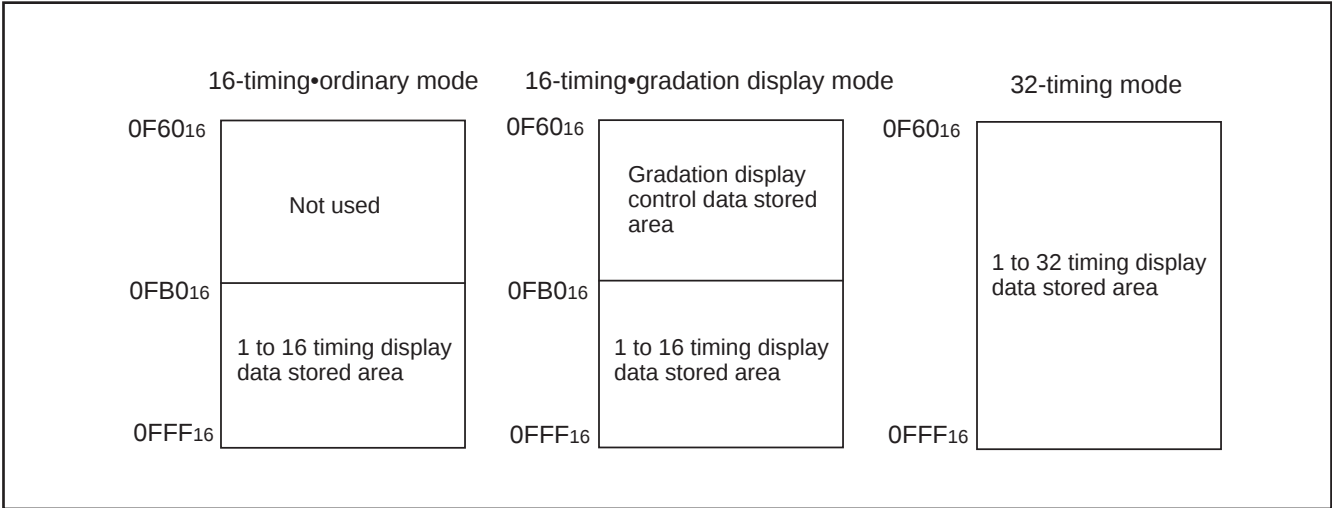


Fig. 44 FLD automatic display RAM assignment

HARDWARE

FUNCTIONAL DESCRIPTION

Data setup

(1) 16-timing•Ordinary Mode

The area of addresses 0FB0₁₆ to 0FFF₁₆ are used as a FLD automatic display RAM.

When data is stored in the FLD automatic display RAM, the last data of FLD port P2 is stored at address 0FB0₁₆, the last data of FLD port P0 is stored at address 0FC0₁₆, the last data of FLD port P1 is stored at address 0FD0₁₆, the last data of FLD port P3 is stored at address 0FE0₁₆, and the last data of FLD port P8 is stored at address 0FF0₁₆, to assign in sequence from the last data respectively.

The first data of the FLD port P2, P0, P1, P3, and P8 is stored at an address which adds the value of (the timing number – 1) to the corresponding address 0FB0₁₆, 0FC0₁₆, 0FD0₁₆, 0FE0₁₆, and 0FF0₁₆.

Set the FLD data pointer reload register to the value given by the timing number – 1. “1” is always written to bits 7, 6, and 5. Note that “0” is always read from bits 7, 6, and 5 when reading. “1” is always set to bit 4, but this bit become written value when reading.

(2) 16-timing•Gradation Display Mode

Display data setting is performed in the same way as that of the 16-timing•ordinary mode. Gradation display control data is arranged at an address resulting from subtracting 0050₁₆ from the display data store address of each timing and pin. Bright display is performed by setting “0,” and dark display is performed by setting “1.”

Set the FLD data pointer reload register to the value given by the timing number – 1. “1” is always written to bits 7, 6, and 5. Note that “0” is always read from bits 7, 6, and 5 when reading. “1” is always set to bit 4, but this bit become written value when reading.

(3) 32-timing Mode

The area of addresses 0F60₁₆ to 0FFF₁₆ are used as a FLD automatic display RAM. When data is stored in the FLD automatic display RAM, the last data of FLD port P2 is stored at address 0F60₁₆, the last data of FLD port P0 is stored at address 0F80₁₆, the last data of FLD port P1 is stored at address 0FA0₁₆, the last data of FLD port P3 is stored at address 0FC0₁₆, and the last data of FLD port P8 is stored at address 0FE0₁₆, to assign in sequence from the last data respectively.

The first data of the FLD port P2, P0, P1, P3, and P8 is stored at an address which adds the value of (the timing number – 1) to the corresponding address 0F60₁₆, 0F80₁₆, 0FA0₁₆, 0FC0₁₆, and 0FE0₁₆.

Set the FLD data pointer reload register to the value given by the timing number – 1. “1” is always written to bits 7, 6, and 5. Note that “0” is always read from bits 7, 6, and 5 when reading.

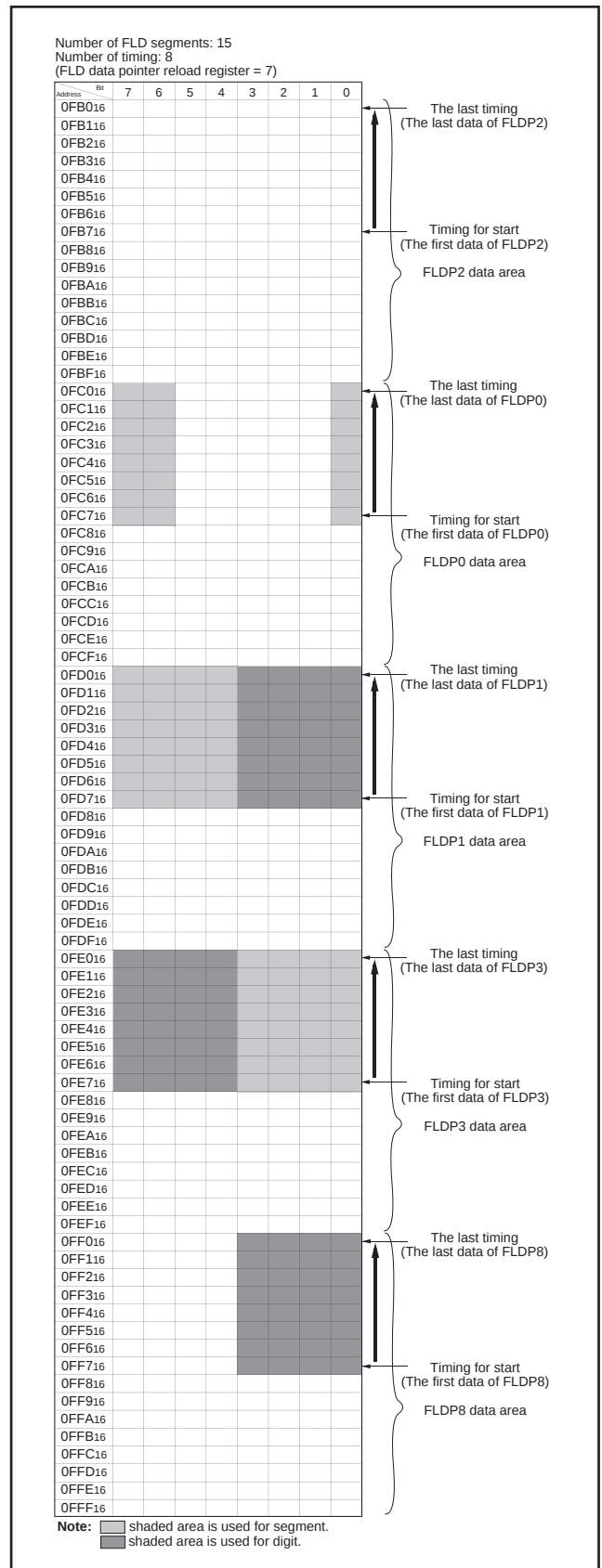


Fig. 45 Example of using FLD automatic display RAM in 16-timing•ordinary mode

Number of FLD segments: 25
 Number of timing: 15
 (FLD data pointer reload register = 14)

Address	Bit	7	6	5	4	3	2	1	0
0FB0 ₁₆									
0FB1 ₁₆									
0FB2 ₁₆									
0FB3 ₁₆									
0FB4 ₁₆									
0FB5 ₁₆									
0FB6 ₁₆									
0FB7 ₁₆									
0FB8 ₁₆									
0FB9 ₁₆									
0FBA ₁₆									
0FBB ₁₆									
0FBC ₁₆									
0FBD ₁₆									
0FBE ₁₆									
0FBF ₁₆									
0FC0 ₁₆									
0FC1 ₁₆									
0FC2 ₁₆									
0FC3 ₁₆									
0FC4 ₁₆									
0FC5 ₁₆									
0FC6 ₁₆									
0FC7 ₁₆									
0FC8 ₁₆									
0FC9 ₁₆									
0FCA ₁₆									
0FCB ₁₆									
0FCC ₁₆									
0FCD ₁₆									
0FCE ₁₆									
0FCF ₁₆									
0FD0 ₁₆									
0FD1 ₁₆									
0FD2 ₁₆									
0FD3 ₁₆									
0FD4 ₁₆									
0FD5 ₁₆									
0FD6 ₁₆									
0FD7 ₁₆									
0FD8 ₁₆									
0FD9 ₁₆									
0FDA ₁₆									
0FDB ₁₆									
0FDC ₁₆									
0FDD ₁₆									
0FDE ₁₆									
0FDF ₁₆									
0FE0 ₁₆									
0FE1 ₁₆									
0FE2 ₁₆									
0FE3 ₁₆									
0FE4 ₁₆									
0FE5 ₁₆									
0FE6 ₁₆									
0FE7 ₁₆									
0FE8 ₁₆									
0FE9 ₁₆									
0FEA ₁₆									
0FEB ₁₆									
0FEC ₁₆									
0FED ₁₆									
0FEE ₁₆									
0FEF ₁₆									
0FF0 ₁₆									
0FF1 ₁₆									
0FF2 ₁₆									
0FF3 ₁₆									
0FF4 ₁₆									
0FF5 ₁₆									
0FF6 ₁₆									
0FF7 ₁₆									
0FF8 ₁₆									
0FF9 ₁₆									
0FFA ₁₆									
0FFB ₁₆									
0FFC ₁₆									
0FFD ₁₆									
0FFE ₁₆									
0FFF ₁₆									

Note:  shaded area is used for segment.
 shaded area is used for digit.

Address	Bit	7	6	5	4	3	2	1	0
0F60 ₁₆									
0F61 ₁₆									
0F62 ₁₆									
0F63 ₁₆									
0F64 ₁₆									
0F65 ₁₆									
0F66 ₁₆									
0F67 ₁₆									
0F68 ₁₆									
0F69 ₁₆									
0F6A ₁₆									
0F6B ₁₆									
0F6C ₁₆									
0F6D ₁₆									
0F6E ₁₆									
0F6F ₁₆									
0F70 ₁₆									
0F71 ₁₆									
0F72 ₁₆									
0F73 ₁₆									
0F74 ₁₆									
0F75 ₁₆									
0F76 ₁₆									
0F77 ₁₆									
0F78 ₁₆									
0F79 ₁₆									
0F7A ₁₆									
0F7B ₁₆									
0F7C ₁₆									
0F7D ₁₆									
0F7E ₁₆									
0F7F ₁₆									
0F80 ₁₆									
0F81 ₁₆									
0F82 ₁₆									
0F83 ₁₆									
0F84 ₁₆									
0F85 ₁₆									
0F86 ₁₆									
0F87 ₁₆									
0F88 ₁₆									
0F89 ₁₆									
0F8A ₁₆									
0F8B ₁₆									
0F8C ₁₆									
0F8D ₁₆									
0F8E ₁₆									
0F8F ₁₆									
0F90 ₁₆									
0F91 ₁₆									
0F92 ₁₆									
0F93 ₁₆									
0F94 ₁₆									
0F95 ₁₆									
0F96 ₁₆									
0F97 ₁₆									
0F98 ₁₆									
0F99 ₁₆									
0F9A ₁₆									
0F9B ₁₆									
0F9C ₁₆									
0F9D ₁₆									
0F9E ₁₆									
0F9F ₁₆									
0FA0 ₁₆									
0FA1 ₁₆									
0FA2 ₁₆									
0FA3 ₁₆									
0FA4 ₁₆									
0FA5 ₁₆									
0FA6 ₁₆									
0FA7 ₁₆									
0FA8 ₁₆									
0FA9 ₁₆									
0FAA ₁₆									
0FAB ₁₆									
0FAC ₁₆									
0FAD ₁₆									
0FAE ₁₆									
0FAF ₁₆									

Note:  shaded area is used for gradation display data.

Fig. 46 Example of using FLD automatic display RAM in 16-timing•gradation display mode

HARDWARE

FUNCTIONAL DESCRIPTION

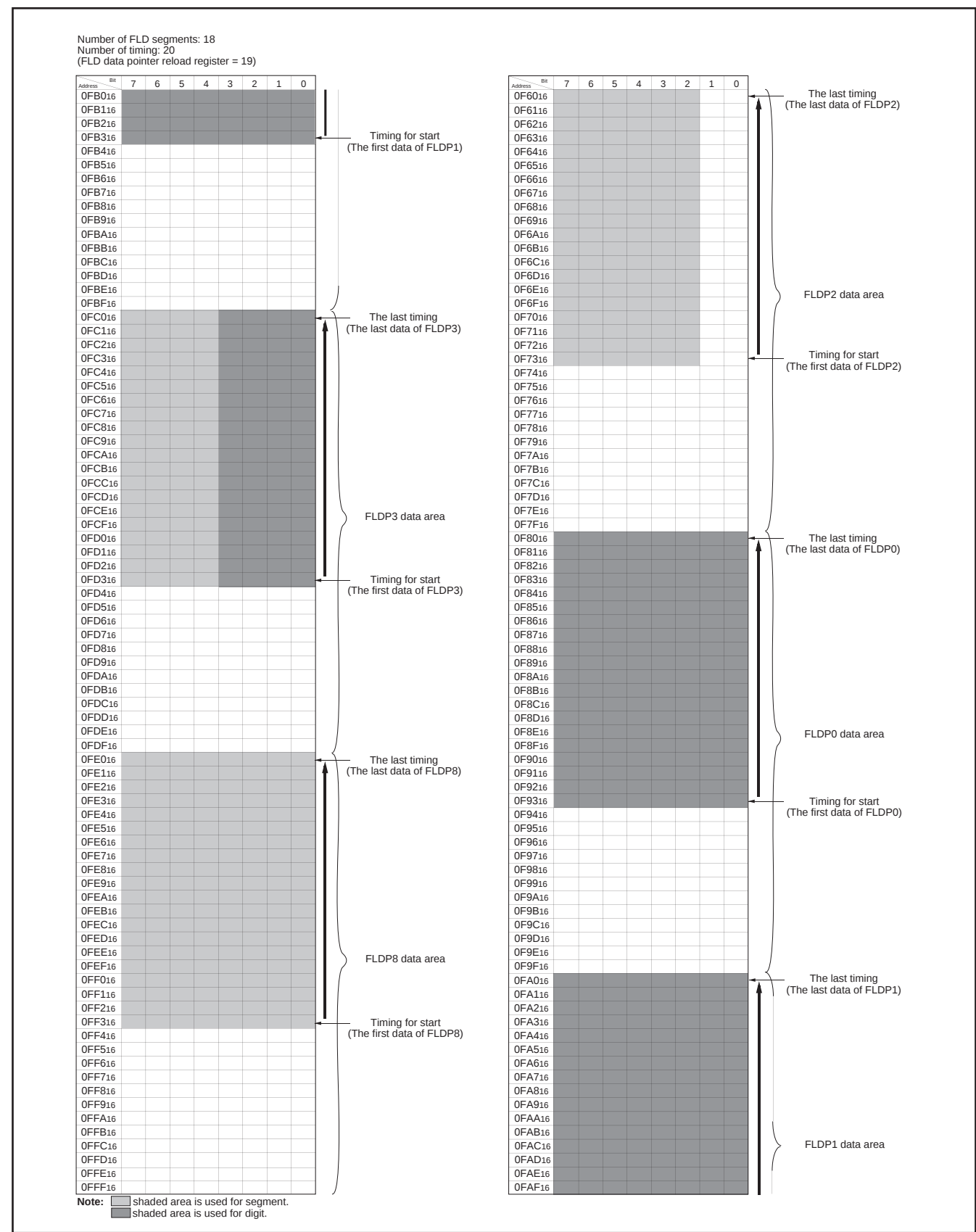


Fig. 47 Example of using FLD automatic display RAM in 32-timing mode

Digit data protect function

The FLD automatic display RAM is provided with a data protect function that disables the RAM area data to be rewritten as digit data.

This function can disable data from being written in optional bits in the RAM area corresponding to P1 to P3. A programming load can be reduced by protecting an area that requires no change after data such as digit data is written.

Write digit data beforehand; then set "1" in the corresponding bits. With this, the setting is completed.

The data protect area becomes the maximum RAM area of P1 and P3. For example, when bit 0 of P1 is protected in the 16-timing•ordinary mode, bits 0 of RAM addresses 0FD0₁₆ to 0FDF₁₆ can be protected. Likewise, in the 16-timing•gradation display mode, bits 0 of addresses 0FD0₁₆ to 0FDF₁₆ and 0F80₁₆ to 0F8F₁₆ can be protected. In the 32-timing mode, bits 0 of addresses 0FA0₁₆ to 0FBF₁₆ can be protected.

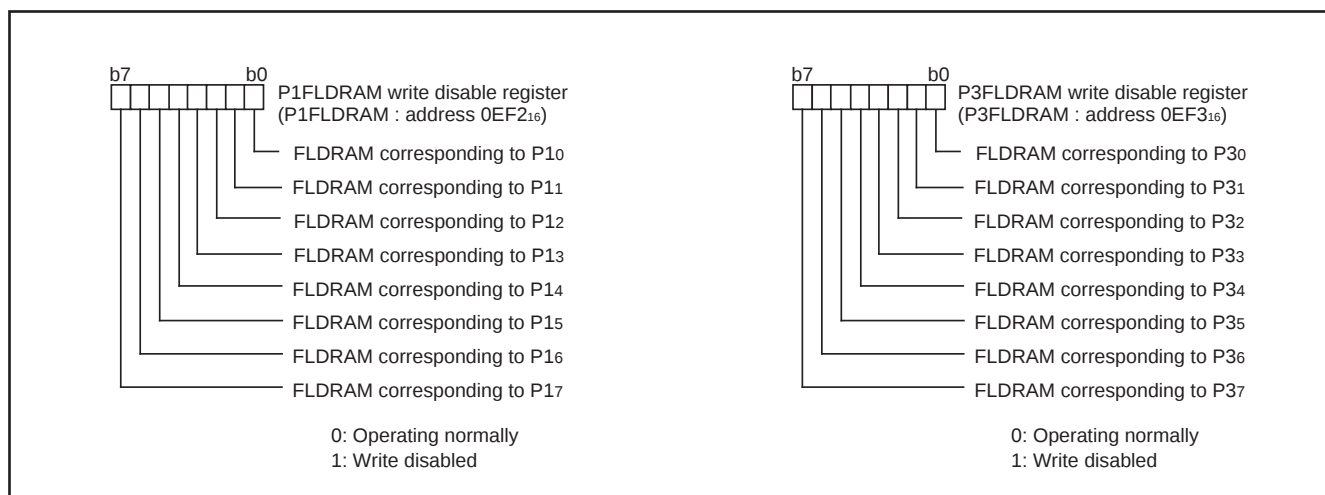


Fig. 48 Structure of FLD RAM write disable register

HARDWARE

FUNCTIONAL DESCRIPTION

Setting method when using the grid scan type FLD

When using the grid scan type FLD, set “1” in the RAM area corresponding to the digit ports that output “1” at each timing. Set “0” in the RAM area corresponding to the other digit ports.

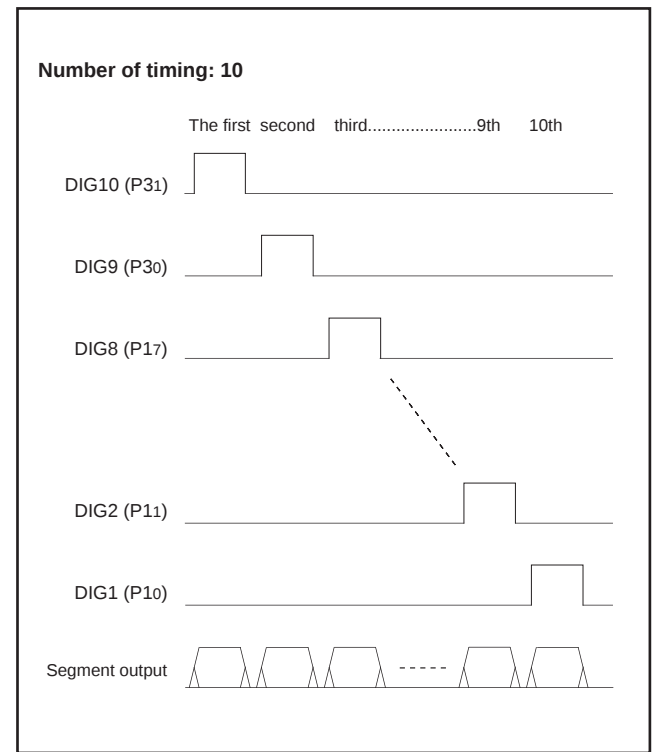


Fig. 49 Example of digit timing using grid scan type

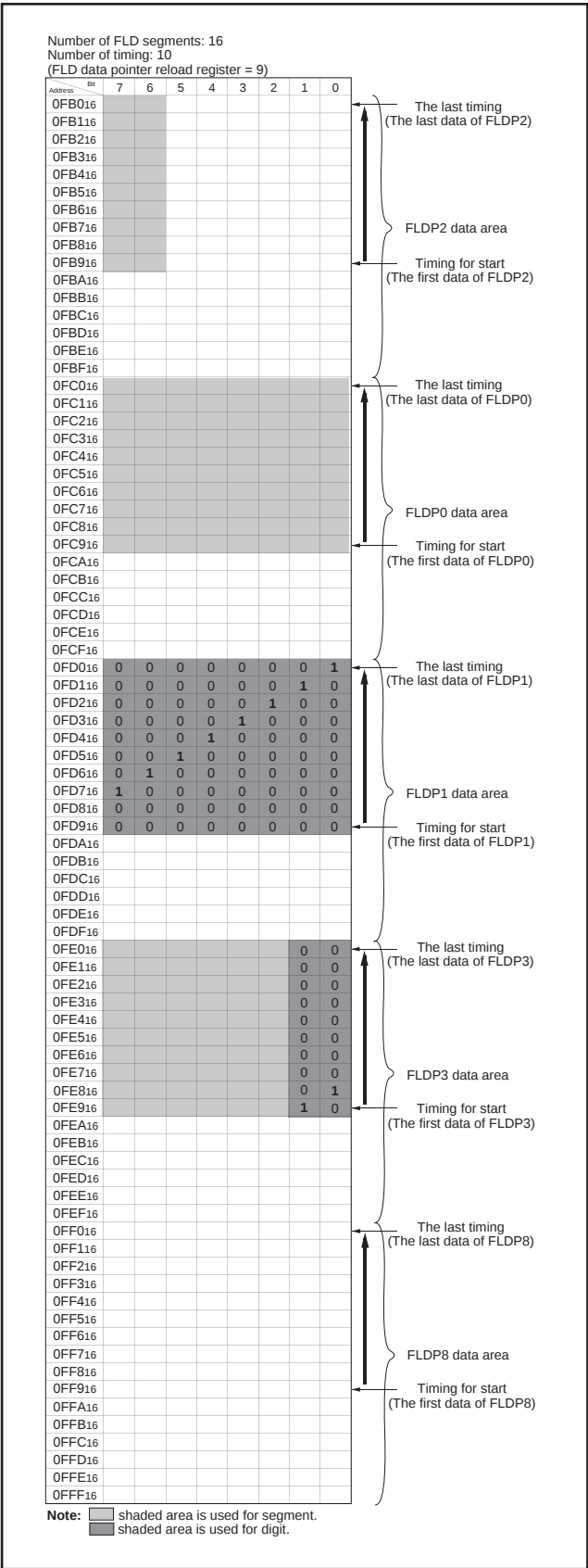


Fig. 50 Example of using FLD automatic display RAM using grid scan type

Timing setting

Each timing is set by the FLDC mode register, Tdisp time set register, Toff1 time set register, and Toff2 time set register.

•Tdisp time setting

Set the Tdisp time by the Tdisp counter count source selection bit of the FLDC mode register and the Tdisp time set register. Supposing that the value of the Tdisp time set register is n , the Tdisp time is represented as $Tdisp = (n+1) \times t$ (t : count source synchronization).

When the Tdisp counter count source selection bit of the FLDC mode register is "0" and the value of the Tdisp time set register is 200 (C8₁₆), the Tdisp time is: $Tdisp = (200+1) \times 4$ (at $X_{IN} = 4$ MHz) = 804 μ s. When reading the Tdisp time set register, the value in the counter is read out.

•Toff1 time setting

Set the Toff1 time by the Toff1 time set register.

Supposing that the value of the Toff1 time set register is n_1 , the Toff1 time is represented as $Toff1 = n_1 \times t$.

When the Tdisp counter count source selection bit of the FLDC mode register is "0" and the value of the Toff1 time set register is 30 (1E₁₆), $Toff1 = 30 \times 4$ (at $X_{IN} = 4$ MHz) = 120 μ s.

Set a value of 03₁₆ or more to the Toff1 time set register (address 0EF6₁₆).

•Toff2 time setting

Set the Toff2 time by the Toff2 time set register.

Supposing that the value of the Toff2 time set register is n_2 , the Toff2 time is represented as $Toff2 = n_2 \times t$.

When the Tdisp counter count source selection bit of the FLDC mode register is "0" and the value of the Toff2 time set register is 180 (B4₁₆), $Toff2 = 180 \times 4$ (at $X_{IN} = 4$ MHz) = 720 μ s.

This Toff2 time setting is valid only for FLD ports which are in the gradation display mode and whose gradation display control RAM value is "1."

When setting "1" to bit 7 of the P8FLD output control register (address 0EFC₁₆), set a value of 03₁₆ or more to the Toff2 time set register (address 0EF7₁₆).

FLD automatic display start

To perform FLD automatic display, set the following registers.

- Port P0FLD/port switch register
- Port P2FLD/port switch register
- Port P8FLD/port switch register
- FLDC mode register
- Tdisp time set register
- Toff1 time set register
- Toff2 time set register
- FLD data pointer

FLD automatic display mode is selected by writing "1" to the bit 0 of the FLDC mode register (address 0EF4₁₆), and the automatic display is started by writing "1" to bit 1. During FLD automatic display, bit 1 of the FLDC mode register (address 0EF4₁₆) always keeps "1," and FLD automatic display can be interrupted by writing "0" to bit 1.

Key-scan

When a key-scan is performed with the segment during key-scan blanking period Tscan, take the following sequence:

1. Write "0" to bit 0 of the FLDC mode register (address 0EF4₁₆).
2. Set the port corresponding to the segment for key-scan to the output port.
3. Perform the key-scan.
4. After the key-scan is performed, write "1" to bit 0 of FLDC mode register (address 0EF4₁₆).

■ Note

When performing a key-scan according to the above step 1 to 4, take the following points into consideration.

1. Do not set "0" in bit 1 of the FLDC mode register (address 0EF4₁₆).
2. Do not set "1" in the ports corresponding to digits.

HARDWARE

FUNCTIONAL DESCRIPTION

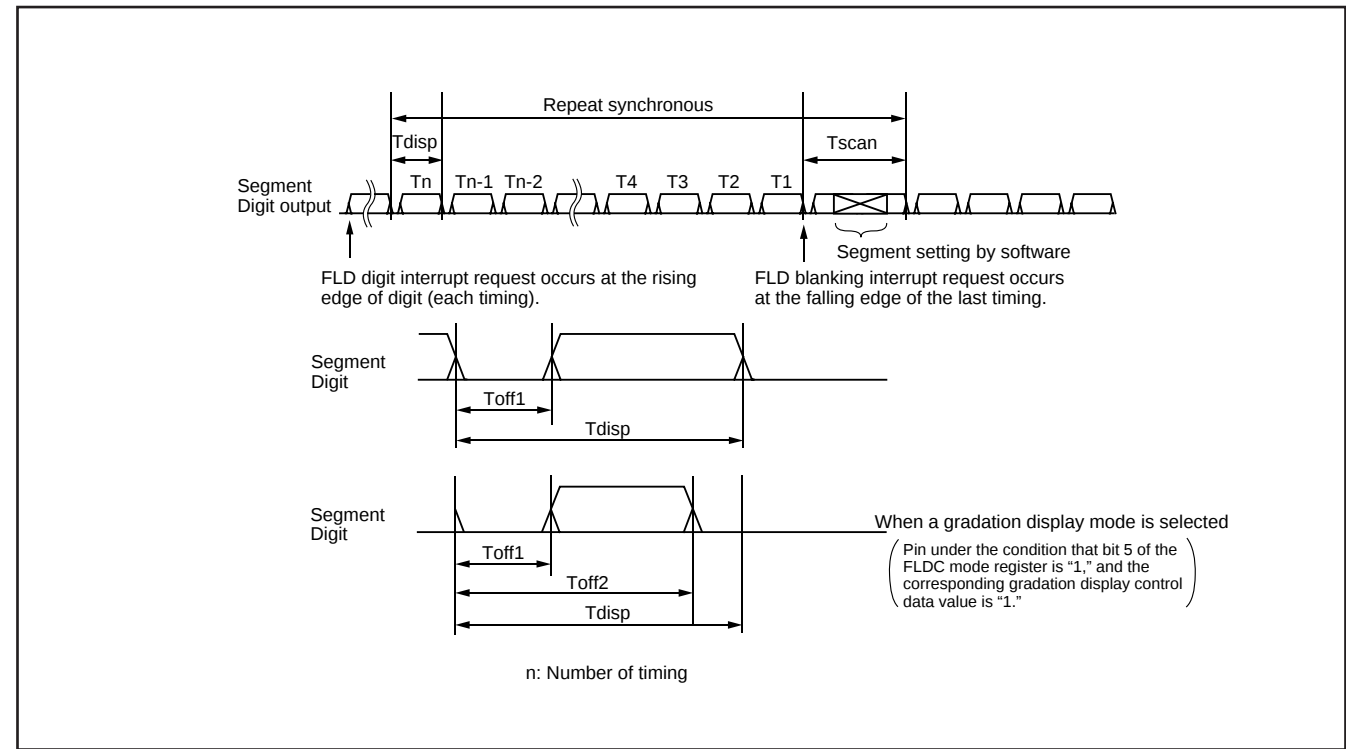


Fig. 51 FLDC timing

P84 to P87 FLD output reverse function

P84 to P87 are provided with a function to reverse the polarity of the FLD output. This function is useful in adjusting the polarity when using an externally installed driver.

The output polarity can be reversed by setting "1" to bit 0 of the port P8 FLD output control register.

P84 to P87 FLDRAM write disable function

This function can disable writing data in the RAM area corresponding to P84 to P87. This function can be set by setting "1" to bit 1 of the port P8FLD output control register (address 0EFC16).

P84 to P87 Toff invalid function

P84 to P87 can output waveform in which Toff is invalid, when P84 to P87 is selected FLD ports (See Figure 52).

The function is useful when using a 4 bits →16 bits decoder. The Toff can be invalid by setting "1" to bit 2 of the port P8FLD output control register (address 0EFC16).

P84 to P87 output delay function

P84 to P87 can output waveform in which is delayed for 16 μs, when selecting FLD port and selecting Toff invalid function (See Figure 52). When using a 4 bits →16 bits decoder, the function can be useful for prevention of leak radiation caused by phase discrepancy between segment output waveform and digit output waveform. This function can be set by setting "1" to bit 3 of the port P8FLD output control register (address 0EFC16).

Dimmer signal output function

P63 can output the dimmer signal. When using a 4 bits →16 bits decoder, the dimmer signal can be used as a control signal for a 4 bits →16 bits decoder. When using M35501FP, the dimmer signal can be used as the CLK signal. The dimmer signal can be output by setting "1" to bit 4 of the port P8FLD output control register (address 0EFC16).

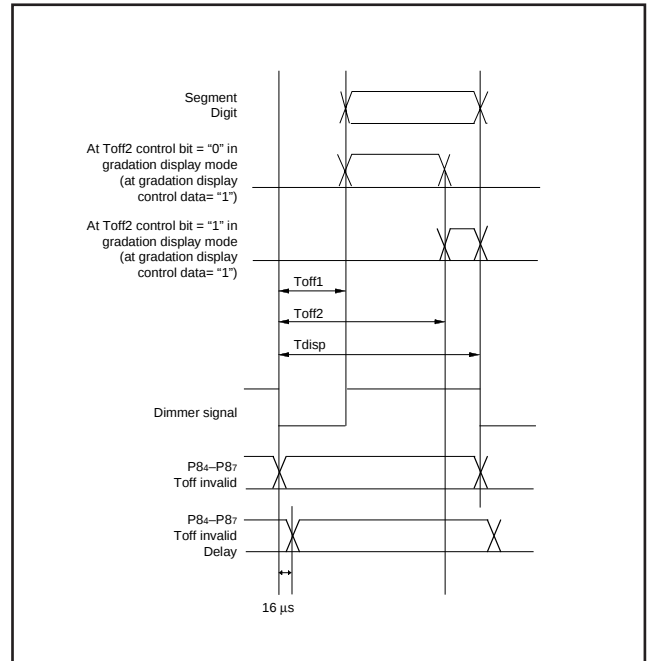


Fig. 52 P84 to P87 FLD output waveform

Toff2 SET/RESET change function

The value of the Toff2 time set register is valid when gradation display mode is selected. The FLD ports output (set) the data of display RAM at the end of the Toff1 time and output "0" (reset) at the end of the Toff2 time, when bit 7 of the port P8FLD output control register is "0".

The FLD ports output (set) the data of display RAM at the end of the Toff2 time and output "0" (reset) at the end of Tdisp time, when bit 7 of the port P8FLD output control register is "1".

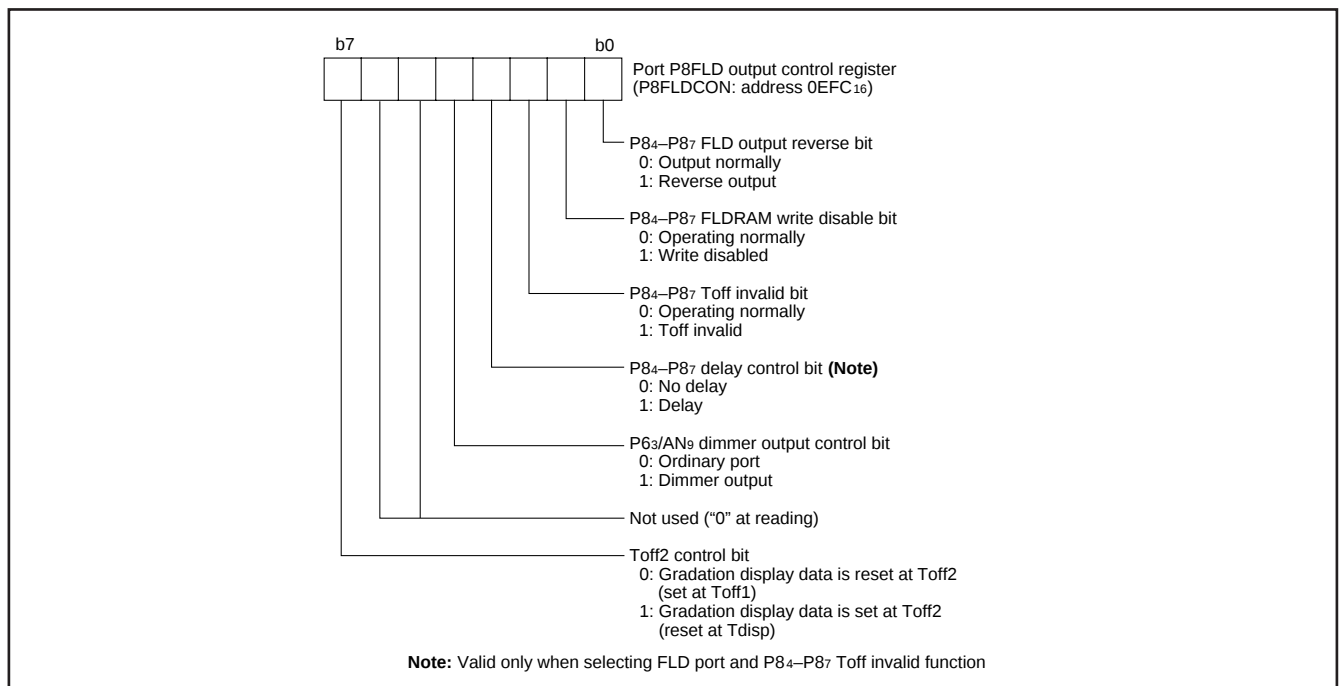


Fig. 53 Structure of port P8 FLD output control register

HARDWARE

FUNCTIONAL DESCRIPTION

A-D Converter

The 38B5 group has a 10-bit A-D converter. The A-D converter performs successive approximation conversion.

[A-D Conversion Register] AD

One of these registers is a high-order register, and the other is a low-order register. The high-order 8 bits of a conversion result is stored in the A-D conversion register (high-order) (address 0034₁₆), and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the A-D conversion register (low-order) (address 0033₁₆). During A-D conversion, do not read these registers.

[A-D Control Register] ADCON

This register controls A-D converter. Bits 3 to 0 are analog input pin selection bits. Bit 4 is an AD conversion completion bit and "0" during A-D conversion. This bit is set to "1" upon completion of A-D conversion.

A-D conversion is started by setting "0" in this bit.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF}, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports P7₇/AN₇–P7₀/AN₀, and P6₅/SSTB₁/AN₁₁–P6₂/SRDY₁/AN₈ and inputs it to the comparator.

When port P6₄ is selected as an analog input pin, an external interrupt function (INT₄) is invalid.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD

conversion interrupt request bit to "1."

Note that the comparator is constructed linked to a capacitor, so set $f(X_{IN})$ to at least 250 kHz during A-D conversion. Use a CPU system clock dividing the main clock X_{IN} as the internal system clock.

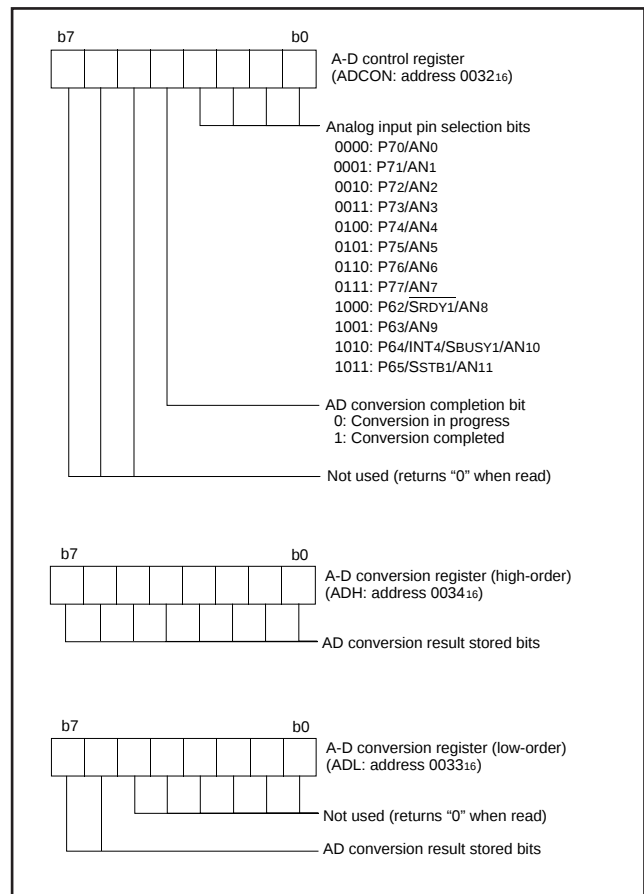


Fig. 54 Structure of A-D control register

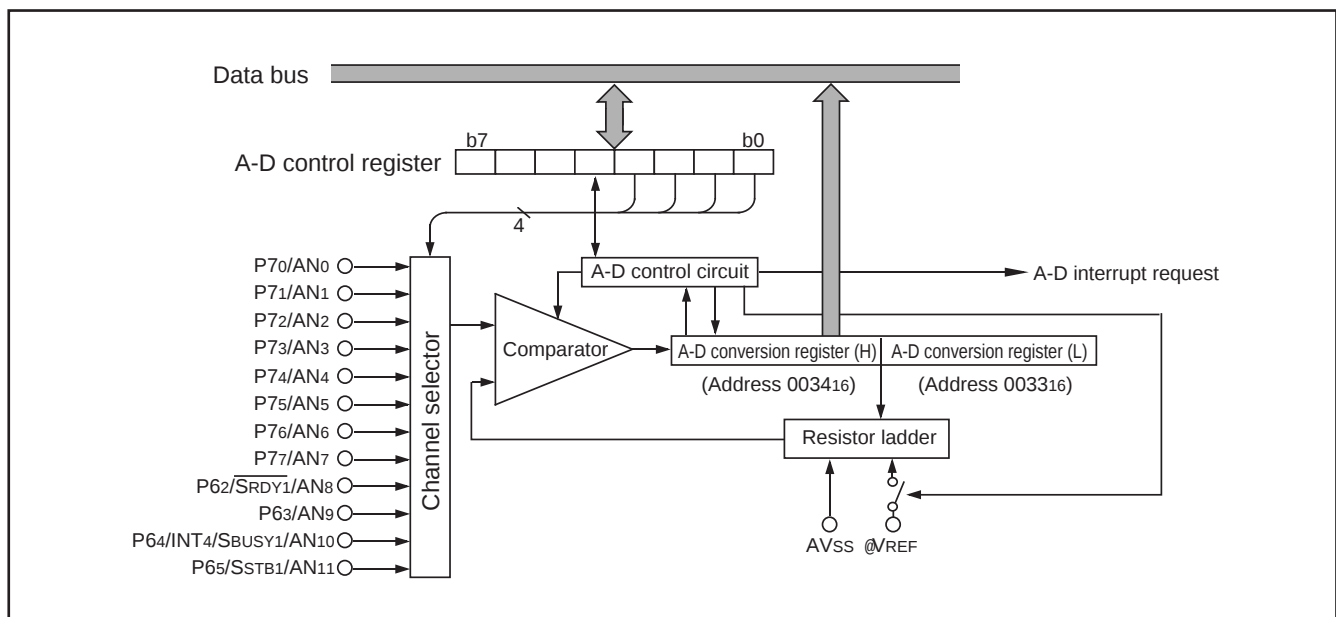


Fig. 55 Block diagram of A-D converter

Pulse Width Modulation (PWM)

The 38B5 group has a PWM function with a 14-bit resolution. When the oscillation frequency X_{IN} is 4 MHz, the minimum resolution bit width is 250 ns and the cycle period is 4096 μ s. The PWM timing generator supplies a PWM control signal based on a signal that is the frequency of the X_{IN} clock.

The explanation in the rest assumes $X_{IN} = 4$ MHz.

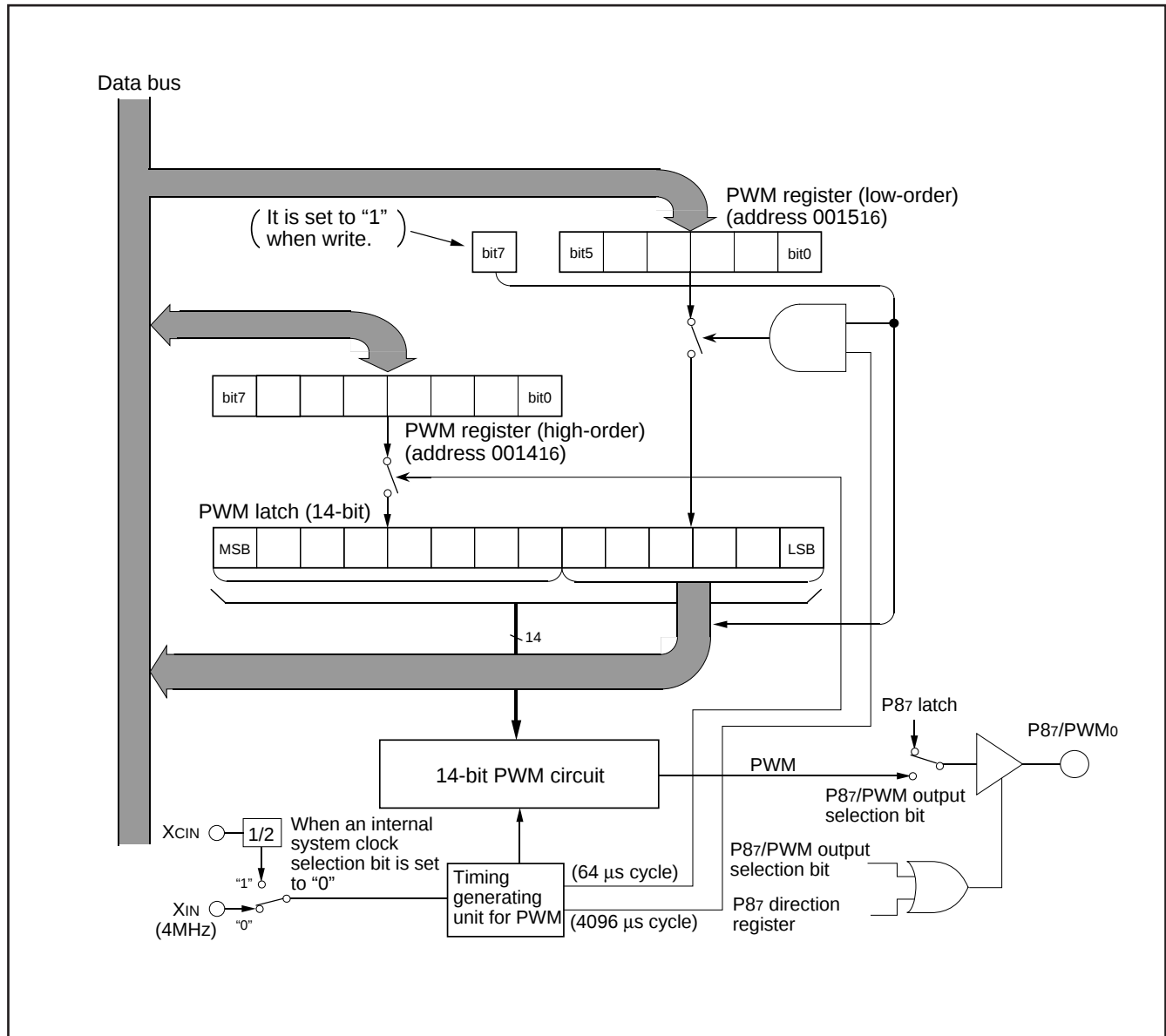


Fig. 56 PWM block diagram

HARDWARE

FUNCTIONAL DESCRIPTION

1. Data setup

The PWM output pin also function as port P87. Set port P87 to be the PWM output pin by setting bit 0 of the PWM control register (address 0026₁₆) to "1." The high-order 8 bits of output data are set in the high-order PWM register PWMH (address 0014₁₆) and the low-order 6 bits are set in the low-order PWM register PWML (address 0015₁₆).

2. PWM operation

The timing of the 14-bit PWM function is shown in Figure 57. The 14-bit PWM data is divided into the low-order 6 bits and the high-order 8 bits in the PWM latch. The high-order 8 bits of data determine how long an "H" level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period t is $256 \times \tau$ ($= 64 \mu\text{s}$) long. The signal's "H" has a length equal to N times τ , and its minimum resolution = 250 ns. The last bit of the sub-period becomes the ADD bit which is specified either "H" or "L," by the contents of PWML. As shown in Table 10, the ADD bit is decided either "H" or "L." That is, only in the sub-period t_m shown in Table 10 in the PWM cycle period $T = 64t$, the "H" duration is lengthened during the minimum resolution width τ period in comparison with the other period. For example, if the high-order eight bits of the 14-bit data are "03₁₆" and the low-order six bits are "05₁₆," the length of the "H" level output in sub-periods t_8 , t_{24} , t_{32} , t_{40} and t_{56} is 4τ , and its length 3τ in all other sub-periods. Time at the "H" level of each sub-period almost becomes equal because the time becomes length set in the high-order 8 bits or becomes the value plus τ , and this sub-period t ($= 64 \mu\text{s}$, approximate 15.6 kHz) becomes cycle period approximately.

3. Transfer from register to latch

Data written to the PWML register is transferred to the PWM latch once in each PWM period (every 4096 μs), and data written to the PWMH register is transferred to the PWM latch once in each sub-period (every 64 μs). When the PWML register is read, the contents of the latch are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed; the transfer is completed when bit 7 is "0."

Table 10 Relationship between low-order 6-bit data and setting period of ADD bit

Low-order 6-bit data	Sub-periods t_m lengthened ($m = 0$ to 63)
0 0 0 0 0 0 ^{LSB}	None
0 0 0 0 0 1	$m = 32$
0 0 0 0 1 0	$m = 16, 48$
0 0 0 1 0 0	$m = 8, 24, 40, 56$
0 0 1 0 0 0	$m = 4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m = 1, 3, 5, 7, \dots, 57, 59, 61, 63$

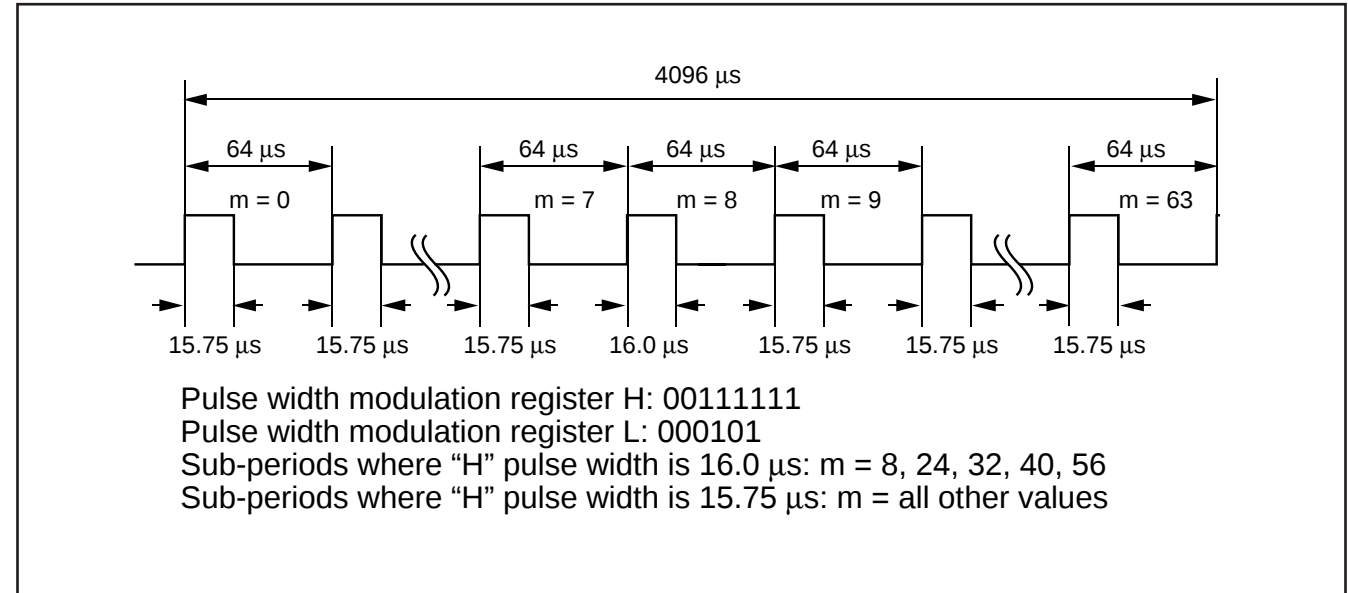


Fig. 57 PWM timing



HARDWARE

FUNCTIONAL DESCRIPTION

Interrupt Interval Determination Function

The 38B5 group has an interrupt interval determination circuit.

This interrupt interval determination circuit has an 8-bit binary up counter. Using this counter, it determines a duration of time from the rising edge (falling edge) of an input signal pulse on the P47/INT2 pin to the rising edge (falling edge) of the signal pulse that is input next. How to determine the interrupt interval is described below.

1. Enable the INT2 interrupt by setting bit 2 of the interrupt control register 1 (address 003E16). Select the rising interval or falling interval by setting bit 2 of the interrupt edge selection register (address 003A16).
2. Set bit 0 of the interrupt interval determination control register (address 003116) to "1" (interrupt interval determination operating).
3. Select the sampling clock of 8-bit binary up counter by setting bit 1 of the interrupt interval determination control register. When writing "0," $f(X_{IN})/128$ is selected (the sampling interval: 32 μ s at $f(X_{IN}) = 4.19$ MHz); when "1," $f(X_{IN})/256$ is selected (the sampling interval: 64 μ s at $f(X_{IN}) = 4.19$ MHz).
4. When the signal of polarity which is set on the INT2 pin (rising or falling edge) is input, the 8-bit binary up counter starts counting up of the selected counter sampling clock.
5. When the signal of polarity above 4 is input again, the value of the 8-bit binary up counter is transferred to the interrupt interval determination register (address 003016), and the remote control interrupt request occurs. Immediately after that, the 8-bit binary up counter continues to count up again from "0016."
6. When count value reaches "FF16," the 8-bit binary up counter stops counting up. Then, simultaneously when the next counter sampling clock is input, the counter sets value "FF16" to the interrupt interval determination register to generate the counter overflow interrupt request.

Noise filter

The P47/INT2 pin builds in the noise filter.

The noise filter operation is described below.

1. Select the sampling clock of the input signal with bits 2 and 3 of the interrupt interval determination control register. When not using the noise filter, set "00."
2. The P47/INT2 input signal is sampled in synchronization with the selected clock. When sampling the same level signal in a series of three sampling, the signal is recognized as the interrupt signal, and the interrupt request occurs. When setting bit 4 of interrupt interval determination control register to "1," the interrupt request can occur at both rising and falling edges. When using the noise filter, set the minimum pulse width of the INT2 input signal to 3 cycles or more of the sample clock.

Note: In the low-speed mode ($CM7 = 1$), the interrupt interval determination function cannot operate.

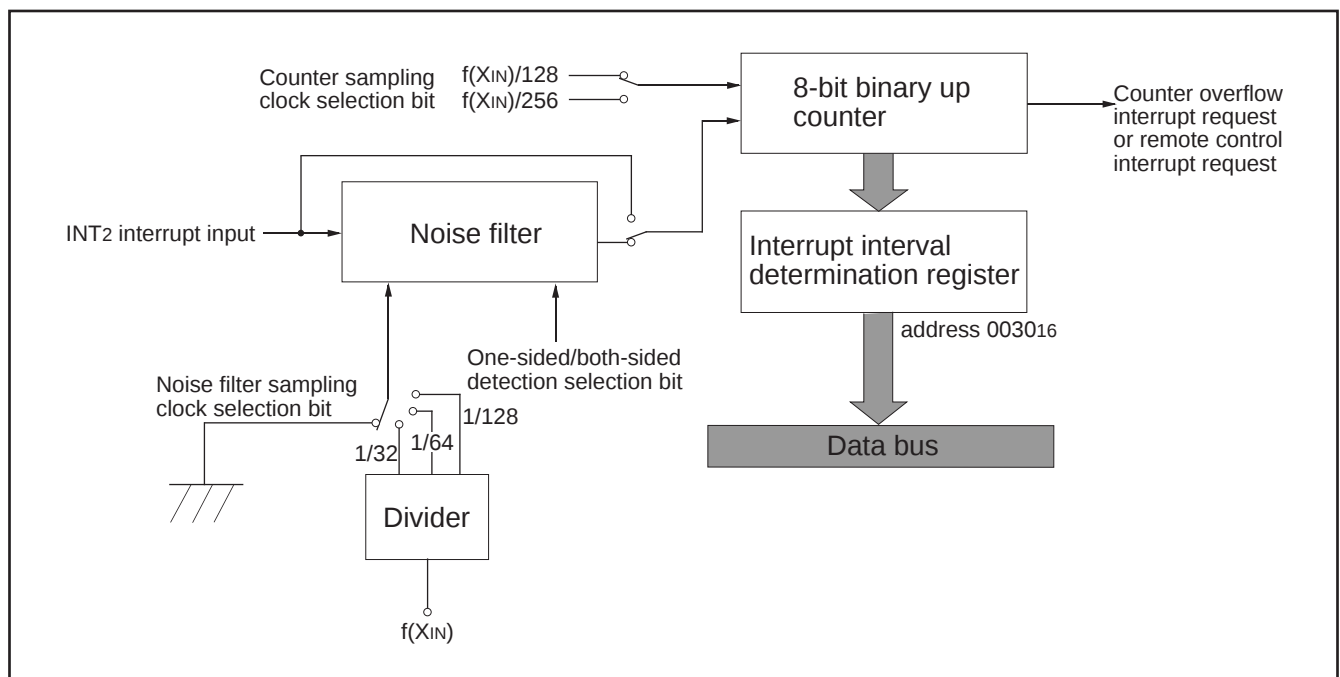


Fig. 60 Interrupt interval determination circuit block diagram

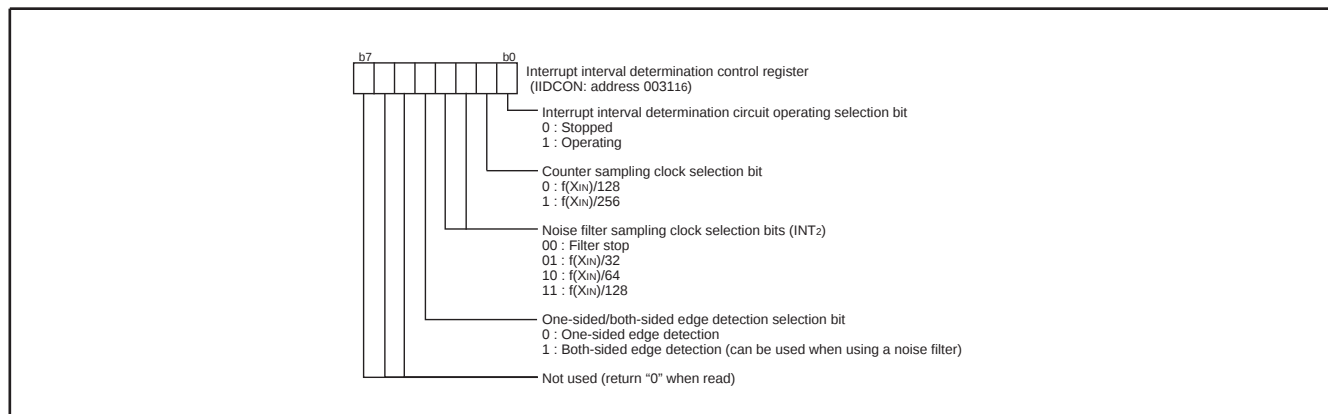


Fig. 61 Structure of interrupt interval determination control register

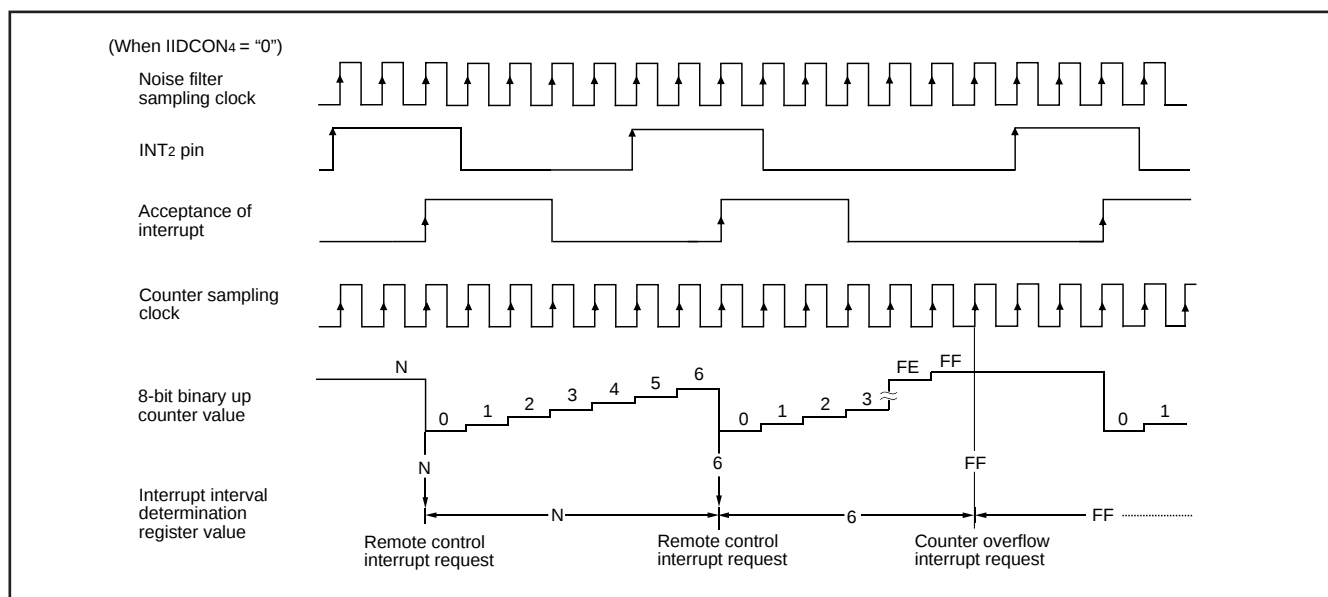


Fig. 62 Interrupt interval determination operation example (at rising edge active)

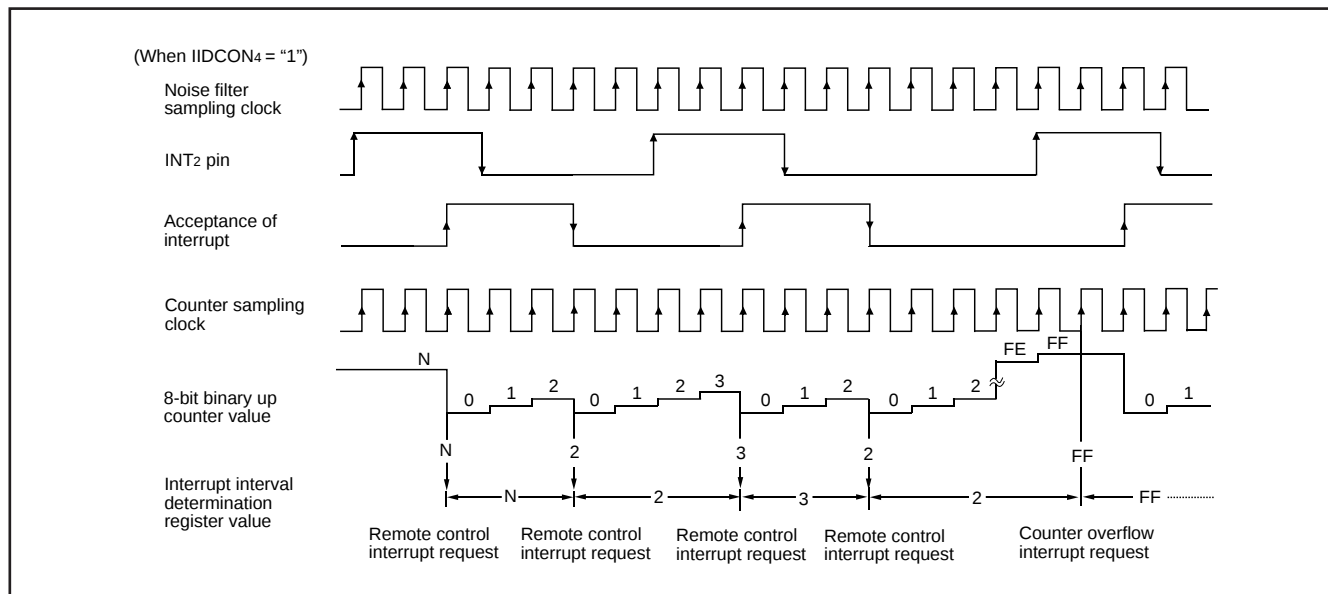


Fig. 63 Interrupt interval determination operation example (at both-sided edge active)

HARDWARE

FUNCTIONAL DESCRIPTION

Watchdog Timer

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software runaway). The watchdog timer consists of an 8-bit watchdog timer L and a 12-bit watchdog timer H.

●Standard operation of watchdog timer

When any data is not written into the watchdog timer control register (address 002B₁₆) after resetting, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (address 002B₁₆) and an internal reset occurs at an underflow of the watchdog timer H. Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 002B₁₆) may be started before an underflow. When the watchdog timer control register (address 002B₁₆) is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

(1) Initial value of watchdog timer

At reset or writing to the watchdog timer control register (address 002B₁₆), a watchdog timer H is set to "FFF₁₆" and a watchdog timer L to "FF₁₆."

(2) Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address 002B₁₆) permits selecting a watchdog timer H count source. When this bit is set to

"0," the underflow signal of watchdog timer L becomes the count source. The detection time is set then to $f(X_{IN}) = 2.1 \text{ s}$ at 4 MHz frequency and $f(X_{CIN}) = 512 \text{ s}$ at 32 kHz frequency.

When this bit is set to "1," the count source becomes the signal divided by 8 for $f(X_{IN})$ (or divided by 16 for $f(X_{CIN})$). The detection time in this case is set to $f(X_{IN}) = 8.2 \text{ ms}$ at 4 MHz frequency and $f(X_{CIN}) = 2 \text{ s}$ at 32 KHz frequency. This bit is cleared to "0" after resetting.

(3) Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address 002B₁₆) permits disabling the STP instruction when the watchdog timer is in operation.

When this bit is "0," the STP instruction is enabled.

When this bit is "1," the STP instruction is disabled.

Once the STP instruction is executed, an internal resetting occurs.

When this bit is set to "1," it cannot be rewritten to "0" by program. This bit is cleared to "0" after resetting.

■ Note

When releasing the stop mode, the watchdog timer performs its count operation even in the stop release waiting time. Be careful not to cause the watchdog timer H to underflow in the stop release waiting time, for example, by writing data in the watchdog timer control register (address 002B₁₆) before executing the STP instruction.

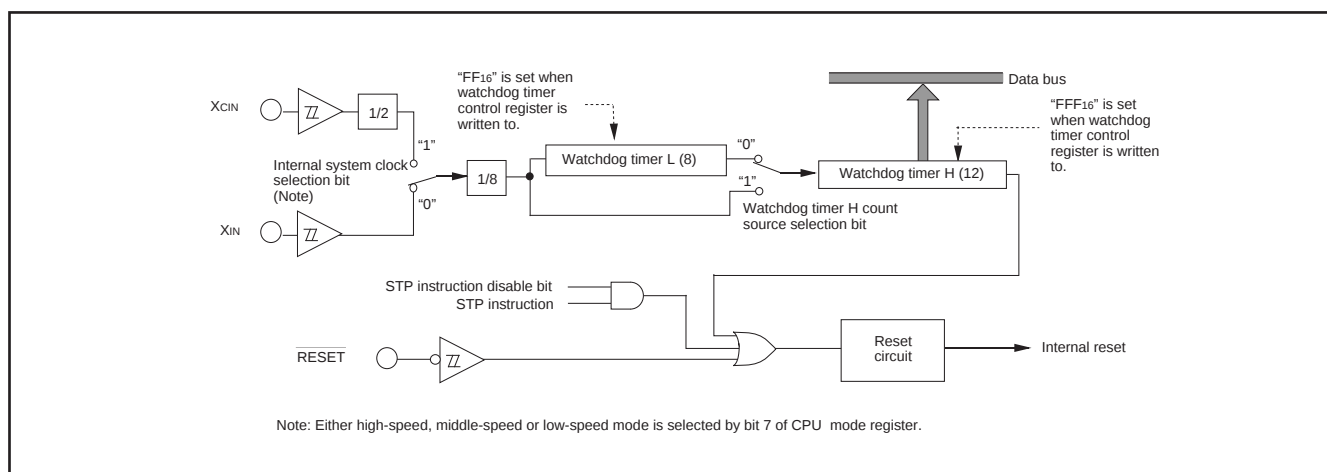


Fig. 64 Block diagram of watchdog timer

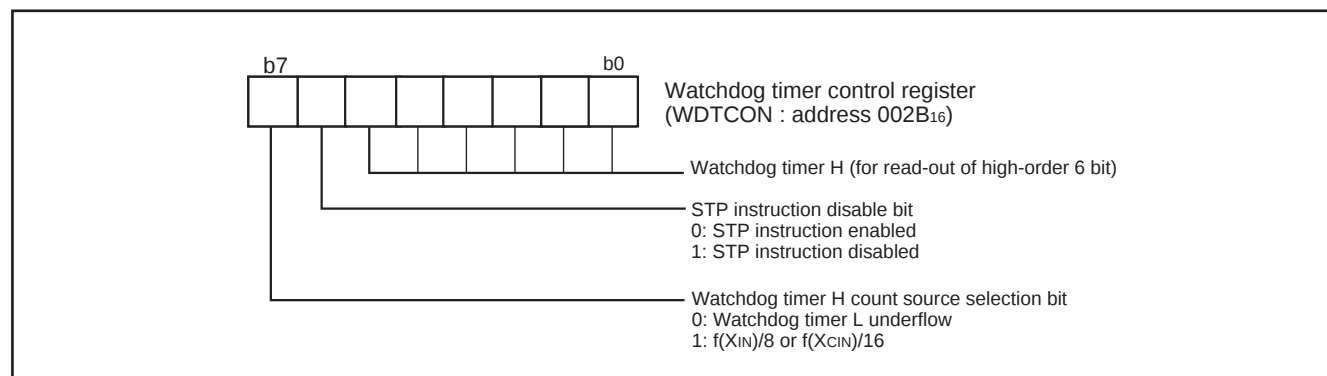


Fig. 65 Structure of watchdog timer control register

Buzzer Output Circuit

The 38B5 group has a buzzer output circuit. One of 1 kHz, 2 kHz and 4 kHz (at $X_{IN} = 4.19$ MHz) frequencies can be selected by the buzzer output control register (address 0EFD16). Either P43/Buz01 or P20/Buz02/FLD0 can be selected as a buzzer output port by the output port selection bits (b2 and b3 of address 0EFD16).

The buzzer output is controlled by the buzzer output ON/OFF bit (b4).

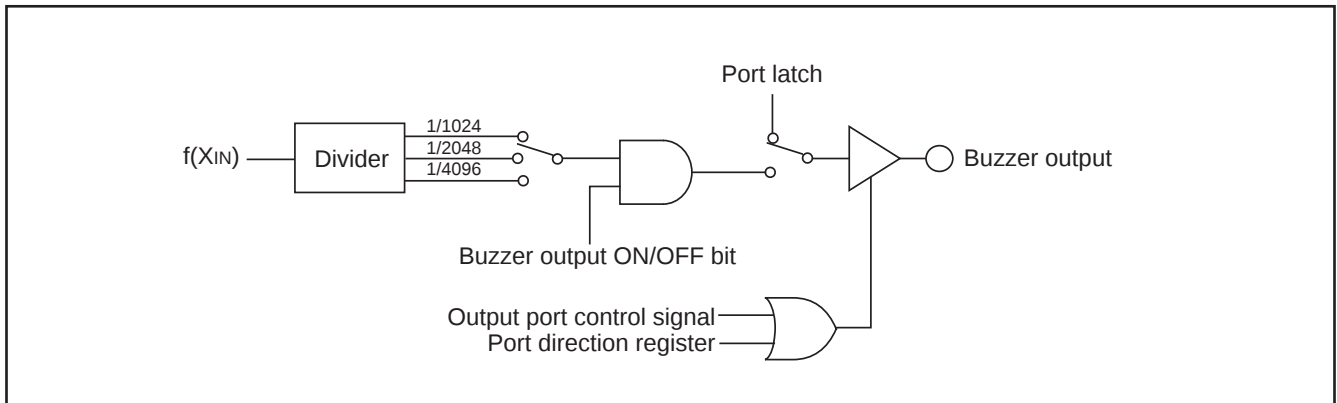


Fig. 66 Block diagram of buzzer output circuit

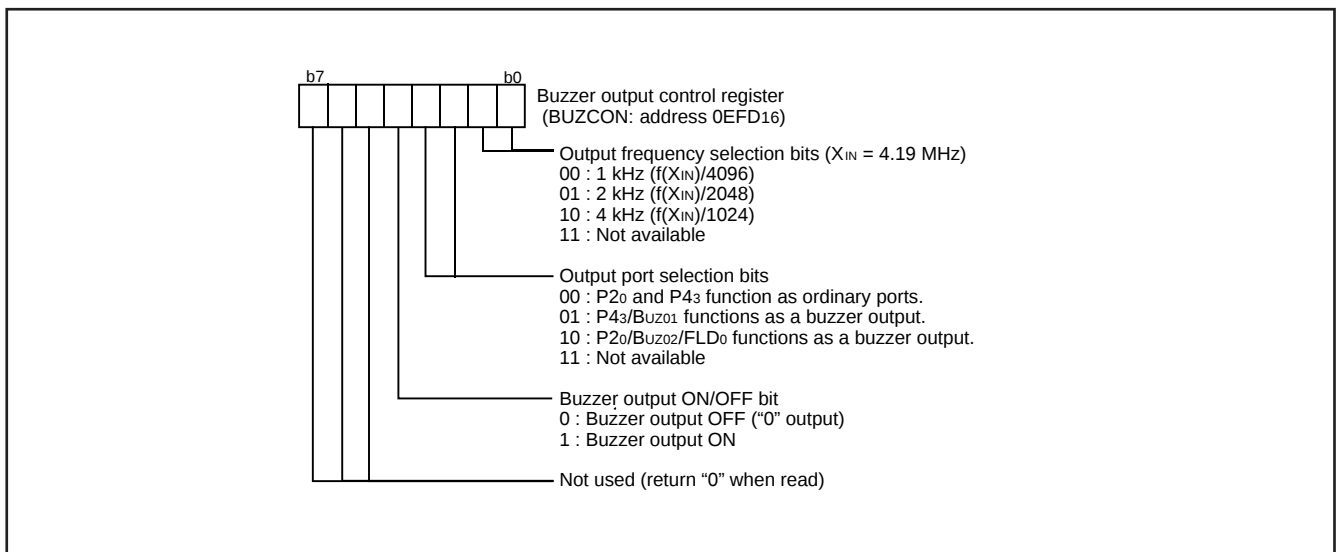


Fig. 67 Structure of buzzer output control register

HARDWARE

FUNCTIONAL DESCRIPTION

Reset Circuit

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage should be between 2.7 V and 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD_{16} (high-order byte) and address FFFC_{16} (low-order byte). Make sure that the reset input voltage is less than 0.5 V for V_{CC} of 2.7 V (switching to the high-speed mode, a power source voltage must be between 4.0 V and 5.5 V).

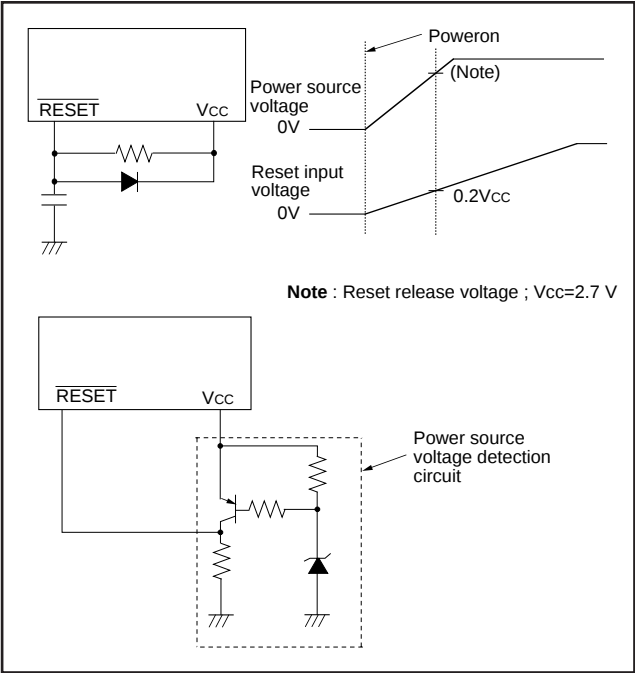


Fig. 68 Reset circuit example

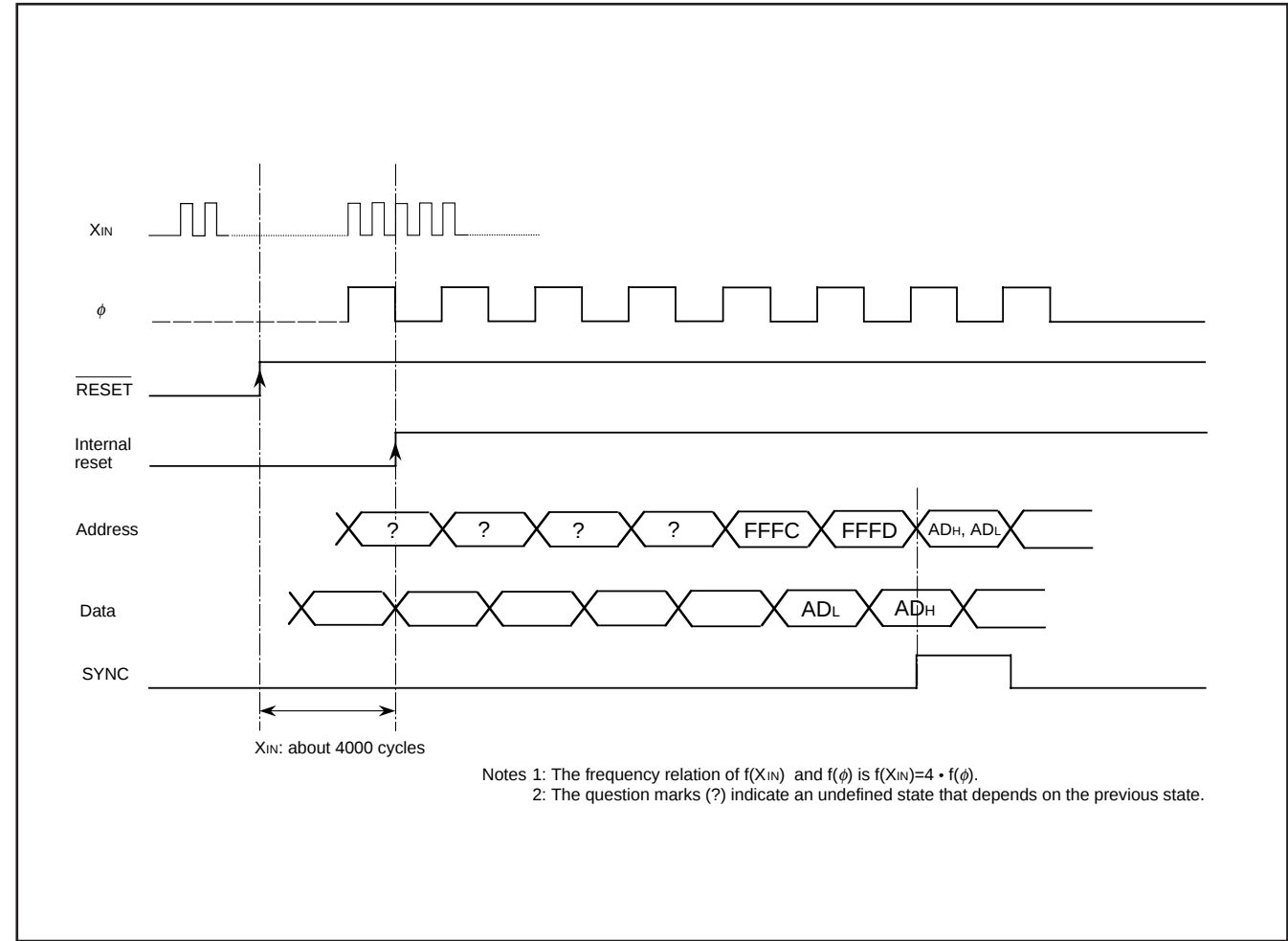


Fig. 69 Reset sequence

	Address	Register contents		Address	Register contents
(1) Port P0	0000 ₁₆	00 ₁₆	(33) Timer 34 mode register	0029 ₁₆	00 ₁₆
(2) Port P0 direction register	0001 ₁₆	00 ₁₆	(34) Timer 56 mode register	002A ₁₆	00 ₁₆
(3) Port P1	0002 ₁₆	00 ₁₆	(35) Watchdog timer control register	002B ₁₆	3F ₁₆
(4) Port P2	0004 ₁₆	00 ₁₆	(36) Timer X (low-order)	002C ₁₆	FF ₁₆
(5) Port P2 direction register	0005 ₁₆	00 ₁₆	(37) Timer X (high-order)	002D ₁₆	FF ₁₆
(6) Port P3	0006 ₁₆	00 ₁₆	(38) Timer X mode register 1	002E ₁₆	00 ₁₆
(7) Port P4	0008 ₁₆	00 ₁₆	(39) Timer X mode register 2	002F ₁₆	00 ₁₆
(8) Port P4 direction register	0009 ₁₆	00 ₁₆	(40) Interrupt interval determination control register	0031 ₁₆	00 ₁₆
(9) Port P5	000A ₁₆	00 ₁₆	(41) A-D control register	0032 ₁₆	10 ₁₆
(10) Port P5 direction register	000B ₁₆	00 ₁₆	(42) Interrupt source switch register	0039 ₁₆	00 ₁₆
(11) Port P6	000C ₁₆	00 ₁₆	(43) Interrupt edge selection register	003A ₁₆	00 ₁₆
(12) Port P6 direction register	000D ₁₆	00 ₁₆	(44) CPU mode register	003B ₁₆	01001000
(13) Port P7	000E ₁₆	00 ₁₆	(45) Interrupt request register 1	003C ₁₆	00 ₁₆
(14) Port P7 direction register	000F ₁₆	00 ₁₆	(46) Interrupt request register 2	003D ₁₆	00 ₁₆
(15) Port P8	0010 ₁₆	00 ₁₆	(47) Interrupt control register 1	003E ₁₆	00 ₁₆
(16) Port P8 direction register	0011 ₁₆	00 ₁₆	(48) Interrupt control register 2	003F ₁₆	00 ₁₆
(17) Port P9	0012 ₁₆	00 ₁₆	(49) Pull-up control register 1	0EF0 ₁₆	00 ₁₆
(18) Port P9 direction register	0013 ₁₆	00 ₁₆	(50) Pull-up control register 2	0EF1 ₁₆	00 ₁₆
(19) UART control register	0017 ₁₆	80 ₁₆	(51) P1FLDRAM write disable register	0EF2 ₁₆	00 ₁₆
(20) Serial I/O1 control register 1	0019 ₁₆	00 ₁₆	(52) P3FLDRAM write disable register	0EF3 ₁₆	00 ₁₆
(21) Serial I/O1 control register 2	001A ₁₆	00 ₁₆	(53) FLDC mode register	0EF4 ₁₆	00 ₁₆
(22) Serial I/O1 control register 3	001C ₁₆	00 ₁₆	(54) Tdisp time set register	0EF5 ₁₆	00 ₁₆
(23) Serial I/O2 control register	001D ₁₆	00 ₁₆	(55) Toff1 time set register	0EF6 ₁₆	FF ₁₆
(24) Serial I/O2 status register	001E ₁₆	80 ₁₆	(56) Toff2 time set register	0EF7 ₁₆	FF ₁₆
(25) Timer 1	0020 ₁₆	FF ₁₆	(57) Port P0FLD/port switch register	0EF9 ₁₆	00 ₁₆
(26) Timer 2	0021 ₁₆	01 ₁₆	(58) Port P2FLD/port switch register	0EFA ₁₆	00 ₁₆
(27) Timer 3	0022 ₁₆	FF ₁₆	(59) Port P8FLD/port switch register	0EFB ₁₆	00 ₁₆
(28) Timer 4	0023 ₁₆	FF ₁₆	(60) Port P8FLD output control register	0EFC ₁₆	00 ₁₆
(29) Timer 5	0024 ₁₆	FF ₁₆	(61) Buzzer output control register	0EFD ₁₆	00 ₁₆
(30) Timer 6	0025 ₁₆	FF ₁₆	(62) Processor status register	(PS)	XXXXX1XX
(31) PWM control register	0026 ₁₆	00 ₁₆	(63) Program counter	(PC _H)	FFFD ₁₆ contents
(32) Timer 12 mode register	0028 ₁₆	00 ₁₆		(PC _L)	FFFC ₁₆ contents

X: Not fixed

Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 70 Internal status at reset

HARDWARE

FUNCTIONAL DESCRIPTION

Clock Generating Circuit

The 38B5 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT} (X_{CIN} and X_{COUT}). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between X_{IN} and X_{OUT} since a feedback resistor exists on-chip. However, an external feedback resistor is needed between X_{CIN} and X_{COUT} .

Immediately after power on, only the X_{IN} oscillation circuit starts oscillating, and X_{CIN} and X_{COUT} pins function as I/O ports.

●Frequency control

(1) Middle-speed mode

The internal system clock is the frequency of X_{IN} divided by 4. After reset, this mode is selected.

(2) High-speed mode

The internal system clock is the frequency of X_{IN} .

(3) Low-speed mode

The internal system clock is the frequency of X_{CIN} divided by 2.

■Note

If you switch the mode between middle/high-speed and low-speed, stabilize both X_{IN} and X_{CIN} oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that $f(X_{IN}) > 3f(X_{CIN})$.

(4) Low power consumption mode

The low power consumption operation can be realized by stopping the main clock X_{IN} in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1." When the main clock X_{IN} is re-started (by setting the main clock stop bit to "0"), set enough time for oscillation to stabilize.

By clearing furthermore the X_{COUT} drivability selection bit (b3) of CPU mode register to "0," low power consumption operation of less than 200 μA ($f(X_{CIN}) = 32$ kHz) can be realized by reducing the drivability between X_{CIN} and X_{COUT} . At reset or during STP instruction execution this bit is set to "1" and a strong drivability that has an easy oscillation start is set.

●Oscillation control

(1) Stop mode

If the STP instruction is executed, the internal system clock stops at an "H" level, and X_{IN} and X_{CIN} oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116."

Either X_{IN} divided by 8 or X_{CIN} divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2. The bits of the timer 12 mode register are cleared to "0." Set the interrupt enable bits of the timer 1 and timer 2 to disabled ("0") before executing the STP instruction. Oscillator restarts when an external interrupt is received, but the internal system clock is not supplied to the CPU until timer 1 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait mode

If the WIT instruction is executed, the internal system clock stops at an "H" level. The states of X_{IN} and X_{CIN} are the same as the state before executing the WIT instruction. The internal system clock re-starts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

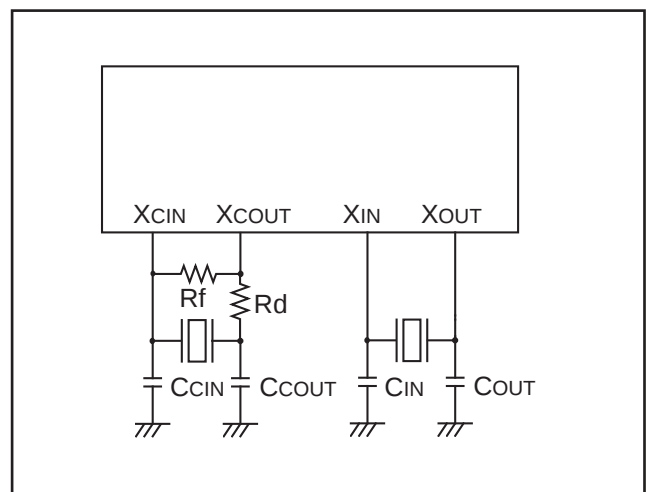


Fig. 71 Ceramic resonator circuit

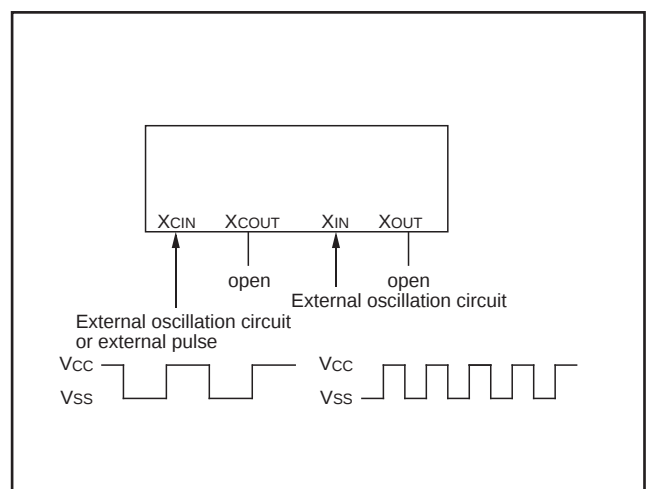
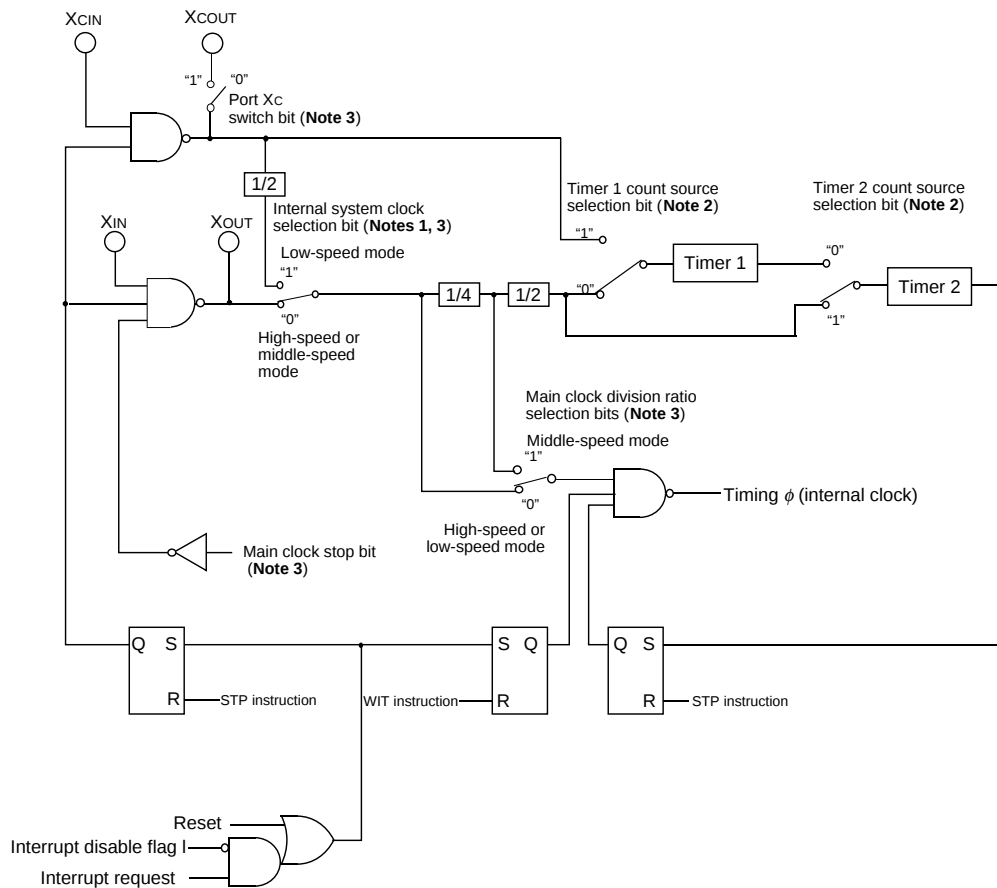


Fig. 72 External clock input circuit



Notes

- 1: When low-speed mode is selected, set the port Xc switch bit (b4) to "1".
- 2: Refer to the structure of the timer 12 mode register.
- 3: Refer to the structure of the CPU mode register.

Fig. 73 Clock generating circuit block diagram

HARDWARE

FUNCTIONAL DESCRIPTION

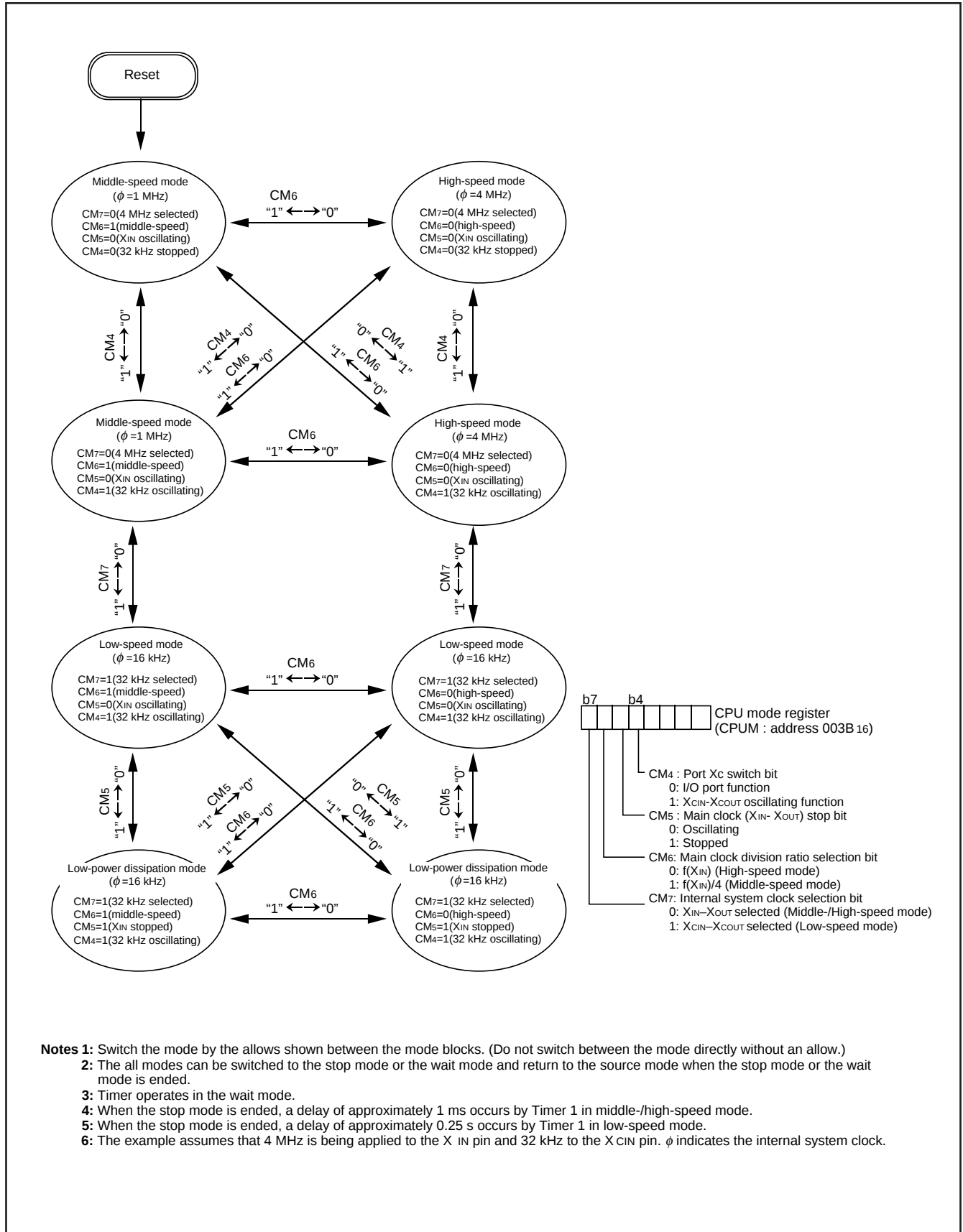


Fig. 74 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1," then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

- Using an external clock

When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing serial I/O transfer and serial I/O automatic transfer.

- Using an internal clock

When using an internal clock, set the synchronous clock to the internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer and serial I/O automatic transfer.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Therefore, make sure that $f(X_{IN})$ is at least on 250 kHz during an A-D conversion.

Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal system clock by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal system clock is the same of the X_{IN} frequency in high-speed mode.

At STP Instruction Release

At the STP instruction release, all bits of the timer 12 mode register are cleared.

The X_{COUT} drivability selection bit (the CPU mode register) is set to "1" (high drive) in order to start oscillating.

NOTES ON USE

Notes on Built-in EPROM Version

The P47 pin of the One Time PROM version or the EPROM version functions as the power source input pin of the internal EPROM.

Therefore, this pin is set at low input impedance, thereby being affected easily by noise.

To prevent a malfunction due to noise, insert a resistor (approx. 5 k Ω) in series with the P47 pin.

HARDWARE

DATA REQUIRED FOR MASK ORDERS/DATA REQUIRED FOR ROM WRITING ORDERS/ROM PROGRAMMING METHOD

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- (1) Mask ROM Order Confirmation Form
- (2) Mark Specification Form
- (3) Data to be written to ROM, in EPROM form (three identical copies)

DATA REQUIRED FOR ROM WRITING ORDERS

The following are necessary when ordering a ROM writing:

- (1) ROM Writing Confirmation Form
- (2) Mark Specification Form
- (3) Data to be written to ROM, in EPROM form (three identical copies)

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and the EPROM version can be read or programmed with a general purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 11 Special programming adapter

Package	Name of Programming Adapter
80P6N-A	PCA7438F-80A
80D0	PCA7438L-80A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 75 is recommended to verify programming.

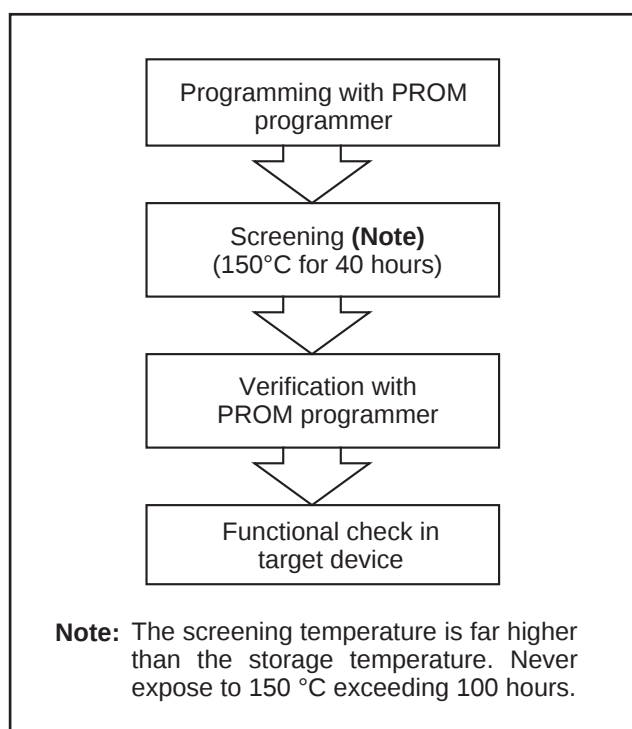


Fig. 75 Programming and testing of One Time PROM version

MASK OPTION OF PULL-DOWN RESISTOR (object product: M38B5MXH-XXXFP)

Whether built-in pull-down resistors are connected or not to high-breakdown voltage ports P20 to P27 and P80 to P83 can be specified in ordering mask ROM. The option type can be specified from among 8 types; A to G, P as shown Table 12.

Table 12 Mask option type of pull-down resistor

Option type	Connective port of pull-down resistor (connected at "1" writing)												Restriction
	P20	P21	P22	P23	P24	P25	P26	P27	P80	P81	P82	P83	
A (\$41)													
B (\$42)							1	1					
C (\$43)					1	1	1	1					
D (\$44)			1	1	1	1	1	1					
E (\$45)	1	1	1	1	1	1	1	1					
F (\$46)	1	1	1	1	1	1	1	1	1	1			
G (\$47)	1	1	1	1	1	1	1	1	1	1	1	1	
P (\$50)	1	1	1	1	1	1	1	1					(Note 4)

- Notes 1:** The electrical characteristics of high-breakdown voltage ports P20 to P27 and P80 to P83's built-in pull-down resistors are the same as that of high-breakdown voltage ports P00 to P07.
- 2:** The absolute maximum ratings of power dissipation may be exceed owing to the number of built-in pull-down resistor. After calculating the power dissipation, specify the option type.
- 3:** One time PROM version and EPROM version cannot be specified whether built-in pull-down resistors are connected or not likewise option type A.
- 4:** INT3 function and CNTR1 function cannot be used in the option type P.

Power Dissipation Calculating Method

● Fixed number depending on microcomputer's standard

- V_{OH} output fall voltage of high-breakdown port
2 V (max.); | Current value | = at 18 mA
- Resistor value 43 V / 900 μA = 48 kΩ (min.)
- Power dissipation of internal circuit (CPU, ROM, RAM etc.) = 5 V X 15 mA = 75 mW

● Fixed number depending on use condition

- Apply voltage to V_{EE} pin: V_{CC} – 45 V
- Timing number a; digit number b; segment number c
- Ratio of T_{off} time corresponding T_{disp} time: 1/16
- Turn ON segment number during repeat cycle: d
- All segment number during repeat cycle: c (= a X c)
- Total number of built-in resistor: for digit; f, for segment; g
- Digit pin current value h (mA)
- Segment pin current value i (mA)

- (1) Digit pin power dissipation
 $\{h \times b \times (1 - T_{\text{off}}/T_{\text{disp}}) \times \text{voltage}\} / a$
- (2) Segment pin power dissipation
 $\{i \times d \times (1 - T_{\text{off}}/T_{\text{disp}}) \times \text{voltage}\} / a$
- (3) Pull-down resistor power dissipation (digit)
 $\{\text{power dissipation per 1 digit} \times (b \times f / b) \times (1 - T_{\text{off}}/T_{\text{disp}})\} / a$
- (4) Pull-down resistor power dissipation (segment)
 $\{\text{power dissipation per 1 segment} \times (d \times g / c) \times (1 - T_{\text{off}}/T_{\text{disp}})\} / a$
- (5) Internal circuit power dissipation (CPU, ROM, RAM etc.) = 75 mW

$$(1) + (2) + (3) + (4) + (5) = \underline{\text{X mW}}$$

Power Dissipation Calculating example 1

● Fixed number depending on microcomputer's standard

- V_{OH} output fall voltage of high-breakdown port
2 V (max.); | Current value | = at 18 mA
- Resistor value 43 V / 900 μA = 48 kΩ (min.)
- Power dissipation of internal circuit (CPU, ROM, RAM etc.) = 5 V X 15 mA = 75 mW

● Fixed number depending on use condition

- Apply voltage to V_{EE} pin: V_{CC} – 45 V
- Timing number 17; digit number 16; segment number 20
- Ratio of T_{off} time corresponding T_{disp} time: 1/16
- Turn ON segment number during repeat cycle: 31
- All segment number during repeat cycle: 340 (= 17 X 20)
- Total number of built-in resistor: for digit; 16, for segment; 20
- Digit pin current value: 18 (mA)
- Segment pin current value: 3 (mA)

- (1) Digit pin power dissipation
 $\{18 \times 16 \times (1 - 1/16) \times 2\} / 17 = 31.77 \text{ mW}$
- (2) Segment pin power dissipation
 $\{3 \times 31 \times (1 - 1/16) \times 2\} / 17 = 10.26 \text{ mW}$
- (3) Pull-down resistor power dissipation (digit)
 $(45 - 2)^2 / 48 \times (16 \times 16/16) \times (1 - 1/16) / 17 = 33.99 \text{ mW}$
- (4) Pull-down resistor power dissipation (segment)
 $(45 - 2)^2 / 48 \times (31 \times 20/20) \times (1 - 1/16) / 17 = 65.86 \text{ mW}$
- (5) Internal circuit power dissipation (CPU, ROM, RAM etc.) = 75 mW

$$(1) + (2) + (3) + (4) + (5) = \underline{217 \text{ mW}}$$

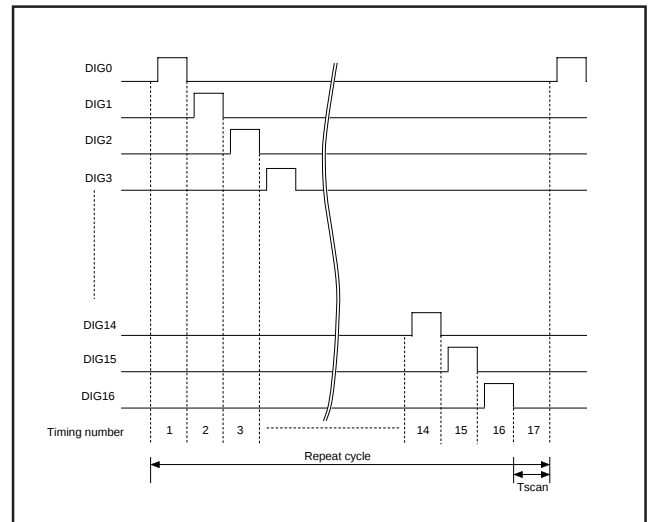


Fig. 76 Digit timing waveform (1)

HARDWARE

MASK OPTION OF PULL-DOWN RESISTOR

Power Dissipation Calculating example 2 (when 2 or more digit is turned ON at same time)

● Fixed number depending on microcomputer's standard

- V_{OH} output fall voltage of high-breakdown port
2 V (max.); | Current value | = at 18 mA
- Resistor value $43 \text{ V} / 900 \mu\text{A} = 48 \text{ k}\Omega$ (min.)
- Power dissipation of internal circuit (CPU, ROM, RAM etc.) = $5 \text{ V} \times 15 \text{ mA} = 75 \text{ mW}$

● Fixed number depending on use condition

- Apply voltage to V_{EE} pin: V_{CC} – 45 V
- Timing number 11; digit number 12; segment number 24
- Ratio of T_{off} time corresponding T_{disp} time: 1/16
- Turn ON segment number during repeat cycle: 114
- All segment number during repeat cycle: 264 (= 11 × 24)
- Total number of built-in resistor: for digit; 10, for segment; 22
- Digit pin current value: 18 (mA)
- Segment pin current value: 3 (mA)

(1) Digit pin power dissipation

$$\{18 \times 12 \times (1 - 1/16) \times 2\} / 11 = 36.82 \text{ mW}$$

(2) Segment pin power dissipation

$$\{3 \times 114 \times (1 - 1/16) \times 2\} / 11 = 58.30 \text{ mW}$$

(3) Pull-down resistor power dissipation (digit)

$$(45 - 2)^2 / 48 \times (12 \times 10/12) \times (1 - 1/16) / 11 = 32.84 \text{ mW}$$

(4) Pull-down resistor power dissipation (segment)

$$(45 - 2)^2 / 48 \times (114 \times 22/24) \times (1 - 1/16) / 11 = 343.08 \text{ mW}$$

(5) Internal circuit power dissipation (CPU, ROM, RAM etc.) = 75 mW

$$(1) + (2) + (3) + (4) + (5) = \underline{547 \text{ mW}}$$

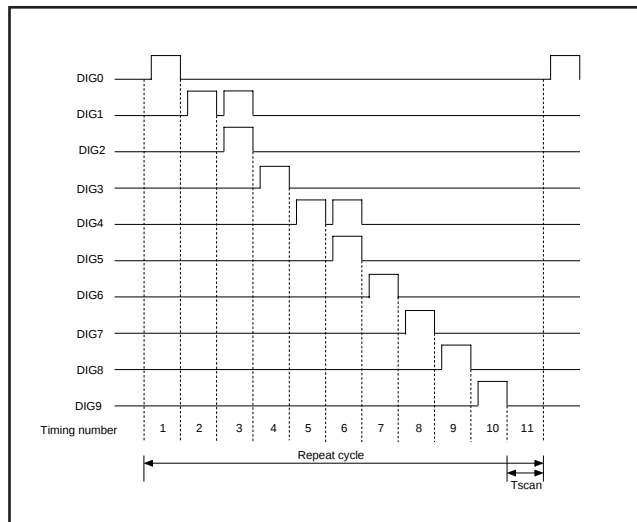


Fig. 77 Digit timing waveform (2)

FUNCTIONAL DESCRIPTION SUPPLEMENT

Interrupt

38B5 group permits interrupts on the basis of 21 sources.

It is vector interrupts with a fixed priority system. Accordingly, when two or more interrupt requests occur during the same sampling, the

higher-priority interrupt is accepted first. This priority is determined by hardware, but various priority processing can be performed by software, using an interrupt enable bit and an interrupt disable flag.

For interrupt sources, vector addresses and interrupt priority, refer to Table 13.

Table 13 Interrupt sources, vector addresses and interrupt priority

Interrupt source	Priority	Vector Addresses (Note 1)		Remarks
		High	Low	
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	Non-maskable
INT ₀	2	FFFB ₁₆	FFFA ₁₆	External interrupt (active edge selectable)
INT ₁	3	FFF9 ₁₆	FFF8 ₁₆	External interrupt (active edge selectable)
INT ₂	4	FFF7 ₁₆	FFF6 ₁₆	External interrupt (active edge selectable)
Remote control/counter overflow				Valid when interrupt interval determination is operating
Serial I/O ₁	5	FFF5 ₁₆	FFF4 ₁₆	Valid when serial I/O ₁ ordinary mode is selected
Serial I/O ₁ automatic transfer				Valid when serial I/O ₁ automatic transfer mode is selected
Timer X	6	FFF3 ₁₆	FFF2 ₁₆	
Timer 1	7	FFF1 ₁₆	FFF0 ₁₆	
Timer 2	8	FFEF ₁₆	FFEE ₁₆	STP release timer underflow
Timer 3	9	FFED ₁₆	FFEC ₁₆	
Timer 4	10	FFEB ₁₆	FFEA ₁₆	(Note 3)
Timer 5	11	FFE9 ₁₆	FFE8 ₁₆	
Timer 6	12	FFE7 ₁₆	FFE6 ₁₆	
Serial I/O ₂ receive	13	FFE5 ₁₆	FFE4 ₁₆	
INT ₃	14	FFE3 ₁₆	FFE2 ₁₆	External interrupt (active edge selectable) (Note 4)
Serial I/O ₂ transmit				
INT ₄	15	FFE1 ₁₆	FFE0 ₁₆	External interrupt (active edge selectable)
A-D conversion				Valid when INT ₄ interrupt is selected Valid when A-D conversion is selected
FLD blanking	16	FFDF ₁₆	FFDE ₁₆	Valid when FLD blanking interrupt is selected
FLD digit				Valid when FLD digit interrupt is selected
BRK instruction	17	FFDD ₁₆	FFDC ₁₆	Non-maskable software interrupt

Notes 1 : Vector addresses contain interrupt jump destination addresses.

2 : Reset function in the same way as an interrupt with the highest priority.

3 : In the mask option type P, timer 4 interrupt whose count source is CNTR₁ input cannot be used.

4 : In the mask option type P, INT₃ interrupt cannot be used.

HARDWARE

FUNCTIONAL DESCRIPTION SUPPLEMENT

Timing After Interrupt

The interrupt processing routine begins with the machine cycle following the completion of the instruction that is currently in execution. Figure 78 shows a timing chart after an interrupt occurs, and Figure 79 shows the time up to execution of the interrupt processing routine.

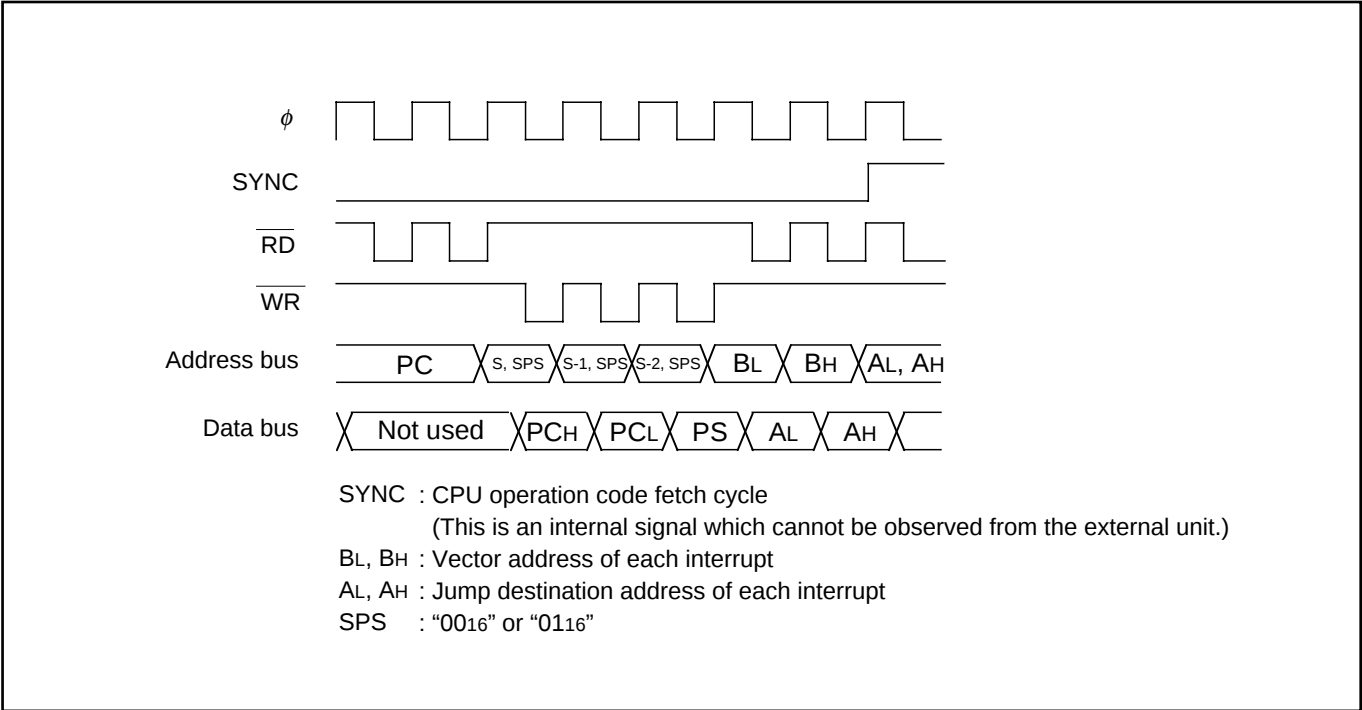


Fig. 78 Timing chart after interrupt occurs

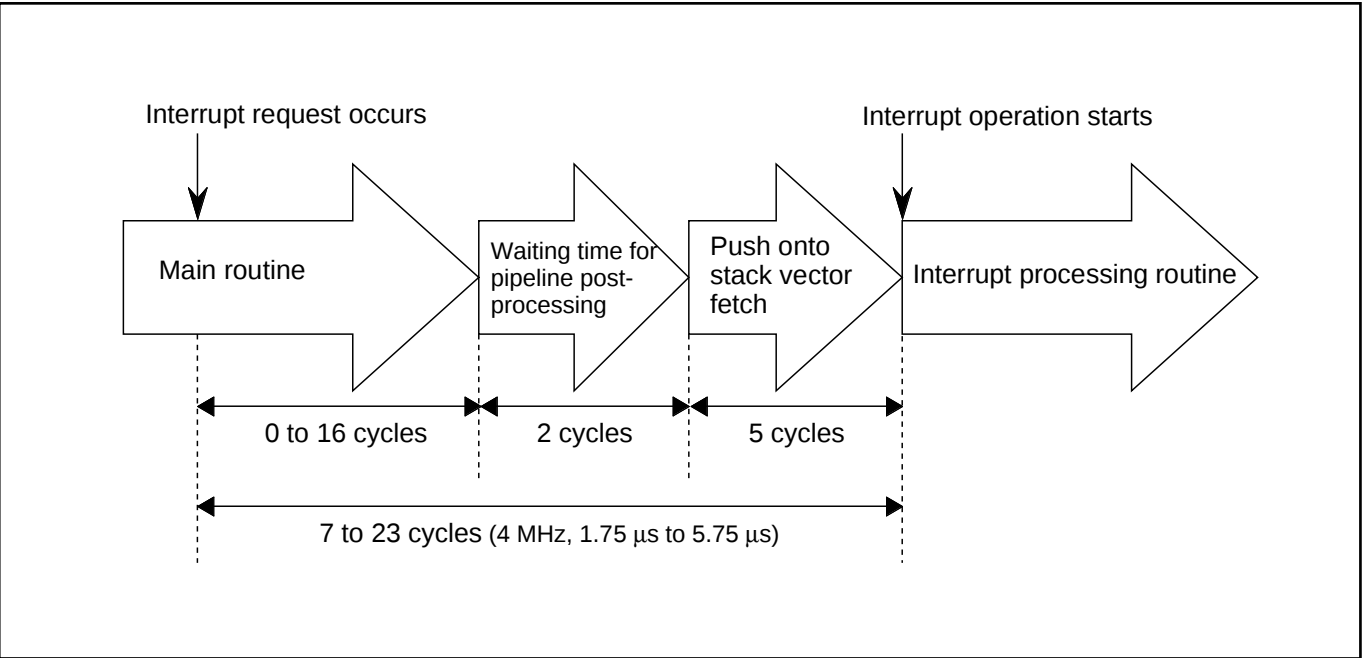


Fig. 79 Time up to execution of interrupt processing routine

A-D Converter

A-D conversion is started by setting AD conversion completion bit to "0." During A-D conversion, internal operations are performed as follows.

1. After the start of A-D conversion, A-D conversion register goes to "0016."
2. The highest-order bit of A-D conversion register is set to "1," and the comparison voltage V_{ref} is input to the comparator. Then, V_{ref} is compared with analog input voltage V_{IN} .
3. As a result of comparison, when $V_{ref} < V_{IN}$, the highest-order bit of A-D conversion register becomes "1." When $V_{ref} > V_{IN}$, the highest-order bit becomes "0."

By repeating the above operations up to the lowest-order bit of the A-D conversion register, an analog value converts into a digital value. A-D conversion completes at 61 clock cycles (15.25 μ s at $f(X_{IN}) = 8$ MHz) after it is started, and the result of the conversion is stored into the A-D conversion register.

Concurrently with the completion of A-D conversion, A-D conversion interrupt request occurs, so that the AD conversion interrupt request bit is set to "1."

Table 14 Relative formula for a reference voltage V_{REF} of A-D converter and V_{ref}

When $n = 0$	$V_{ref} = 0$
When $n = 1$ to 1023	$V_{ref} = \frac{V_{REF}}{1024} \times n$

n: Value of A-D converter (decimal numeral)

Table 15 Change of A-D conversion register during A-D conversion

	Change of A-D conversion register	Value of comparison voltage (V_{ref})
At start of conversion	0 0 0 0 0 0 0 0 0 0 0 0	0
First comparison	1 0 0 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2}$
Second comparison	*1 1 0 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4}$
Third comparison	*1 *2 1 0 0 0 0 0 0 0 0 0	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \frac{V_{REF}}{8}$
≈		
After completion of tenth comparison	A result of A-D conversion *1 *2 *3 *4 *5 *6 *7 *8 *9 *10	$\frac{V_{REF}}{2} \pm \frac{V_{REF}}{4} \pm \dots \pm \frac{V_{REF}}{1024}$

*1~*10: A result of the first comparison to the tenth comparison

HARDWARE

FUNCTIONAL DESCRIPTION SUPPLEMENT

Figures 80 shows the A-D conversion equivalent circuit, and Figure 81 shows the A-D conversion timing chart.

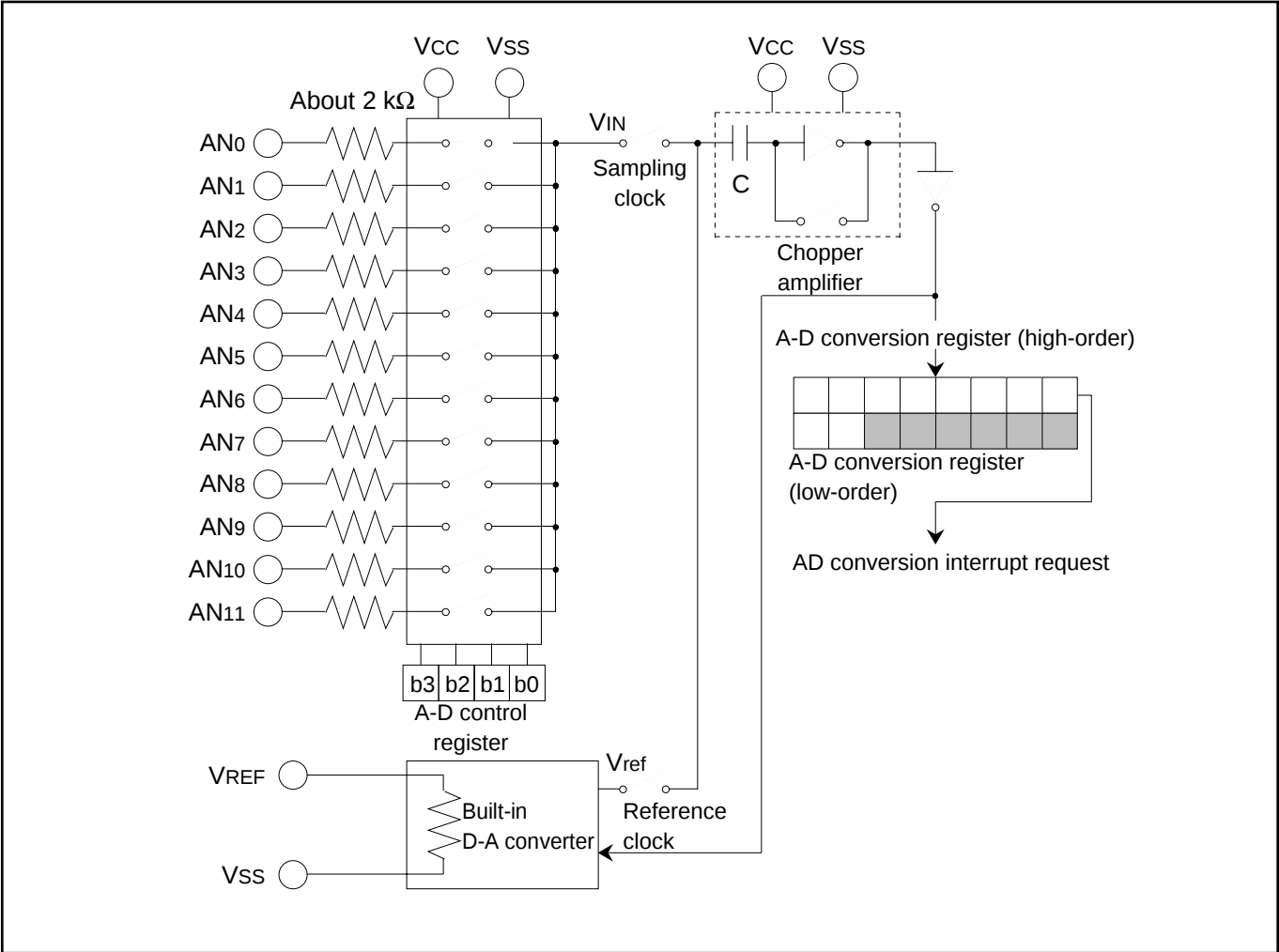


Fig. 80 A-D conversion equivalent circuit

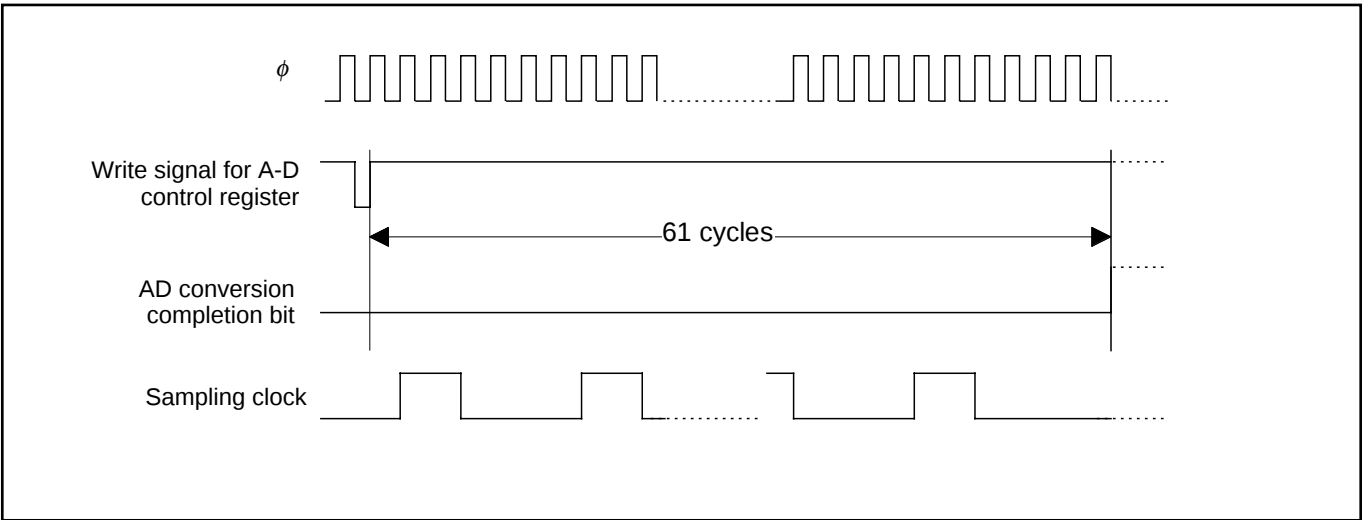


Fig. 81 A-D conversion timing chart

CHAPTER 2

APPLICATION

- 2.1 I/O port
- 2.2 Timer
- 2.3 Serial I/O
- 2.4 FLD controller
- 2.5 A-D converter
- 2.6 PWM
- 2.7 Interrupt interval determination
function
- 2.8 Watchdog timer
- 2.9 Buzzer output circuit
- 2.10 Reset circuit
- 2.11 Clock generating circuit

APPLICATION

2.1 I/O port

2.1 I/O port

This paragraph describes the setting method of I/O port relevant registers, notes etc.

2.1.1 Memory assignment

Address

0000 ₁₆	Port P0 (P0)
0001 ₁₆	Port P0 direction register (P0D)
0002 ₁₆	Port P1 (P1)
0003 ₁₆	
0004 ₁₆	Port P2 (P2)
0005 ₁₆	Port P2 direction register (P2D)
0006 ₁₆	Port P3 (P3)
0007 ₁₆	
0008 ₁₆	Port P4 (P4)
0009 ₁₆	Port P4 direction register (P4D)
000A ₁₆	Port P5 (P5)
000B ₁₆	Port P5 direction register (P5D)
000C ₁₆	Port P6 (P6)
000D ₁₆	Port P6 direction register (P6D)
000E ₁₆	Port P7 (P7)
000F ₁₆	Port P7 direction register (P7D)
0010 ₁₆	Port P8 (P8)
0011 ₁₆	Port P8 direction register (P8D)
0012 ₁₆	Port P9 (P9)
0013 ₁₆	Port P9 direction register (P9D)
≈	
0EF0 ₁₆	Pull-up control register 1 (PULL1)
0EF1 ₁₆	Pull-up control register 2 (PULL2)

Fig. 2.1.1 Memory assignment of I/O port relevant registers

2.1.2 Relevant registers

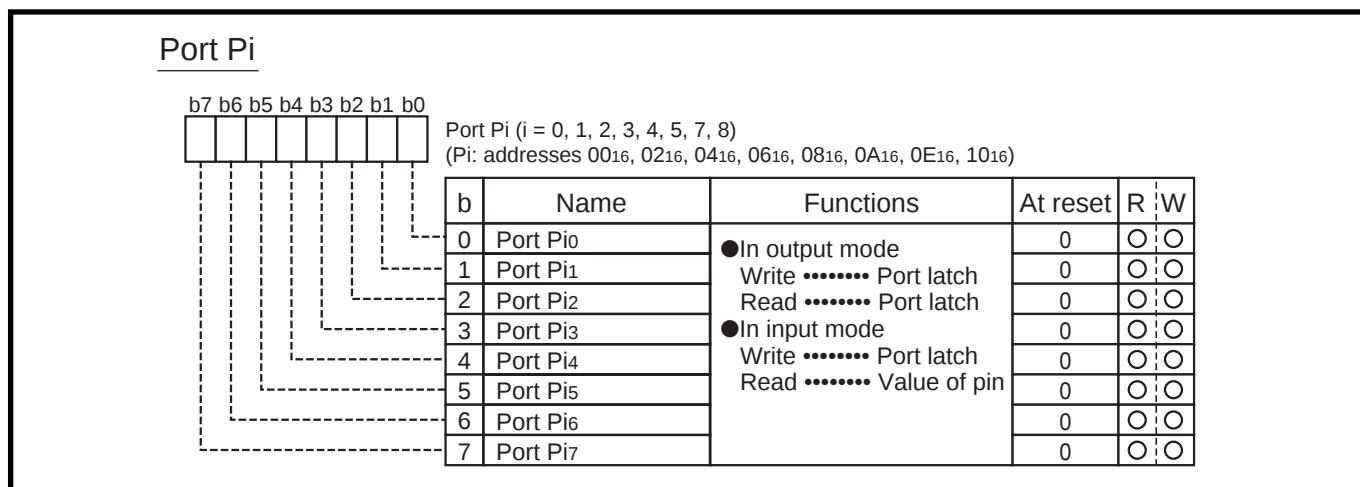


Fig. 2.1.2 Structure of port Pi (i = 0, 1, 2, 3, 4, 5, 7, 8)

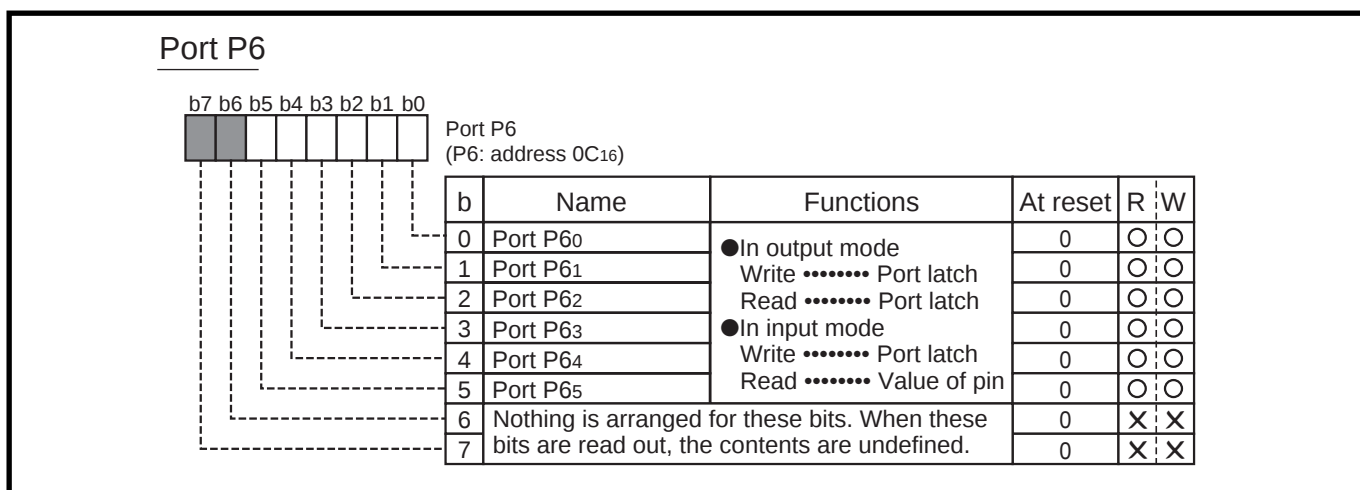


Fig. 2.1.3 Structure of port P6

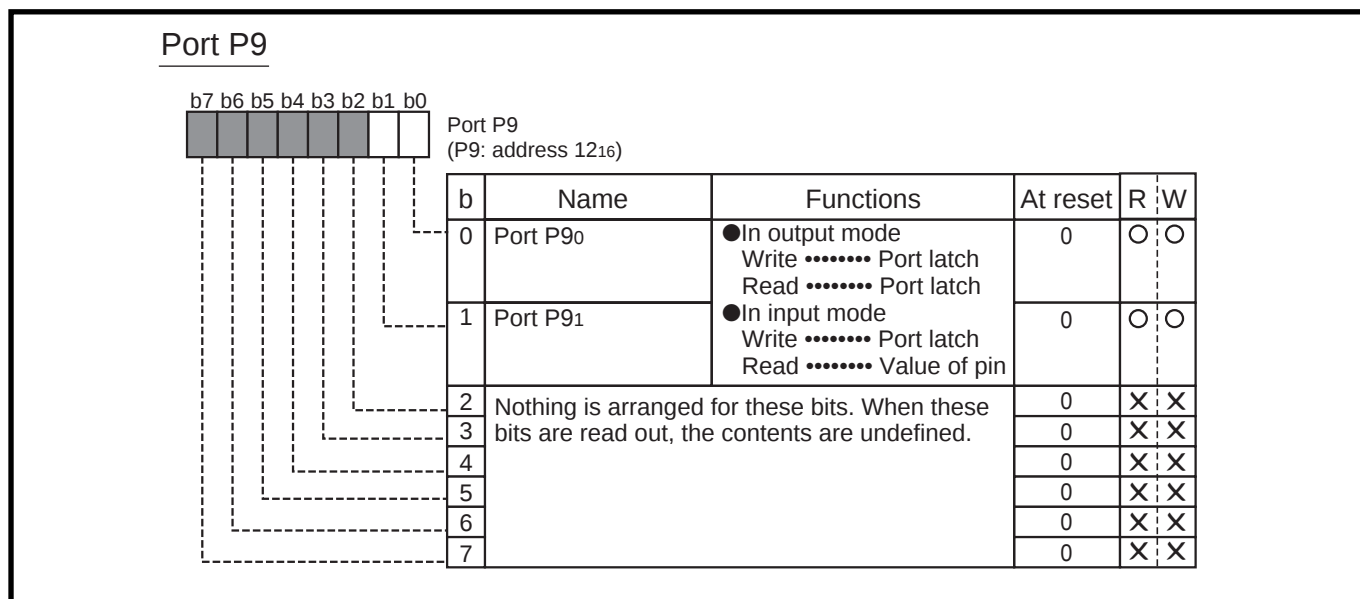


Fig. 2.1.4 Structure of port P9

APPLICATION

2.1 I/O port

Port Pi direction register

b7	b6	b5	b4	b3	b2	b1	b0				
								Port Pi direction register (i = 0, 2, 4, 5, 7, 8) (PiD: addresses 01 ₁₆ , 05 ₁₆ , 09 ₁₆ , 0B ₁₆ , 0F ₁₆ , 11 ₁₆)			

Note: Bit 7 of the port P4 direction register (address 09₁₆) does not have direction register function because P4₇ is input port. When writing to bit 7 of the port P4 direction register, write "0" to the bit.

Fig. 2.1.5 Structure of port Pi (i = 0, 2, 4, 5, 7, 8) direction register

Port P6 direction register

b7	b6	b5	b4	b3	b2	b1	b0				
								Port P6 direction register (P6D: address 0D ₁₆)			
	</										

Fig. 2.1.6 Structure of port P6 direction register

Port P9 direction register

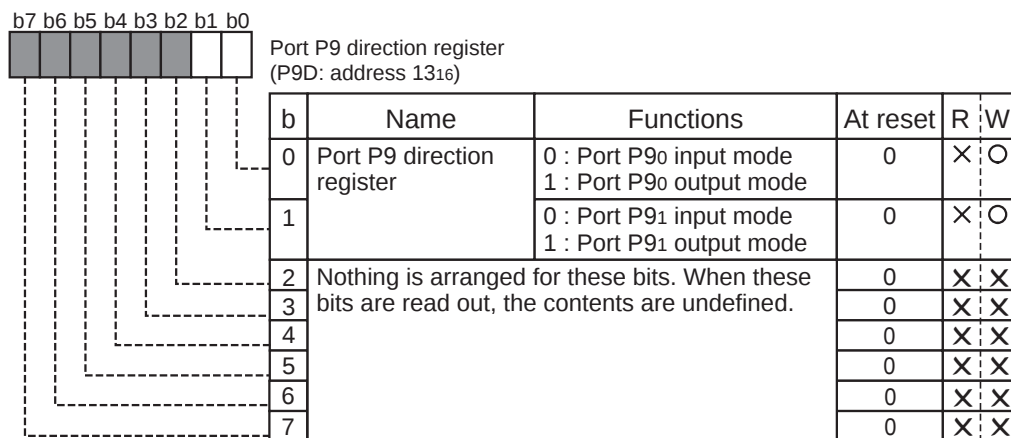
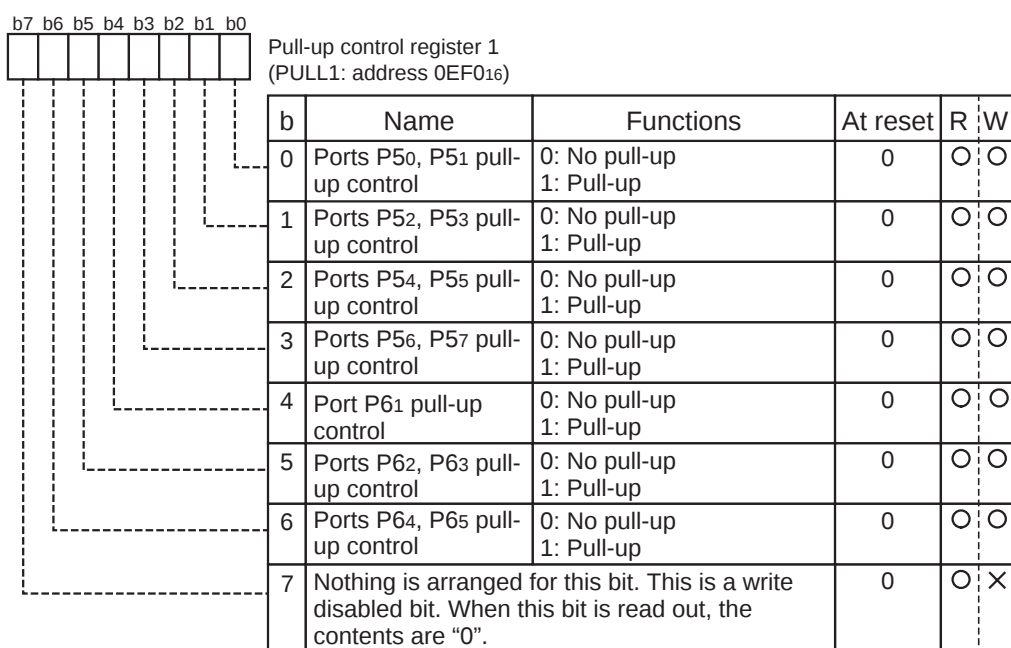


Fig. 2.1.7 Structure of port P9 direction register

Pull-up control register 1



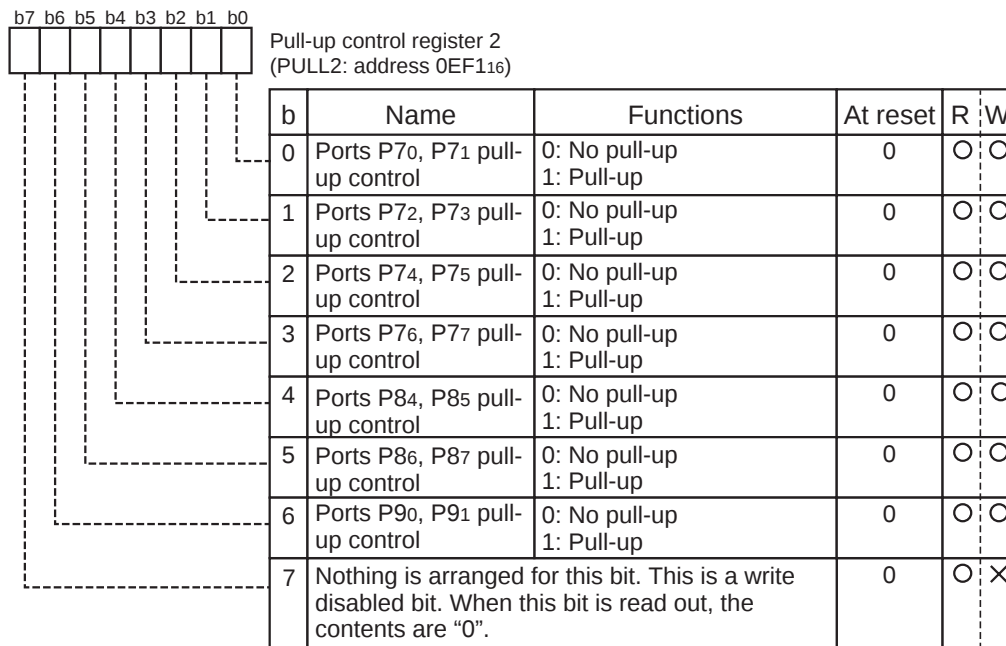
Note: The pin set to output port is cut off from pull-up control.

Fig. 2.1.8 Structure of pull-up control register 1

APPLICATION

2.1 I/O port

Pull-up control register 2



Note: The pin set to output port is cut off from pull-up control.

Fig. 2.1.9 Structure of pull-up control register 2

2.1.3 Terminate unused pins

Table 2.1.1 Termination of unused pins

Pins	Termination
P1, P3	Open at "H" output state.
P5, P6 ₁ –P6 ₅ , P7, P8 ₄ –P8 ₇ , P9	- Set to the input mode and connect each to V_{CC} or V_{SS} through a resistor of 1 kΩ to 10 kΩ. - Set to the output mode and open at "L" or "H" output state.
P4 ₀ –P4 ₆ , P6 ₀	- Set to the input mode and connect each to V_{CC} or V_{SS} through a resistor of 1 kΩ to 10 kΩ. - Set to the output mode and open at "L" output state.
P0, P2, P8 ₀ –P8 ₃	- Set to the input mode and connect each to V_{CC} or V_{SS} through a resistor of 1 kΩ to 10 kΩ. - Set to the output mode and open at "H" output state.
P4 ₇	Disable INT ₂ interrupt and connect to V _{CC} or V _{SS} through a resistor of 1 KΩ to 10 kΩ.
V _{REF}	Open
X _{OUT}	Open (only when using external clock)
AV _{SS} , V _{EE}	Connect to V _{SS} (GND).

2.1.4 Notes on use

(1) Notes in standby state

In standby state*¹ for low-power dissipation, do not make input levels of an input port and an I/O port “undefined”, especially for I/O ports of the P-channel open-drain and the N-channel open-drain.

Pull-up (connect the port to Vcc) or pull-down (connect the port to Vss) these ports through a resistor.

When determining a resistance value, note the following points:

- External circuit
- Variation of output levels during the ordinary operation

When using built-in pull-up resistor, note on varied current values:

- When setting as an input port : Fix its input level
- When setting as an output port : Prevent current from flowing out to external

● Reason

Even when setting as an output port with its direction register, in the following state :

- P-channel.....when the content of the port latch is “0”
- N-channel.....when the content of the port latch is “1”

the transistor becomes the OFF state, which causes the ports to be the high-impedance state.

Note that the level becomes “undefined” depending on external circuits.

Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of a input port and an I/O port are “undefined”. This may cause power source current.

*1 standby state: stop mode by executing **STP** instruction
wait mode by executing **WIT** instruction

(2) N-channel open-drain port

P4₀–P4₂, P4₅, P4₆, P6₀ of N-channel open-drain output ports have the built-in hysteresis circuit for input. In standby state for low-power dissipation, do not make these pins floating state.

● Reason

When power sources for pull-up of these pins are cut off in standby state, these ports become floating. Accordingly, a current may flow from Vcc to Vss through the built-in hysteresis circuit.

APPLICATION

2.1 I/O port

(3) Modifying port latch of I/O port with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction*2, the value of the unspecified bit may be changed.

● Reason

The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit. Accordingly, when these instructions are executed on a bit of the port latch of an I/O port, the following is executed to all bits of the port latch.

- As for bit which is set for input port:

The pin state is read in the CPU, and is written to this bit after bit managing.

- As for bit which is set for output port:

The bit value is read in the CPU, and is written to this bit after bit managing.

Note the following:

- Even when a port which is set as an output port is changed for an input port, its port latch holds the output data.

- As for a bit of which is set for an input port, its value may be changed even when not specified with a bit managing instruction in case where the pin state differs from its port latch contents.

*2 Bit managing instructions: **SEB** and **CLB** instructions

(4) Pull-up control

When each port which has built-in pull-up resistor (P5, P6₁–P6₅, P7, P8₄–P8₇, P9) is set to output port, pull-up control of corresponding port become invalid. (Pull-up cannot be set.)

● Reason

Pull-up control is valid only when each direction register is set to the input mode.

2.1.5 Termination of unused pins

(1) Terminate unused pins

① Output ports : Open

② Input ports :

Connect each pin to Vcc or Vss through each resistor of 1 kΩ to 10 kΩ.

As for pins whose potential affects to operation modes such as pin INT or others, select the Vcc pin or the Vss pin according to their operation mode.

③ I/O ports :

- Set the I/O ports for the input mode and connect them to Vcc or Vss through each resistor of 1 kΩ to 10 kΩ.

Ports that permit the selecting of a built-in pull-up resistor can also use this resistor. Set the I/O ports for the output mode and open them at “L” or “H”.

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.

- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

(2) Termination remarks

① Input ports and I/O ports :

Do not open in the input mode.

● **Reason**

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination ② and ③ shown on the above.

② I/O ports :

When setting for the input mode, do not connect to Vcc or Vss directly.

● **Reason**

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between a port and Vcc (or Vss).

③ I/O ports :

When setting for the input mode, do not connect multiple ports in a lump to Vcc or Vss through a resistor.

● **Reason**

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

- At the termination of unused pins, perform wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

APPLICATION

2.2 Timer

2.2 Timer

This paragraph explains the registers setting method and the notes relevant to the timers.

2.2.1 Memory map

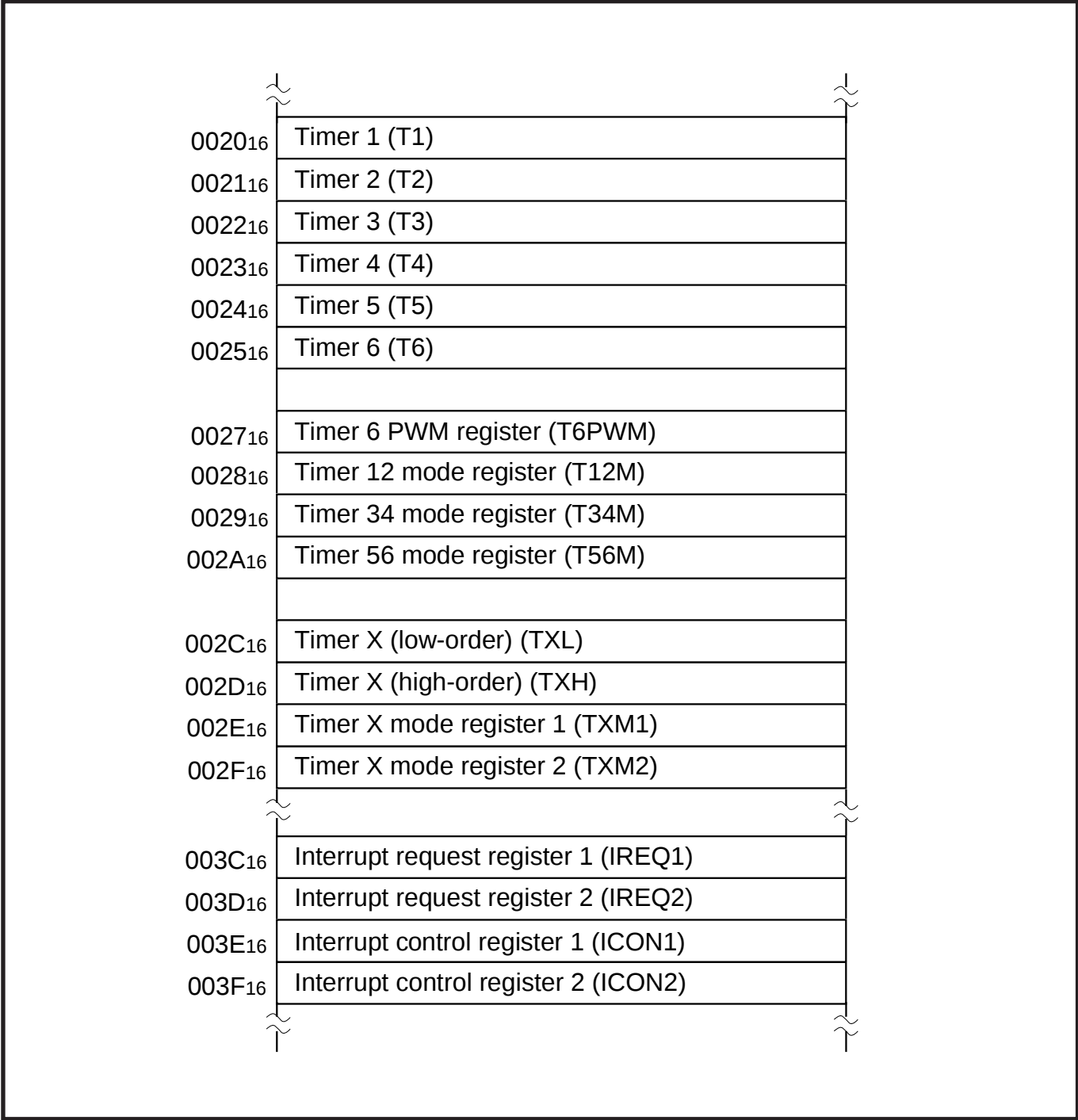


Fig. 2.2.1 Memory map of registers relevant to timers

2.2.2 Relevant registers

(1) 8-bit timer

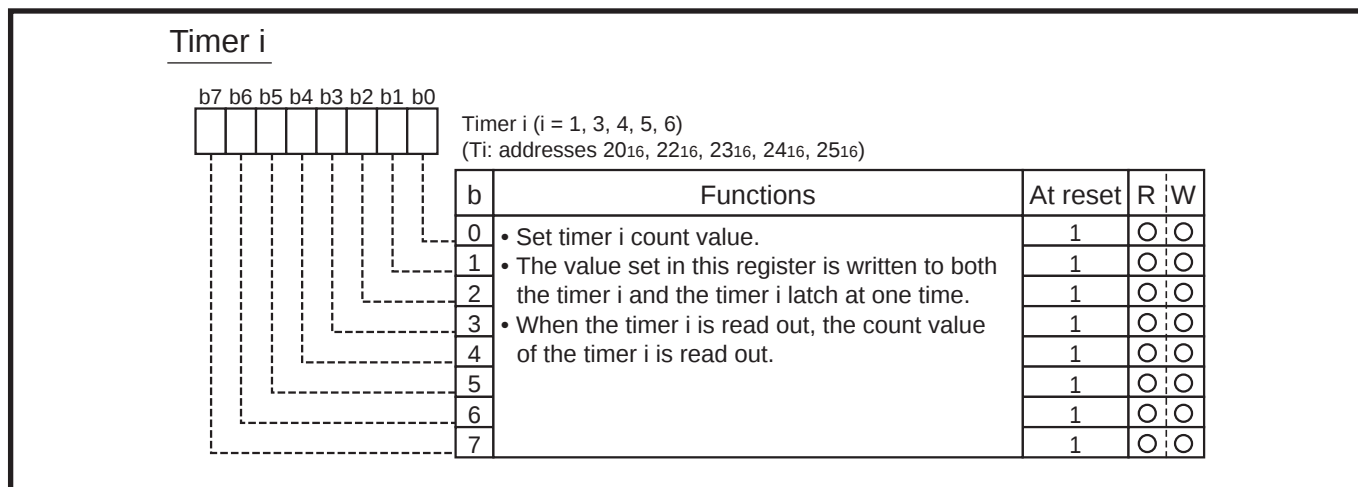


Fig. 2.2.2 Structure of Timer i (i=1, 3, 4, 5, 6)

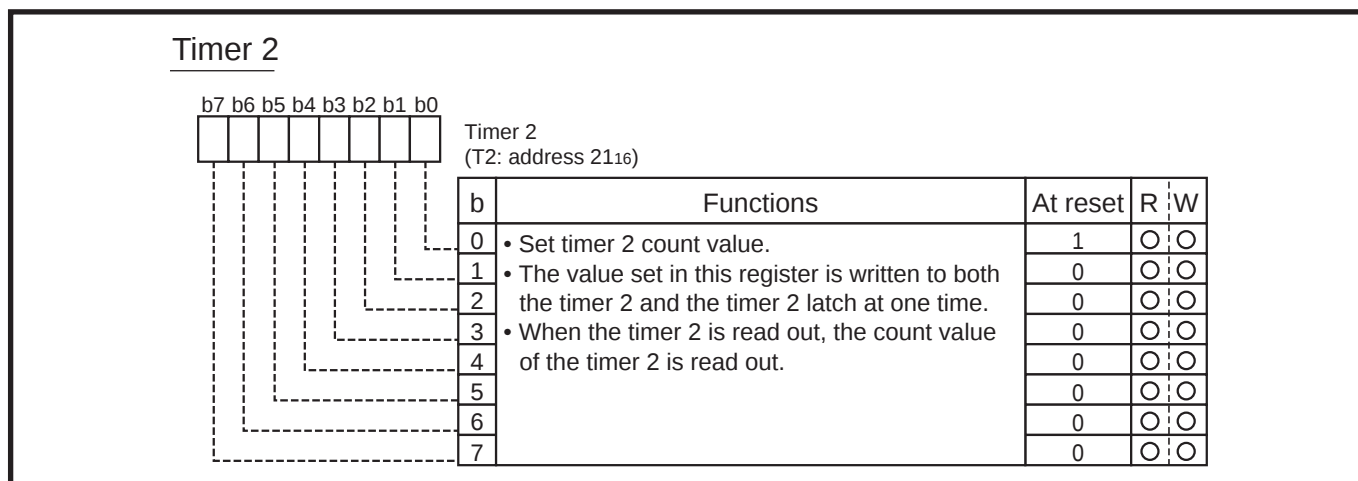


Fig. 2.2.3 Structure of Timer 2

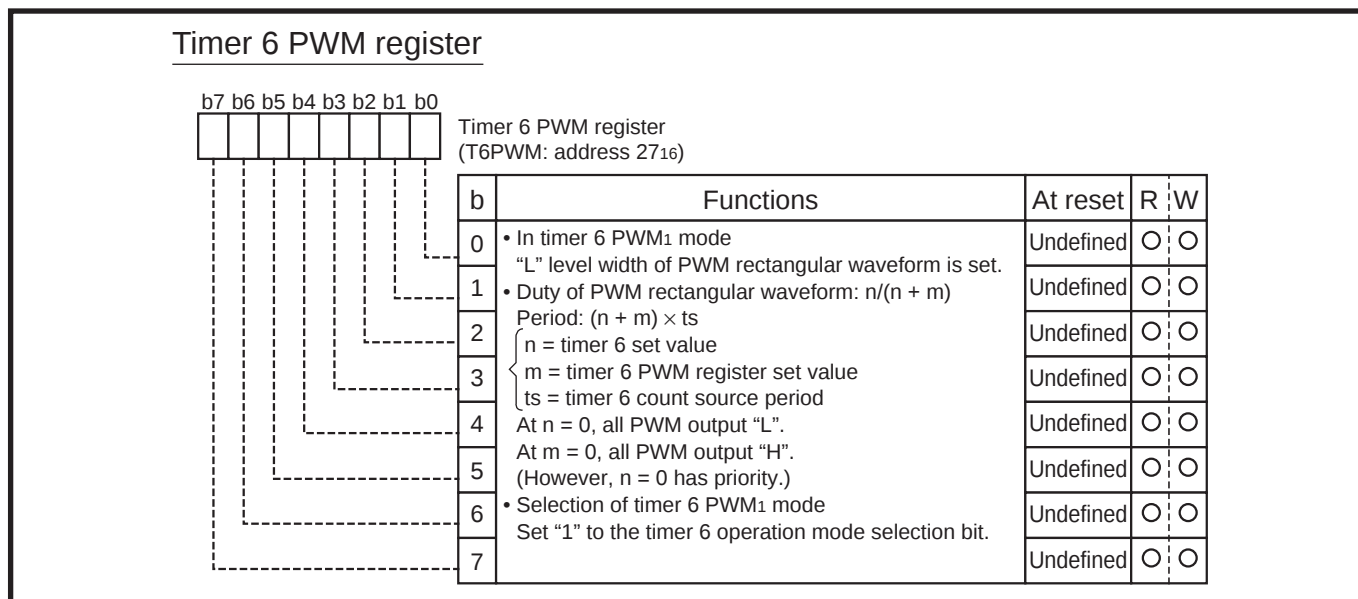


Fig. 2.2.4 Structure of Timer 6 PWM register

APPLICATION

2.2 Timer

Timer 12 mode register

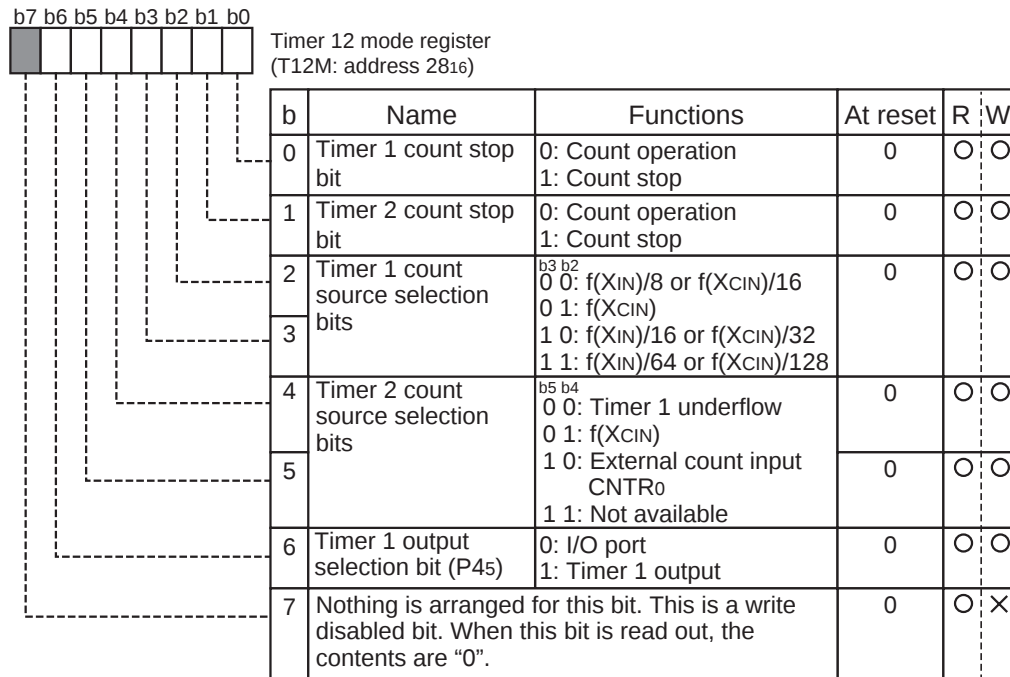
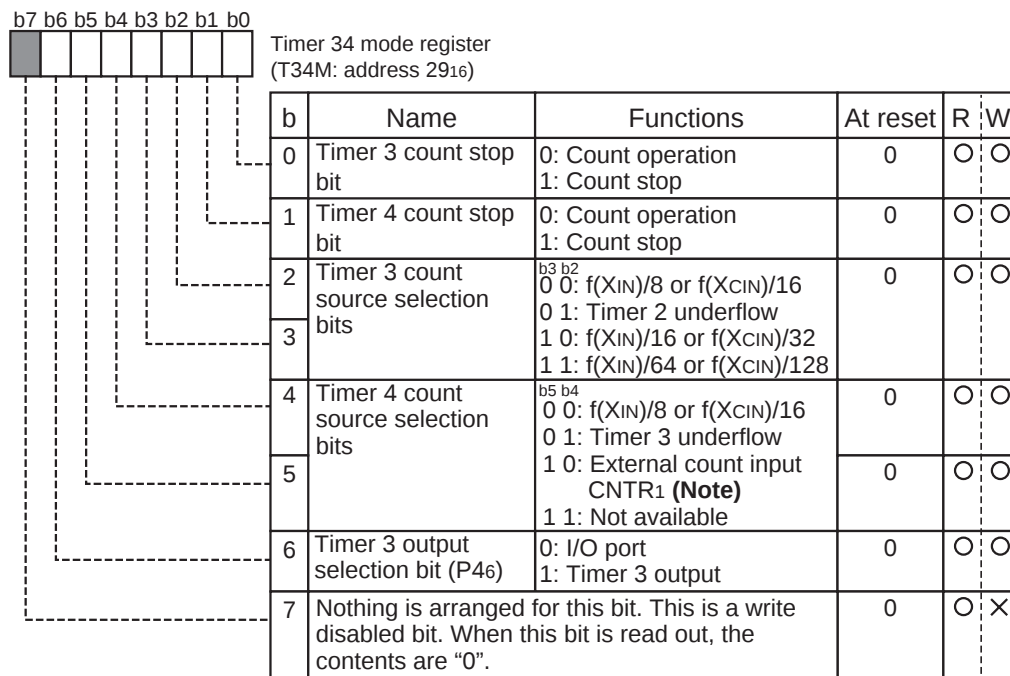


Fig. 2.2.5 Structure of Timer 12 mode register

Timer 34 mode register



Note: In the mask option type P, CNTR₁ function cannot be used.

Fig. 2.2.6 Structure of Timer 34 mode register

Timer 56 mode register

b7

b6

b5

b4

b3

b2

b1

b0

Timer 56 mode register

(T56M: address 2A16)

b	Name	Functions	At reset	R	W
0	Timer 5 count stop bit	0: Count operation 1: Count stop	0	○	○
1	Timer 6 count stop bit	0: Count operation 1: Count stop	0	○	○
2	Timer 5 count source selection bit	0: f(XIN)/8 or f(XCIN)/16 1: Timer 4 underflow	0	○	○
3	Timer 6 operation mode selection bit	0: Timer mode 1: PWM mode	0	○	○
4	Timer 6 count source selection bits	b5 b4 0 0: f(XIN)/8 or f(XCIN)/16 0 1: Timer 5 underflow 1 0: Timer 4 underflow 1 1: Not available	0	○	○
5			0	○	○
6	Timer 6 (PWM) output selection bit (P44)	0: I/O port 1: Timer 6 output	0	○	○
7	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	×

Fig. 2.2.7 Structure of Timer 56 mode register

(2) 16-bit timer

Timer X (low-order, high-order)

b7	b6	b5	b4	b3	b2	b1	b0	
								Timer X (low-order, high-order) (TXL, TXH: addresses 2C16, 2D16)

Notes 1: When reading and writing, perform them to both the high-order and low-order bytes.

2: Read both registers in order of TXH and TXL following.

3: Write both registers in order of TXL and TXH following.

4: Do not read both registers during a write, and do not write to both registers during a read.

Fig. 2.2.8 Structure of Timer X (low-order, high-order)

APPLICATION

2.2 Timer

Timer X mode register 1

b7

b6

b5

b4

b3

b2

b1

b0

</

Fig. 2.2.9 Structure of Timer X mode register 1

Timer X mode register 2

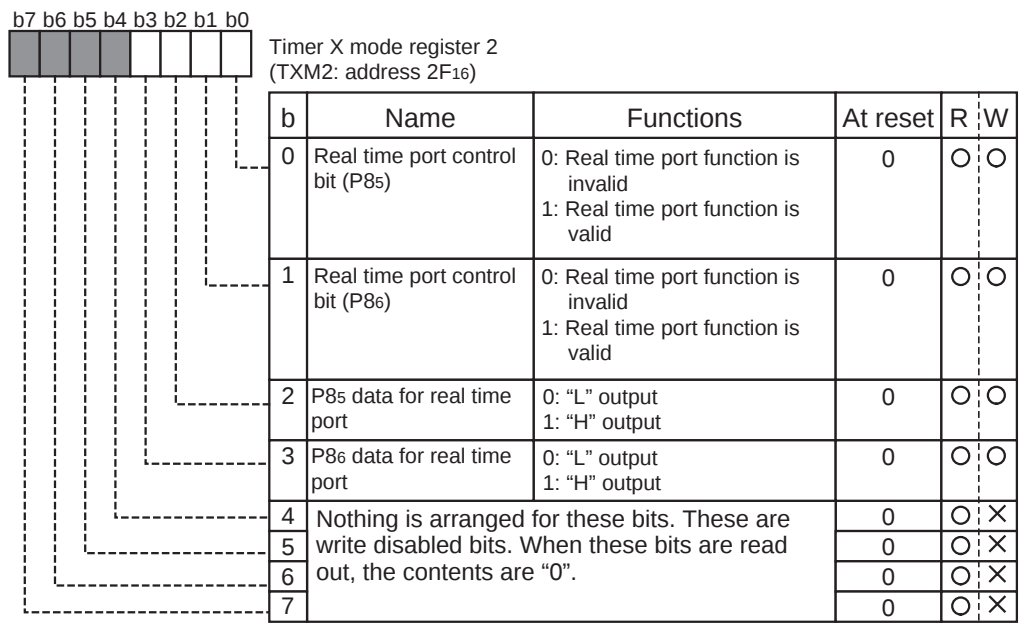


Fig. 2.2.10 Structure of Timer X mode register 2

APPLICATION

2.2 Timer

(3) 8-bit timer, 16-bit timer

Interrupt request register 1

b7	b6	b5	b4	b3	b2	b1	b0	Interrupt request register 1 (IREQ1 : address 3C16)					
								b	Name	Functions	At reset	R	W
								0	INT0 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								1	INT1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								2	INT2 interrupt request bit Remote controller /counter overflow interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								3	Serial I/O1 interrupt request bit Serial I/O automatic transfer interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								4	Timer X interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								5	Timer 1 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								6	Timer 2 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								7	Timer 3 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*

※: "0" can be set by software, but "1" cannot be set.

Fig. 2.2.11 Structure of Interrupt request register 1

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0								Interrupt request register 2 (IREQ2 : address 3D16)					
								b	Name	Functions	At reset	R	W
								0	Timer 4 interrupt request bit (Note)	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								1	Timer 5 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								2	Timer 6 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								3	Serial I/O2 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								4	INT3/Serial I/O2 transmit interrupt request bit (Note)	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								5	INT4 interrupt request bit A-D converter interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								6	FLD blanking interrupt request bit FLD digit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
								7	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	×

*: "0" can be set by software, but "1" cannot be set.

Note: In the mask option type P, if timer 4 interrupt whose count source is CNTR1 input and INT3 interrupt are selected, these bits do not become "1".

Fig. 2.2.12 Structure of Interrupt request register 2

APPLICATION

2.2 Timer

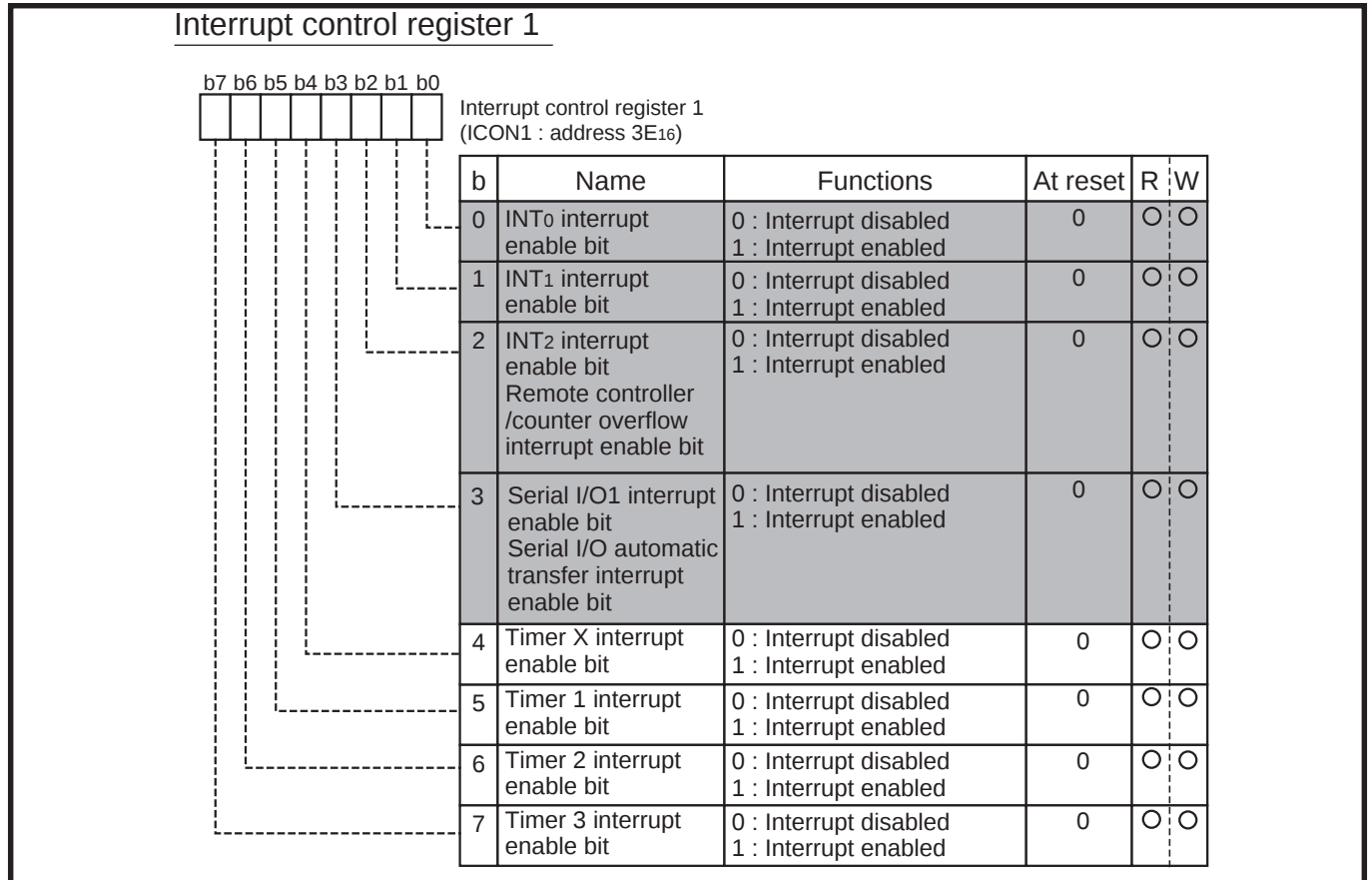


Fig. 2.2.13 Structure of Interrupt control register 1

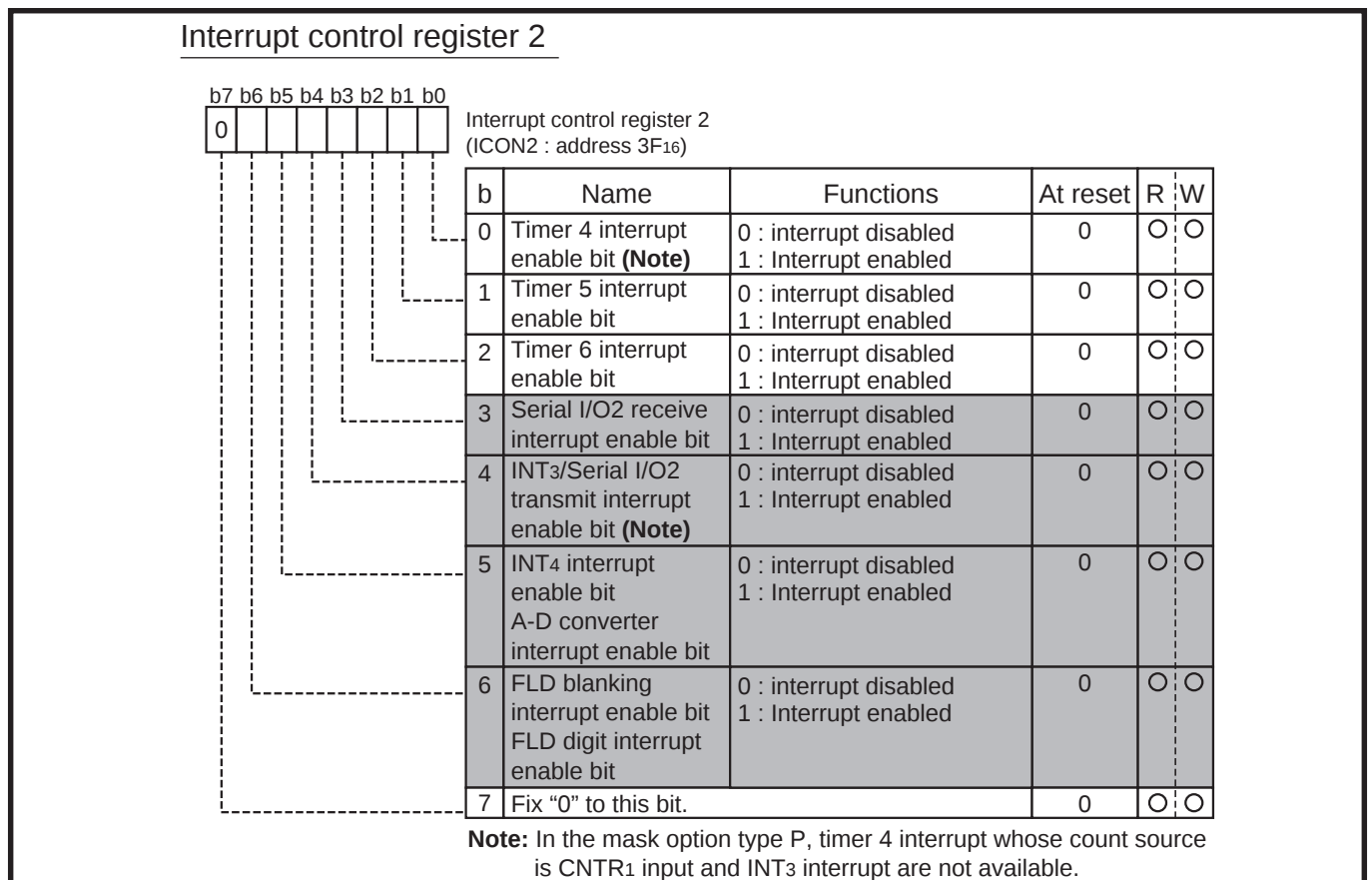


Fig. 2.2.14 Structure of Interrupt control register 2

2.2.3 Timer application examples

(1) Basic functions and uses

[Function 1] Control of event interval (Timer 1 to Timer 6, Timer X: timer mode)

When a certain time, by setting a count value to each timer, has passed, the timer interrupt request occurs.

<Use>

- Generating of an output signal timing
- Generating of a wait time

[Function 2] Control of cyclic operation (Timer 1 to Timer 6, Timer X: timer mode)

The value of the timer latch is automatically written to the corresponding timer each time the timer underflows, and each timer interrupt request occurs in cycles.

<Use>

- Generating of cyclic interrupts
- Clock function (measurement of 1 s); see "(2) Timer application example 1"
- Control of a main routine cycle

[Function 3] Output of rectangular waveform

(Timer 1, Timer 3, Timer 6, Timer X: pulse output mode)

The output level of the T_{1OUT} pin, T_{3OUT} pin, PWM₁ pin or CNTR₂ pin is inverted each time the timer underflows.

<Use>

- Piezoelectric buzzer output; see "(3) Timer application example 2"
- Generating of the remote control carrier waveforms

[Function 4] Count of external pulses (Timer 2, Timer 4, Timer X: event counter mode)

External pulses input to the CNTR₀ pin, CNTR₁ pin, CNTR₂ pin are counted as the timer count source (in the event counter mode).

<Use>

- Frequency measurement; see "(4) Timer application example 3"
- Division of external pulses
- Generating of interrupts due to a cycle using external pulses as the count source; count of a reel pulse

[Function 5] Output of PWM signal (Timer 6)

"H" interval and "L" interval are specified, respectively, and the output of pulses from P4₄/PWM₁ pin is repeated.

<Use>

- Control of electric volume

[Function 6] Measurement of external pulse width (Timer X: pulse width measurement mode)

The "H" or "L" level width of external pulses input to CNTR₂ pin is measured.

<Use>

- Measurement of external pulse frequency (measurement of pulse width of FG pulse* for a motor); see "(5) Timer application example 4"
 - Measurement of external pulse duty (when the frequency is fixed)
- FG pulse*: Pulse used for detecting the motor speed to control the motor speed.

[Function 7] Control of real time port (Timer X: real time port function)

The data for real time is output from the P8₅ pin or P8₆ pin each time the timer underflows.

<Use>

- Stepping motor control; see "(6) Timer application example 5"

APPLICATION

2.2 Timer

(2) Timer application example 1: Clock function (measurement of 1 s)

Outline: The input clock is divided by the timer so that the clock can count up at 1 s intervals.

Specifications: •The clock $f(X_{IN}) = 4.19 \text{ MHz}$ (2^{22} Hz) is divided by the timer.

- The timer 3 interrupt request bit is checked in main routine, and if the interrupt request is issued, the clock is counted up.
- The timer 1 interrupt occurs every $244 \mu\text{s}$ to execute processing of other interrupts.

Figure 2.2.15 shows the timers connection and setting of division ratios; Figure 2.2.16 shows the relevant registers setting; Figure 2.2.17 shows the control procedure.

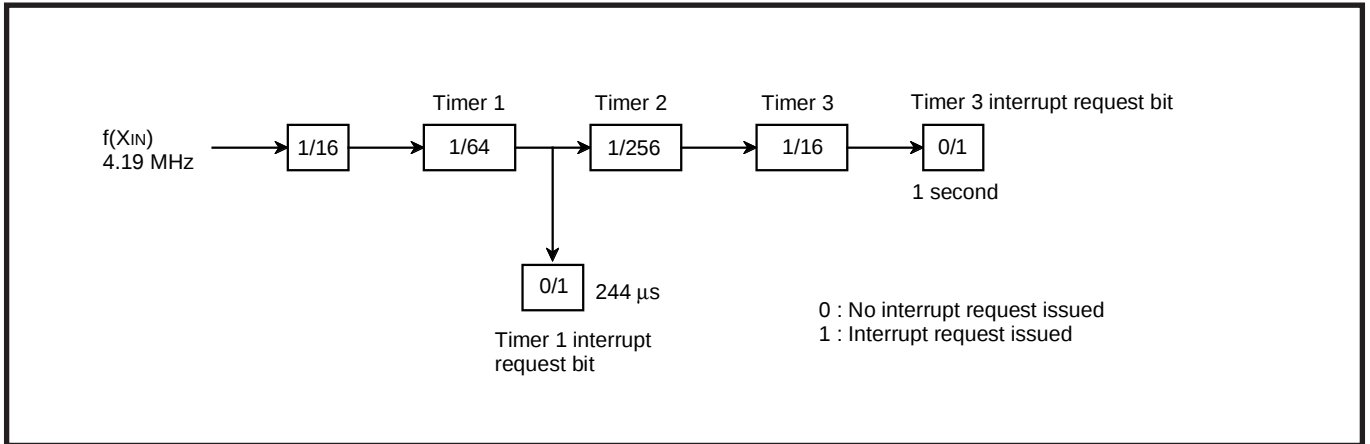


Fig. 2.2.15 Timers connection and setting of division ratios

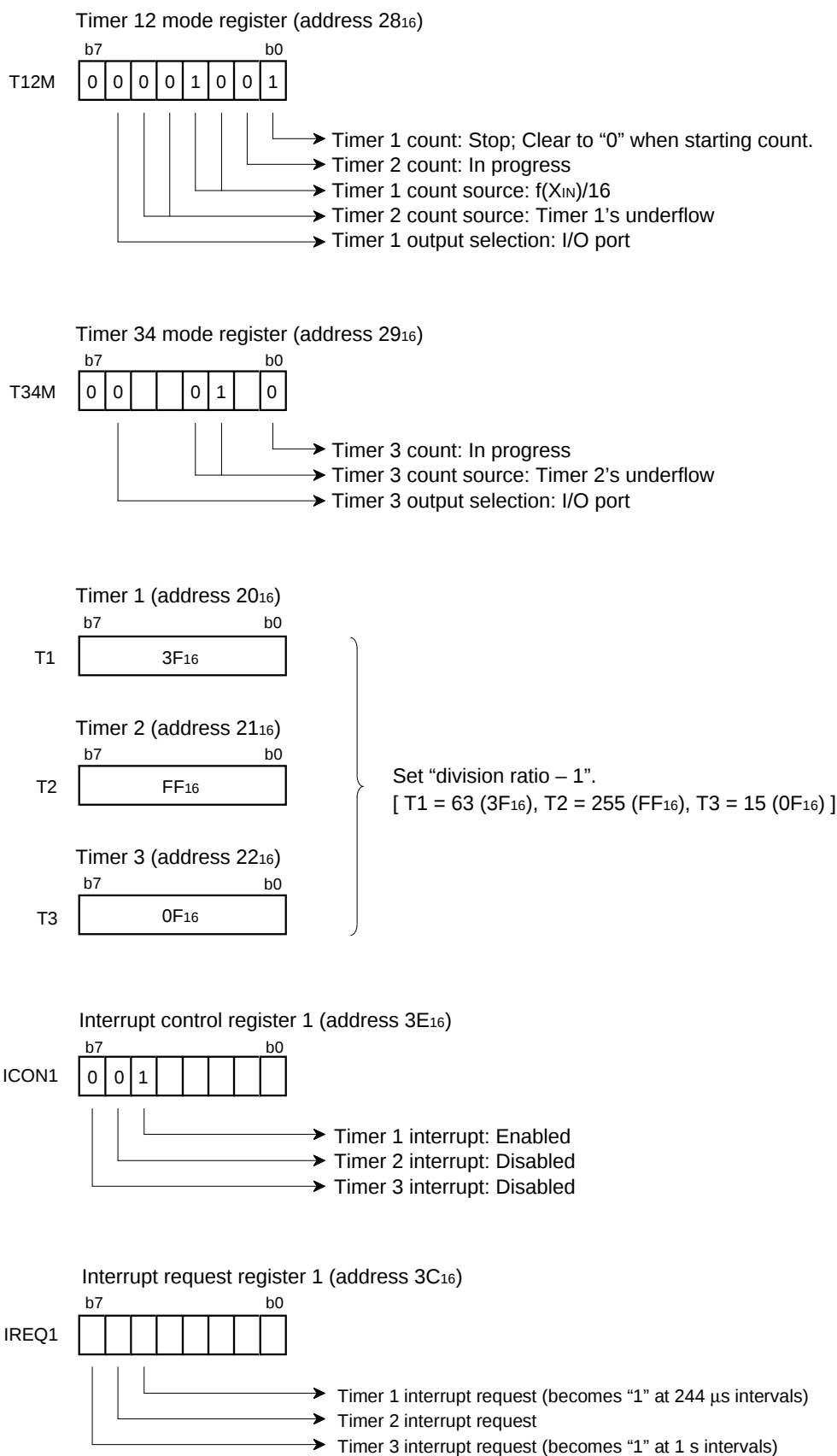


Fig. 2.2.16 Relevant registers setting

APPLICATION

2.2 Timer

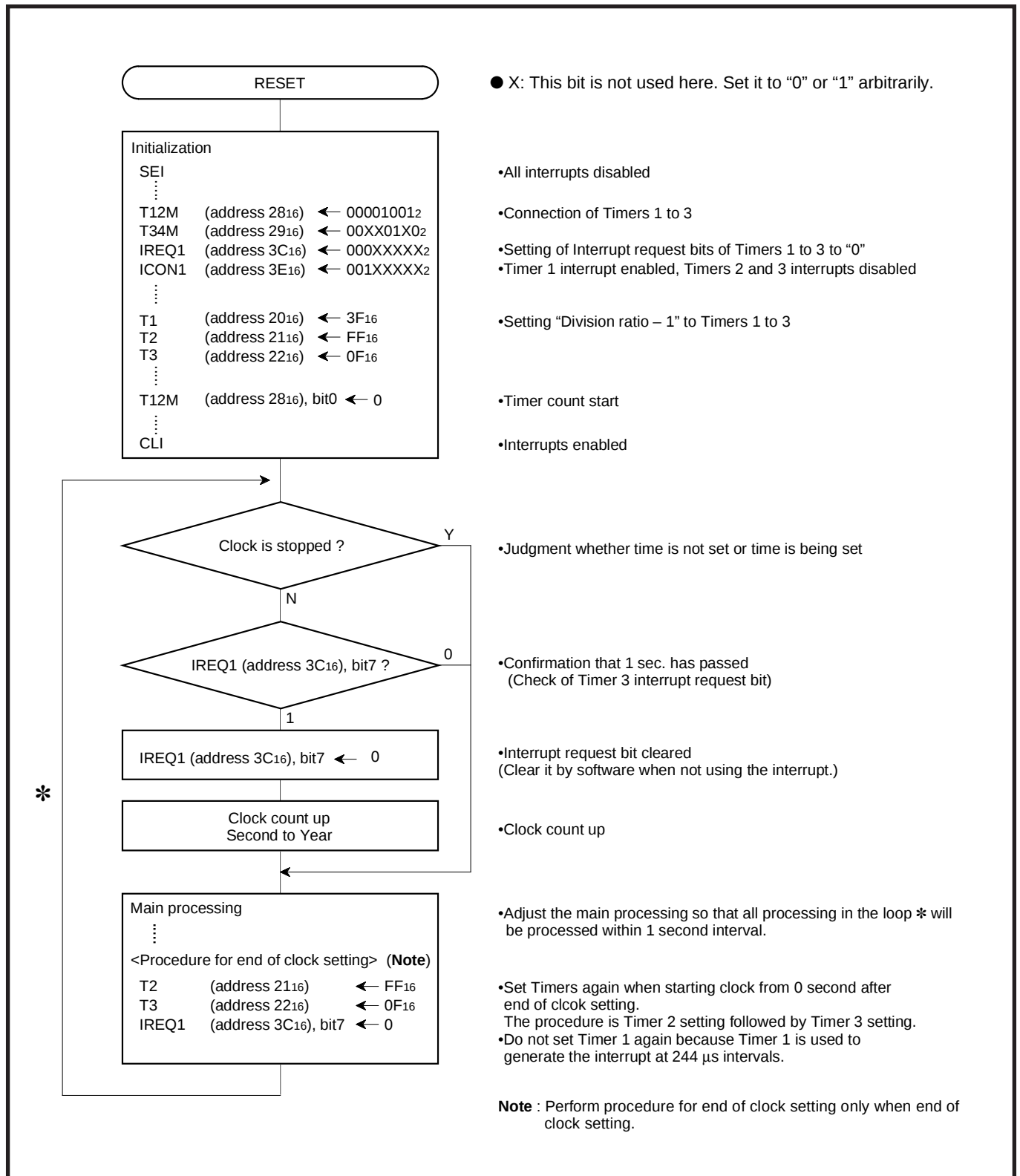


Fig. 2.2.17 Control procedure

(3) Timer application example 2: Piezoelectric buzzer output

Outline: The rectangular waveform output function of the timer is applied for a piezoelectric buzzer output.

Specifications:

- The rectangular waveform, dividing the clock $f(X_{IN}) = 4.19 \text{ MHz}$ (2^{22} Hz) into about 2 kHz (2048 Hz), is output from the P4₆/T_{3OUT} pin.
- The level of the P4₆/T_{3OUT} pin is fixed to “H” while a piezoelectric buzzer output stops.

Figure 2.2.18 shows a peripheral circuit example, and Figure 2.2.19 shows the timers connection and setting of division ratios. Figures 2.2.20 shows the relevant registers setting, and Figure 2.2.21 shows the control procedure.

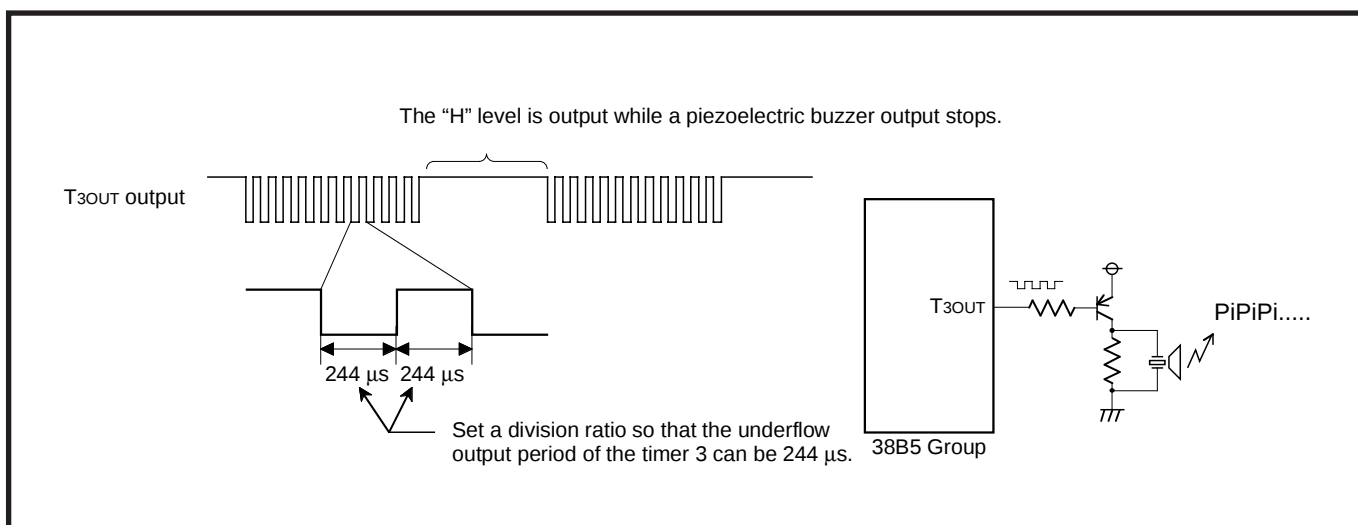


Fig. 2.2.18 Peripheral circuit example

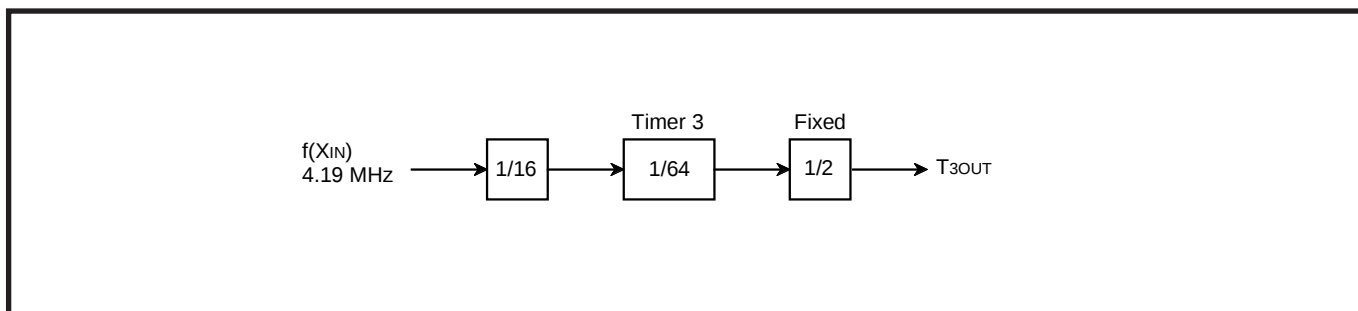


Fig. 2.2.19 Timers connection and setting of division ratios

APPLICATION

2.2 Timer

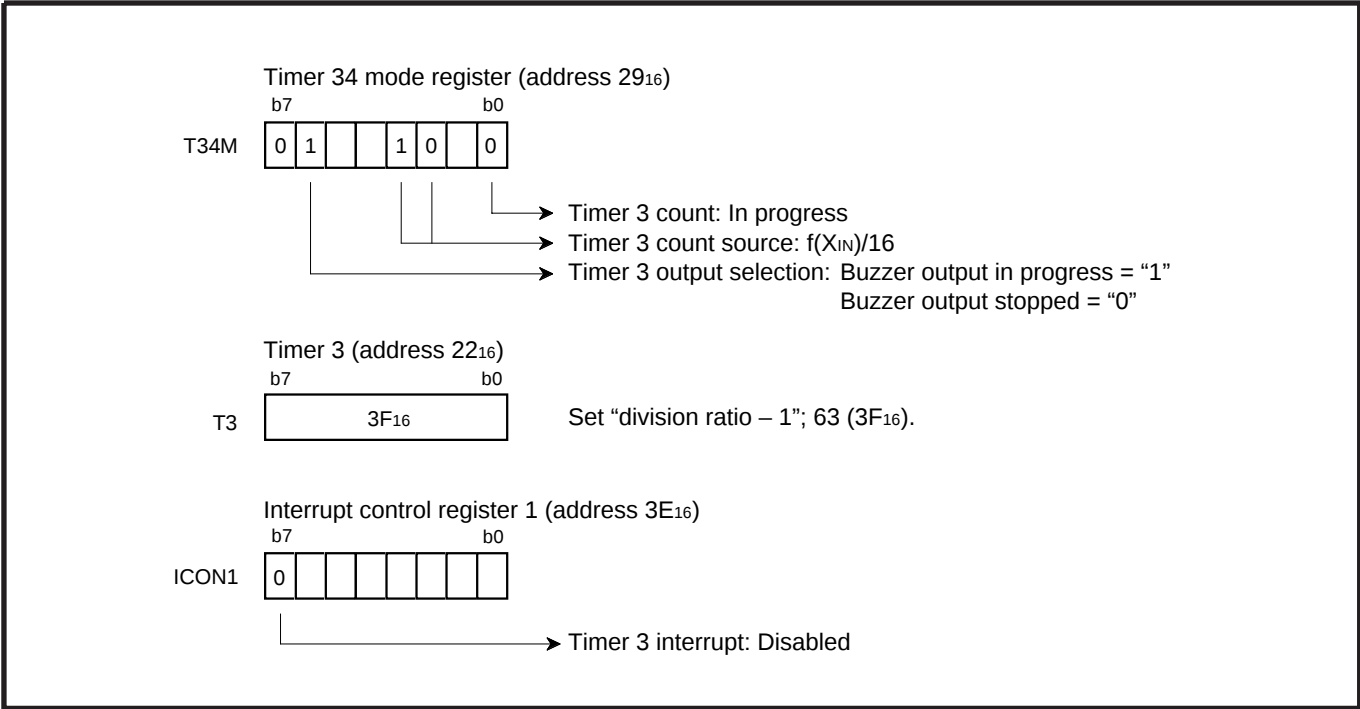


Fig. 2.2.20 Relevant registers setting

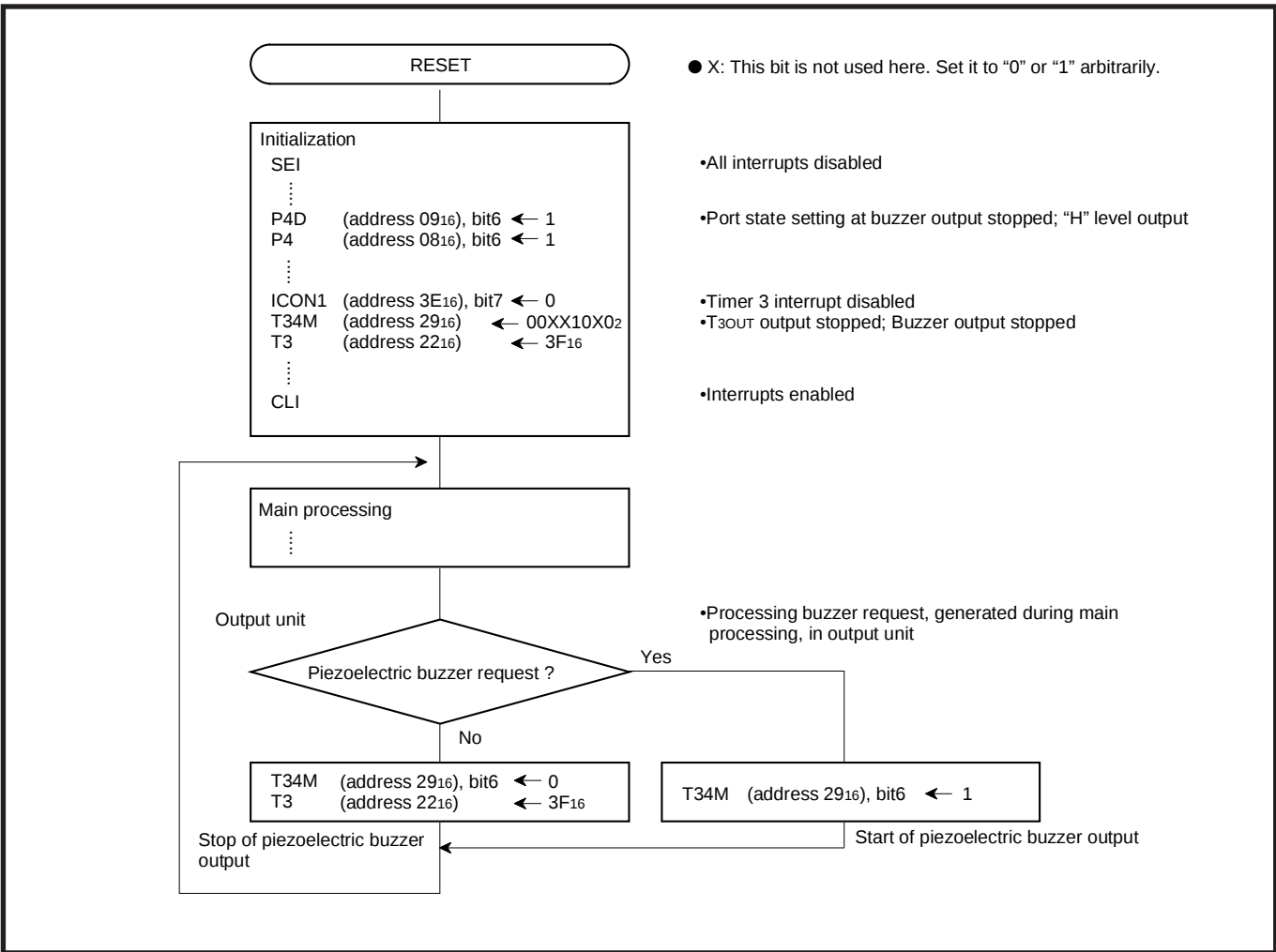


Fig. 2.2.21 Control procedure

(4) Timer application example 3: Frequency measurement

Outline: The following two values are compared to judge whether the frequency is within a valid range.

- A value by counting pulses input to P60/CNTR₁ pin with the timer.
- A reference value

Specifications: •The pulse is input to the P60/CNTR₁ pin and counted by the timer 4. (**Note 1**)
 •A count value of timer 4 is read out at about 2 ms intervals, the timer 1 interrupt interval. When the count value is 28 to 40, it is judged that the input pulse is valid.
 •Because the timer is a down-counter, the count value is compared with 227 to 215 (**Note 2**).

Notes 1: In the mask option type P, use the CNTR₀ pin and timer 2.

2: 227 to 215 = {255 (initial value of counter) – 28} to {255 – 40}; 28 to 40 means the number of valid value.

Figure 2.2.22 shows the judgment method of valid/invalid of input pulses; Figure 2.2.23 shows the relevant registers setting; Figure 2.2.24 shows the control procedure.

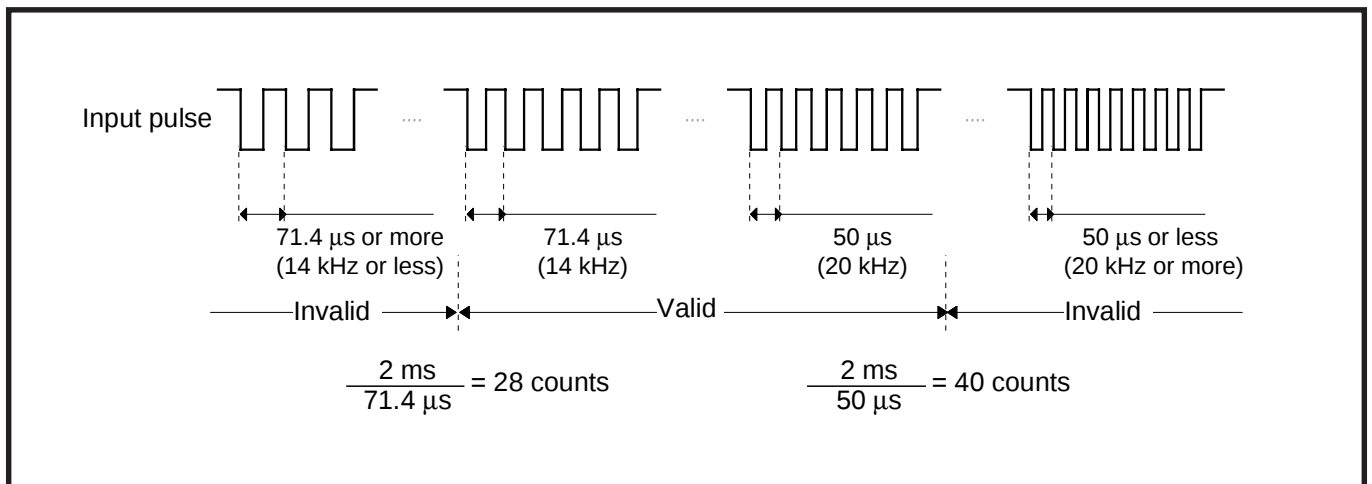


Fig. 2.2.22 Judgment method of valid/invalid of input pulses

APPLICATION

2.2 Timer

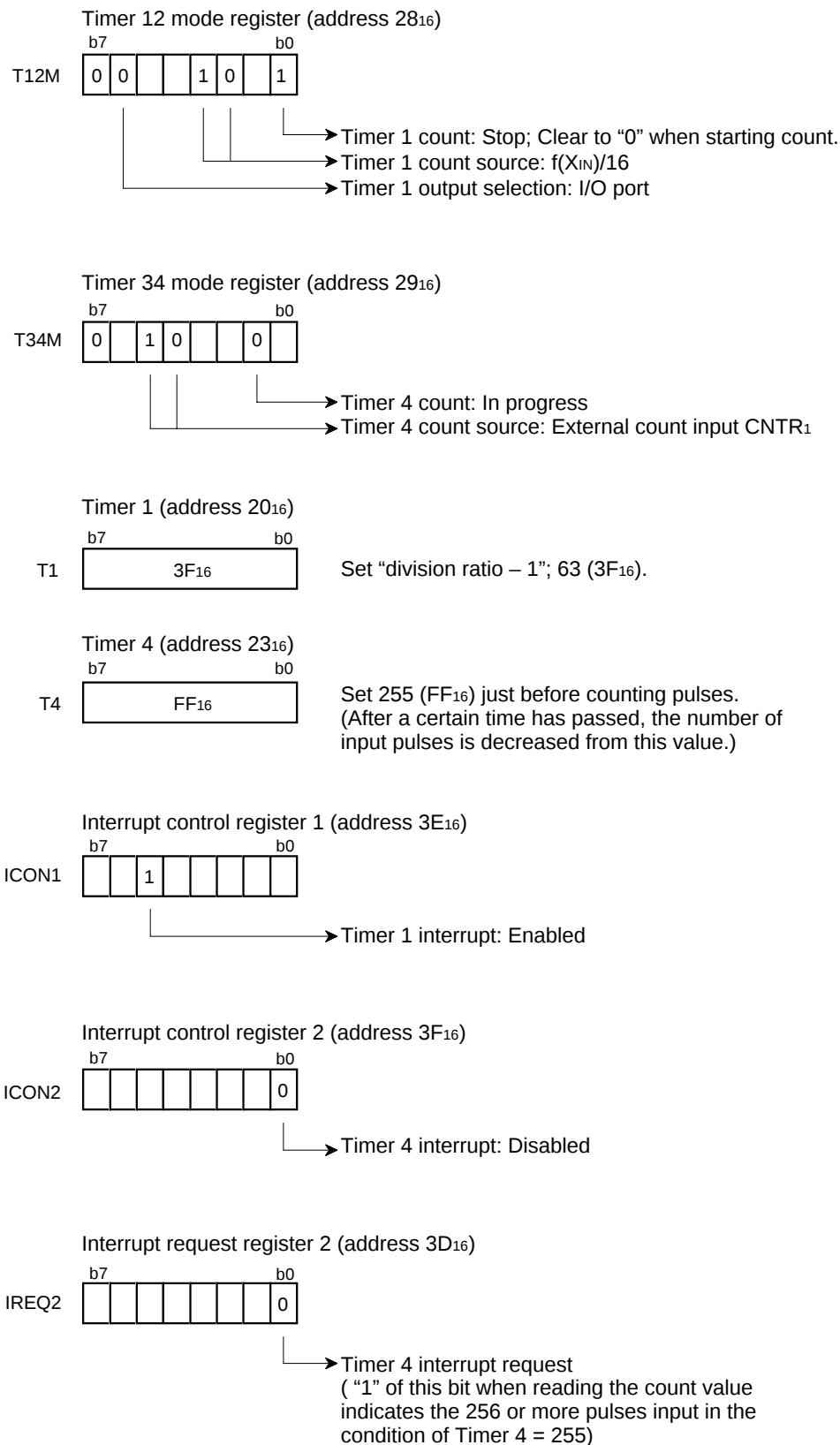


Fig. 2.2.23 Relevant registers setting

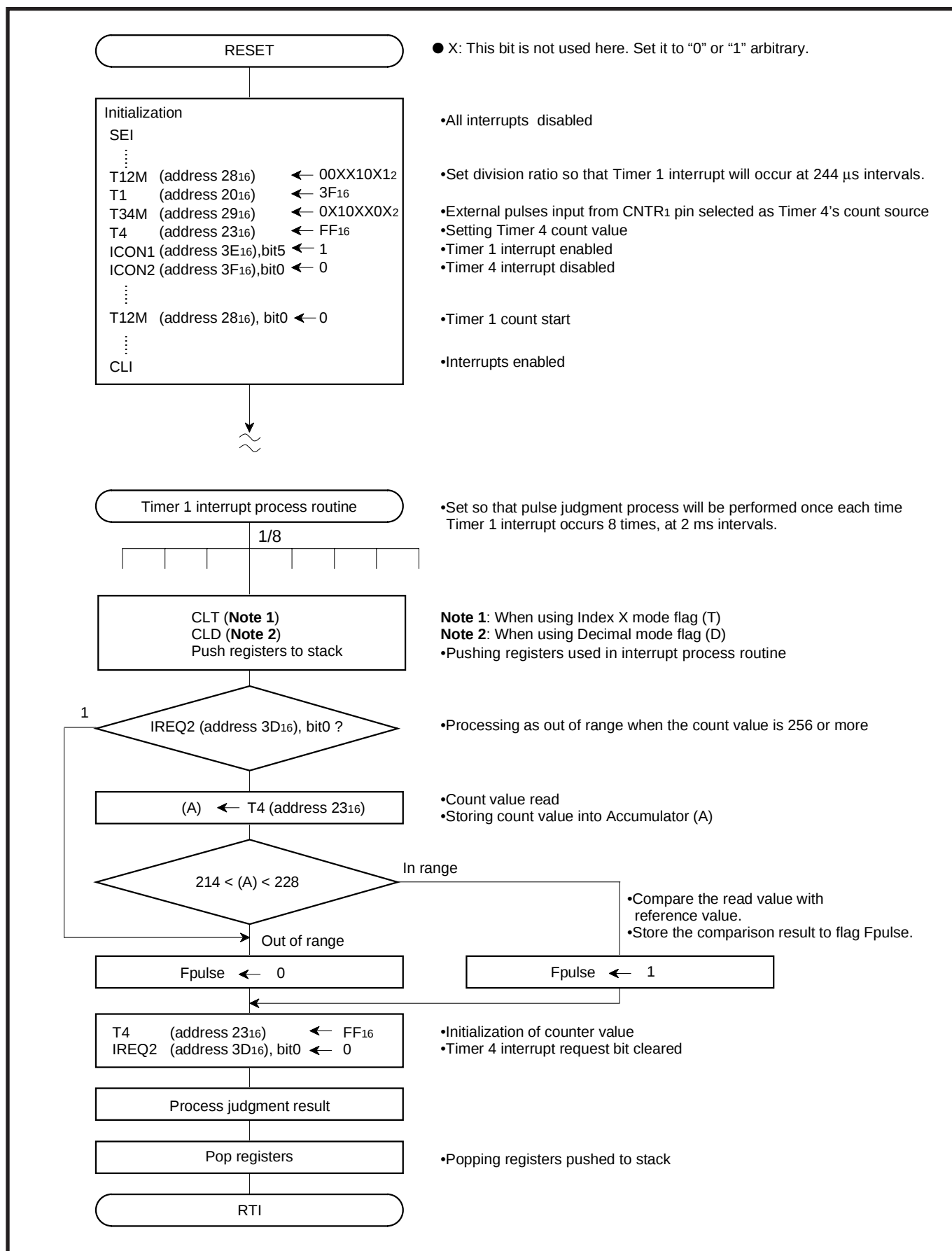


Fig. 2.2.24 Control procedure

APPLICATION

2.2 Timer

(5) Timer application example 4: Measurement of FG pulse width for motor

Outline: The timer X counts the “H” level width of the pulses input to the P6₁/CNTR₀/CNTR₂ pin. An underflow is detected by the timer X interrupt and an end of the input pulse “H” level is detected by the timer 2 interrupt of which count source is the input to P6₁/CNTR₀/CNTR₂ pin.

Specifications: •The timer X counts the “H” level width of the FG pulse input to the P6₁/CNTR₀/CNTR₂ pin.

<Example>

When $f(X_{IN}) = 4.19 \text{ MHz}$, the count source is $15.2 \mu\text{s}$, which is obtained by dividing the clock frequency by 64. Measurement can be made up to 1 s in the range of FFFF_{16} to 0000_{16} .

Figure 2.2.25 shows the timers connection and setting of division ratio; Figure 2.2.26 shows the relevant registers setting; Figure 2.2.27 shows the control procedure.

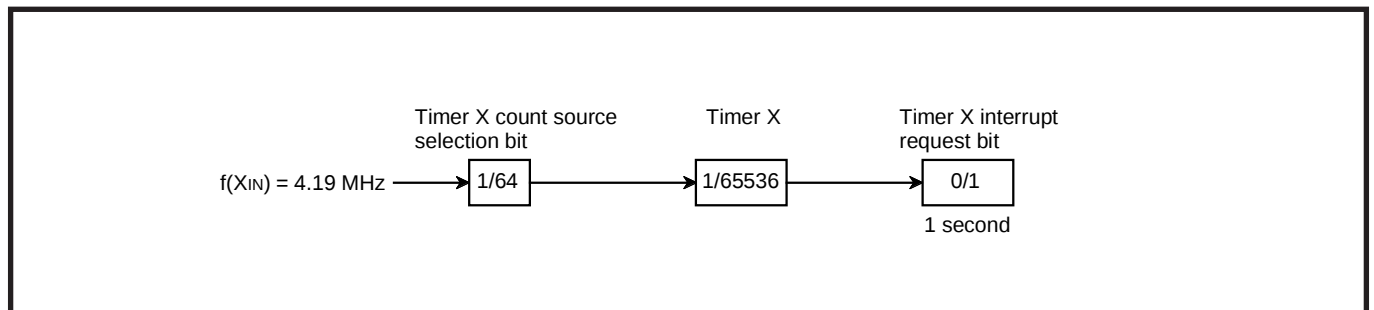


Fig. 2.2.25 Timers connection and setting of division ratios

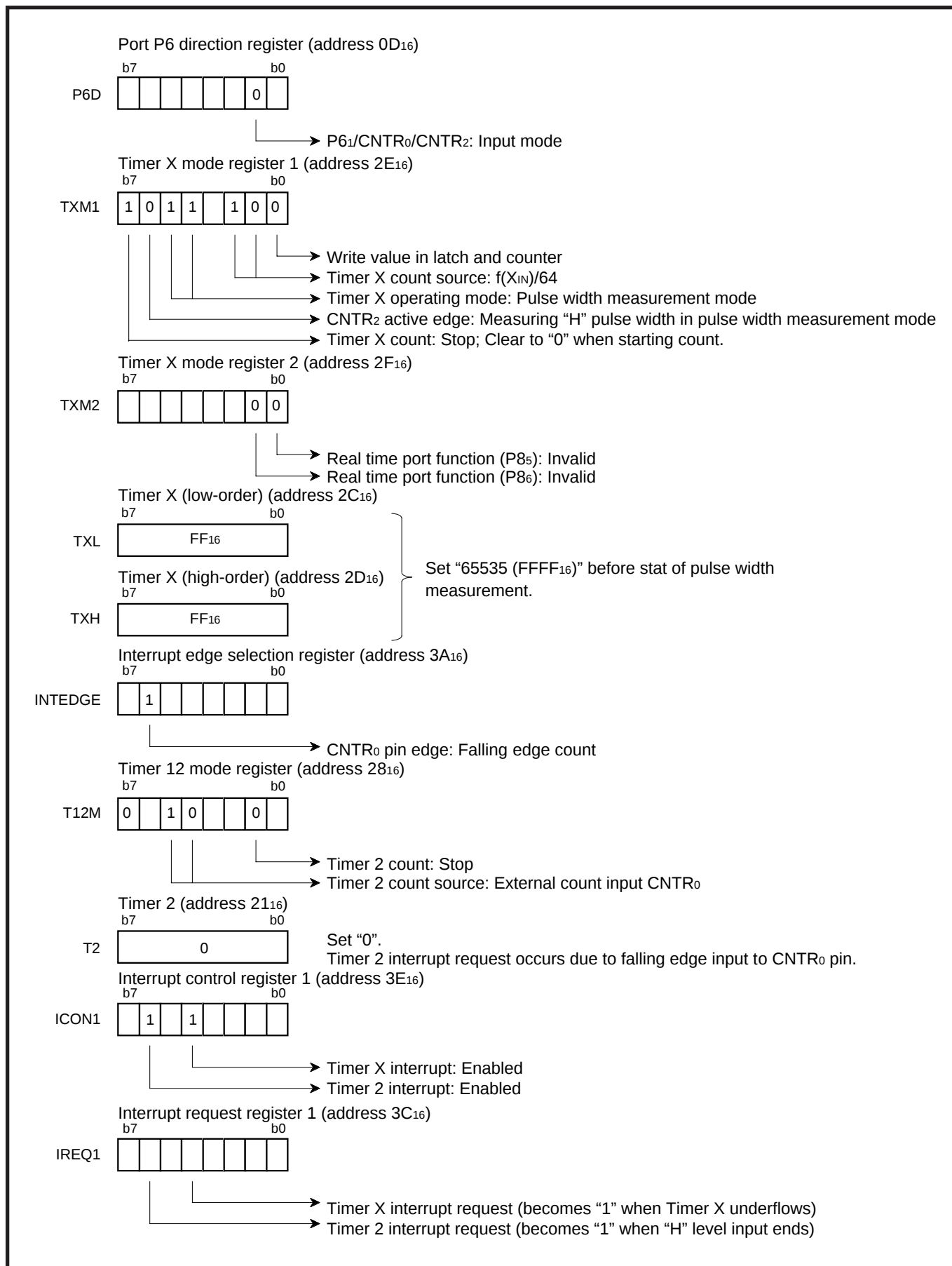
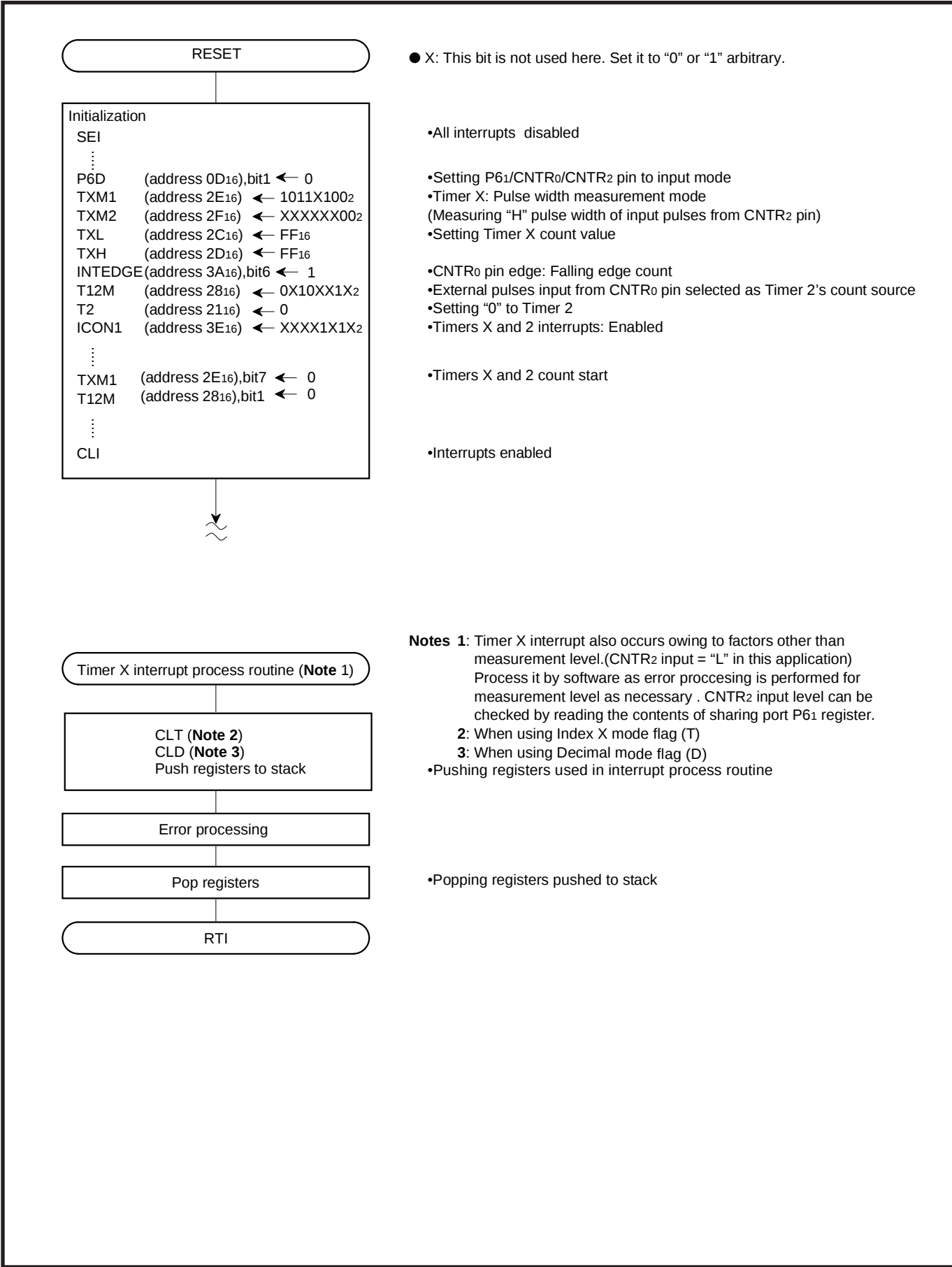
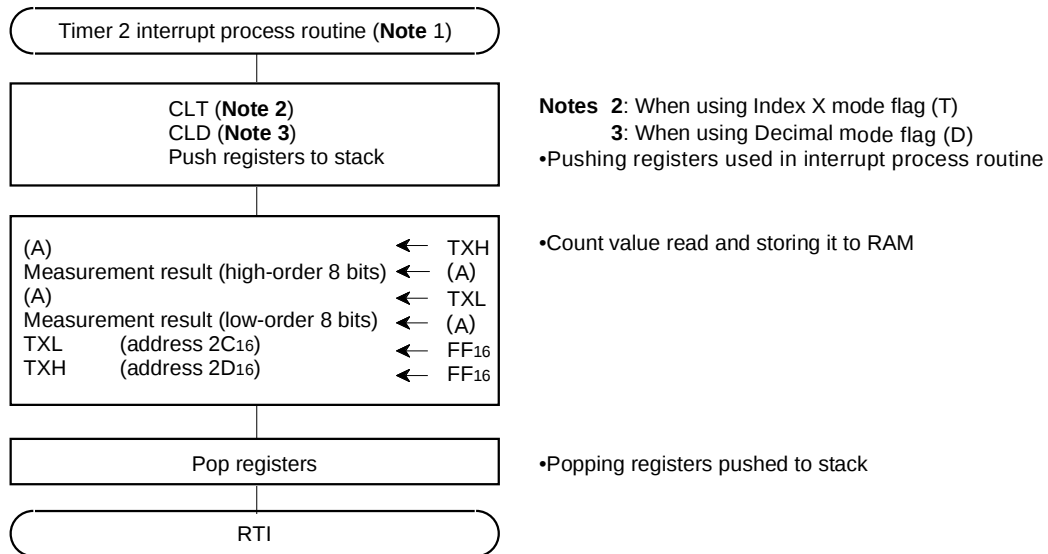


Fig. 2.2.26 Relevant registers setting

APPLICATION

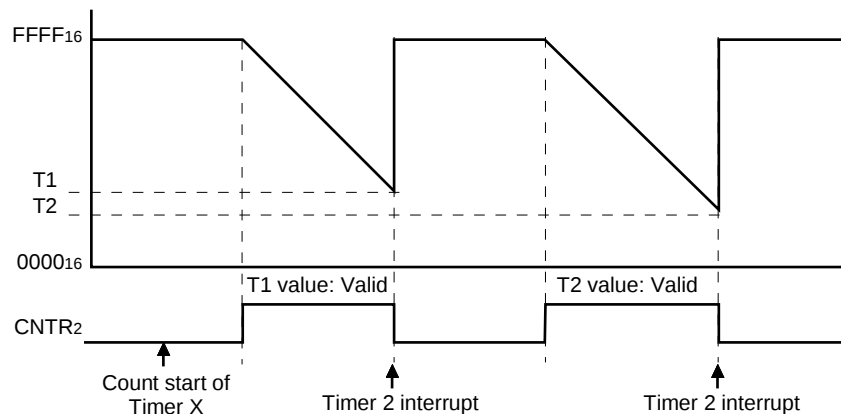
2.2 Timer



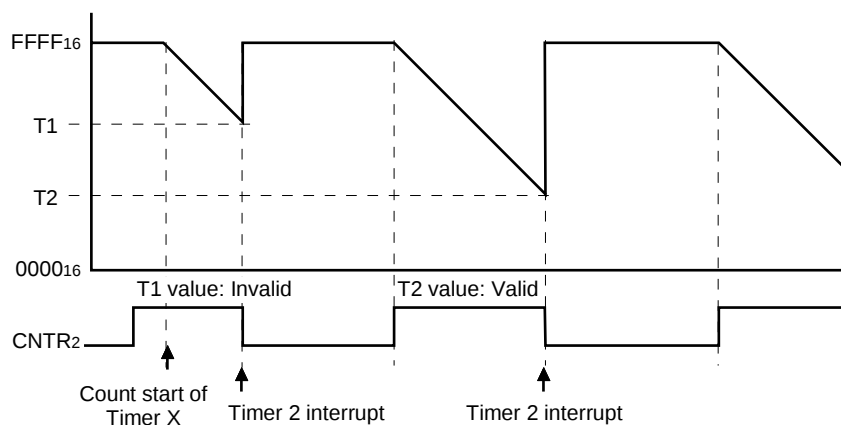


Note 1: The first value becomes invalid depending on start timing of Time X count shown by the following figure.
Process it by software as necessary.

[Example 1] • Start Timer X count when CNTR2 input level is "L".
(CNTR2 input level can be checked by reading the contents of sharing port P61 register.)



[Example 2] • Start Timer X count when CNTR2 input level is "H".
Invalidate the first Timer 2 interrupt after start of Timer X count.



APPLICATION

2.2 Timer

(6) Timer application example 5: Control of stepping motor

Outline: The rotating of stepping motor is controlled by using real time output ports.

- Specifications:**
- The motor is controlled by using 2 real time output ports.
 - The count source is $f(X_{IN}) = 4.19 \text{ MHz}$ divided by 8.
 - Values of Timer X and real time output are updated in the timer X interrupt routine

Figure 2.2.28 shows the timers connection and the table example of timer X/RTP setting values; Figure 29 shows the RTP output example; Figure 2.2.30 shows the relevant registers setting; Figure 2.2.31 shows the control procedure.

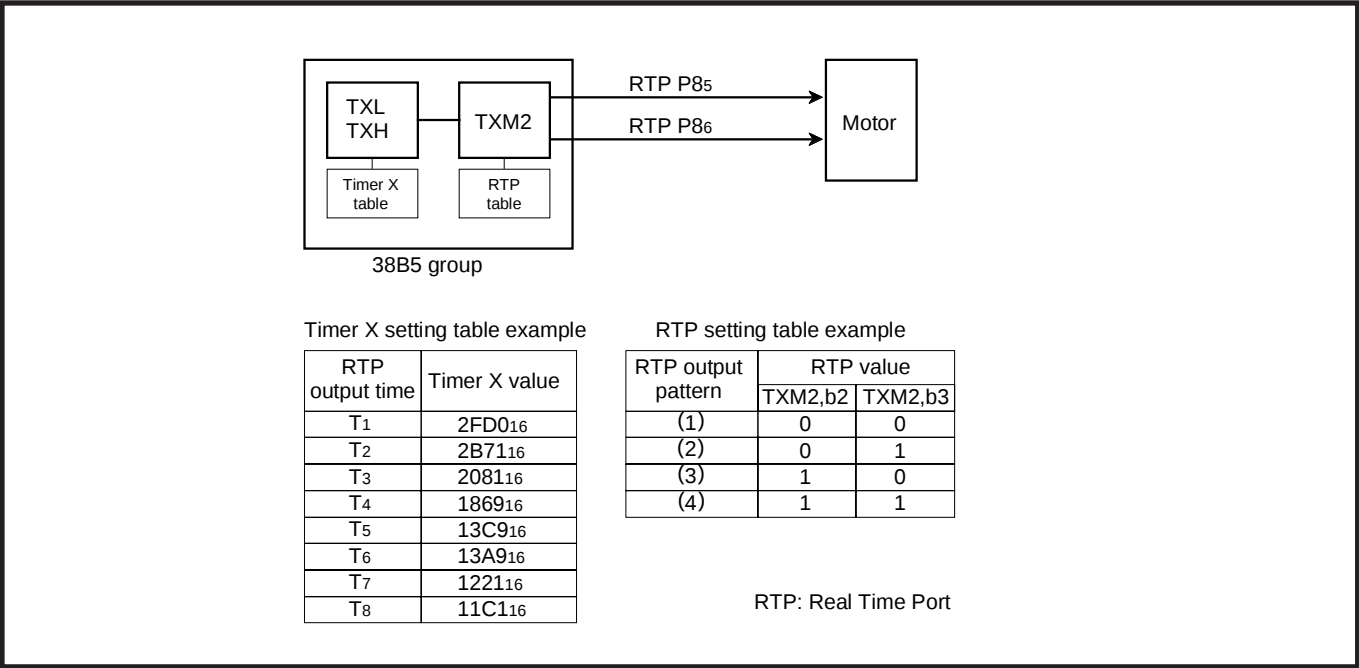


Fig. 2.2.28 Timers connection and table example of timer X/RTP setting values

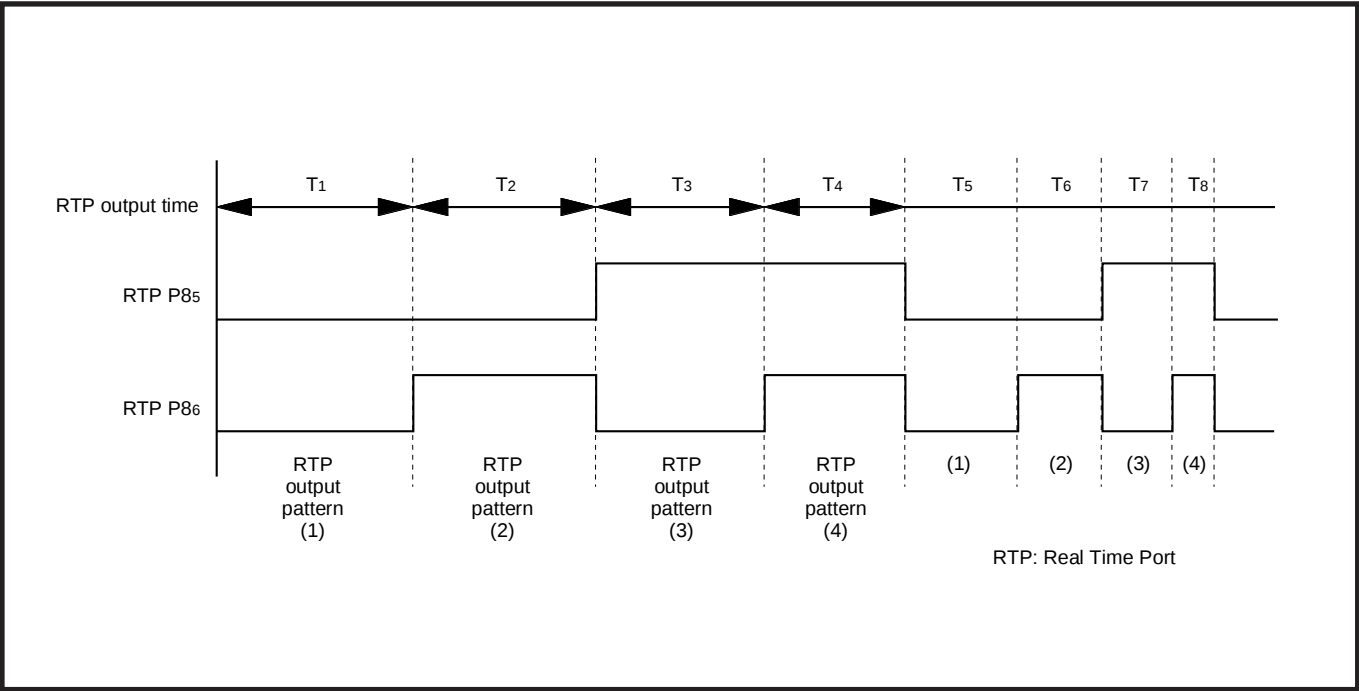


Fig. 2.2.29 RTP output example

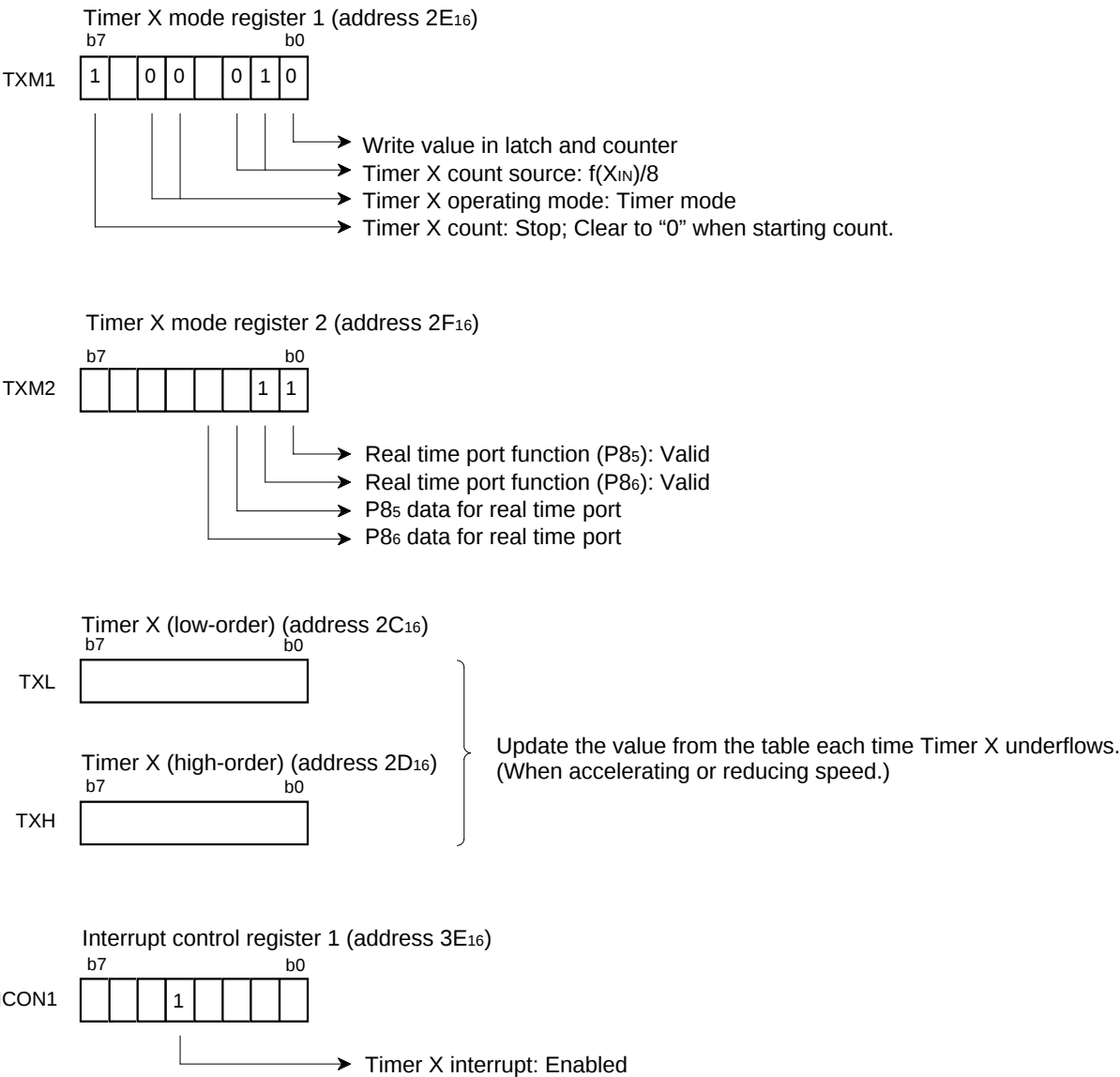


Fig. 2.2.30 Relevant registers setting

APPLICATION

2.2 Timer

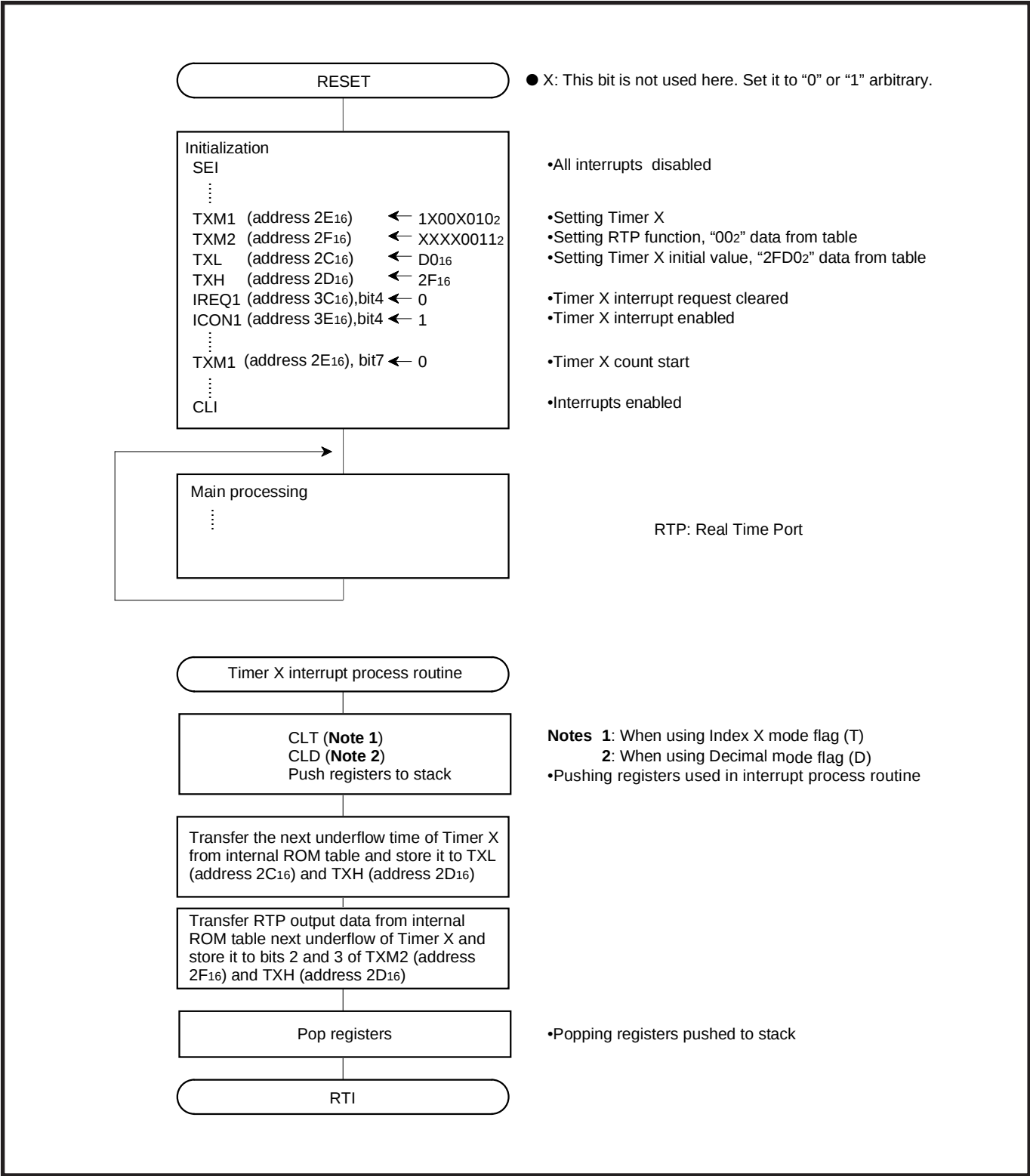


Fig. 2.2.31 Control procedure

2.3 Serial I/O

This paragraph explains the registers setting method and the notes relevant to the serial I/O.

2.3.1 Memory map

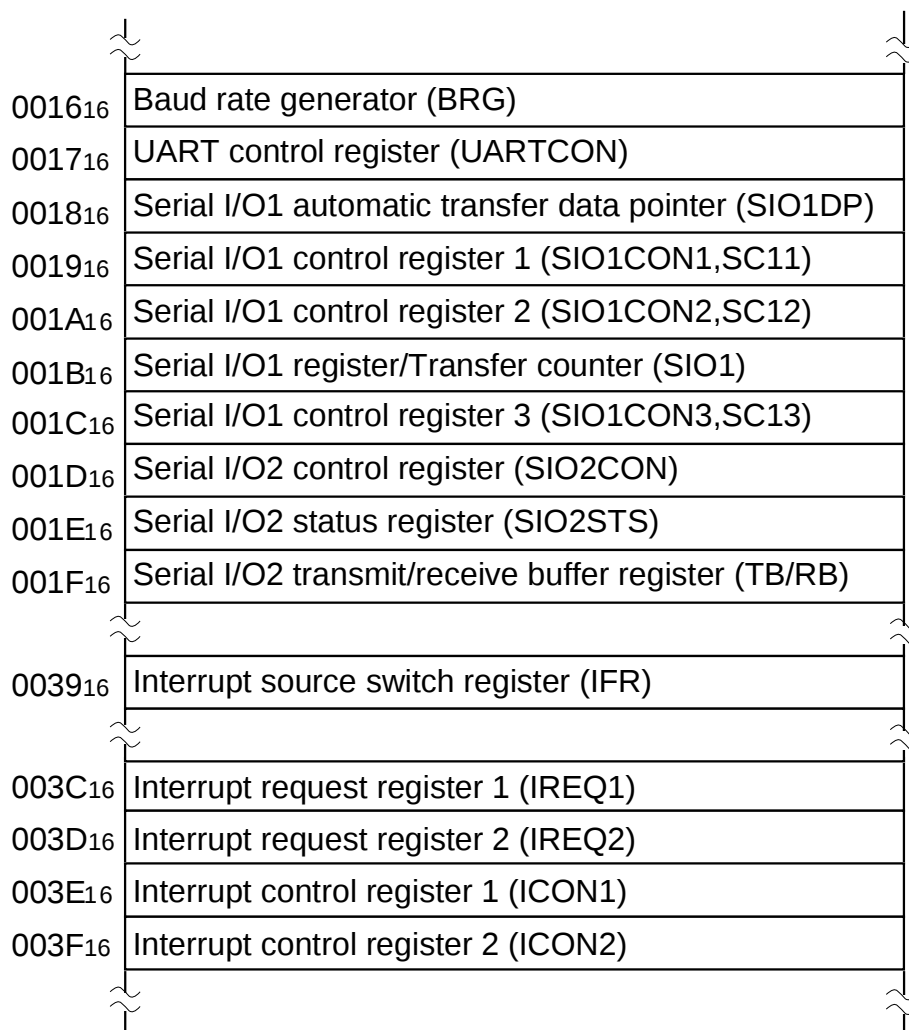


Fig. 2.3.1 Memory map of registers relevant to Serial I/O

APPLICATION

2.3 Serial I/O

2.3.2 Relevant registers

(1) Serial I/O1

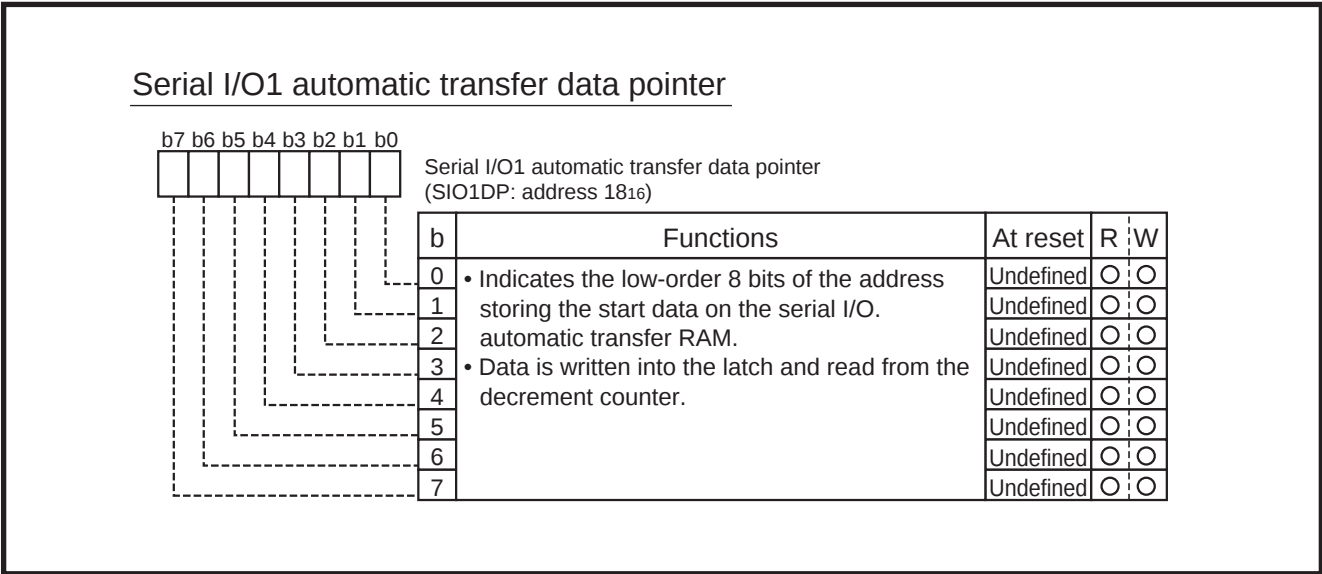


Fig. 2.3.2 Structure of Serial I/O1 automatic transfer data pointer

b7	b6	b5	b4	b3	b2	b1	b0
----	----	----	----	----	----	----	----

b	Name	Functions	At reset	R	W
0	Serial transfer selection bits	b1b0 0 0: Serial I/O disabled (Pins P62, P64, P65, P50–P53 pins are I/O ports.) 0 1: 8-bit serial I/O 1 0: Not available 1 1: Automatic transfer serial I/O (8 bits)	0	○	○
1			0	○	○
2	Serial I/O1 synchronous clock selection bits (P65/SSTB1 pin control bits)	b3b2 0 0: Internal synchronous clock (P65 pin is I/O port.) 0 1: External synchronous clock (P65 pin is I/O port.) 1 0: Internal synchronous <u>clock</u> (P65 pin is SSTB1 output.) 1 1: Internal synchronous clock (P65 pin is SSTB1 output.)	0	○	○
3			0	○	○
4	Serial I/O initialization bit	0: Serial I/O initialization 1: Serial I/O enabled	0	○	○
5	Transfer mode selection bit	0: Full-duplex (transmit/receive) mode (P50 pin is S _{IN1} input.) 1: Transmit-only mode (P50 pin is I/O port.)	0	○	○
6	Transfer direction selection bit	0: LSB first 1: MSB first	0	○	○
7	Serial I/O1 clock pin selection bit	0: SCLK11 (P53/SCLK12 pin is I/O port.) 1: SCLK12 (P52/SCLK11 pin is I/O port.)	0	○	○

Fig. 2.3.3 Structure of Serial I/O1 control register 1

APPLICATION

2.3 Serial I/O

Serial I/O1 control register 2

Serial I/O1 control register 2 (SIO1CON2 • SC12: address 1A16)							
b7	b6	b5	b4	b3	b2	b1	b0
b	Name		Functions		At reset	R	W
0	P62/SRDY1 • P64/SBUSY1 pin control bits		b3b2b1b0 0 0 0 0: P62, P64 pins are I/O ports. 0 0 0 1: Not used 0 0 1 0: P62 pin is SRDY1 output; P64 pin is I/O port. 0 0 1 1: P62 pin is SRDY1 output; P64 pin is I/O port. 0 1 0 0: P62 pin is I/O port; P64 pin is SBUSY1 input. 0 1 0 1: P62 pin is I/O port; P64 pin is SBUSY1 input. 0 1 1 0: P62 pin is I/O port; P64 pin is SBUSY1 output. 0 1 1 1: P62 pin is I/O port; P64 pin is SBUSY1 output.		0	○	○
1					0	○	○
2					0	○	○
3					0	○	○
4	SBUSY1 output • SSTB1 output function selection bit (Valid in serial I/O1 automatic transfer mode)		0: Functions as signal for each 1-byte 1: Functions as signal for each transfer data set		0	○	○
5	Serial transfer status flag		0: Serial transfer completed 1: Serial transfer in-progress		0	○	×
6	Sout1 pin control bit (when serial data is not transferred)		0: Output active 1: Output high-impedance		0	○	○
7	P51/Sout1 P-channel output disable bit		0: CMOS 3 state (P-channel output is valid.) 1: N-channel open-drain output (P-channel output is invalid.)		0	○	○

Fig. 2.3.4 Structure of Serial I/O1 control register 2

Serial I/O1 register/Transfer counter

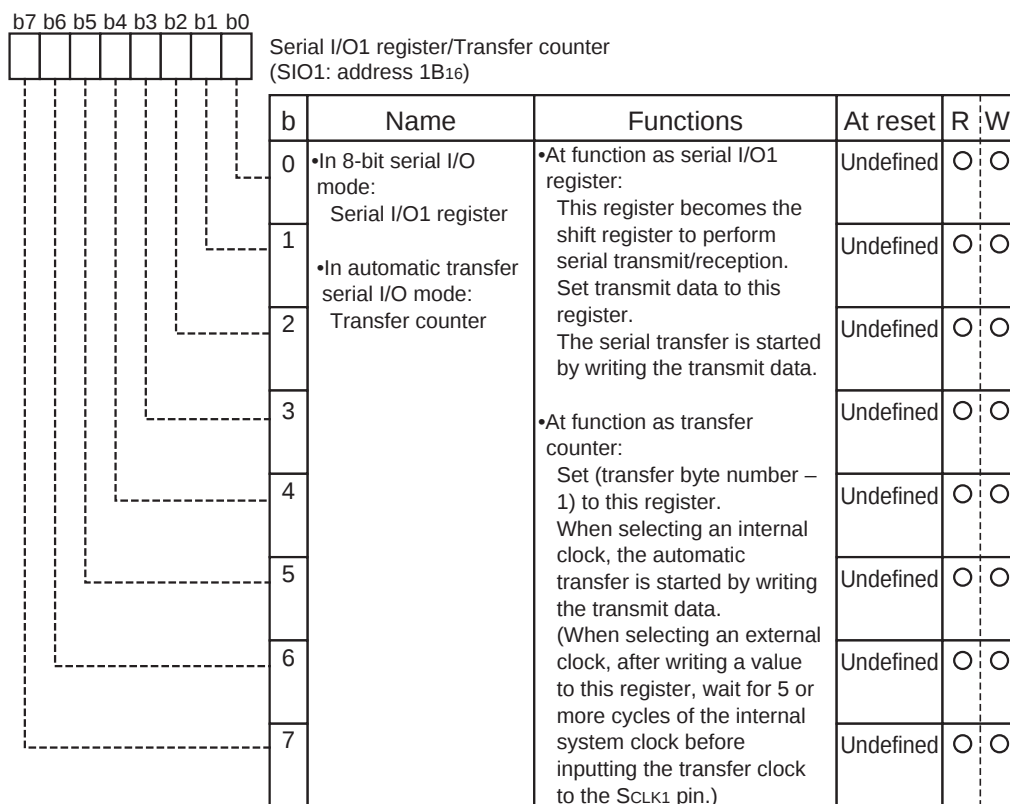


Fig. 2.3.5 Structure of Serial I/O1 register/Transfer counter

APPLICATION

2.3 Serial I/O

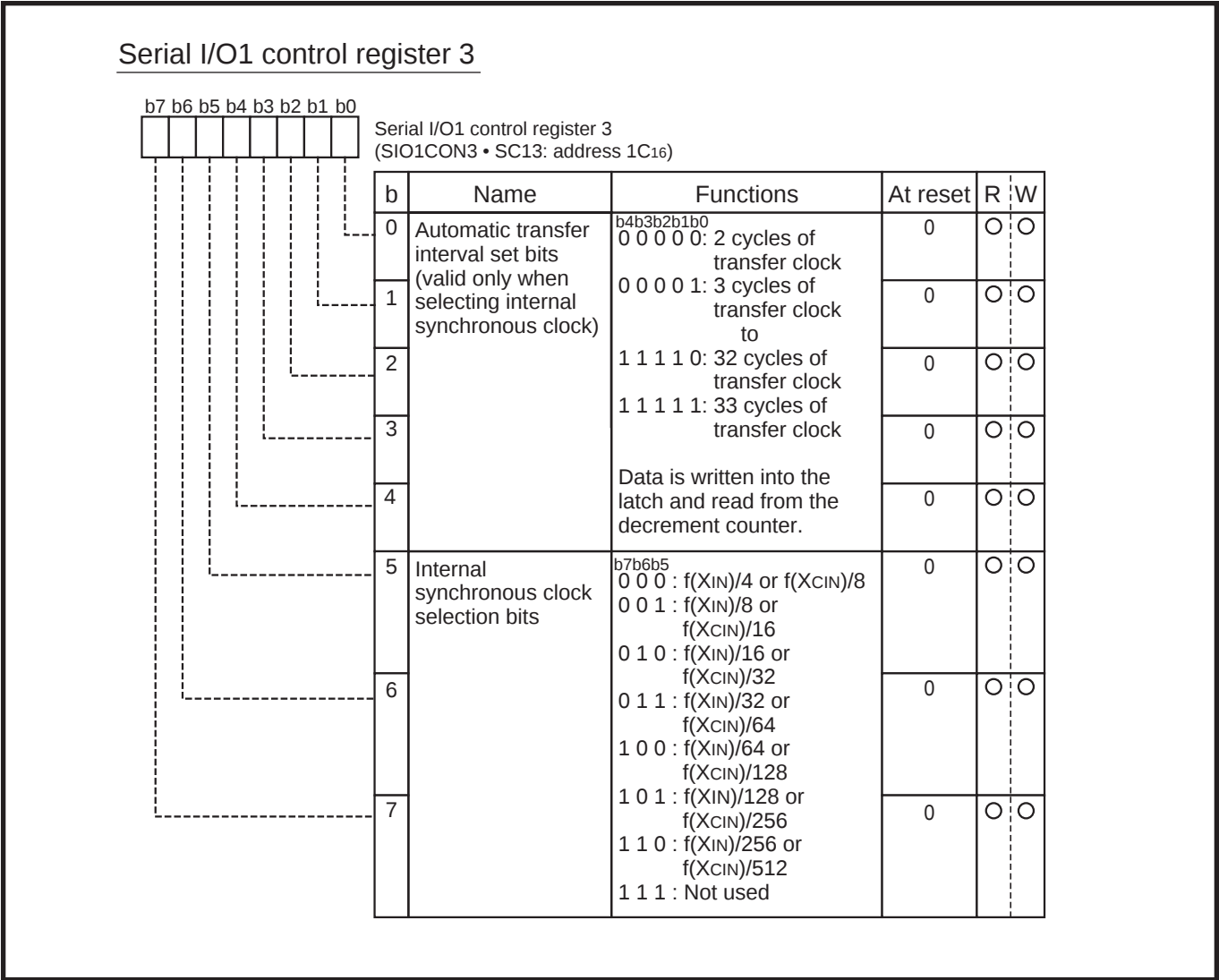


Fig. 2.3.6 Structure of Serial I/O1 control register 3

(2) Serial I/O2

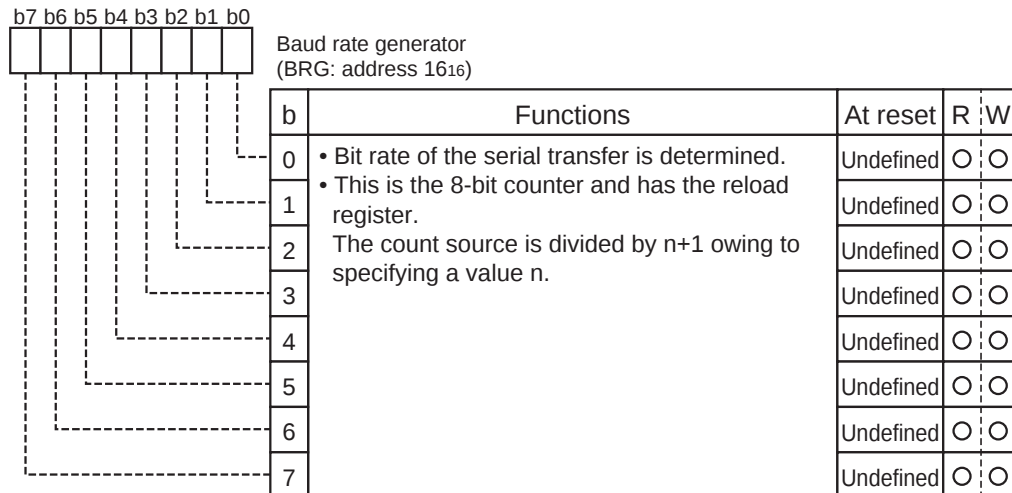
Baud rate generator

Fig. 2.3.7 Structure of Baud rate generator

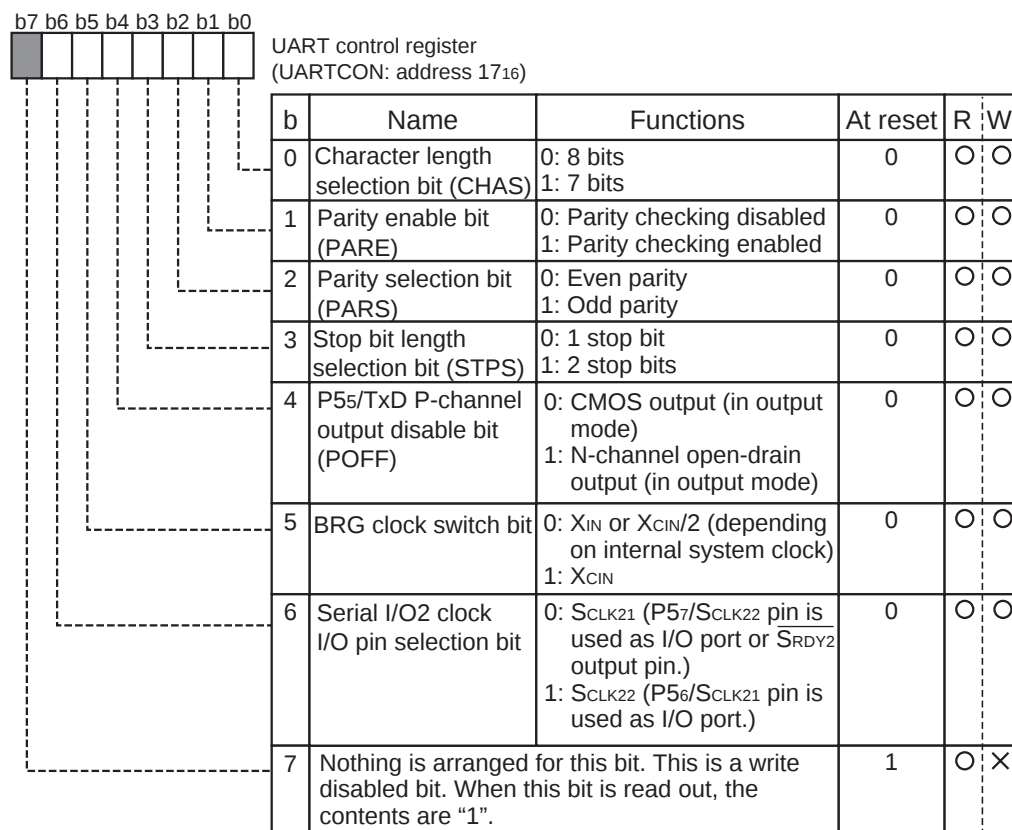
UART control register

Fig. 2.3.8 Structure of UART control register

APPLICATION

2.3 Serial I/O

Serial I/O2 control register

Serial I/O2 control register (SIO2CON: address 1D16)							
b7	b6	b5	b4	b3	b2	b1	b0
b	Name	Functions	At reset	R	W		
0	BRG count source selection bit (CSS)	0: $f(X_{IN})$ or $f(X_{CIN})/2$ or $f(X_{CIN})$ 1: $f(X_{IN})/4$ or $f(X_{CIN})/8$ or $f(X_{CIN})/4$	0	○	○		
1	Serial I/O2 synchronous clock selection bit (SCS)	•In clock synchronous mode 0: BRG output/4 1: External clock input •In UART mode 0: BRG output/16 1: External clock input/16	0	○	○		
2	SRDY2 output enable bit (SRDY)	0: P57 pin operates as normal I/O pin 1: P57 pin operates as SRDY2 output pin	0	○	○		
3	Transmit interrupt source selection bit (TIC)	0: When transmit buffer has emptied 1: When transmit shift operation is completed	0	○	○		
4	Transmit enable bit (TE)	0: Transmit disabled 1: Transmit enabled	0	○	○		
5	Receive enable bit (RE)	0: Receive disabled 1: Receive enabled	0	○	○		
6	Serial I/O2 mode selection bit (SIOM)	0: Clock asynchronous serial I/O (UART) mode 1: Clock synchronous serial I/O mode	0	○	○		
7	Serial I/O2 enable bit (SIOE)	0: Serial I/O2 disabled (pins P54–P57 operate as normal I/O pins) 1: Serial I/O2 enabled (pins P54–P57 operate as serial I/O pins)	0	○	○		

Fig. 2.3.9 Structure of Serial I/O2 control register

Serial I/O2 status register

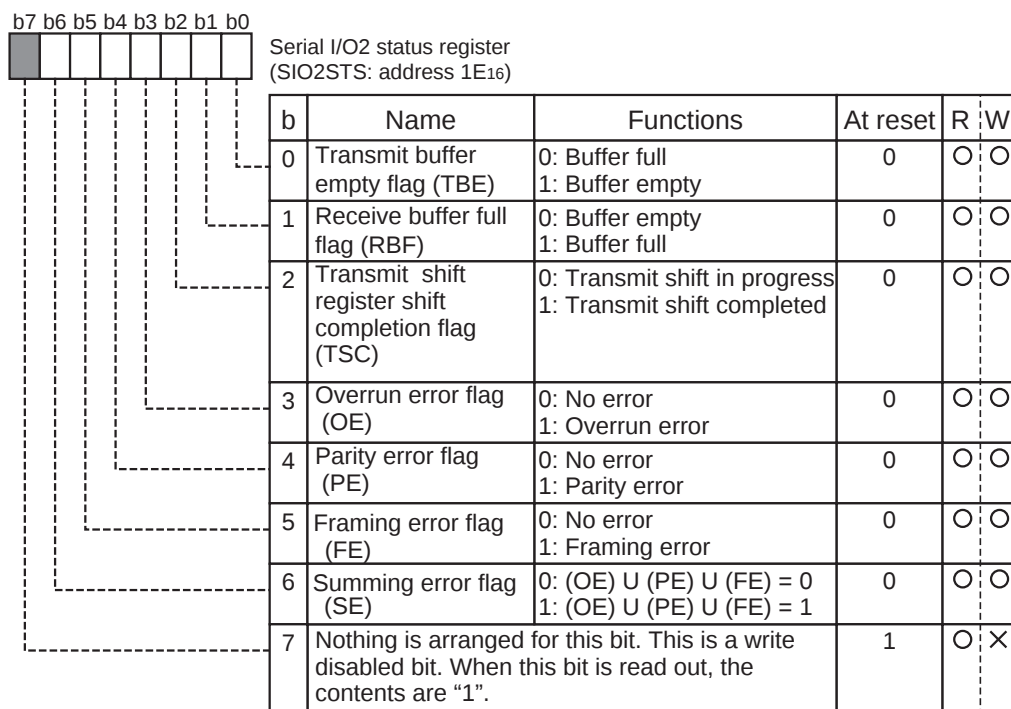


Fig. 2.3.10 Structure of Serial I/O2 status register

Serial I/O2 transmit/receive buffer register

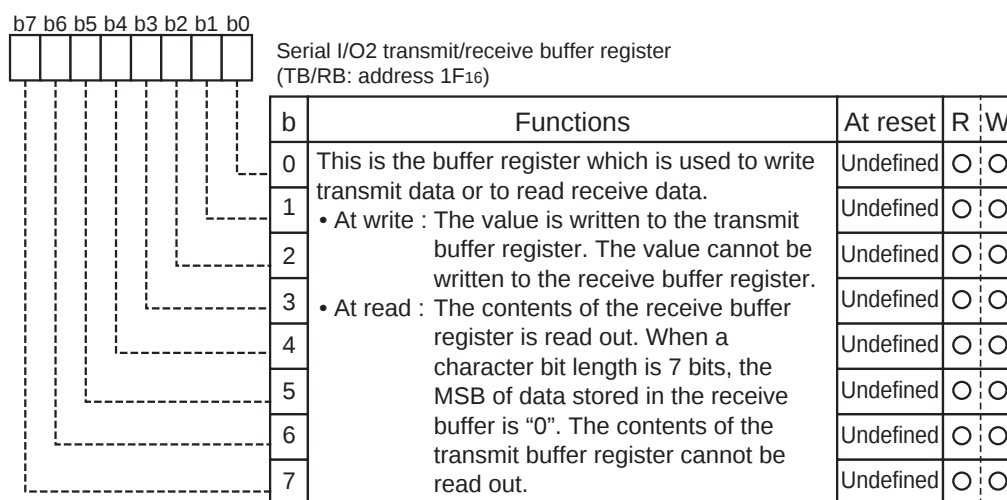


Fig. 2.3.11 Structure of Serial I/O2 transmit/receive buffer register

APPLICATION

2.3 Serial I/O

(3) Serial I/O1 and Serial I/O2

Interrupt source switch register

b7

b6

b5

b4

b3

b2

b1

b0

Interrupt source switch register

(IFR: address 39₁₆)

b	Name	Functions	At reset	R	W
0	INT3/serial I/O2 transmit interrupt switch bit (Note)	0: INT3 intrrupt 1: Serial I/O2 transmit interrupt	0	○	○
1	INT4/A-D conversion interrupt switch bit	0: INT4 interrupt 1: A-D conversion intrrerrupt	0	○	○
2	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are "0".		0	○	×
3			0	○	×
4			0	○	×
5			0	○	×
6			0	○	×
7			0	○	×

Note: In the mask option type P, this bit is not available because INT3 function is not used.

Fig. 2.3.12 Structure of Interrupt source switch register

Interrupt request register 1

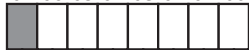
b7	b6	b5	b4	b3	b2	b1	b0	
								Interrupt request register 1 (IREQ1: address 3C16)
b	Name	Functions	At reset	R	W			
0	INT0 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	○	*			
1	INT1 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	○	*			
2	INT2 interrupt request bit Remote controller /counter overflow interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	○	*			
3	Serial I/O1 interrupt request bit Serial I/O automatic transfer interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	○	*			
4	Timer X interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	○	*			
5	Timer 1 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	○	*			
6	Timer 2 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	○	*			
7	Timer 3 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	○	*			

*: "0" can be set by software, but "1" cannot be set.

Fig. 2.3.13 Structure of Interrupt request register 1

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2
(IREQ2 : address 3D16)

b	Name	Functions	At reset	R	W
0	Timer 4 interrupt request bit (Note)	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
1	Timer 5 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
2	Timer 6 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
3	Serial I/O2 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
4	INT3/Serial I/O2 transmit interrupt request bit (Note)	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
5	INT4 interrupt request bit A-D converter interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
6	FLD blanking interrupt request bit FLD digit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
7	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are "0".		0	○	×

*: "0" can be set by software, but "1" cannot be set.

Note: In the mask option type P, if timer 4 interrupt whose count source is CNTR₁ input and INT3 interrupt are selected, these bits do not become "1".

Fig. 2.3.14 Structure of Interrupt request register 2

APPLICATION

2.3 Serial I/O

Interrupt control register 1

b7	b6	b5	b4	b3	b2	b1	b0	
								Interrupt control register 1 (ICON1 : address 3E16)
b	Name	Functions	At reset	R	W			
0	INT0 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○			
1	INT1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○			
2	INT2 interrupt enable bit Remote controller /counter overflow interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○			
3	Serial I/O1 interrupt enable bit Serial I/O automatic transfer interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○			
4	Timer X interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○			
5	Timer 1 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○			
6	Timer 2 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○			
7	Timer 3 interrupt enable bit	0 : Interrupt disabled 1 : Interrupt enabled	0	○	○			

Fig. 2.3.15 Structure of Interrupt control register 1

Interrupt control register 2

b7	b6	b5	b4	b3	b2	b1	b0
0							

Interrupt control register 2
(ICON2 : address 3F16)

b	Name	Functions	At reset	R	W
0	Timer 4 interrupt enable bit (Note)	0 : interrupt disabled 1 : Interrupt enabled	0	○	○
1	Timer 5 interrupt enable bit	0 : interrupt disabled 1 : Interrupt enabled	0	○	○
2	Timer 6 interrupt enable bit	0 : interrupt disabled 1 : Interrupt enabled	0	○	○
3	Serial I/O2 receive interrupt enable bit	0 : interrupt disabled 1 : Interrupt enabled	0	○	○
4	INT3/Serial I/O2 transmit interrupt enable bit (Note)	0 : interrupt disabled 1 : Interrupt enabled	0	○	○
5	INT4 interrupt enable bit A-D converter interrupt enable bit	0 : interrupt disabled 1 : Interrupt enabled	0	○	○
6	FLD blanking interrupt enable bit FLD digit interrupt enable bit	0 : interrupt disabled 1 : Interrupt enabled	0	○	○
7	Fix "0" to this bit.		0	○	○

Note: In the mask option type P, timer 4 interrupt whose count source is CNTR1 input and INT3 interrupt are not available.

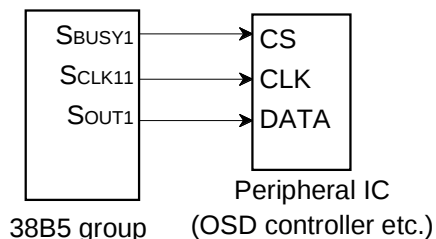
Fig. 2.3.16 Structure of Interrupt control register 2

2.3.3 Serial I/O1 connection examples

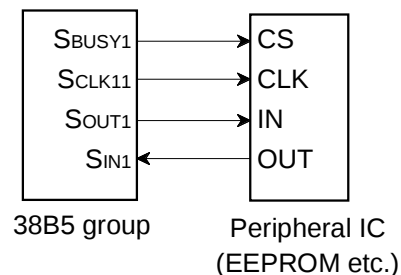
(1) Control of peripheral IC equipped with CS pin

Figure 2.3.17 shows connection examples with peripheral ICs equipped with the CS pin. All examples can use the automatic transfer function.

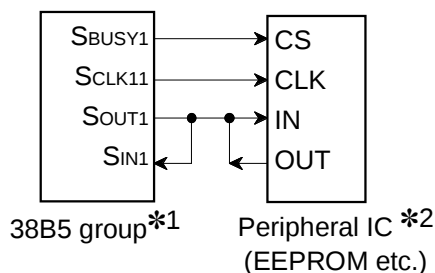
(1) Only transmission
(Using S_{IN1} pin as I/O port)



(2) Transmission and reception



(3) Transmission and reception
(When connecting S_{IN1} with S_{OUT1})
(When connecting IN with OUT in peripheral IC)



*1: Select an N-channel open-drain output for S_{OUT1} pin output control.

*2: Use the OUT pin of peripheral IC which is an N-channel open-drain output and becomes high impedance during receiving data.

Note: "Port" means an output port controlled by software.

(4) Connection of plural IC

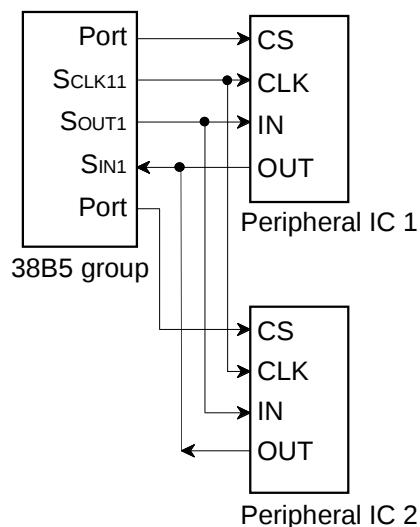


Fig. 2.3.17 Serial I/O1 connection examples (1)

APPLICATION

2.3 Serial I/O

(2) Connection with microcomputer

Figure 2.3.18 shows connection examples with another microcomputer.

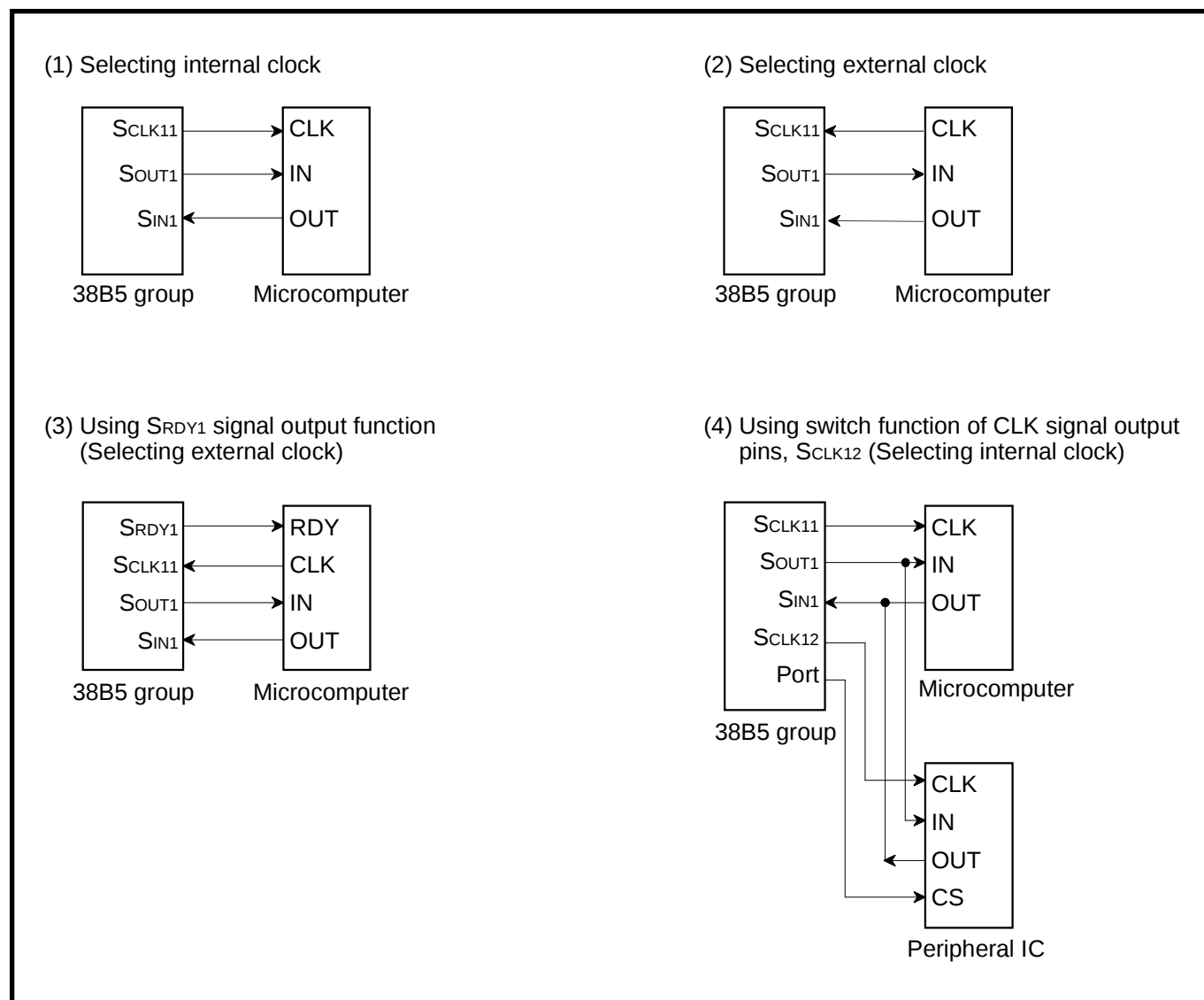


Fig. 2.3.18 Serial I/O1 connection examples (2)

2.3.4 Serial I/O1's modes

Figure 2.3.19 shows the serial I/O1's modes.

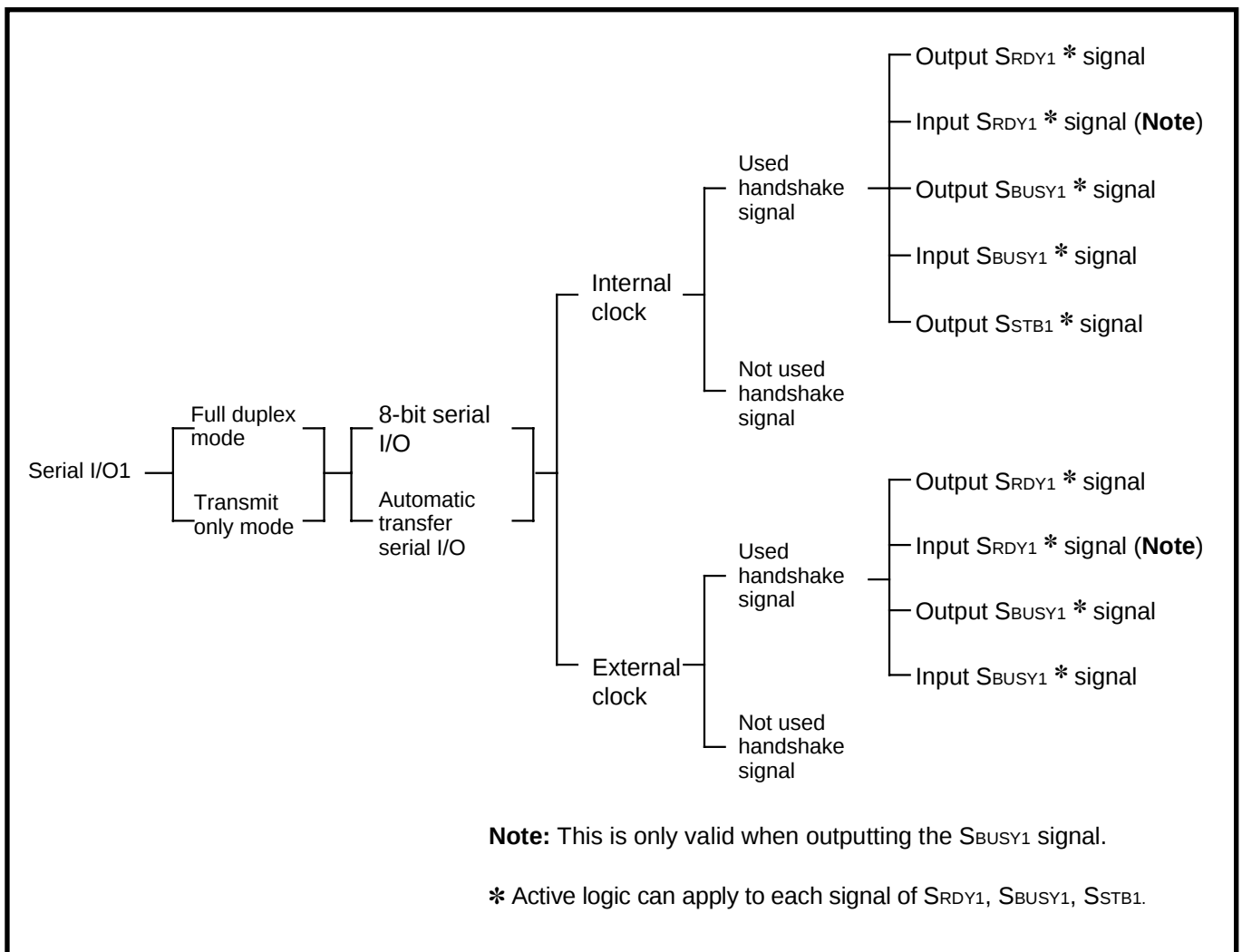


Fig. 2.3.19 Serial I/O1's modes

APPLICATION

2.3 Serial I/O

2.3.5 Serial I/O1 application examples

(1) Output of serial data (control of peripheral IC)

Outline : Serial communication is performed, connecting ports with the $\overline{CS}$ pin of a peripheral IC.

Figure 2.3.20 shows a connection diagram, and Figure 2.3.21 shows a timing chart.

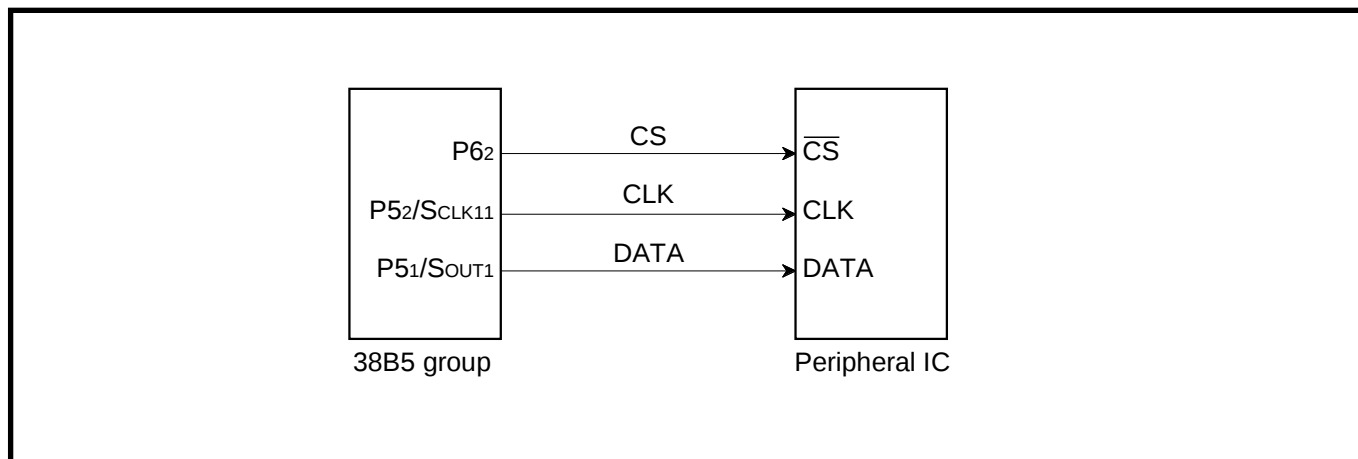


Fig. 2.3.20 Connection diagram

Specifications :

- Use of serial I/O1 (Not using automatic transfer function)

- Synchronous clock frequency : 131 kHz ($f(X_{IN}) = 4.19 \text{ MHz}$ is divided by 32)
- Transfer direction : LSB first
- Not use of serial I/O1 interrupt
- Port P6₂ is connected to the $\overline{CS}$ pin ("L" active) of the peripheral IC for transmission control; the output level of port P6₂ is controlled by software.

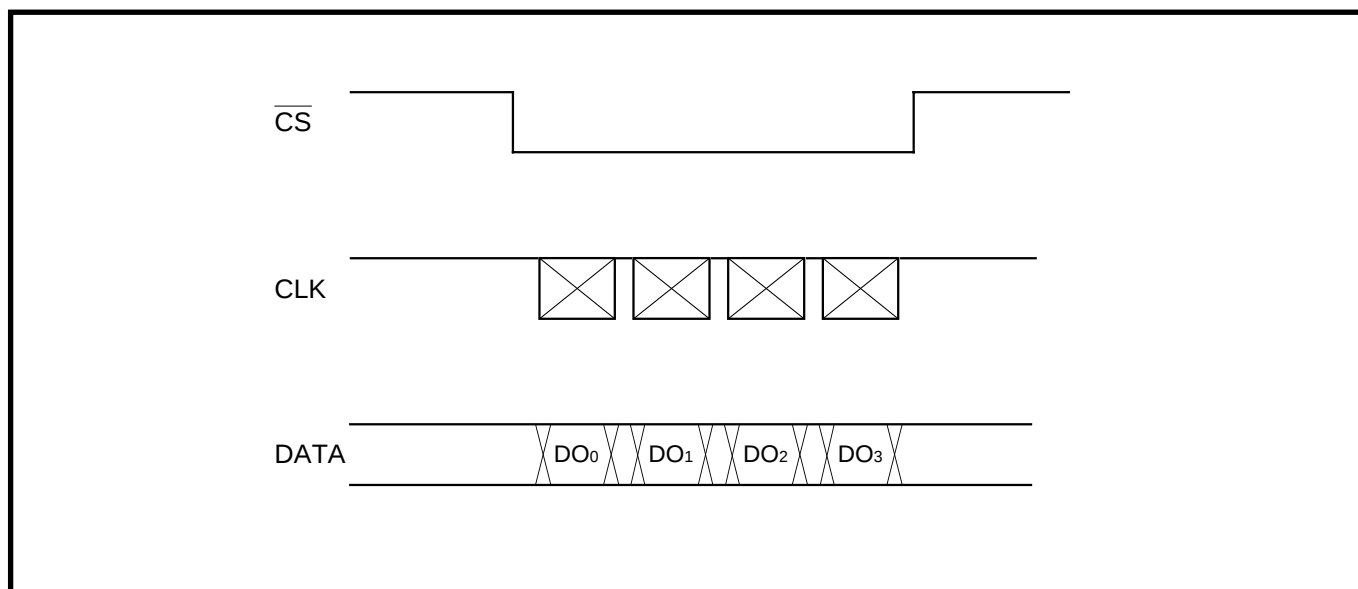


Fig. 2.3.21 Timing chart

Figure 2.3.22 shows the registers setting relevant to the transmission side, and Figure 2.3.23 shows the setting of transmission data.

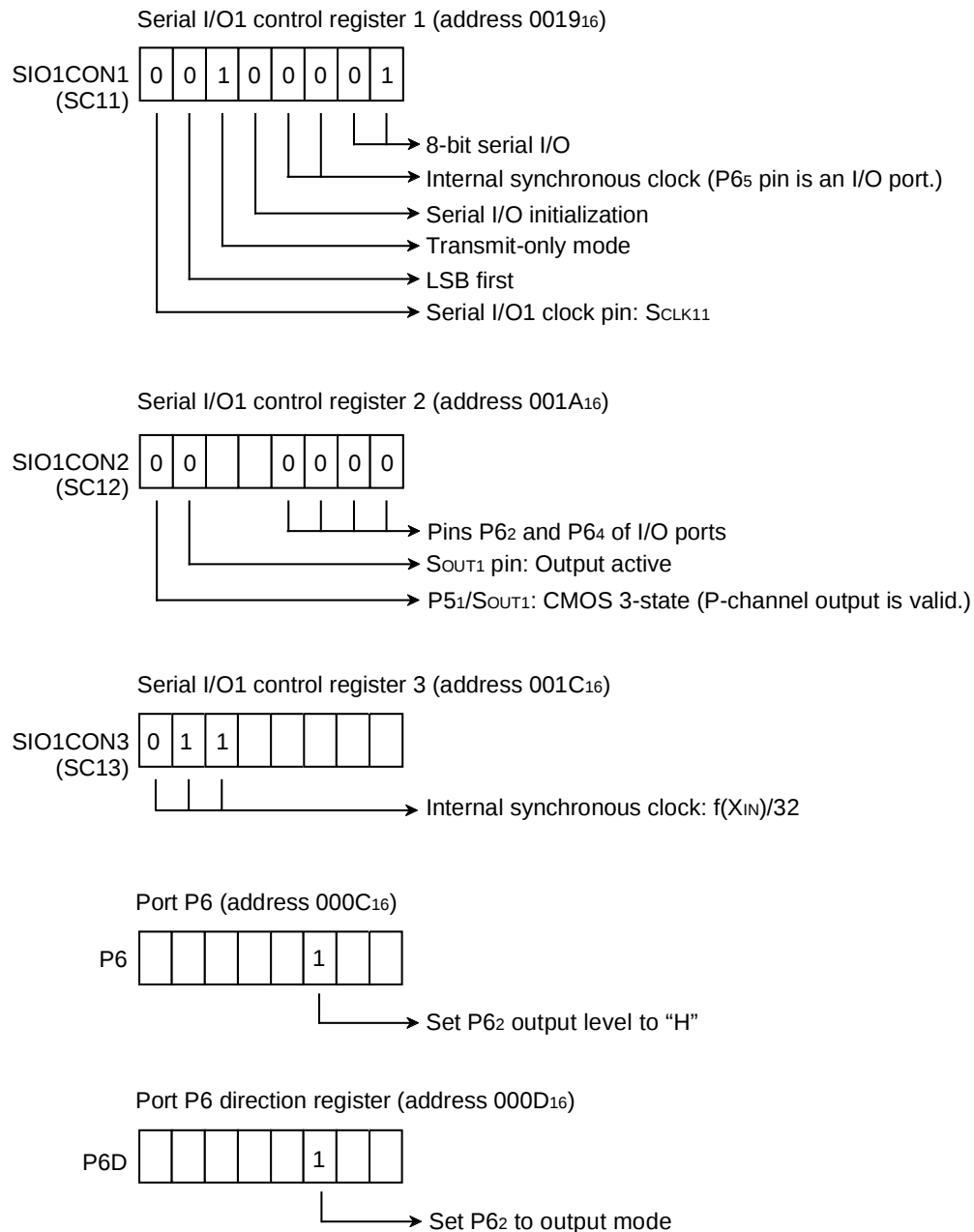


Fig. 2.3.22 Registers setting relevant to transmission side

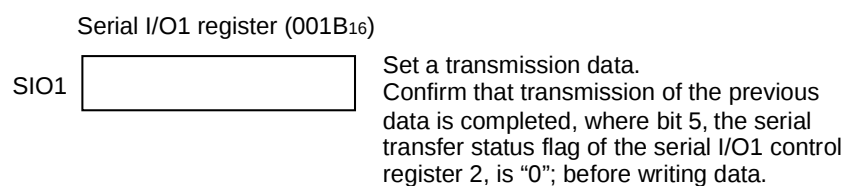


Fig. 2.3.23 Setting of transmission data

APPLICATION

2.3 Serial I/O

Control procedure: When the registers are set as shown in Figure 2.3.22, the serial I/O1 can transmit 1-byte data by writing data to the serial I/O1 register. Thus, after setting the $\overline{CS}$ signal to “L”, write the transmission data to the serial I/O1 register by each 1 byte; and return the $\overline{CS}$ signal to “H” when the target number of bytes has been transmitted. Figure 2.3.24 shows a control procedure.

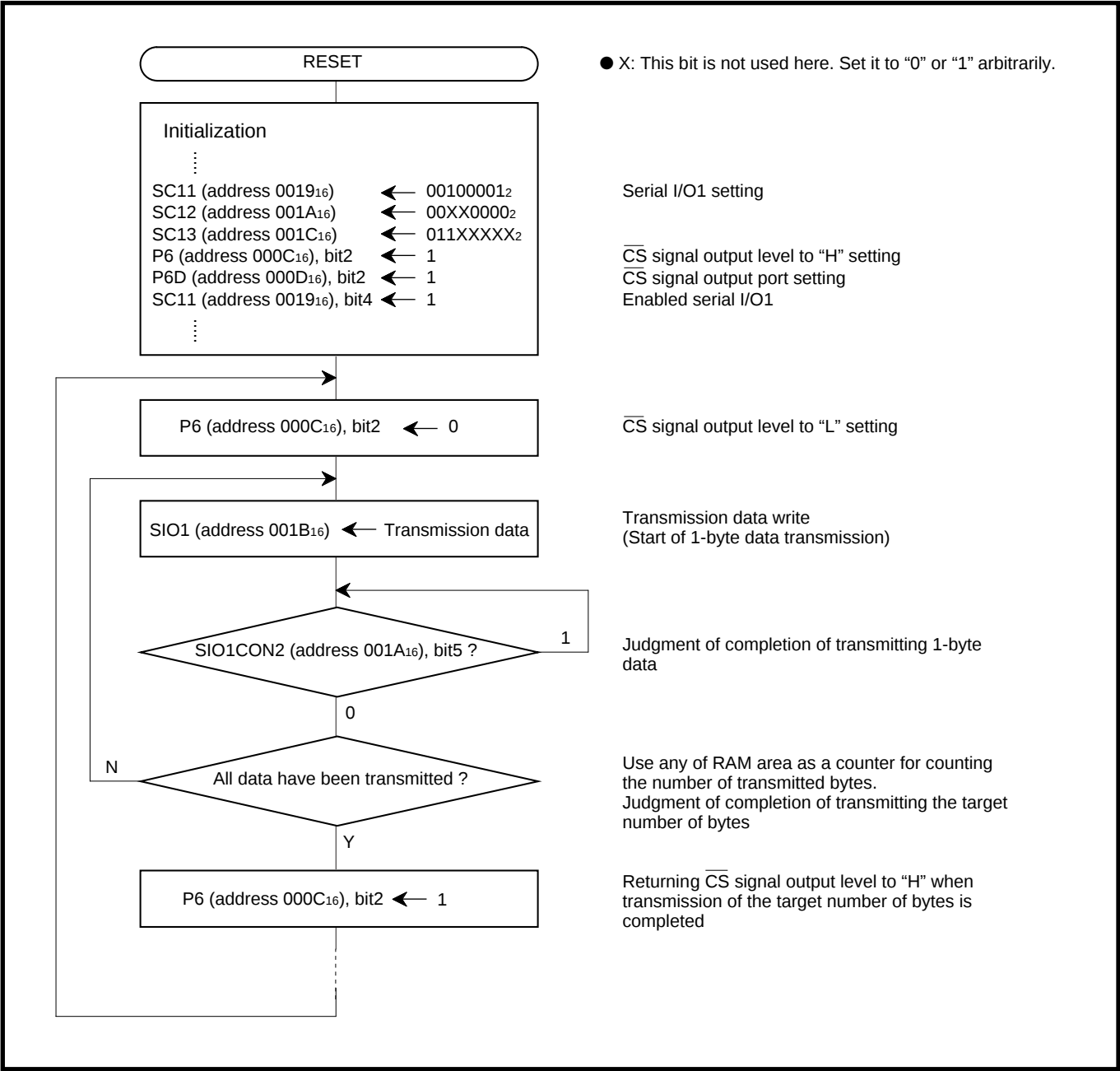


Fig. 2.3.24 Control procedure

(2) Transmission/Reception using automatic transfer

Outline: Serial transmission/reception control is performed, using the serial automatic transfer function.

Figure 2.3.25 shows a connection diagram, and Figure 2.3.26 shows a timing chart of serial data transmission/reception.

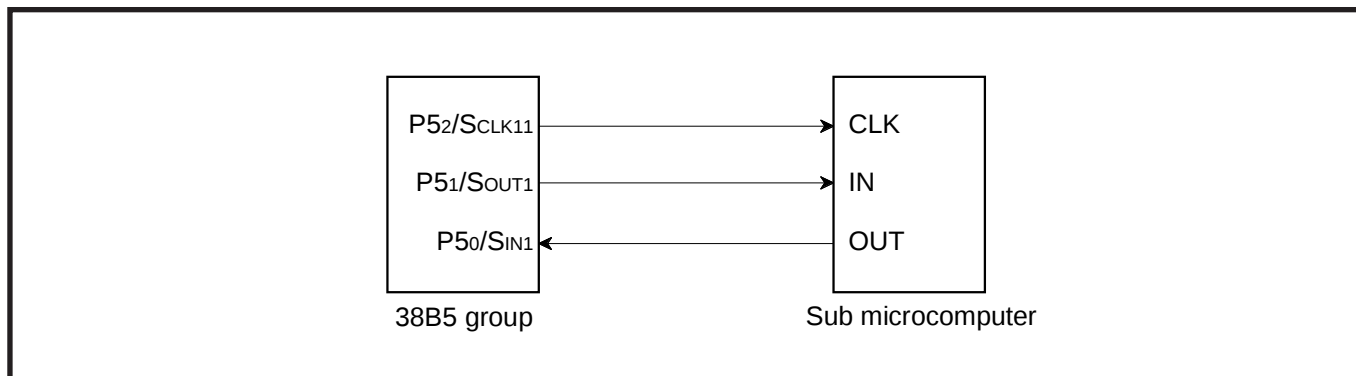


Fig. 2.3.25 Connection diagram

- Specifications:**
- Use of serial I/O1 using automatic transfer function
 - Synchronous clock frequency: 131 kHz ($f(X_{IN}) = 4.19 \text{ MHz}$ is divided by 32.)
 - Transfer direction: LSB first
 - Transmission/reception byte number: 8 bytes/block each
 - Transfer interval for 1-byte: $244 \mu\text{s}$ (32 cycles of transfer clock)
 - Not use of serial I/O1 automatic transfer interrupt

Figure 2.3.27 shows the relevant registers setting, and Figure 2.3.28 shows the control procedure.

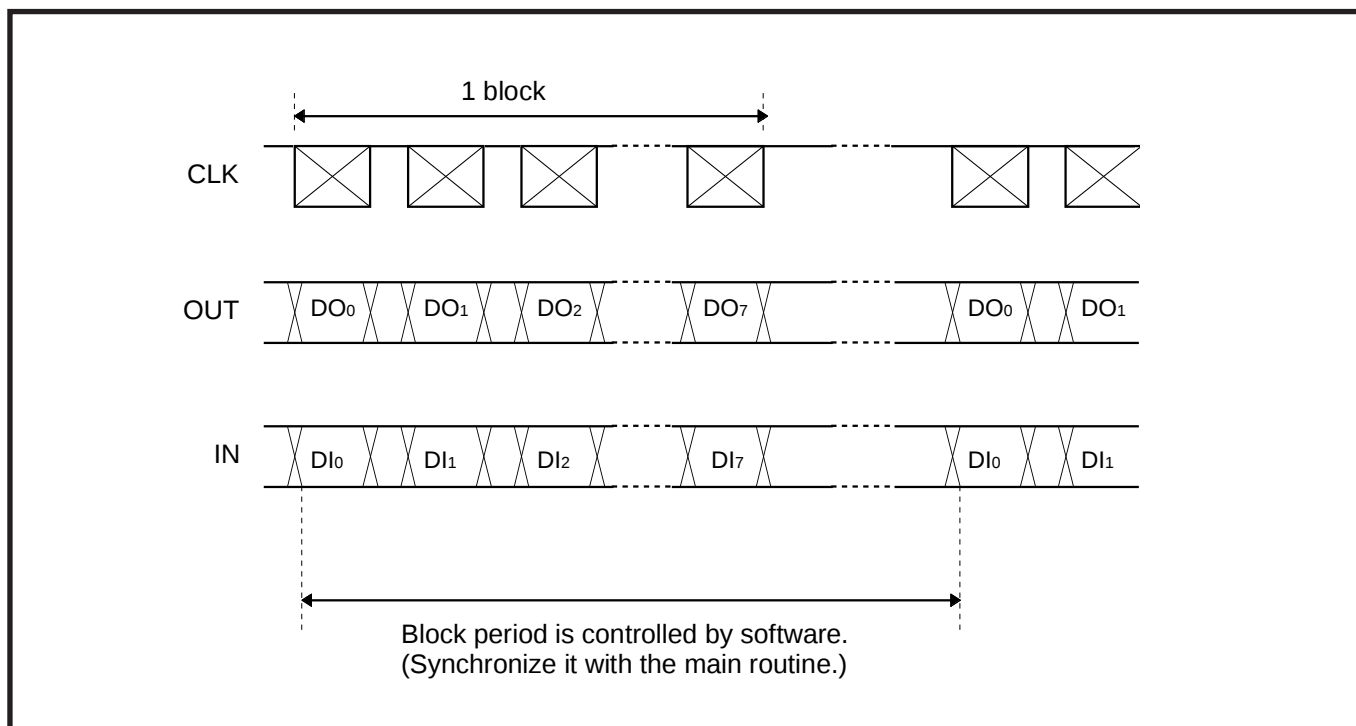


Fig. 2.3.26 Timing chart of serial data transmission/reception

APPLICATION

2.3 Serial I/O

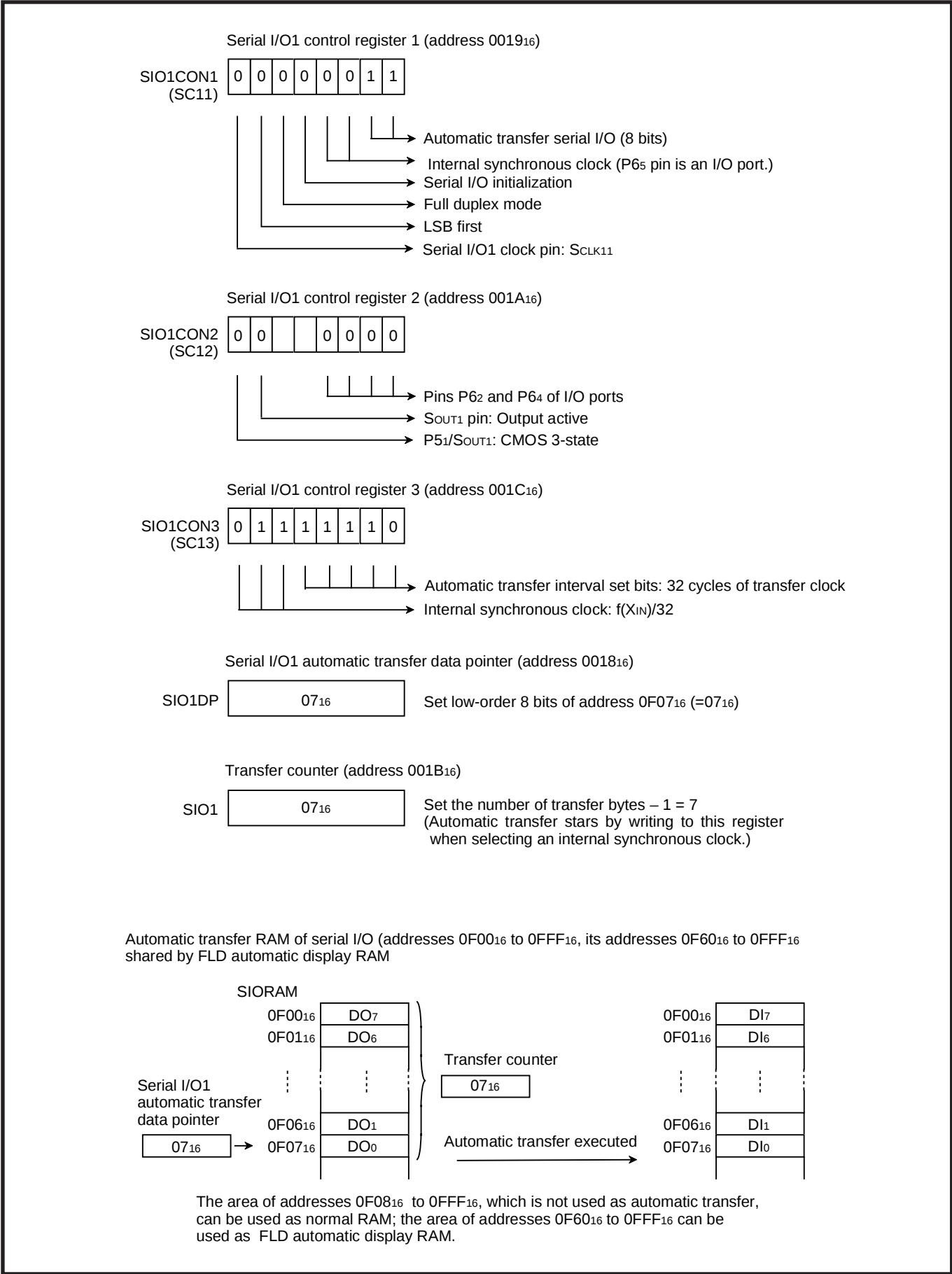


Fig. 2.3.27 Relevant registers setting

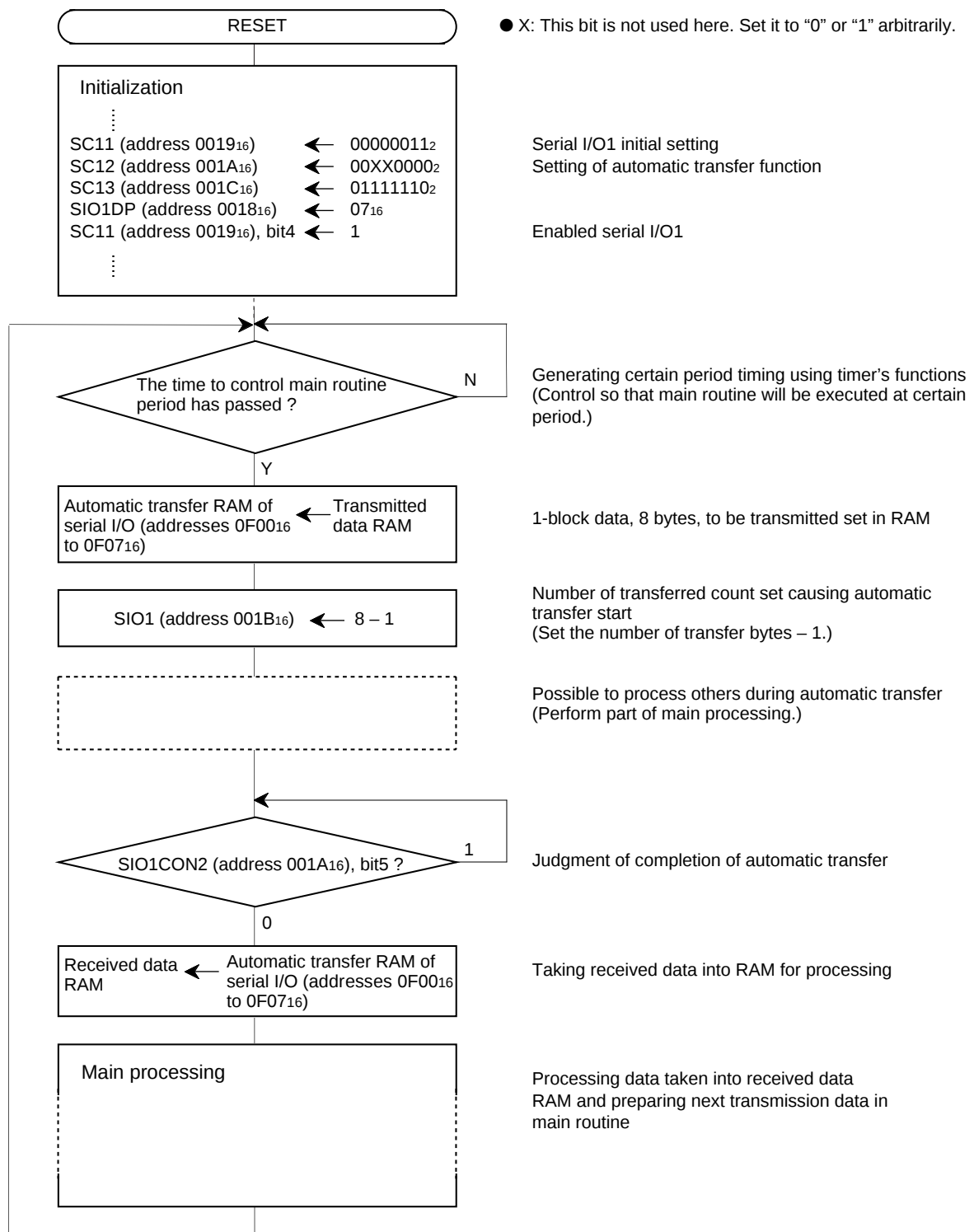


Fig. 2.3.28 Control procedure

(2) Connection with microcomputer

Figure 2.3.30 shows connection examples with another microcomputer.

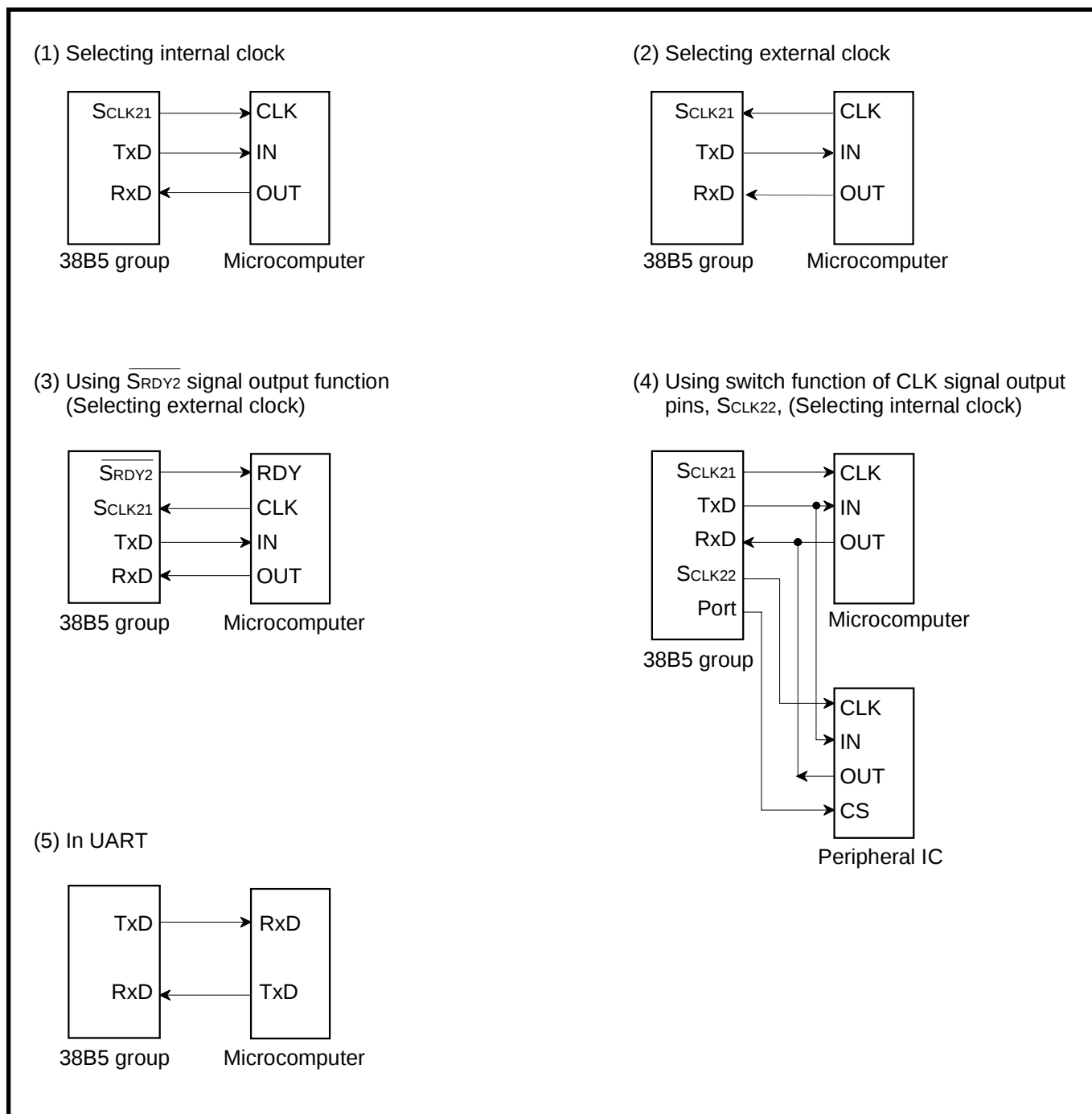


Fig. 2.3.30 Serial I/O2 connection examples (2)

APPLICATION

2.3 Serial I/O

2.3.7 Serial I/O2's modes

A clock synchronous or clock asynchronous (UART) can be selected for the serial I/O2.
Figure 2.3.31 shows the serial I/O2's modes, and Figure 2.3.32 shows the serial I/O2 transfer data format.

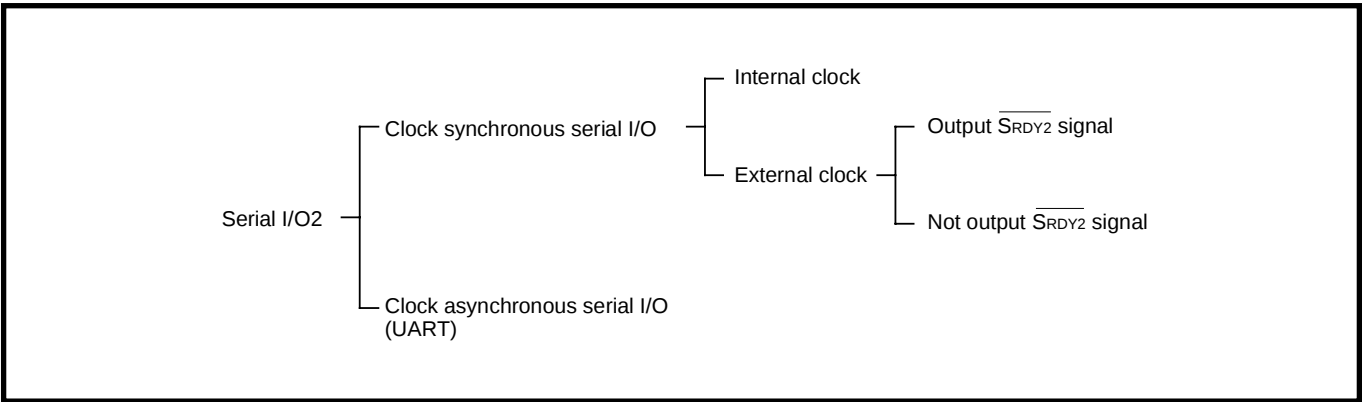


Fig. 2.3.31 Serial I/O2's modes

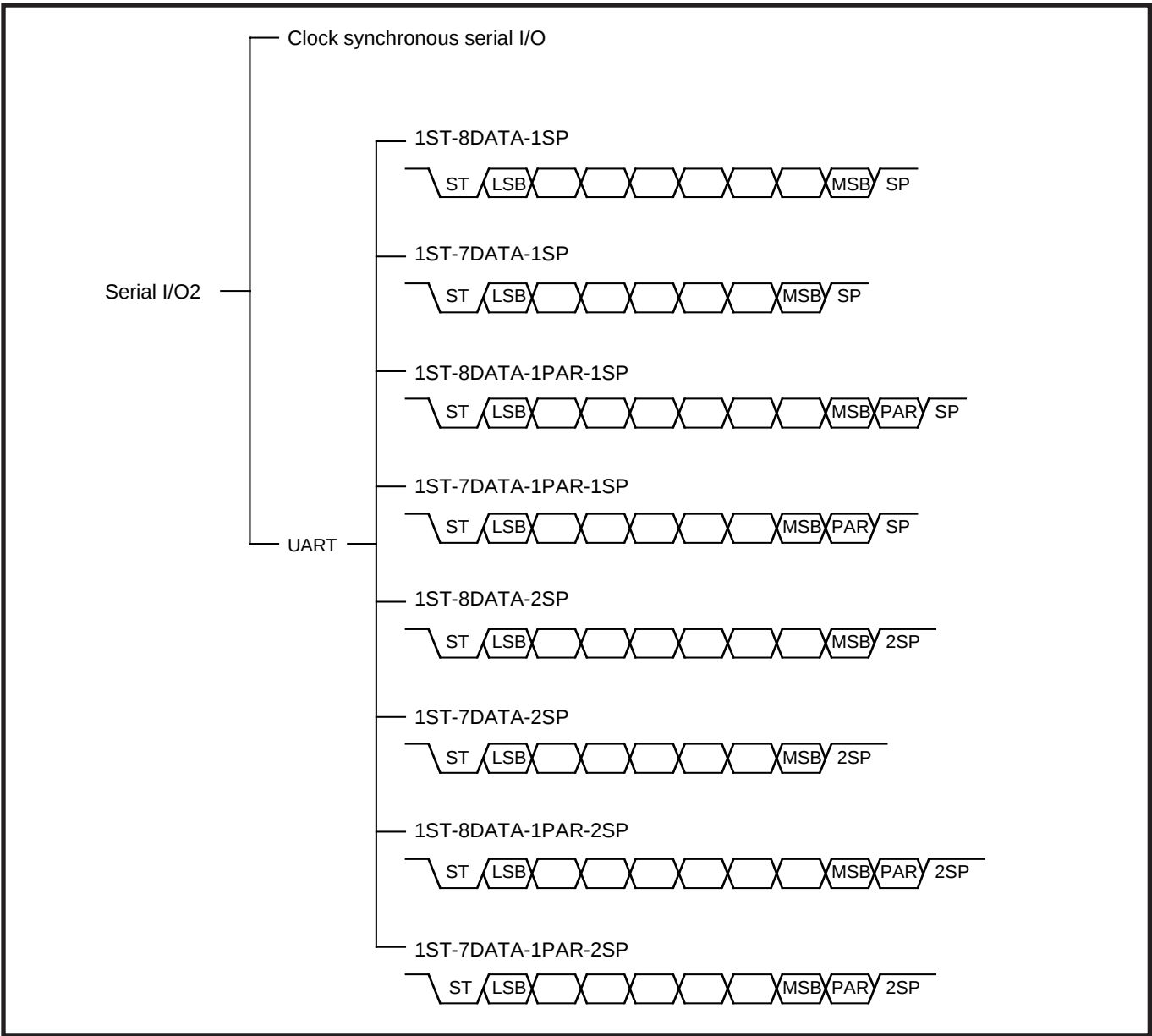


Fig. 2.3.32 Serial I/O2 transfer data format

2.3.8 Serial I/O2 application examples

(1) Communication (transmission/reception) using clock synchronous serial I/O

Outline : 2-byte data is transmitted and received, using the clock synchronous serial I/O.
The $\overline{\text{SRDY2}}$ signal is used for communication control.

Figure 2.3.33 shows a connection diagram, and Figure 2.3.34 shows a timing chart.

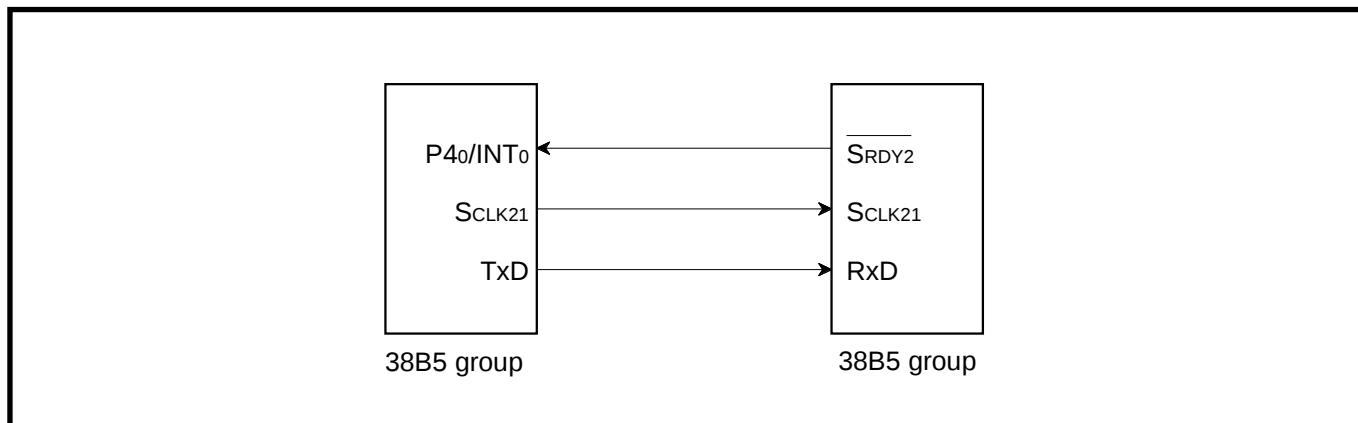


Fig. 2.3.33 Connection diagram

Specifications : • Use of serial I/O2 in clock synchronous serial I/O

- Synchronous clock frequency : 125 kHz ($f(X_{IN}) = 4 \text{ MHz}$ is divided by 32)
- Use of $\overline{\text{SRDY2}}$ (receivable signal)
- The reception side outputs the $\overline{\text{SRDY2}}$ signal at intervals of 2 ms (generated by the timer), and 2-byte data is transferred from the transmission side to the reception side.

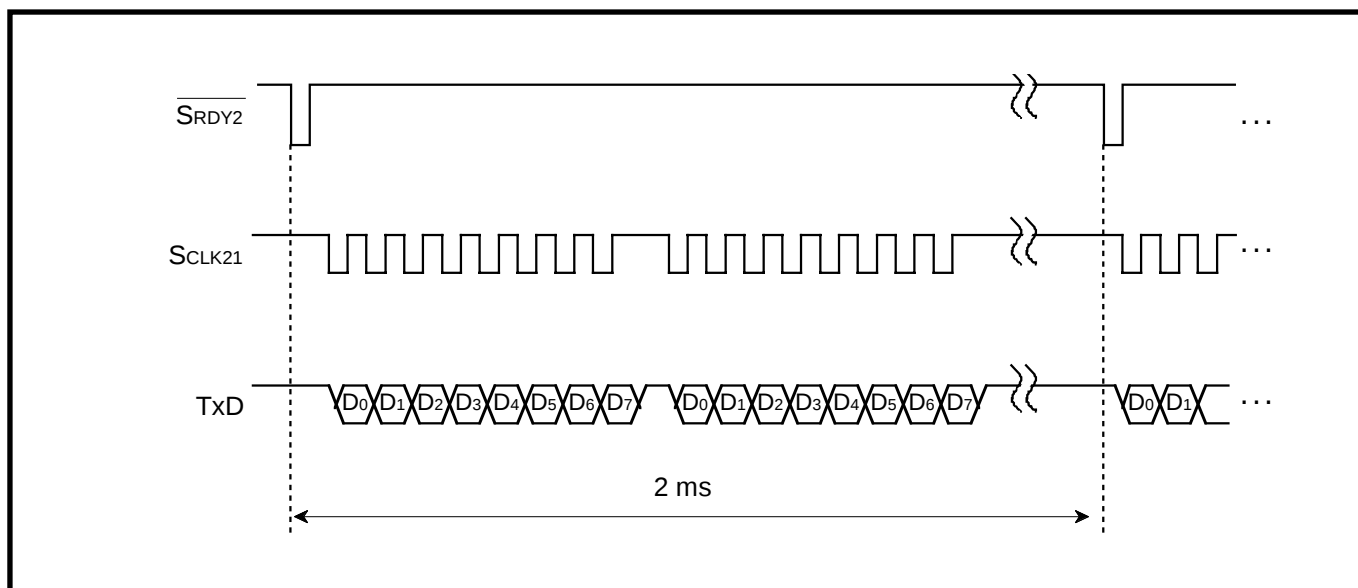


Fig. 2.3.34 Timing chart

APPLICATION

2.3 Serial I/O

Figure 2.3.35 shows the registers setting relevant to the transmission side, and Figure 2.3.36 shows the registers setting relevant to the reception side.

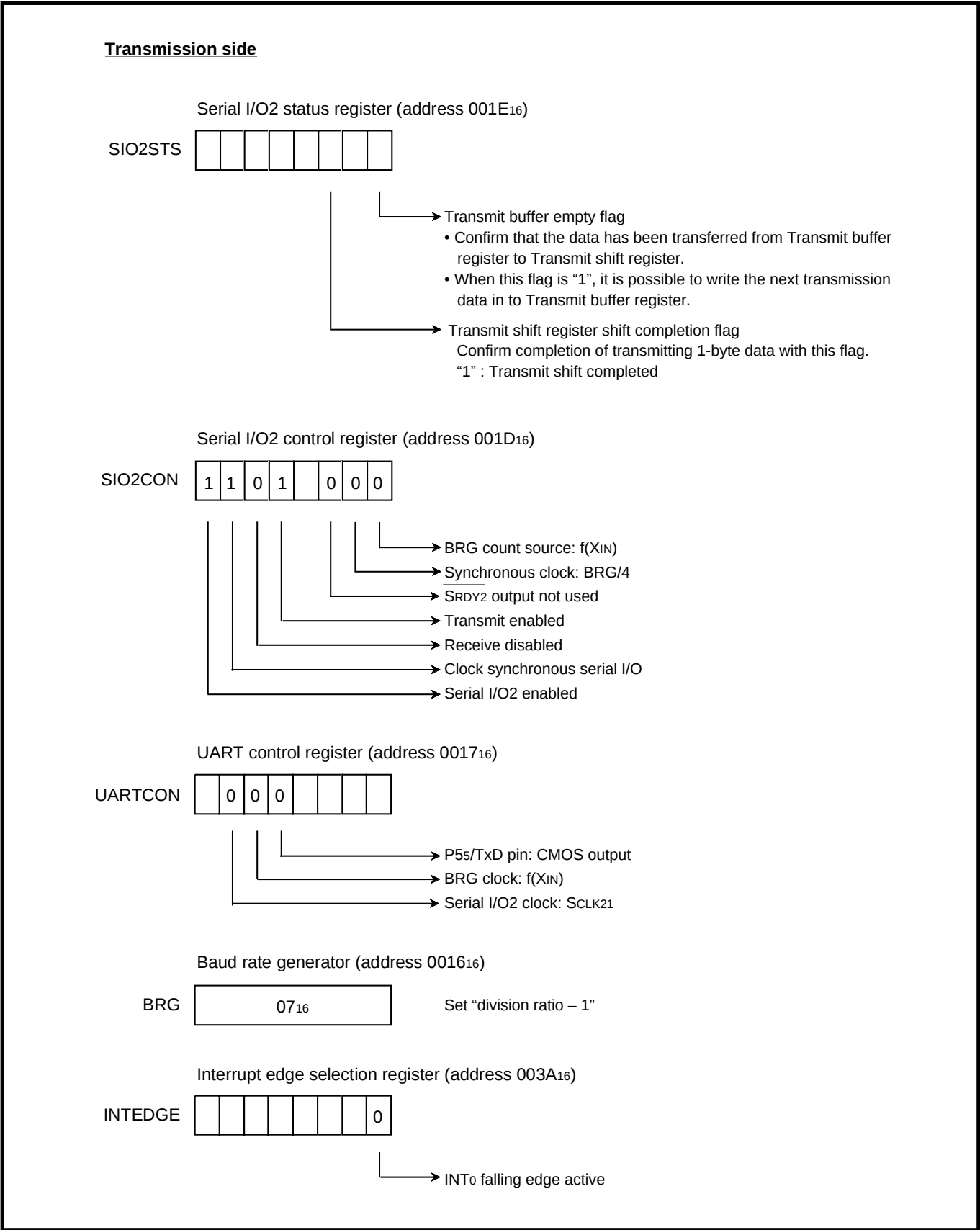


Fig. 2.3.35 Registers setting relevant to transmission side

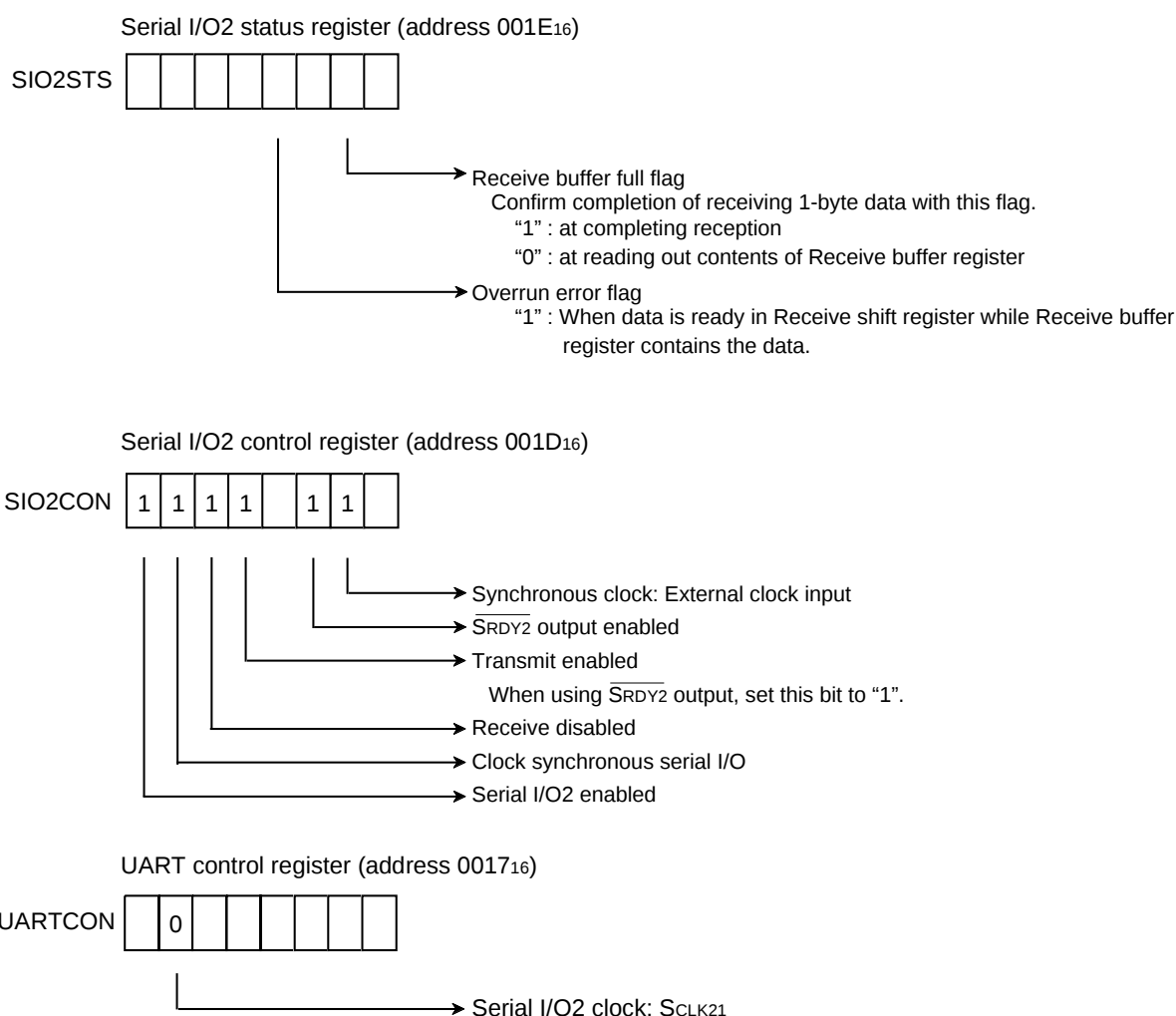
Reception side

Fig. 2.3.36 Registers setting relevant to reception side

APPLICATION

2.3 Serial I/O

Figure 2.3.37 shows a control procedure of the transmission side, and Figure 2.3.38 shows a control procedure of the reception side.

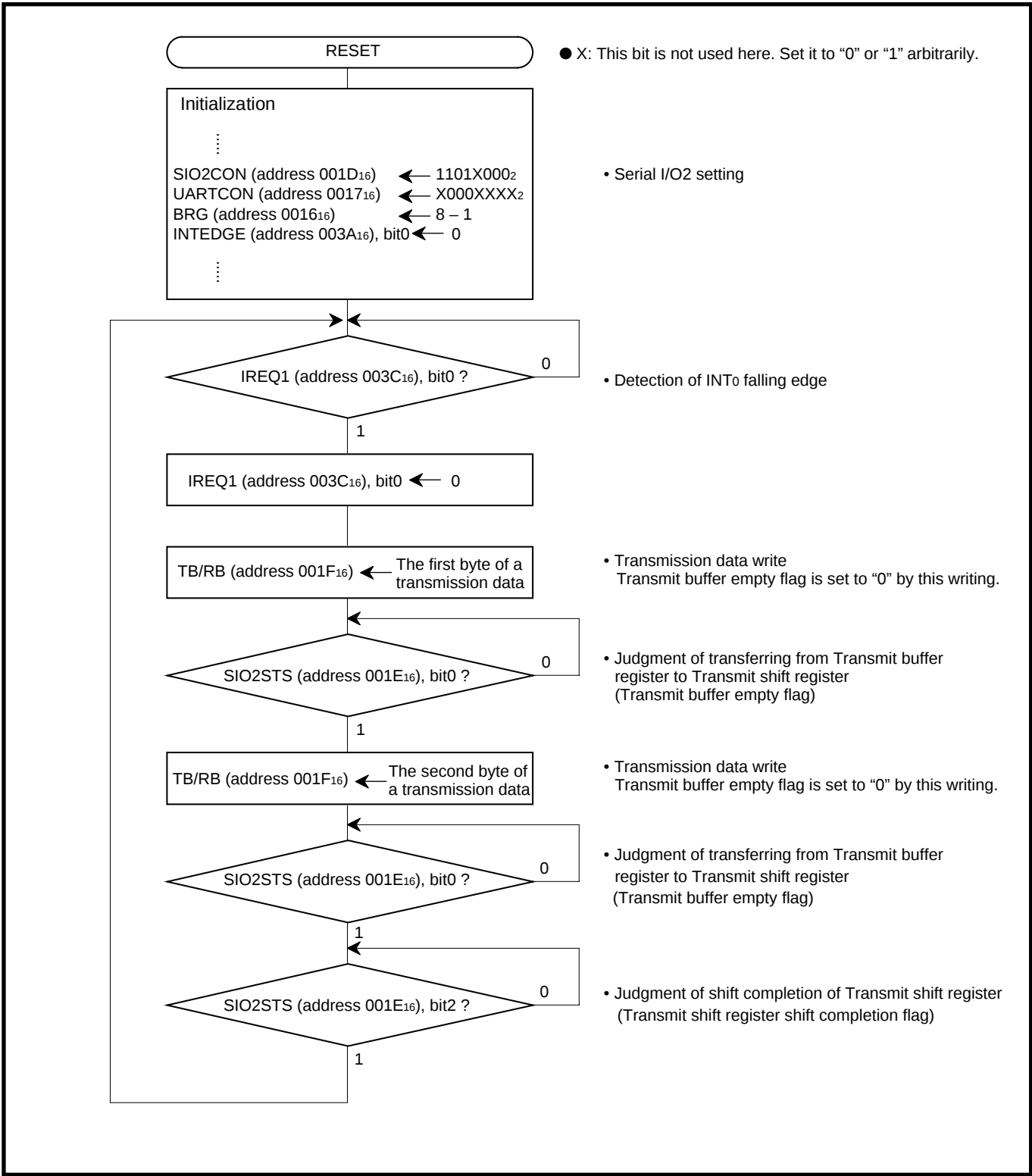


Fig. 2.3.37 Control procedure of transmission side

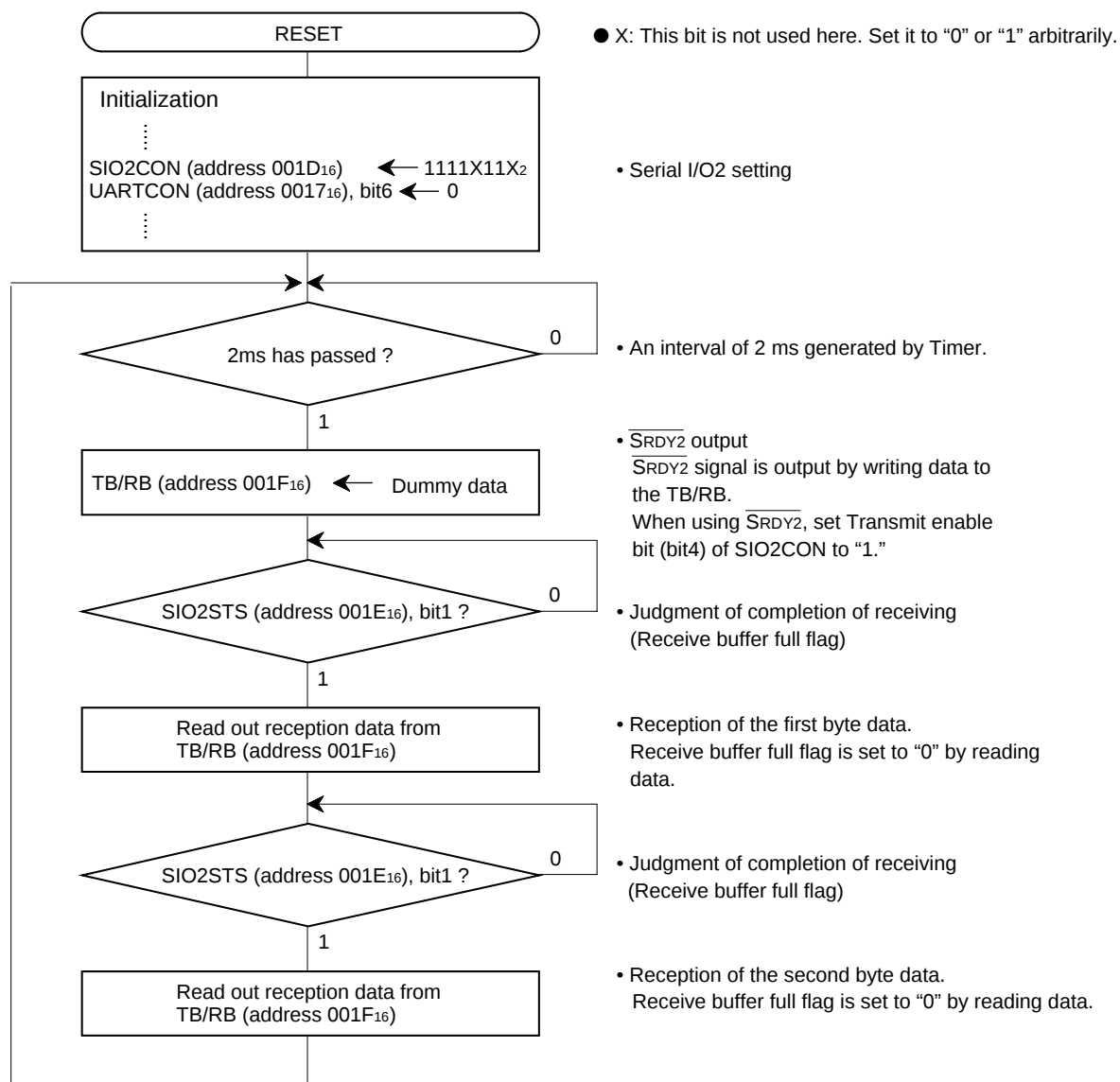


Fig. 2.3.38 Control procedure of reception side

APPLICATION

2.3 Serial I/O

(2) Output of serial data (control of peripheral IC)

Outline : Serial communication is performed, connecting port P5₇ with the $\overline{\text{CS}}$ pin of a peripheral IC.

Figure 2.3.39 shows a connection diagram, and Figure 2.3.40 shows a timing chart.

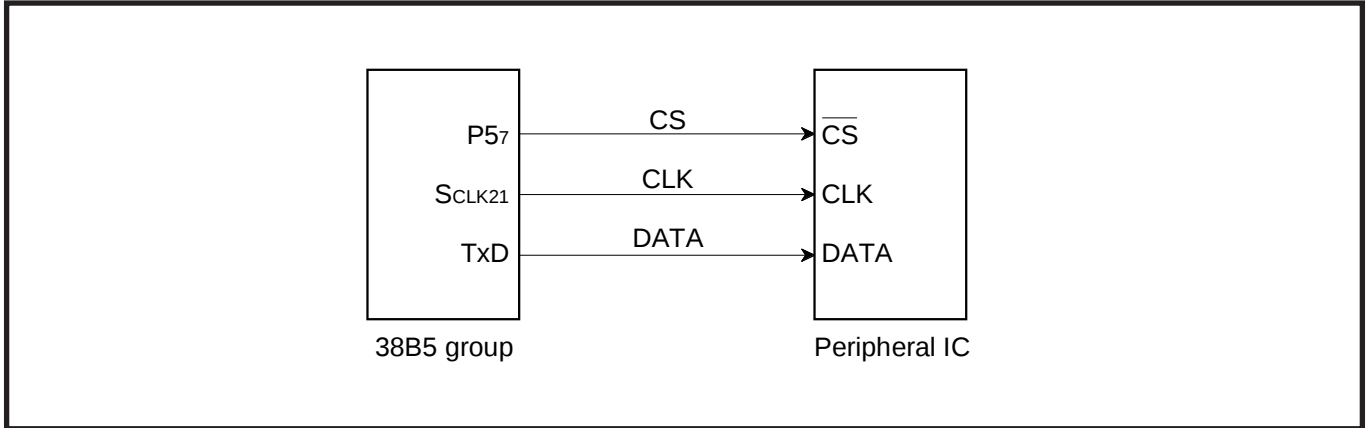


Fig. 2.3.39 Connection diagram

- Specifications :**
- Use of serial I/O2 in clock synchronous serial I/O
 - Synchronous clock frequency : 125 kHz ($f(X_{IN}) = 4 \text{ MHz}$ is divided by 32)
 - Transfer direction : LSB first
 - Not use of receive/transmit interrupts of serial I/O2
 - Port P5₇ is connected with the CS pin ("L" active) of the peripheral IC for transmission control; the output level of port P5₇ is controlled by software.

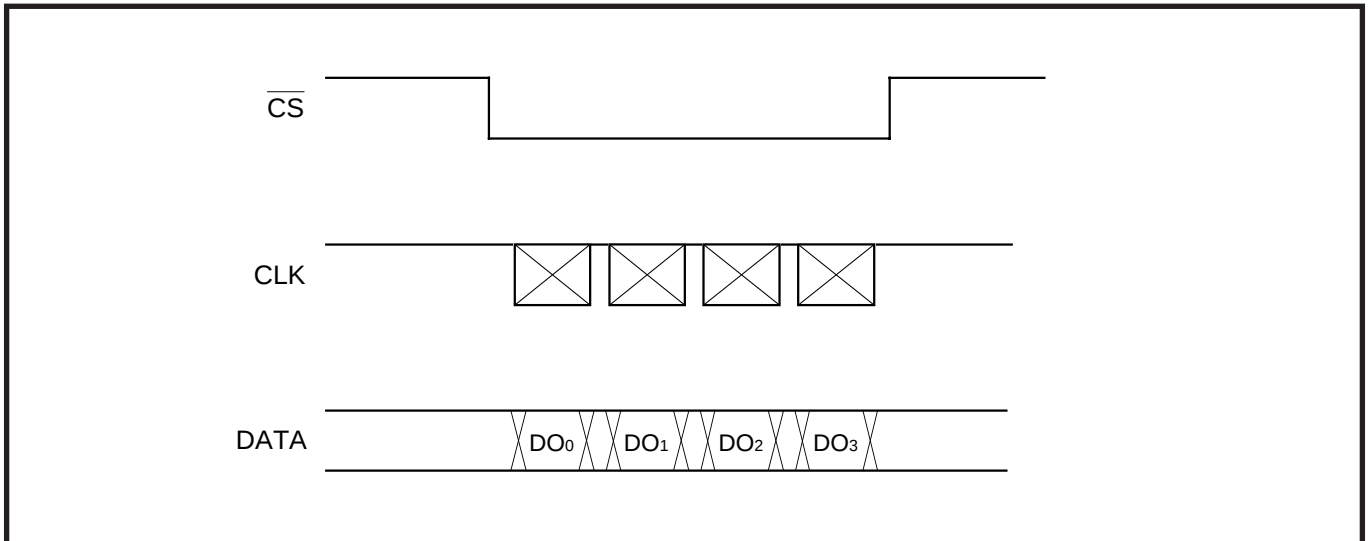


Fig. 2.3.40 Timing chart

Figure 2.3.41 shows the relevant registers setting and Figure 2.3.42 shows the setting of transmission data.

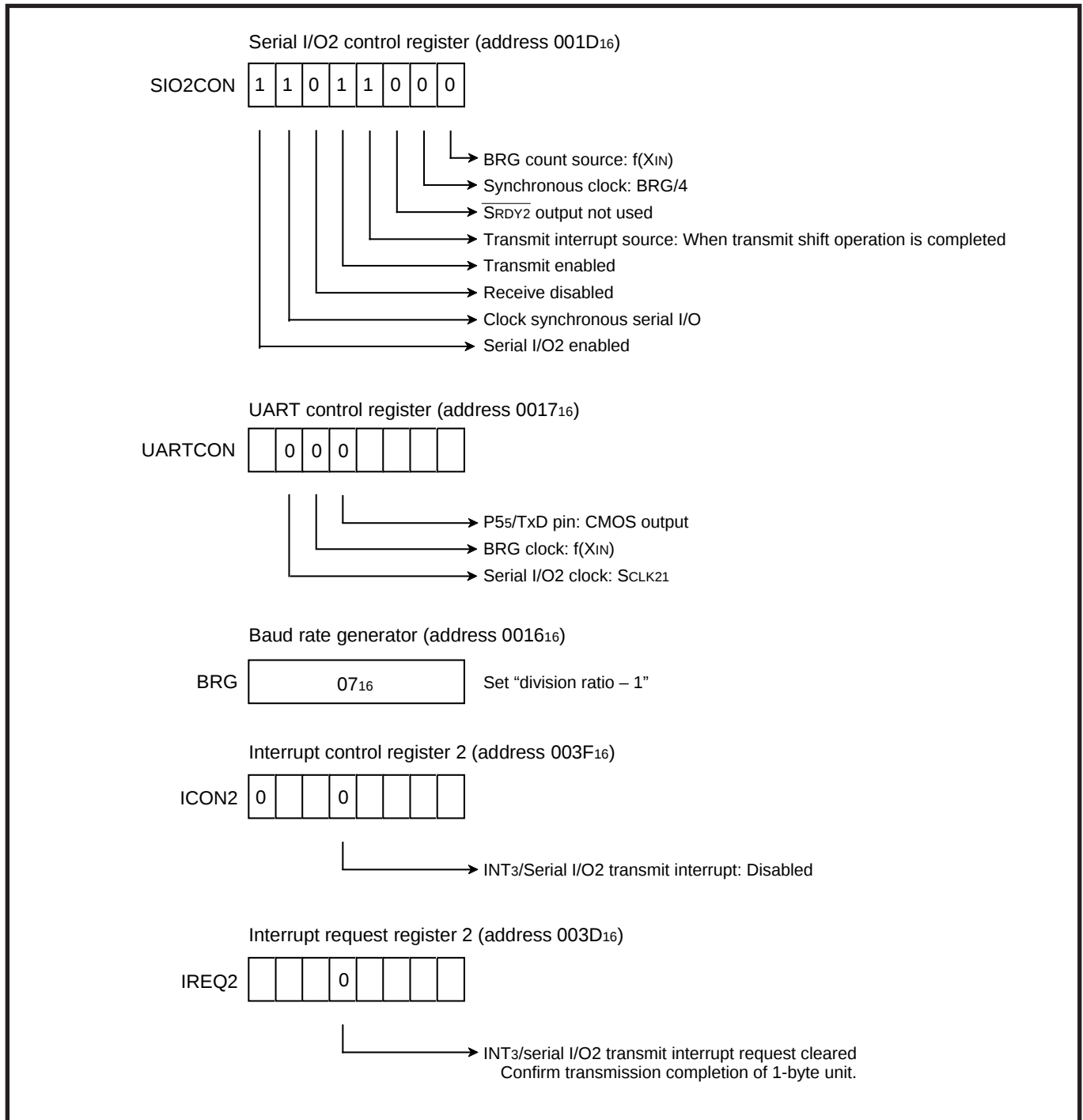


Fig. 2.3.41 Relevant registers setting

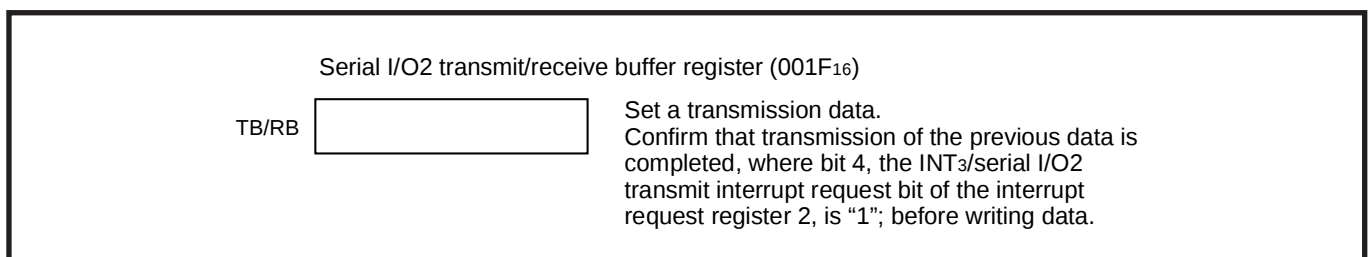


Fig. 2.3.42 Setting of transmission data

APPLICATION

2.3 Serial I/O

Figure 2.3.43 shows a control procedure.

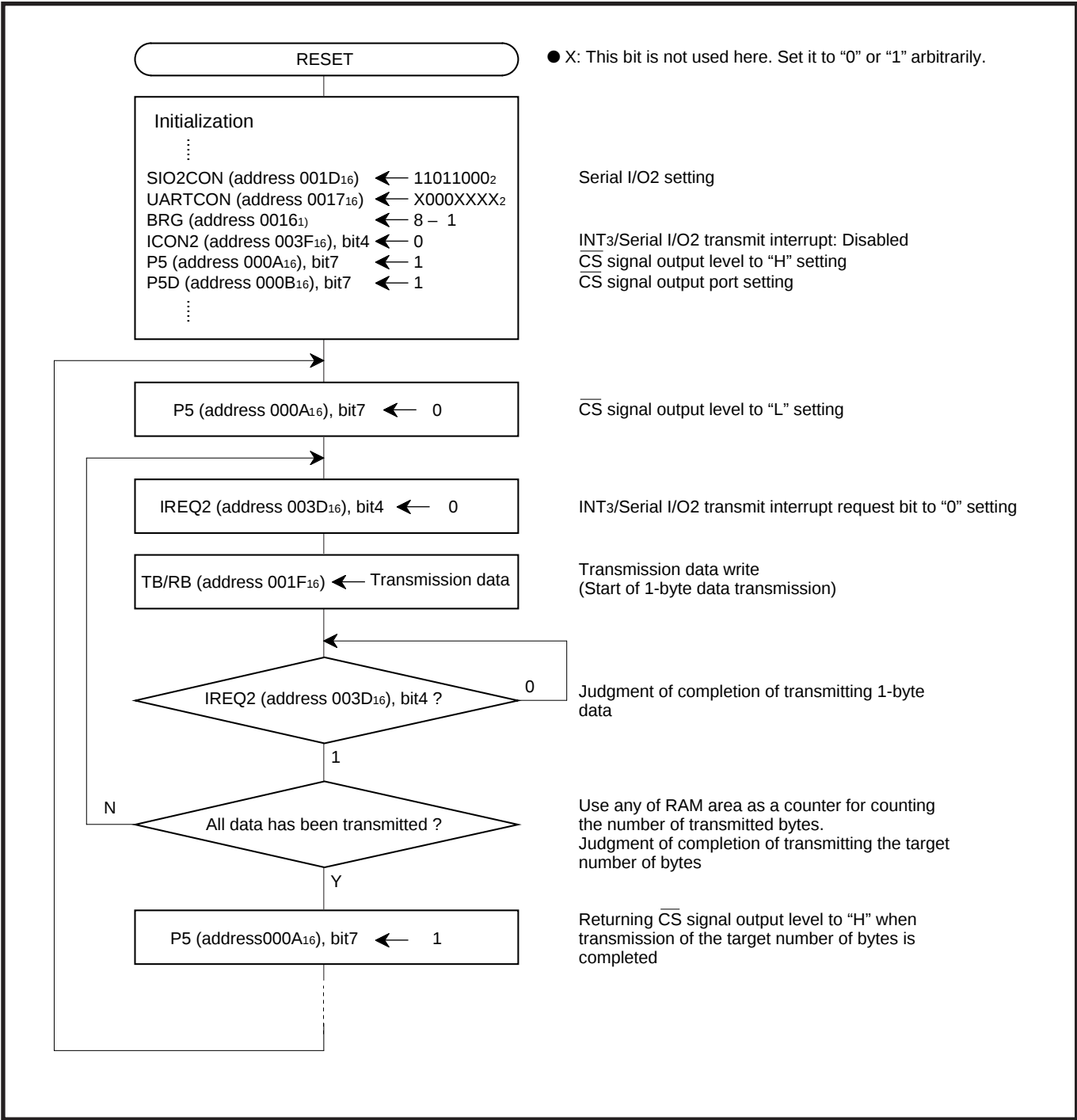


Fig. 2.3.43 Control procedure

(3) Cyclic transmission or reception of block data (data of specified number of bytes) between two microcomputers

Outline : When the clock synchronous serial I/O is used for communication, synchronization of the clock and the data between the transmitting and receiving sides may be lost because of noise included in the synchronous clock. It is necessary to correct that constantly, using “heading adjustment”.

This “heading adjustment” is carried out by using the interval between blocks in this example.

Figure 2.3.44 shows a connection diagram.

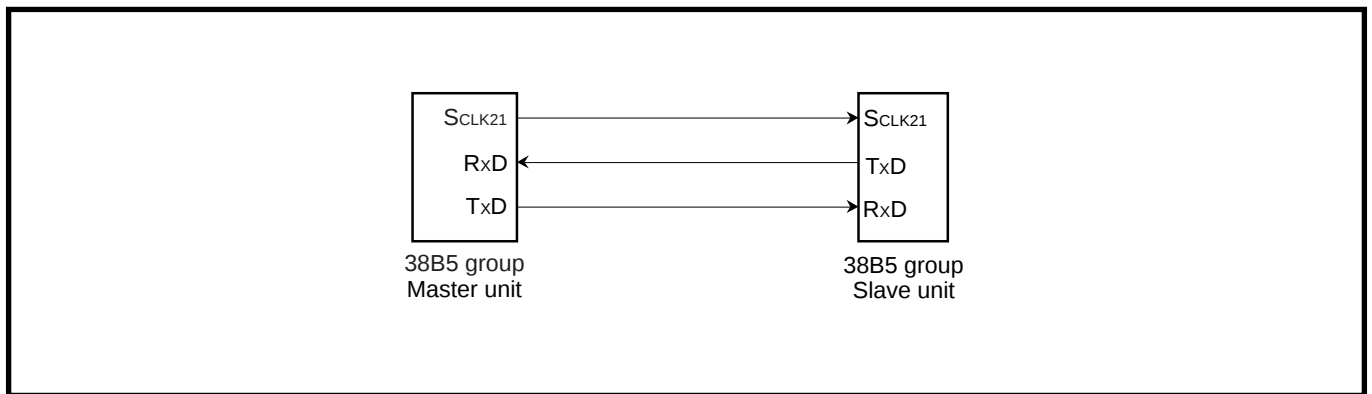


Fig. 2.3.44 Connection diagram

- Specifications:**
- Use of serial I/O2 in clock synchronous serial I/O
 - Synchronous clock frequency : 131 kHz ($f(X_{IN}) = 4.19 \text{ MHz}$ is divided by 32.)
 - Byte cycle: 488 μs
 - Number of bytes for transmission or reception : 8 bytes/block each
 - Block transfer cycle : 16 ms
 - Block transfer term : 3.5 ms
 - Interval between blocks : 12.5 ms
 - Heading adjustment time : 8 ms
 - Transfer direction : LSB first

Limitations of the specifications:

- Reading of the reception data and setting of the next transmission data must be completed within the time obtained from “byte cycle – time for transferring 1-byte data” (in this example, the time taken from generating of the serial I/O2 receive interrupt request to input of the next synchronous clock is 431 μs).
- “Heading adjustment time < interval between blocks” must be satisfied.

APPLICATION

2.3 Serial I/O

The communication is performed according to the timing shown in Figure 2.3.45. In the slave unit, when a synchronous clock is not input within a certain time (heading adjustment time), the next clock input is processed as the beginning (heading) of a block.

When a clock is input again after one block (8 bytes) is received, the clock is ignored.

Figure 2.3.46 shows the relevant registers setting in the master unit and Figure 2.3.47 shows the relevant registers setting in the slave unit.

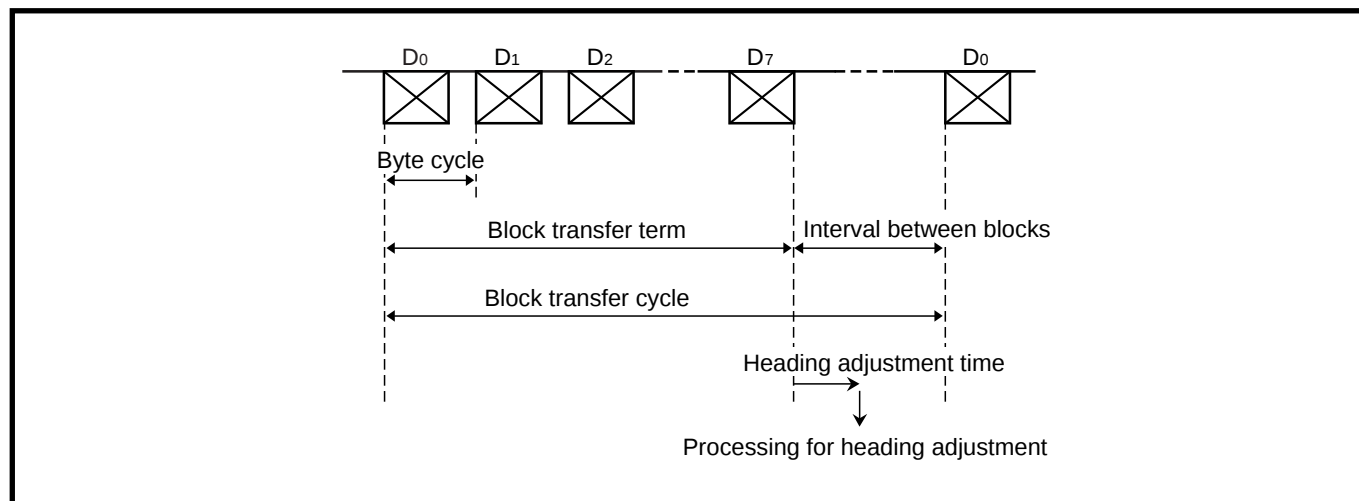


Fig. 2.3.45 Timing chart

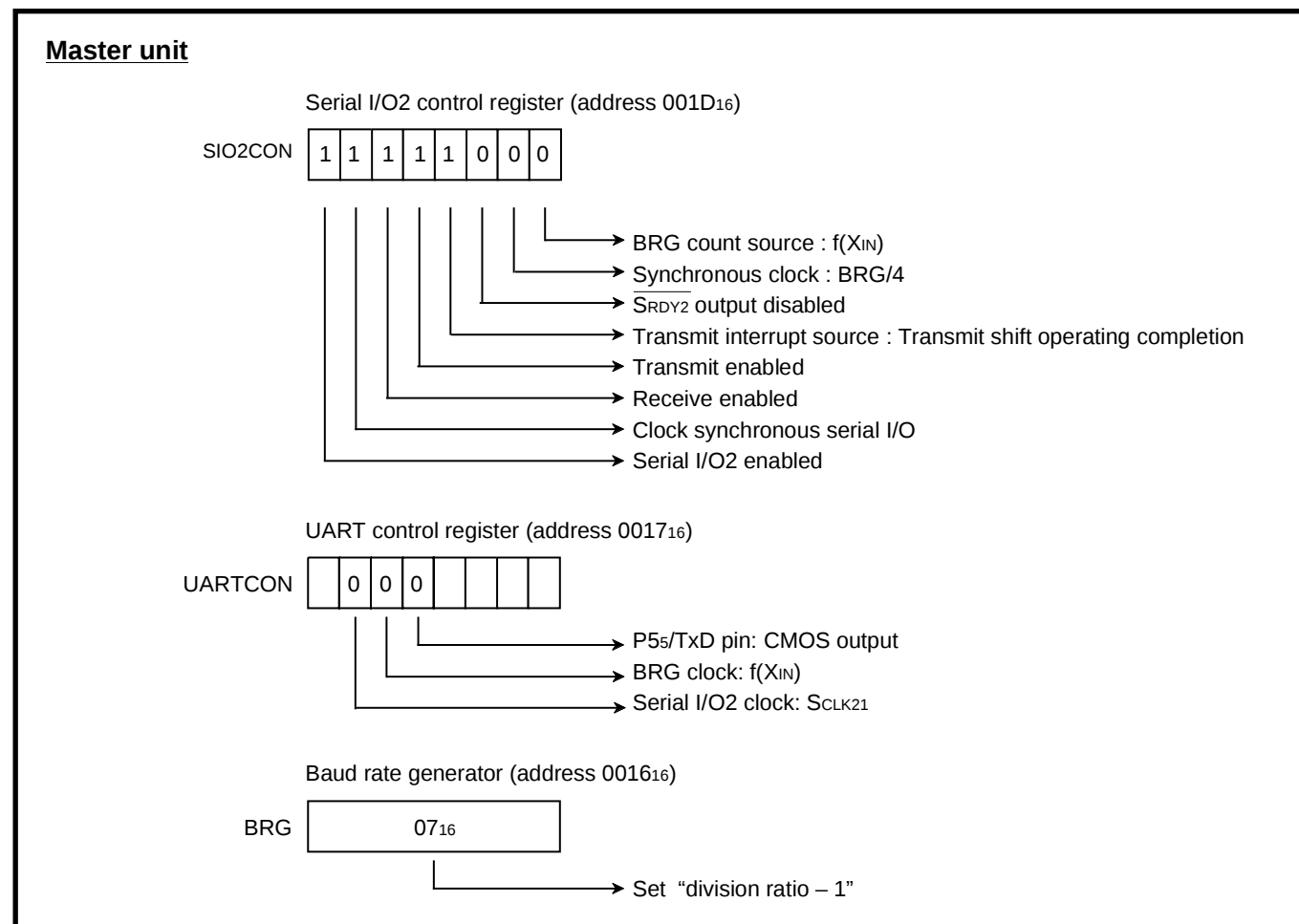


Fig. 2.3.46 Relevant registers setting in master unit

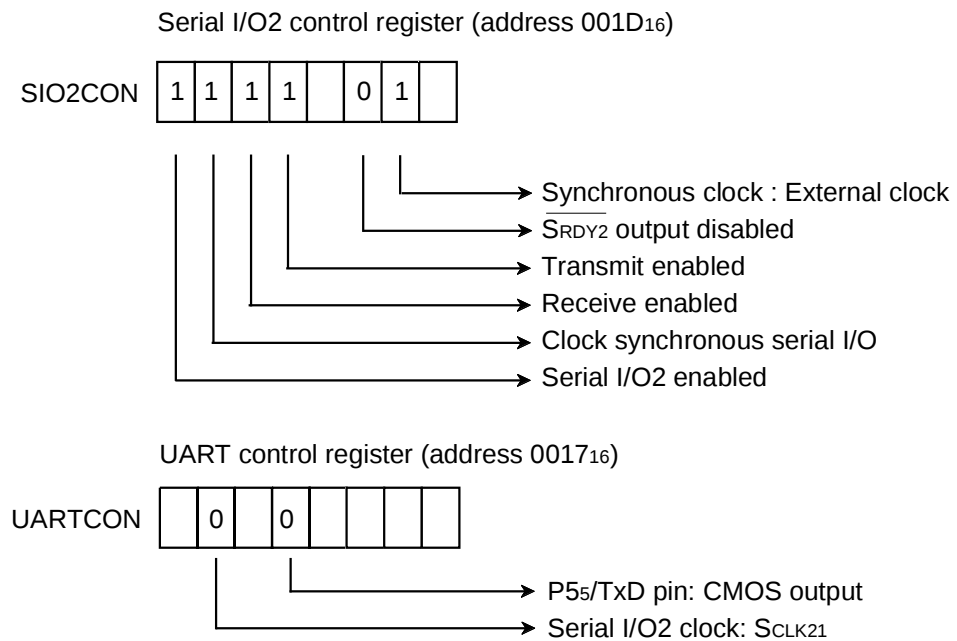
Slave unit

Fig. 2.3.47 Relevant registers setting in slave unit

APPLICATION

2.3 Serial I/O

Control procedure by software:

● Control in the master unit

After setting the relevant registers shown in Figure 2.3.46, the master unit starts transmission or reception of 1-byte data by writing transmission data to the serial I/O2 transmit buffer register. To perform the communication in the timing shown in Figure 2.3.45, take the timing into account and write transmission data. Additionally, read out the reception data when the serial I/O2 transmit interrupt request bit is set to "1," or before the next transmission data is written to the serial I/O2 transmit buffer register.

Figure 2.3.48 shows a control procedure of the master unit using timer interrupts.

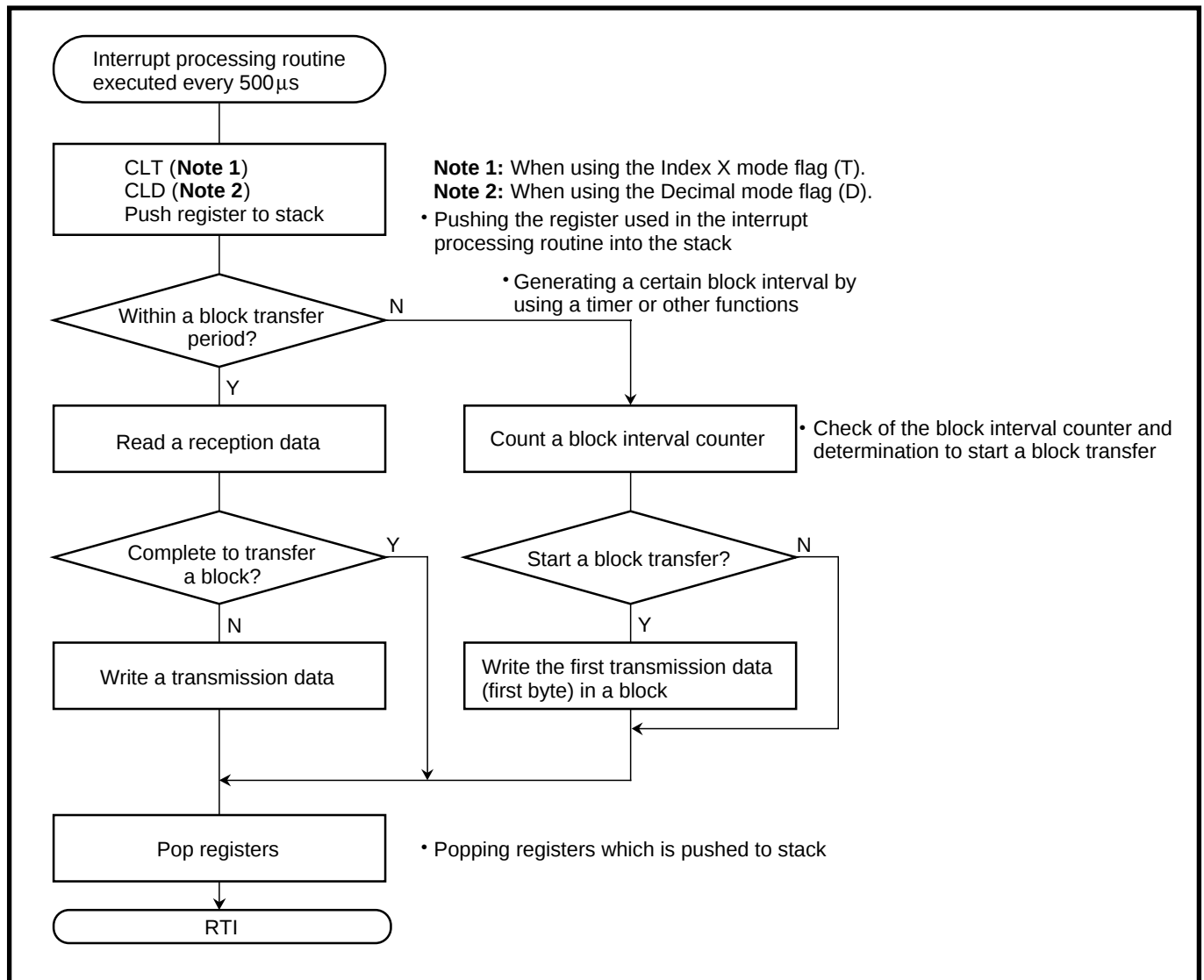


Fig. 2.3.48 Control procedure of master unit

● Control in the slave unit

After setting the relevant registers as shown in Figure 2.3.47, the slave unit becomes the state where a synchronous clock can be received at any time, and the serial I/O2 receive interrupt request bit is set to “1” each time an 8-bit synchronous clock is received.

In the serial I/O2 receive interrupt processing routine, the data to be transmitted next is written to the transmit buffer register after the received data is read out.

However, if no serial I/O2 receive interrupt occurs for a certain time (heading adjustment time or more), the following processing will be performed.

1. The first 1-byte data of the transmission data in the block is written into the transmit buffer register.
2. The data to be received next is processed as the first 1 byte of the received data in the block.

Figure 2.3.49 shows a control procedure of the slave unit using the serial I/O2 receive interrupt and any timer interrupt (for heading adjustment).

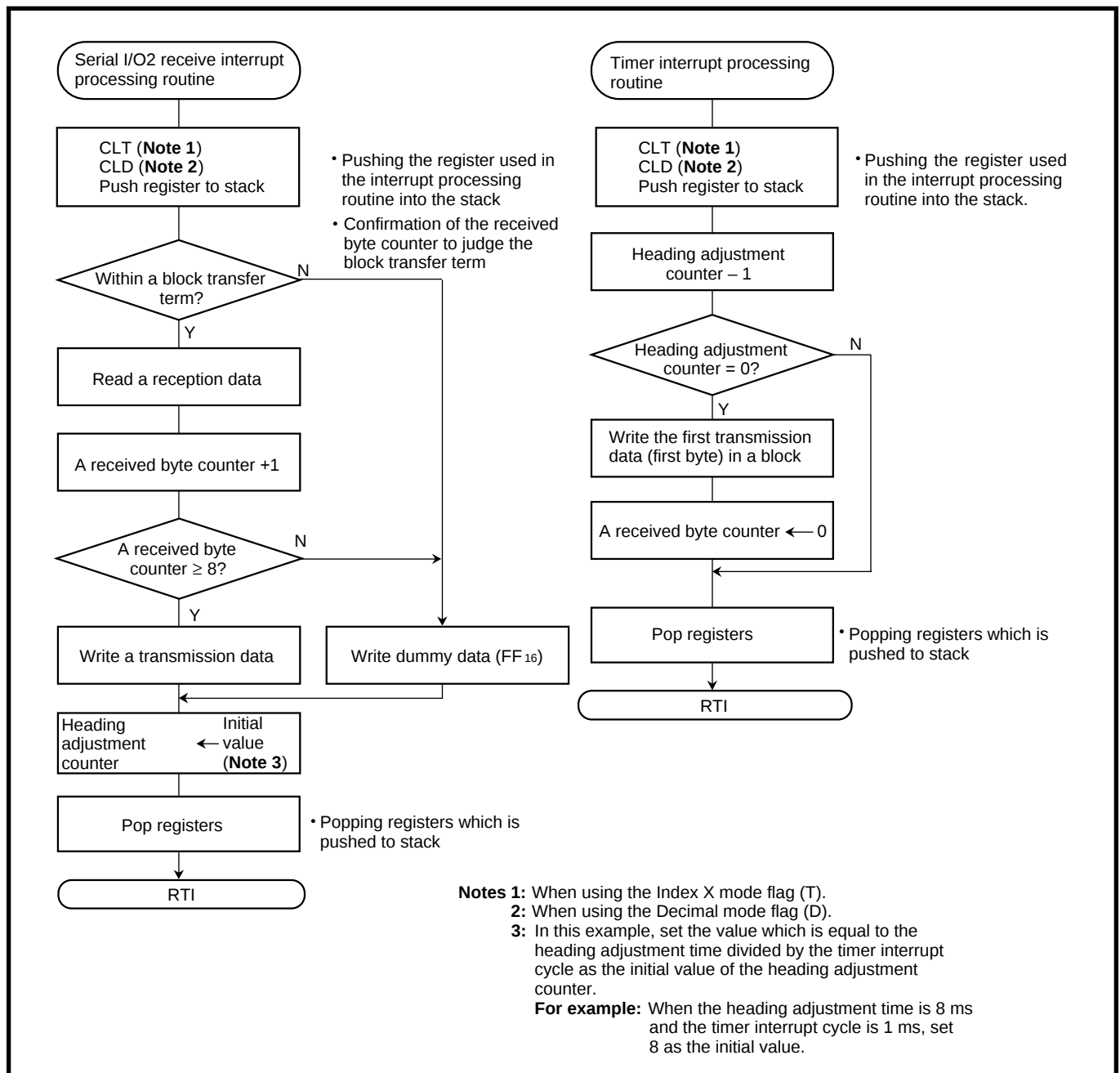


Fig. 2.3.49 Control procedure of slave unit

APPLICATION

2.3 Serial I/O

(4) Communication (transmission/reception) using asynchronous serial I/O (UART)

Outline : 2-byte data is transmitted and received, using the asynchronous serial I/O.
Port P5₆ is used for communication control.

Figure 2.3.50 shows a connection diagram, and Figure 2.3.51 shows a timing chart.

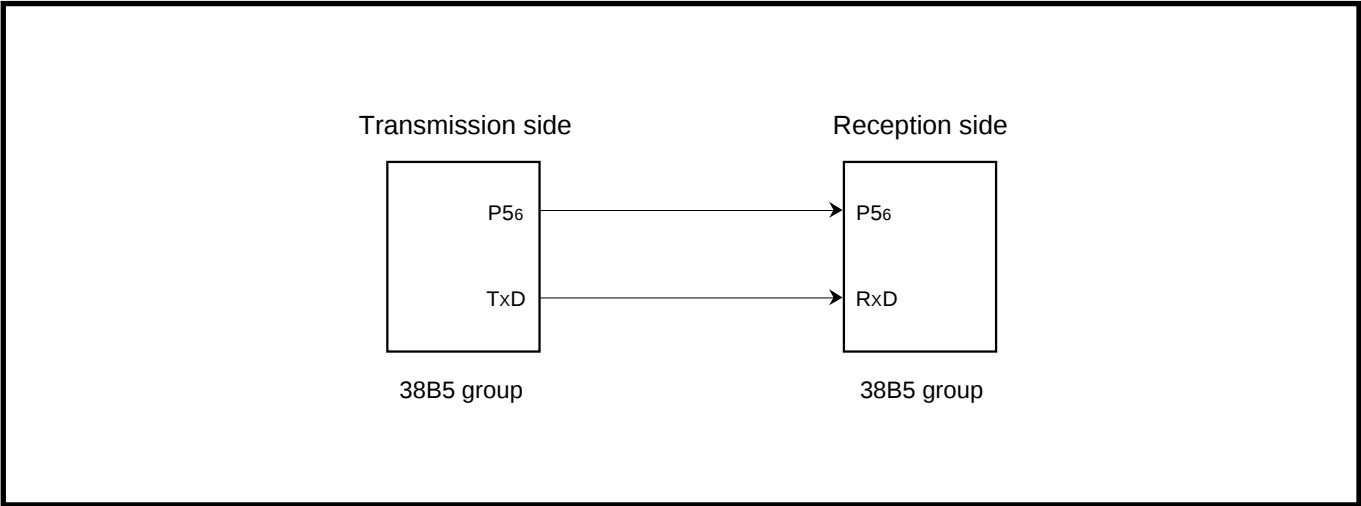


Fig. 2.3.50 Connection diagram

Specifications : • Use of serial I/O₂ in UART

- Transfer bit rate : 9600 bps ($f(X_{IN}) = 3.6864 \text{ MHz}$ is divided by 384)
- Data format : 1ST-8DADA-2ST
- Communication control using port P5₆
(The output level of port P5₆ is controlled by software.)
- 2-byte data is transferred from the transmission side to the reception side at intervals of 10 ms generated by the timer.

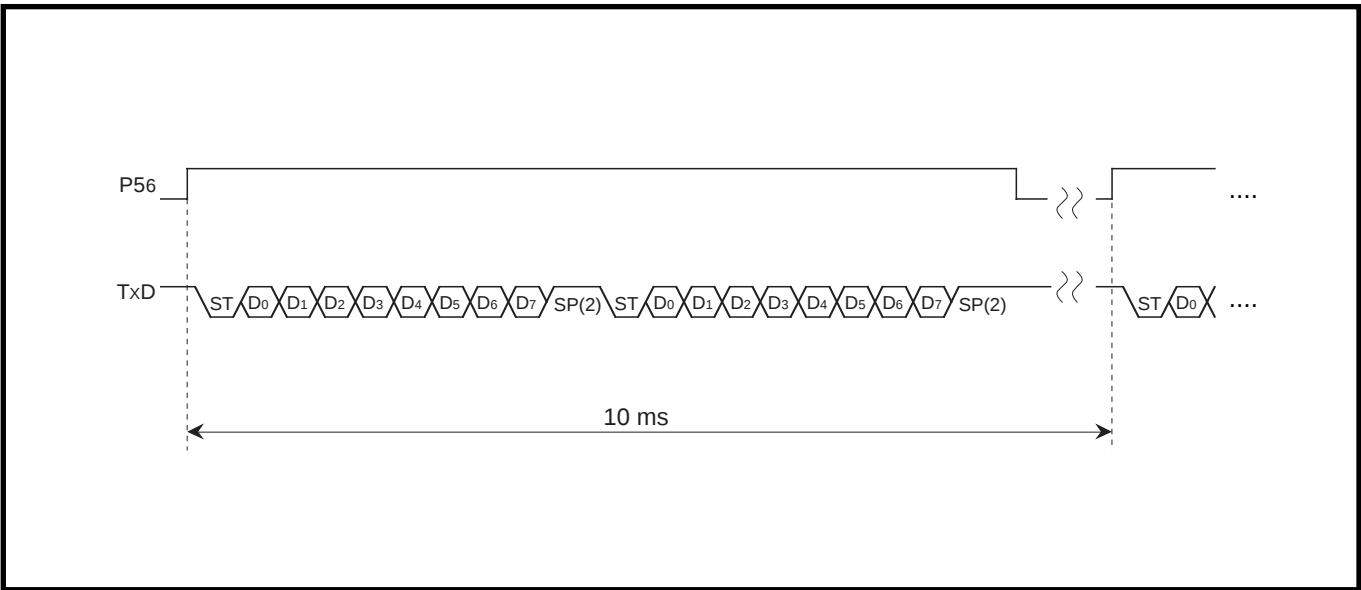


Fig. 2.3.51 Timing chart

Table 2.3.1 shows setting examples of the baud rate generator (BRG) values and transfer bit rate values.

Table 2.3.1 Setting examples of baud rate generator values and transfer bit rate values

Transfer bit rate (Note 1)	f(XIN) = 3.6864 MHz			f(XIN) = 4 MHz		
	BRG count source (Note 2)	BRG setting value	Actual rate	BRG count source (Note 2)	BRG setting value	Actual rate
600	f(XIN)/4	95(5F ₁₆)	600.00	f(XIN)/4	103(67 ₁₆)	600.96
1200	f(XIN)/4	47(2F ₁₆)	1200.00	f(XIN)/4	51(33 ₁₆)	1201.92
2400	f(XIN)/4	23(17 ₁₆)	2400.00	f(XIN)/4	25(19 ₁₆)	2403.85
4800	f(XIN)/4	11(0B ₁₆)	4800.00	f(XIN)/4	12(0C ₁₆)	4807.69
9600	f(XIN)/4	5(05 ₁₆)	9600.00	f(XIN)	25(19 ₁₆)	9615.38
19200	f(XIN)/4	2(02 ₁₆)	19200.00	f(XIN)	12(0C ₁₆)	19230.77
38400	f(XIN)	5(05 ₁₆)	38400.00	f(XIN)	5(05 ₁₆)	41666.67
76800	f(XIN)	2(02 ₁₆)	76800.00	f(XIN)	2(02 ₁₆)	83333.33
31250	—	—	—	f(XIN)	7(07 ₁₆)	31250.00
62500	—	—	—	f(XIN)	3(03 ₁₆)	62500.00

Notes 1: Equation of transfer bit rate:

$$\text{Transfer bit rate (bps)} = \frac{f(\text{XIN})}{(\text{BRG setting value} + 1) \times 16 \times m^*}$$

*m: When bit 0 of the serial I/O2 control register (address 001D₁₆) is set to “0”, a value of m is 1.

When bit 0 of the serial I/O2 control register is set to “1”, a value of m is 4.

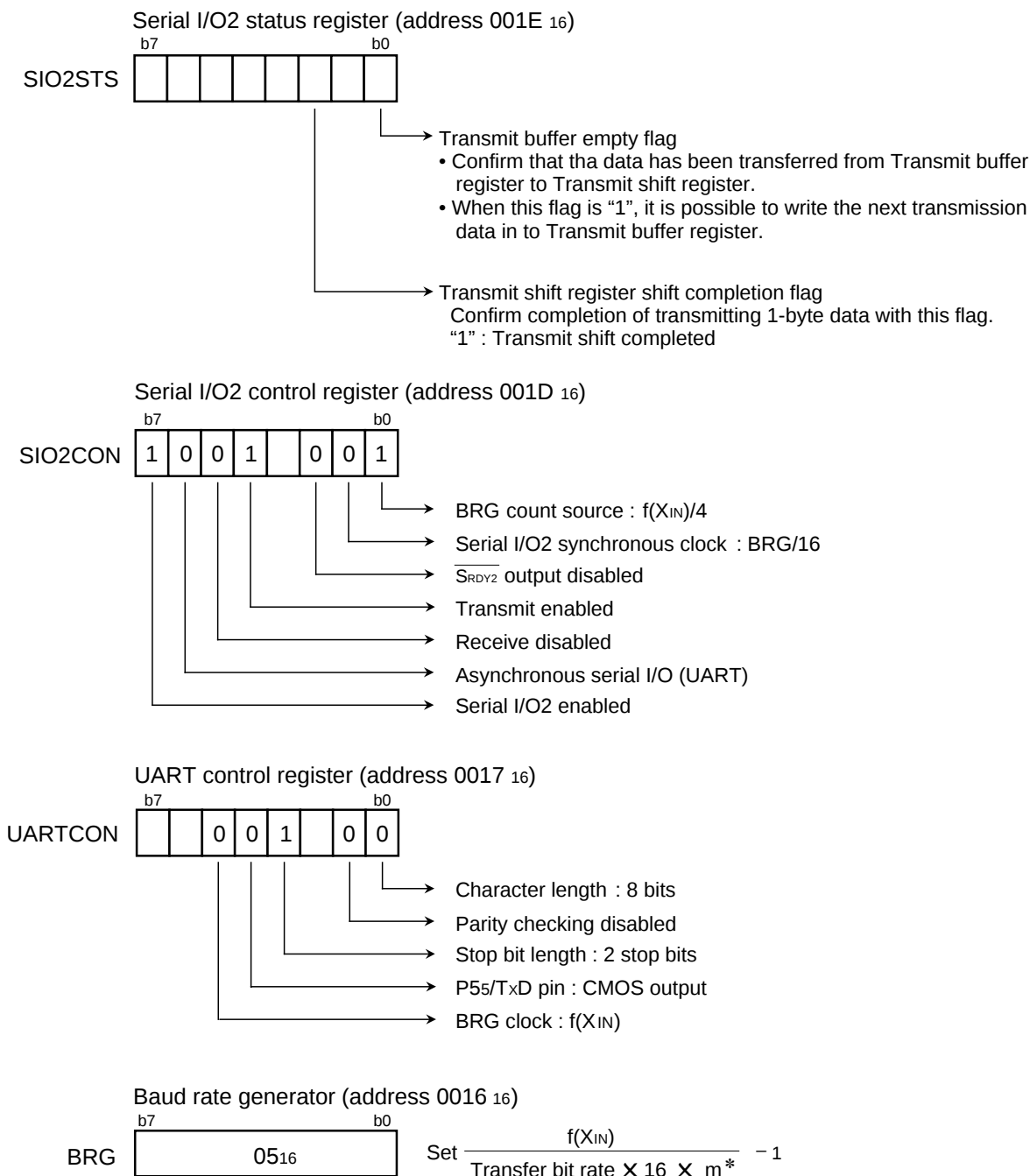
2: Select the BRG count source with bit 0 of the serial I/O2 control register (address 001D₁₆).

APPLICATION

2.3 Serial I/O

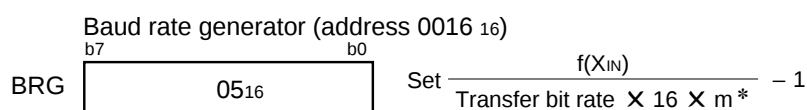
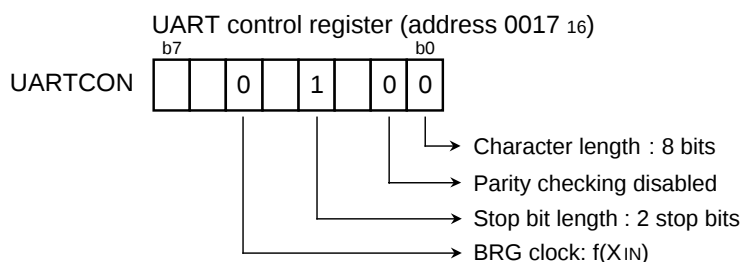
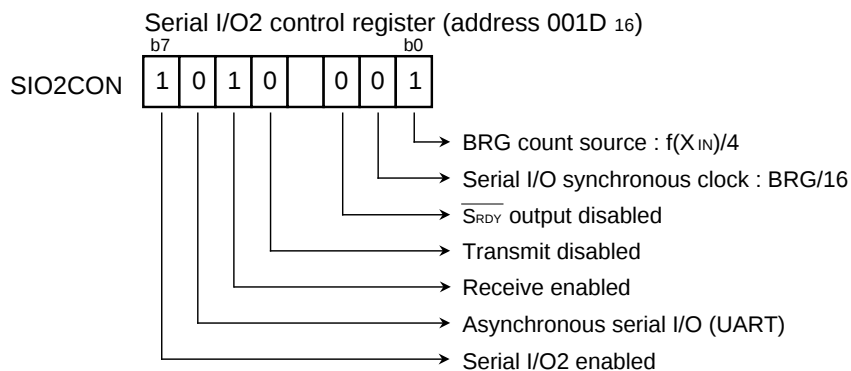
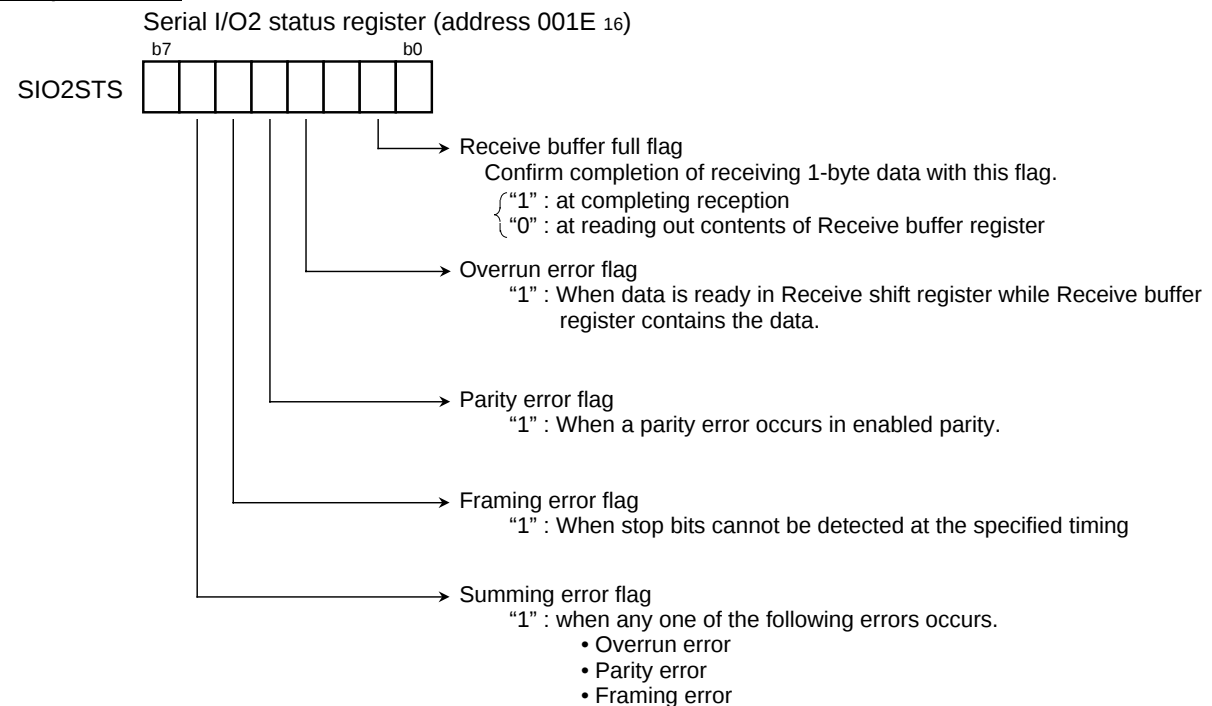
Figure 2.3.52 shows the registers setting relevant to the transmission side; Figure 2.3.53 shows the registers setting relevant to the reception side.

Transmission side



* When bit 0 of SIO2CON (address 001D₁₆) is set to "0", a value of m is 1.
When bit 0 of SIO2CON is set to "1", a value of m is 4.

Fig. 2.3.52 Registers setting relevant to transmission side

Reception side

* When bit 0 of SIO2CON (address 001D₁₆) is set to "0", a value of m is 1.
 When bit 0 of SIO2CON is set to "1", a value of m is 4.

Fig. 2.3.53 Registers setting relevant to reception side

APPLICATION

2.3 Serial I/O

Figure 2.3.54 shows a control procedure of the transmission side, and Figure 2.3.55 shows a control procedure of the reception side.

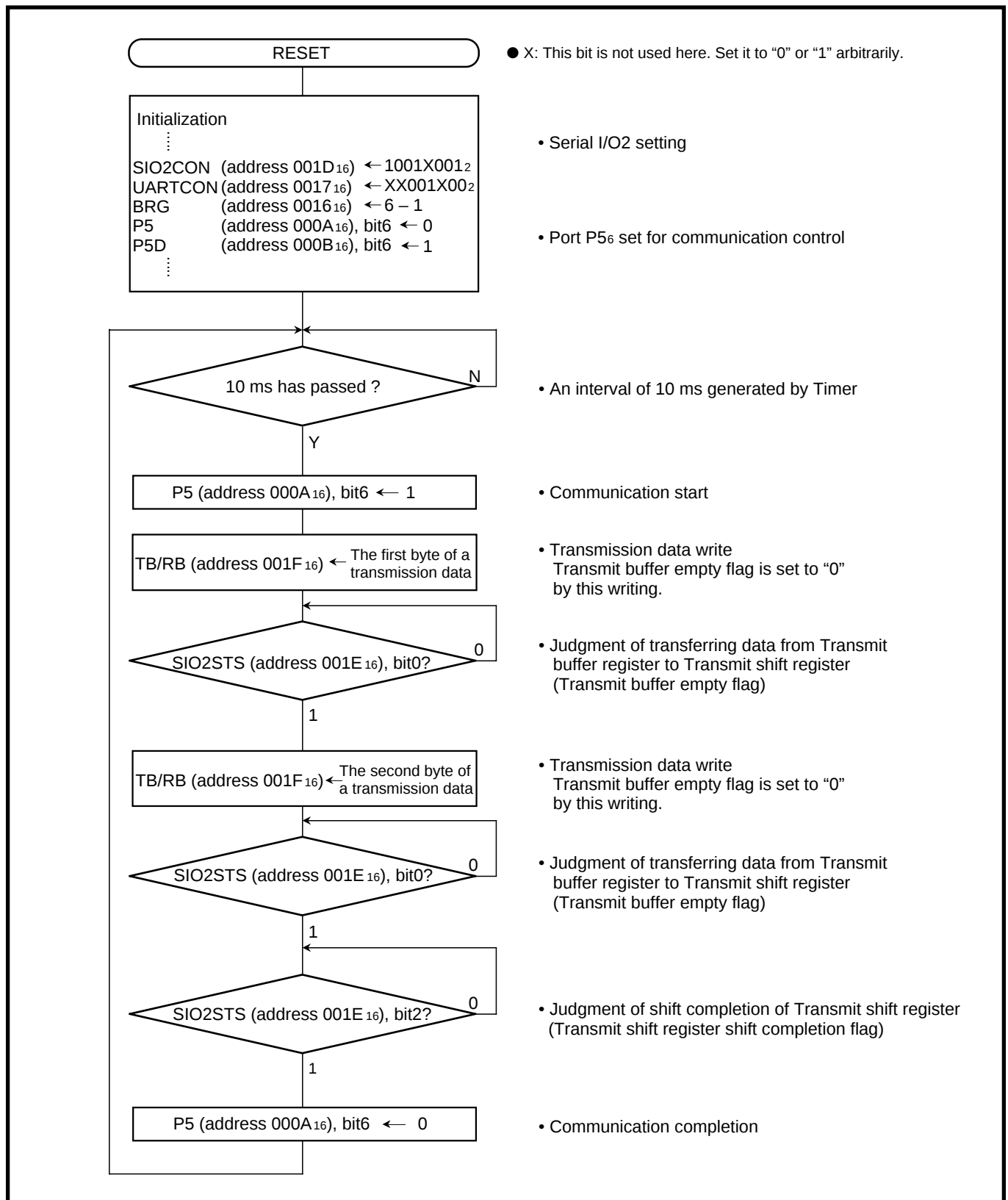


Fig. 2.3.54 Control procedure of transmission side

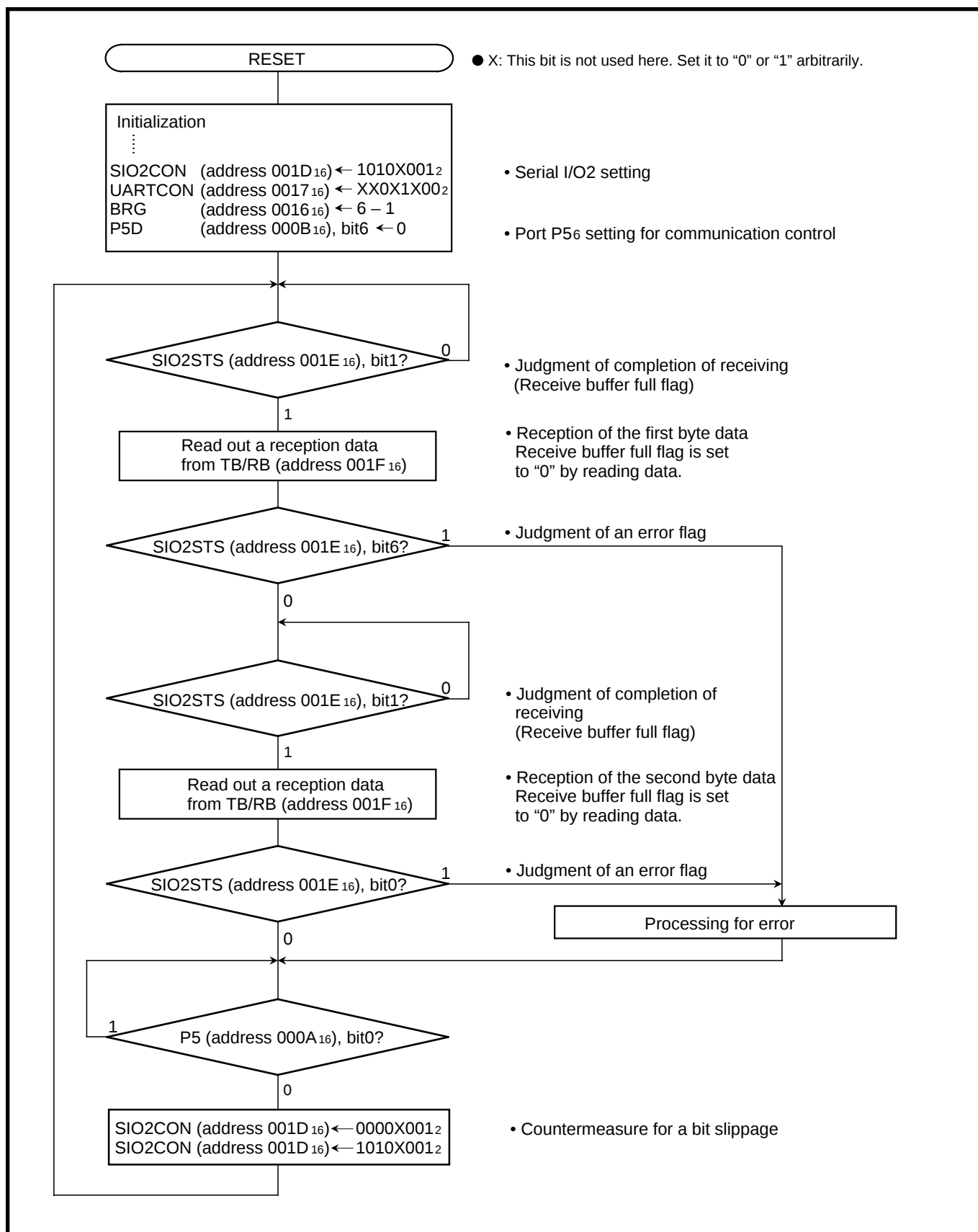


Fig. 2.3.55 Control procedure of reception side

APPLICATION

2.3 Serial I/O

2.3.9 Notes on serial I/O1

(1) Clock

■ Using internal clock

After setting the synchronous clock to an internal clock, clear the serial I/O interrupt request bit before perform the normal serial I/O transfer or the serial I/O automatic transfer.

■ Using external clock

After inputting “H” level to the external clock input pin, clear the serial I/O interrupt request bit before performing the normal serial I/O transfer or the serial I/O automatic transfer.

(2) Using serial I/O1 interrupt

Clear bit 3 of the interrupt request register 1 to “0” by software.

(3) State of S_{OUT1} pin

The S_{OUT1} pin control bit of the serial I/O1 control register 2 can be used to select the state of the S_{OUT1} pin when serial data is not transferred; either output active or high-impedance. However, when selecting an external synchronous clock; the S_{OUT1} pin can become the high-impedance state by setting the S_{OUT1} pin control bit to “1” when the serial I/O1 clock input is at “H” after transfer completion.

(4) Serial I/O initialization bit

- Set “0” to the serial I/O initialization bit of the serial I/O1 control register 1 when terminating a serial transfer during transferring.
- When writing “1” to the serial I/O initialization bit, the serial I/O1 is enabled, but each register is not initialized. Set the value of each register by program.

(5) Handshake signal

■ S_{BUSY1} input signal

Input an “H” level to the S_{BUSY1} input and an “L” level signal to the $\overline{\text{S}}_{\text{BUSY1}}$ input in the initial state. When the external synchronous clock is selected, switch the input level to the S_{BUSY1} input and the $\overline{\text{S}}_{\text{BUSY1}}$ input while the serial I/O1 clock input is in “H” state.

■ S_{RDY1} input-output signal

When selecting the internal synchronous clock, input an “L” level to the S_{RDY1} input and an “H” level signal to the $\overline{\text{S}}_{\text{RDY1}}$ input in the initial state.

(6) 8-bit serial I/O mode

■ When selecting external synchronous clock

When an external synchronous clock is selected, the contents of the serial I/O1 register are being shifted continually while the transfer clock is input to the serial I/O1 clock pin. In this case, control the clock externally.

(7) In automatic transfer serial I/O mode

■ Set of automatic transfer interval

- When the S_{BUSY1} output is used, and the S_{BUSY1} output and the S_{STB1} output function as signals for each transfer data set by the S_{BUSY1} output•S_{STB1} output function selection bit of serial I/O1 control register 2; the transfer interval is inserted before the first data is transmitted/received, and after the last data is transmitted/received. Accordingly, regardless of the contents of the S_{BUSY1} output•S_{STB1} output function selection bit, this transfer interval for each 1-byte data becomes 2 cycles longer than the value set by the automatic transfer interval set bits of serial I/O1 control register 3.

- When using the S_{STB1} output, regardless of the contents of the S_{BUSY1} output, S_{STB1} output function selection bit, this transfer interval for each 1-byte data becomes 2 cycles longer than the value set by the automatic transfer interval set bits of serial I/O1 control register 3.
- When using the combined output of S_{BUSY1} and S_{STB1} as the signal for each of all transfer data set, the transfer interval after completion of transmission/reception of the last data becomes 2 cycles longer than the value set by the automatic transfer interval set bits.
- Set the transfer interval of each 1-byte data transfer to 5 or more cycles of the internal clock ϕ after the rising edge of the last bit of a 1-byte data.
- When selecting an external clock, the set of automatic transfer interval becomes invalid.

■ Set of serial I/O1 transfer counter

- Write the value decreased by 1 from the number of transfer data bytes to the serial I/O1 transfer counter.
- When selecting an external clock, after writing a value to the serial I/O1 register/transfer counter, wait for 5 or more cycles of internal clock ϕ before inputting the transfer clock to the serial I/O1 clock pin.

■ Serial I/O initialization bit

A serial I/O1 automatic transfer interrupt request occurs when "0" is written to the serial I/O initialization bit during an operation. Disable it with the interrupt enable bit as necessary by program.

APPLICATION

2.3 Serial I/O

2.3.10 Notes on serial I/O2

(1) Notes when selecting clock synchronous serial I/O

① Stop of transmission operation

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the transmit enable bit to “0” (transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O2 enable bit is cleared to “0” (serial I/O2 disabled), the internal transmission is running (in this case, since pins TxD, RxD, S_{CLK21}, S_{CLK22} and S_{RDY2} function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O2 enable bit is set to “1” at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

② Stop of receive operation

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the receive enable bit to “0” (receive disabled), or clear the serial I/O2 enable bit to “0” (serial I/O2 disabled).

③ Stop of transmit/receive operation

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, simultaneously clear both the transmit enable bit and receive enable bit to “0” (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

● Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to “0” (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O2 enable bit to “0” (serial I/O2 disabled) (refer to (1), ①).

(2) Notes when selecting clock asynchronous serial I/O**① Stop of transmission operation**

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the transmit enable bit to "0" (transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O2 enable bit is cleared to "0" (serial I/O2 disabled), the internal transmission is running (in this case, since pins TxD, RxD, S_{CLK21}, S_{CLK22} and S_{RDY2} function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O2 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

② Stop of receive operation

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the receive enable bit to "0" (receive disabled).

③ Stop of transmit/receive operation**Only transmission operation is stopped.**

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the transmit enable bit to "0" (transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O2 enable bit is cleared to "0" (serial I/O2 disabled), the internal transmission is running (in this case, since pins TxD, RxD, S_{CLK21}, S_{CLK22} and S_{RDY2} function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O2 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

Only receive operation is stopped.

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the receive enable bit to "0" (receive disabled).

(3) S_{RDY2} output of reception side

When signals are output from the S_{RDY2} pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the S_{RDY2} output enable bit, and the transmit enable bit to "1" (transmit enabled).

(4) Setting serial I/O2 control register again

Set the serial I/O2 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0."

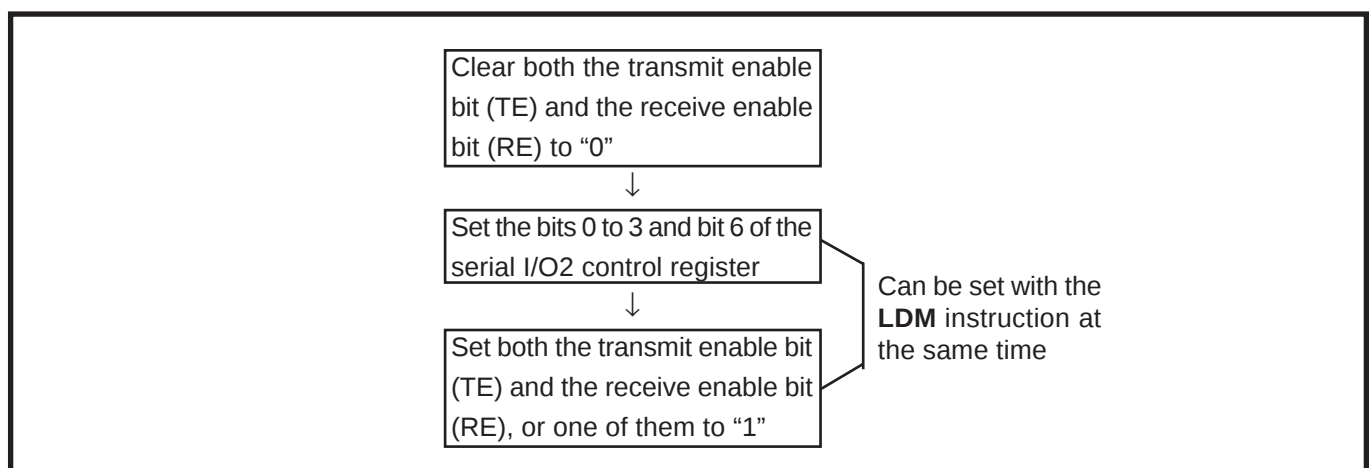


Fig. 2.3.56 Sequence of setting serial I/O2 control register again

APPLICATION

2.3 Serial I/O

(5) Data transmission control with referring to transmit shift register completion flag

The transmit shift register completion flag changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

(6) Transmission control when external clock is selected

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to “1” at “H” of the serial I/O2 clock input level. Also, write the transmit data to the transmit buffer register (serial I/O shift register) at “H” of the serial I/O2 clock input level.

(7) Transmit interrupt request when transmit enable bit is set

The transmission interrupt request bit is set and the interruption request is generated even when selecting timing that either of the following flags is set to “1” as timing where the transmission interruption is generated.

- Transmit buffer empty flag is set to “1”
- Transmit shift register completion flag is set to “1”

Therefore, when the transmit interrupt is used, set the transmit interrupt enable bit to transmit enabled as the following sequence.

- ① Transmit enable bit is set to “1”
- ② Transmit interrupt request bit is set to “0”

● Reason

When the transmission enable bit is set to “1”, the transmit buffer empty flag and transmit shift register completion flag are set to “1”.

(8) Using TxD pin

The P5s/TxD P-channel output disable bit of UART control register is valid in both cases: using as a normal I/O port and as the TxD pin. Do not supply $V_{cc} + 0.3\text{ V}$ or more even when using the P5s/TxD pin as an N-channel open-drain output.

Additionally, in the serial I/O2, the TxD pin latches the last bit and continues to output it after completing transmission.

2.4 FLD controller

This paragraph describes the setting method of FLD controller relevant registers, notes etc.

2.4.1 Memory assignment

Address	
003D ₁₆	Interrupt request register 2 (IREQ2)
003F ₁₆	Interrupt control register 2 (ICON2)
≈	≈
0EF2 ₁₆	P1FLDRAM write disable register (P1FLDRAM)
0EF3 ₁₆	P3FLDRAM write disable register (P3FLDRAM)
0EF4 ₁₆	FLDC mode register (FLDM)
0EF5 ₁₆	Tdisp time set register (TDISP)
0EF6 ₁₆	Toff1 time set register (TOFF1)
0EF7 ₁₆	Toff2 time set register (TOFF2)
0EF8 ₁₆	FLD data pointer (FLDDP)
0EF9 ₁₆	Port P0FLD/port switch register (P0FPR)
0EFA ₁₆	Port P2FLD/port switch register (P2FPR)
0EFB ₁₆	Port P8FLD/port switch register (P8FPR)
0EFC ₁₆	Port P8FLD output control register (P8FLDCON)

Fig. 2.4.1 Memory assignment of FLD controller relevant registers

APPLICATION

2.4 FLD controller

2.4.2 Relevant registers

P1FLDRAM write disable register

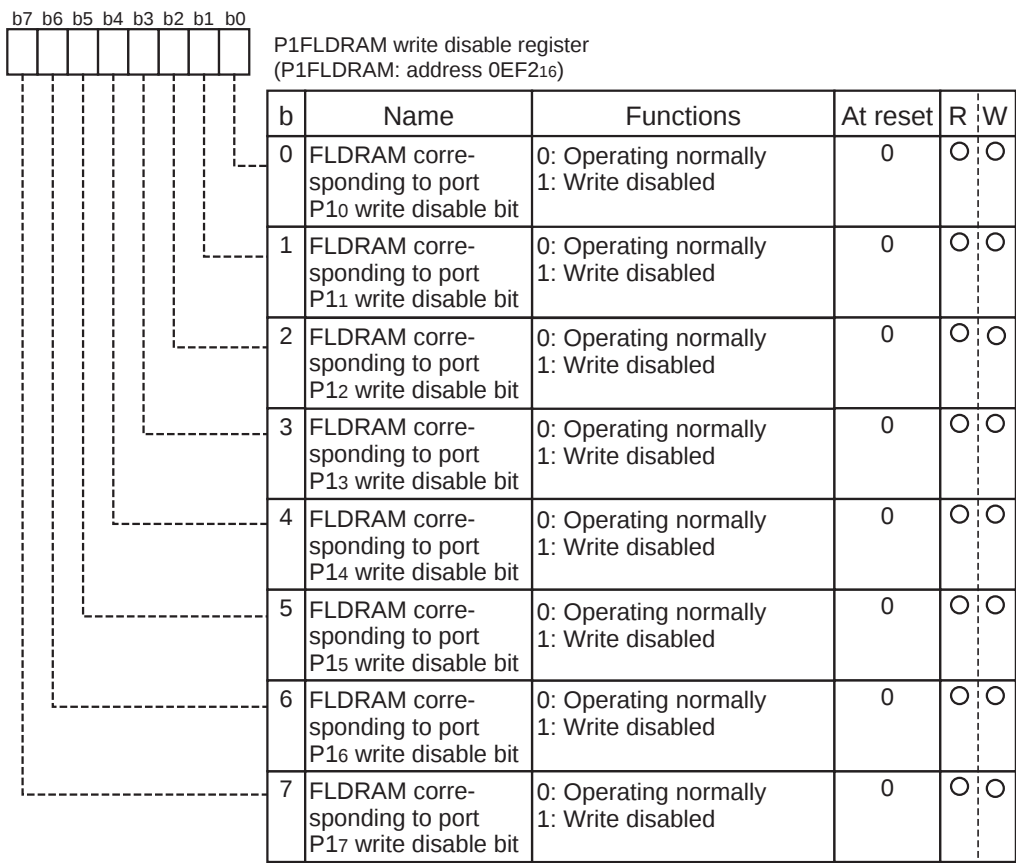


Fig. 2.4.2 Structure of P1FLDRAM write disable register

P3FLDRAM write disable register

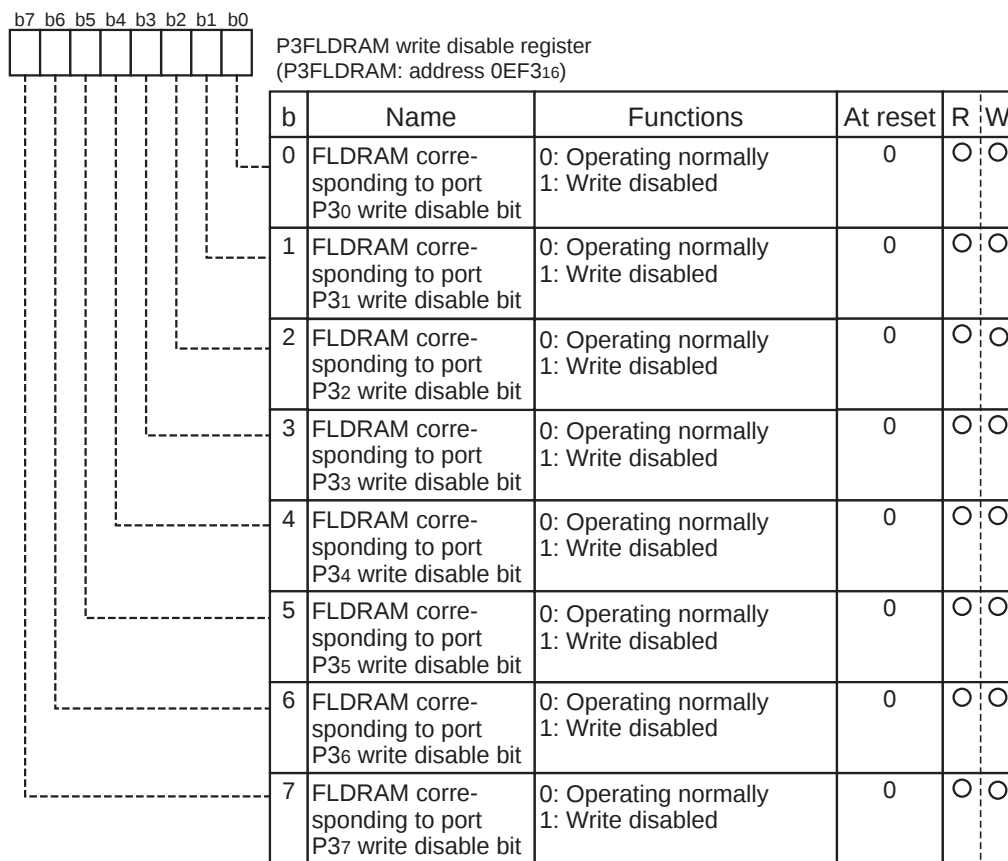


Fig. 2.4.3 Structure of P3FLDRAM write disable register

APPLICATION

2.4 FLD controller

FLDC mode register

b7	b6	b5	b4	b3	b2	b1	b0	
								FLDC mode register (FLDM: address 0EF4 ₁₆)
b	Name	Functions	At reset	R	W			
0	Automatic display control bit (P0, P1, P2, P3, P8)	0 : General-purpose mode 1 : Automatic display mode	0	○	○			
1	Display start bit	0 : Display stopped 1 : Display in progress (display starts by writing "1")	0	○	○			
2	Tscan control bits	b3 b2 0 0 : 0 FLD digit interrupt (at rising edge of each digit) 0 1 : 1 × Tdisp 1 0 : 2 × Tdisp 1 1 : 3 × Tdisp FLD blanking interrupt (at falling edge of last digit)	0	○	○			
3			0	○	○			
4	Timing number control bit	0 : 16 timing mode 1 : 32 timing mode (Note 2)	0	○	○			
5	Gradation display mode selection control bit	0 : Not selected 1 : Selected (Notes 1, 2)	0	○	○			
6	Tdisp counter count source selection bit	0 : f(X _{IN})/16 or f(X _{CIN})/32 1 : f(X _{IN})/64 or f(X _{CIN})/128	0	○	○			
7	High-breakdown voltage port drivability selection bit	0 : Drivability strong 1 : Drivability weak	0	○	○			

Notes 1: When the gradation display mode is selected, the number of timing is max. 16 timing. (Set "0" to the timing number control bit (b4).)

2: When switching the timing number control bit (b4) or the gradation display mode selection control bit (b5), set "0" to the display start bit (b1) (display stop state) before that.

Fig. 2.4.4 Structure of FLD mode register

Tdisp time set register

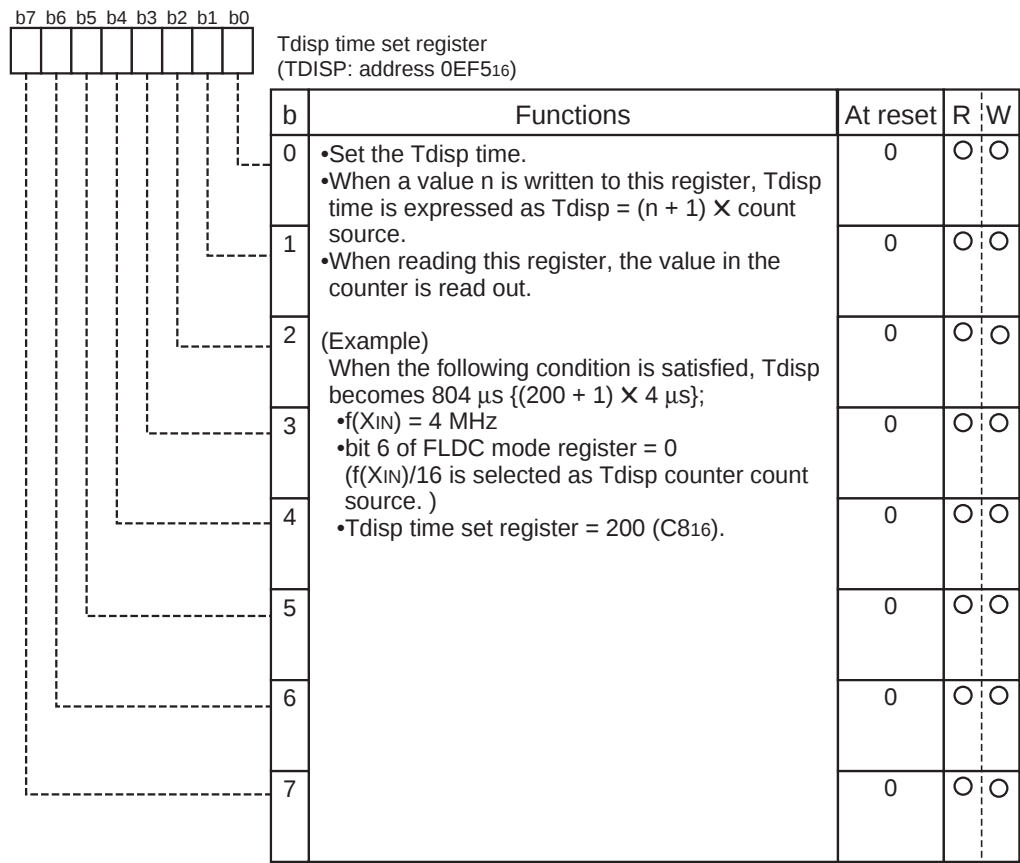


Fig. 2.4.5 Structure of Tdisp time set register

APPLICATION

2.4 FLD controller

Toff1 time set register

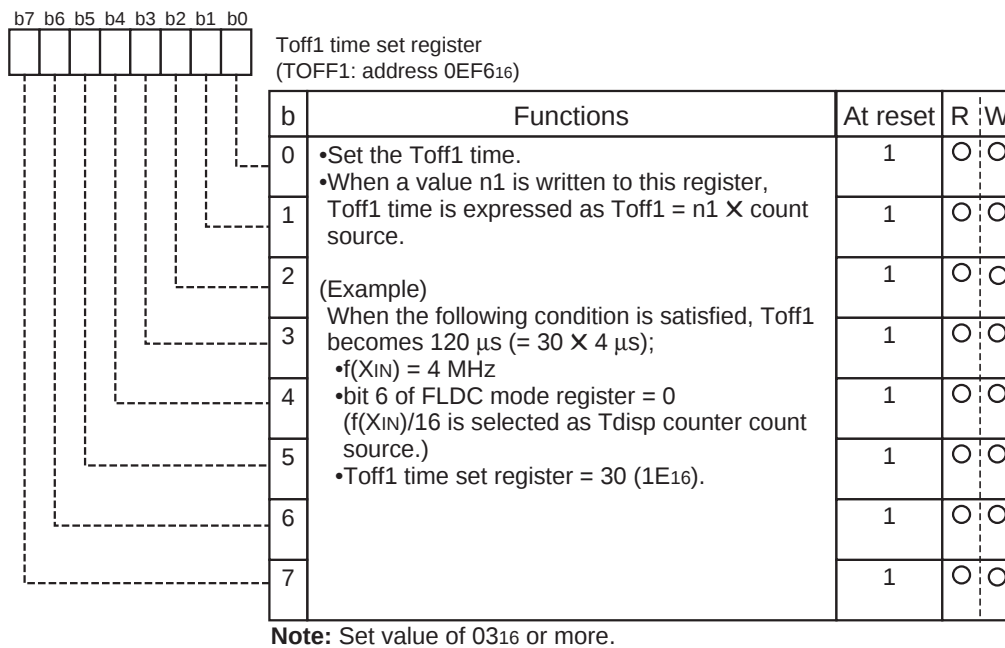


Fig. 2.4.6 Structure of Toff1 time set register

Toff2 time set register

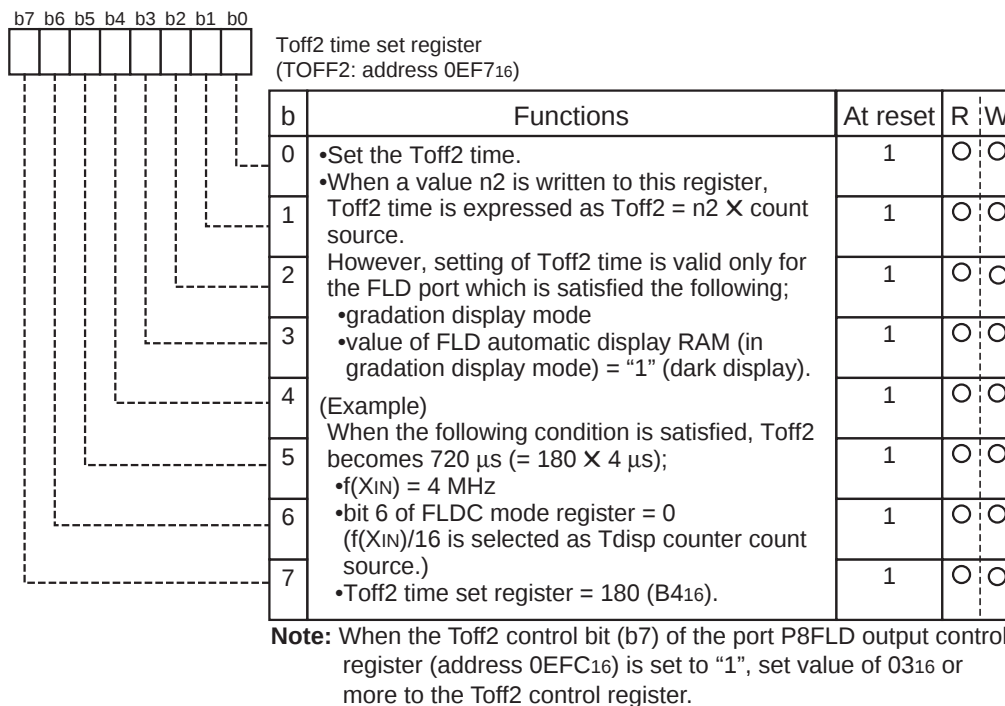


Fig. 2.4.7 Structure of Toff2 time set register

FLD data pointer/FLD data pointer reload register

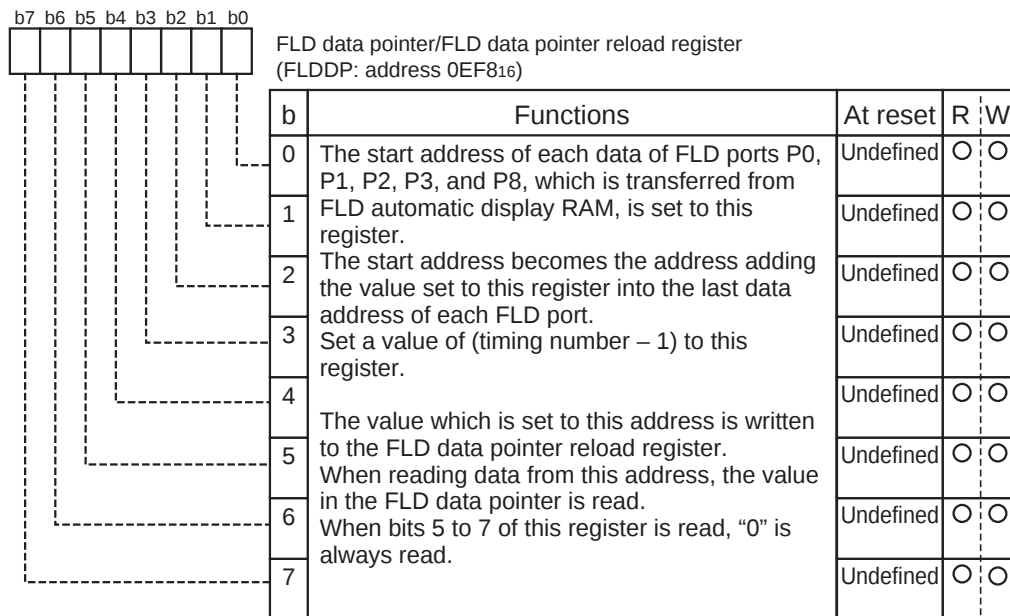


Fig. 2.4.8 Structure of FLD data pointer/FLD data pointer reload register

Port P0FLD/port switch register

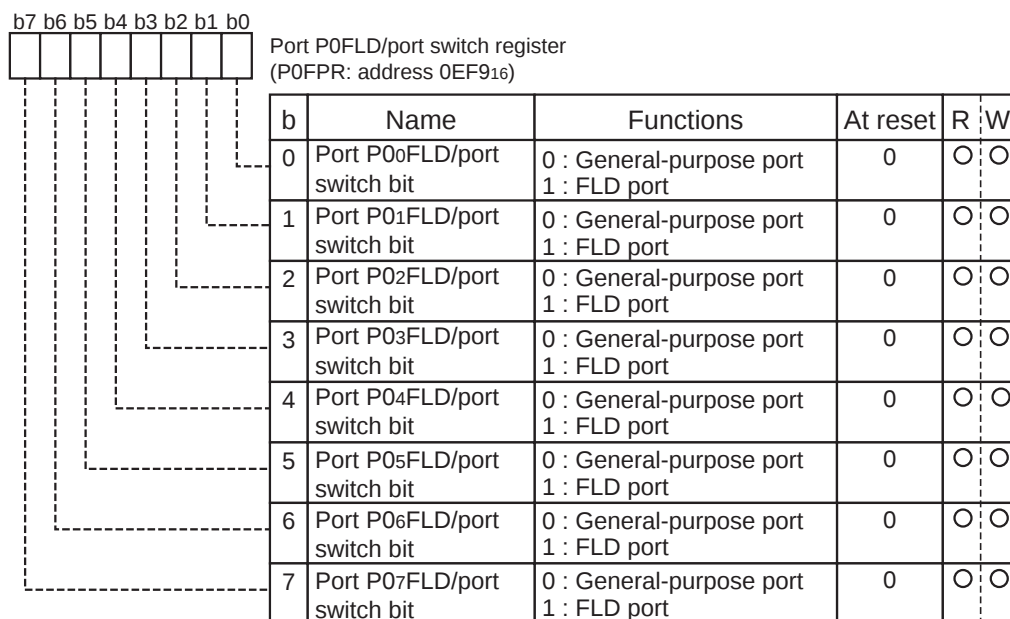


Fig. 2.4.9 Structure of port P0FLD/port switch register

APPLICATION

2.4 FLD controller

Port P2FLD/port switch register

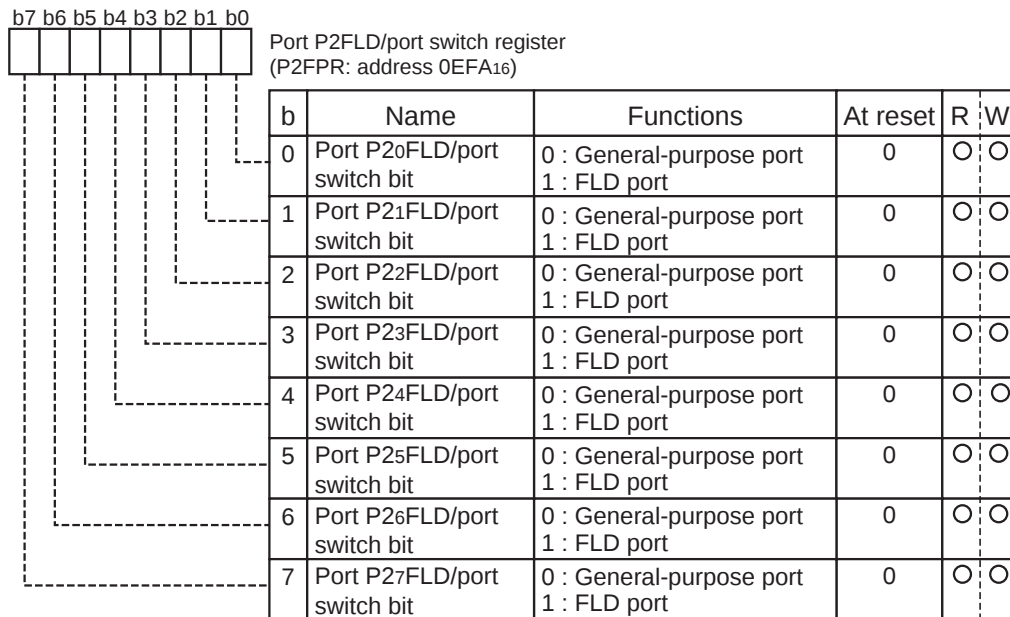


Fig. 2.4.10 Structure of port P2FLD/port switch register

Port P8FLD/port switch register

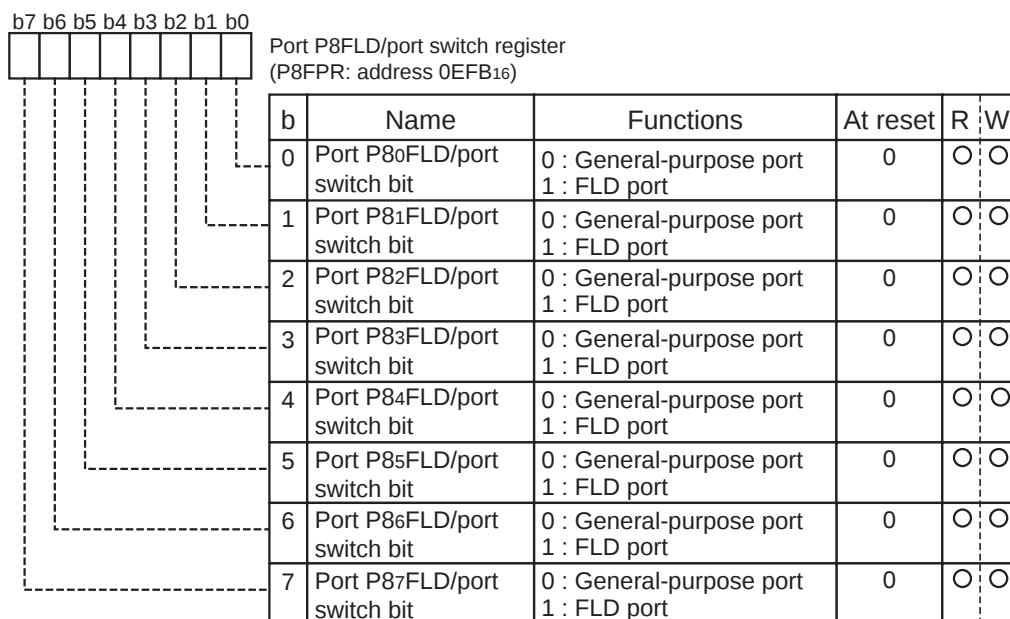
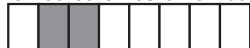


Fig. 2.4.11 Structure of port P8FLD/port switch register

Port P8FLD output control register

b7 b6 b5 b4 b3 b2 b1 b0

Port P8FLD output control register
(P8FLDCON : address 0EFC16)

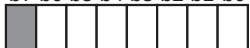
b	Name	Functions	At reset	R	W
0	P84–P87 FLD output reverse bit	0 : Output normally 1 : Reverse output	0	○	○
1	P84–P87/FLDRAM write disable bit	0 : Operating normally 1 : Write disabled	0	○	○
2	P84–P87 Toff invalid bit	0 : Operating normally 1 : Toff invalid	0	○	○
3	P84–P87 delay control bit (Note)	0 : No delay 1 : Delay	0	○	○
4	P63/AN9 dimmer output control bit	0 : Ordinary port 1 : Dimmer output	0	○	○
5	Nothing is arranged for these bits. These are write disabled bits. When these bits are read out, the contents are “0”.		0	○	×
6			0	○	×
7	Toff2 control bit	0 : Operating normally (falling operation) 1 : Rising operation	0	○	○

Note: Valid only when selecting FLD port and P84–P87 Toff invalid function

Fig. 2.4.12 Structure of port P8FLD output control register

Interrupt request register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2
(IREQ2 : address 3D16)

b	Name	Functions	At reset	R	W
0	Timer 4 interrupt request bit (Note)	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
1	Timer 5 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
2	Timer 6 interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
3	Serial I/O2 receive interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
4	INT3/serial I/O2 transmit interrupt request bit (Note)	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
5	INT4 interrupt request bit A-D converter interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
6	FLD blanking interrupt request bit FLD digit interrupt request bit	0 : No interrupt request issued 1 : Interrupt request issued	0	○	*
7	Nothing is arranged for this bit. This is a write disabled bit. When this bit is read out, the contents are “0”.		0	○	×

*: “0” can be set by software, but “1” cannot be set.

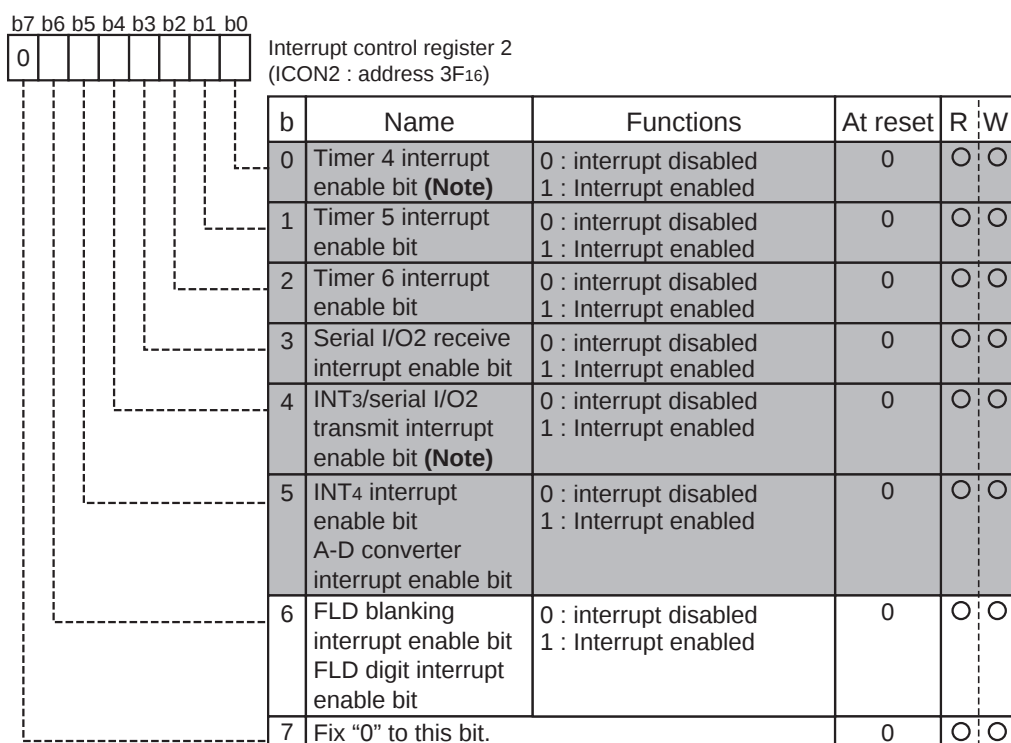
Note: In the mask option type P, if timer 4 interrupt whose count source is CNTR1 input and INT3 interrupt are selected, these bits do not become “1”.

Fig. 2.4.13 Structure of interrupt request register 2

APPLICATION

2.4 FLD controller

Interrupt control register 2



Note: In the mask option type P, timer 4 interrupt whose count source is CNTR1 input and INT3 interrupt are not available.

Fig. 2.4.14 Structure of interrupt control register 2

(1) Key-scan using FLD automatic display and segments

Outline: Key read-in with segment pins is performed by software using the FLD automatic display mode.



- Specifications:**
- Use of total 20 FLD ports (10 digits; 10 segments (8 key-scan included))
 - Use of FLD automatic display mode
 - Display in gradation display mode and 16 timing mode
 - $T_{off1} = 40 \mu s$, $T_{off2} = 64 \mu s$, $T_{disp} = 204 \mu s$, $T_{scan} = 3 \times T_{disp} = 720 \mu s$, $f(X_{IN}) = 4 \text{ MHz}$
 - Use of FLD blanking interrupt

Figure 2.4.16 shows the timing chart of key-scan, and Figure 2.4.17 shows the enlarged view of Tscan. After switching the segment pin to an output port, generate the waveform shown Figure 2.4.17 by software and perform key-scan.



APPLICATION

2.4 FLD controller

Figure 2.4.18 shows the setting of relevant registers.

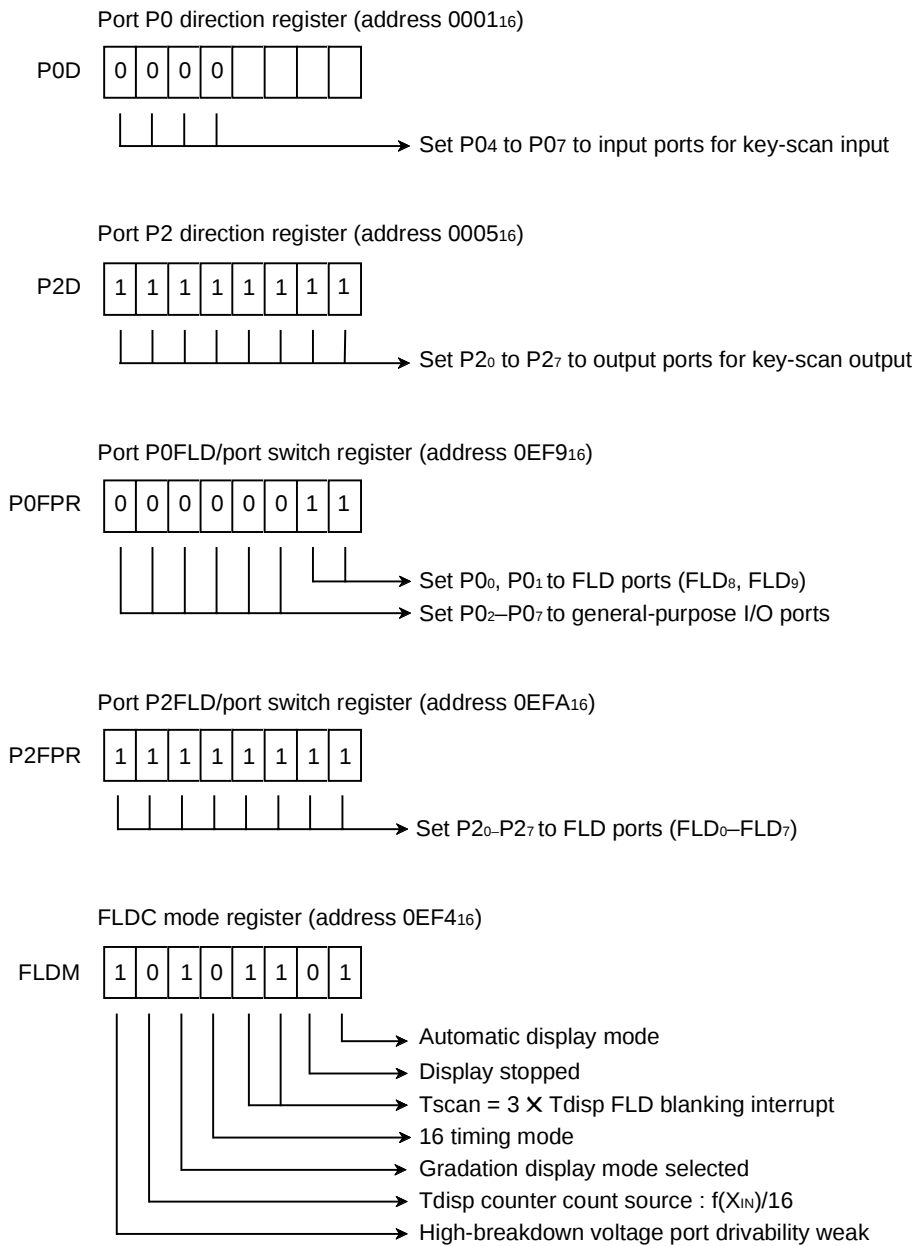


Fig. 2.4.18 Setting of relevant registers

Tdisp time set register (address 0EF5₁₆)

TDISP

32 ₁₆

50 (32₁₆) set; $(50 + 1) \times \text{count source} = 204 \mu\text{s}$
 Count source = $f(X_{\text{IN}})/16 = 4 \mu\text{s}$, at $f(X_{\text{IN}}) = 4 \text{ MHz}$

Toff1 time set register (address 0EF6₁₆)

TOFF1

A ₁₆

10 (A₁₆) set; $10 \times \text{count source} = 40 \mu\text{s}$
 Count source = $f(X_{\text{IN}})/16 = 4 \mu\text{s}$, at $f(X_{\text{IN}}) = 4 \text{ MHz}$

Toff2 time set register (address 0EF7₁₆)

TOFF2

10 ₁₆

16 (10₁₆) set; $16 \times \text{count source} = 64 \mu\text{s}$
 Count source = $f(X_{\text{IN}})/16 = 4 \mu\text{s}$, at $f(X_{\text{IN}}) = 4 \text{ MHz}$

Note: Perform this setting when the gradation display mode is selected.FLD data pointer (address 0EF8₁₆)

FLDDP

0	0	0	0	1	0	0	1
---	---	---	---	---	---	---	---

--	--	--	--	--	--	--	--

 → Set {(digit number) – 1} = 9

P1FLDRAM write disable register (address 0EF2₁₆)

P1FLDRAM

1	1	1	1	1	1	1	1
---	---	---	---	---	---	---	---

--	--	--	--	--	--	--	--

 → Disable writing to FLDRAM corresponding to P10 to P17

P3FLDRAM write disable register (address 0EF3₁₆)

P3FLDRAM

						1	1
--	--	--	--	--	--	---	---

--	--

 → Disable writing to FLDRAM corresponding to P30, P31

Interrupt request register 2 (address 003D₁₆)

IREQ2

0							
---	--	--	--	--	--	--	--

--

 → Clear FLD blanking interrupt request bit

Interrupt control register 2 (address 003F₁₆)

ICON2

0	1						
---	---	--	--	--	--	--	--

--

 → FLD blanking interrupt: Enabled

FLDC mode register (address 0EF4₁₆)

FLDM

1	0	1	0	1	1	1	1
---	---	---	---	---	---	---	---

--

 → Display start

APPLICATION

2.4 FLD controller

Setting of FLD automatic display RAM:

Table 2.4.1 FLD automatic display RAM map

1 to 16 timing display data stored area

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0FB0 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB1 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB2 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB3 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB4 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB5 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB6 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB7 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB8 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB9 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FBA ₁₆								
0FBB ₁₆								
0FBC ₁₆								
0FBD ₁₆								
0FBE ₁₆								
0FBF ₁₆								
0FC0 ₁₆							FLD9	FLD8
0FC1 ₁₆							FLD9	FLD8
0FC2 ₁₆							FLD9	FLD8
0FC3 ₁₆							FLD9	FLD8
0FC4 ₁₆							FLD9	FLD8
0FC5 ₁₆							FLD9	FLD8
0FC6 ₁₆							FLD9	FLD8
0FC7 ₁₆							FLD9	FLD8
0FC8 ₁₆							FLD9	FLD8
0FC9 ₁₆							FLD9	FLD8
0FCA ₁₆								
0FCB ₁₆								
0FCC ₁₆								
0FCD ₁₆								
0FCE ₁₆								
0FCF ₁₆								
0FD0 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD1 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD2 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD3 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD4 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD5 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD6 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD7 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD8 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD9 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FDA ₁₆								
0FDB ₁₆								
0FDC ₁₆								
0FDD ₁₆								
0FDE ₁₆								
0FDF ₁₆								
0FE0 ₁₆							FLD25	FLD24
0FE1 ₁₆							FLD25	FLD24
0FE2 ₁₆							FLD25	FLD24
0FE3 ₁₆							FLD25	FLD24
0FE4 ₁₆							FLD25	FLD24
0FE5 ₁₆							FLD25	FLD24
0FE6 ₁₆							FLD25	FLD24
0FE7 ₁₆							FLD25	FLD24
0FE8 ₁₆							FLD25	FLD24
0FE9 ₁₆							FLD25	FLD24

Gradation display control data stored area

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0F60 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F61 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F62 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F63 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F64 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F65 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F66 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F67 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F68 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F69 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F6A ₁₆								
0F6B ₁₆								
0F6C ₁₆								
0F6D ₁₆								
0F6E ₁₆								
0F6F ₁₆								
0F70 ₁₆							FLD9	FLD8
0F71 ₁₆							FLD9	FLD8
0F72 ₁₆							FLD9	FLD8
0F73 ₁₆							FLD9	FLD8
0F74 ₁₆							FLD9	FLD8
0F75 ₁₆							FLD9	FLD8
0F76 ₁₆							FLD9	FLD8
0F77 ₁₆							FLD9	FLD8
0F78 ₁₆							FLD9	FLD8
0F79 ₁₆							FLD9	FLD8
0F7A ₁₆								
0F7B ₁₆								
0F7C ₁₆								
0F7D ₁₆								
0F7E ₁₆								
0F7F ₁₆								
0F80 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F81 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F82 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F83 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F84 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F85 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F86 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F87 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F88 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F89 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F8A ₁₆								
0F8B ₁₆								
0F8C ₁₆								
0F8D ₁₆								
0F8E ₁₆								
0F8F ₁₆								
0F90 ₁₆							FLD25	FLD24
0F91 ₁₆							FLD25	FLD24
0F92 ₁₆							FLD25	FLD24
0F93 ₁₆							FLD25	FLD24
0F94 ₁₆							FLD25	FLD24
0F95 ₁₆							FLD25	FLD24
0F96 ₁₆							FLD25	FLD24
0F97 ₁₆							FLD25	FLD24
0F98 ₁₆							FLD25	FLD24
0F99 ₁₆							FLD25	FLD24

Corresponding digit pin

→ FLD₂₅ (P₃₁)
→ FLD₂₄ (P₃₀)
→ FLD₂₃ (P₁₇)
→ FLD₂₂ (P₁₆)
→ FLD₂₁ (P₁₅)
→ FLD₂₀ (P₁₄)
→ FLD₁₉ (P₁₃)
→ FLD₁₈ (P₁₂)
→ FLD₁₇ (P₁₁)
→ FLD₁₆ (P₁₀)

→ FLD₂₅ (P₃₁)
→ FLD₂₄ (P₃₀)
→ FLD₂₃ (P₁₇)
→ FLD₂₂ (P₁₆)
→ FLD₂₁ (P₁₅)
→ FLD₂₀ (P₁₄)
→ FLD₁₉ (P₁₃)
→ FLD₁₈ (P₁₂)
→ FLD₁₇ (P₁₁)
→ FLD₁₆ (P₁₀)

 : Area which is used to set segment data

 : Area which is used to set digit data

 : Area which is available as ordinary RAM

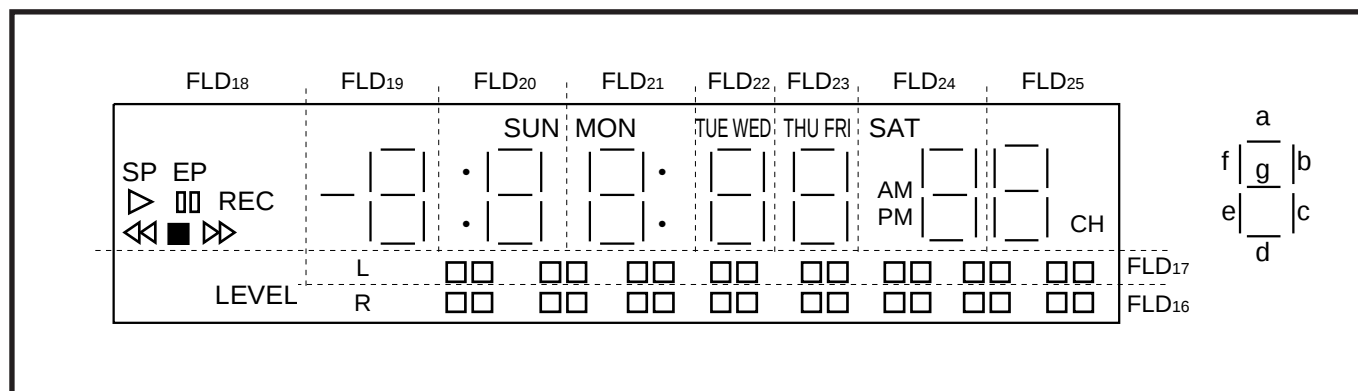


Fig. 2.4.19 FLD digit allocation example

Table 2.4.2 FLD automatic display RAM map example

1 to 16 timing display data stored area									Gradation display control data stored area									Corresponding digit pin
Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0FB0 ₁₆	CH	g	f	e	d	c	b	a	0F60 ₁₆	CH	g	f	e	d	c	b	a	→ FLD ₂₅ (P ₃₁)
0FB1 ₁₆	SAT	g	f	e	d	c	b	a	0F61 ₁₆	SAT	g	f	e	d	c	b	a	→ FLD ₂₄ (P ₃₀)
0FB2 ₁₆	FRI	g	f	e	d	c	b	a	0F62 ₁₆	FRI	g	f	e	d	c	b	a	→ FLD ₂₃ (P ₁₇)
0FB3 ₁₆	WED	g	f	e	d	c	b	a	0F63 ₁₆	WED	g	f	e	d	c	b	a	→ FLD ₂₂ (P ₁₆)
0FB4 ₁₆	MON	g	f	e	d	c	b	a	0F64 ₁₆	MON	g	f	e	d	c	b	a	→ FLD ₂₁ (P ₁₅)
0FB5 ₁₆	SUN	g	f	e	d	c	b	a	0F65 ₁₆	SUN	g	f	e	d	c	b	a	→ FLD ₂₀ (P ₁₄)
0FB6 ₁₆	—	g	f	e	d	c	b	a	0F66 ₁₆	—	g	f	e	d	c	b	a	→ FLD ₁₉ (P ₁₃)
0FB7 ₁₆	■	◀	▶	◻	◻	REC	SP	EP	0F67 ₁₆	■	◀	▶	◻	◻	REC	SP	EP	→ FLD ₁₈ (P ₁₂)
0FB8 ₁₆	◻	◻	◻	◻	◻	◻	◻	◻	0F68 ₁₆	◻	◻	◻	◻	◻	◻	◻	◻	→ FLD ₁₇ (P ₁₁)
0FB9 ₁₆	◻	◻	◻	◻	◻	◻	◻	◻	0F69 ₁₆	◻	◻	◻	◻	◻	◻	◻	◻	→ FLD ₁₆ (P ₁₀)
0FBA ₁₆									0F6A ₁₆									
0FBB ₁₆									0F6B ₁₆									
0FBC ₁₆									0F6C ₁₆									
0FBD ₁₆									0F6D ₁₆									
0FBE ₁₆									0F6E ₁₆									
0FBF ₁₆									0F6F ₁₆									
0FC0 ₁₆									0F70 ₁₆									→ FLD ₂₅ (P ₃₁)
0FC1 ₁₆							PM	AM	0F71 ₁₆							PM	AM	→ FLD ₂₄ (P ₃₀)
0FC2 ₁₆								THU	0F72 ₁₆								THU	→ FLD ₂₃ (P ₁₇)
0FC3 ₁₆								TUE	0F73 ₁₆								TUE	→ FLD ₂₂ (P ₁₆)
0FC4 ₁₆								:	0F74 ₁₆								:	→ FLD ₂₁ (P ₁₅)
0FC5 ₁₆								:	0F75 ₁₆								:	→ FLD ₂₀ (P ₁₄)
0FC6 ₁₆									0F76 ₁₆									→ FLD ₁₉ (P ₁₃)
0FC7 ₁₆									0F77 ₁₆									→ FLD ₁₈ (P ₁₂)
0FC8 ₁₆							L		0F78 ₁₆							L		→ FLD ₁₇ (P ₁₁)
0FC9 ₁₆							R	LEVEL	0F79 ₁₆							R	LEVEL	→ FLD ₁₆ (P ₁₀)

◻ : Unused

APPLICATION

2.4 FLD controller

Control procedure:

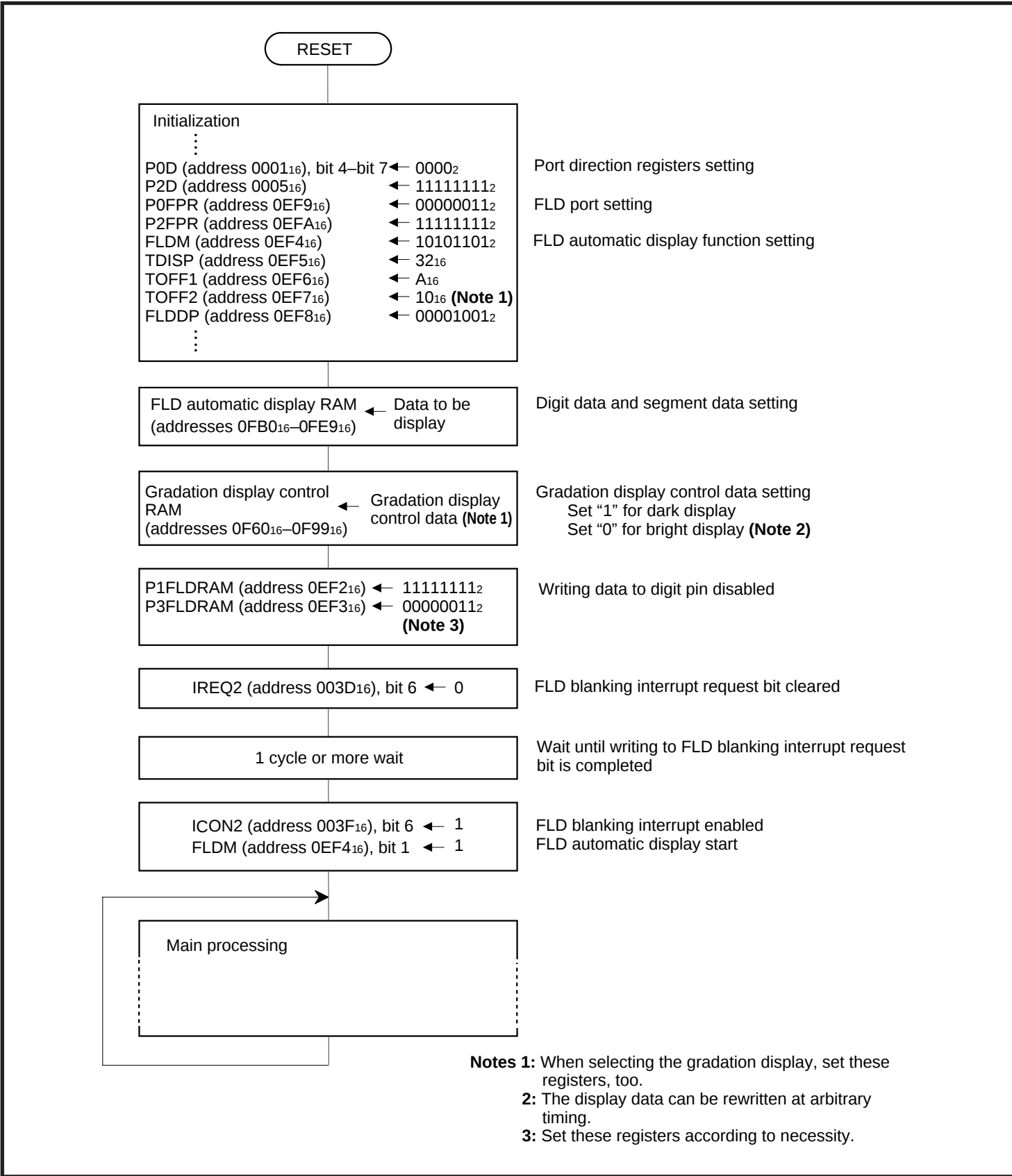
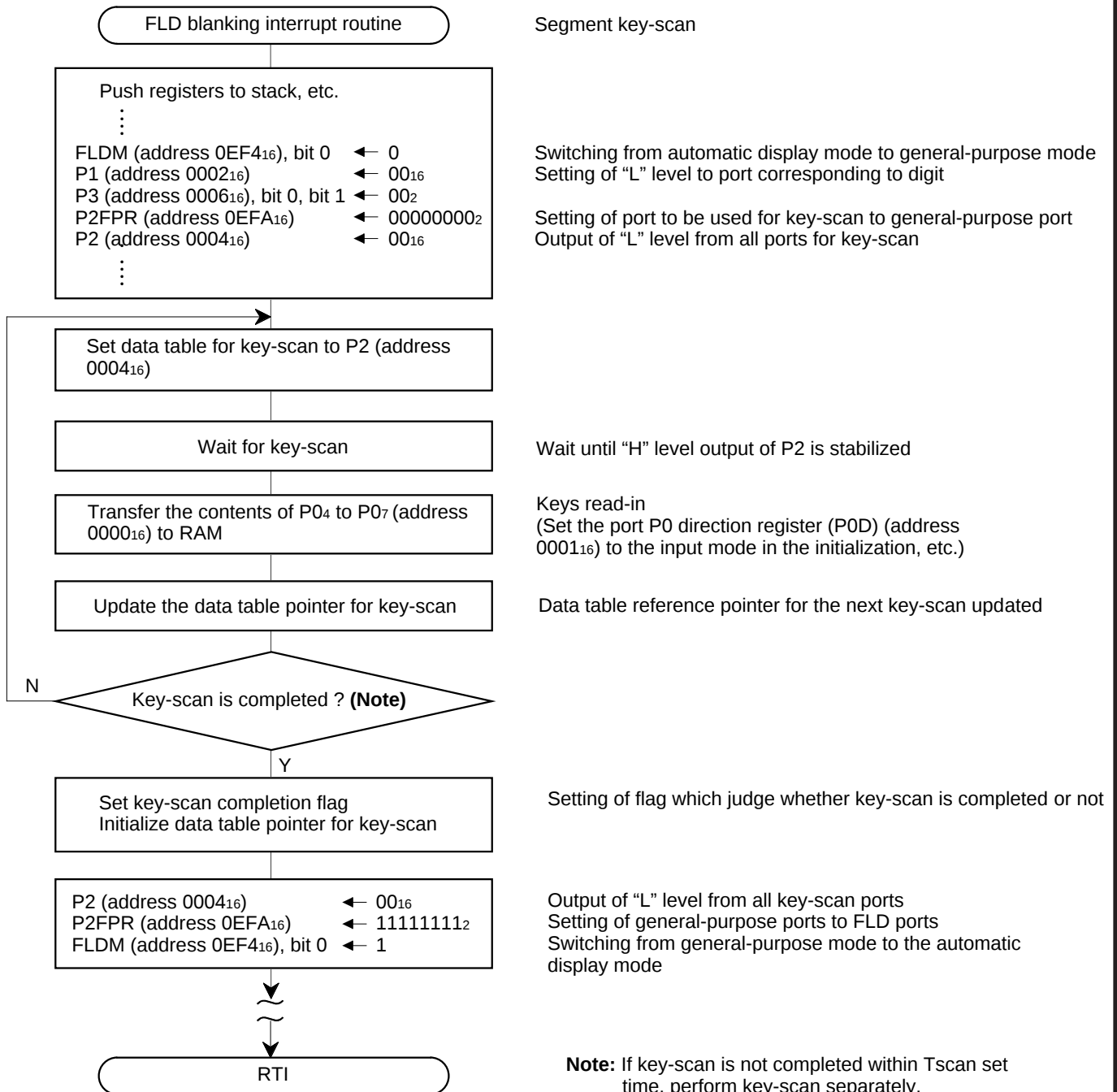


Fig. 2.4.20 Control procedure



APPLICATION

2.4 FLD controller

(2) Key-scan using FLD automatic display and digits

Outline: Key read-in with digit output waveforms is performed by software using the FLD automatic display mode.

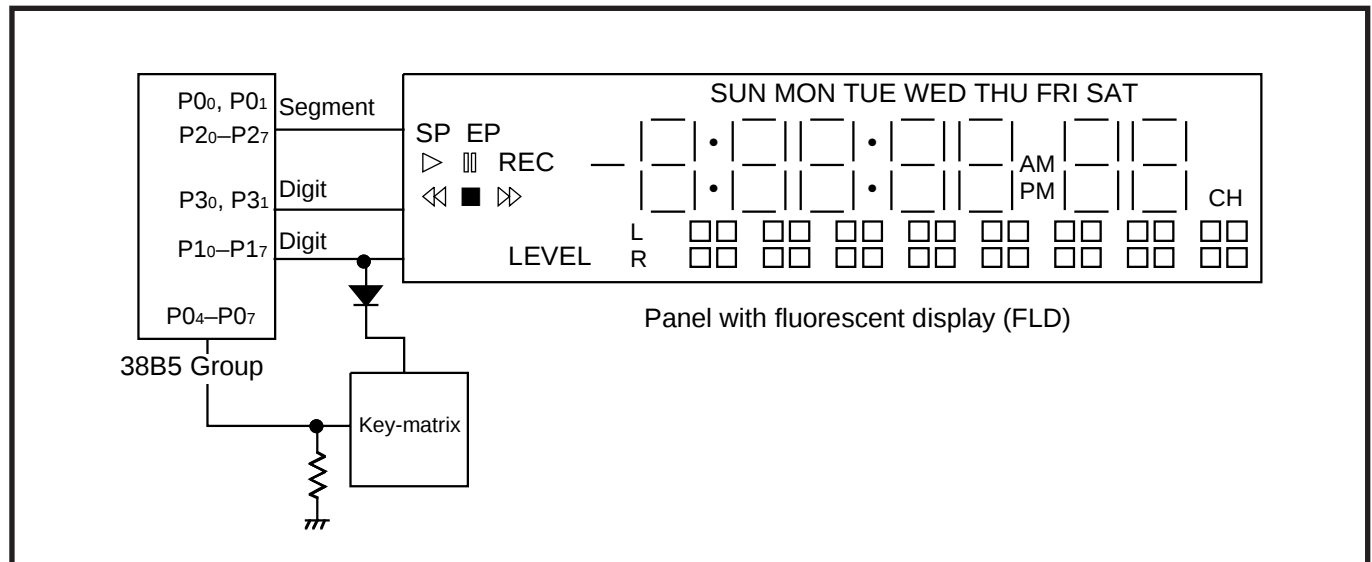


Fig. 2.4.21 Connection diagram

- Specifications:**
- Use of total 20 FLD ports (10 digits, 8 key-scan included; 10 segments)
 - Use of FLD automatic display mode
 - Display in gradation display mode and 16 timing mode
 - Toff1 = 40 ms, Toff2 = 64 ms, Tdisp = 204 ms, Tscan = 0 ms, $f(X_{IN}) = 4 \text{ MHz}$
 - Use of FLD digit interrupt

Figure 2.4.22 shows the timing chart of key-scan.

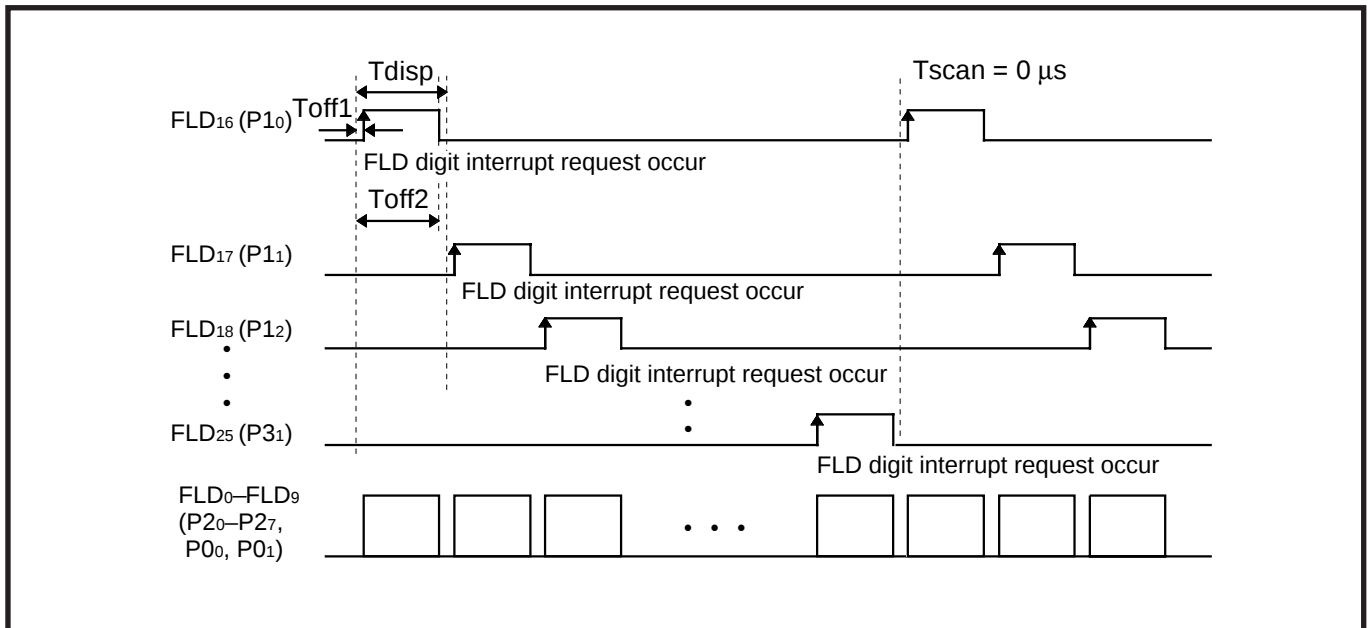


Fig. 2.4.22 Timing chart of key-scan using FLD automatic display mode and digits

APPLICATION

2.4 FLD controller

Figure 2.4.23 shows the setting of relevant registers.

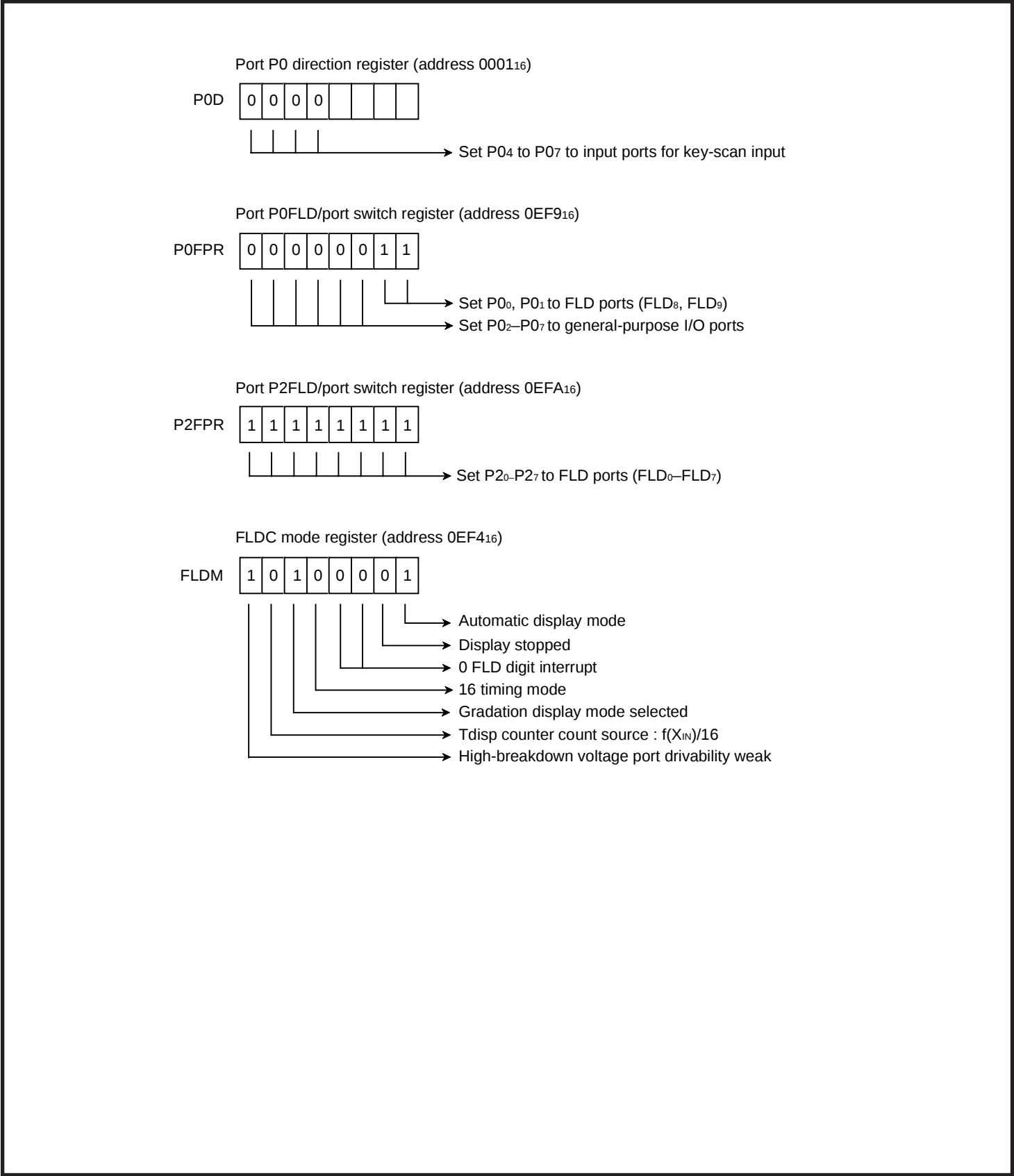


Fig. 2.4.23 Setting of relevant registers

Tdisp time set register (address 0EF5₁₆)

TDISP

32 ₁₆

50 (32₁₆) set; (50 + 1) × count source = 204 μs
 Count source = $f(X_{IN})/16 = 4 \mu s$, at $f(X_{IN}) = 4 \text{ MHz}$

Toff1 time set register (address 0EF6₁₆)

TOFF1

A ₁₆

10 (A₁₆) set; 10 × count source = 40 μs
 Count source = $f(X_{IN})/16 = 4 \mu s$, at $f(X_{IN}) = 4 \text{ MHz}$

Toff2 time set register (address 0EF7₁₆)

TOFF2

10 ₁₆

16 (10₁₆) set; 16 × count source = 64 μs
 Count source = $f(X_{IN})/16 = 4 \mu s$, at $f(X_{IN}) = 4 \text{ MHz}$

Note: Perform this setting when the gradation display mode is selected.FLD data pointer (address 0EF8₁₆)

FLDDP

0	0	0	0	1	0	0	1
---	---	---	---	---	---	---	---

Set {(digit number) – 1} = 9

P1FLDRAM write disable register (address 0EF2₁₆)

P1FLDRAM

1	1	1	1	1	1	1	1
---	---	---	---	---	---	---	---

Disable writing to FLDRAM corresponding to P10 to P17.

P3FLDRAM write disable register (address 0EF3₁₆)

P3FLDRAM

						1	1
--	--	--	--	--	--	---	---

Disable writing to FLDRAM corresponding to P30, P31.

Interrupt request register 2 (address 003D₁₆)

IREQ2

0							
---	--	--	--	--	--	--	--

Clear FLD digit interrupt request bit

Interrupt control register 2 (address 003F₁₆)

ICON2

0	1						
---	---	--	--	--	--	--	--

FLD digit interrupt: Enabled

FLDC mode register (address 0EF4₁₆)

FLDM

1	0	1	0	0	0	1	1
---	---	---	---	---	---	---	---

Display start

APPLICATION

2.4 FLD controller

Setting of FLD automatic display RAM:

Table 2.4.3 FLD automatic display RAM map

1 to 16 timing display data stored area

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0FB0 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB1 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB2 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB3 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB4 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB5 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB6 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB7 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB8 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FB9 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0FBA ₁₆								
0FBB ₁₆								
0FBC ₁₆								
0FBD ₁₆								
0FBE ₁₆								
0FBF ₁₆								
0FC0 ₁₆							FLD9	FLD8
0FC1 ₁₆							FLD9	FLD8
0FC2 ₁₆							FLD9	FLD8
0FC3 ₁₆							FLD9	FLD8
0FC4 ₁₆							FLD9	FLD8
0FC5 ₁₆							FLD9	FLD8
0FC6 ₁₆							FLD9	FLD8
0FC7 ₁₆							FLD9	FLD8
0FC8 ₁₆							FLD9	FLD8
0FC9 ₁₆							FLD9	FLD8
0FCA ₁₆								
0FCB ₁₆								
0FCC ₁₆								
0FCD ₁₆								
0FCE ₁₆								
0FCF ₁₆								
0FD0 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD1 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD2 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD3 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD4 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD5 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD6 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD7 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD8 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FD9 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0FDA ₁₆								
0FDB ₁₆								
0FDC ₁₆								
0FDD ₁₆								
0FDE ₁₆								
0FDF ₁₆								
0FE0 ₁₆							FLD25	FLD24
0FE1 ₁₆							FLD25	FLD24
0FE2 ₁₆							FLD25	FLD24
0FE3 ₁₆							FLD25	FLD24
0FE4 ₁₆							FLD25	FLD24
0FE5 ₁₆							FLD25	FLD24
0FE6 ₁₆							FLD25	FLD24
0FE7 ₁₆							FLD25	FLD24
0FE8 ₁₆							FLD25	FLD24
0FE9 ₁₆							FLD25	FLD24

Gradation display control data stored area

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0F60 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F61 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F62 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F63 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F64 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F65 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F66 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F67 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F68 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F69 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0
0F6A ₁₆								
0F6B ₁₆								
0F6C ₁₆								
0F6D ₁₆								
0F6E ₁₆								
0F6F ₁₆								
0F70 ₁₆							FLD9	FLD8
0F71 ₁₆							FLD9	FLD8
0F72 ₁₆							FLD9	FLD8
0F73 ₁₆							FLD9	FLD8
0F74 ₁₆							FLD9	FLD8
0F75 ₁₆							FLD9	FLD8
0F76 ₁₆							FLD9	FLD8
0F77 ₁₆							FLD9	FLD8
0F78 ₁₆							FLD9	FLD8
0F79 ₁₆							FLD9	FLD8
0F7A ₁₆								
0F7B ₁₆								
0F7C ₁₆								
0F7D ₁₆								
0F7E ₁₆								
0F7F ₁₆								
0F80 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F81 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F82 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F83 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F84 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F85 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F86 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F87 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F88 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F89 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16
0F8A ₁₆								
0F8B ₁₆								
0F8C ₁₆								
0F8D ₁₆								
0F8E ₁₆								
0F8F ₁₆								
0F90 ₁₆							FLD25	FLD24
0F91 ₁₆							FLD25	FLD24
0F92 ₁₆							FLD25	FLD24
0F93 ₁₆							FLD25	FLD24
0F94 ₁₆							FLD25	FLD24
0F95 ₁₆							FLD25	FLD24
0F96 ₁₆							FLD25	FLD24
0F97 ₁₆							FLD25	FLD24
0F98 ₁₆							FLD25	FLD24
0F99 ₁₆							FLD25	FLD24

Corresponding digit pin

→ FLD₂₅ (P₃₁)
→ FLD₂₄ (P₃₀)
→ FLD₂₃ (P₁₇)
→ FLD₂₂ (P₁₆)
→ FLD₂₁ (P₁₅)
→ FLD₂₀ (P₁₄)
→ FLD₁₉ (P₁₃)
→ FLD₁₈ (P₁₂)
→ FLD₁₇ (P₁₁)
→ FLD₁₆ (P₁₀)

→ FLD₂₅ (P₃₁)
→ FLD₂₄ (P₃₀)
→ FLD₂₃ (P₁₇)
→ FLD₂₂ (P₁₆)
→ FLD₂₁ (P₁₅)
→ FLD₂₀ (P₁₄)
→ FLD₁₉ (P₁₃)
→ FLD₁₈ (P₁₂)
→ FLD₁₇ (P₁₁)
→ FLD₁₆ (P₁₀)

: Area which is used to set segment data

: Area which is used to set digit data

: Area which is available as ordinary RAM

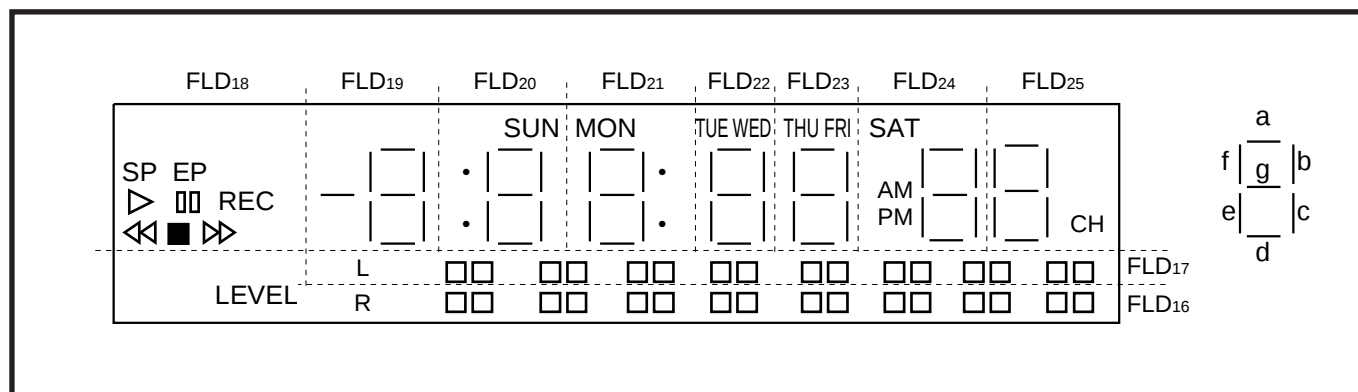


Fig. 2.4.24 FLD digit allocation example

Table 2.4.4 FLD automatic display RAM map example

1 to 16 timing display data stored area									Gradation display control data stored area									Corresponding digit pin
Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0FB0 ₁₆	CH	g	f	e	d	c	b	a	0F60 ₁₆	CH	g	f	e	d	c	b	a	→ FLD ₂₅ (P ₃₁)
0FB1 ₁₆	SAT	g	f	e	d	c	b	a	0F61 ₁₆	SAT	g	f	e	d	c	b	a	→ FLD ₂₄ (P ₃₀)
0FB2 ₁₆	FRI	g	f	e	d	c	b	a	0F62 ₁₆	FRI	g	f	e	d	c	b	a	→ FLD ₂₃ (P ₁₇)
0FB3 ₁₆	WED	g	f	e	d	c	b	a	0F63 ₁₆	WED	g	f	e	d	c	b	a	→ FLD ₂₂ (P ₁₆)
0FB4 ₁₆	MON	g	f	e	d	c	b	a	0F64 ₁₆	MON	g	f	e	d	c	b	a	→ FLD ₂₁ (P ₁₅)
0FB5 ₁₆	SUN	g	f	e	d	c	b	a	0F65 ₁₆	SUN	g	f	e	d	c	b	a	→ FLD ₂₀ (P ₁₄)
0FB6 ₁₆	—	g	f	e	d	c	b	a	0F66 ₁₆	—	g	f	e	d	c	b	a	→ FLD ₁₉ (P ₁₃)
0FB7 ₁₆	■	◀	▶	◻	◻	REC	SP	EP	0F67 ₁₆	■	◀	▶	◻	◻	REC	SP	EP	→ FLD ₁₈ (P ₁₂)
0FB8 ₁₆	◻	◻	◻	◻	◻	◻	◻	◻	0F68 ₁₆	◻	◻	◻	◻	◻	◻	◻	◻	→ FLD ₁₇ (P ₁₁)
0FB9 ₁₆	◻	◻	◻	◻	◻	◻	◻	◻	0F69 ₁₆	◻	◻	◻	◻	◻	◻	◻	◻	→ FLD ₁₆ (P ₁₀)
0FBA ₁₆									0F6A ₁₆									
0FBB ₁₆									0F6B ₁₆									
0FBC ₁₆									0F6C ₁₆									
0FBD ₁₆									0F6D ₁₆									
0FBE ₁₆									0F6E ₁₆									
0FBF ₁₆									0F6F ₁₆									
0FC0 ₁₆									0F70 ₁₆									→ FLD ₂₅ (P ₃₁)
0FC1 ₁₆							PM	AM	0F71 ₁₆							PM	AM	→ FLD ₂₄ (P ₃₀)
0FC2 ₁₆									0F72 ₁₆									→ FLD ₂₃ (P ₁₇)
0FC3 ₁₆									0F73 ₁₆									→ FLD ₂₂ (P ₁₆)
0FC4 ₁₆									0F74 ₁₆									→ FLD ₂₁ (P ₁₅)
0FC5 ₁₆									0F75 ₁₆									→ FLD ₂₀ (P ₁₄)
0FC6 ₁₆									0F76 ₁₆									→ FLD ₁₉ (P ₁₃)
0FC7 ₁₆									0F77 ₁₆									→ FLD ₁₈ (P ₁₂)
0FC8 ₁₆							L		0F78 ₁₆							L		→ FLD ₁₇ (P ₁₁)
0FC9 ₁₆							R	LEVEL	0F79 ₁₆							R	LEVEL	→ FLD ₁₆ (P ₁₀)

◻ : Unused

APPLICATION

2.4 FLD controller

Control procedure:

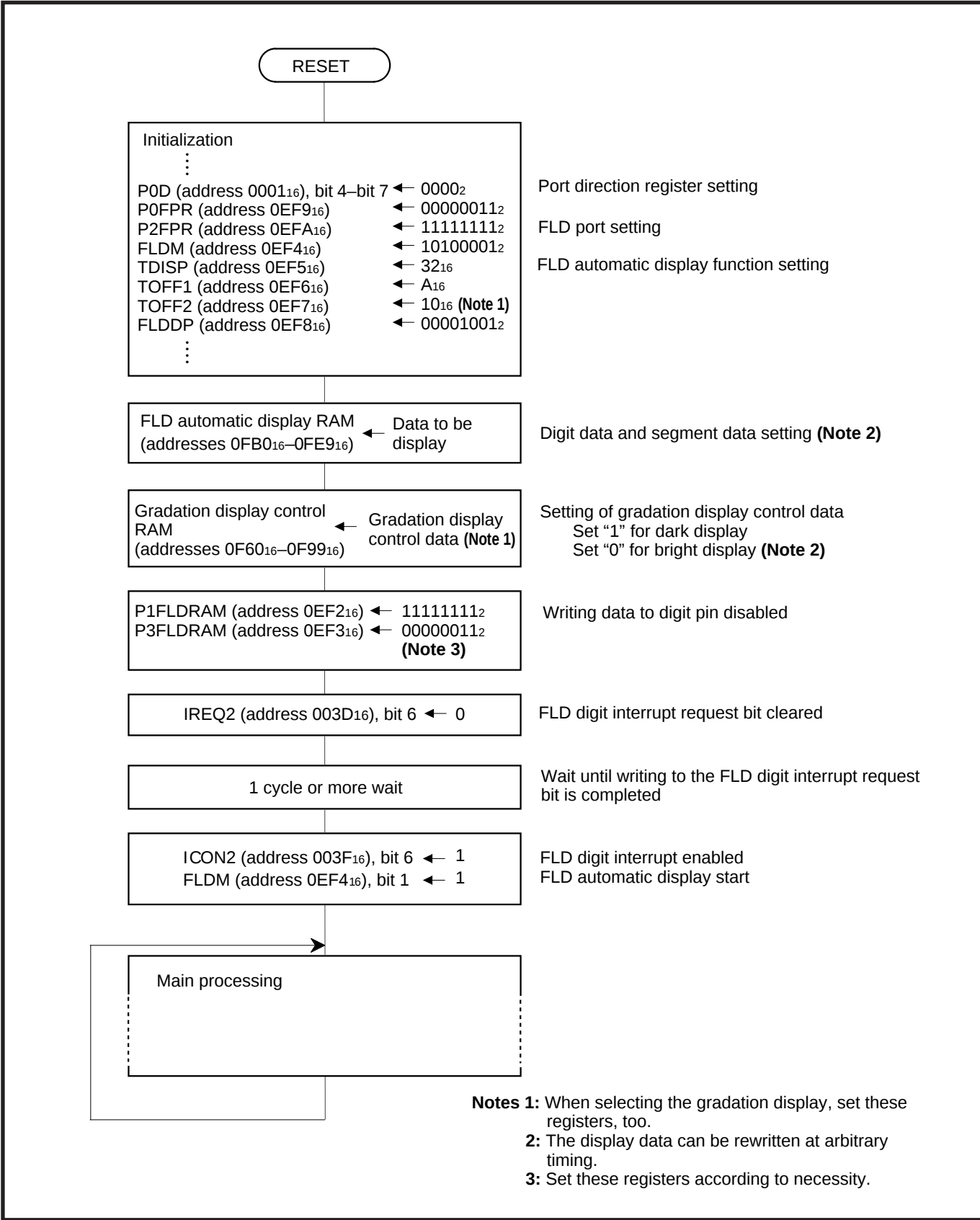
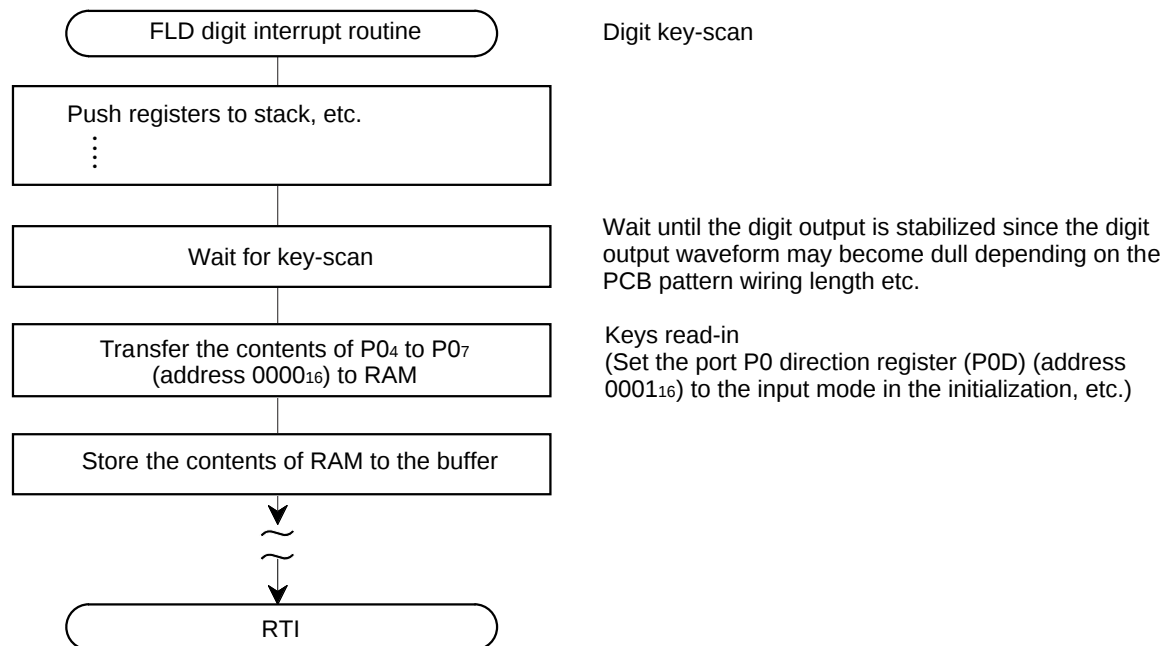


Fig. 2.4.25 Control procedure



APPLICATION

2.4 FLD controller

(3) FLD display by software (example of not used FLD controller)

Outline: FLD display and key read-in is performed, using a timer interrupt.

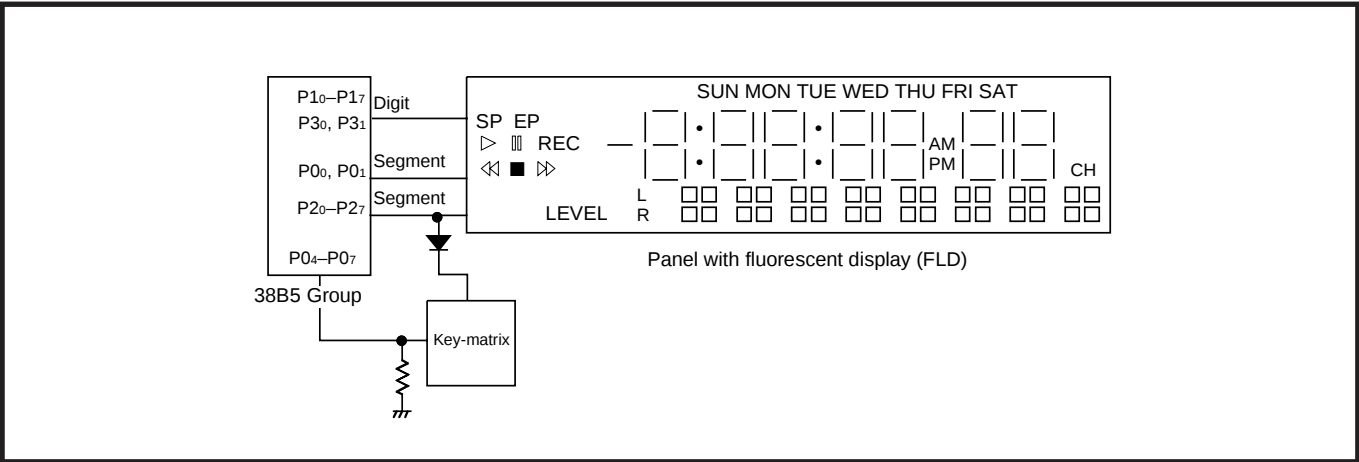


Fig. 2.4.26 Connection diagram

- Specifications:**
- Use of 10 digits and 10 segments (8 key-scan included)
 - Display controlled by software
 - Use of timer 1 interrupt

Figure 2.4.27 shows the timing chart of FLD display by software, and Figure 2.4.28 shows the enlarged view of P20 to P27 key-scan. Generate the waveform shown Figure 2.4.28 by software and perform key-scan.

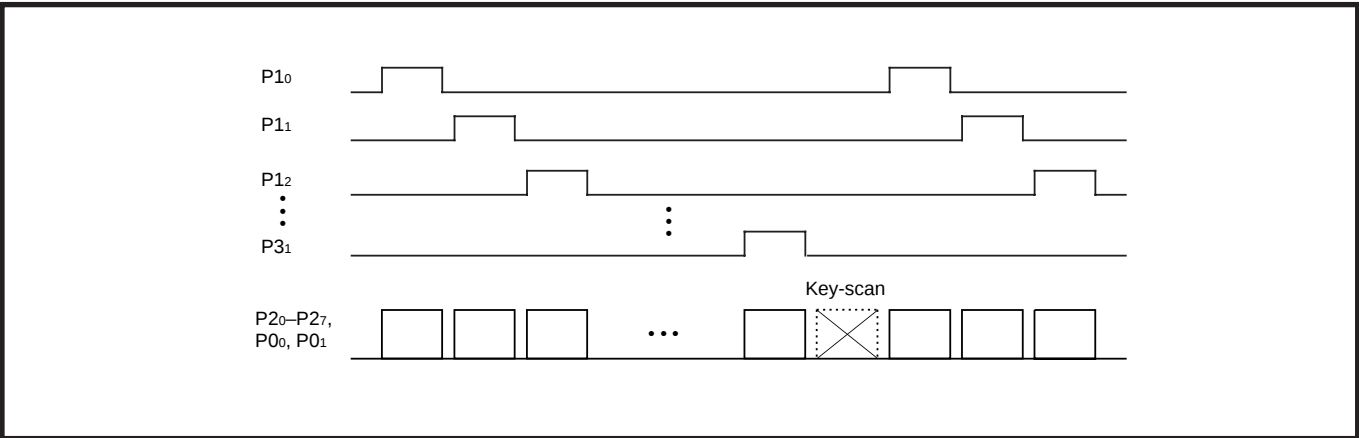


Fig. 2.4.27 Timing chart of FLD display by software

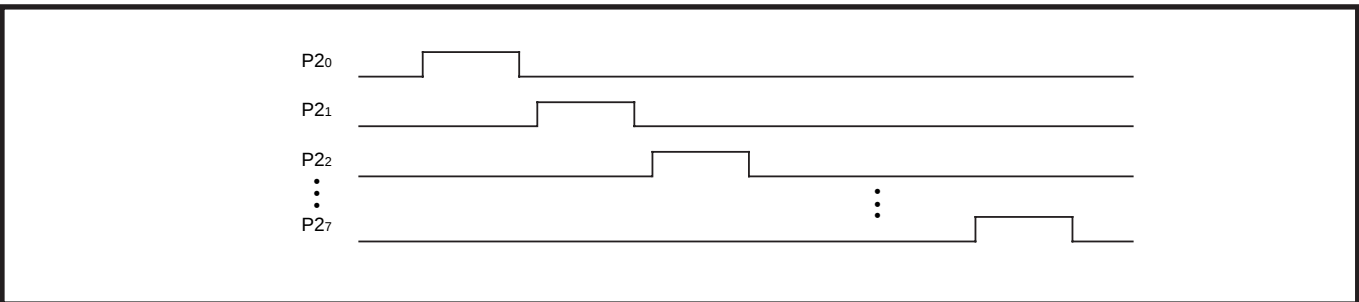


Fig. 2.4.28 Enlarged view of P20 to P27 key-scan

Figure 2.4.29 shows the setting of relevant registers.

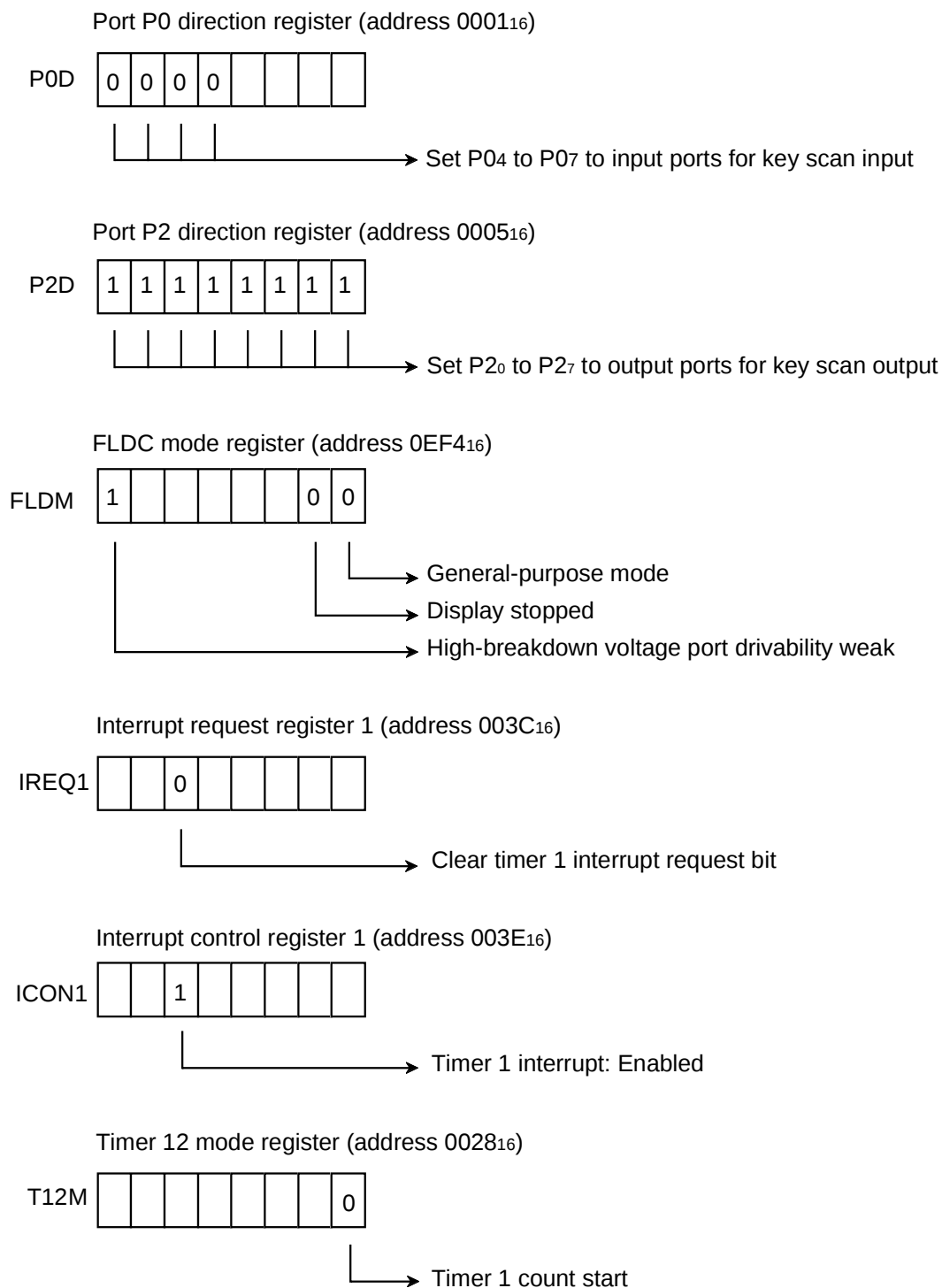


Fig. 2.4.29 Setting of relevant registers

2.4 FLD controller

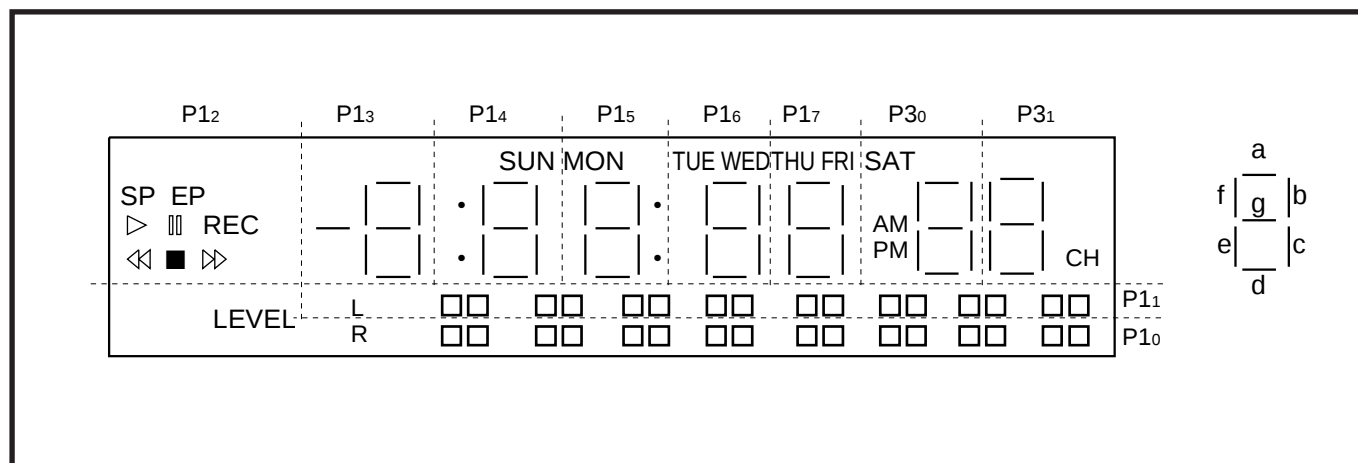


Fig. 2.4.30 FLD digit allocation example

Table 2.4.5 FLD automatic display RAM map example

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Corresponding digit pin
0FB0 ₁₆	CH	g	f	e	d	c	b	a	→ P ₃₁
0FB1 ₁₆	SAT	g	f	e	d	c	b	a	→ P ₃₀
0FB2 ₁₆	FRI	g	f	e	d	c	b	a	→ P ₁₇
0FB3 ₁₆	WED	g	f	e	d	c	b	a	→ P ₁₆
0FB4 ₁₆	MON	g	f	e	d	c	b	a	→ P ₁₅
0FB5 ₁₆	SUN	g	f	e	d	c	b	a	→ P ₁₄
0FB6 ₁₆	—	g	f	e	d	c	b	a	→ P ₁₃
0FB7 ₁₆	■	◀◀	▶▶		▶	REC	SP	EP	→ P ₁₂
0FB8 ₁₆	□□	□□	□□	□□	□□	□□	□□	□□	→ P ₁₁
0FB9 ₁₆	□□	□□	□□	□□	□□	□□	□□	□□	→ P ₁₀
0FBA ₁₆									
0FBB ₁₆									
0FBC ₁₆									
0FBD ₁₆									
0FBE ₁₆									
0FBF ₁₆									
0FC0 ₁₆									→ P ₃₁
0FC1 ₁₆							PM	AM	→ P ₃₀
0FC2 ₁₆								THU	→ P ₁₇
0FC3 ₁₆								TUE	→ P ₁₆
0FC4 ₁₆								:	→ P ₁₅
0FC5 ₁₆								:	→ P ₁₄
0FC6 ₁₆									→ P ₁₃
0FC7 ₁₆									→ P ₁₂
0FC8 ₁₆							L		→ P ₁₁
0FC9 ₁₆							R	LEVEL	→ P ₁₀

 : Unused

(The automatic display is not performed because FLD controller is not used.)

Control procedure:

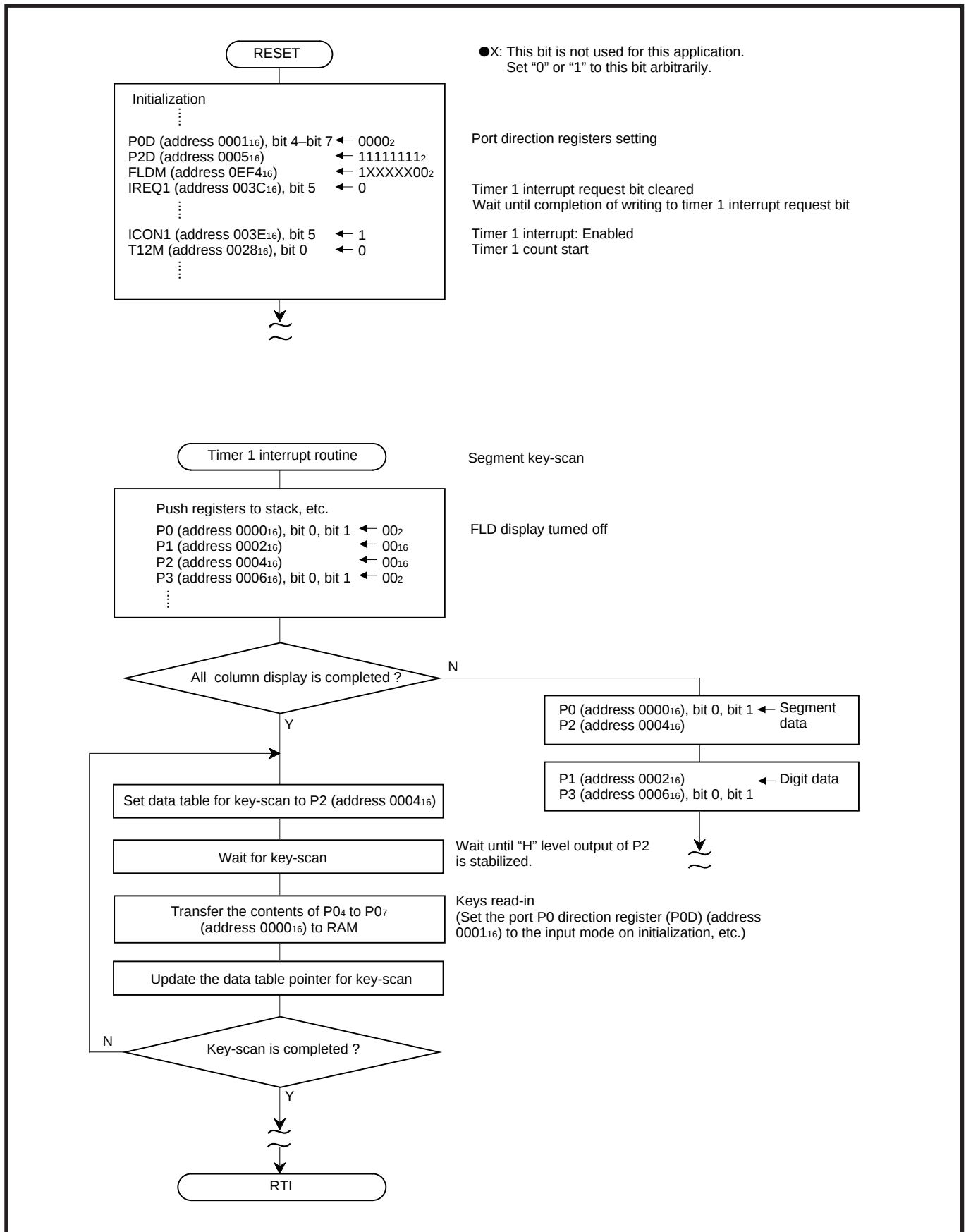


Fig. 2.4.31 Control procedure

APPLICATION

2.4 FLD controller

(4) Display by combination with digit expander (M35501FP*) (basic combination example)

* For M35501FP, refer to section “3.12 M35501FP”.

Outline: The fluorescent display which has many display numbers (36 segments × 16 digits) is displayed by using the digit expander (M35501FP).

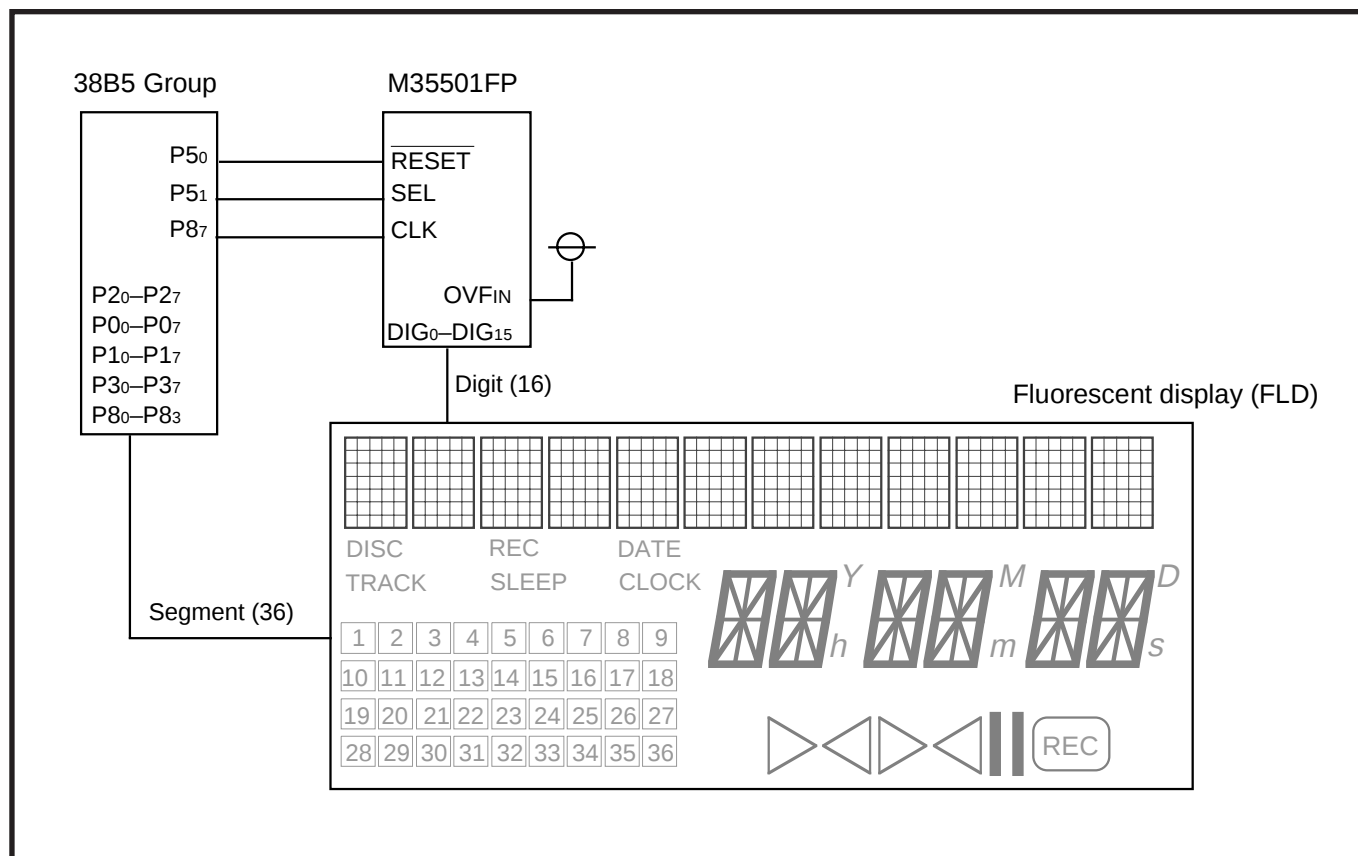


Fig. 2.4.32 Connection diagram

Specifications: •Use of M35501FP (M35501FP: 16 digits, 38B5 Group: 36 segments)

Ports P50 and P51 of 38B5 Group supply signals to the RESET and SEL pins of M35501FP respectively.

The P87 pin (FLD port vacant pin) supply signals to the CLK pin of M35501FP.

•Use of FLD automatic display mode of 38B5 Group

•Display in gradation display mode and 16 timing mode

•Toff1 = 40 μs, Toff2 = 64 μs, Tdisp = 204 μs, f(XIN) = 4 MHz

Figure 2.4.33 shows the timing chart of 38B5 Group and M35501FP, and Figure 2.4.34 shows the timing chart (enlarged view) of digit and segment output.

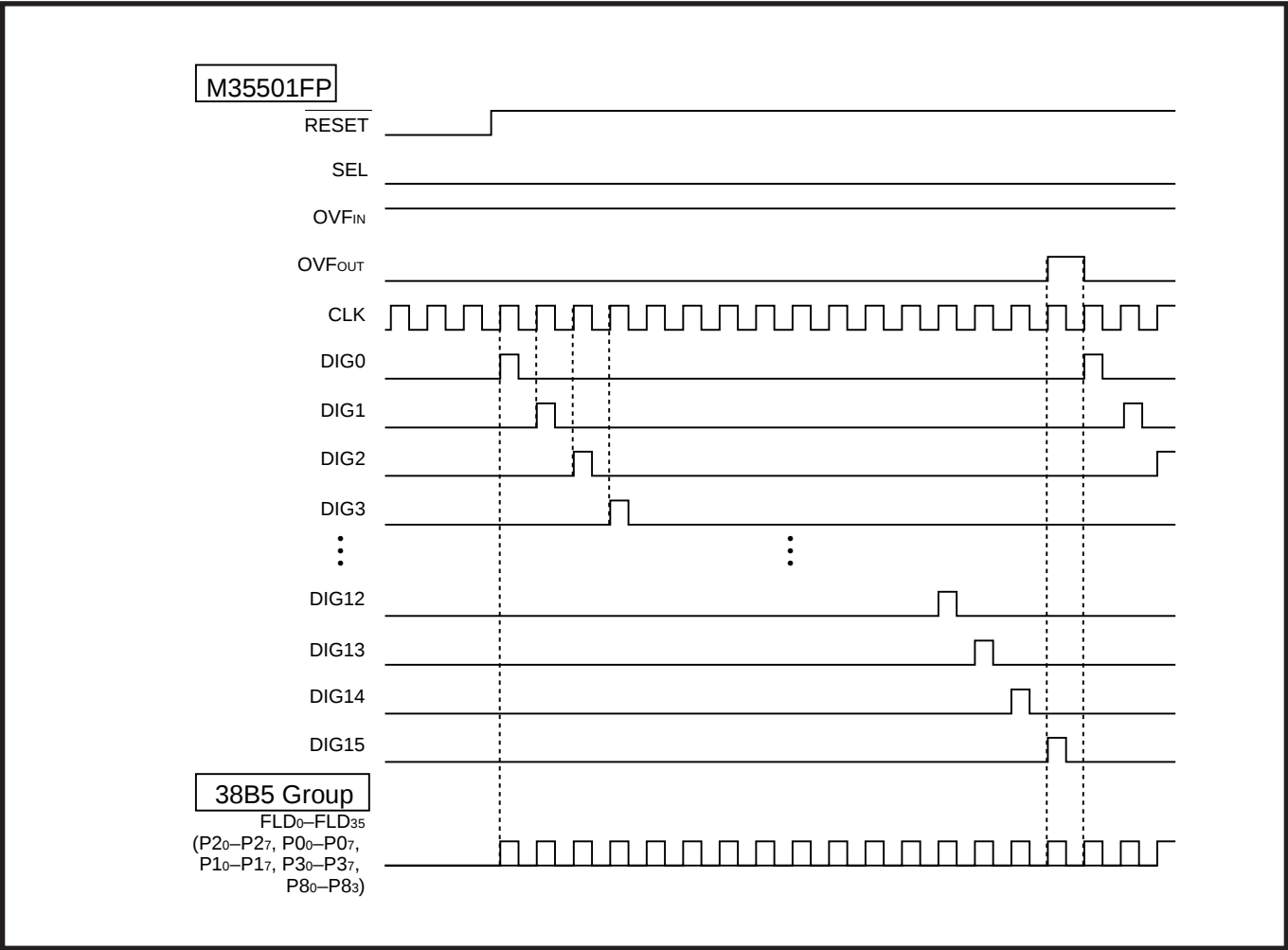


Fig. 2.4.33 Timing chart of 38B5 Group and M35501FP

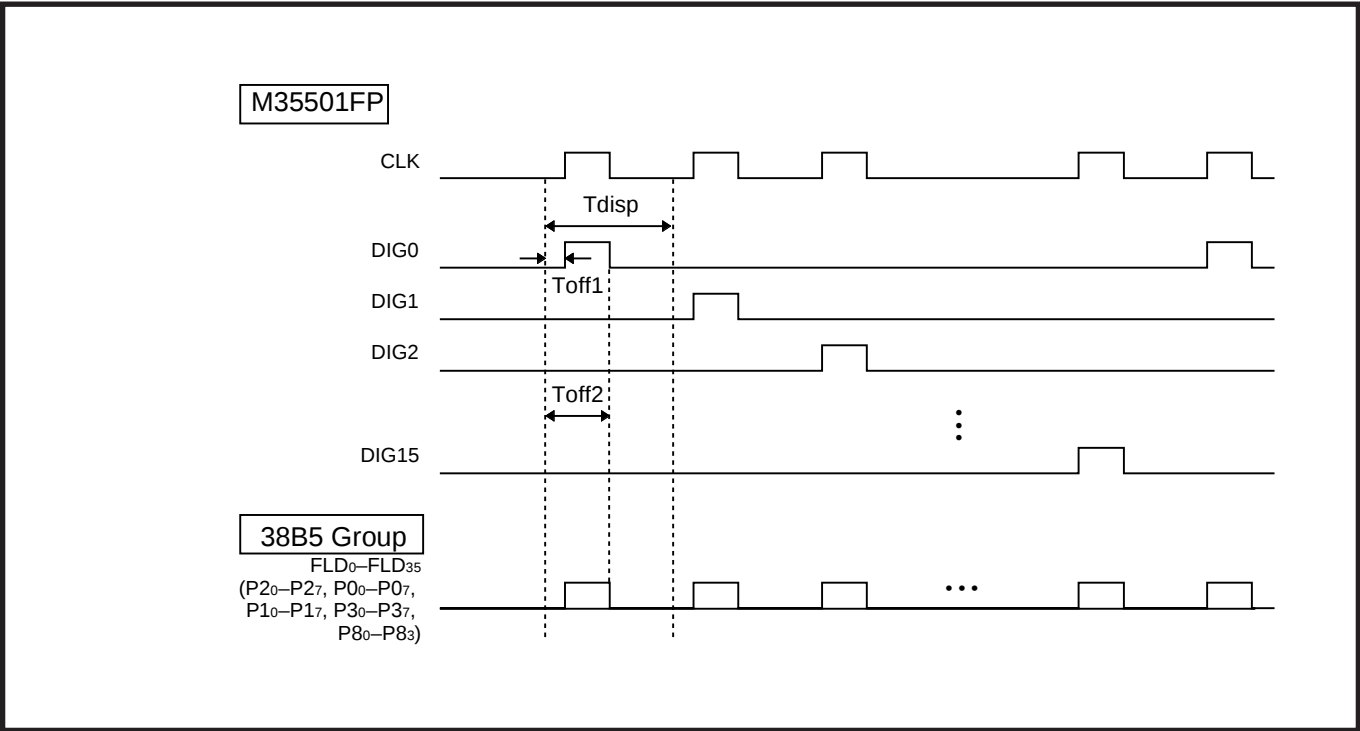
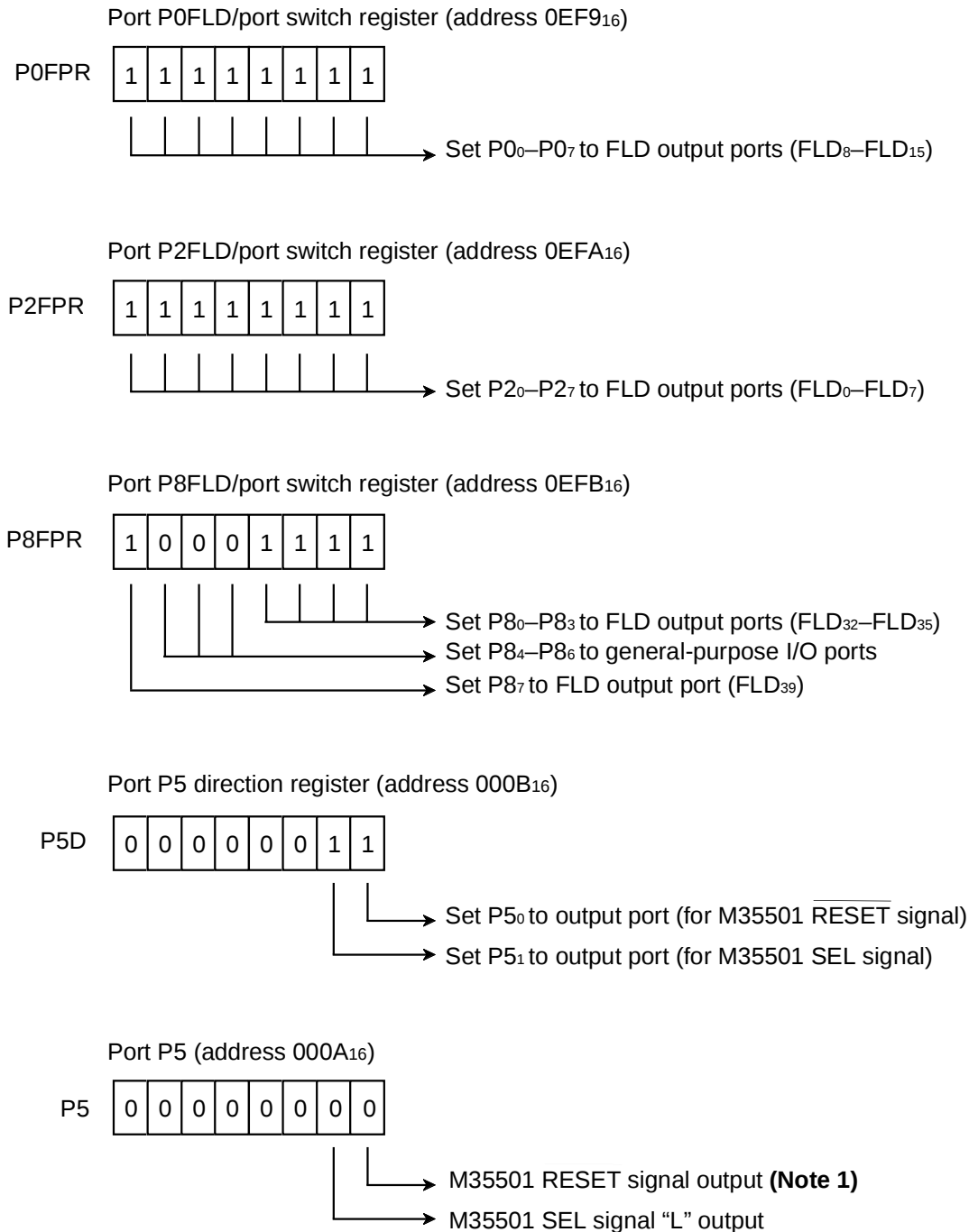


Fig. 2.4.34 Timing chart (enlarged view) of digit and segment output

APPLICATION

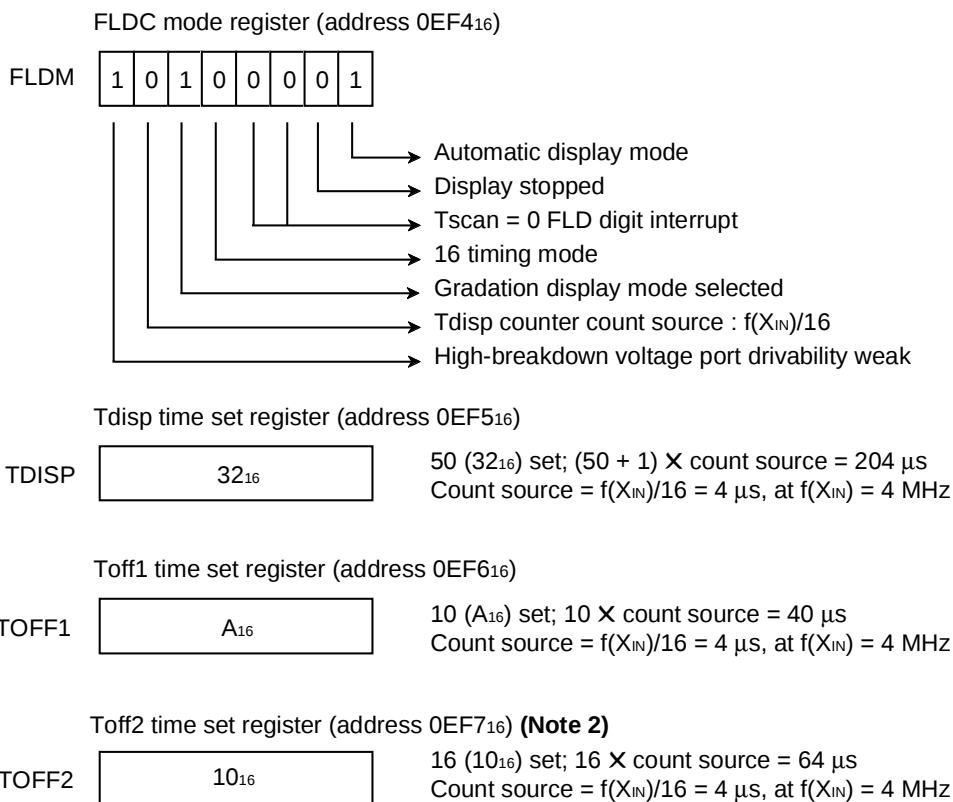
2.4 FLD controller

Figure 2.4.35 shows the setting of relevant registers.

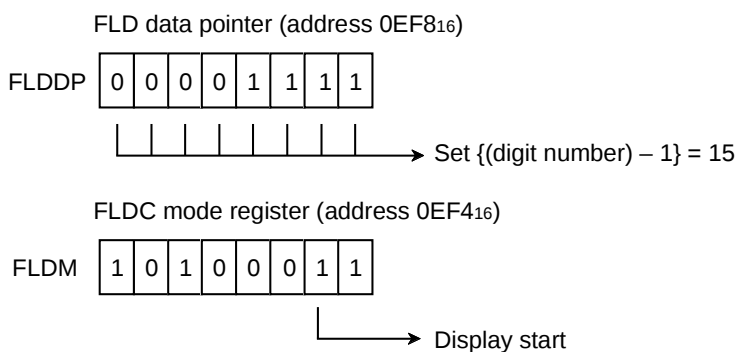


Note 1: After retain $\overline{\text{RESET}}$ signal output “L” for 2 μs or more, release reset by outputting “H” level from RESET signal output at CLK signal = “L” .

Fig. 2.4.35 Setting of relevant registers



Note 2: Perform this setting when the gradation display mode is selected.



APPLICATION

2.4 FLD controller

Setting of FLD automatic display RAM:

Table 2.4.6 FLD automatic display RAM map

1 to 16 timing display data stored area									Gradation display control data stored area									Corresponding digit pin of M35501FP
Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0FB0 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0	0F60 ₁₆	FLD7	FLD6	FLD5	FLD4	FLD3	FLD2	FLD1	FLD0	→ DIG ₁₅
0FB1 ₁₆									0F61 ₁₆									→ DIG ₁₄
0FB2 ₁₆									0F62 ₁₆									→ DIG ₁₃
0FB3 ₁₆									0F63 ₁₆									→ DIG ₁₂
0FB4 ₁₆									0F64 ₁₆									→ DIG ₁₁
0FB5 ₁₆									0F65 ₁₆									→ DIG ₁₀
0FB6 ₁₆									0F66 ₁₆									→ DIG ₉
0FB7 ₁₆									0F67 ₁₆									→ DIG ₈
0FB8 ₁₆									0F68 ₁₆									→ DIG ₇
0FB9 ₁₆									0F69 ₁₆									→ DIG ₆
0FBA ₁₆									0F6A ₁₆									→ DIG ₅
0FBB ₁₆									0F6B ₁₆									→ DIG ₄
0FBC ₁₆									0F6C ₁₆									→ DIG ₃
0FBD ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	0F6D ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	→ DIG ₂
0FBE ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	0F6E ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	→ DIG ₁
0FBF ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	0F6F ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	→ DIG ₀
0FC0 ₁₆	FLD15	FLD14	FLD13	FLD12	FLD11	FLD10	FLD9	FLD8	0F70 ₁₆	FLD15	FLD14	FLD13	FLD12	FLD11	FLD10	FLD9	FLD8	→ DIG ₁₅
0FC1 ₁₆									0F71 ₁₆									→ DIG ₁₄
0FC2 ₁₆									0F72 ₁₆									→ DIG ₁₃
0FC3 ₁₆									0F73 ₁₆									→ DIG ₁₂
0FC4 ₁₆									0F74 ₁₆									→ DIG ₁₁
0FC5 ₁₆									0F75 ₁₆									→ DIG ₁₀
0FC6 ₁₆									0F76 ₁₆									→ DIG ₉
0FC7 ₁₆									0F77 ₁₆									→ DIG ₈
0FC8 ₁₆									0F78 ₁₆									→ DIG ₇
0FC9 ₁₆									0F79 ₁₆									→ DIG ₆
0FCA ₁₆									0F7A ₁₆									→ DIG ₅
0FCB ₁₆									0F7B ₁₆									→ DIG ₄
0FCC ₁₆									0F7C ₁₆									→ DIG ₃
0FCD ₁₆									0F7D ₁₆									→ DIG ₂
0FCE ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	0F7E ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	→ DIG ₁
0CFE ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	0F7F ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	→ DIG ₀
0FD0 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16	0F80 ₁₆	FLD23	FLD22	FLD21	FLD20	FLD19	FLD18	FLD17	FLD16	→ DIG ₁₅
0FD1 ₁₆									0F81 ₁₆									→ DIG ₁₄
0FD2 ₁₆									0F82 ₁₆									→ DIG ₁₃
0FD3 ₁₆									0F83 ₁₆									→ DIG ₁₂
0FD4 ₁₆									0F84 ₁₆									→ DIG ₁₁
0FD5 ₁₆									0F85 ₁₆									→ DIG ₁₀
0FD6 ₁₆									0F86 ₁₆									→ DIG ₉
0FD7 ₁₆									0F87 ₁₆									→ DIG ₈
0FD8 ₁₆									0F88 ₁₆									→ DIG ₇
0FD9 ₁₆									0F89 ₁₆									→ DIG ₆
0FDA ₁₆									0F8A ₁₆									→ DIG ₅
0FDB ₁₆									0F8B ₁₆									→ DIG ₄
0FDC ₁₆									0F8C ₁₆									→ DIG ₃
0FDD ₁₆									0F8D ₁₆									→ DIG ₂
0FDE ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	0F8E ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	→ DIG ₁
0FDE ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	0F8F ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	→ DIG ₀
0FE0 ₁₆	FLD31	FLD30	FLD29	FLD28	FLD27	FLD26	FLD25	FLD24	0F90 ₁₆	FLD31	FLD30	FLD29	FLD28	FLD27	FLD26	FLD25	FLD24	→ DIG ₁₅
0FE1 ₁₆									0F91 ₁₆									→ DIG ₁₄
0FE2 ₁₆									0F92 ₁₆									→ DIG ₁₃
0FE3 ₁₆									0F93 ₁₆									→ DIG ₁₂
0FE4 ₁₆									0F94 ₁₆									→ DIG ₁₁
0FE5 ₁₆									0F95 ₁₆									→ DIG ₁₀
0FE6 ₁₆									0F96 ₁₆									→ DIG ₉
0FE7 ₁₆									0F97 ₁₆									→ DIG ₈
0FE8 ₁₆									0F98 ₁₆									→ DIG ₇
0FE9 ₁₆									0F99 ₁₆									→ DIG ₆
0FEA ₁₆									0F9A ₁₆									→ DIG ₅
0FEB ₁₆									0F9B ₁₆									→ DIG ₄
0FEC ₁₆									0F9C ₁₆									→ DIG ₃
0FED ₁₆									0F9D ₁₆									→ DIG ₂
0FEE ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	0F9E ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	→ DIG ₁
0FEE ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	0F9F ₁₆	▼	▼	▼	▼	▼	▼	▼	▼	→ DIG ₀
0FF0 ₁₆	1	1	1	1	1	1	1	1	0FA0 ₁₆	1	1	1	1	1	1	1	1	→ DIG ₁₅
0FF1 ₁₆	1	1	1	1	1	1	1	1	0FA1 ₁₆	1	1	1	1	1	1	1	1	→ DIG ₁₄
0FF2 ₁₆	1	1	1	1	1	1	1	1	0FA2 ₁₆	1	1	1	1	1	1	1	1	→ DIG ₁₃
0FF3 ₁₆	1	1	1	1	1	1	1	1	0FA3 ₁₆	1	1	1	1	1	1	1	1	→ DIG ₁₂
0FF4 ₁₆	1	1	1	1	1	1	1	1	0FA4 ₁₆	1	1	1	1	1	1	1	1	→ DIG ₁₁
0FF5 ₁₆	1	1	1	1	1	1	1	1	0FA5 ₁₆	1	1	1	1	1	1	1	1	→ DIG ₁₀
0FF6 ₁₆	1	1	1	1	1	1	1	1	0FA6 ₁₆	1	1	1	1	1	1	1	1	→ DIG ₉
0FF7 ₁₆	1	1	1	1	1	1	1	1	0FA7 ₁₆	1	1	1	1	1	1	1	1	→ DIG ₈
0FF8 ₁₆	1	1	1	1	1	1	1	1	0FA8 ₁₆	1	1	1	1	1	1	1	1	→ DIG ₇
0FF9 ₁₆	1	1	1	1	1	1	1	1	0FA9 ₁₆	1	1	1	1	1	1	1	1	→ DIG ₆
0FFA ₁₆	1	1	1	1	1	1	1	1	0FAA ₁₆	1	1	1	1	1	1	1	1	→ DIG ₅
0FFB ₁₆	1	1	1	1	1	1	1	1	0FAB ₁₆	1	1	1	1	1	1	1	1	→ DIG ₄
0FFC ₁₆	1	1	1	1	1	1	1	1	0FAC ₁₆	1	1	1	1	1	1	1	1	→ DIG ₃
0FFD ₁₆	1	1	1	1	1	1	1	1	0FAD ₁₆	1	1	1	1	1	1	1	1	→ DIG ₂
0FFE ₁₆	1	1	1	1	1	1	1	1	0FAE ₁₆	1	1	1	1	1	1	1	1	→ DIG ₁
0FFF ₁₆	1	1	1	1	1	1	1	1	0FAF ₁₆	1	1	1	1	1	1	1	1	→ DIG ₀

 : CLK signal set area to M35501FP
 : Unused

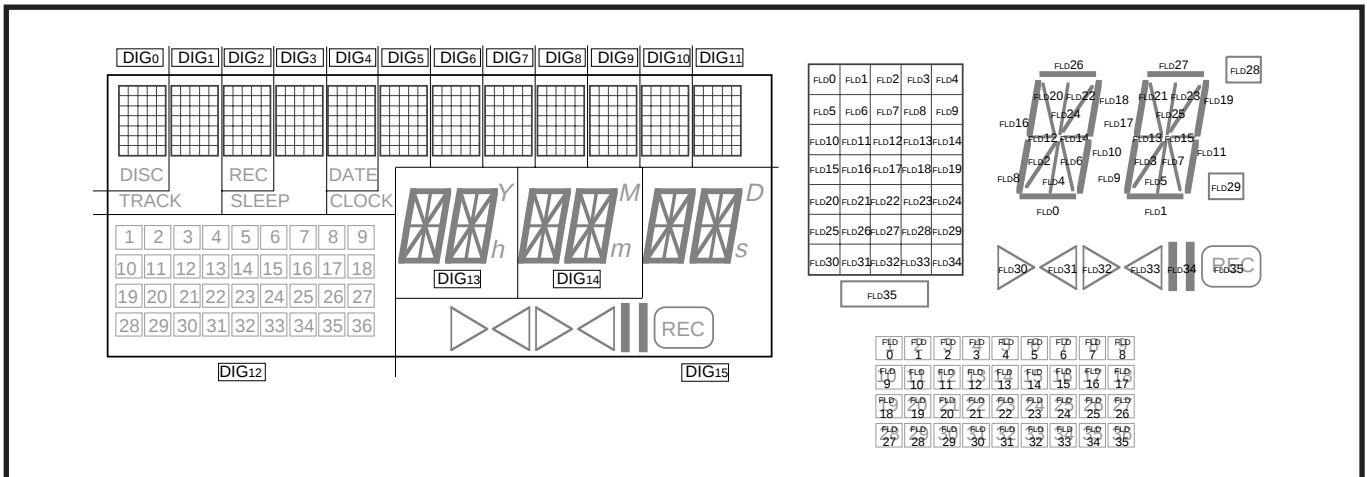


Fig. 2.4.36 FLD digit allocation example

Control procedure:

Figure 2.4.37 shows the control procedure.

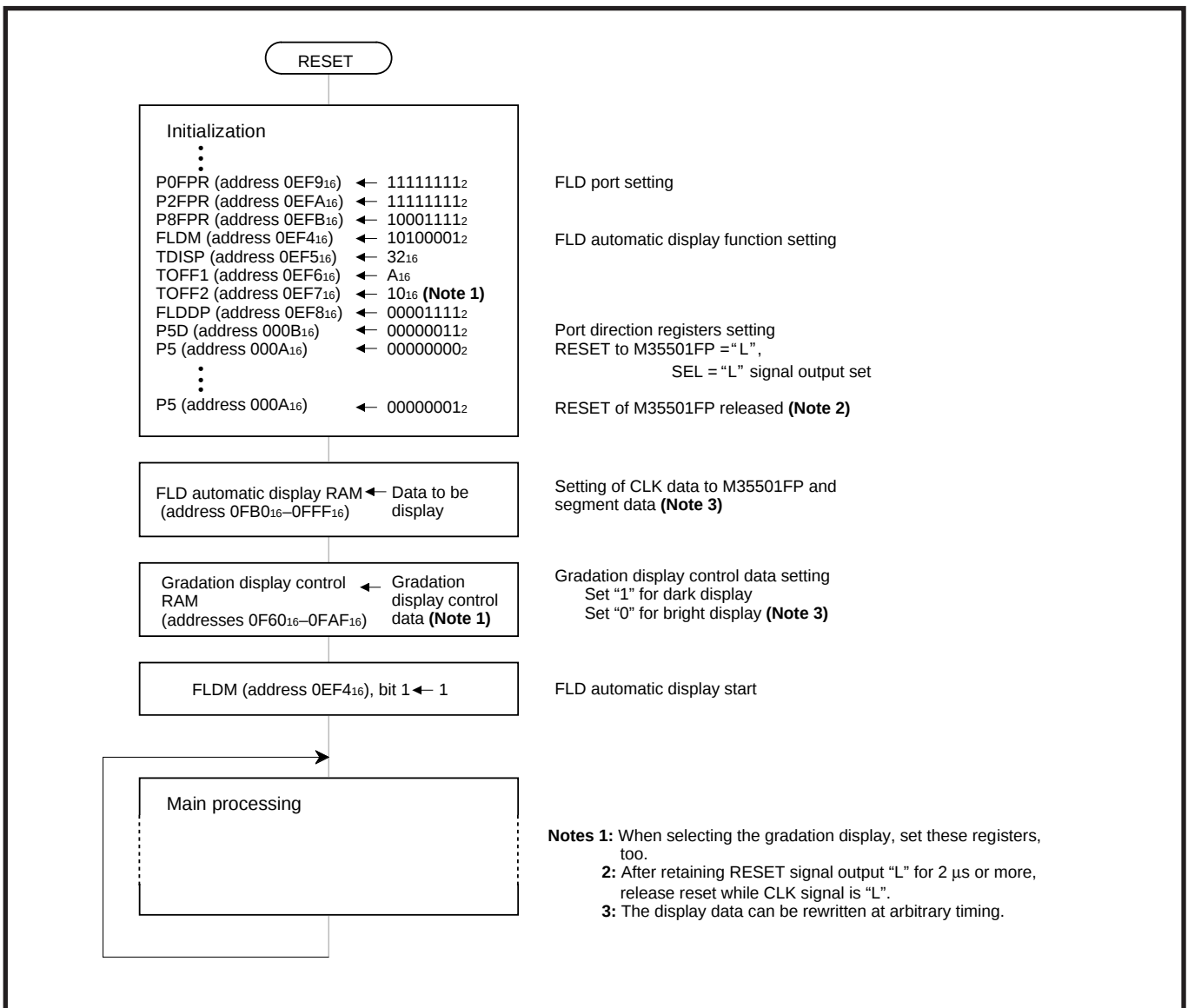


Fig. 2.4.37 Control procedure

APPLICATION

2.4 FLD controller

(5) Display by combination with digit expander (M35501FP*) (example considering column discrepancy prevention)

* For M35501FP, refer to section “3.12 M35501FP”.

Outline: In the case of (4), which is displayed by using the digit expander (M35501FP), if a noise enters signals between 38B5 Group and M35501FP, a column discrepancy of display may occur. Prevent the column discrepancy by using the OVF_{OUT} output of M35501FP.

The OVF_{OUT} pin of M35501FP outputs an overflow signal. The overflow signal is the signal which outputs “H” synchronizing to the last digit output signal of M35501FP, and the signal is output at definite intervals in the correct state. Incorrect state is detected by measuring the output period of this signal, and a column discrepancy is prevented.

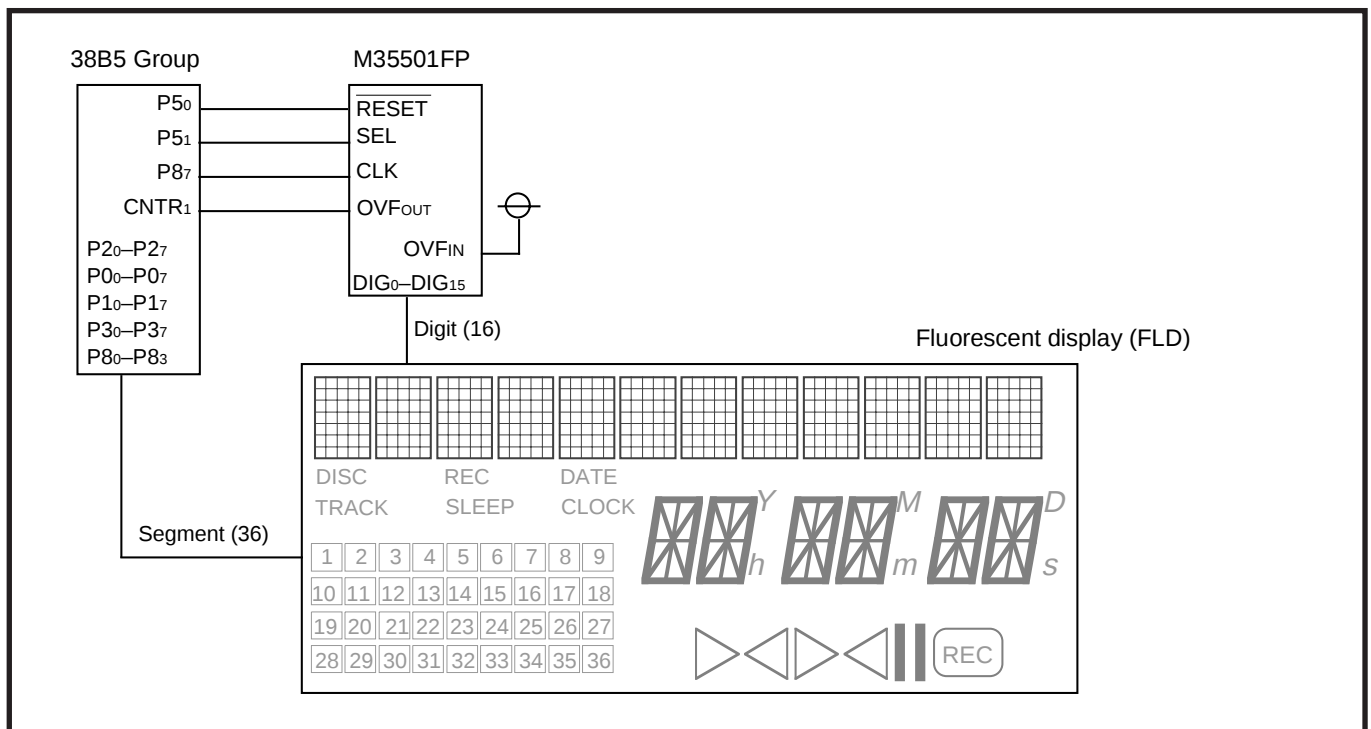


Fig. 2.4.38 Connection diagram

Specifications: •Use of M35501FP (M35501: 16 digits, 38B5 Group: 36 segments)

Ports P5₀ and P5₁ of 38B5 Group supply signal to the RESET and SEL pins of M35501FP respectively.

The P8₇ pin (FLD port vacant pin) supply signals to the CLK pin of M35501FP.

•Use of FLD automatic display mode of 38B5 Group

•Display in gradation display mode and 16 timing mode

•Toff1 = 40 μs, Toff2 = 64 μs, Tdisp = 204 μs, f(X_{IN}) = 4 MHz

Countermeasures against column discrepancy → •OVF_{OUT} output of M35501FP input to CNTR₁ pin of 38B5 Group
Input signal to CNTR₁ pin is counted as a count source by timer 4 of 38B5 Group

The timer 6 interrupt is generated each time FLD display period (Tdisp (204 μs) × 16 column = 3.264 ms), and a value of timer 4 is confirmed. M35501FP is reset at incorrect state.

Figure 2.4.39 shows the timing chart (at correct state) of 38B5 Group and M35501FP, and Figure 2.4.40 shows the timing chart (at incorrect state) of 38B5 Group and M35501FP.

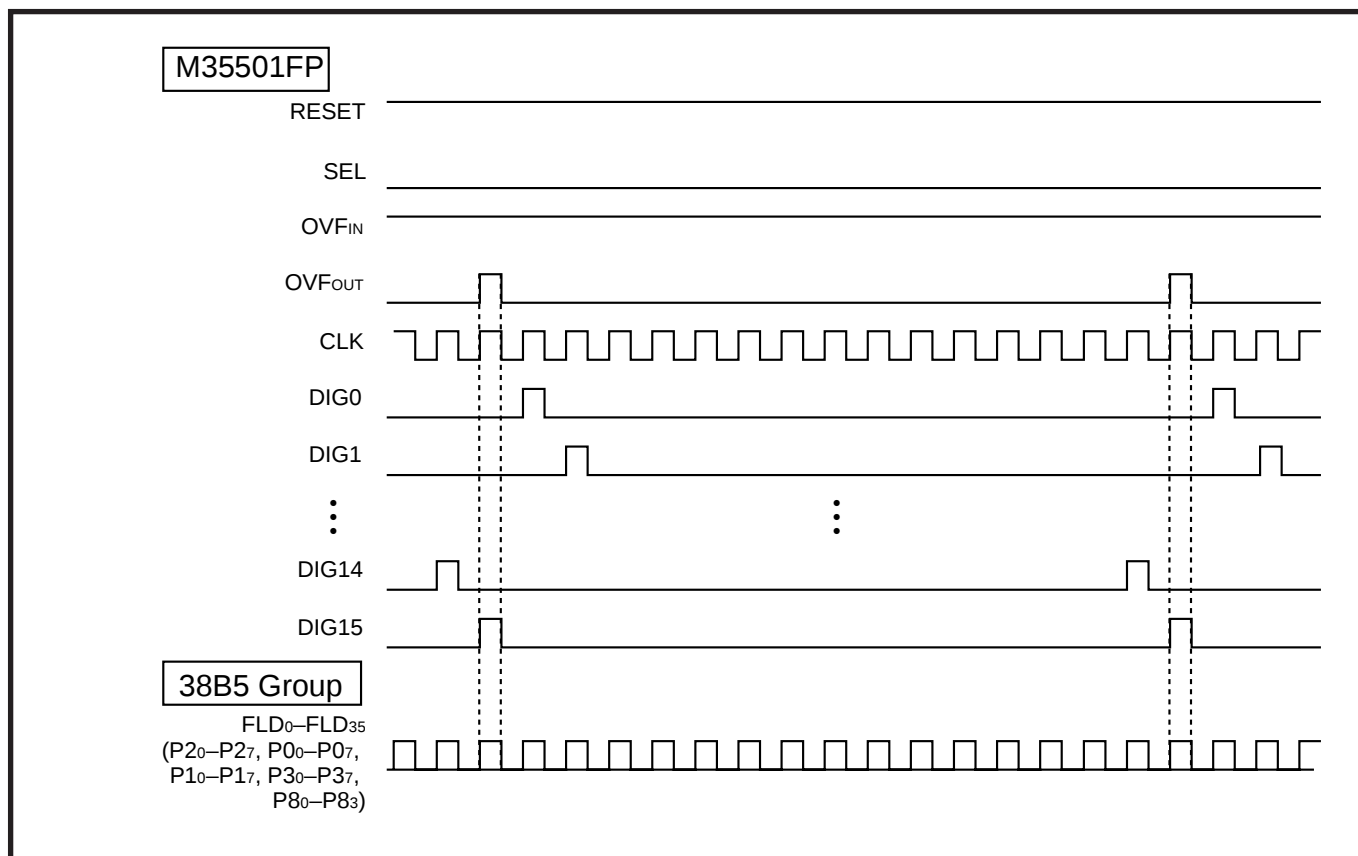


Fig. 2.4.39 Timing chart (at correct state) of 38B5 Group and M35501FP

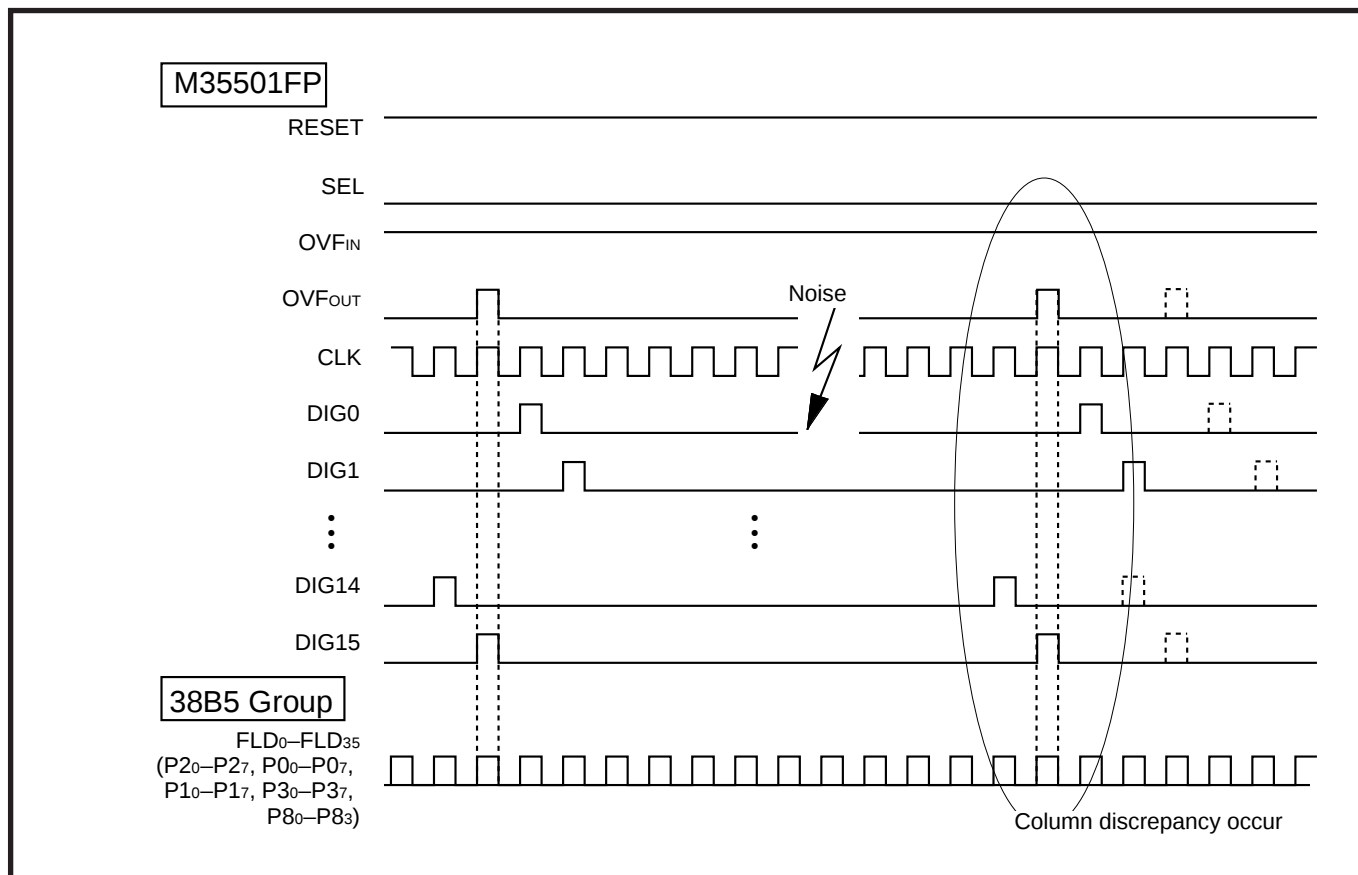


Fig. 2.4.40 Timing chart (at incorrect state) of 38B5 Group and M35501FP

2.4 FLD controller

Figure 2.4.41 shows the setting of relevant registers.

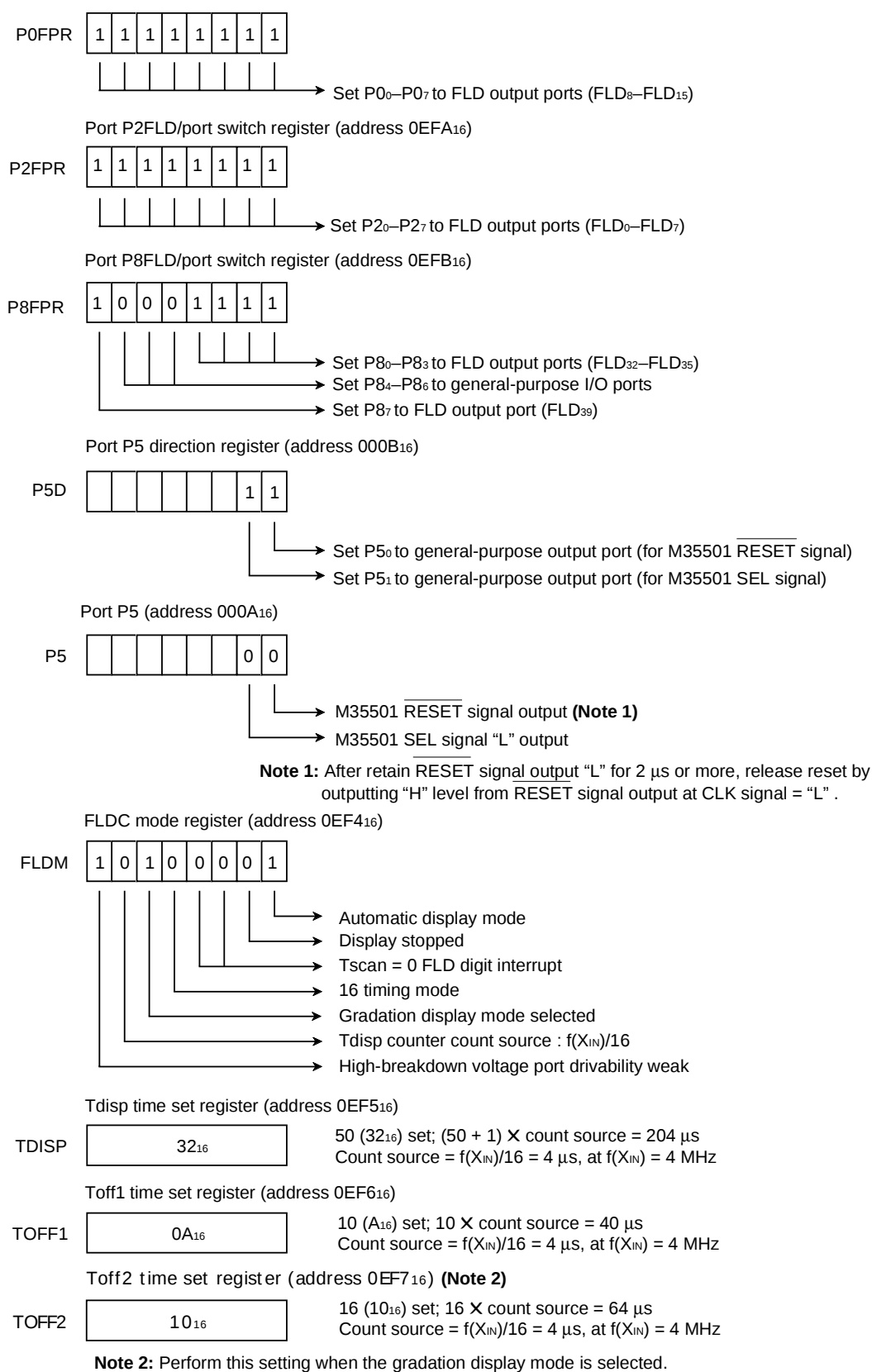
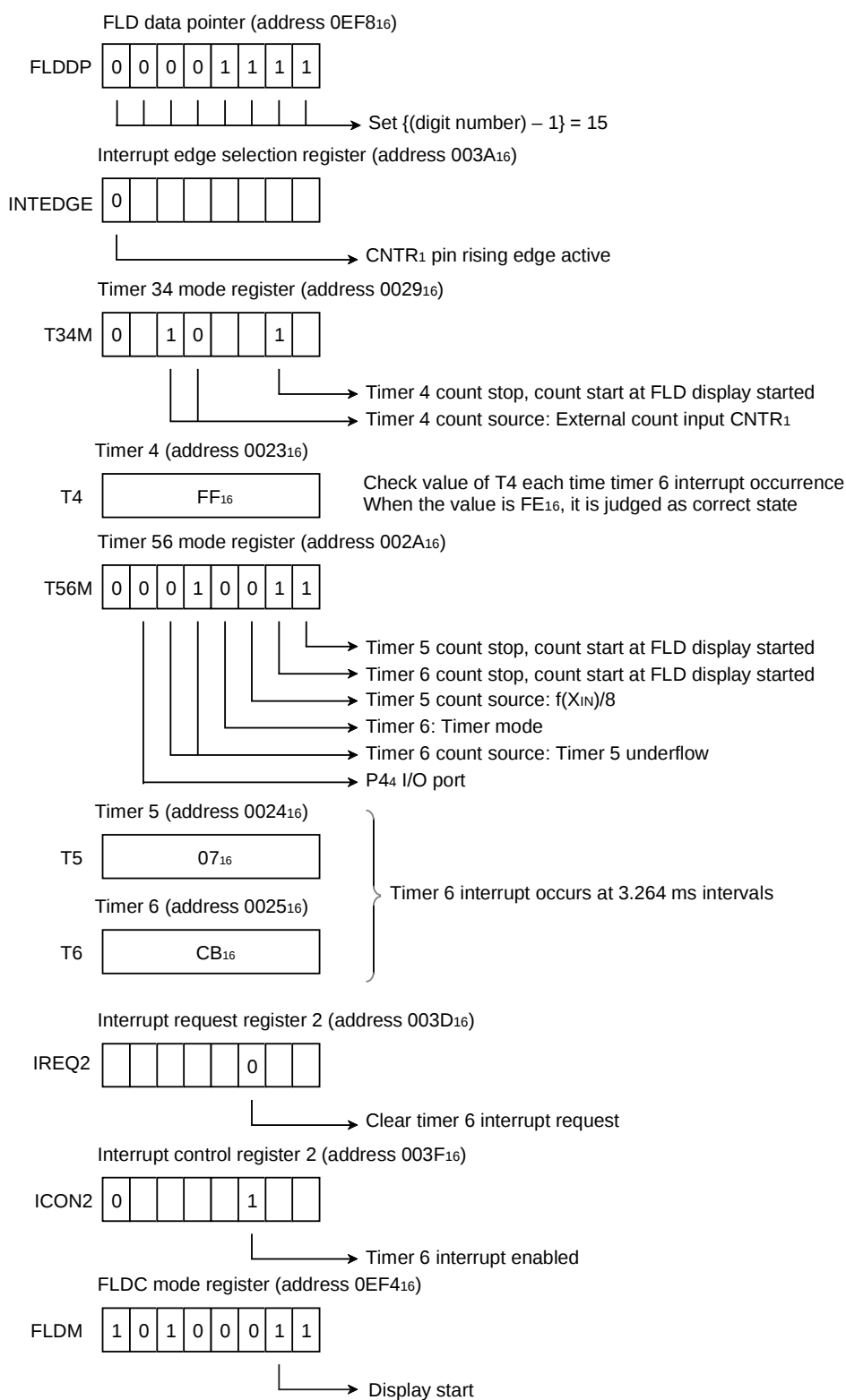


Fig. 2.4.41 Setting of relevant registers

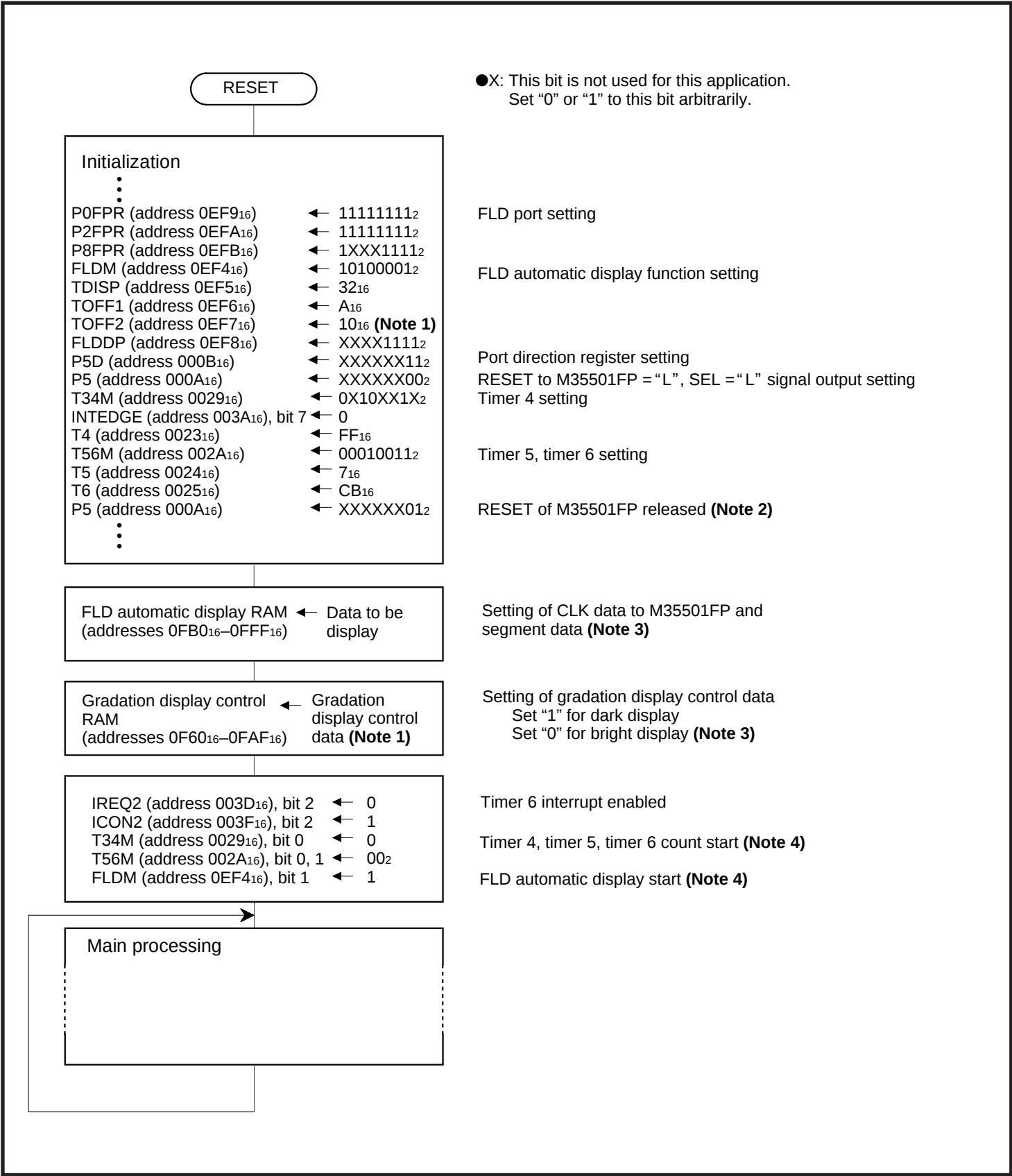


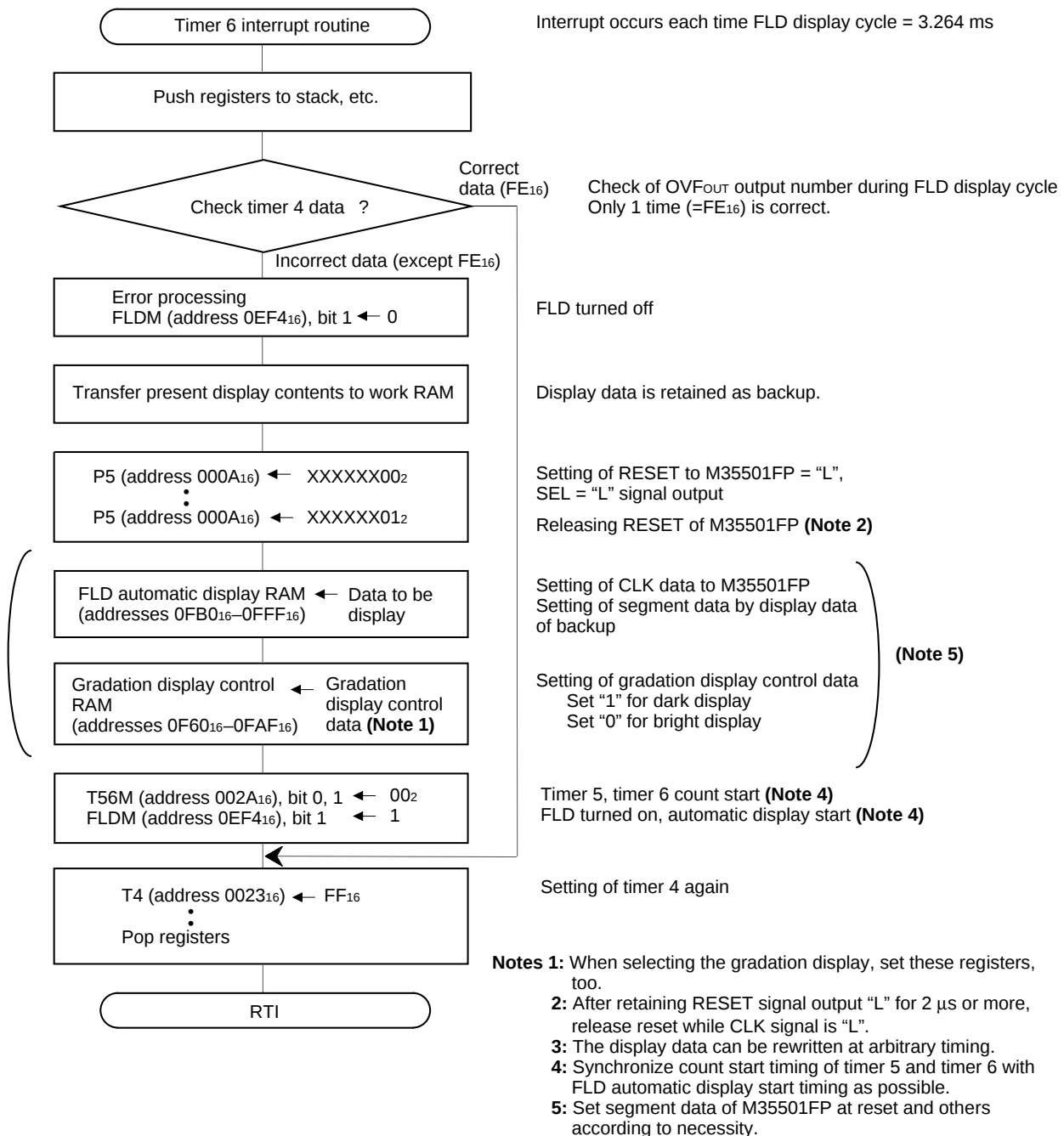
APPLICATION

2.4 FLD controller

Control procedure:

Figure 2.4.42 shows the control procedure.





APPLICATION

2.4 FLD controller

2.4.4 Notes on use

- Set a value of 03₁₆ or more to the Toff1 time set register.
- When displaying in the gradation display mode, select the 16 timing mode by the timing number control bit (bit 4 of FLDC mode register (address 0EF4₁₆) = "0").

2.5 A-D converter

This paragraph describes the setting method of A-D converter relevant registers, notes etc.

2.5.1 Memory assignment

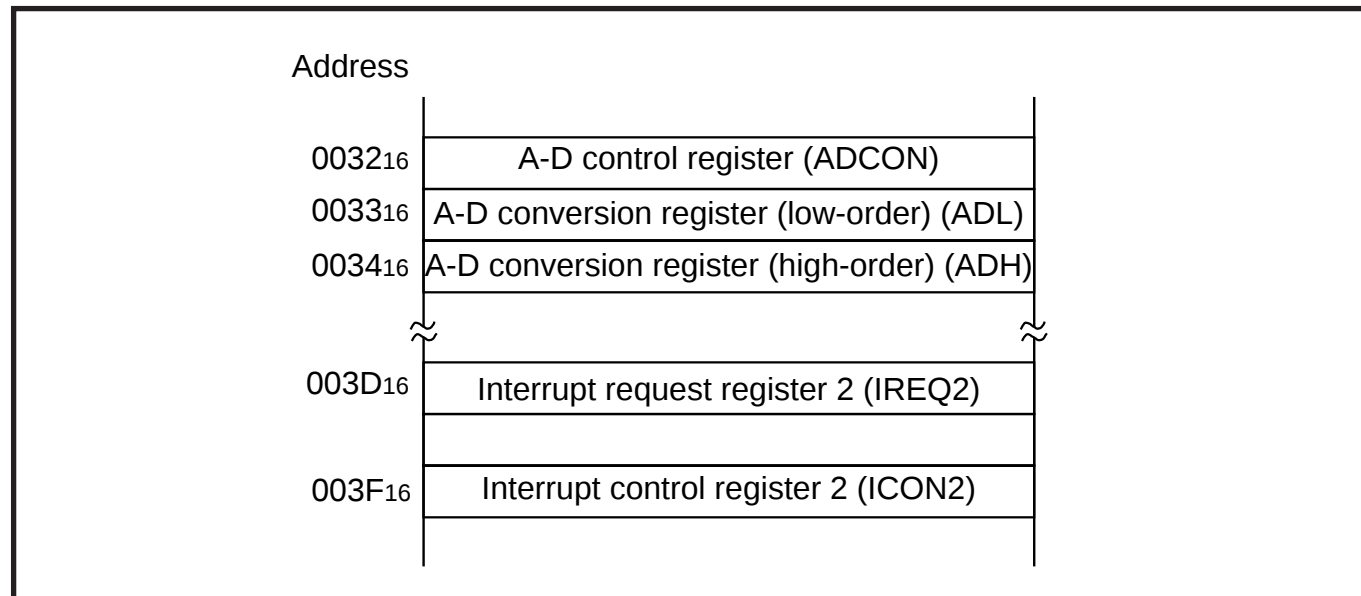


Fig. 2.5.1 Memory assignment of A-D converter relevant registers

2.5.2 Relevant registers

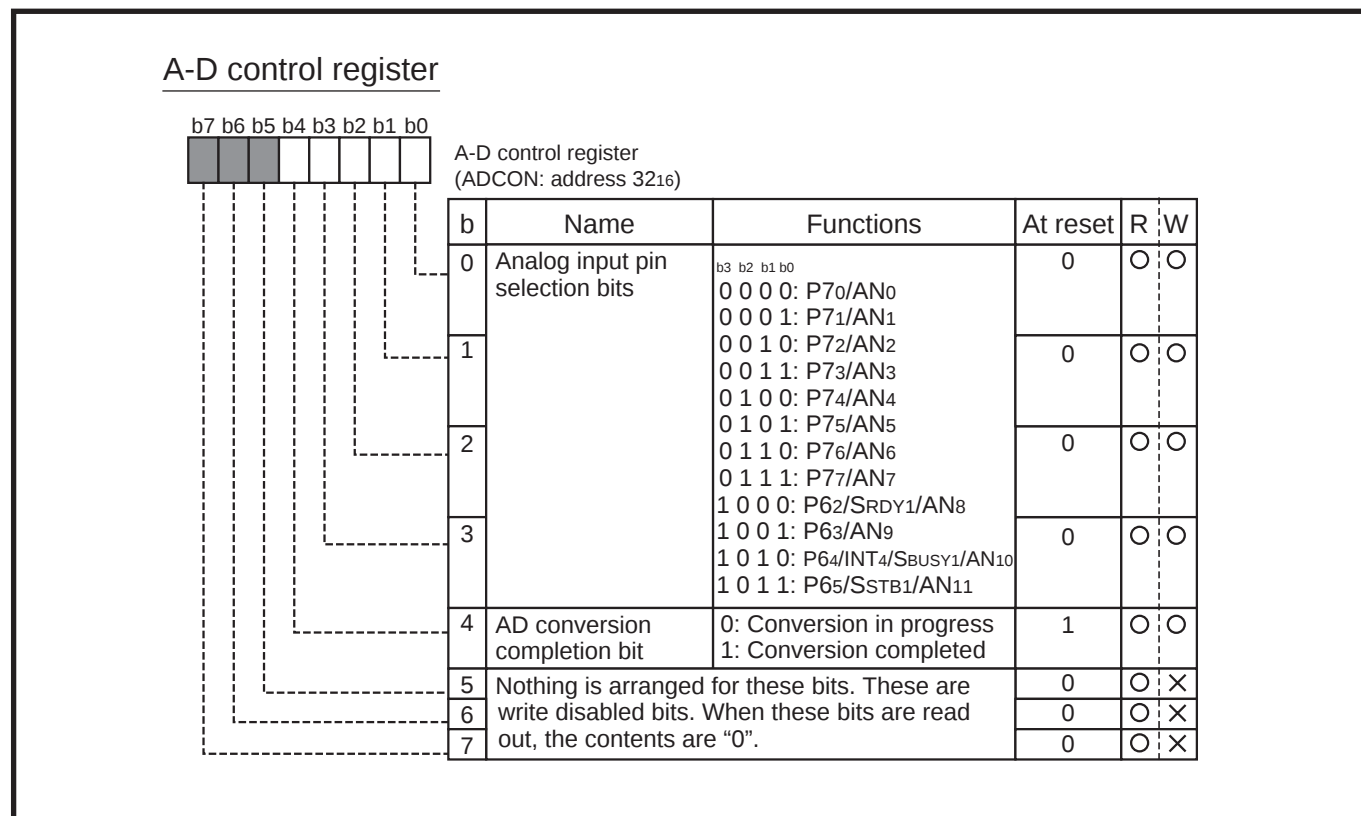


Fig. 2.5.2 Structure of A-D control register

APPLICATION

2.5 A-D converter

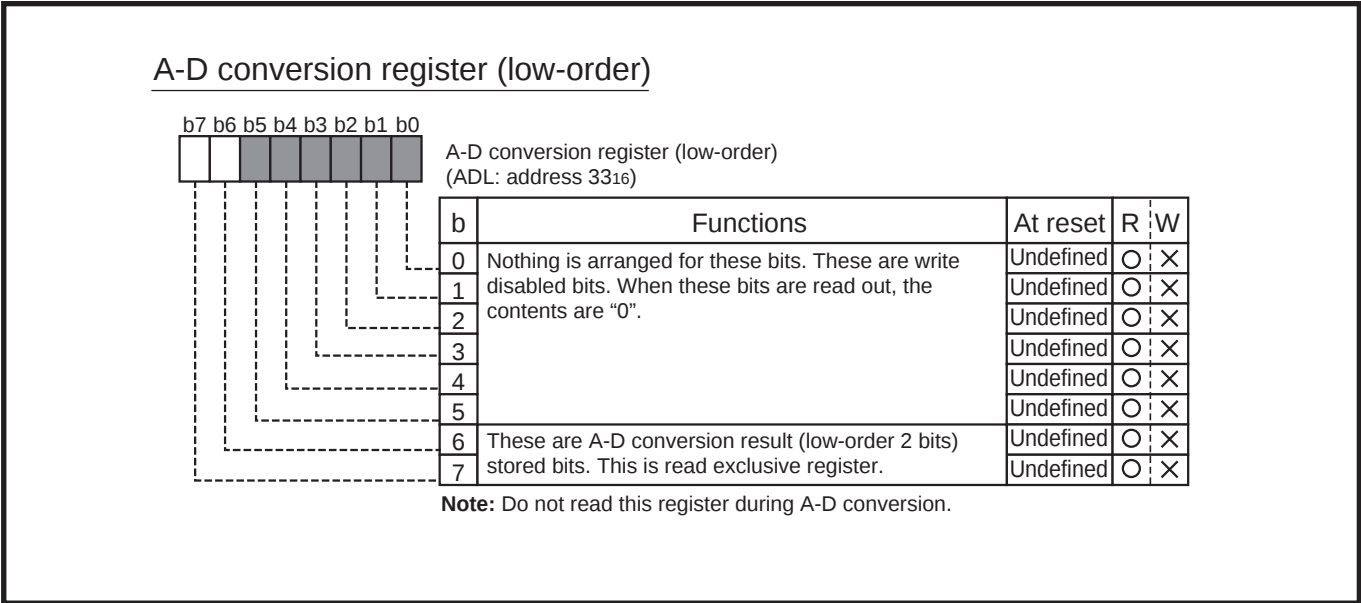


Fig. 2.5.3 Structure of A-D conversion register (low-order)

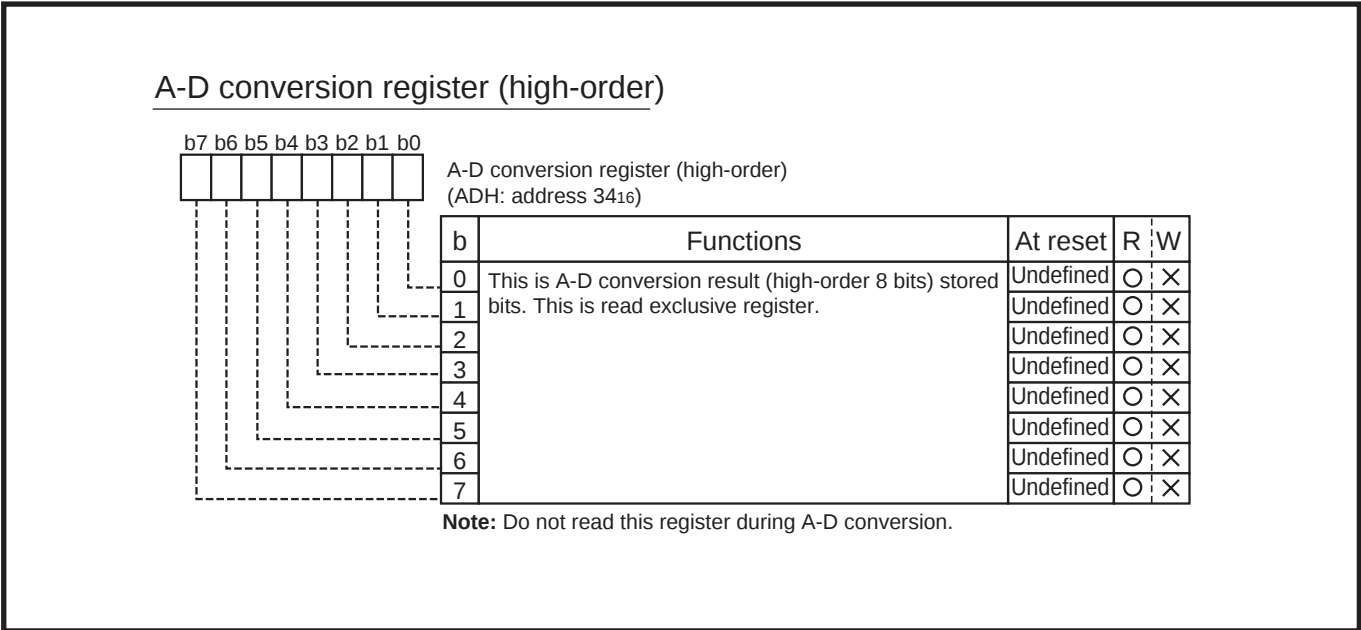
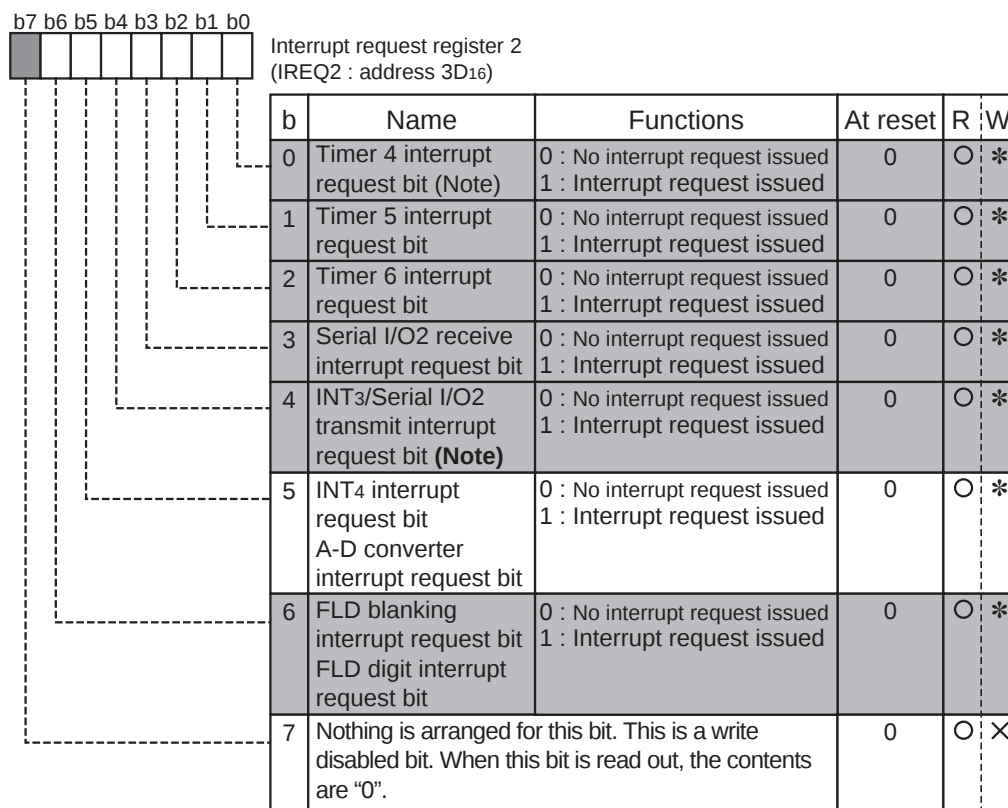


Fig. 2.5.4 Structure of A-D conversion register (high-order)

Interrupt request register 2



*: "0" can be set by software, but "1" cannot be set.

Note: In the mask option type P, if timer 4 interrupt whose count source is CNTR1 input and INT3 interrupt are selected, these bits do not become "1".

Fig. 2.5.5 Structure of interrupt request register 2

APPLICATION

2.5 A-D converter

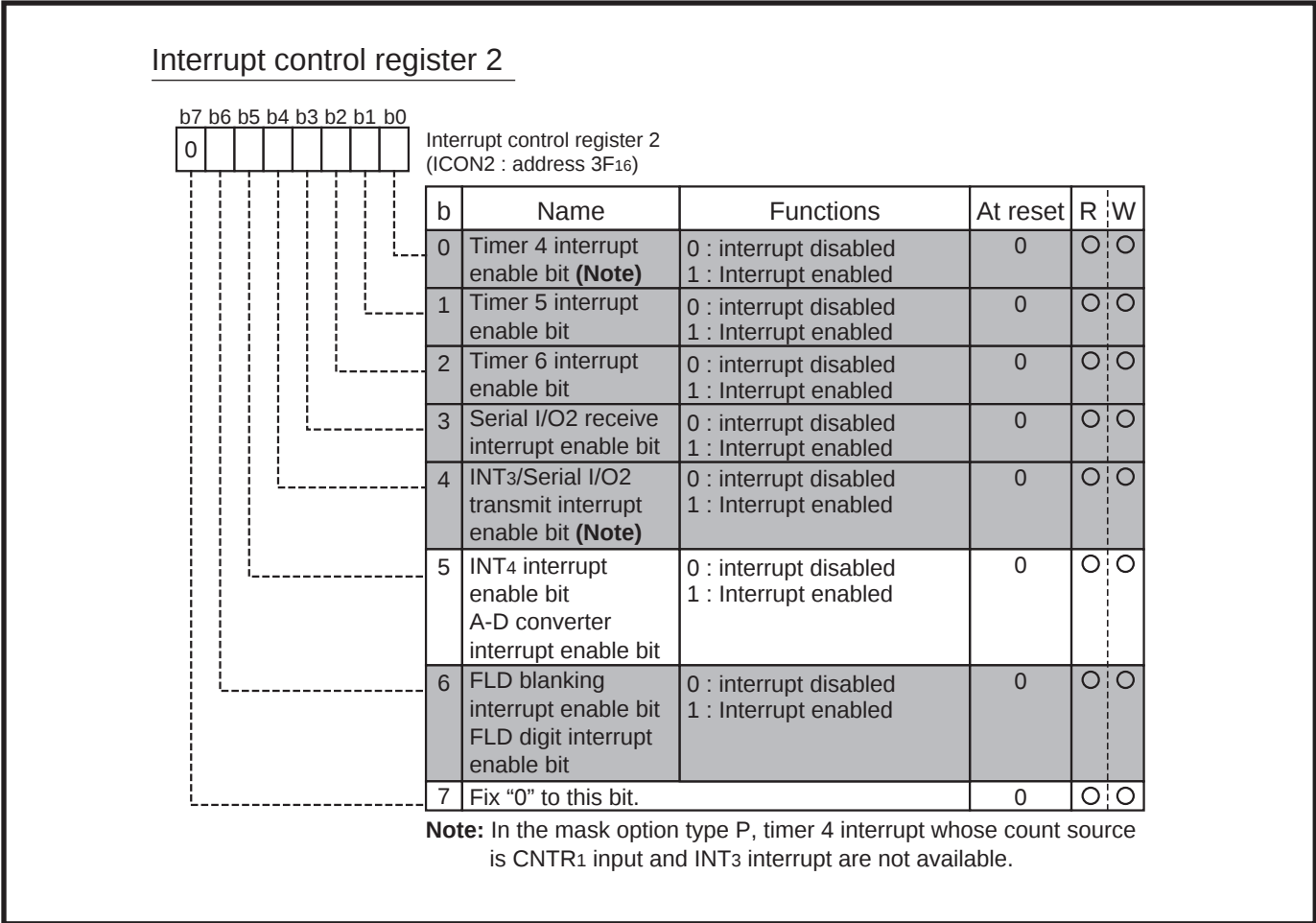


Fig. 2.5.6 Structure of interrupt control register 2

2.5.3 A-D converter application examples

(1) Read-in of analog signal

Outline: The analog input voltage input from a sensor is converted to digital values.

Figure 2.5.7 shows a connection diagram, and Figure 2.5.8 shows the setting of relevant registers.

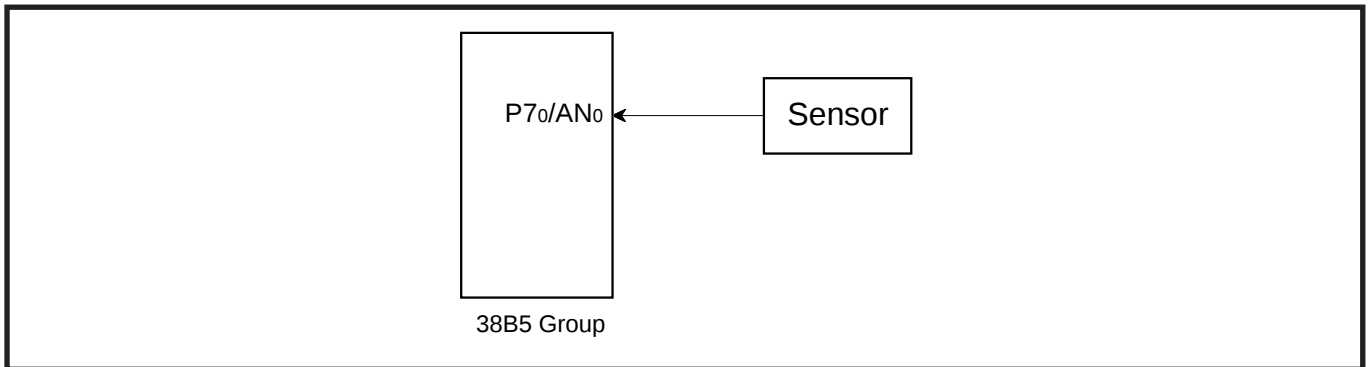


Fig. 2.5.7 Connection diagram

Specifications:

- Conversion of analog input voltage input from sensor to digital values
- Use of P70/AN0 pin as analog input pin

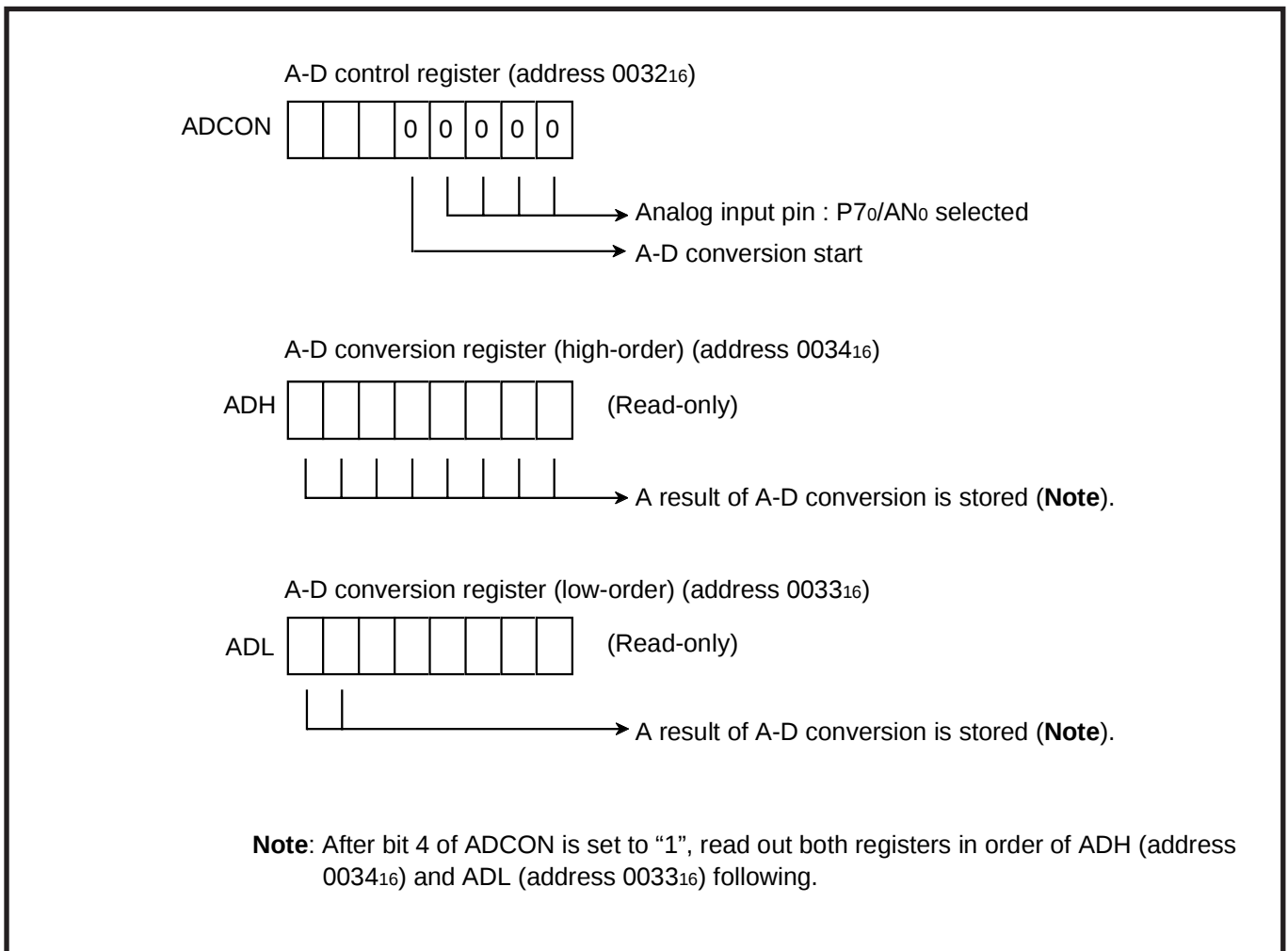


Fig. 2.5.8 Setting of relevant registers

APPLICATION

2.5 A-D converter

Control procedure: A-D converter is started by performing register setting shown Figure 2.5.8. Figure 2.5.9 shows the control procedure.

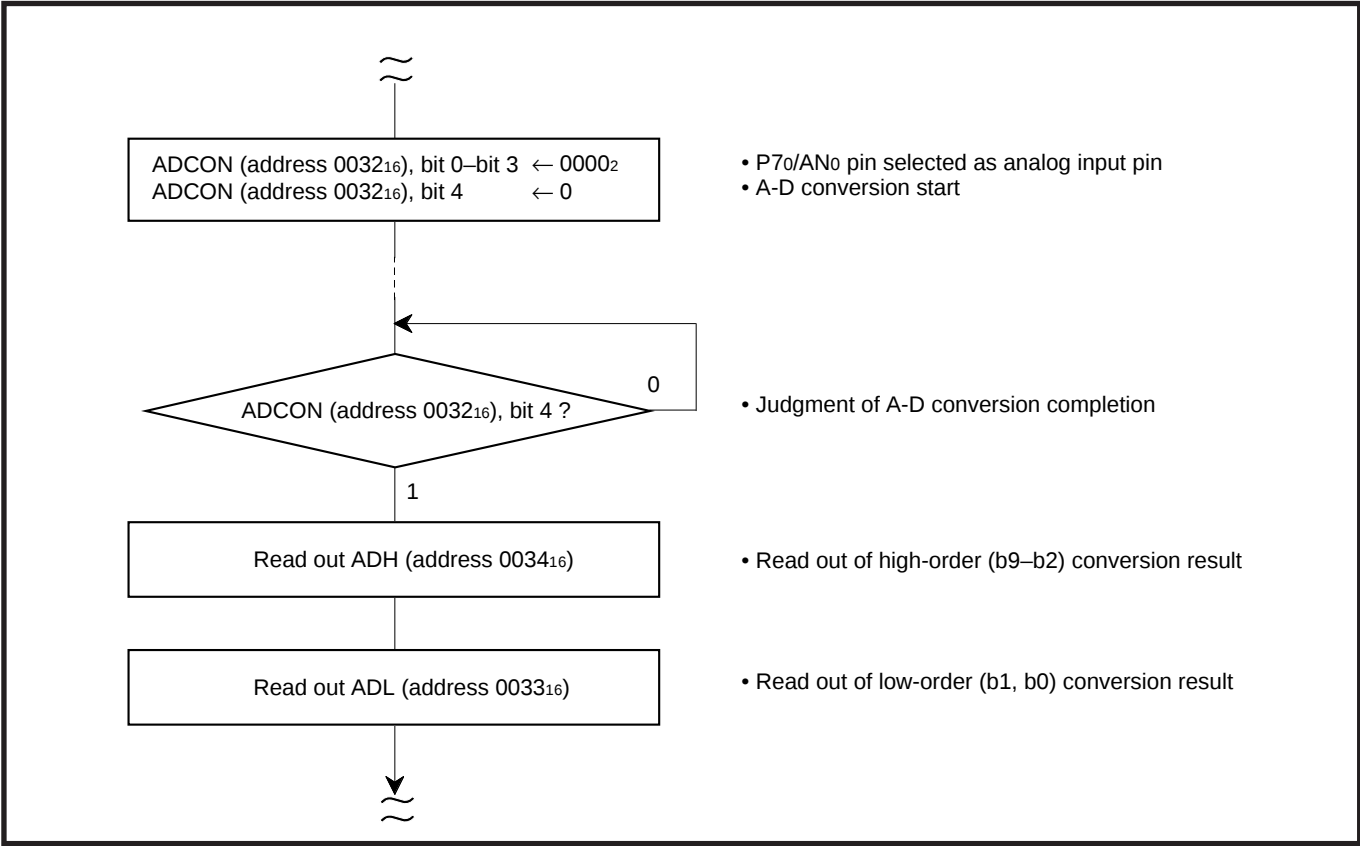


Fig. 2.5.9 Control procedure

2.5.4 Notes on use

(1) Analog input pin

- Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 μF to 1 μF . Further, be sure to verify the operation of application products on the user side.

● Reason

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A-D conversion precision to be worse.

- When the P64/INT4/SBUSY1/AN10 pin is selected as analog input pin, external interrupt function (INT4) becomes invalid.

(2) A-D converter power source pin

The AVss pin is A-D converter power source pin. Regardless of using the A-D conversion function or not, connect it as following :

- AVss : Connect to the Vss line

● Reason

If the AVss pin is opened, the microcomputer may have a failure because of noise or others.

(3) Clock frequency during A-D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. Thus, make sure the following during an A-D conversion.

- $f(X_{IN})$ is 250 kHz or more
- Use clock divided by main clock ($f(X_{IN})$) as internal system clock.
- Do not execute the **STP** instruction and **WIT** instruction

APPLICATION

2.6 PWM

2.6 PWM

This paragraph describes the setting method of PWM relevant registers, notes etc.

2.6.1 Memory assignment

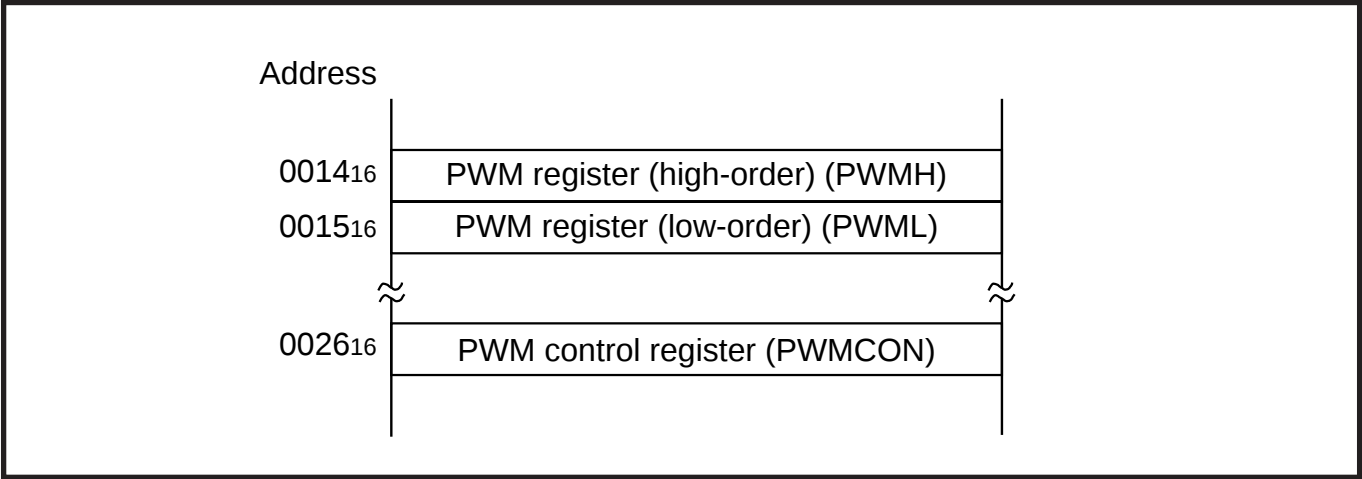


Fig. 2.6.1 Memory assignment of PWM relevant registers

2.6.2 Relevant registers

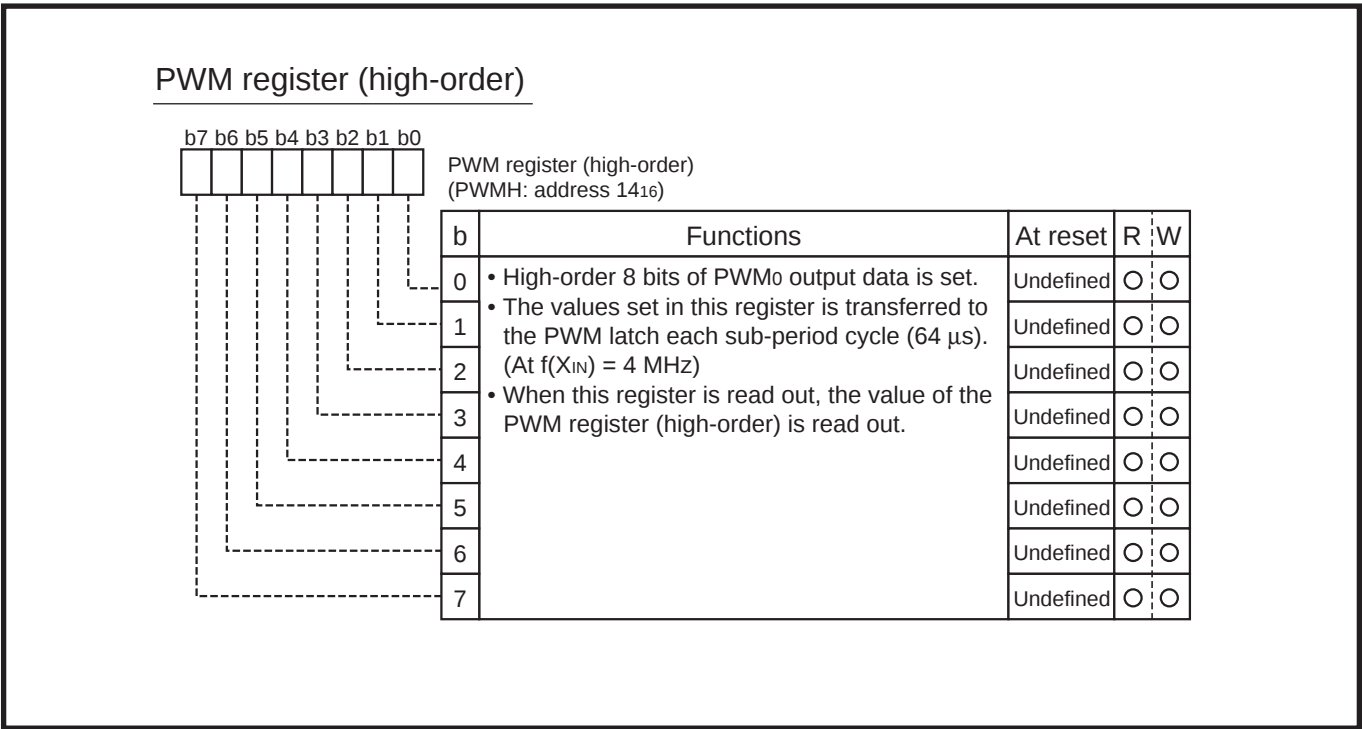


Fig. 2.6.2 Structure of PWM register (high-order)

PWM register (low-order)

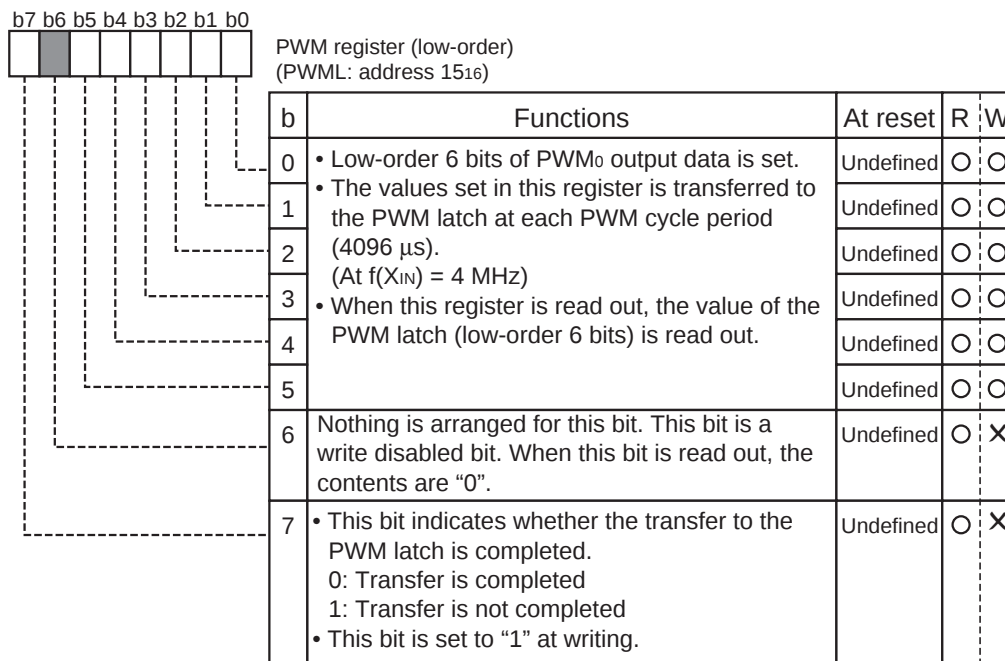


Fig. 2.6.3 Structure of PWM register (low-order)

PWM control register

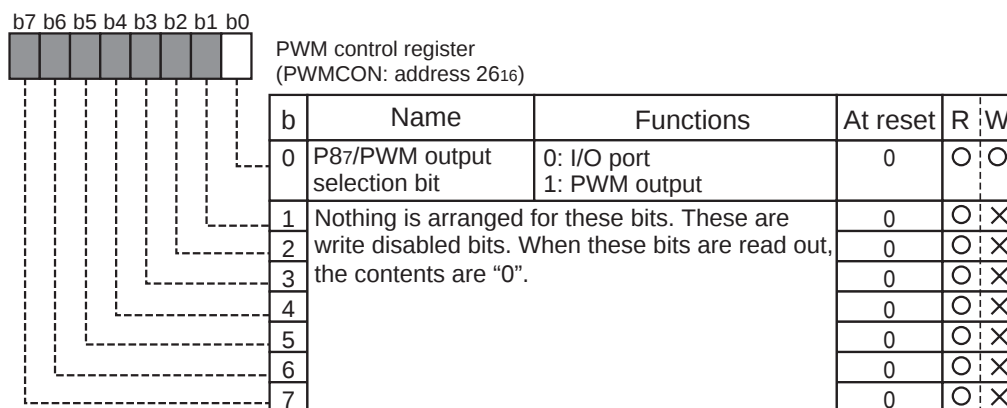


Fig. 2.6.4 Structure of PWM control register

APPLICATION

2.6 PWM

2.6.3 PWM application example

(1) Control of VS tuner

Figure 2.6.5 shows a connection diagram, and Figure 2.6.6 shows the setting of relevant registers.

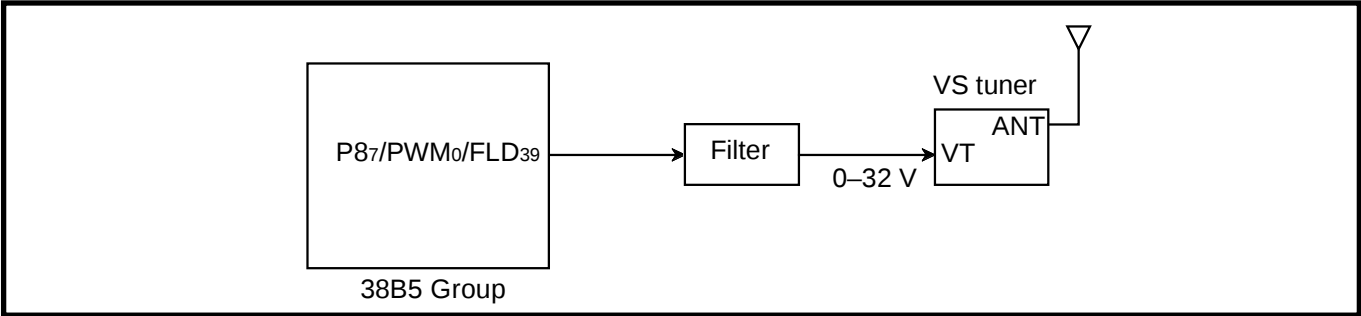


Fig. 2.6.5 Connection diagram

- Outline:**
- Control of VS tuner by using the 14-bit resolution PWM₀ output function
 - $f(X_{IN}) = 4 \text{ MHz}$

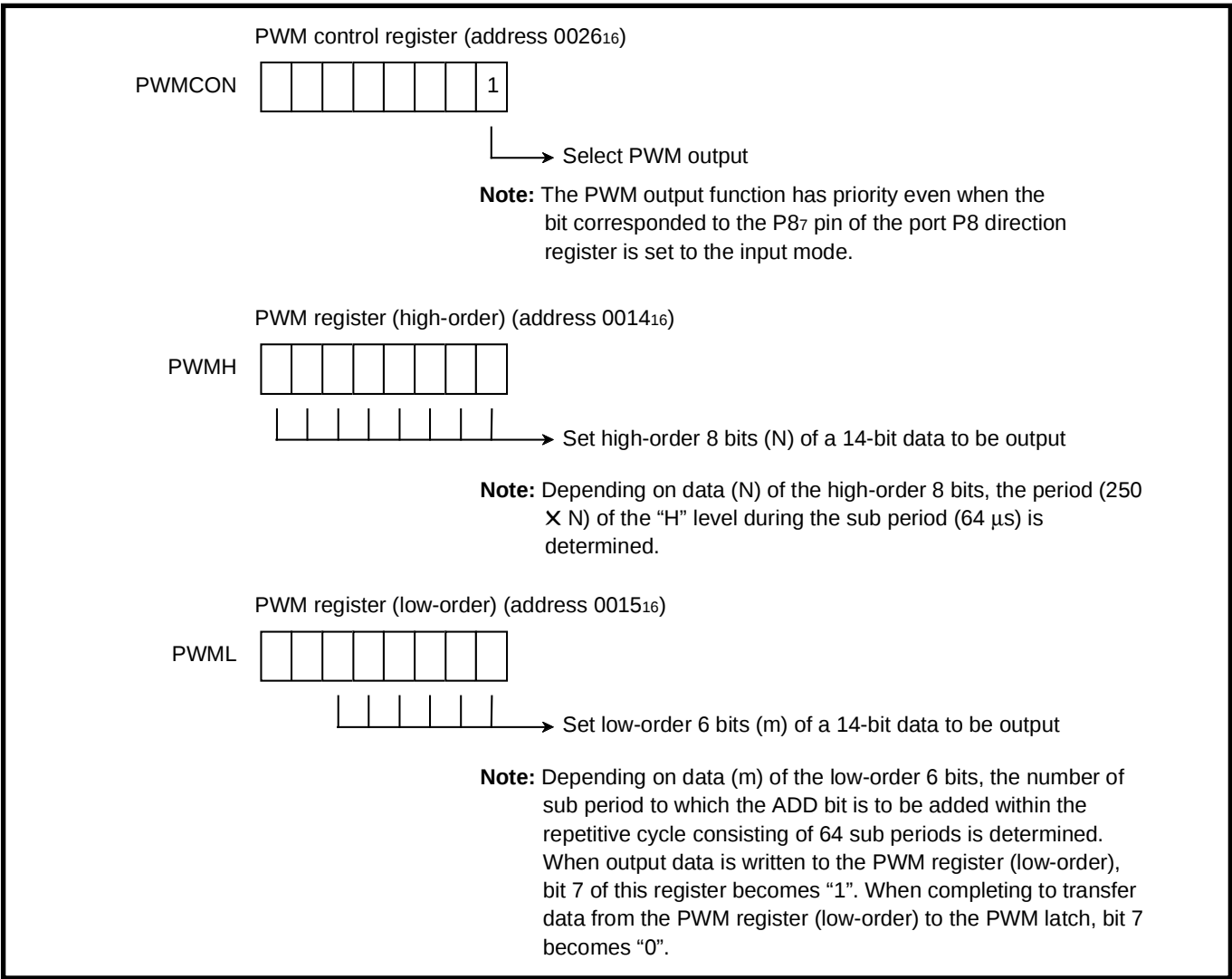


Fig. 2.6.6 Setting of relevant registers

Control procedure: PWM waveform is output to the external by setting relevant registers shown Figure 2.6.6. This PWM₀ output is integrated through the low pass filter and converted into DC signals for control of the VS tuner. Figure 2.6.7 shows the control procedure.

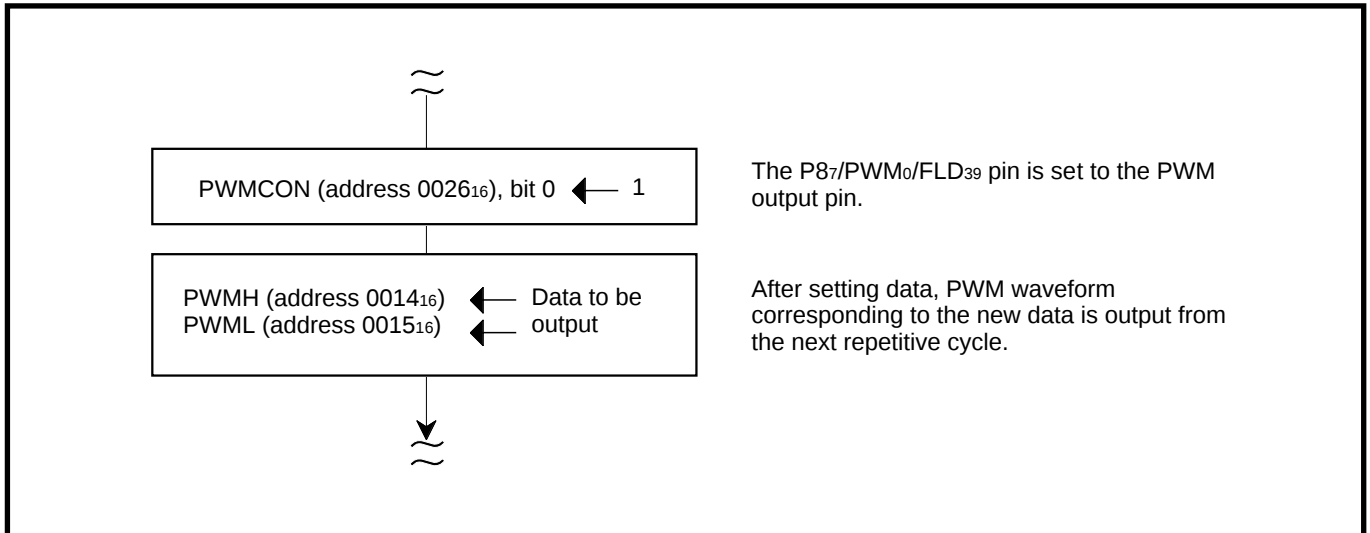


Fig. 2.6.7 Control procedure

2.6.4 Notes on use

- For PWM₀ output, “L” level is output first.
- After data is set to the PWM register (low-order) and the PWM register (high-order), PWM waveform corresponding to new data is output from next repetitive cycle.

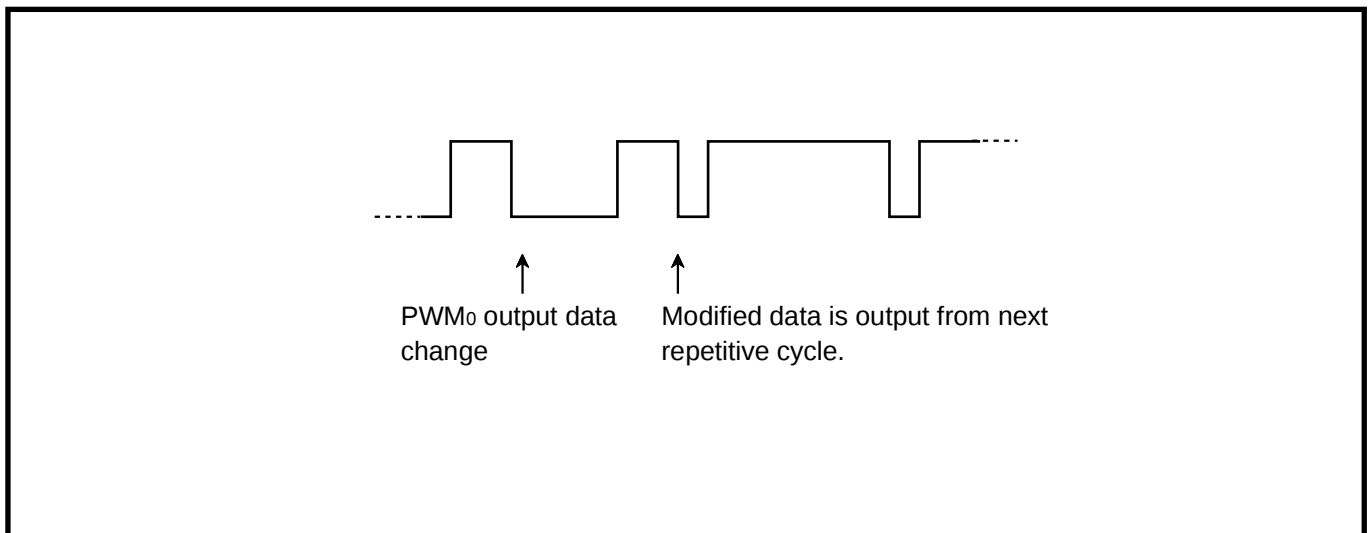


Fig. 2.6.8 PWM₀ output

APPLICATION

2.7 Interrupt interval determination function

2.7 Interrupt interval determination function

This paragraph describes the setting method of interrupt interval determination function relevant registers, notes etc.

2.7.1 Memory assignment

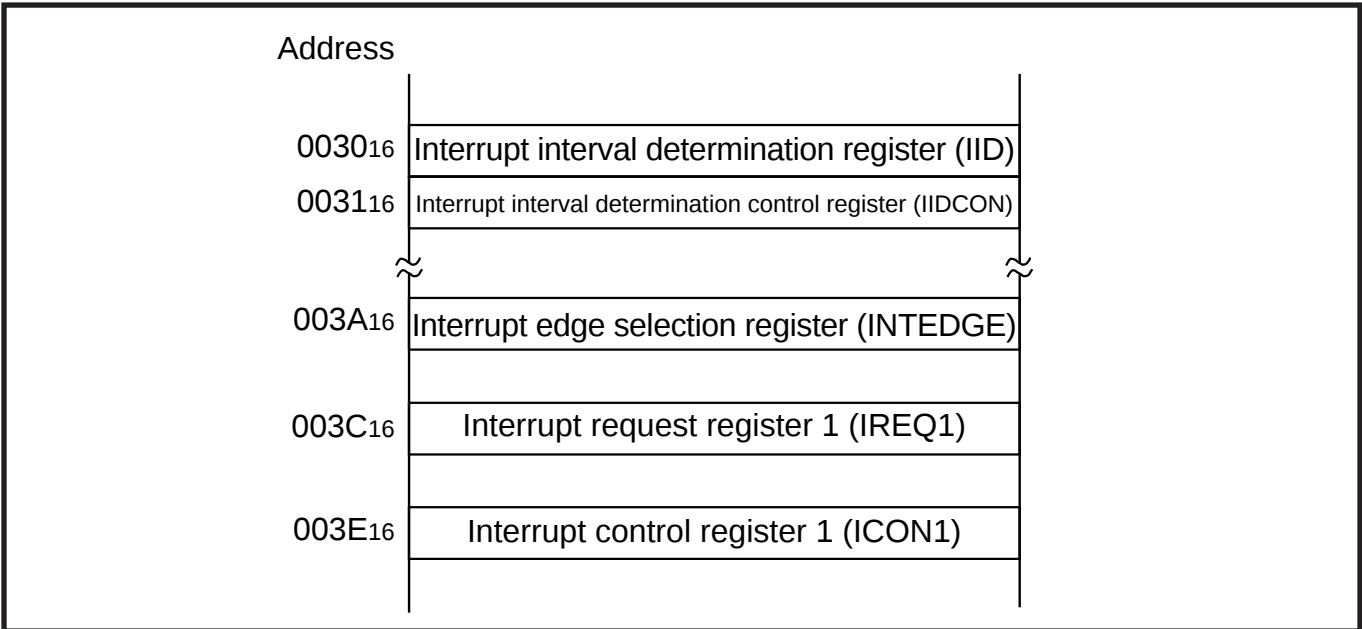


Fig. 2.7.1 Memory assignment of interrupt interval determination function relevant registers

2.7.2 Relevant registers

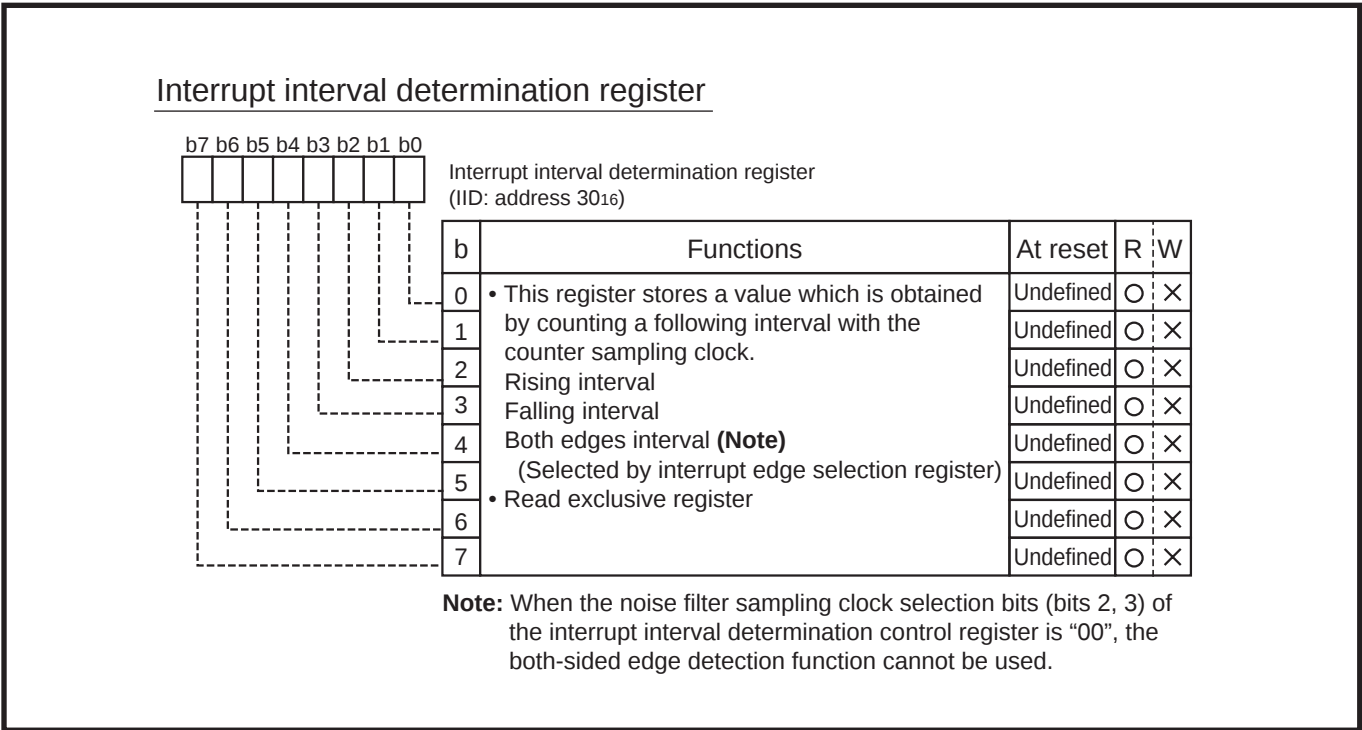
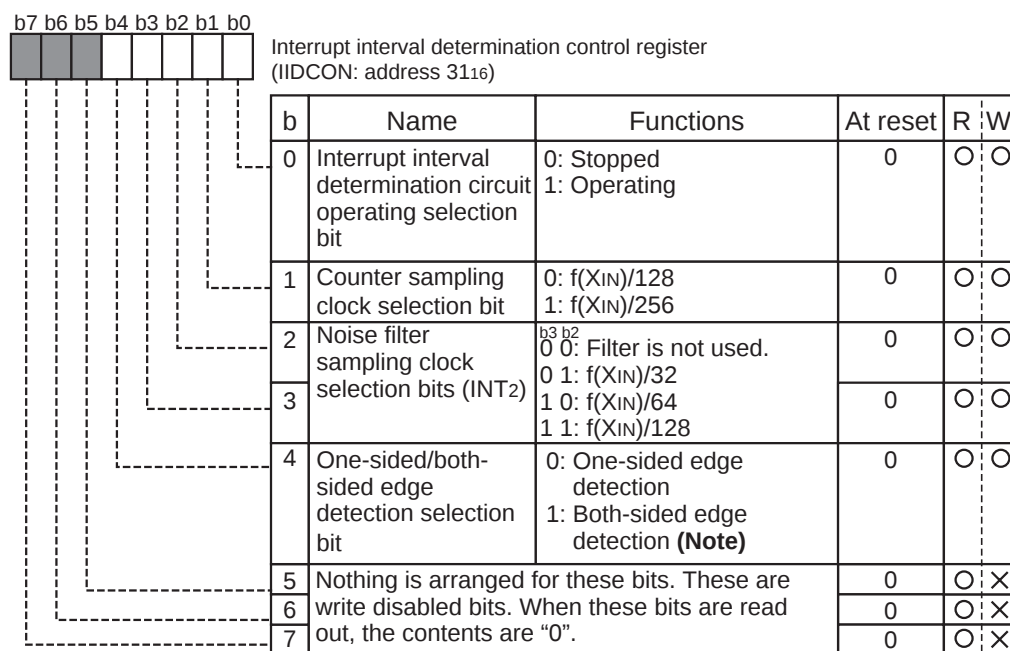


Fig. 2.7.2 Structure of interrupt interval determination register

2.7 Interrupt interval determination function

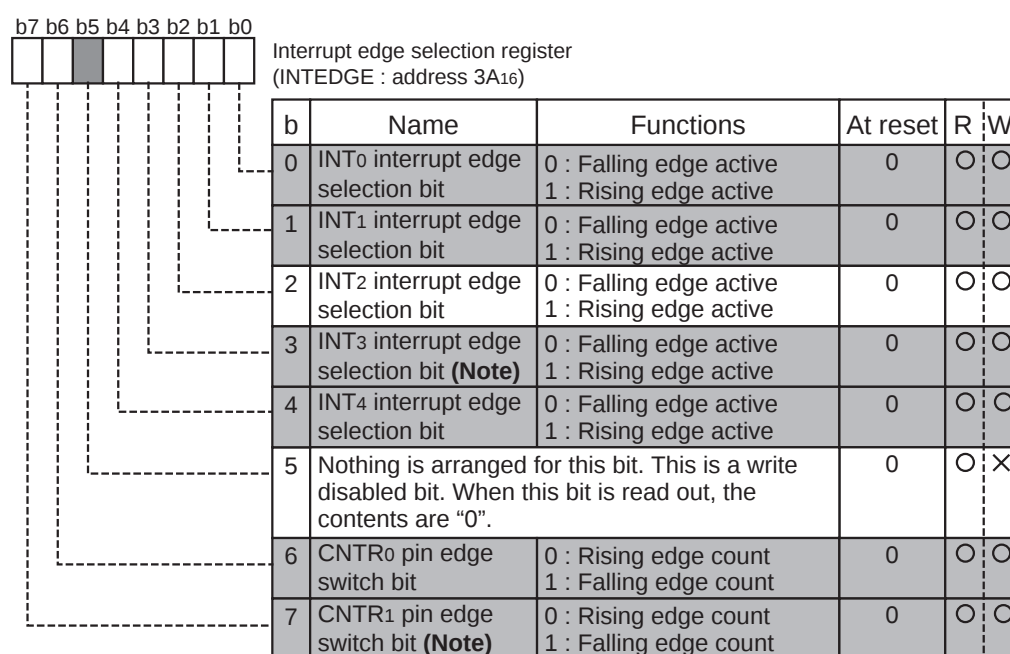
Interrupt interval determination control register



Note: When the noise filter sampling clock selection bits (bits 2, 3) is "00", the both-sided edge detection function cannot be used.

Fig. 2.7.3 Structure of interrupt interval determination control register

Interrupt edge selection register



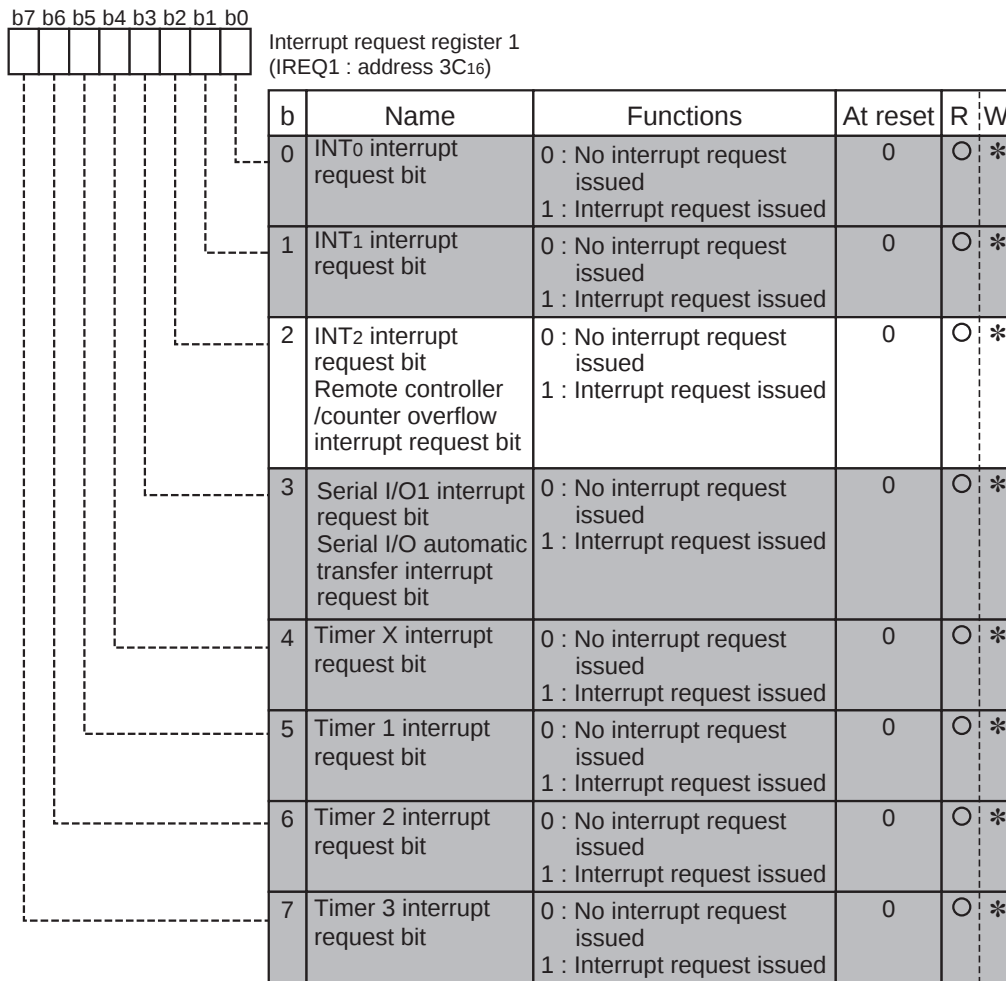
Note: In the mask option type P, these bits are not available because CNTR₁ function and INT₃ function cannot be used.

Fig. 2.7.4 Structure of interrupt edge selection register

APPLICATION

2.7 Interrupt interval determination function

Interrupt request register 1



*: "0" can be set by software, but "1" cannot be set.

Fig. 2.7.5 Structure of interrupt request register 1

2.7 Interrupt interval determination function

Interrupt control register 1

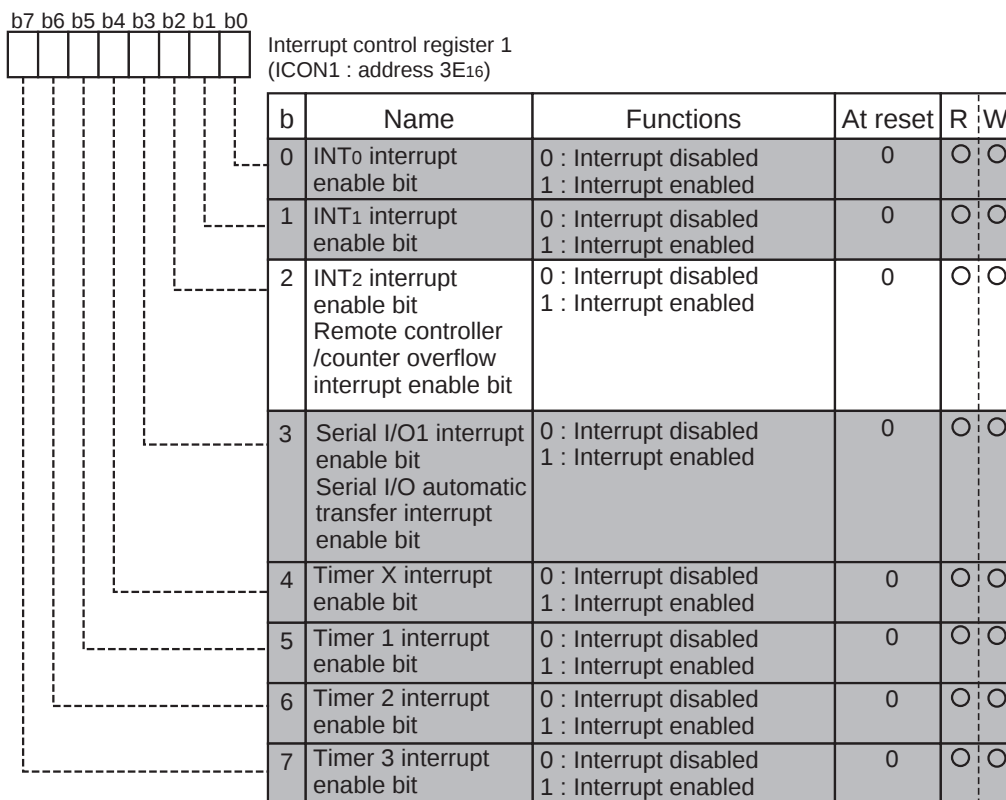


Fig. 2.7.6 Structure of interrupt control register 1

APPLICATION

2.7 Interrupt interval determination function

2.7.3 Interrupt interval determination function application examples

(1) Reception of remote-control signal

Outline: Remote-control signal is read in by both of the interrupt interval determination function using a noise filter and a timer interrupt.

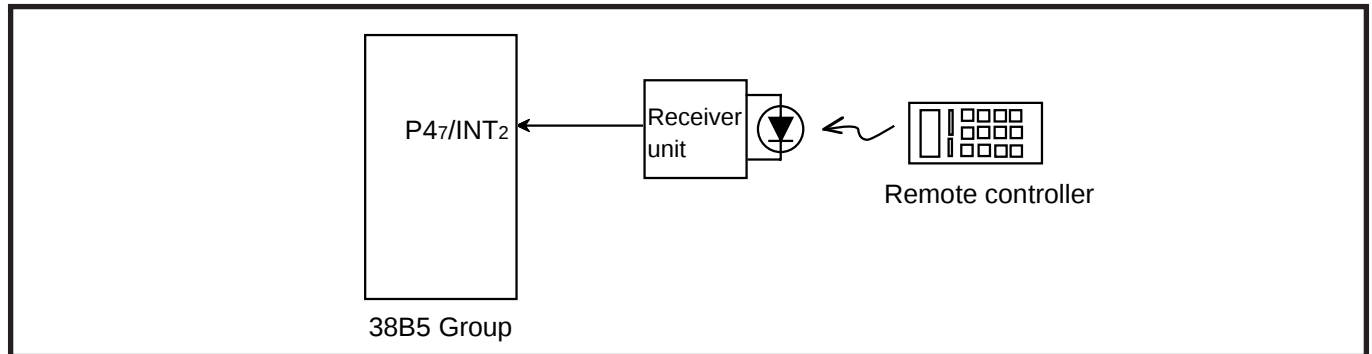


Fig. 2.7.7 Connection diagram

- Specifications:**
- Measurement of one-sided edge interval
 - Use of noise filter
 - Check of remote control interrupt request within the timer 2 interrupt (488 μ s period) processing routine
 - Operation at $f(X_{IN}) = 4$ MHz in high-speed mode

Figure 2.7.8 shows the function block diagram, and Figure 2.7.9 shows a timing chart of data determination.

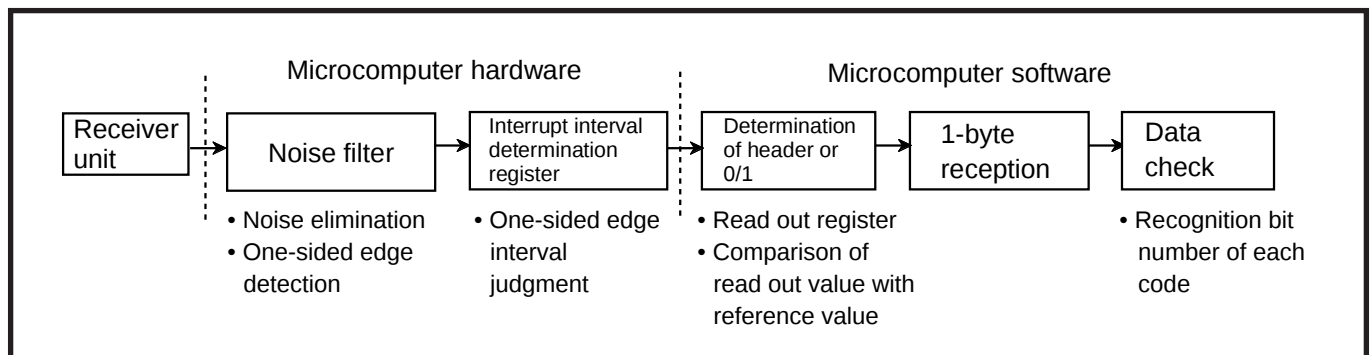


Fig. 2.7.8 Function block diagram

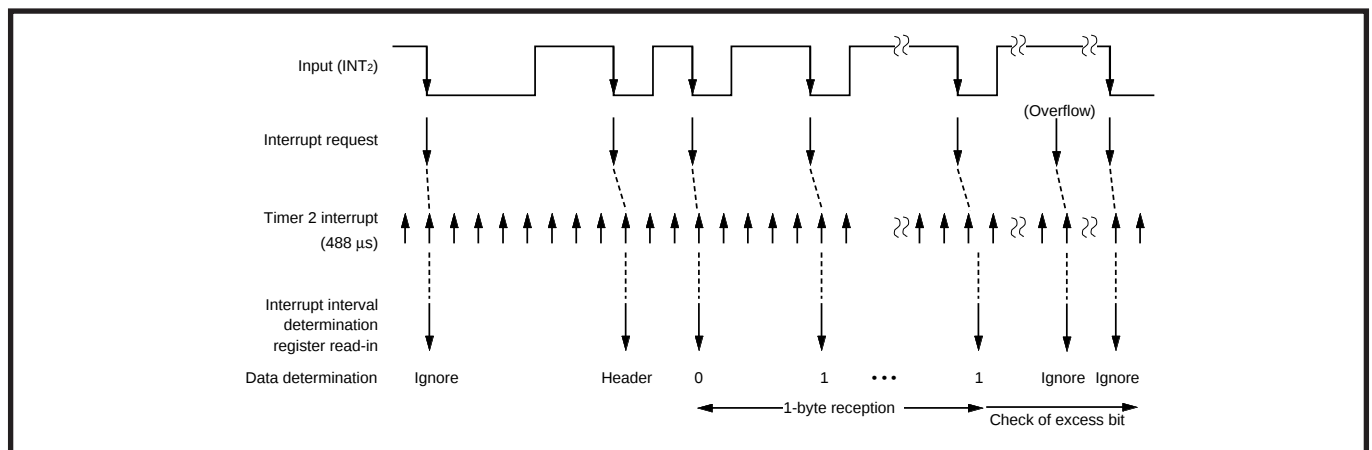


Fig. 2.7.9 Timing chart of data determination

2.7 Interrupt interval determination function

Figure 2.7.10 shows the setting of relevant registers.

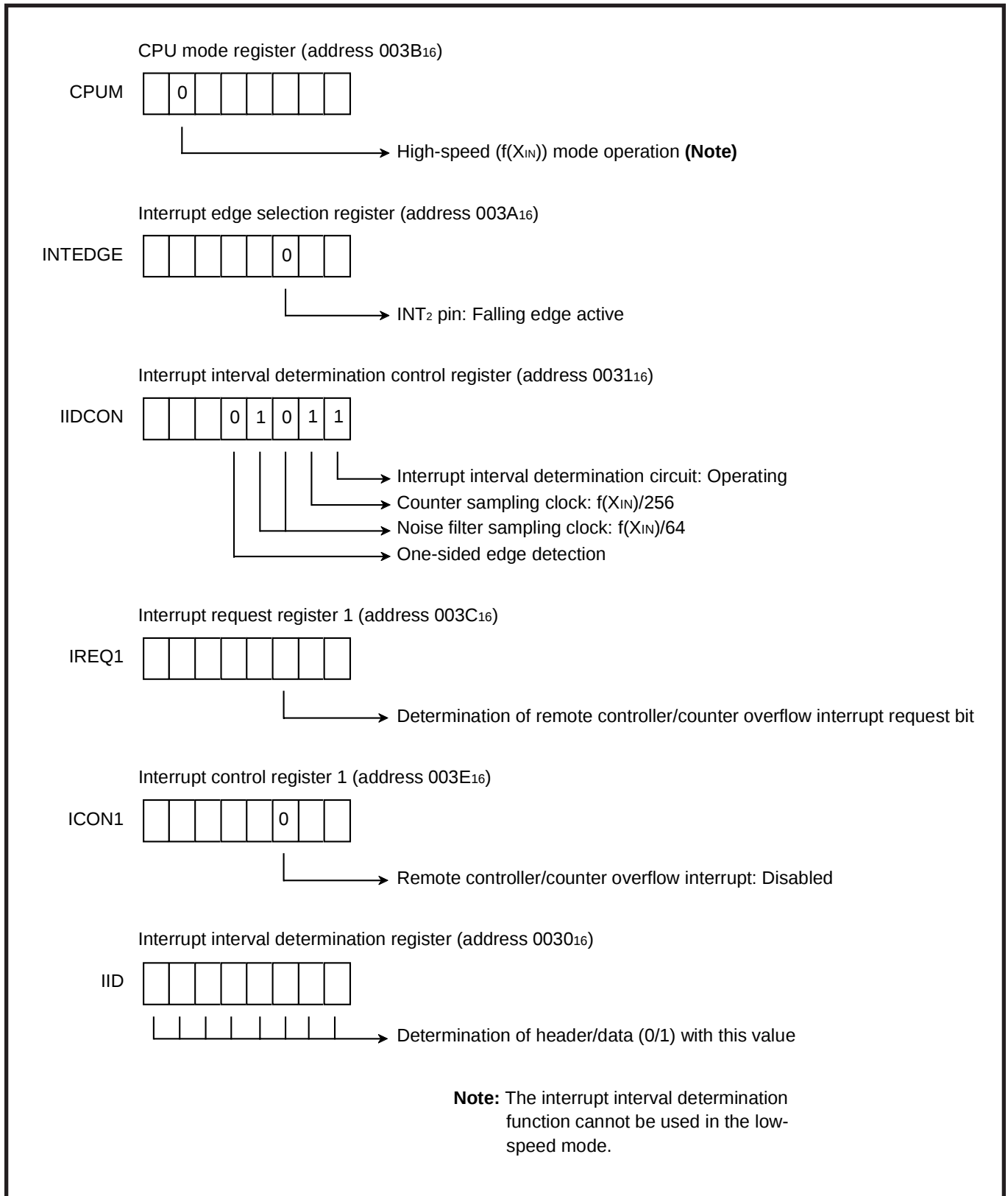


Fig. 2.7.10 Setting of relevant registers

APPLICATION

2.7 Interrupt interval determination function

Control procedure: When the registers are set as shown Figure 2.7.10, remote-control signals are receivable. Figure 2.7.11 shows the control procedure, and Figure 2.7.12 shows the reception of remote-control data (timer 2 interrupt).

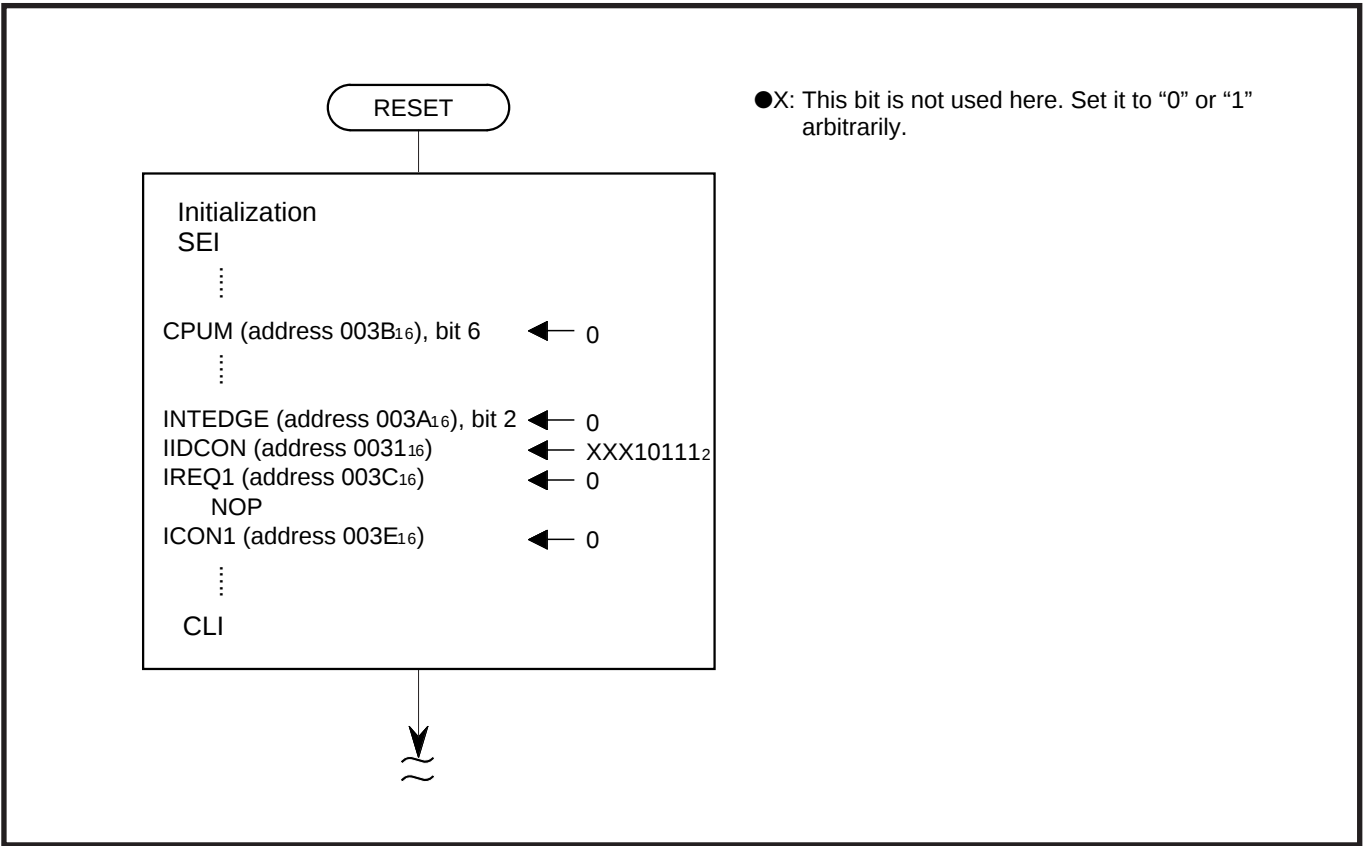


Fig. 2.7.11 Control procedure

2.7 Interrupt interval determination function

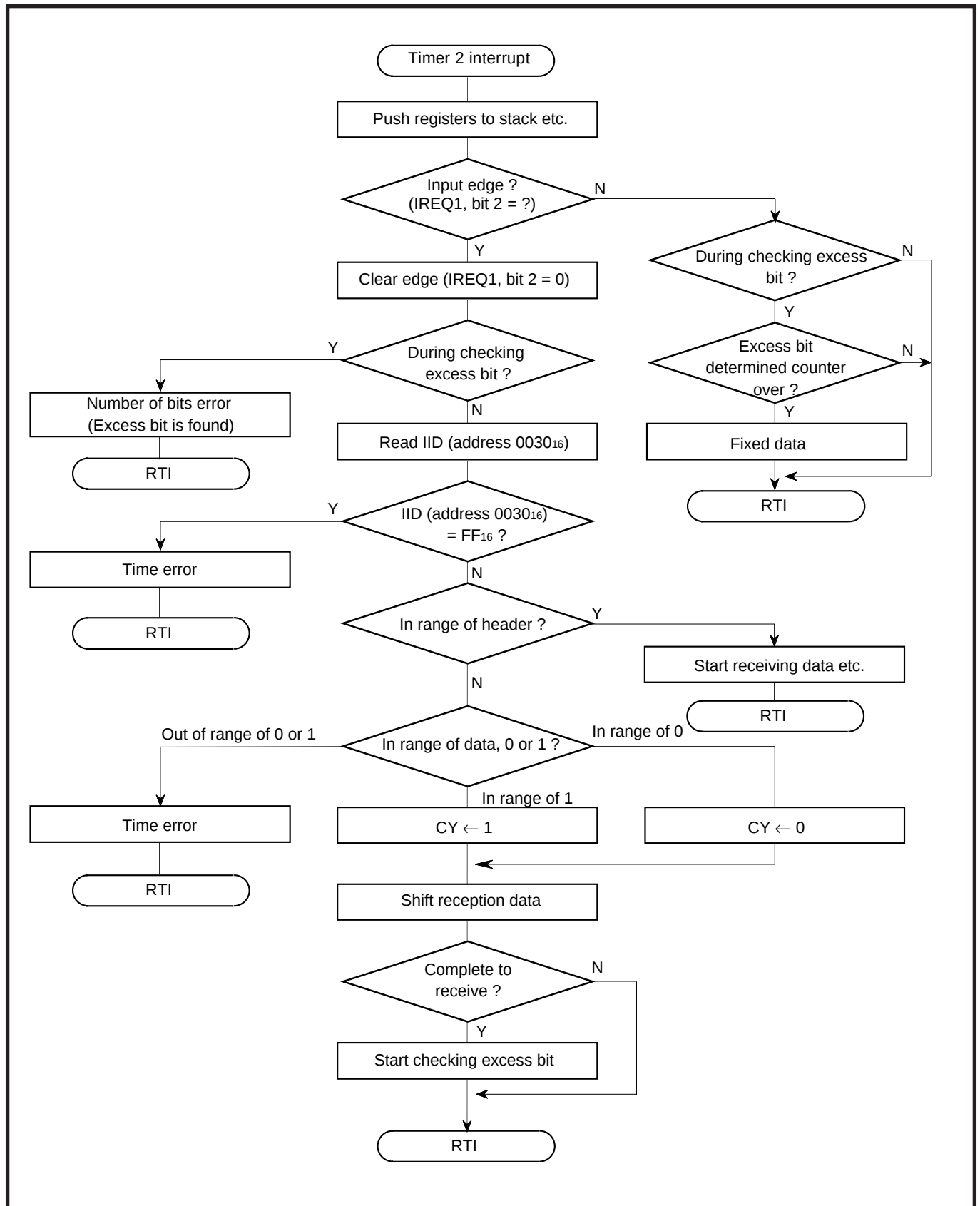


Fig. 2.7.12 Reception of remote-control data (timer 2 interrupt)

APPLICATION

2.8 Watchdog timer

2.8 Watchdog timer

The watchdog timer is a 20-bit down-count counter consisting of a low-order 8 bits and a high-order 12 bits. “1” is subtracted from the watchdog timer each time a count source inputs. This paragraph describes the setting method of watchdog timer relevant register, notes etc.

2.8.1 Memory assignment

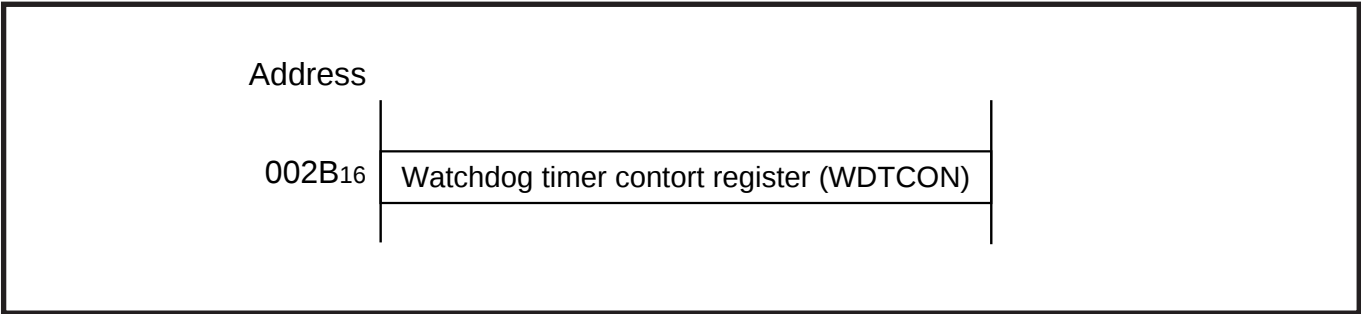


Fig. 2.8.1 Memory assignment of watchdog timer relevant register

2.8.2 Relevant register

The watchdog timer starts counting by writing an arbitrary value to the watchdog timer control register. Figure 2.8.2 shows the structure of the watchdog timer control register.

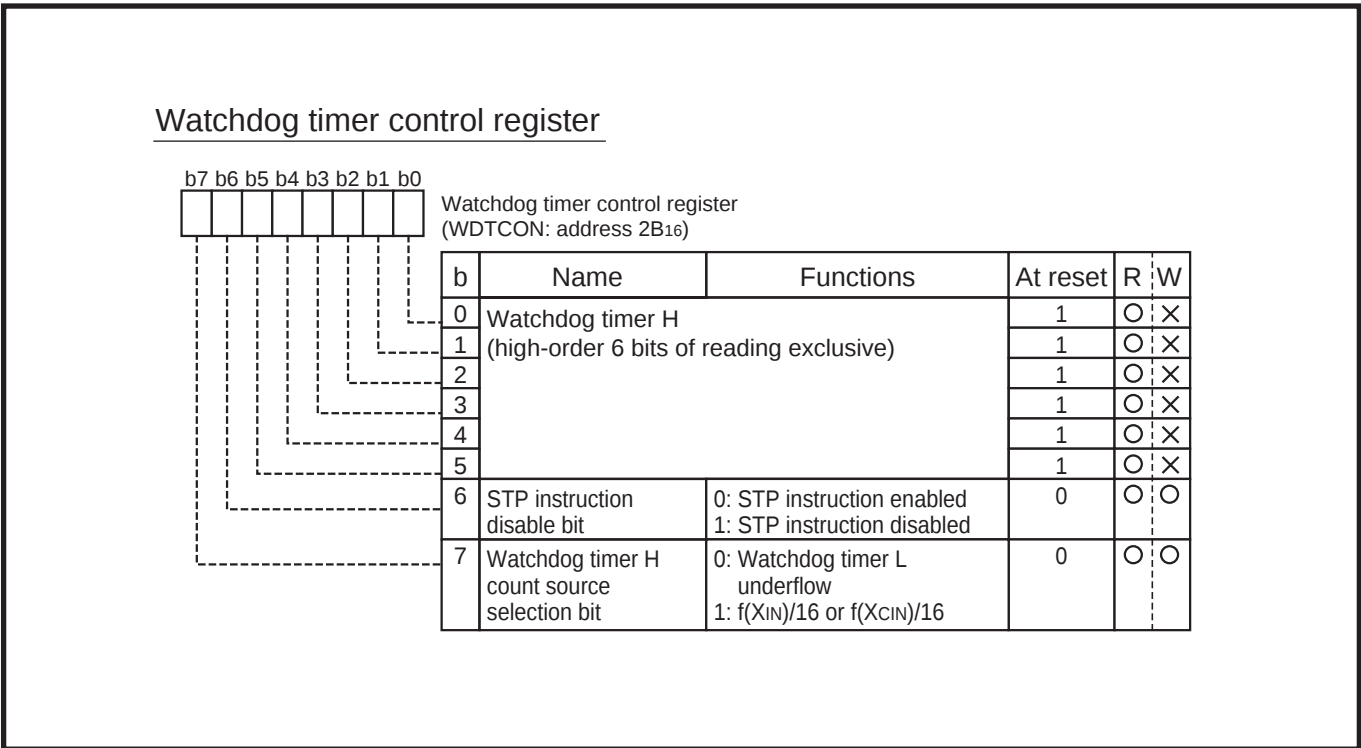


Fig. 2.8.2 Structure of watchdog timer control register

2.8.3 Watchdog timer application examples

Outline: When a program runs away, the watchdog timer makes the microcomputer return to the reset state.

- Specifications:**
- When the watchdog timer H underflows, it is judged as incorrect program, and the microcomputer is returned to the reset state.
 - Bit 7 of the watchdog timer control register is set to "0" at 1-cycle intervals in the main routine before underflow of the watchdog timer H. (Initialization of watchdog timer value)
 - Use of watchdog timer L underflow as count source of watchdog timer H
 - Setting of main clock division ratio to $f(X_{IN})$ (high-speed mode)

Figure 2.8.3 shows the connection of watchdog timer and the setting of the division ratio.

Figure 2.8.4 shows the setting of relevant registers.

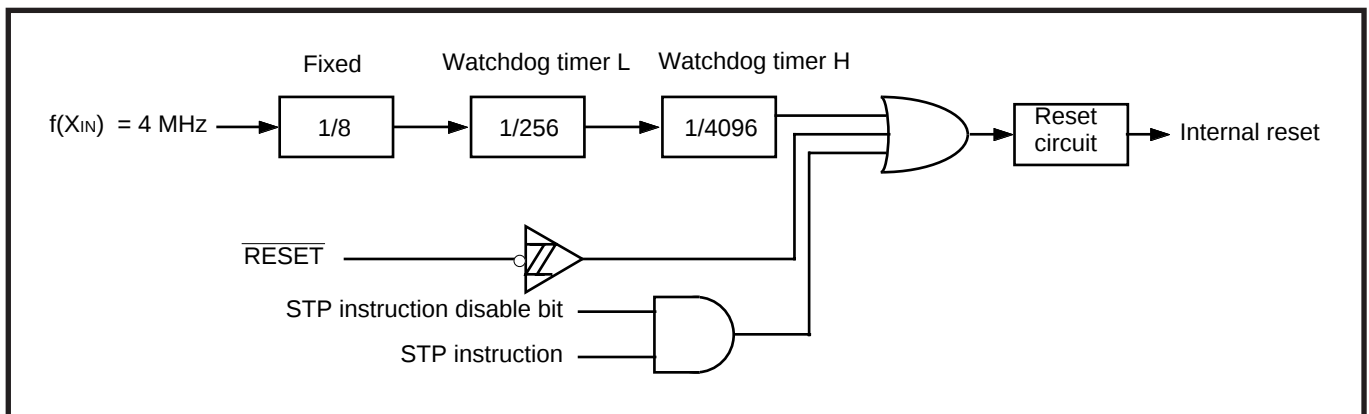


Fig. 2.8.3 Connection of watchdog timer and setting of division ratio

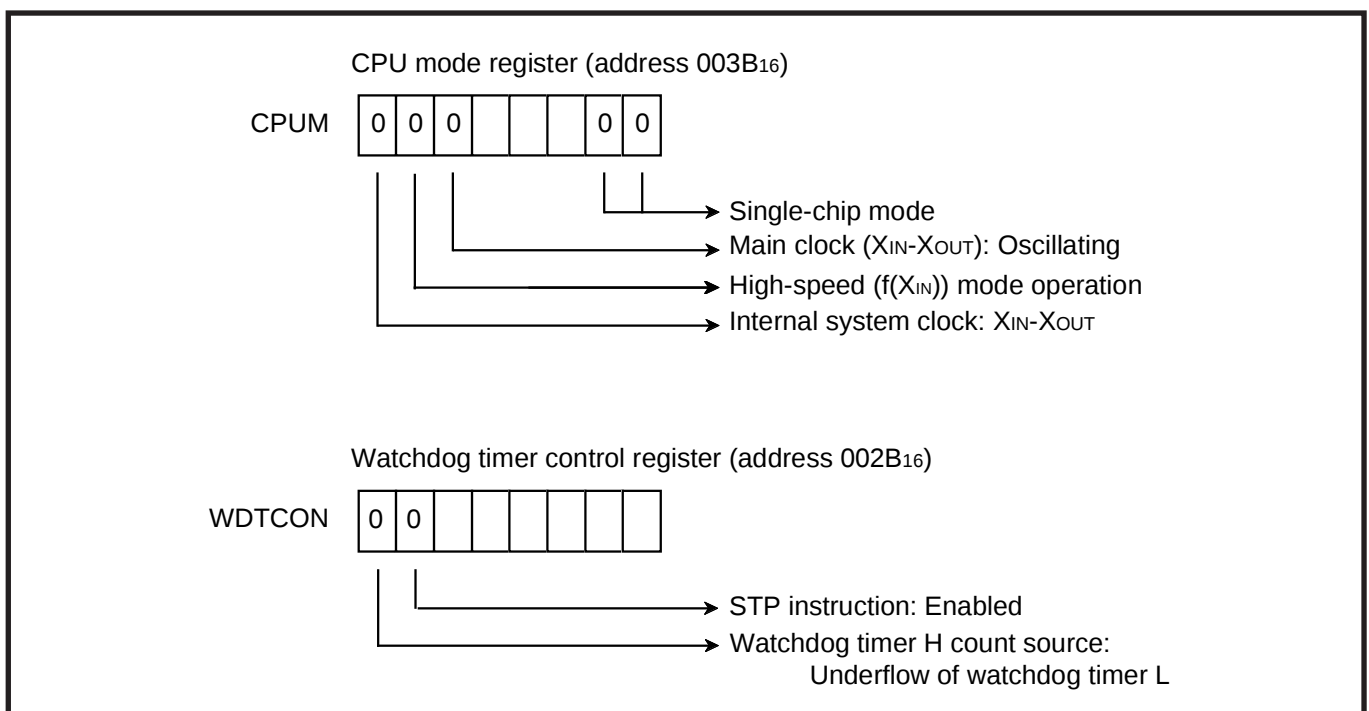


Fig. 2.8.4 Setting of relevant registers

APPLICATION

2.8 Watchdog timer

Figure 2.8.5 shows the control procedure.

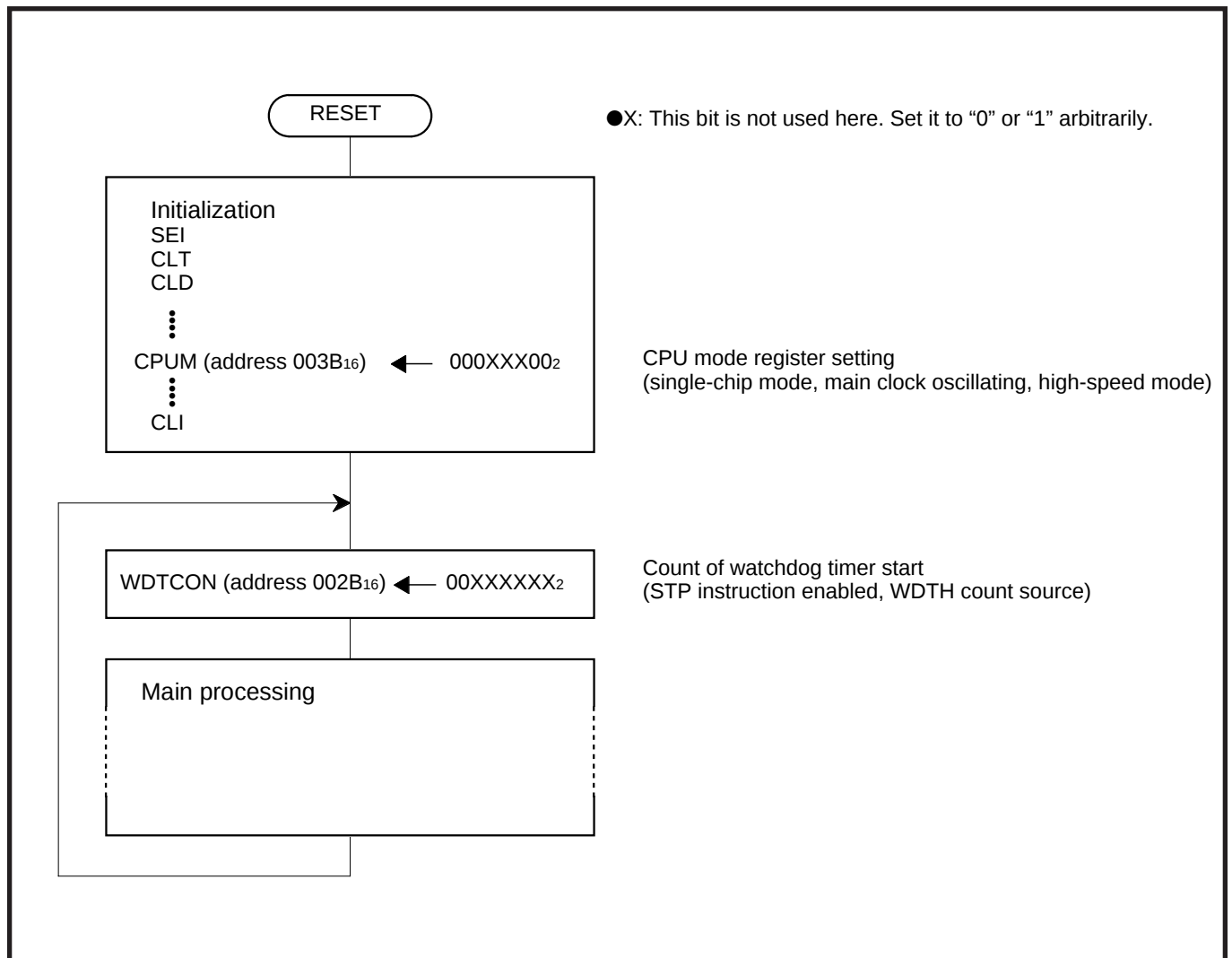


Fig. 2.8.5 Control procedure

2.8.4 Notes on use

- The watchdog timer continues to count even while waiting for stop release. Accordingly, make sure that watchdog timer does not underflow during this term by writing to the watchdog timer control register (address 002B₁₆) once before executing the STP instruction, etc.
- Once a "1" is written to the STP instruction disable bit (bit 6) of the watchdog timer control register (address 002B₁₆), it cannot be programmed to "0" again. This bit becomes "0" after reset.

2.9 Buzzer output circuit

The output frequency can be selected from 1 kHz, 2 kHz, or 4 kHz (at $f(X_{IN}) = 4.19 \text{ MHz}$), and the output port can be selected between either the BUZ01 pin or the BUZ02 pin.

This paragraph describes the setting method of buzzer output circuit relevant register, notes etc.

2.9.1 Memory assignment

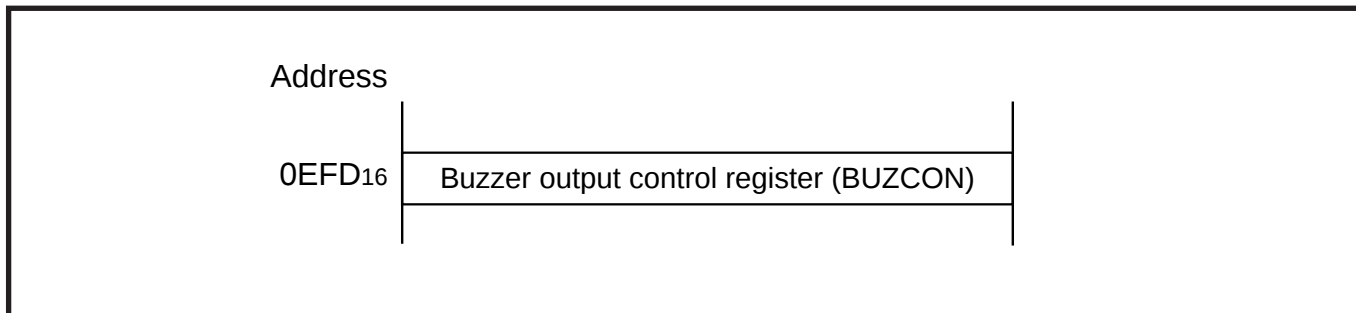


Fig. 2.9.1 Memory assignment of buzzer output circuit relevant register

2.9.2 Relevant register

The buzzer output circuit starts outputting a buzzer by setting the buzzer output ON/OFF bit (bit 4) of the buzzer output control register.

Figure 2.9.2 shows the structure of the buzzer output control register.

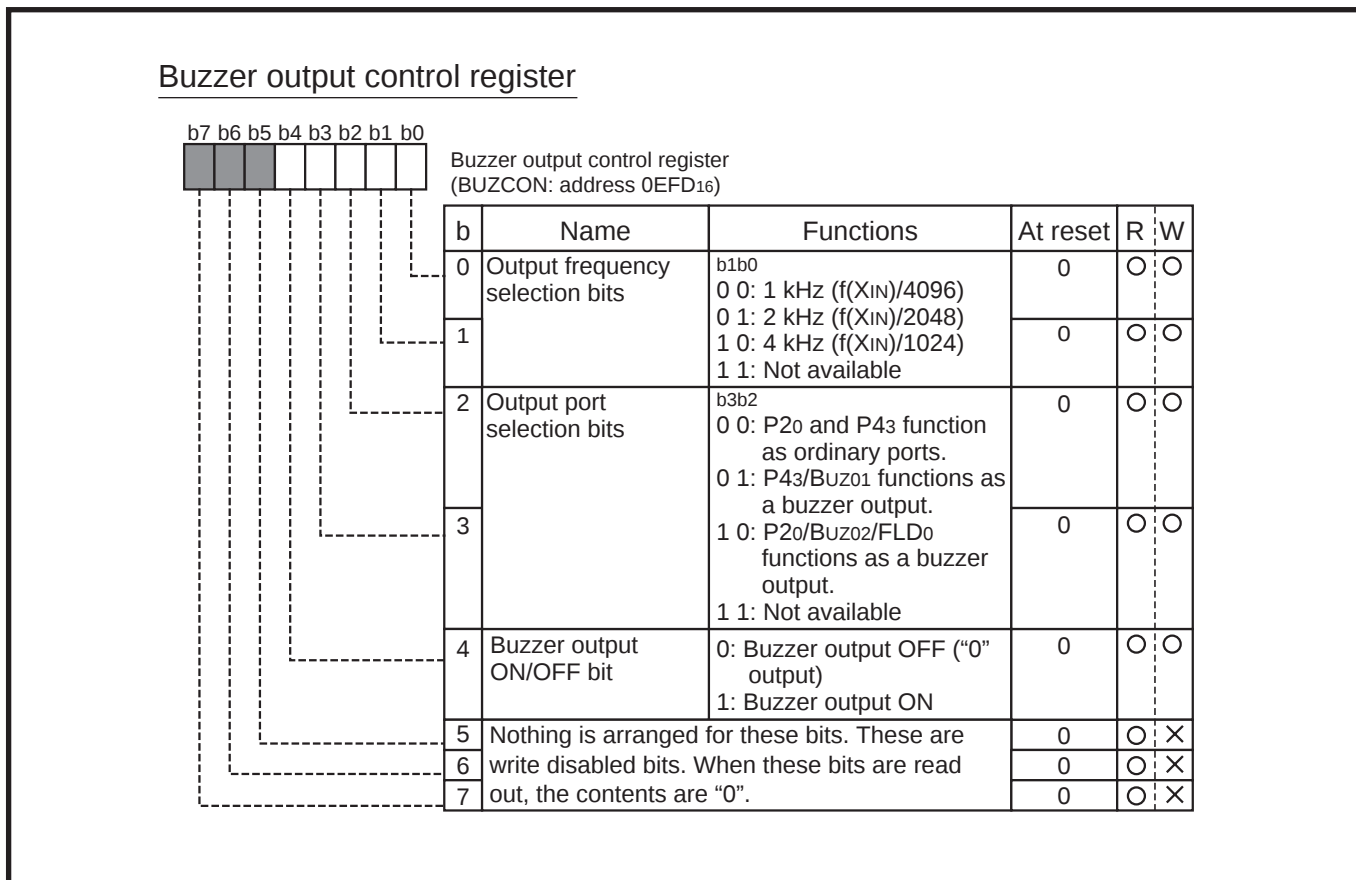


Fig. 2.9.2 Structure of buzzer output control register

APPLICATION

2.9 Buzzer output circuit

2.9.3 Buzzer output circuit application examples

Outline: A buzzer output is performed by using the buzzer output circuit.

Specifications:

- $f(X_{IN}) = 4.19\text{ MHz}$, buzzer output frequency = 4 kHz
- Buzzer output from BUZ01 pin

Figure 2.9.3 shows the connection of buzzer output circuit and the setting of the division ratio. Figure 2.9.4 shows the setting of relevant register. Figure 2.9.5 shows the control procedure.

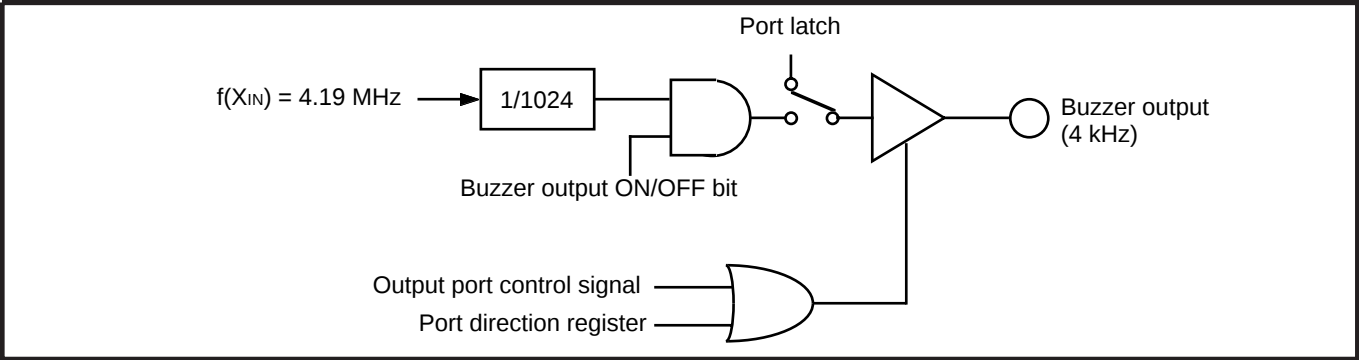


Fig. 2.9.3 Connection of buzzer output circuit and setting of division ratio

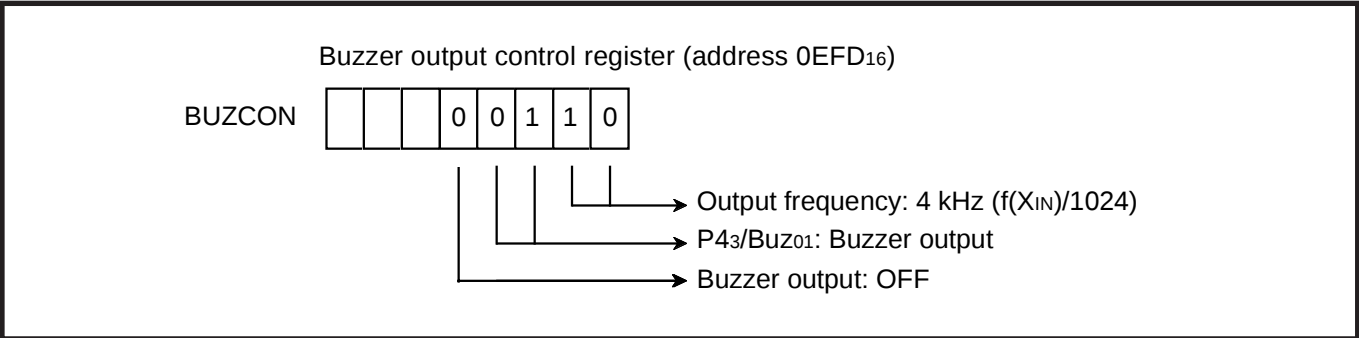


Fig. 2.9.4 Setting of relevant register

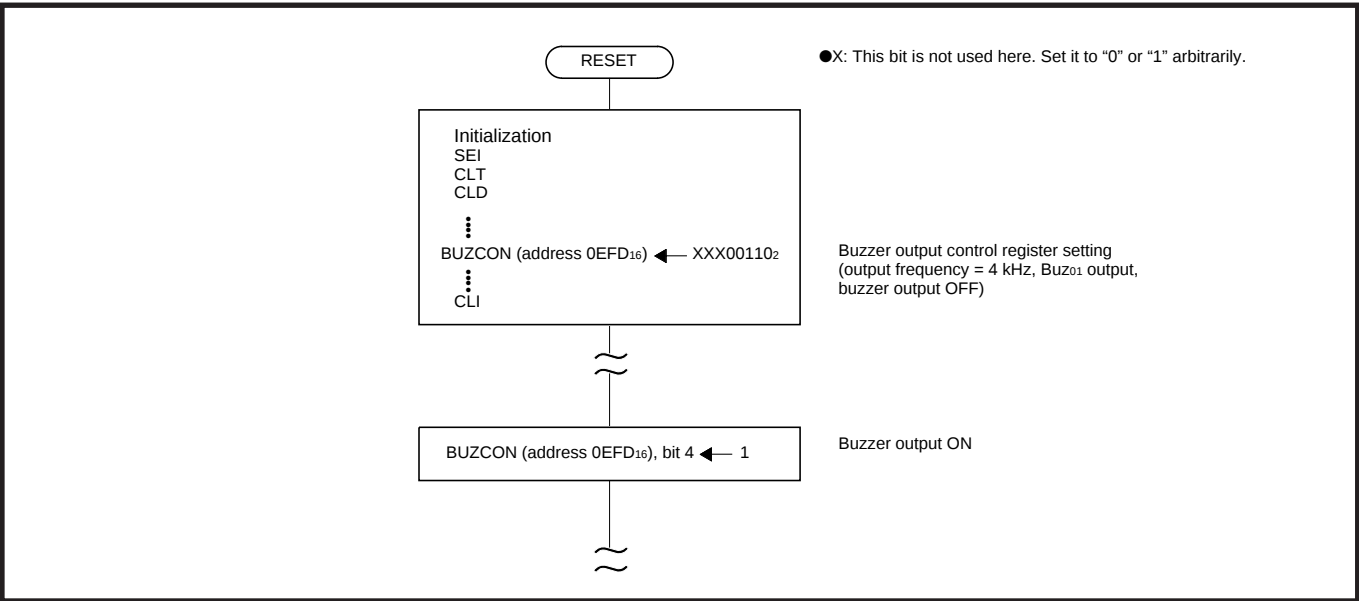


Fig. 2.9.5 Control procedure

2.10 Reset circuit

The reset state is caused by applying an “L” level to the $\overline{\text{RESET}}$ pin. After that, the reset state is released by applying an “H” level to the $\overline{\text{RESET}}$ pin, so that the program is executed in the middle-speed mode from the contents of the reset vector address.

2.10.1 Connection example of reset IC

Figure 2.10.1 shows the example of power-on reset circuit. Figure 2.10.2 shows the system example which switches to the RAM backup mode by detecting a drop of the system power source voltage with the INT interrupt.

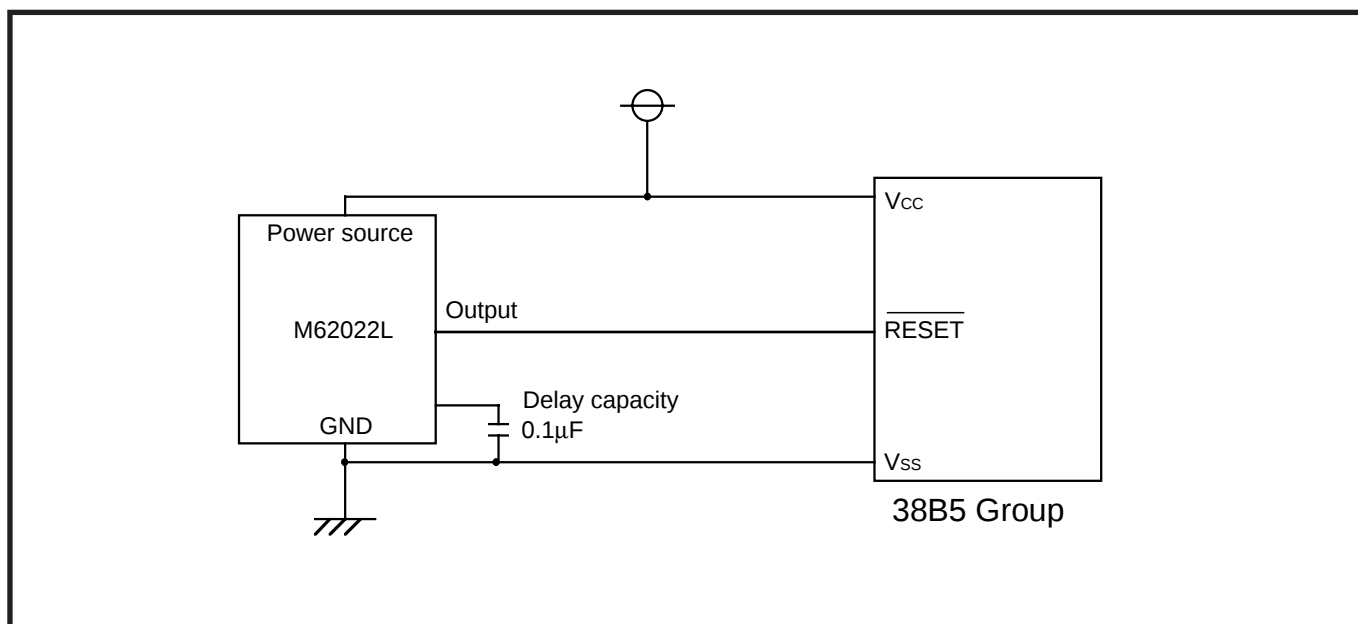


Fig. 2.10.1 Example of power-on reset circuit

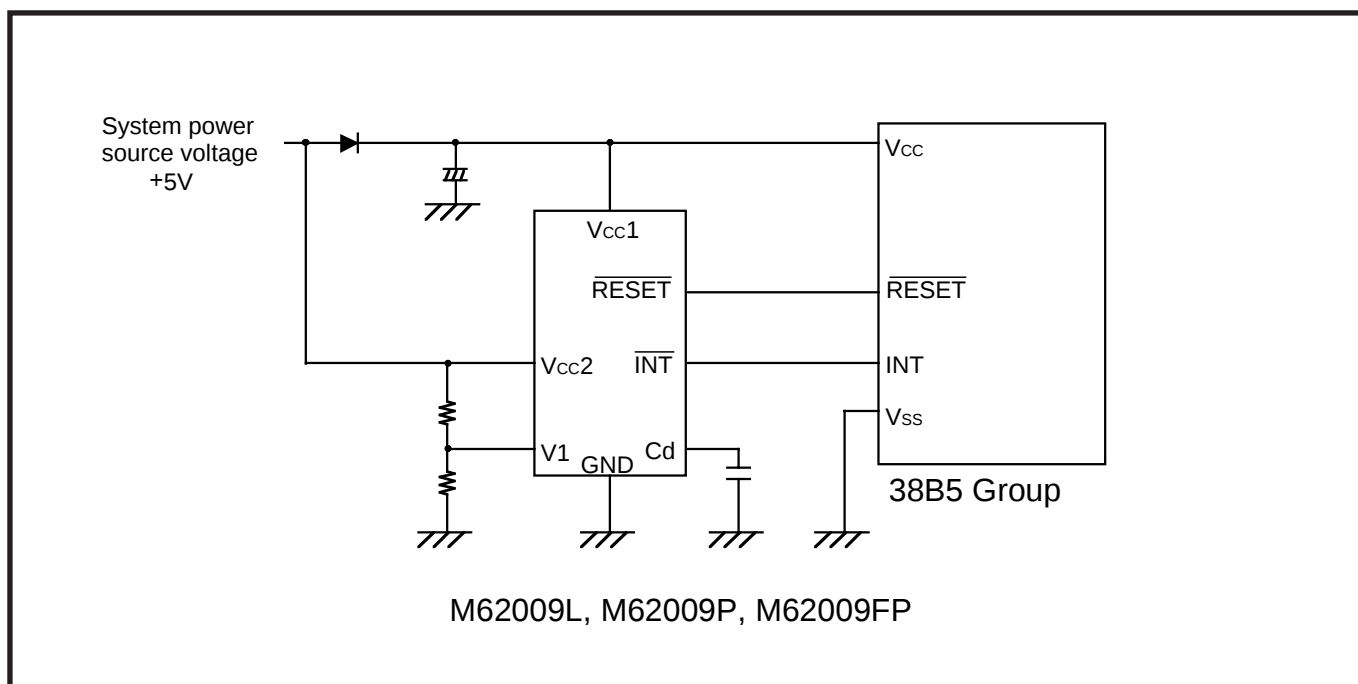


Fig. 2.10.2 RAM backup system example

APPLICATION

2.10 Reset circuit

2.10.2 Notes on use

(1) Reset input voltage control

Make sure that the reset input voltage is 0.5 V or less for V_{CC} of 2.7 V.

Perform switch to the high-speed mode when power source voltage is within 4.0 to 5.5 V.

(2) Countermeasure when $\overline{\text{RESET}}$ signal rise time is long

In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the V_{SS} pin. And use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

● Reason

If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

2.11 Clock generating circuit

2.11.1 Relevant register

Figure 2.11.1 shows the structure of the CPU mode register.

CPU mode register

b7 b6 b5 b4 b3 b2 b1 b0								CPU mode register (CPUM, CM: address 3B16)		
b	Name	Functions	At reset	R	W					
0	Processor mode bits	b1 b0 00 : Single-chip mode	0	○	○					
1		01 : 10 : 11 : } Not available	0	○	○					
2		Stack page selection bit	0 : Page 0 1 : Page 1	0	○	○				
3		XcOUT drivability selection bit	0: Low drive 1: High drive	1	○	○				
4	Port Xc switch bit	0: I/O port function 1: XCIN-XcOUT oscillation function	0	○	○					
5	Main clock (XIN-XOUT) stop bit	0: Oscillating 1: Stopped	0	○	○					
6	Main clock division ratio selection bit	0: f(XIN) (high-speed mode) 1: f(XIN)/4 (middle-speed mode)	1	○	○					
7	Internal system clock selection bit	0: XIN-XOUT selection (middle-/high-speed mode) 1: XCIN-XcOUT selection (low-speed mode)	0	○	○					

Fig. 2.11.1 Structure of CPU mode register

APPLICATION

2.11 Clock generating circuit

2.11.2 Clock generating circuit application examples

(1) Status transition during power failure

Outline: The clock is counted up every one second by using the timer interrupt during a power failure.

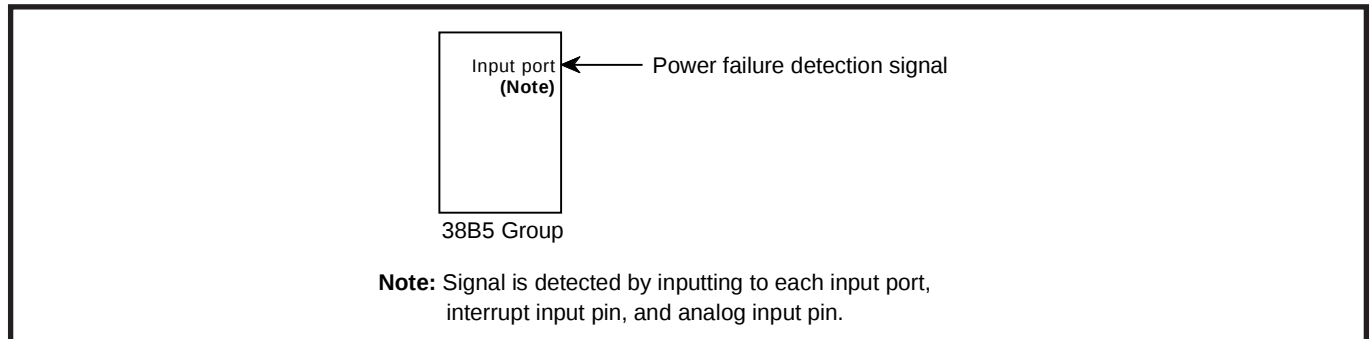


Fig. 2.11.2 Connection diagram

- Specifications:**
- Reducing power dissipation as low as possible while maintaining clock function
 - Clock: $f(X_{IN}) = 4.19 \text{ MHz}$, $f(X_{CIN}) = 32.768 \text{ kHz}$
 - Port processing
 - Input port: Fixed to "H" or "L" level on the external
 - Output port: Fixed to output level that does not cause current flow to the external
(Example) When a circuit turns on LED at "L" output level, fix the output level to "H".
 - I/O port: Input port → Fixed to "H" or "L" level on the external
Output port → Output of data that does not consume current
 - V_{REF} : Stop to supply to reference voltage input pin by external circuit

Figure 2.11.3 shows the status transition diagram during power failure and Figure 2.11.4 shows the setting of relevant registers.

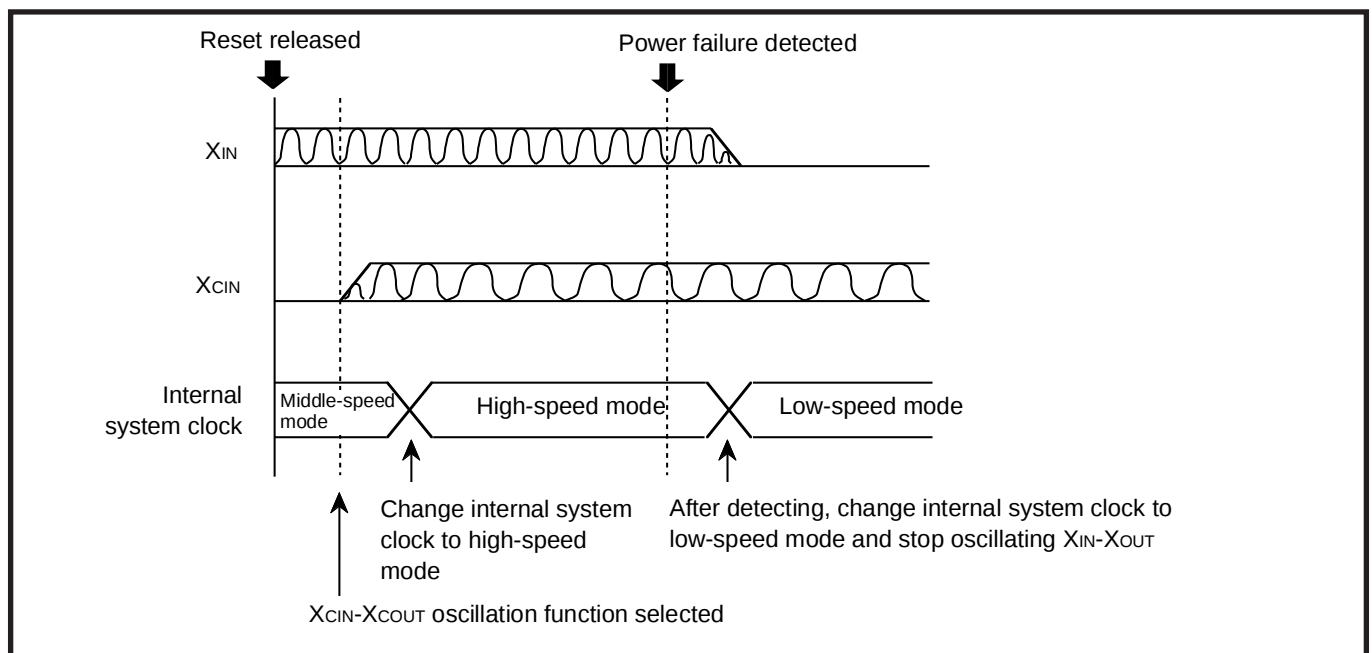
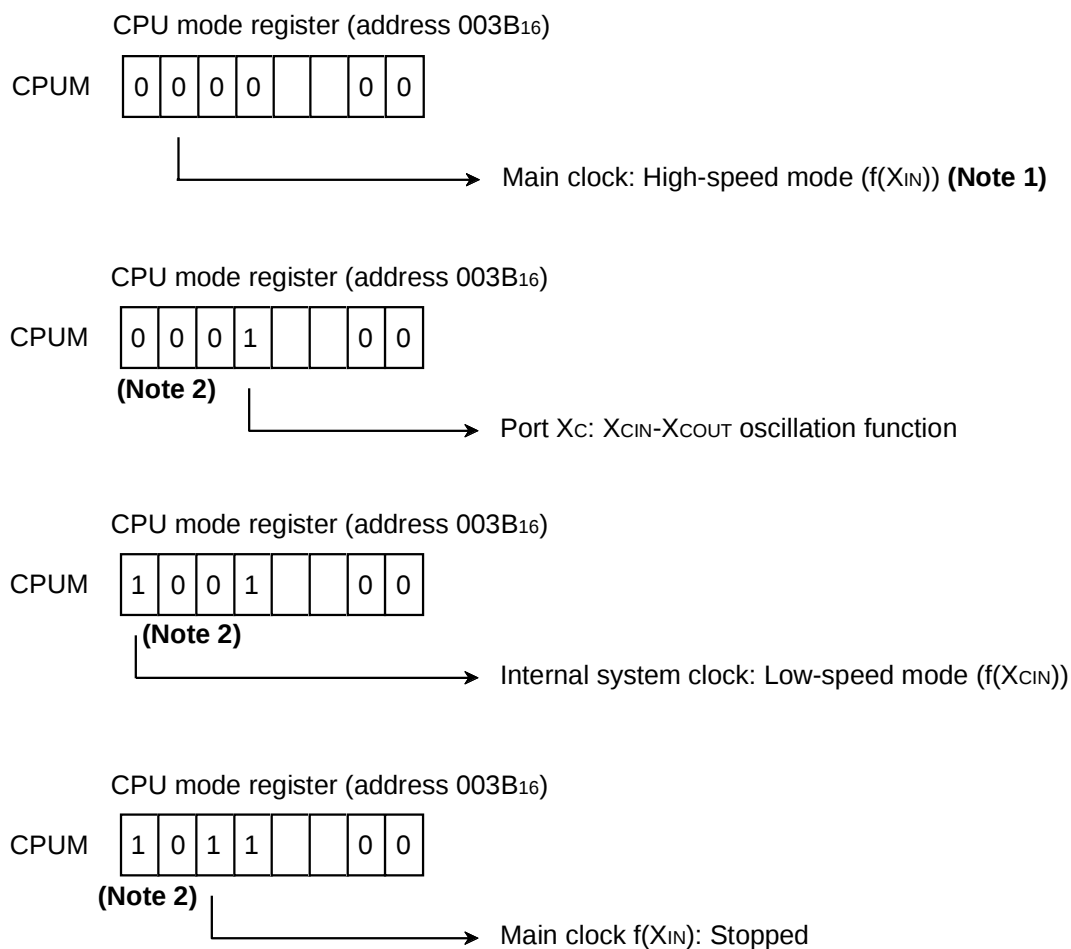


Fig. 2.11.3 Status transition diagram during power failure



Notes 1: This setting is necessary only when selecting the high-speed mode.

2: When selecting the middle-speed mode, bit 6 is "1".

Fig. 2.11.4 Setting of relevant registers

APPLICATION

2.11 Clock generating circuit

Control procedure: Set the relevant registers in the order shown below to prepare for a power failure.

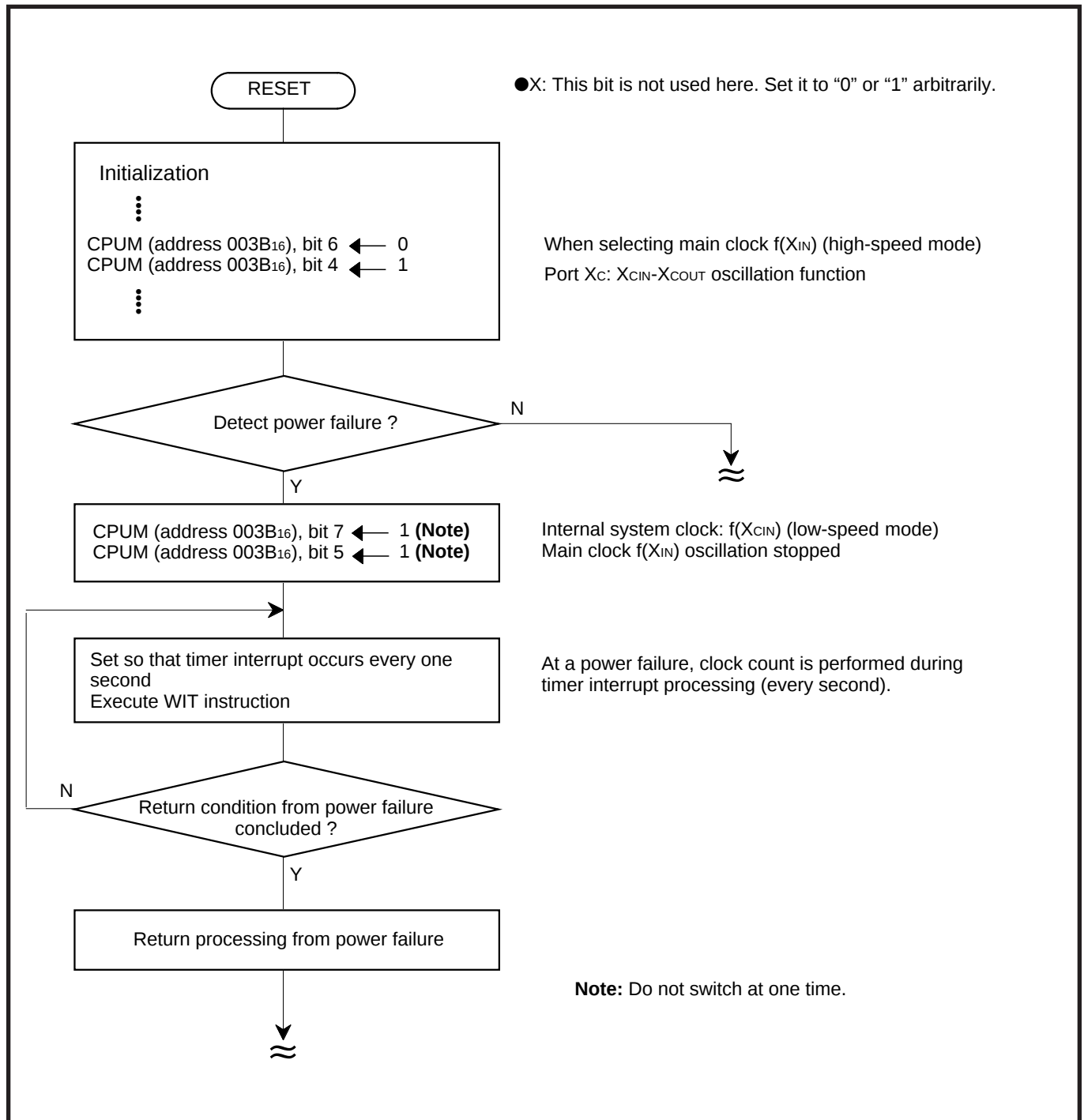


Fig. 2.11.5 Control procedure

(2) Counting without clock error during power failure

Outline: It keeps counting without clock error during a power failure.

Specifications: •Reducing power consumption as low as possible while maintaining clock function

•Clock: $f(X_{IN}) = 4.19 \text{ MHz}$

•Sub clock: $f(X_{CIN}) = 32.768 \text{ kHz}$

•Use of Timer 3 interrupt

For the peripheral circuit and the status transition during a power failure, refer to “**Figures 2.11.2 and 2.11.3**”.

Figure 2.11.6 shows the structure of clock counter, Figures 2.11.7 and 2.11.8 show the setting of relevant registers.

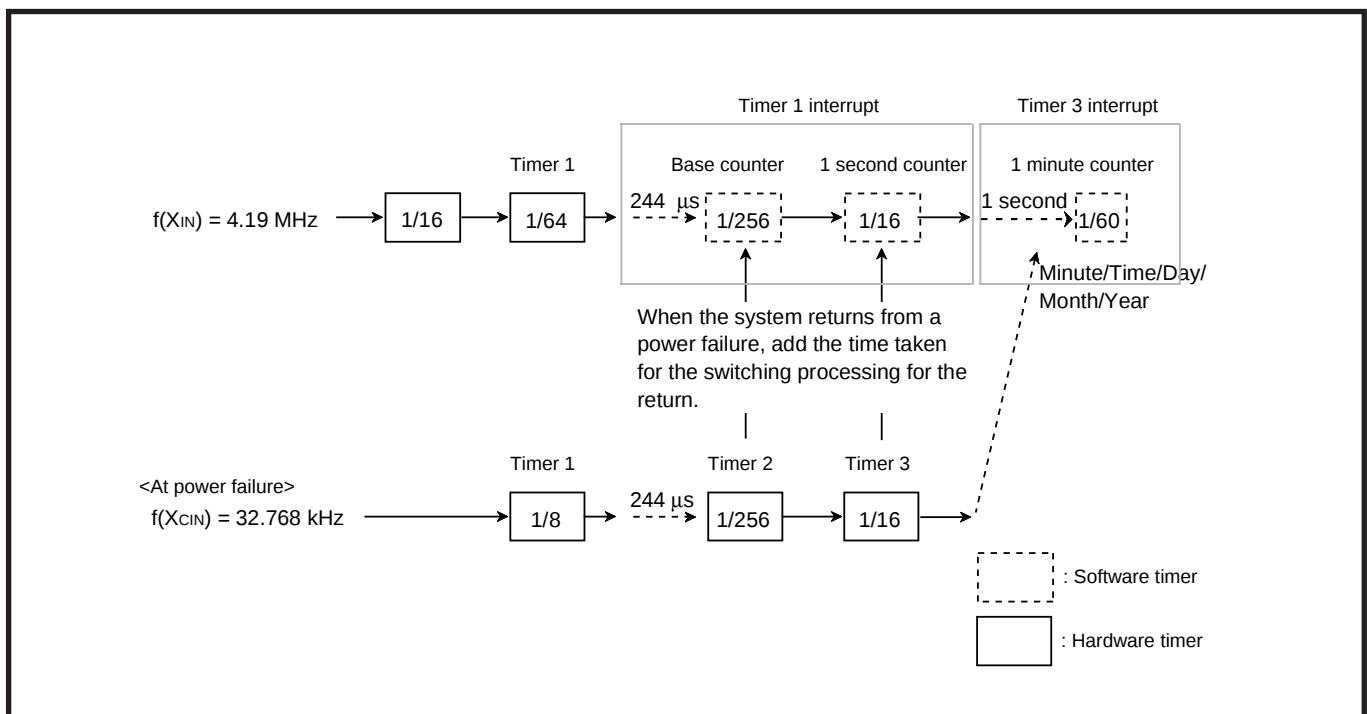


Fig. 2.11.6 Structure of clock counter

APPLICATION

2.11 Clock generating circuit

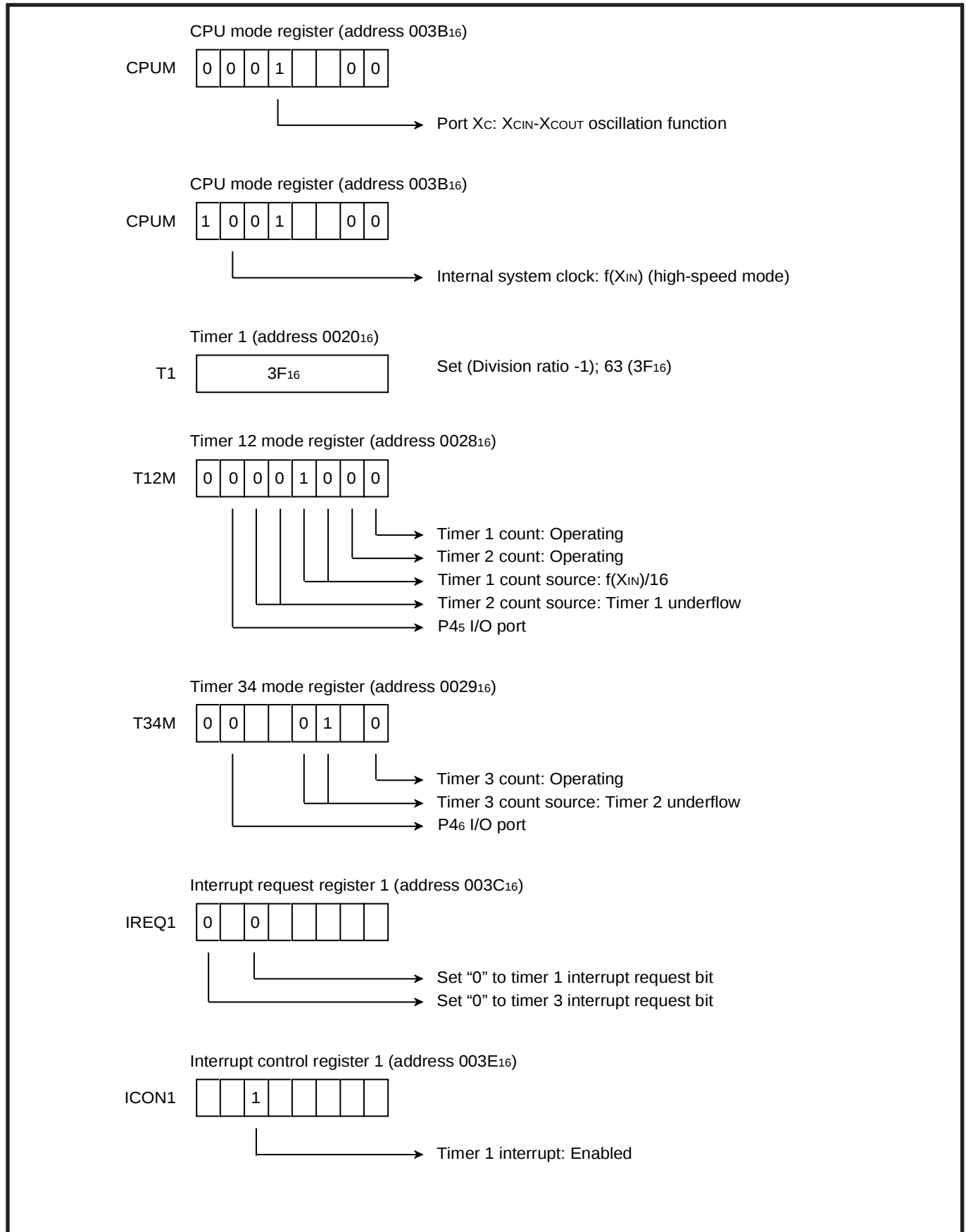


Fig. 2.11.7 Initial setting of relevant registers

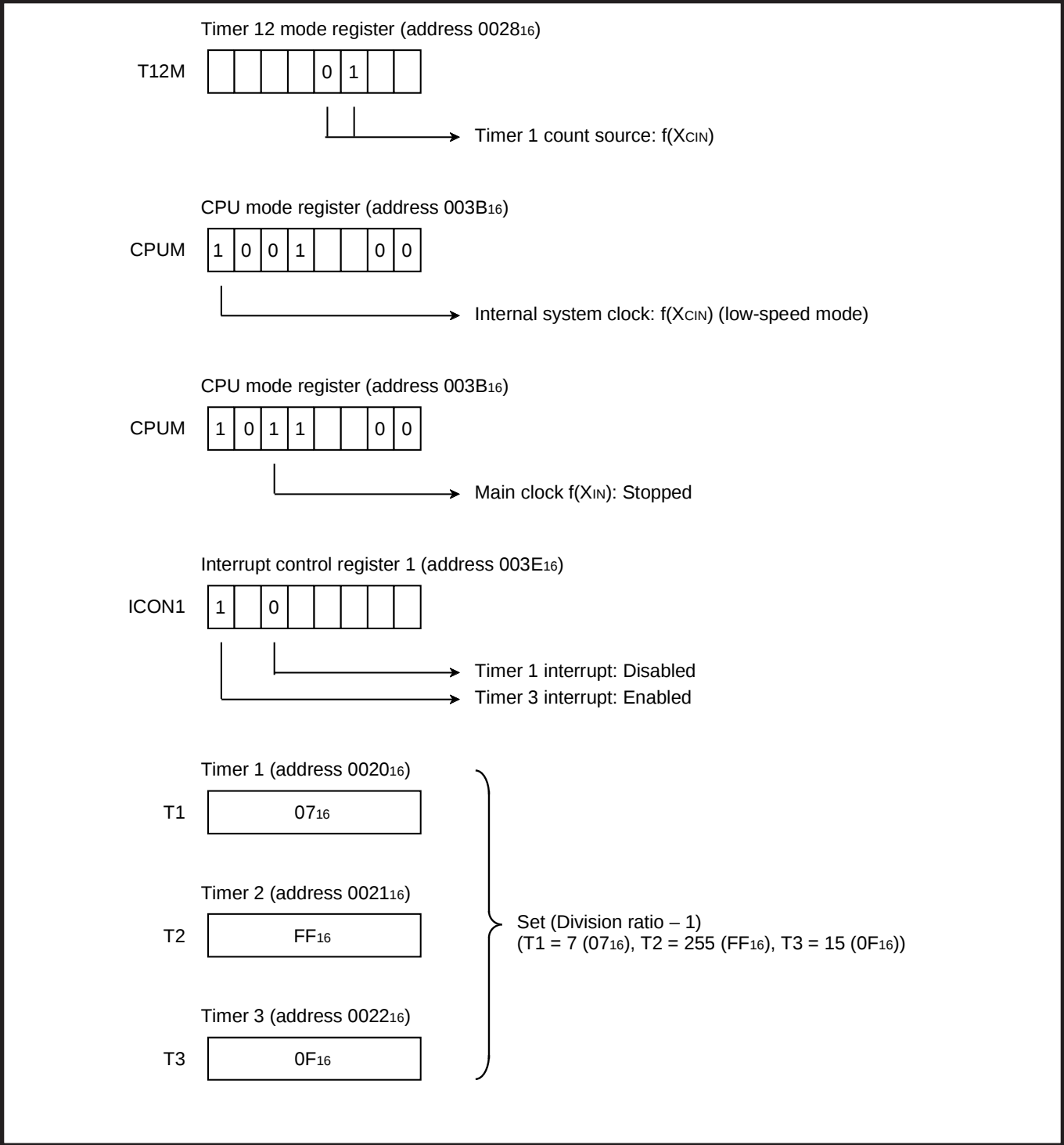


Fig. 2.11.8 Setting of relevant registers after detecting power failure

APPLICATION

2.11 Clock generating circuit

Control procedure: Set the relevant registers in the order shown below to prepare for a power failure.

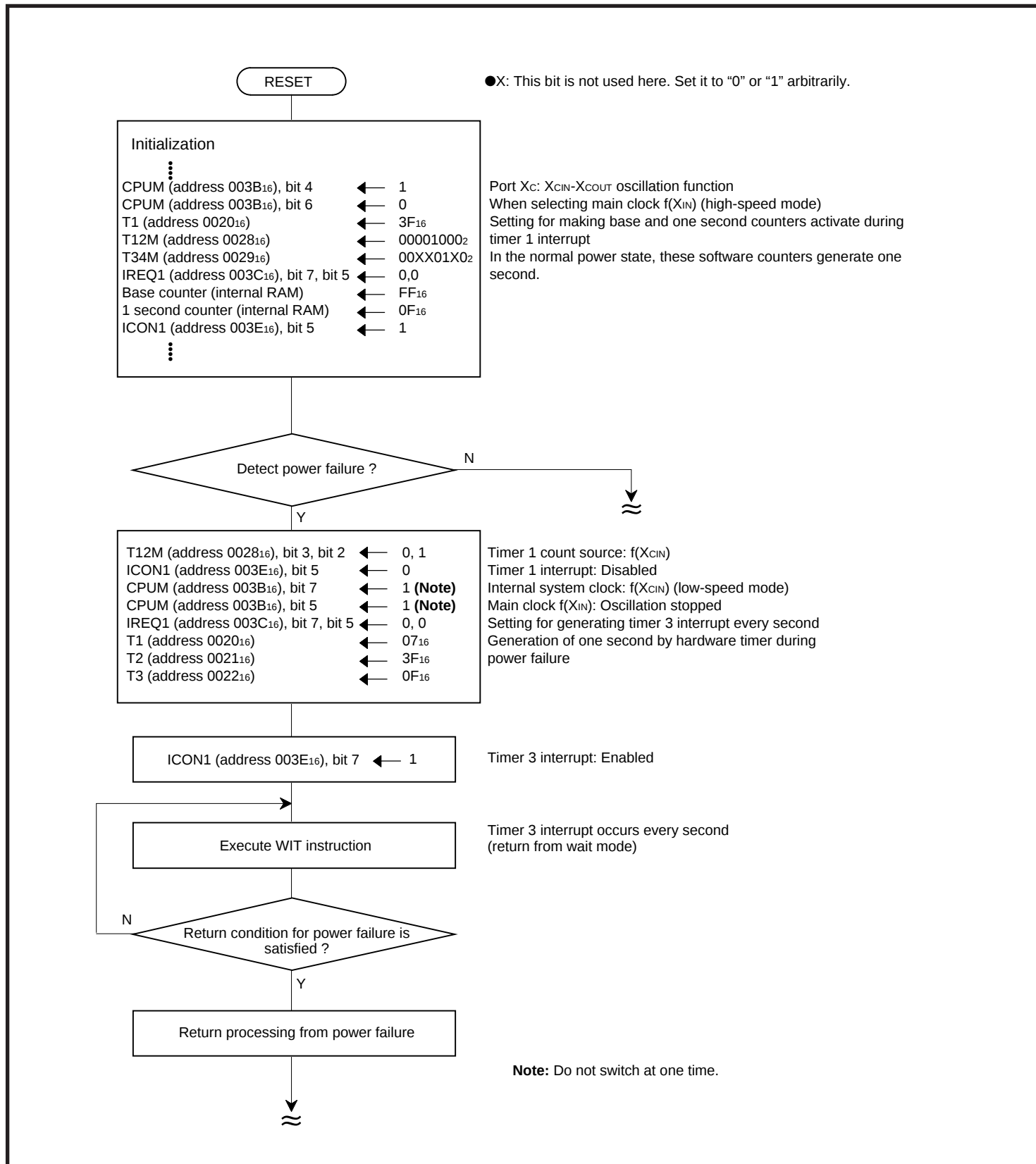
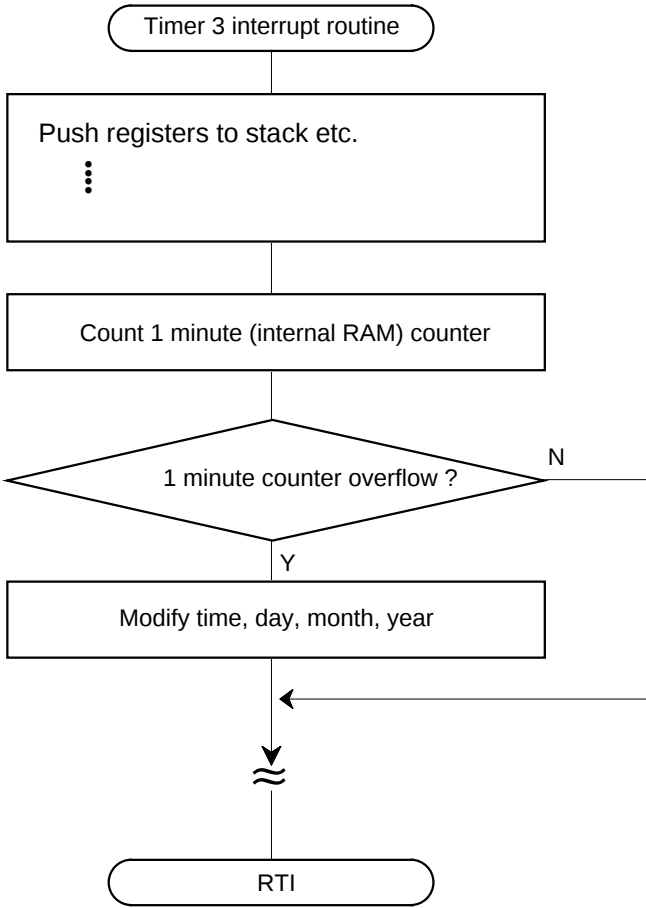


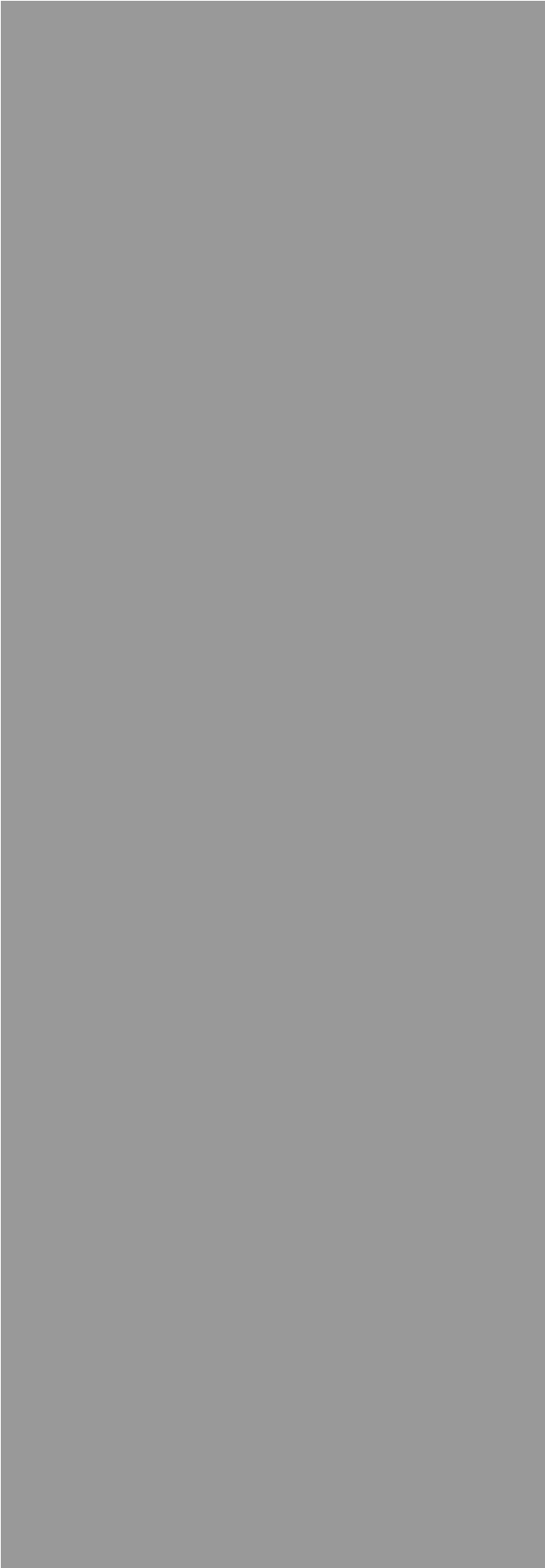
Fig. 2.11.9 Control procedure



APPLICATION

2.11 Clock generating circuit

MEMORANDUM



CHAPTER 3

APPENDIX

- 3.1 Electrical characteristics
- 3.2 Standard characteristics
- 3.3 Notes on use
- 3.4 Countermeasures against noise
- 3.5 Control registers
- 3.6 Mask ROM confirmation form
- 3.7 ROM programming confirmation form
- 3.8 Mark specification form
- 3.9 Package outline
- 3.10 List of instruction code
- 3.11 Machine instructions
- 3.12 M35501FP
- 3.13 SFR memory map
- 3.14 Pin configuration

APPENDIX

3.1 Electrical characteristics

3.1 Electrical characteristics

3.1.1 Absolute maximum ratings

Table 3.1.1 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Power source voltage	All voltages are based on V _{SS} . Output transistors are cut off.	−0.3 to 7.0	V
V _{EE}	Pull-down power source voltage		V _{CC} − 45 to V _{CC} + 0.3	V
V _I	Input voltage P47, P50–P57, P61–P65, P70–P77, P84–P87, P90, P91		−0.3 to V _{CC} + 0.3	V
V _I	Input voltage P40–P46, P60		−0.3 to 13	V
V _I	Input voltage P00–P07, P20–P27, P80–P83		V _{CC} − 45 to V _{CC} + 0.3	V
V _I	Input voltage $\overline{\text{RESET}}$, X _{IN}		−0.3 to V _{CC} + 0.3	V
V _I	Input voltage X _{CIN}		−0.3 to V _{CC} + 0.3	V
V _O	Output voltage P00–P07, P10–P17, P20–P27, P30–P37, P80–P83		V _{CC} − 45 to V _{CC} + 0.3	V
V _O	Output voltage P50–P57, P61–P65, P70–P77, P84–P87, P90, P91, X _{OUT} , X _{COUT}		−0.3 to V _{CC} + 0.3	V
V _O	Output voltage P40–P46, P60		−0.3 to 13	V
P _d	Power dissipation	T _a = −20 to 65 °C	800	mW
		T _a = 65 to 85 °C	800 − 12.5 × (T _a − 65)	mW
T _{opr}	Operating temperature		−20 to 85	°C
T _{stg}	Storage temperature		−40 to 125	°C

3.1 Electrical characteristics

3.1.2 Recommended operating conditions

Table 3.1.2 Recommended operating conditions (1)

(V_{CC} = 4.0 to 5.5 V, T_a = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Power source voltage	In high-speed mode	4.0	5.0	5.5	V
		In middle-/low-speed mode	2.7	5.0	5.5	V
V _{SS}	Power source voltage			0		V
V _{EE}	Pull-down power source voltage		V _{CC} -43		V _{CC}	V
V _{REF}	Analog reference voltage (when A-D converter is used)		2.0		V _{CC}	V
AV _{SS}	Analog power source voltage			0		V
V _{IA}	Analog input voltage	AN0-AN11	0		V _{CC}	V
V _{IH}	"H" input voltage	P40-P47, P50-P57, P60-P65, P70-P77, P90, P91	0.75V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	P84-P87	0.4V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	P00-P07	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	P20-P27, P80-P83	0.52V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	RESET	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage	XIN, XCIN	0.8V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage	P40-P47, P50-P57, P60-P65, P70-P77, P90, P91	0		0.25V _{CC}	V
V _{IL}	"L" input voltage	P84-P87	0		0.16V _{CC}	V
V _{IL}	"L" input voltage	P00-P07, P20-P27, P80-P83	0		0.2V _{CC}	V
V _{IL}	"L" input voltage	RESET	0		0.2V _{CC}	V
V _{IL}	"L" input voltage	XIN, XCIN	0		0.2V _{CC}	V
ΣIOH(peak)	"H" total peak output current (Note 1) P00-P07, P10-P17, P20-P27, P30-P37, P80-P83				-240	mA
ΣIOH(peak)	"H" total peak output current (Note 1) P50-P57, P61-P65, P70-P77, P90, P91				-60	mA
ΣIOL(peak)	"L" total peak output current (Note 1) P50-P57, P60-P65, P70-P77, P90, P91				100	mA
ΣIOL(peak)	"L" total peak output current (Note 1) P40-P46, P84-P87				60	mA
ΣIOH(avg)	"H" total average output current (Note 1) P00-P07, P10-P17, P20-P27, P30-P37, P80-P87				-120	mA
ΣIOH(avg)	"H" total average output current (Note 1) P50-P57, P61-P65, P70-P77, P90, P91				-30	mA
ΣIOL(avg)	"L" total average output current (Note 1) P50-P57, P60-P65, P70-P77, P90, P91				50	mA
ΣIOL(avg)	"L" total average output current (Note 1) P40-P46, P84-P87				30	mA
IOH(peak)	"H" peak output current (Note 2) P00-P07, P10-P17, P20-P27, P30-P37, P80-P83				-40	mA
IOH(peak)	"H" peak output current (Note 2) P50-P57, P61-P65, P70-P77, P84-P87, P90, P91				-10	mA
IOL(peak)	"L" peak output current (Note 2) P50-P57, P61-P65, P70-P77, P84-P87, P90, P91				10	mA
IOL(peak)	"L" peak output current (Note 2) P40-P46, P60				30	mA
IOH(avg)	"H" average output current (Note 3) P00-P07, P10-P17, P20-P27, P30-P37, P80-P83				-18	mA
IOH(avg)	"H" average output current (Note 3) P50-P57, P60-P65, P70-P77, P84-P87, P90, P91				-5	mA
IOL(avg)	"L" average output current (Note 3) P50-P57, P61-P65, P70-P77, P84-P87, P90, P91				5	mA
IOL(avg)	"L" average output current (Note 3) P40-P46, P60				15	mA

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current IOL (avg), IOH (avg) in an average value measured over 100 ms.

APPENDIX

3.1 Electrical characteristics

Table 3.1.3 Recommended operating conditions (2)

(V_{CC} = 4.0 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
f(CNTR0) f(CNTR1)	Clock input frequency for timers 2, 4, and X (duty cycle 50 %)			250	kHz
f(XIN)	Main clock input oscillation frequency (Note 1)			4.2	MHz
f(XCIN)	Sub-clock input oscillation frequency (Notes 1, 2)		32.768	50	kHz

Notes 1: When the oscillation frequency has a duty cycle of 50%.

2: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

3.1.3 Electrical characteristics

Table 3.1.4 Electrical characteristics (1)

(V_{CC} = 4.0 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00–P07, P10–P17, P20–P27, P30–P37, P80–P83	I _{OH} = –18 mA	V _{CC} –2.0			V
VOH	"H" output voltage P50–P57, P60–P65, P70–P77, P84–P87, P90, P91	I _{OH} = –10 mA	V _{CC} –2.0			V
VOL	"L" output voltage P50–P57, P61–P65, P84–P87, P90, P91	I _{OL} = 10 mA			2.0	V
VOL	"L" output voltage P40–P46, P60	I _{OL} = 15 mA		0.6	2.0	V
VT+–VT–	Hysteresis P40–P42, P45–P47, P5, P60, P61, P64 (Note 1)			0.4		V
VT+–VT–	Hysteresis $\overline{\text{RESET}}$, XIN			0.5		V
VT+–VT–	Hysteresis XCIN			0.5		V
I _{IH}	"H" input current P47, P50–P57, P61–P65, P70–P77, P84–P87	V _I = V _{CC}			5.0	μA
I _{IH}	"H" input current P40–P46, P60	V _I = 12 V			10.0	μA
I _{IH}	"H" input current P00–P07, P20–P27, P80–P83 (Note 2)	V _I = V _{CC}			5.0	μA
I _{IH}	"H" input current $\overline{\text{RESET}}$, XCIN	V _I = V _{CC}			5.0	μA
I _{IH}	"H" input current XIN	V _I = V _{CC}		4.0		μA
I _{IL}	"L" input current P40–P47, P60	V _I = V _{SS}			–5.0	μA
I _{IL}	"L" input current P50–P57, P61–P65, P70–P77, P84–P87, P90, P91	V _I = V _{SS} Pull-up "off"			–5.0	μA
		V _{CC} = 5 V, V _I = V _{SS} Pull-up "on"	–30	–70	–140	μA
		V _{CC} = 3 V, V _I = V _{SS} Pull-up "on"	–6.0	–25	–45	μA
I _{IL}	"L" input current P00–P07, P20–P27, P80–P83 (Note 2)	V _I = V _{SS}			–5.0	μA
I _{IL}	"L" input current $\overline{\text{RESET}}$, XCIN	V _I = V _{SS}			–5.0	μA
I _{IL}	"L" input current XIN	V _I = V _{SS}		–4.0		μA
I _{LOAD}	Output load current P00–P07, P10–P17, P30–P37	V _{EE} = V _{CC} –43 V, V _{OL} = V _{CC} Output transistors "off"	300	600	900	μA
I _{LEAK}	Output leak current P00–P07, P10–P17, P20–P27, P30–P37, P80–P83	V _{EE} = V _{CC} –43 V, V _{OL} = V _{CC} –43 V Output transistors "off"			–10	μA
I _{READH}	"H" read current P00–P07, P20–P27, P80–P83	V _I = 5 V		1		μA
V _{RAM}		When clock is stopped	2		5.5	V

Notes 1: P42, P45, P46, and P60 of the mask option type P do not have hysteresis characteristics.

2: Except when reading ports P0, P2, or P8.

3.1 Electrical characteristics

Table 3.1.5 Electrical characteristics (2)(V_{CC} = 4.0 to 5.5 V, T_a = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{CC}	Power source current	High-speed mode f(X _{IN}) = 4.2 MHz f(X _{CIN}) = 32 kHz Output transistors "off"		7.5	15	mA
		High-speed mode f(X _{IN}) = 4.2 MHz (in WIT state) f(X _{CIN}) = 32 kHz Output transistors "off"		1		mA
		Middle-speed mode f(X _{IN}) = 4.2 MHz f(X _{CIN}) = stopped Output transistors "off"		3		mA
		Middle-speed mode f(X _{IN}) = 4.2 MHz (in WIT state) f(X _{CIN}) = stopped Output transistors "off"		1		mA
		Low-speed mode f(X _{IN}) = stopped f(X _{CIN}) = 32 kHz Low-power dissipation mode (CM ₃ = 0) Output transistors "off"		60	200	μA
		Low-speed mode f(X _{IN}) = stopped f(X _{CIN}) = 32 kHz (in WIT state) Low-power dissipation mode (CM ₃ = 0) Output transistors "off"		20	40	μA
		Increment when A-D conversion is executed		0.6		mA
		All oscillation stopped (in STP state) Output transistors "off"	T _a = 25 °C	0.1	1	μA
			T _a = 85 °C		10	μA

3.1.4 A-D converter characteristics

Table 3.1.6 A-D converter characteristics(V_{CC} = 4.0 to 5.5V, V_{SS} = 0 V, T_a = -20 to 85 °C, f(X_{IN}) = 250 kHz to 4.2 MHz in high-speed mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy (excluding quantization error)	V _{CC} = V _{REF} = 5.12 V		±1	±2.5	LSB
T _{CONV}	Conversion time		61		62	tc(φ)
I _{VREF}	Reference input current	V _{REF} = 5.0 V	50	150	200	μA
I _{IA}	Analog port input current			0.5	5.0	μA
RLADDER	Ladder resistor			35		kΩ

APPENDIX

3.1 Electrical characteristics

3.1.5 Timing requirements and switching characteristics

Table 3.1.7 Timing requirements

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input “L” pulse width	2.0			μs
t _c (X _{IN})	Main clock input cycle time (X _{IN} input)	238			ns
t _{WH} (X _{IN})	Main clock input “H” pulse width	60			ns
t _{WL} (X _{IN})	Main clock input “L” pulse width	60			ns
t _c (X _{CIN})	Sub-clock input cycle time (X _{CIN} input)	20			μs
t _{WH} (X _{CIN})	Sub-clock input “H” pulse width	5.0			μs
t _{WL} (X _{CIN})	Sub-clock input “L” pulse width	5.0			μs
t _c (CNTR)	CNTR0, CNTR1 input cycle time	4.0			μs
t _{WH} (CNTR)	CNTR0, CNTR1 input “H” pulse width	1.6			μs
t _{WL} (CNTR)	CNTR0, CNTR1 input “L” pulse width	1.6			μs
t _{WH} (INT)	INT0 to INT4 input “H” pulse width	80			ns
t _{WL} (INT)	INT0 to INT4 input “L” pulse width	80			ns
t _c (SCLK)	Serial I/O clock input cycle time	0.95			μs
t _{WH} (SCLK)	Serial I/O clock input “H” pulse width	400			ns
t _{WL} (SCLK)	Serial I/O clock input “L” pulse width	400			ns
t _{su} (SCLK–SIN)	Serial I/O input set up time	200			ns
t _h (SCLK–SIN)	Serial I/O input hold time	200			ns

Table 3.1.8 Switching characteristics

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{WH} (SCLK)	Serial I/O clock output “H” pulse width	C _L = 100 pF	t _c (SCLK)/2–160			ns
t _{WL} (SCLK)	Serial I/O clock output “L” pulse width	C _L = 100 pF	t _c (SCLK)/2–160			ns
t _d (SCLK–SOUT)	Serial I/O output delay time				0.2 t _c	ns
t _v (SCLK–SOUT)	Serial I/O output valid time		0			ns
t _r (SCLK)	Serial I/O clock output rising time	C _L = 100 pF			40	ns
t _f (SCLK)	Serial I/O clock output falling time	C _L = 100 pF			40	ns
t _r (Pch–strg)	P-channel high-breakdown voltage output rising time (Note 1)	C _L = 100 pF V _{EE} = V _{CC} –43 V		55		ns
t _r (Pch–weak)	P-channel high-breakdown voltage output rising time (Note 2)	C _L = 100 pF V _{EE} = V _{CC} –43 V		1.8		μs

Notes 1: When bit 7 of the FLDC mode register (address 0EF416) is at “0”.

2: When bit 7 of the FLDC mode register (address 0EF416) is at “1”.

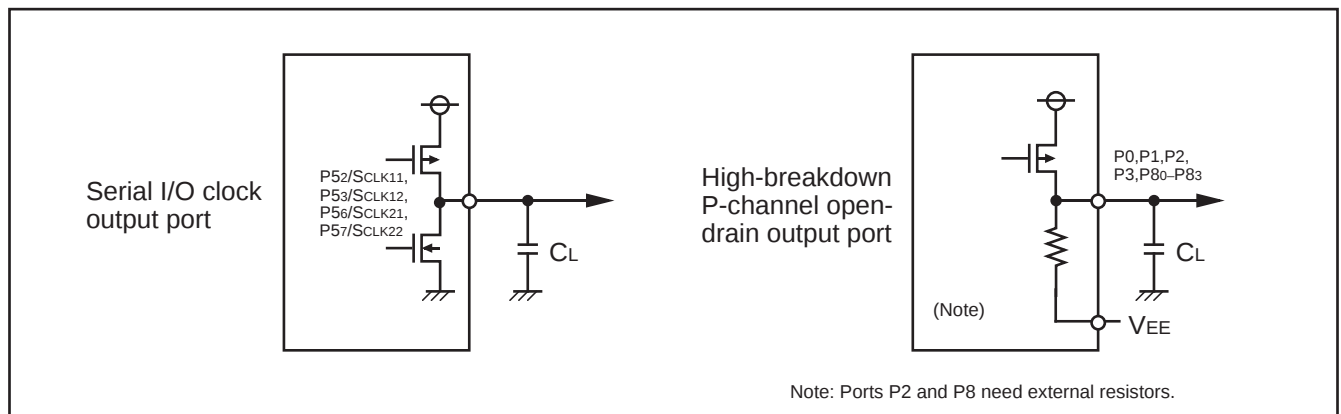


Fig. 3.1.1 Circuit for measuring output switching characteristics

Timing Diagram

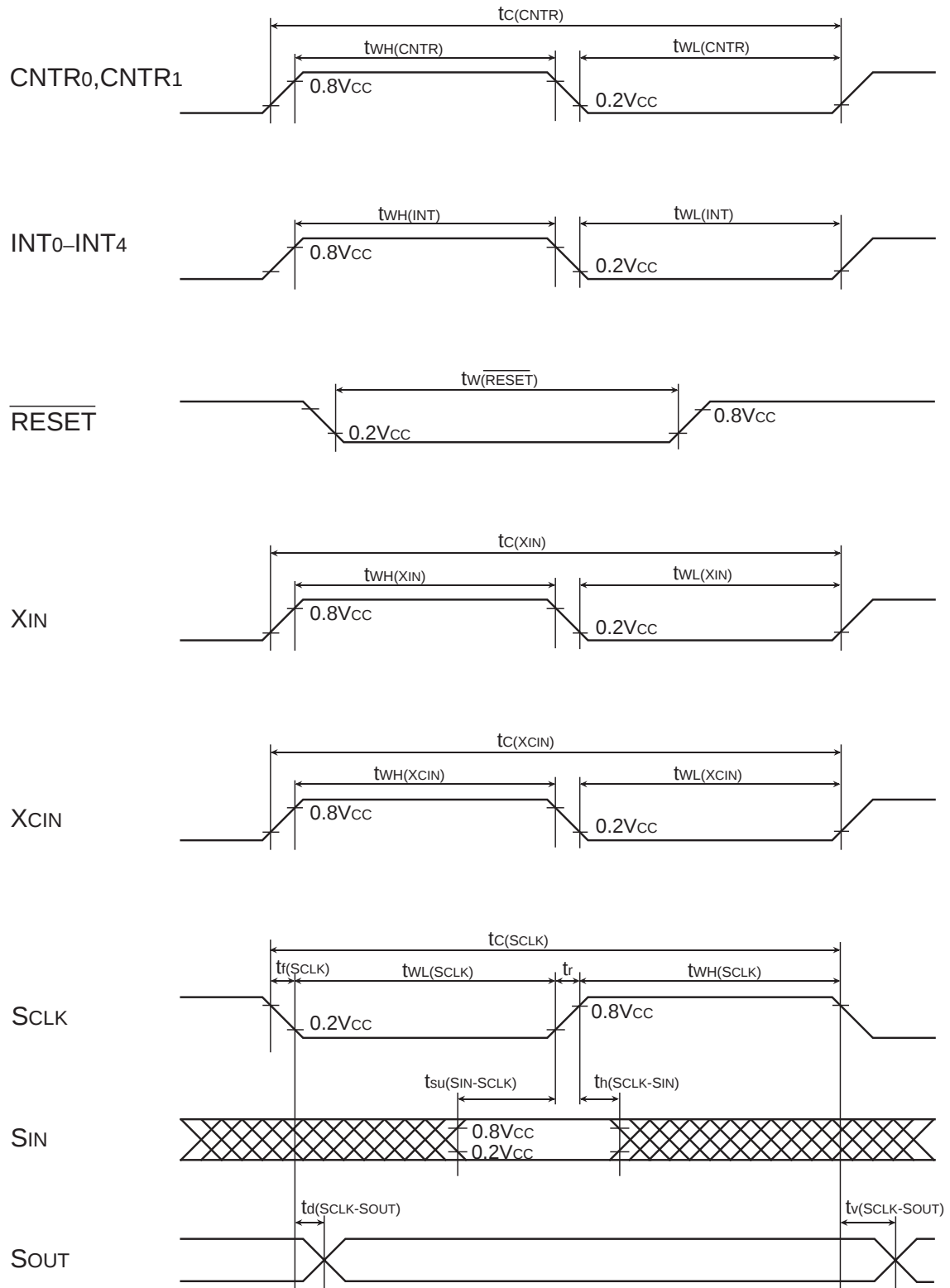


Fig. 3.1.2 Timing diagram

APPENDIX

3.2 Standard characteristics

3.2 Standard characteristics

3.2.1 Power source current standard characteristics

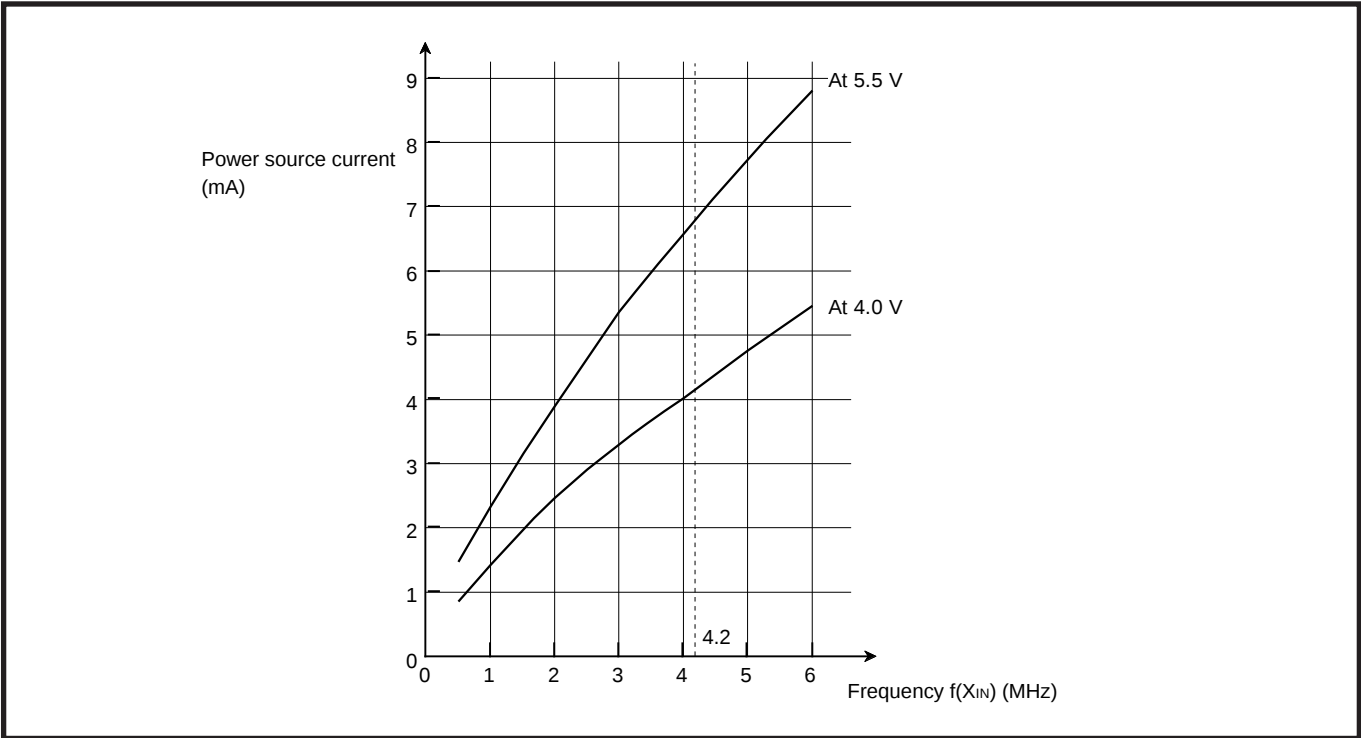


Fig. 3.2.1 Power source current standard characteristics

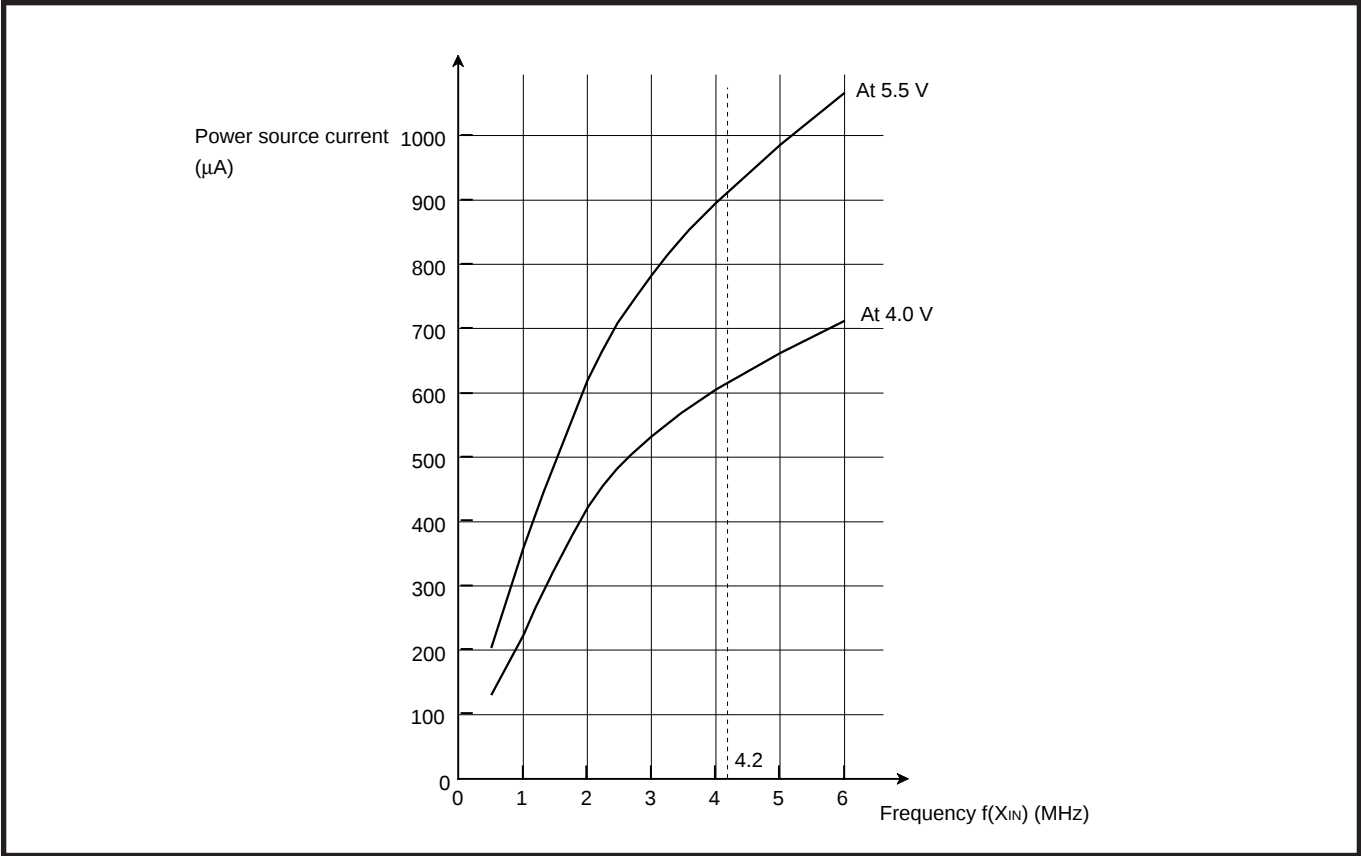


Fig. 3.2.2 Power source current standard characteristics (in wait mode)

3.2.2 Port standard characteristics

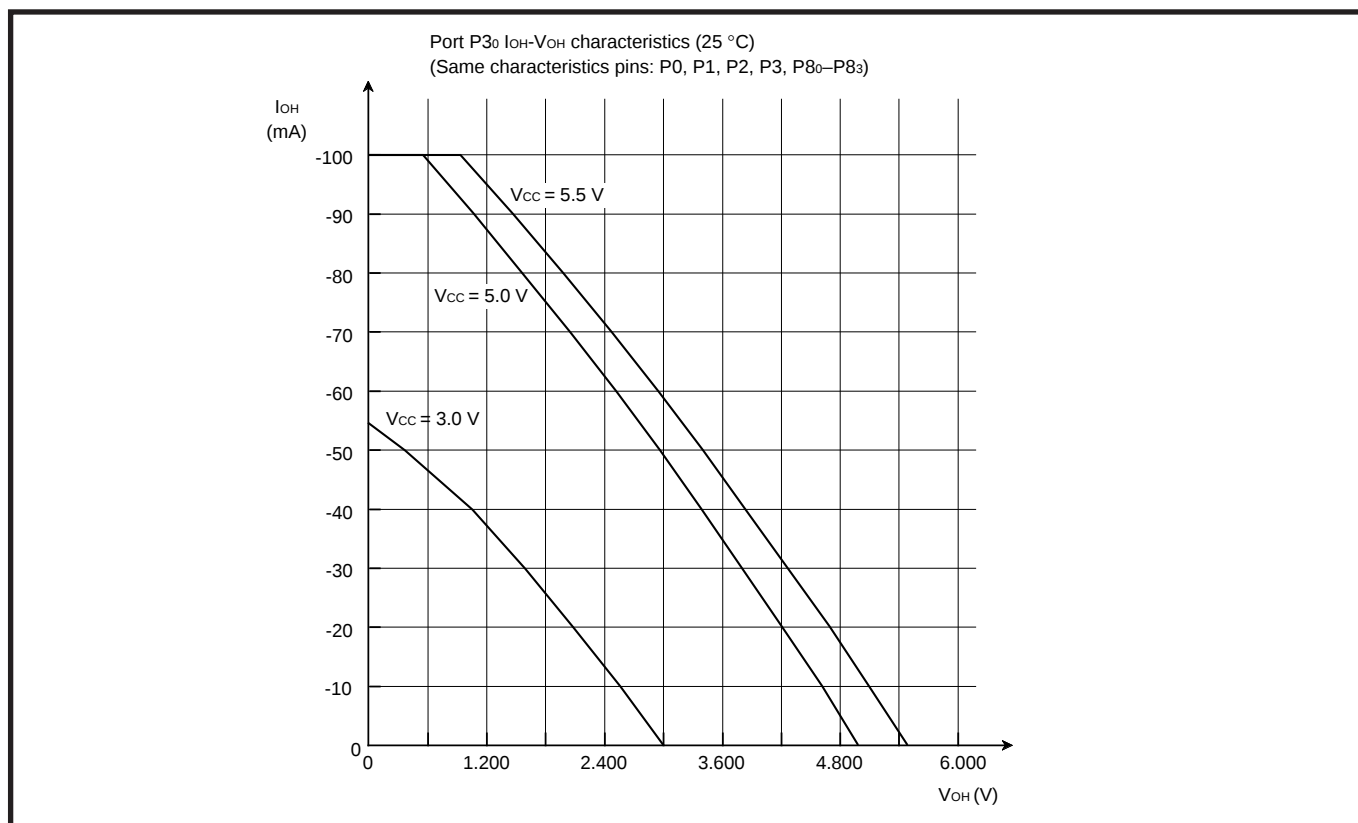


Fig. 3.2.3 High-breakdown P-channel open-drain output port characteristics (25 °C)

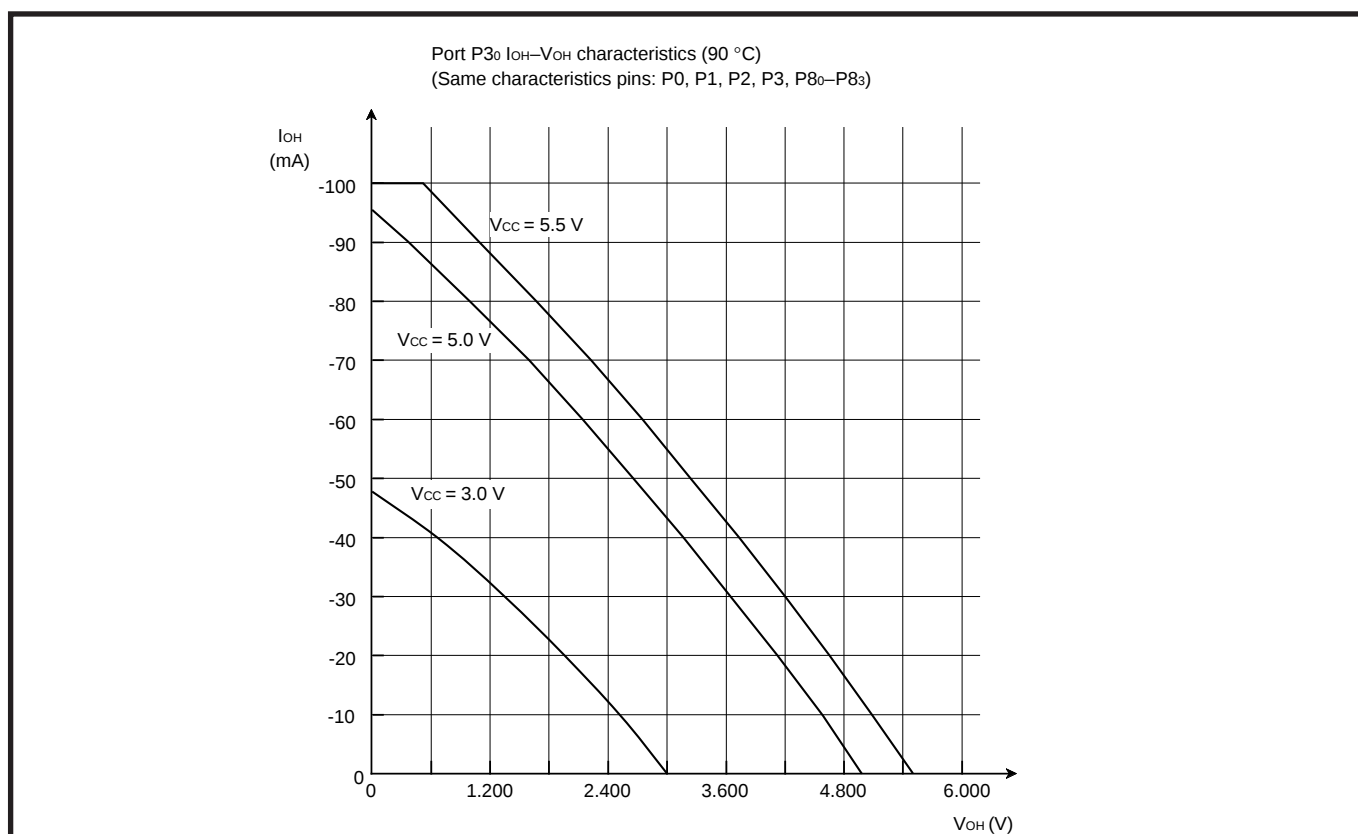


Fig. 3.2.4 High-breakdown P-channel open-drain output port characteristics (90 °C)

APPENDIX

3.2 Standard characteristics

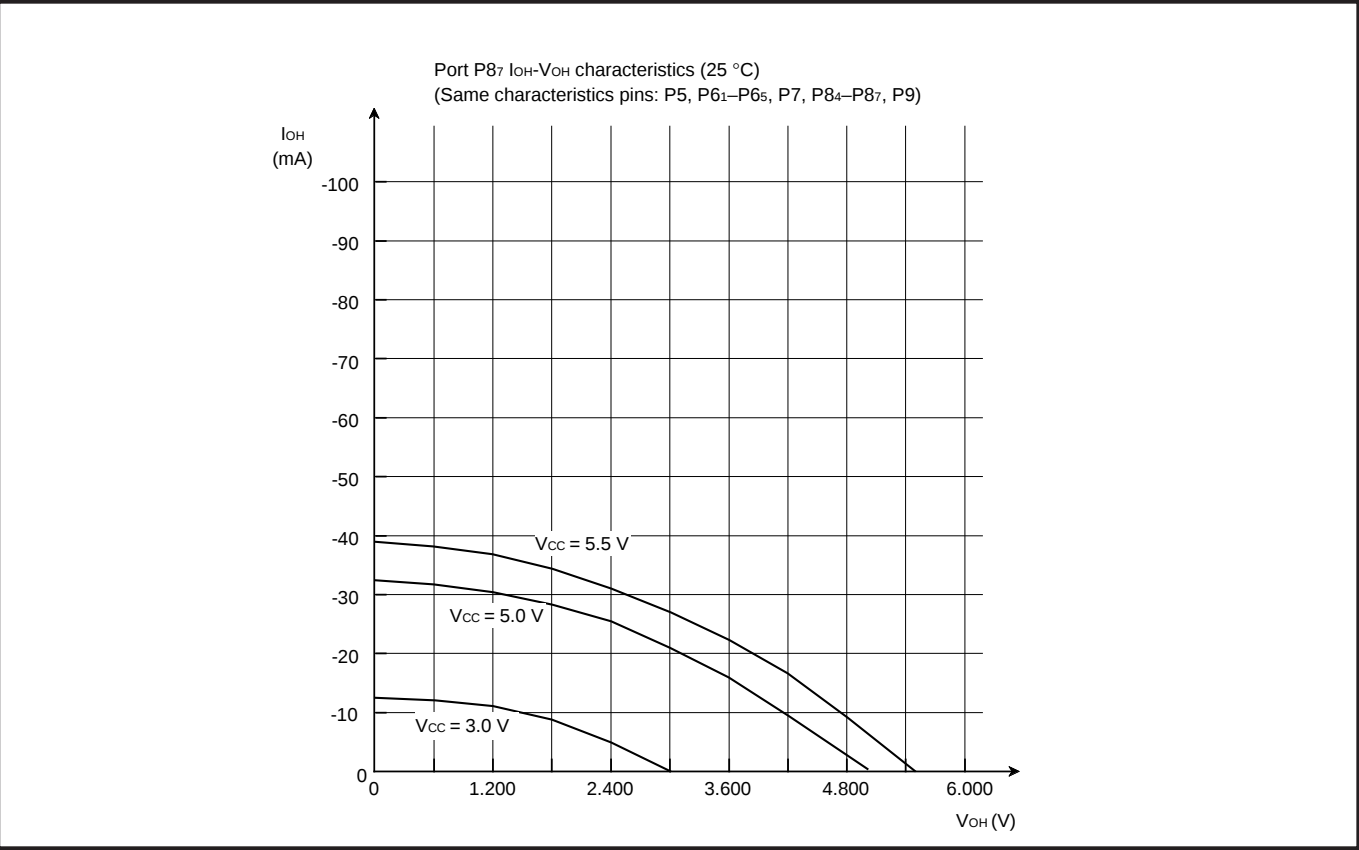


Fig. 3.2.5 CMOS output port P-channel side characteristics (25 °C)

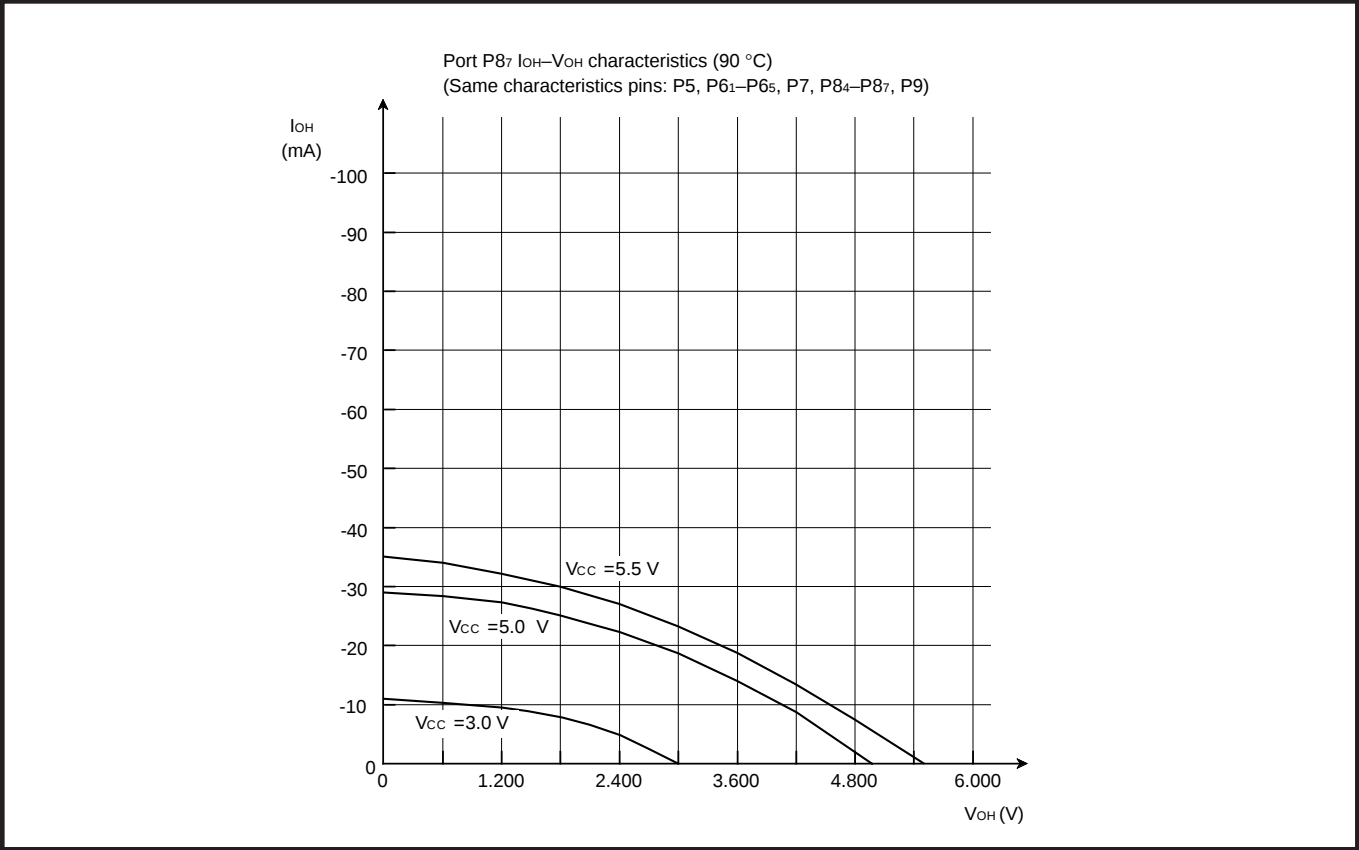


Fig. 3.2.6 CMOS output port P-channel side characteristics (90 °C)

3.2 Standard characteristics

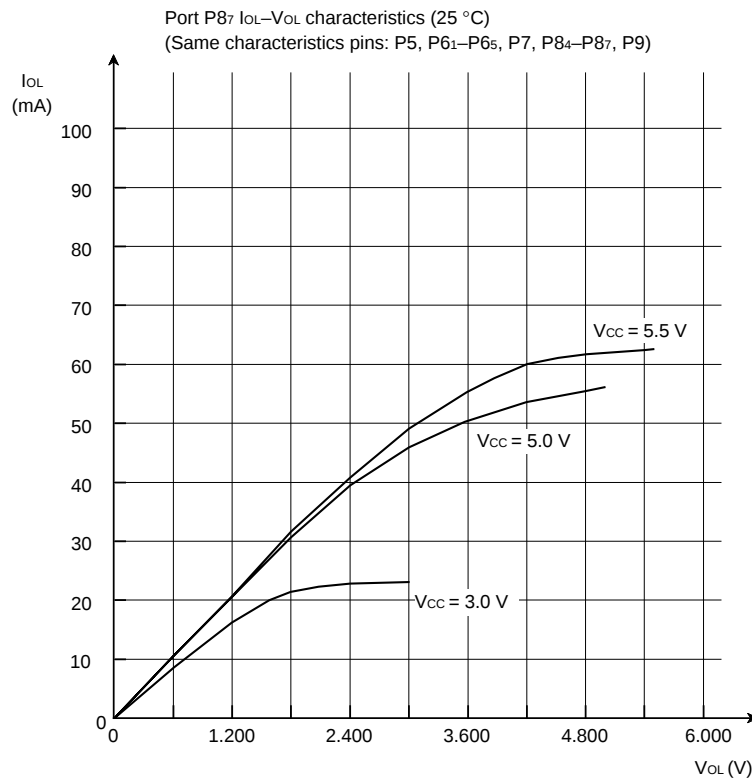


Fig. 3.2.7 CMOS output port N-channel side characteristics (25 °C)

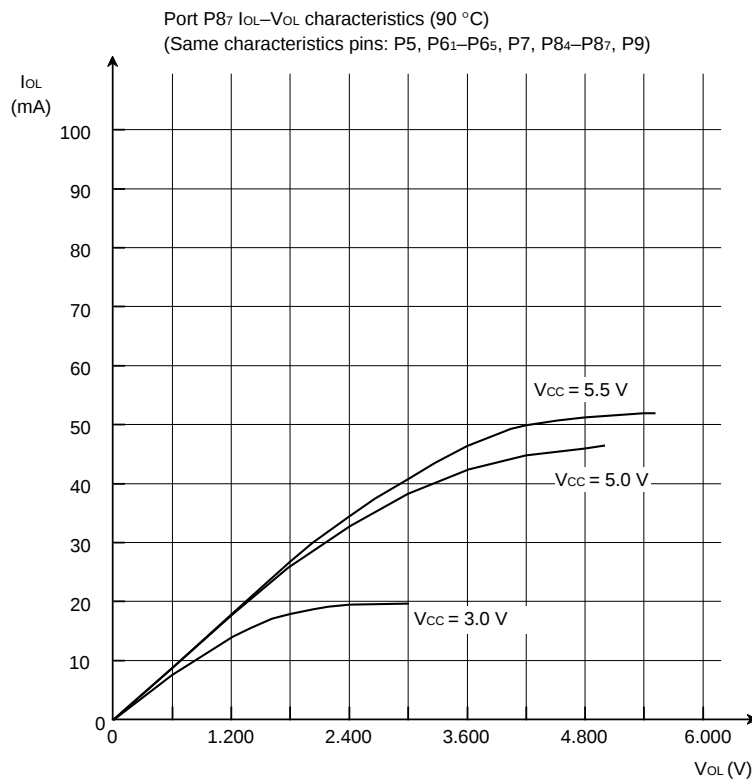


Fig. 3.2.8 CMOS output port N-channel side characteristics (90 °C)

APPENDIX

3.2 Standard characteristics

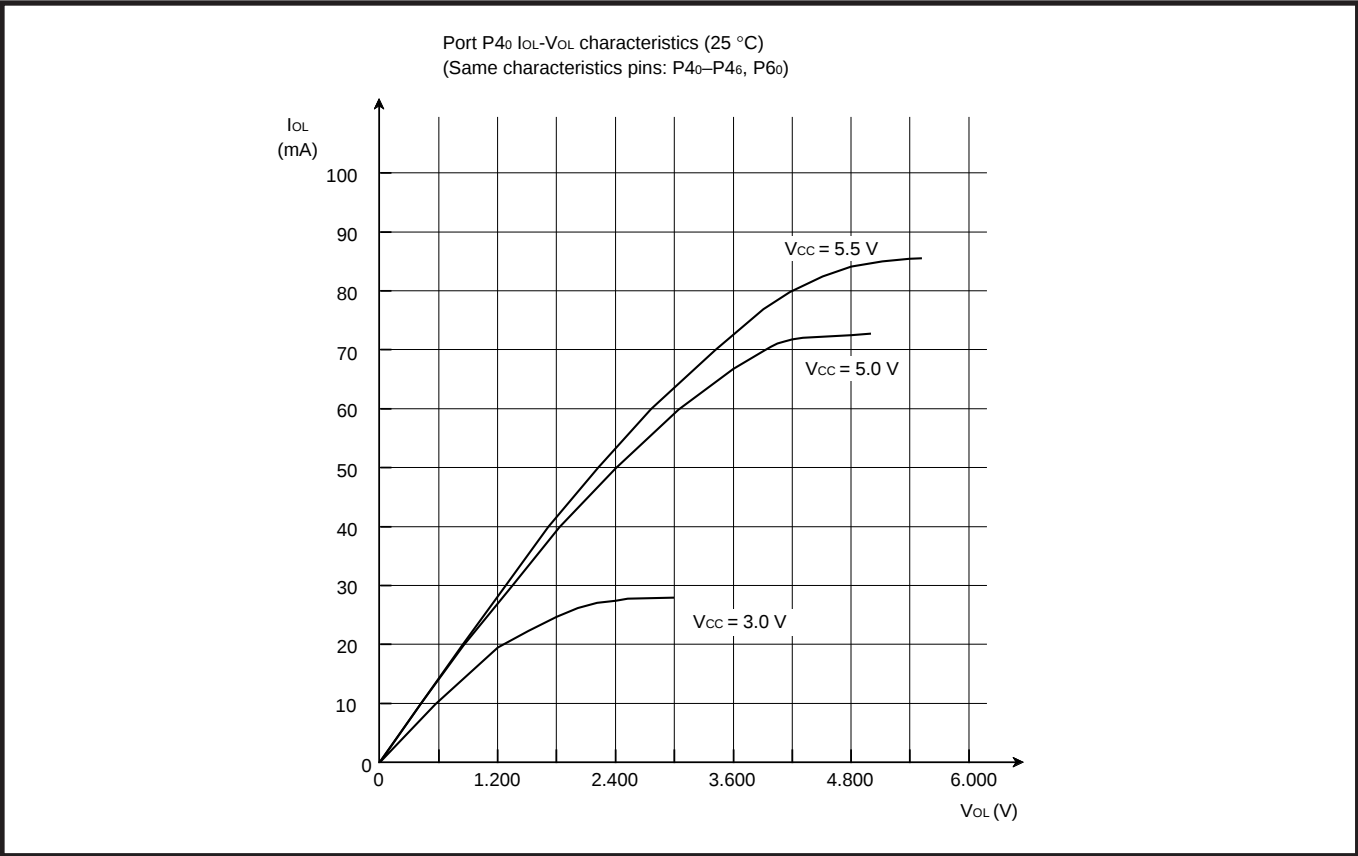


Fig. 3.2.9 N-channel open-drain output port characteristics (25 °C)

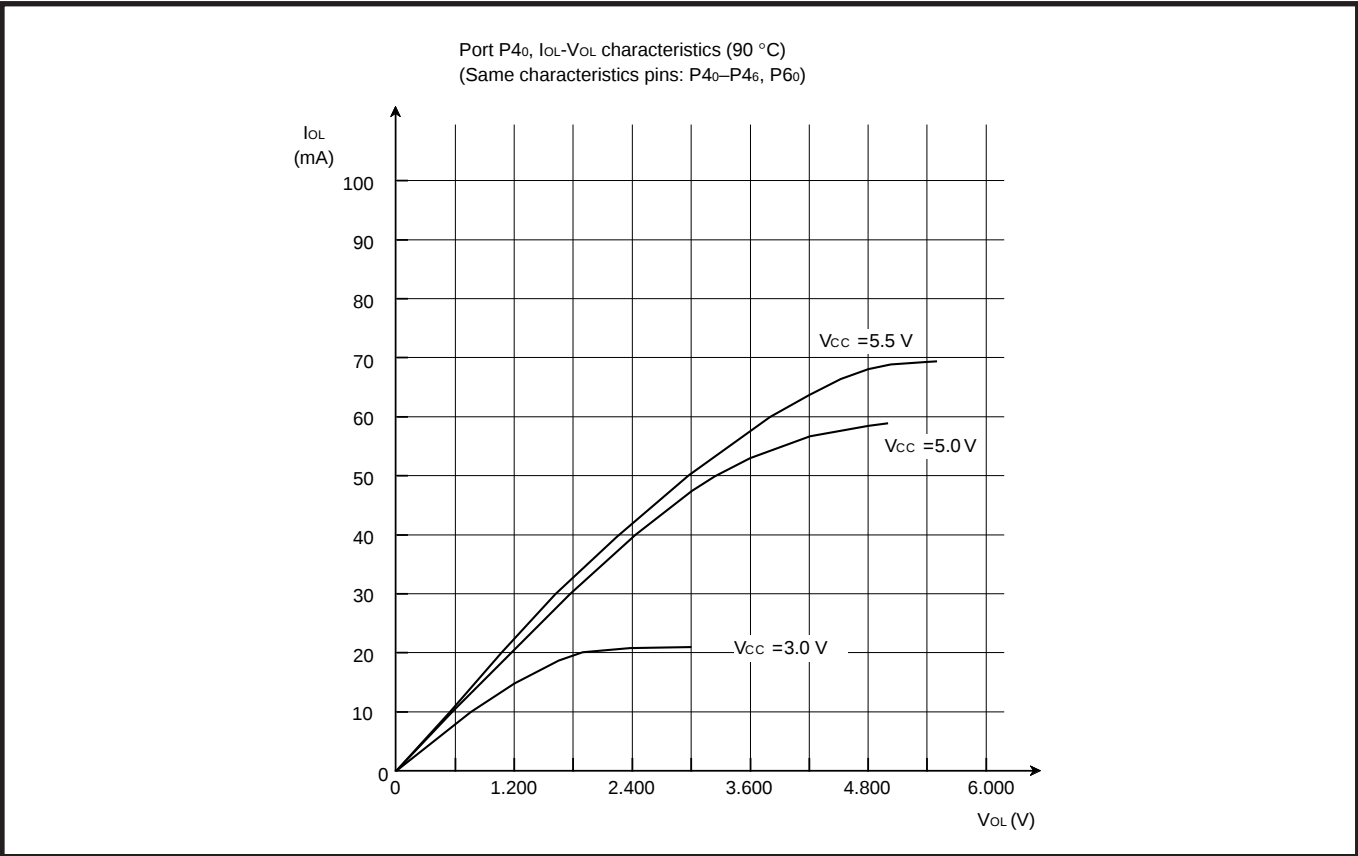


Fig. 3.2.10 N-channel open-drain output port characteristics (90 °C)

3.2.3 A-D conversion standard characteristics

Figure 3.2.11 shows the A-D conversion standard characteristics.

The lower line on the graph indicates the absolute precision error. It expresses the deviation from the ideal value. For example, the conversion of output code from 00_{16} to 01_{16} occurs ideally at the point of $AN_0 = 2.5 \text{ mV}$, but the measured value is -2 mV . Accordingly, the measured point of conversion is defined as " $2.5 - 2 = 0.5 \text{ mV}$ ".

The upper line on the graph indicates the width of input voltages equivalent to output codes. For example, the measured width of the input voltage for output code 60_{16} is 6 mV , so that the differential nonlinear error is defined as " $6 - 5 = 1 \text{ mV}$ (0.2 LSB)".

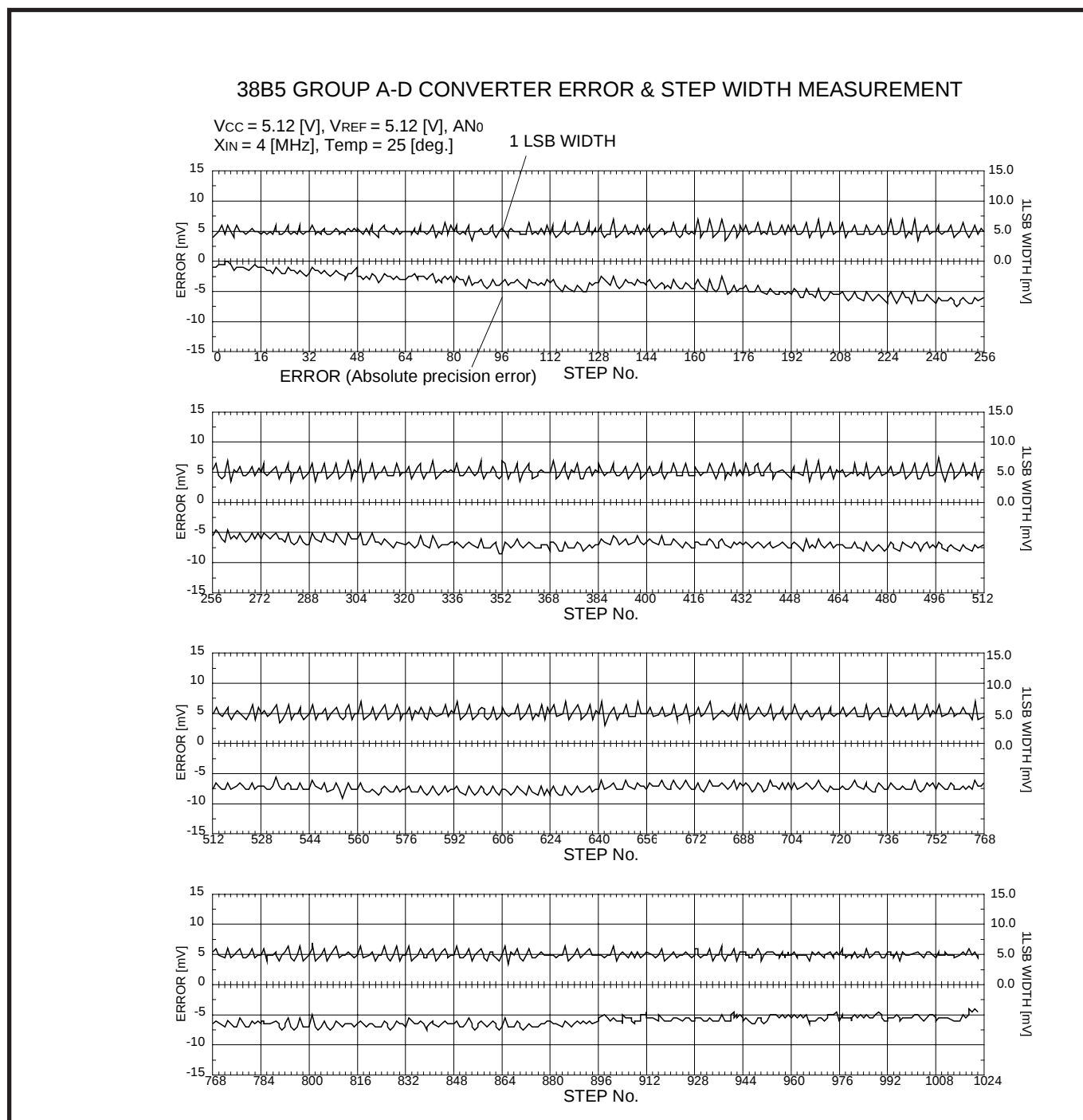


Fig. 3.2.11 A-D conversion standard characteristics

APPENDIX

3.3 Notes on use

3.3 Notes on use

3.3.1 Notes on interrupts

(1) Switching external interrupt detection edge

For the products able to switch the external interrupt detection edge, switch it as the following sequence.

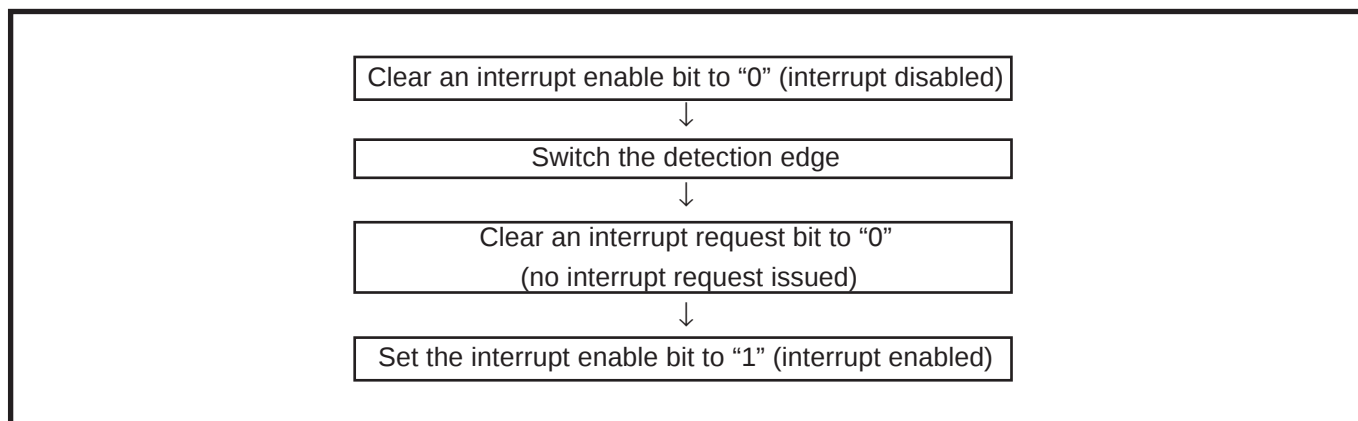


Fig. 3.3.1 Sequence of switch detection edge

■ Reason

The interrupt circuit recognizes the switching of the detection edge as the change of external input signals. This may cause an unnecessary interrupt.

(2) Check of interrupt request bit

- When executing the **BBC** or **BBS** instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to "0" by using a data transfer instruction, execute one or more instructions before executing the **BBC** or **BBS** instruction.

■ Reason

If the **BBC** or **BBS** instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to "0", the value of the interrupt request bit before being cleared to "0" is read.

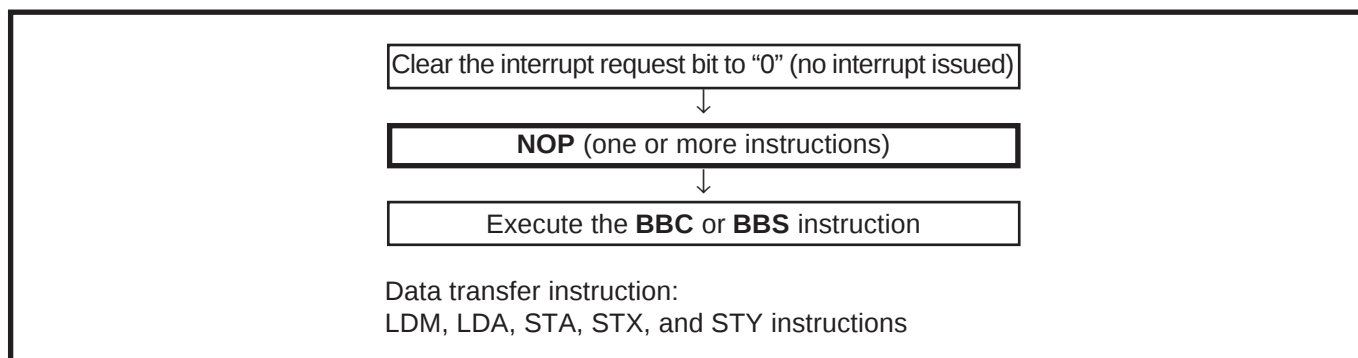


Fig. 3.3.2 Sequence of check of interrupt request bit

(3) Structure of interrupt control register 2

Fix the bit 7 of the interrupt control register 2 to "0". Figure 3.3.3 shows the structure of the interrupt control register 2.

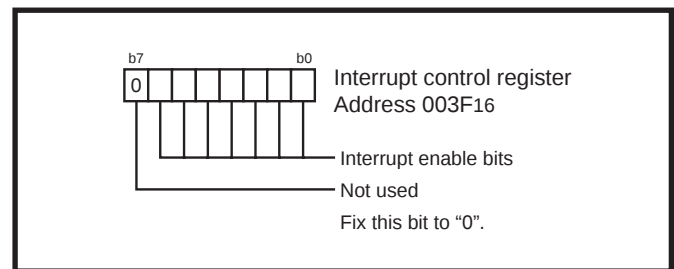


Fig. 3.3.3 Structure of interrupt control register 2

3.3.2 Notes on serial I/O1**(1) Clock****■ Using internal clock**

After setting the synchronous clock to an internal clock, clear the serial I/O interrupt request bit before perform the normal serial I/O transfer or the serial I/O automatic transfer.

■ Using external clock

After inputting "H" level to the external clock input pin, clear the serial I/O interrupt request bit before performing the normal serial I/O transfer or the serial I/O automatic transfer.

(2) Using serial I/O1 interrupt

Clear bit 3 of the interrupt request register 1 to "0" by software.

(3) State of S_{OUT1} pin

The S_{OUT1} pin control bit of the serial I/O1 control register 2 can be used to select the state of the S_{OUT1} pin when serial data is not transferred; either output active or high-impedance. However, when selecting an external synchronous clock; the S_{OUT1} pin can become the high-impedance state by setting the S_{OUT1} pin control bit to "1" when the serial I/O1 clock input is at "H" after transfer completion.

(4) Serial I/O initialization bit

- Set "0" to the serial I/O initialization bit of the serial I/O1 control register 1 when terminating a serial transfer during transferring.
- When writing "1" to the serial I/O initialization bit, the serial I/O1 is enabled, but each register is not initialized. Set the value of each register by program.

(5) Handshake signal**■ S_{BUSY1} input signal**

Input an "H" level to the S_{BUSY1} input and an "L" level signal to the $\overline{\text{S}}_{\text{BUSY1}}$ input in the initial state. When the external synchronous clock is selected, switch the input level to the S_{BUSY1} input and the $\overline{\text{S}}_{\text{BUSY1}}$ input while the serial I/O1 clock input is in "H" state.

■ S_{RDY1} input-output signal

When selecting the internal synchronous clock, input an "L" level to the S_{RDY1} input and an "H" level signal to the $\overline{\text{S}}_{\text{RDY1}}$ input in the initial state.

(6) 8-bit serial I/O mode**■ When selecting external synchronous clock**

When an external synchronous clock is selected, the contents of the serial I/O1 register are being shifted continually while the transfer clock is input to the serial I/O1 clock pin. In this case, control the clock externally.

APPENDIX

3.3 Notes on use

(7) In automatic transfer serial I/O mode

■ Set of automatic transfer interval

- When the S_{BUSY1} output is used, and the S_{BUSY1} output and the S_{STB1} output function as signals for each transfer data set by the S_{BUSY1} output• S_{STB1} output function selection bit of serial I/O1 control register 2; the transfer interval is inserted before the first data is transmitted/received, and after the last data is transmitted/received. Accordingly, regardless of the contents of the S_{BUSY1} output• S_{STB1} output function selection bit, this transfer interval for each 1-byte data becomes 2 cycles longer than the value set by the automatic transfer interval set bits of serial I/O1 control register 3.
- When using the S_{STB1} output, regardless of the contents of the S_{BUSY1} output• S_{STB1} output function selection bit, this transfer interval for each 1-byte data becomes 2 cycles longer than the value set by the automatic transfer interval set bits of serial I/O1 control register 3.
- When using the combined output of S_{BUSY1} and S_{STB1} as the signal for each of all transfer data set, the transfer interval after completion of transmission/reception of the last data becomes 2 cycles longer than the value set by the automatic transfer interval set bits.
- Set the transfer interval of each 1-byte data transfer to 5 or more cycles of the internal clock ϕ after the rising edge of the last bit of a 1-byte data.
- When selecting an external clock, the set of automatic transfer interval becomes invalid.

■ Set of serial I/O1 transfer counter

- Write the value decreased by 1 from the number of transfer data bytes to the serial I/O1 transfer counter.
- When selecting an external clock, after writing a value to the serial I/O1 register/transfer counter, wait for 5 or more cycles of internal clock ϕ before inputting the transfer clock to the serial I/O1 clock pin.

■ Serial I/O initialization bit

A serial I/O1 automatic transfer interrupt request occurs when “0” is written to the serial I/O initialization bit during an operation. Disable it with the interrupt enable bit as necessary by program.

3.3.3 Notes on serial I/O2

(1) Notes when selecting clock synchronous serial I/O

① Stop of transmission operation

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the transmit enable bit to “0” (transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O2 enable bit is cleared to “0” (serial I/O2 disabled), the internal transmission is running (in this case, since pins TxD, RxD, S_{CLK21} , S_{CLK22} and S_{RDY2} function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O2 enable bit is set to “1” at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

② Stop of receive operation

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the receive enable bit to “0” (receive disabled), or clear the serial I/O2 enable bit to “0” (serial I/O2 disabled).

③ Stop of transmit/receive operation

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, simultaneously clear both the transmit enable bit and receive enable bit to "0" (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

● Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O2 enable bit to "0" (serial I/O2 disabled) (refer to (1), ①).

(2) Notes when selecting clock asynchronous serial I/O**① Stop of transmission operation**

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the transmit enable bit to "0" (transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O2 enable bit is cleared to "0" (serial I/O2 disabled), the internal transmission is running (in this case, since pins TxD, RxD, S_{CLK21}, S_{CLK22} and S_{RDY2} function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O2 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

② Stop of receive operation

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the receive enable bit to "0" (receive disabled).

③ Stop of transmit/receive operation**Only transmission operation is stopped.**

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the transmit enable bit to "0" (transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O2 enable bit is cleared to "0" (serial I/O2 disabled), the internal transmission is running (in this case, since pins TxD, RxD, S_{CLK21}, S_{CLK22} and S_{RDY2} function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O2 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD pin and an operation failure occurs.

Only receive operation is stopped.

As for the serial I/O2 that can be used as either a clock synchronous or an asynchronous (UART) serial I/O, clear the receive enable bit to "0" (receive disabled).

(3) S_{RDY2} output of reception side

When signals are output from the S_{RDY2} pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the S_{RDY2} output enable bit, and the transmit enable bit to "1" (transmit enabled).

APPENDIX

3.3 Notes on use

(4) Setting serial I/O2 control register again

Set the serial I/O2 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0."

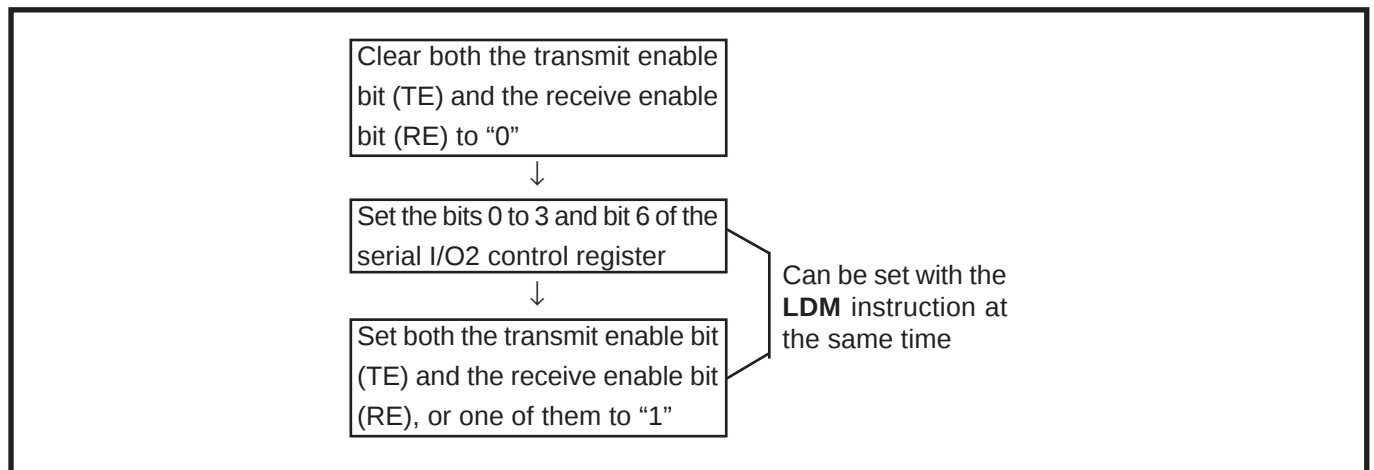


Fig. 3.3.4 Sequence of setting serial I/O2 control register again

(5) Data transmission control with referring to transmit shift register completion flag

The transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

(6) Transmission control when external clock is selected

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the serial I/O2 clock input level. Also, write the transmit data to the transmit buffer register (serial I/O shift register) at "H" of the serial I/O2 clock input level.

(7) Transmit interrupt request when transmit enable bit is set

The transmission interrupt request bit is set and the interruption request is generated even when selecting timing that either of the following flags is set to "1" as timing where the transmission interruption is generated.

- Transmit buffer empty flag is set to "1"
- Transmit shift register completion flag is set to "1"

Therefore, when the transmit interrupt is used, set the transmit interrupt enable bit to transmit enabled as the following sequence.

- ① Transmit enable bit is set to "1"
- ② Transmit interrupt request bit is set to "0"

● Reason

When the transmission enable bit is set to "1", the transmit buffer empty flag and transmit shift register completion flag are set to "1".

(8) Using TxD pin

The P5s/TxD P-channel output disable bit of UART control register is valid in both cases: using as a normal I/O port and as the TxD pin. Do not supply $V_{cc} + 0.3$ V or more even when using the P5s/TxD pin as an N-channel open-drain output.

Additionally, in the serial I/O2, the TxD pin latches the last bit and continues to output it after completing transmission.

3.3.4 Notes on FLD controller

- Set a value of 03₁₆ or more to the Toff1 time set register.
- When displaying in the gradation display mode, select the 16 timing mode by the timing number control bit (bit 4 of FLDC mode register (address 0EF4₁₆) = "0").

3.3.5 Notes on A-D converter

(1) Analog input pin

- Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 μ F to 1 μ F. Further, be sure to verify the operation of application products on the user side.

● Reason

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A-D conversion precision to be worse.

- When the P6₄/INT₄/S_{BUSY1}/AN₁₀ pin is selected as analog input pin, external interrupt function (INT₄) becomes invalid.

(2) A-D converter power source pin

The AVss pin is A-D converter power source pin. Regardless of using the A-D conversion function or not, connect it as following :

- AVss : Connect to the Vss line

● Reason

If the AVss pin is opened, the microcomputer may have a failure because of noise or others.

(3) Clock frequency during A-D conversion

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. Thus, make sure the following during an A-D conversion.

- $f(X_{IN})$ is 250 kHz or more
- Use clock divided by main clock ($f(X_{IN})$) as internal system clock.
- Do not execute the **STP** instruction and **WIT** instruction

3.3.6 Notes on PWM

- For PWM₀ output, "L" level is output first.
- After data is set to the PWM register (low-order) and the PWM register (high-order), PWM waveform corresponding to new data is output from next repetitive cycle.

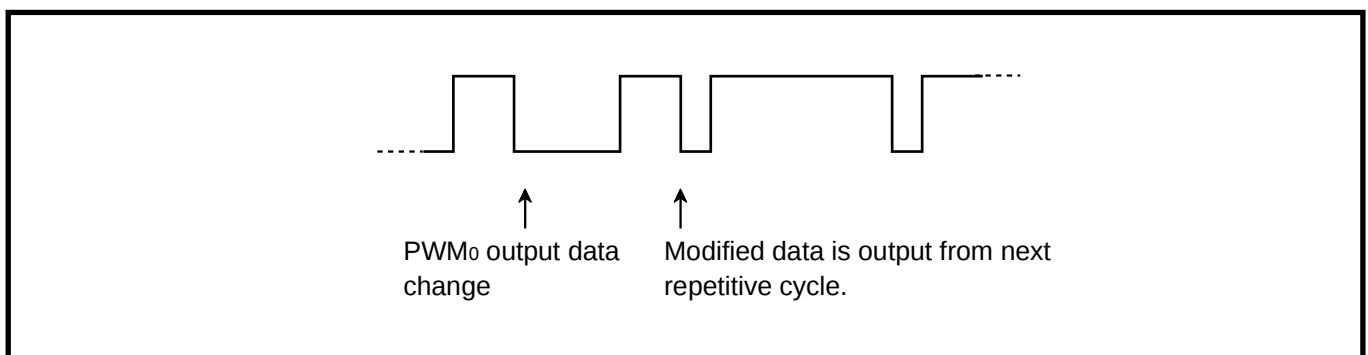


Fig. 3.3.5 PWM output

APPENDIX

3.3 Notes on use

3.3.7 Notes on watchdog timer

- The watchdog timer continues to count even while waiting for stop release. Accordingly, make sure that watchdog timer does not underflow during this term by writing to the watchdog timer control register (address 002B₁₆) once before executing the STP instruction, etc.
- Once a “1” is written to the STP instruction disable bit (bit 6) of the watchdog timer control register (address 002B₁₆), it cannot be programmed to “0” again. This bit becomes “0” after reset.

3.3.8 Notes on reset circuit

(1) Reset input voltage control

Make sure that the reset input voltage is 0.5 V or less for V_{CC} of 2.7 V.

Perform switch to the high-speed mode when power source voltage is within 4.0 to 5.5 V.

(2) Countermeasure when $\overline{\text{RESET}}$ signal rise time is long

In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the V_{SS} pin. And use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following :

- Make the length of the wiring which is connected to a capacitor as short as possible.
- Be sure to verify the operation of application products on the user side.

● Reason

If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

3.3.9 Notes on input and output pins

(1) Notes in stand-by state

In stand-by state*¹ for low-power dissipation, do not make input levels of an input port and an I/O port “undefined”, especially for I/O ports of the N-channel open-drain.

Pull-up (connect the port to V_{CC}) or pull-down (connect the port to V_{SS}) these ports through a resistor.

When determining a resistance value, note the following points:

- External circuit
- Variation of output levels during the ordinary operation

When using built-in pull-up resistor, note on varied current values:

- When setting as an input port : Fix its input level
- When setting as an output port : Prevent current from flowing out to external

● Reason

Even when setting as an output port with its direction register, in the following state :

- P-channel.....when the content of the port latch is “0”
- N-channel.....when the content of the port latch is “1”

the transistor becomes the OFF state, which causes the ports to be the high-impedance state. Note that the level becomes “undefined” depending on external circuits.

Accordingly, the potential which is input to the input buffer in a microcomputer is unstable in the state that input levels of a input port and an I/O port are “undefined”. This may cause power source current.

*¹ stand-by state : the stop mode by executing the **STP** instruction
the wait mode by executing the **WIT** instruction

(2) N-channel open-drain port

P4₀–P4₂, P4₅, P4₆, P6₀ of N-channel open-drain output ports have built-in hysteresis circuit for input. In standby state for low-power dissipation, do not make these pins floating state.

● Reason

When power sources for pull-up of these pins are cut off in standby state, these ports become floating. Accordingly, a current may flow from Vcc to Vss through built-in hysteresis circuit.

(3) Modifying output data with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction*², the value of the unspecified bit may be changed.

● Reason

The bit managing instructions are read-modify-write form instructions for reading and writing data by a byte unit. Accordingly, when these instructions are executed on a bit of the port latch of an I/O port, the following is executed to all bits of the port latch.

- As for a bit which is set for an input port :
The pin state is read in the CPU, and is written to this bit after bit managing.
- As for a bit which is set for an output port :
The bit value of the port latch is read in the CPU, and is written to this bit after bit managing.

Note the following :

- Even when a port which is set as an output port is changed for an input port, its port latch holds the output data.
- As for a bit of the port latch which is set for an input port, its value may be changed even when not specified with a bit managing instruction in case where the pin state differs from its port latch contents.

*² bit managing instructions : **SEB**, and **CLB** instructions

APPENDIX

3.3 Notes on use

3.3.10 Notes on programming

(1) Processor status register

① **Initializing of processor status register**

Flags which affect program execution must be initialized after a reset. In particular, it is essential to initialize the T and D flags because they have an important effect on calculations.

● **Reason**

After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1".

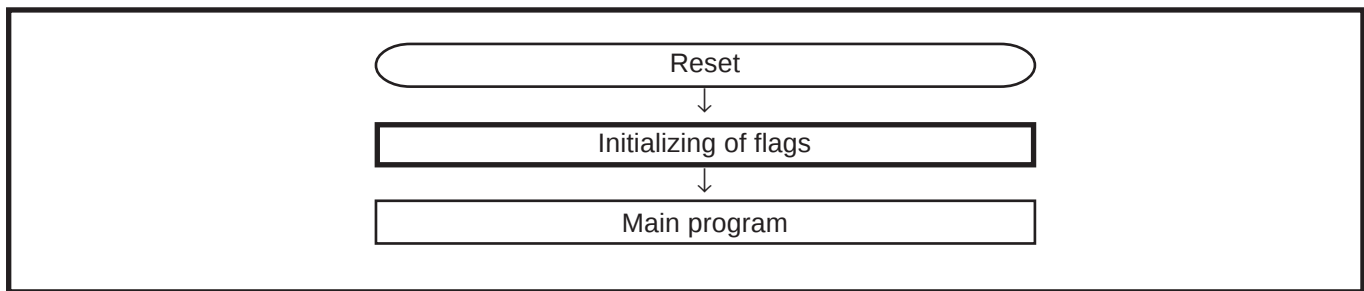


Fig. 3.3.6 Initialization of processor status register

② **How to reference the processor status register**

To reference the contents of the processor status register (PS), execute the **PHP** instruction once then read the contents of (S+1). If necessary, execute the **PLP** instruction to return the PS to its original status.

A **NOP** instruction should be executed after every **PLP** instruction.

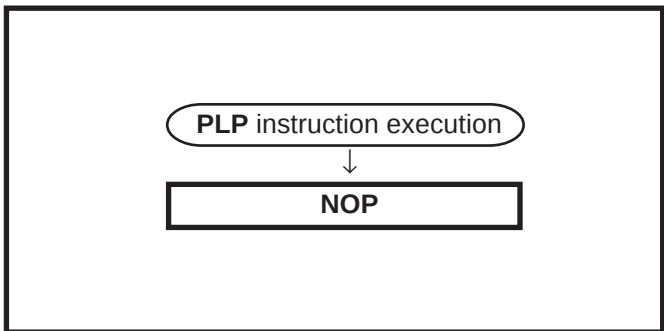


Fig. 3.3.7 Sequence of PLP instruction execution

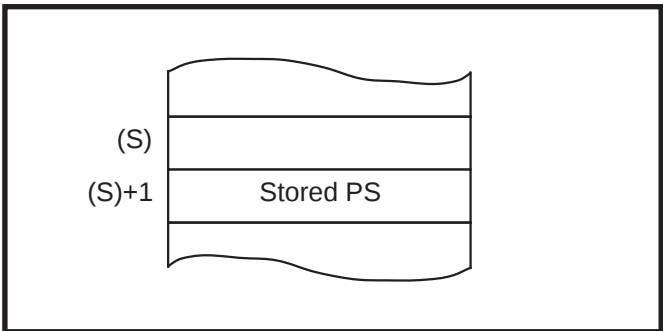


Fig. 3.3.8 Stack memory contents after PHP instruction execution

(2) Decimal calculations**① Execution of decimal calculations**

The **ADC** and **SBC** are the only instructions which will yield proper decimal notation, set the decimal mode flag (D) to “1” with the **SED** instruction. After executing the **ADC** or **SBC** instruction, execute another instruction before executing the **SEC**, **CLC**, or **CLD** instruction.

② Notes on status flag in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a **ADC** or **SBC** instruction is executed.

The carry flag (C) is set to “1” if a carry is generated as a result of the calculation, or is cleared to “0” if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to “0” before each calculation. To check for a borrow, the C flag must be initialized to “1” before each calculation.

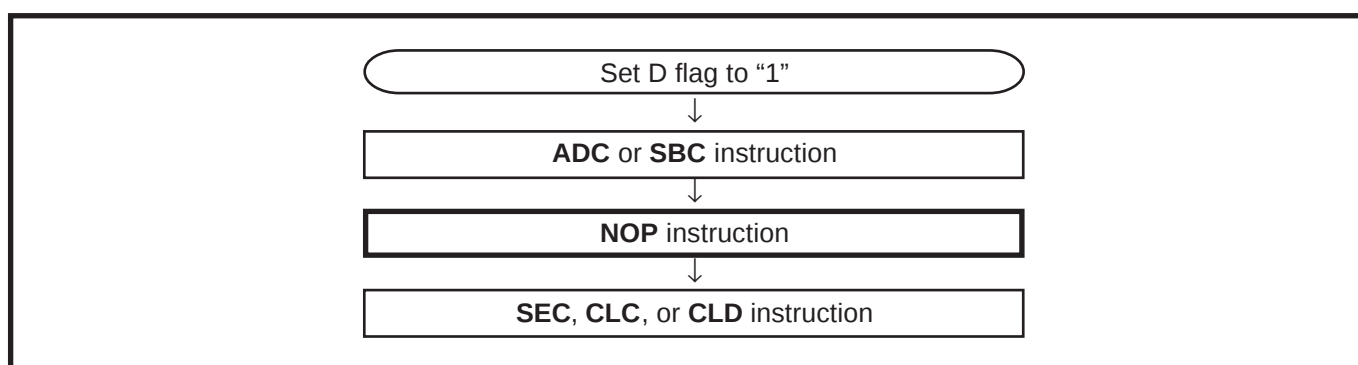


Fig. 3.3.9 Status flag at decimal calculations

(3) JMP instruction

When using the **JMP** instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

3.3.11 Programming and test of built-in PROM version

As for in the One Time PROM version (shipped in blank) and the built-in EPROM version, their built-in PROM can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

The built-in EPROM version is available only for program development and on-chip program evaluation. The programming test and screening for PROM of the One Time PROM version (shipped in blank) are not performed in the assembly process and the following processes. To ensure reliability after programming, performing programming and test according to the Figure 3.3.10 before actual use are recommended.

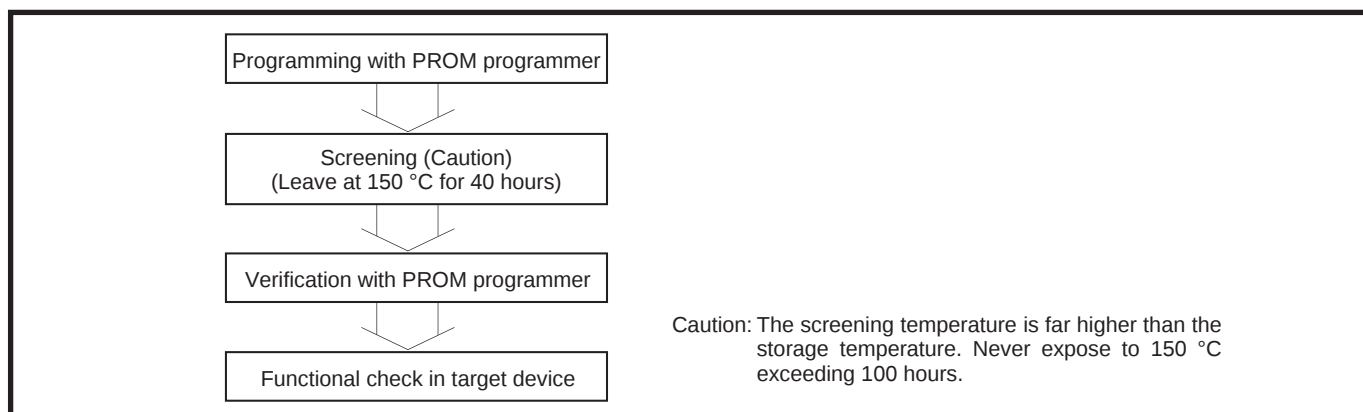


Fig. 3.3.10 Programming and testing of One Time PROM version

APPENDIX

3.3 Notes on use

3.3.12 Notes on built-in PROM version

(1) Programming adapter

Use a special programming adapter shown in Table 3.3.1 and a general-purpose PROM programmer when reading from or programming to the built-in PROM in the built-in PROM version.

Table 3.3.1 Programming adapter

Microcomputer	Programming adapter
M38B59EFP (One Time PROM version shipped in blank)	PCA4738F-80A
M38B59EFS	PCA4738L-80A

(2) Programming/reading

In PROM mode, operation is the same as that of the M5M27C101K, but programming conditions of PROM programmer are not set automatically because there are no internal device ID codes.

Accurately set the following conditions for data programming/reading. Take care not to apply 21 V to the VPP pin (is also used as port P4₇), or the product may be permanently damaged.

① Programming voltage: 12.5 V

② Setting of PROM programmer address: Refer to “**Table 3.3.2**”

Table 3.3.2 PROM programmer address setting

Microcomputer	PROM programmer start address	PROM programmer end address
M38B59EFP	Address 1080 ₁₆	Address FFFD ₁₆
M38B59EFS		

(3) Erasing

Contents of the windowed EPROM are erased through an ultraviolet light source with the wavelength 2537 Ångstrom. At least 15 W•sec/cm² are required to erase EPROM contents.

3.3.13 Termination of unused pins

(1) Terminate unused pins

① Output ports : Open

② Input ports :

Connect each pin to Vss through each resistor of 1 kΩ to 10 kΩ.

As for pins whose potential affects to operation modes such as pins INT or others, select the Vcc pin or the Vss pin according to their operation mode.

③ I/O ports :

- Set the I/O ports for the input mode and connect them to Vss through each resistor of 1 kΩ to 10 kΩ.

Ports that permit the selecting of a built-in pull-up resistor can also use this resistor. Set the I/O ports for the output mode and open them at “L” or “H”.

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

(2) Termination remarks

① Input ports and I/O ports :

Do not open in the input mode.

● Reason

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination ② and ③ shown on the above.

② I/O ports :

When setting for the input mode, do not connect to Vcc or Vss directly.

● Reason

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between a port and Vcc (or Vss).

③ I/O ports :

When setting for the input mode, do not connect multiple ports in a lump to Vcc or Vss through a resistor.

● Reason

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

- At the termination of unused pins, perform wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

APPENDIX

3.4 Countermeasures against noise

3.4 Countermeasures against noise

Countermeasures against noise are described below. The following countermeasures are effective against noise in theory, however, it is necessary not only to take measures as follows but to evaluate before actual use.

3.4.1 Shortest wiring length

The wiring on a printed circuit board can function as an antenna which feeds noise into the microcomputer. The shorter the total wiring length (by mm unit), the less the possibility of noise insertion into a microcomputer.

(1) Package

Select the smallest possible package to make the total wiring length short.

● Reason

The wiring length depends on a microcomputer package. Use of a small package, for example QFP and not DIP, makes the total wiring length short to reduce influence of noise.

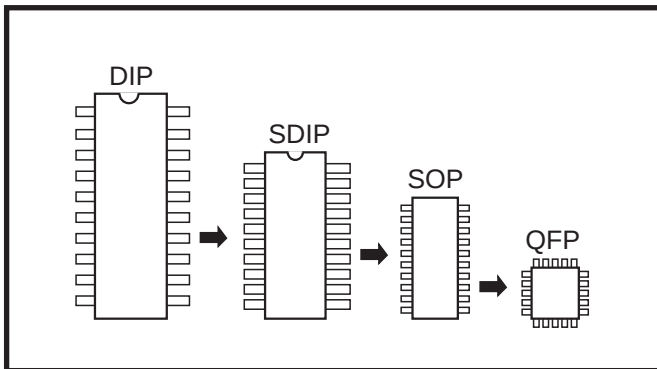


Fig. 3.4.1 Selection of packages

(2) Wiring for $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20mm).

● Reason

The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

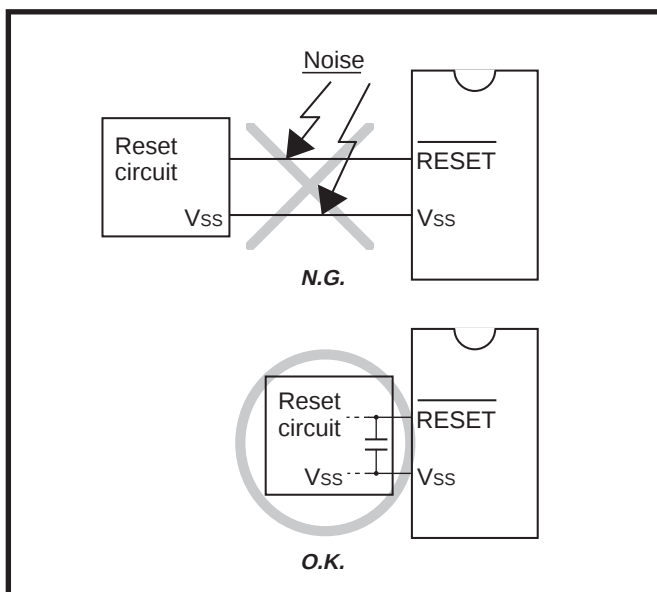


Fig. 3.4.2 Wiring for the $\overline{\text{RESET}}$ pin

(3) Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

● Reason

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

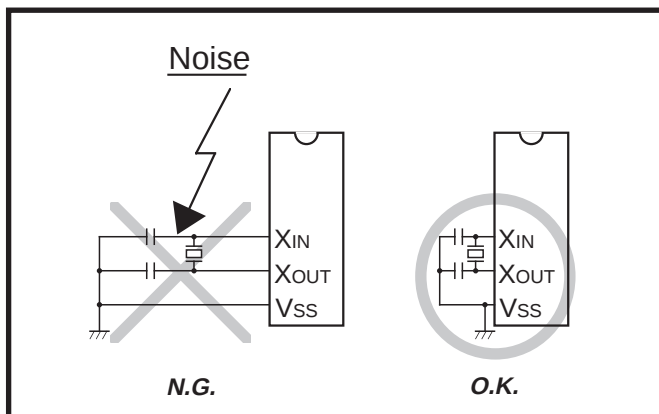


Fig. 3.4.3 Wiring for clock I/O pins

APPENDIX

3.4 Countermeasures against noise

(4) Wiring to VPP pin of One Time PROM version and EPROM version

Connect an approximately 5 kΩ resistor to the VPP pin the shortest possible in series. When not connecting the resistor, make the length of wiring between the VPP pin and the Vss pin the shortest possible.

Note: Even when a circuit which included an approximately 5 kΩ resistor is used in the Mask ROM version, the microcomputer operates correctly.

● Reason

The VPP pin of the One Time PROM and the EPROM version is the power source input pin for the built-in PROM. When programming in the built-in PROM, the impedance of the VPP pin is low to allow the electric current for writing flow into the PROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the built-in PROM, which may cause a program runaway.

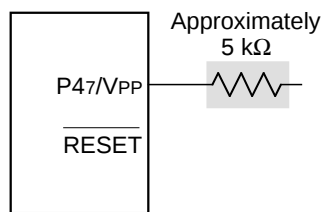


Fig. 3.4.4 Wiring for the VPP pin of the One Time PROM and the EPROM version

3.4.2 Connection of bypass capacitor across Vss line and Vcc line

Connect an approximately 0.1 μF bypass capacitor across the Vss line and the Vcc line as follows:

- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the Vcc pin.

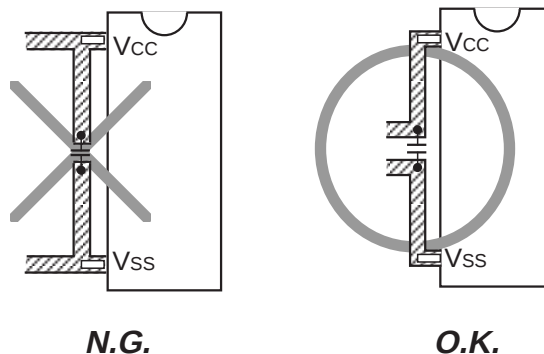


Fig. 3.4.5 Bypass capacitor across the Vss line and the Vcc line

3.4.3 Wiring to analog input pins

- Connect an approximately $100\ \Omega$ to $1\ \text{k}\Omega$ resistor to an analog signal line which is connected to an analog input pin in series. Besides, connect the resistor to the microcomputer as close as possible.
- Connect an approximately $1000\ \text{pF}$ capacitor across the V_{SS} pin and the analog input pin. Besides, connect the capacitor to the V_{SS} pin as close as possible. Also, connect the capacitor across the analog input pin and the V_{SS} pin at equal length.

● Reason

Signals which is input in an analog input pin (such as an A-D converter/comparator input pin) are usually output signals from sensor. The sensor which detects a change of event is installed far from the printed circuit board with a microcomputer, the wiring to an analog input pin is longer necessarily. This long wiring functions as an antenna which feeds noise into the microcomputer, which causes noise to an analog input pin.

If a capacitor between an analog input pin and the V_{SS} pin is grounded at a position far away from the V_{SS} pin, noise on the GND line may enter a microcomputer through the capacitor.

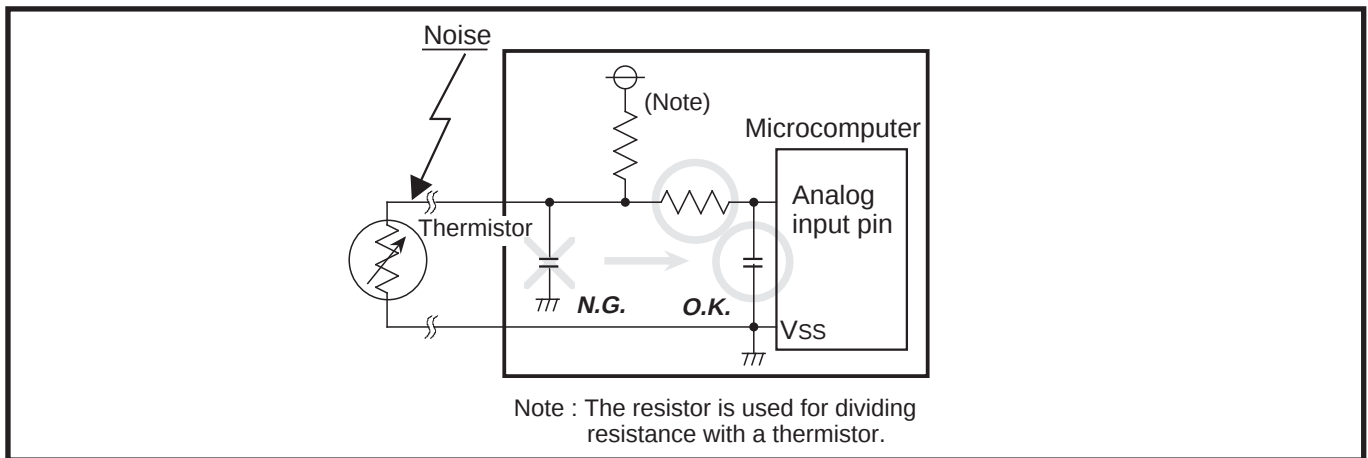


Fig. 3.4.6 Analog signal line and a resistor and a capacitor

3.4.4 Oscillator concerns

Take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

(1) Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

● Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

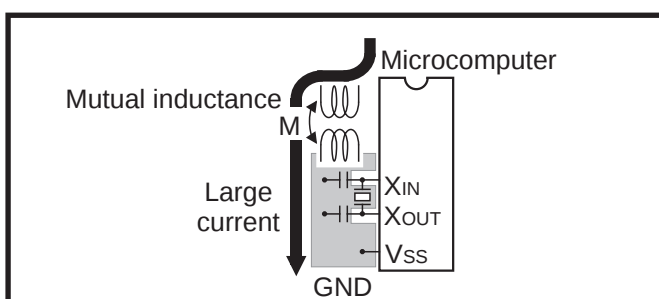


Fig. 3.4.7 Wiring for a large current signal line

APPENDIX

3.4 Countermeasures against noise

(2) Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

● Reason

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

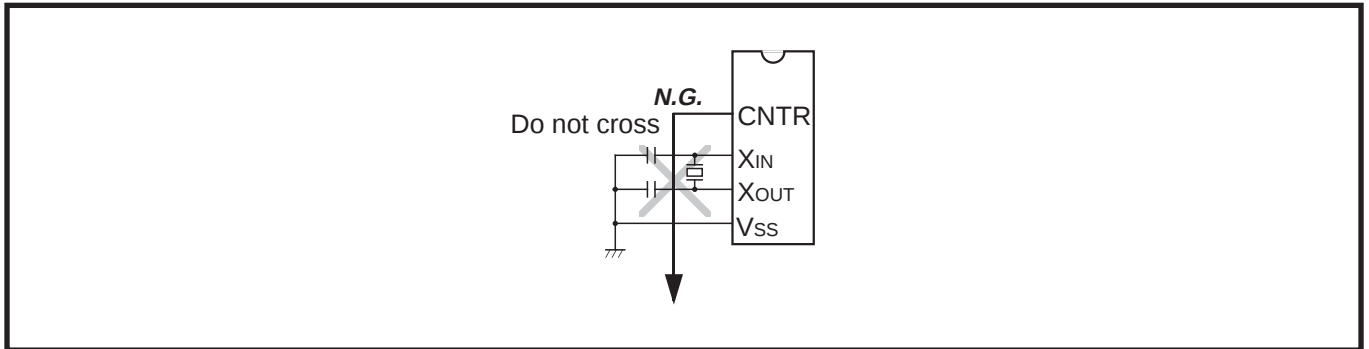


Fig. 3.4.8 Wiring of signal lines where potential levels change frequently

(3) Oscillator protection using Vss pattern

As for a two-sided printed circuit board, print a Vss pattern on the underside (soldering side) of the position (on the component side) where an oscillator is mounted.

Connect the Vss pattern to the microcomputer Vss pin with the shortest possible wiring. Besides, separate this Vss pattern from other Vss patterns.

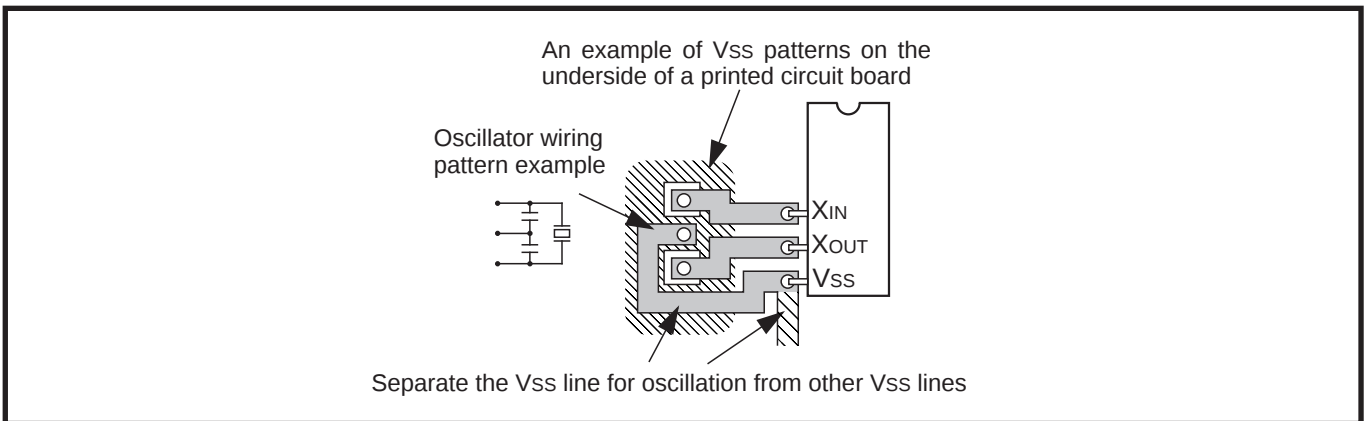


Fig. 3.4.9 Vss pattern on the underside of an oscillator

3.4 Countermeasures against noise

3.4.5 Setup for I/O ports

Setup I/O ports using hardware and software as follows:

<Hardware>

- Connect a resistor of 100 Ω or more to an I/O port in series.

<Software>

- As for an input port, read data several times by a program for checking whether input levels are equal or not.
- As for an output port, since the output data may reverse because of noise, rewrite data to its port latch at fixed periods.
- Rewrite data to direction registers and pull-up control registers at fixed periods.

Note: When a direction register is set for input port again at fixed periods, a several-nanosecond short pulse may be output from this port. If this is undesirable, connect a capacitor to this port to remove the noise pulse.

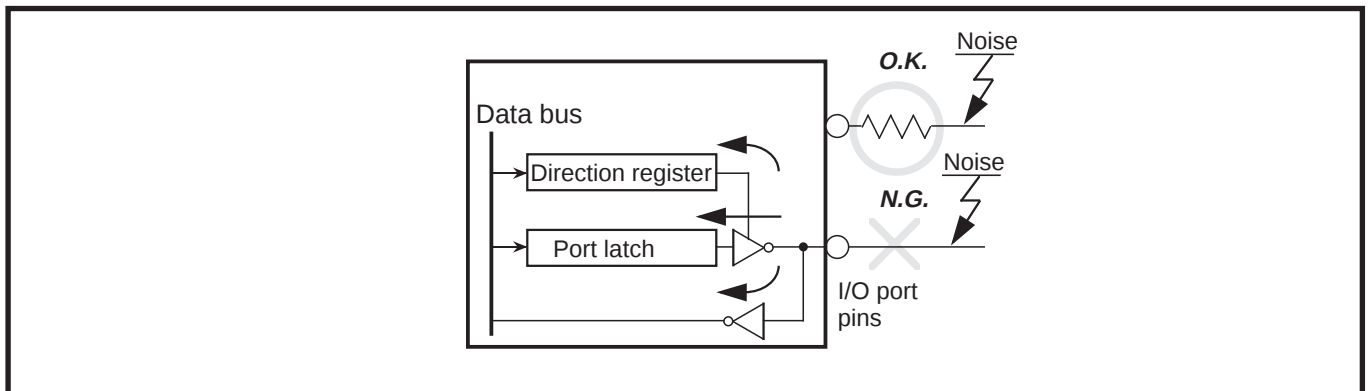


Fig. 3.4.10 Setup for I/O ports

APPENDIX

3.4 Countermeasures against noise

3.4.6 Providing of watchdog timer function by software

If a microcomputer runs away because of noise or others, it can be detected by a software watchdog timer and the microcomputer can be reset to normal operation. This is equal to or more effective than program runaway detection by a hardware watchdog timer. The following shows an example of a watchdog timer provided by software.

In the following example, to reset a microcomputer to normal operation, the main routine detects errors of the interrupt processing routine and the interrupt processing routine detects errors of the main routine. This example assumes that interrupt processing is repeated multiple times in a single main routine processing.

<The main routine>

- Assigns a single byte of RAM to a software watchdog timer (SWDT) and writes the initial value N in the SWDT once at each execution of the main routine. The initial value N should satisfy the following condition:
$$N+1 \geq (\text{Counts of interrupt processing executed in each main routine})$$

As the main routine execution cycle may change because of an interrupt processing or others, the initial value N should have a margin.
- Watches the operation of the interrupt processing routine by comparing the SWDT contents with counts of interrupt processing after the initial value N has been set.
- Detects that the interrupt processing routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
If the SWDT contents do not change after interrupt processing.

<The interrupt processing routine>

- Decrements the SWDT contents by 1 at each interrupt processing.
- Determines that the main routine operates normally when the SWDT contents are reset to the initial value N at almost fixed cycles (at the fixed interrupt processing count).
- Detects that the main routine has failed and determines to branch to the program initialization routine for recovery processing in the following case:
If the SWDT contents are not initialized to the initial value N but continued to decrement and if they reach 0 or less.

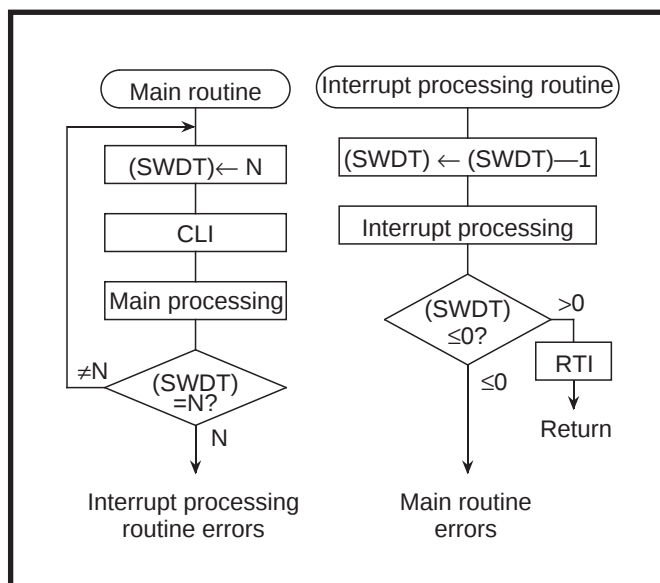
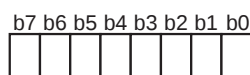


Fig. 3.4.11 Watchdog timer by software

3.5 Control registers

Port Pi



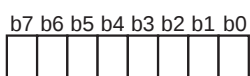
Port Pi (i = 0, 1, 2, 3, 4, 5, 7, 8)

(Pi: addresses 00₁₆, 02₁₆, 04₁₆, 06₁₆, 08₁₆, 0A₁₆, 0E₁₆, 10₁₆)

b	Name	Functions	At reset	R	W
0	Port Pi ₀	● In output mode	0	○	○
1	Port Pi ₁	Write Port latch	0	○	○
2	Port Pi ₂	Read Port latch	0	○	○
3	Port Pi ₃	● In input mode	0	○	○
4	Port Pi ₄	Write Port latch	0	○	○
5	Port Pi ₅	Read Value of pin	0	○	○
6	Port Pi ₆		0	○	○
7	Port Pi ₇		0	○	○

Fig. 3.5.1 Structure of port Pi

Port Pi direction register



Port Pi direction register (i = 0, 2, 4, 5, 7, 8)

(PiD: addresses 01₁₆, 05₁₆, 09₁₆, 0B₁₆, 0F₁₆, 11₁₆)

b	Name	Functions	At reset	R	W
0	Port Pi ₀ direction register	0 : Port Pi ₀ input mode 1 : Port Pi ₀ output mode	0	×	○
1		0 : Port Pi ₁ input mode 1 : Port Pi ₁ output mode	0	×	○
2		0 : Port Pi ₂ input mode 1 : Port Pi ₂ output mode	0	×	○
3		0 : Port Pi ₃ input mode 1 : Port Pi ₃ output mode	0	×	○
4		0 : Port Pi ₄ input mode 1 : Port Pi ₄ output mode	0	×	○
5		0 : Port Pi ₅ input mode 1 : Port Pi ₅ output mode	0	×	○
6		0 : Port Pi ₆ input mode 1 : Port Pi ₆ output mode	0	×	○
7		0 : Port Pi ₇ input mode 1 : Port Pi ₇ output mode (Note)	0	×	○

Note: Bit 7 of the port P4 direction register (address 09₁₆) does not have direction register function because P4₇ is input port. When writing to bit 7 of the port P4 direction register, write "0" to the bit.

Fig. 3.5.2 Structure of port Pi direction register

APPENDIX

3.5 Control registers

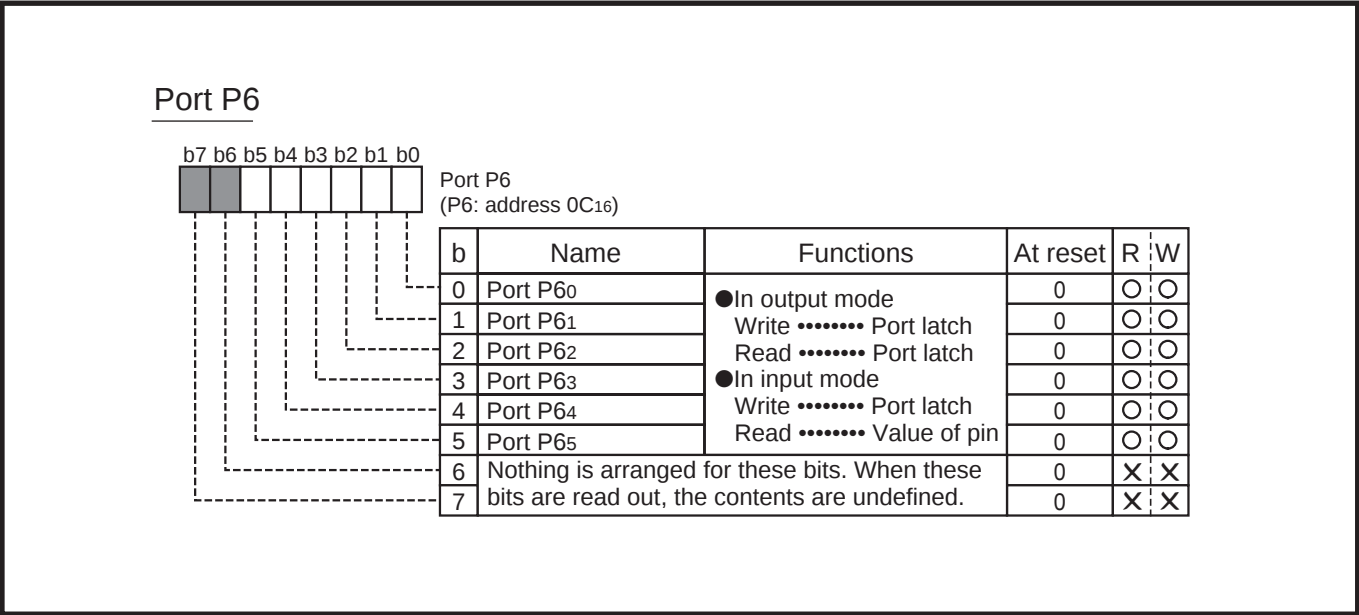


Fig. 3.5.3 Structure of port P6

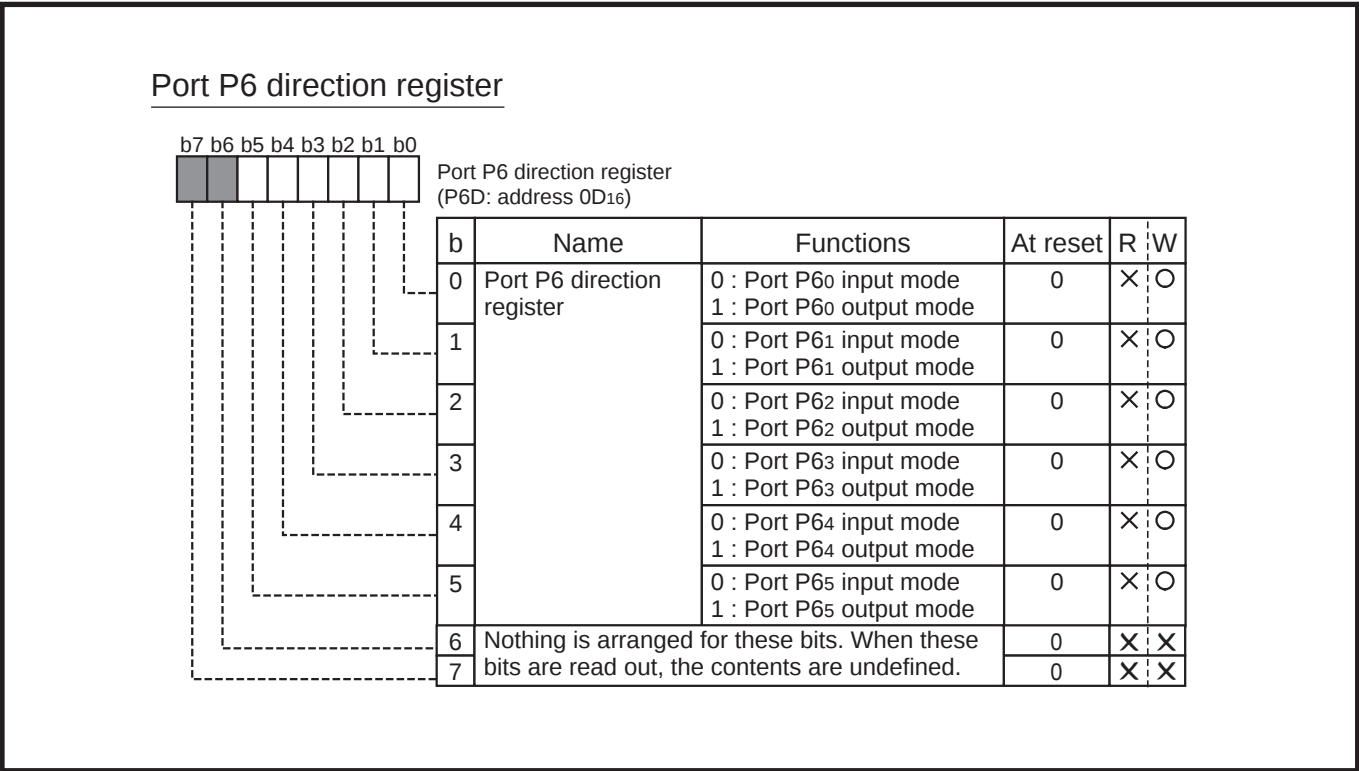


Fig. 3.5.4 Structure of port P6 direction register

Port P9

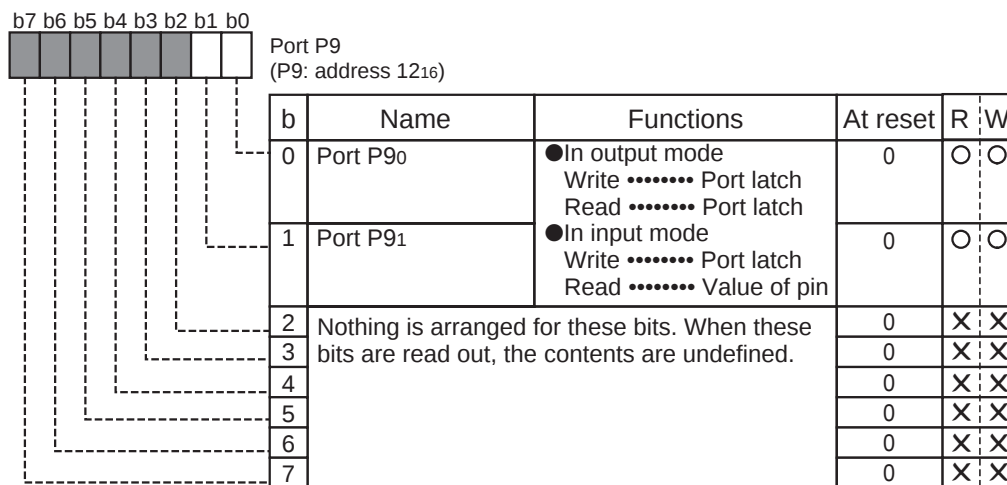


Fig. 3.5.5 Structure of port P9

Port P9 direction register

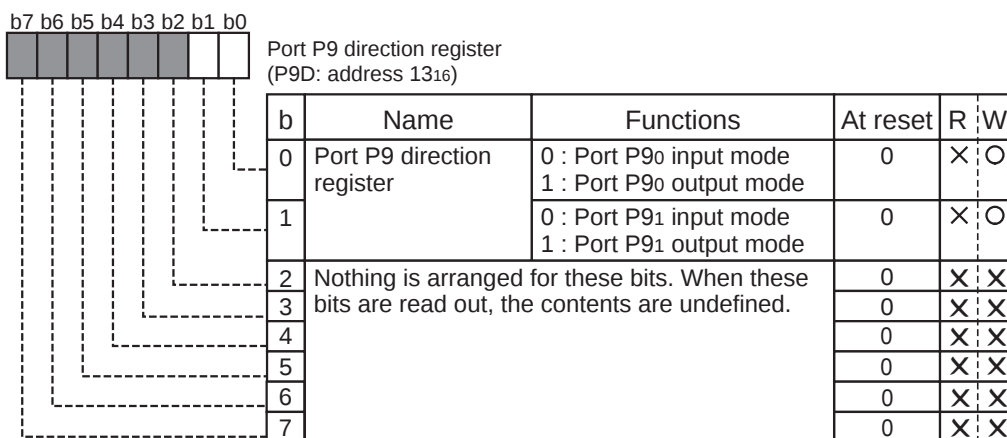


Fig. 3.5.6 Structure of port P9 direction register

APPENDIX

3.5 Control registers

PWM register (high-order)

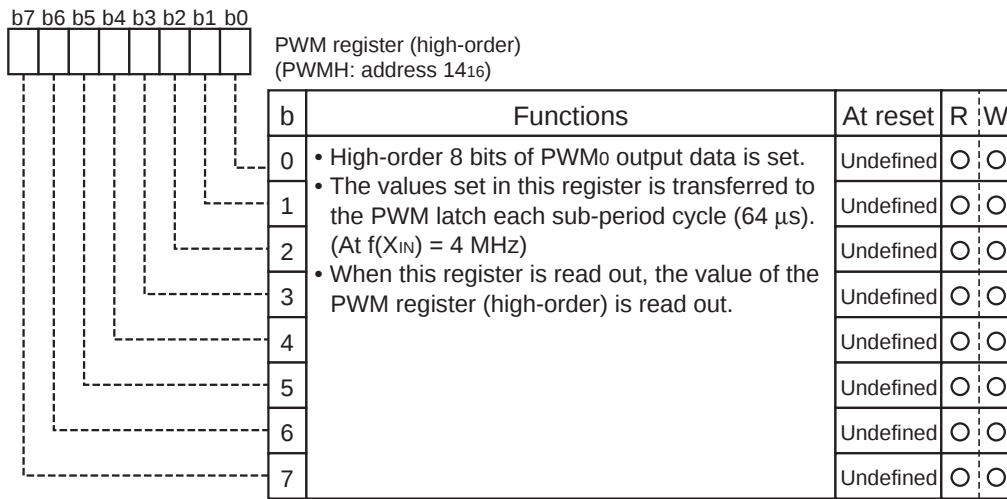


Fig. 3.5.7 Structure of PWM register (high-order)

PWM register (low-order)

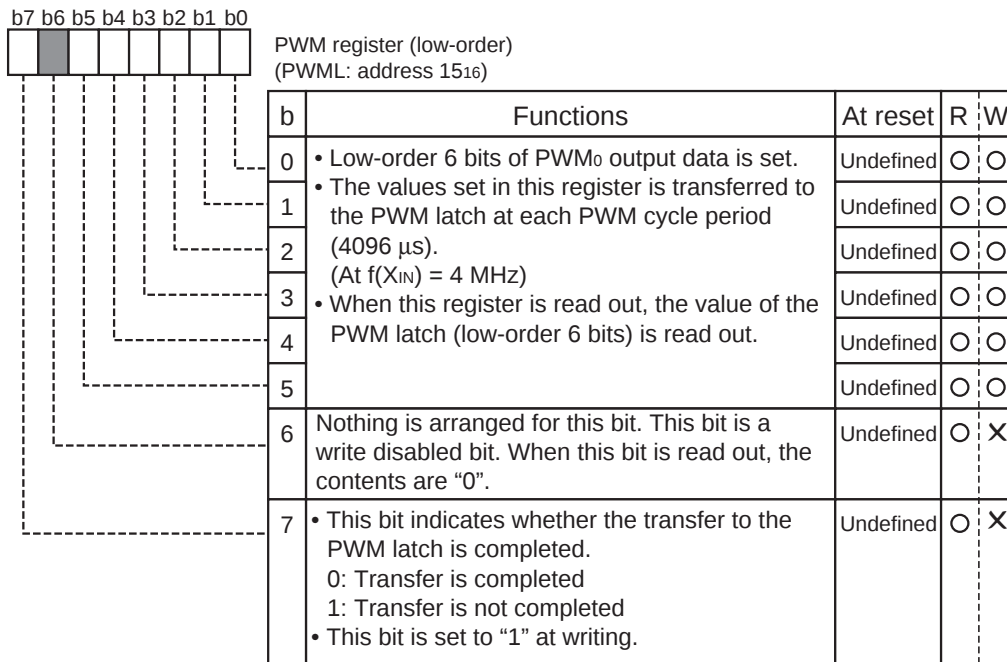


Fig. 3.5.8 Structure of PWM register (low-order)

Baud rate generator

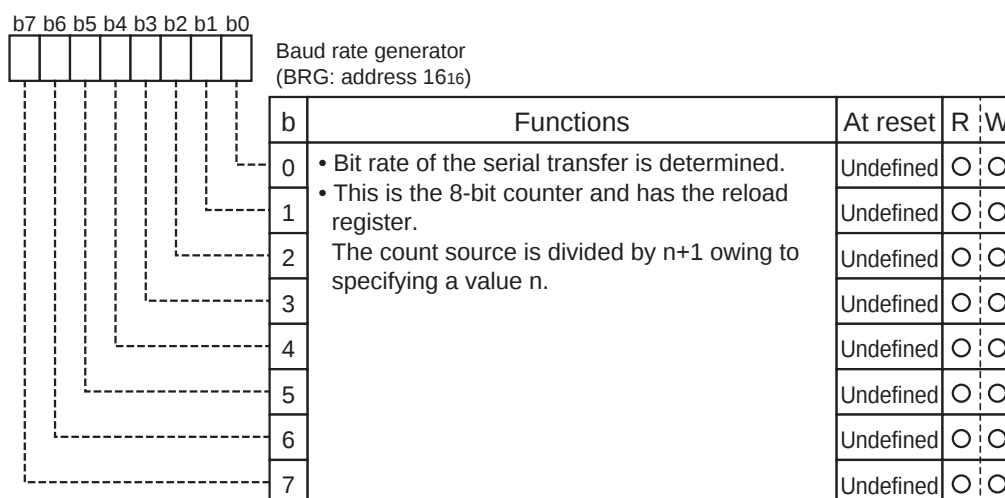


Fig. 3.5.9 Structure of baud rate generator

UART control register

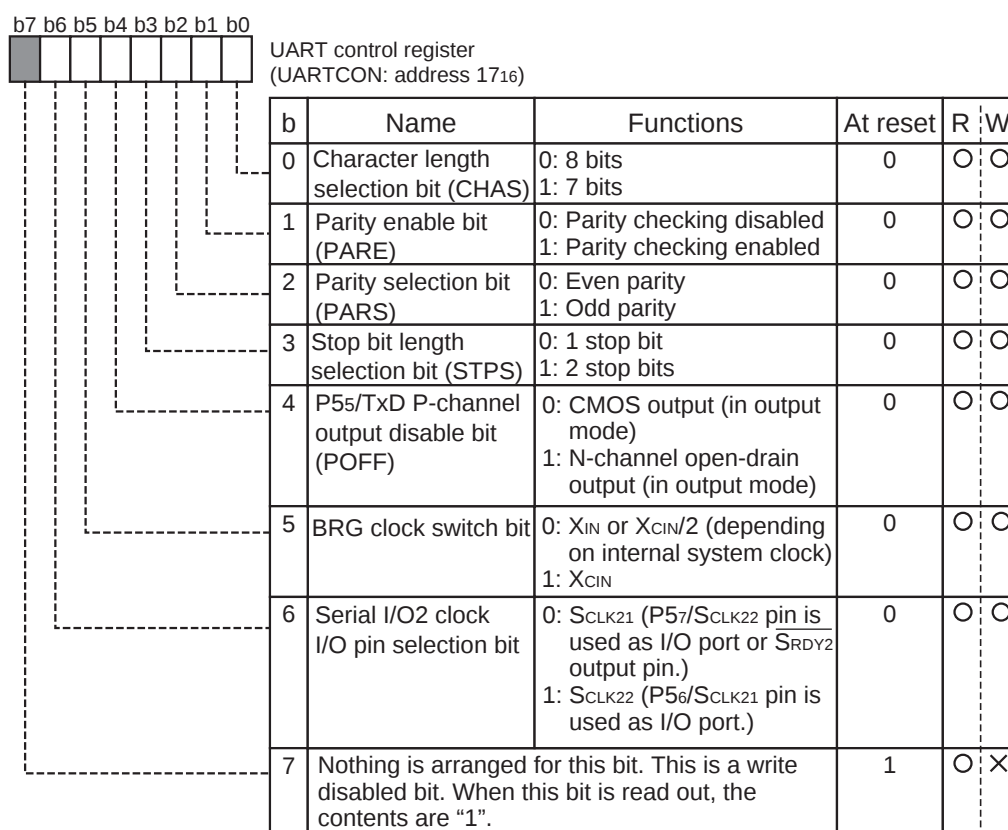


Fig. 3.5.10 Structure of UART control register

APPENDIX

3.5 Control registers

Serial I/O1 automatic transfer data pointer

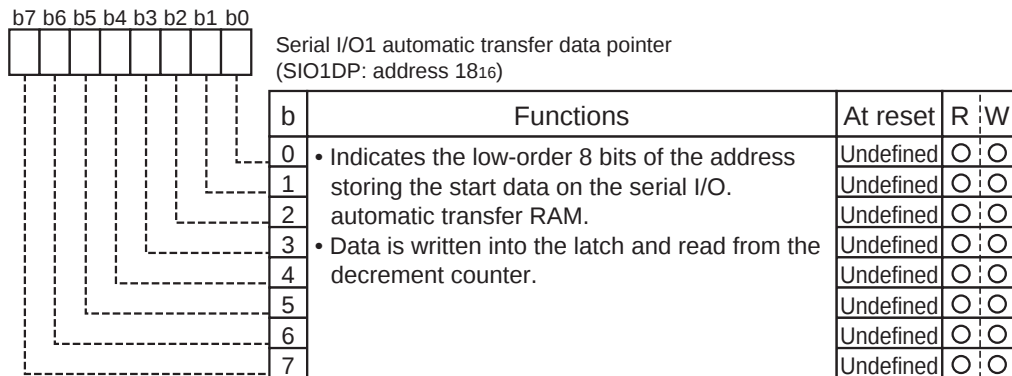


Fig. 3.5.11 Structure of serial I/O1 automatic transfer data pointer

Serial I/O1 control register 1

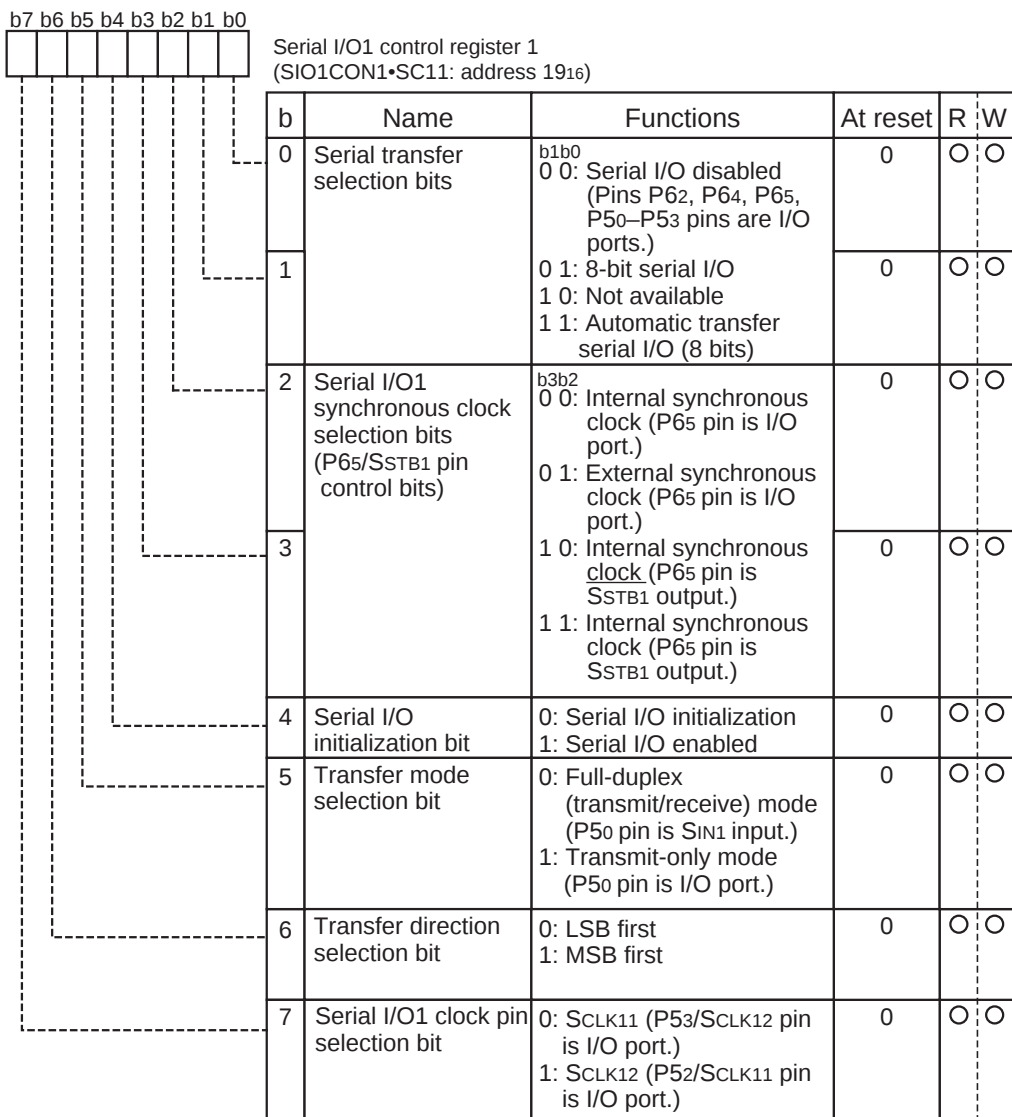


Fig. 3.5.12 Structure of serial I/O1 control register 1

Serial I/O1 control register 2

b7	b6	b5	b4	b3	b2	b1	b0	Serial I/O1 control register 2 (SIO1CON2 • SC12: address 1A16)					
								b	Name	Functions	At reset	R	W
								0	P62/SRDY1 • P64/SBUSY1 pin control bits b3b2b1b0 0 0 0 0: P62, P64 pins are I/O ports. 0 0 0 1: Not used 0 0 1 0: P62 pin is SRDY1 output; P64 pin is I/O port. 0 0 1 1: P62 pin is SRDY1 output; P64 pin is I/O port.		0	○	○
								1	0 1 0 0: P62 pin is I/O port; P64 pin is SBUSY1 input. 0 1 0 1: P62 pin is I/O port; P64 pin is SBUSY1 input. 0 1 1 0: P62 pin is I/O port; P64 pin is SBUSY1 output. 0 1 1 1: P62 pin is I/O port; P64 pin is SBUSY1 output.		0	○	○
								2	1 0 0 0: P62 pin is SRDY1 input; P64 pin is SBUSY1 output. 1 0 0 1: P62 pin is SRDY1 input; P64 pin is SBUSY1 output. 1 0 1 0: P62 pin is SRDY1 input; P64 pin is SBUSY1 output. 1 0 1 1: P62 pin is SRDY1 input; P64 pin is SBUSY1 output.		0	○	○
								3	1 1 0 0: P62 pin is SRDY1 output; P64 pin is SBUSY1 input. 1 1 0 1: P62 pin is SRDY1 output; P64 pin is SBUSY1 input. 1 1 1 0: P62 pin is SRDY1 output; P64 pin is SBUSY1 input. 1 1 1 1: P62 pin is SRDY1 output; P64 pin is SBUSY1 input.		0	○	○
								4	SBUSY1 output • SSTB1 output function selection bit (Valid in serial I/O1 automatic transfer mode)	0: Functions as signal for each 1-byte 1: Functions as signal for each transfer data set	0	○	○
								5	Serial transfer status flag	0: Serial transfer completed 1: Serial transfer in- progress	0	○	×
								6	Sout1 pin control bit (when serial data is not transferred)	0: Output active 1: Output high-impedance	0	○	○
								7	P51/Sout1 P-channel output disable bit	0: CMOS 3 state (P- channel output is valid.) 1: N-channel open-drain output (P-channel output is invalid.)	0	○	○

Fig. 3.5.13 Structure of serial I/O1 control register 2

APPENDIX

3.5 Control registers

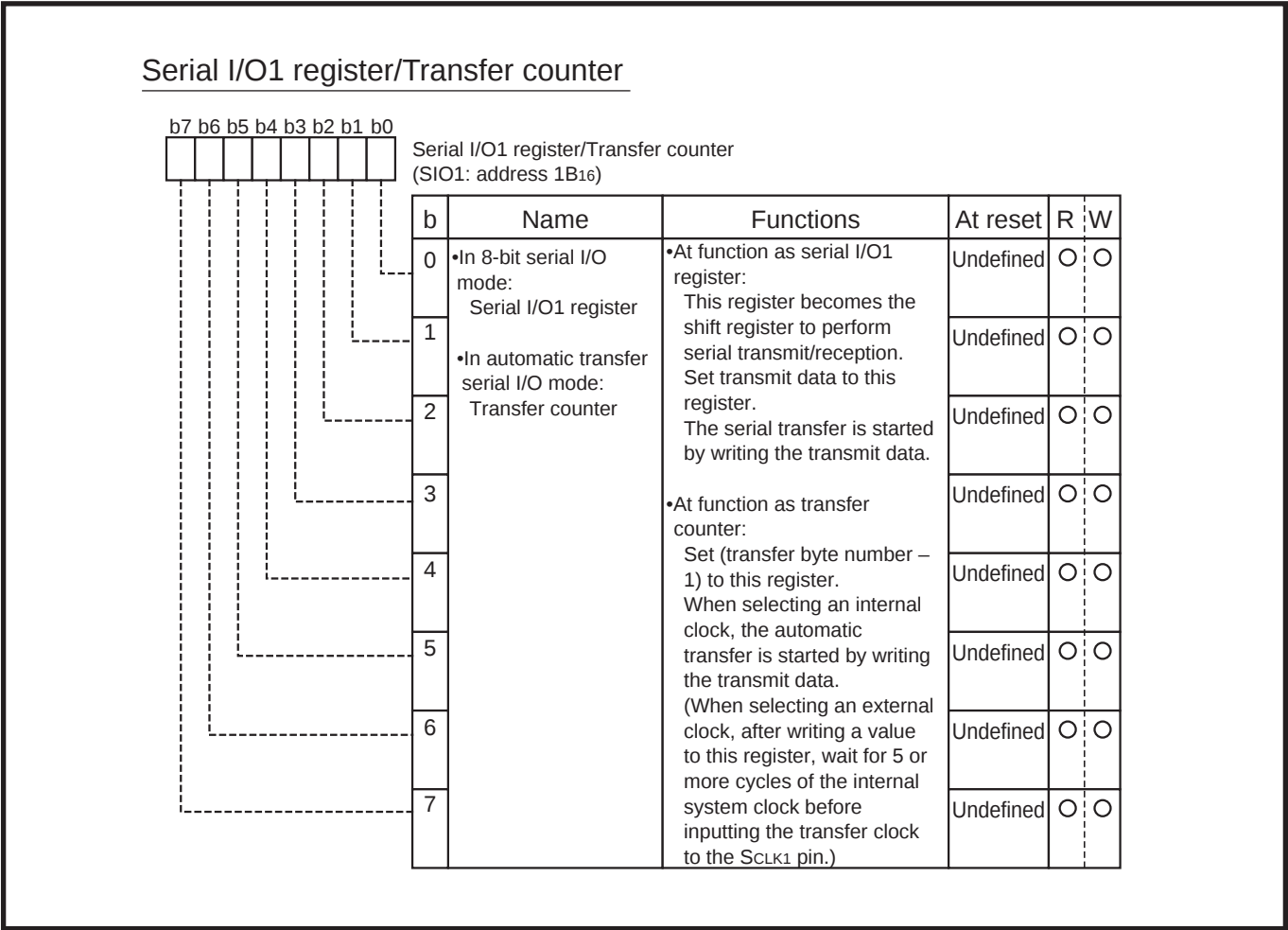


Fig. 3.5.14 Structure of serial I/O1 register/Transfer counter

Serial I/O1 control register 3

b7 b6 b5 b4 b3 b2 b1 b0								Serial I/O1 control register 3 (SIO1CON3 • SC13: address 1C16)					
								b	Name	Functions	At reset	R	W
								0	Automatic transfer interval set bits (valid only when selecting internal synchronous clock)	b4b3b2b1b0 0 0 0 0 0: 2 cycles of transfer clock	0	○	○
								1		0 0 0 0 1: 3 cycles of transfer clock to	0	○	○
								2		1 1 1 1 0: 32 cycles of transfer clock	0	○	○
								3		1 1 1 1 1: 33 cycles of transfer clock	0	○	○
								4		Data is written into the latch and read from the decrement counter.	0	○	○
								5	Internal synchronous clock selection bits	b7b6b5 0 0 0 : f(XIN)/4 or f(XCIN)/8 0 0 1 : f(XIN)/8 or f(XCIN)/16 0 1 0 : f(XIN)/16 or f(XCIN)/32 0 1 1 : f(XIN)/32 or f(XCIN)/64 1 0 0 : f(XIN)/64 or f(XCIN)/128 1 0 1 : f(XIN)/128 or f(XCIN)/256 1 1 0 : f(XIN)/256 or f(XCIN)/512 1 1 1 : Not used	0	○	○
								6		0 1 1 : f(XIN)/32 or f(XCIN)/64 1 0 0 : f(XIN)/64 or f(XCIN)/128	0	○	○
								7		1 0 1 : f(XIN)/128 or f(XCIN)/256 1 1 0 : f(XIN)/256 or f(XCIN)/512	0	○	○
										1 1 1 : Not used			

Fig. 3.5.15 Structure of serial I/O1 control register 3

APPENDIX

3.5 Control registers

Serial I/O2 control register

b7	b6	b5	b4	b3	b2	b1	b0	Serial I/O2 control register (SIO2CON: address 1D16)			
b	Name							Functions	At reset	R	W
0	BRG count source selection bit (CSS)							0: f(XIN) or f(XCIN)/2 or f(XCIN) 1: f(XIN)/4 or f(XCIN)/8 or f(XCIN)/4	0	○	○
1	Serial I/O2 synchronous clock selection bit (SCS)							•In clock synchronous mode 0: BRG output/4 1: External clock input •In UART mode 0: BRG output/16 1: External clock input/16	0	○	○
2	SRDY2 output enable bit (SRDY)							0: P57 pin operates as normal I/O pin 1: P57 pin operates as SRDY2 output pin	0	○	○
3	Transmit interrupt source selection bit (TIC)							0: When transmit buffer has emptied 1: When transmit shift operation is completed	0	○	○
4	Transmit enable bit (TE)							0: Transmit disabled 1: Transmit enabled	0	○	○
5	Receive enable bit (RE)							0: Receive disabled 1: Receive enabled	0	○	○
6	Serial I/O2 mode selection bit (SIOM)							0: Clock asynchronous serial I/O (UART) mode 1: Clock synchronous serial I/O mode	0	○	○
7	Serial I/O2 enable bit (SIOE)							0: Serial I/O2 disabled (pins P54–P57 operate as normal I/O pins) 1: Serial I/O2 enabled (pins P54–P57 operate as serial I/O pins)	0	○	○

Fig. 3.5.16 Structure of serial I/O2 control register

Serial I/O2 status register

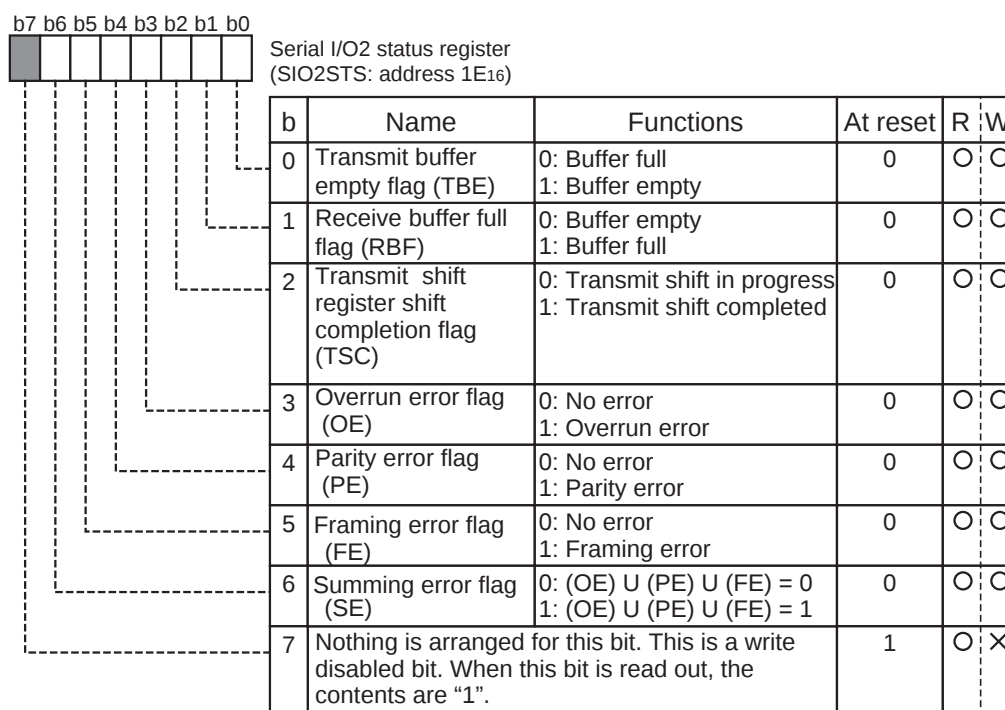


Fig. 3.5.17 Structure of serial I/O2 status register

Serial I/O2 transmit/receive buffer register

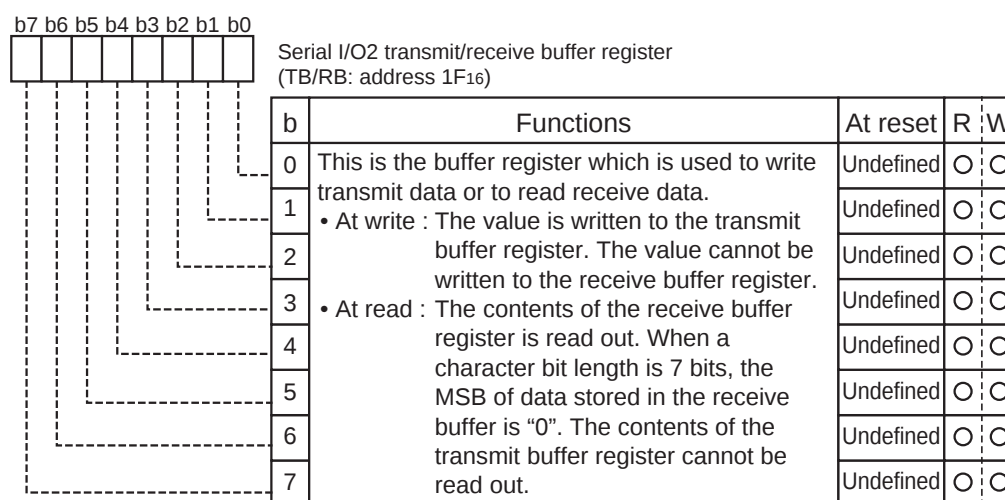


Fig. 3.5.18 Structure of serial I/O2 transmit/receive buffer register

APPENDIX

3.5 Control registers

Timer i

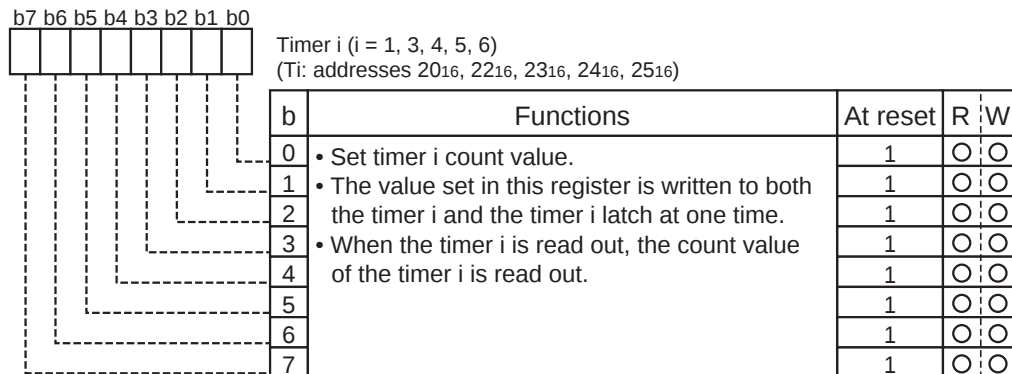


Fig. 3.5.19 Structure of timer i

Timer 2

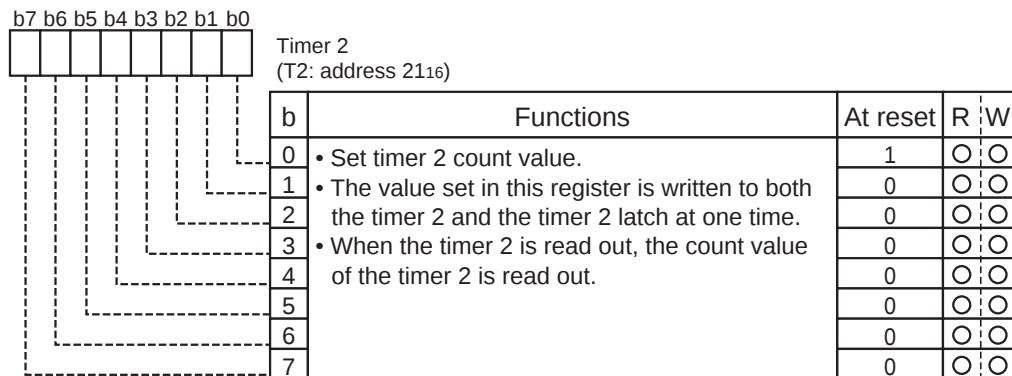


Fig. 3.5.20 Structure of timer 2

PWM control register

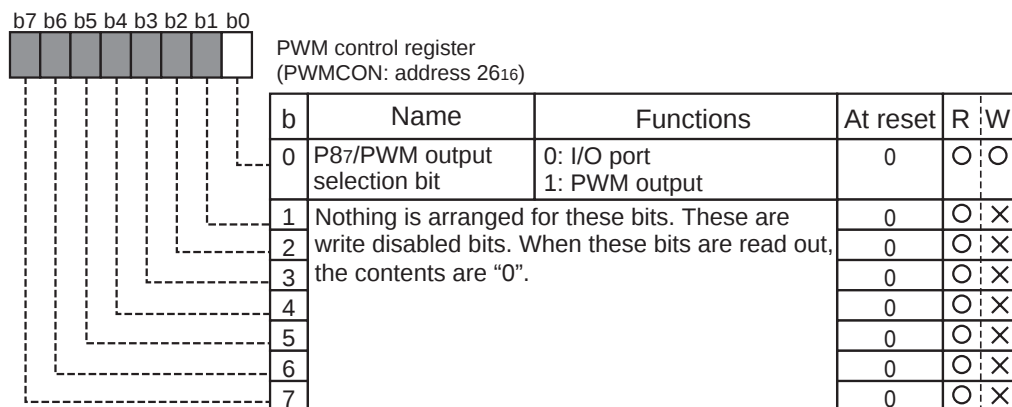


Fig. 3.5.21 Structure of PWM control register

Timer 6 PWM register

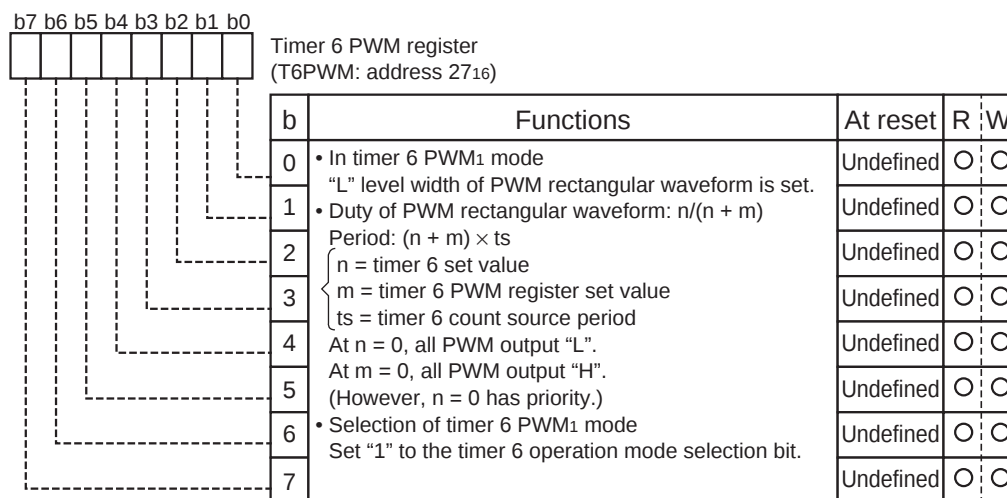


Fig. 3.5.22 Structure of timer 6 PWM register

Timer 12 mode register

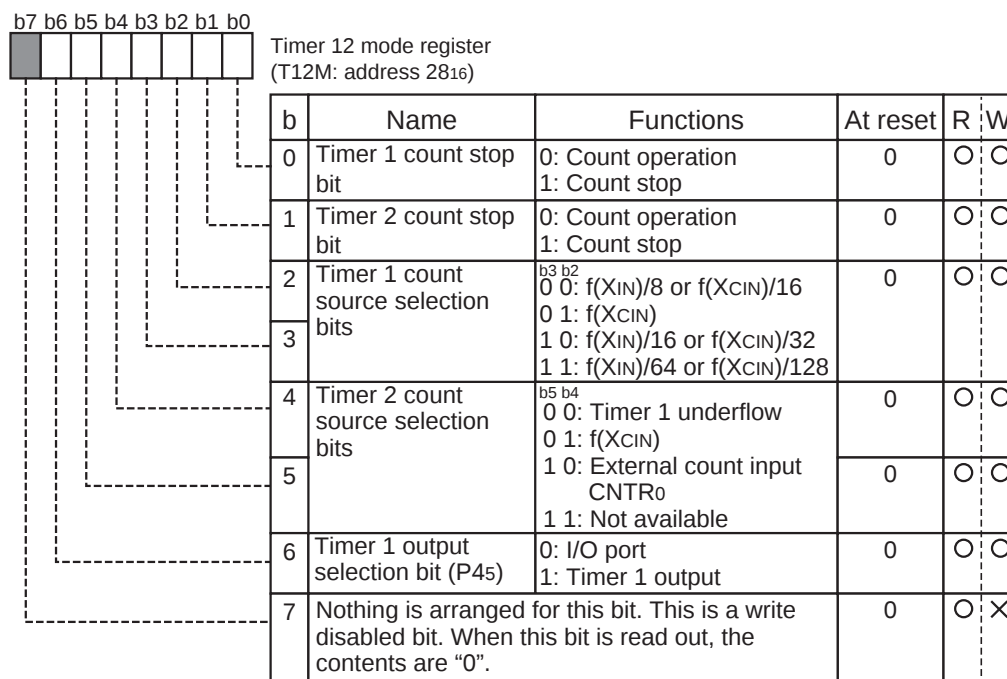
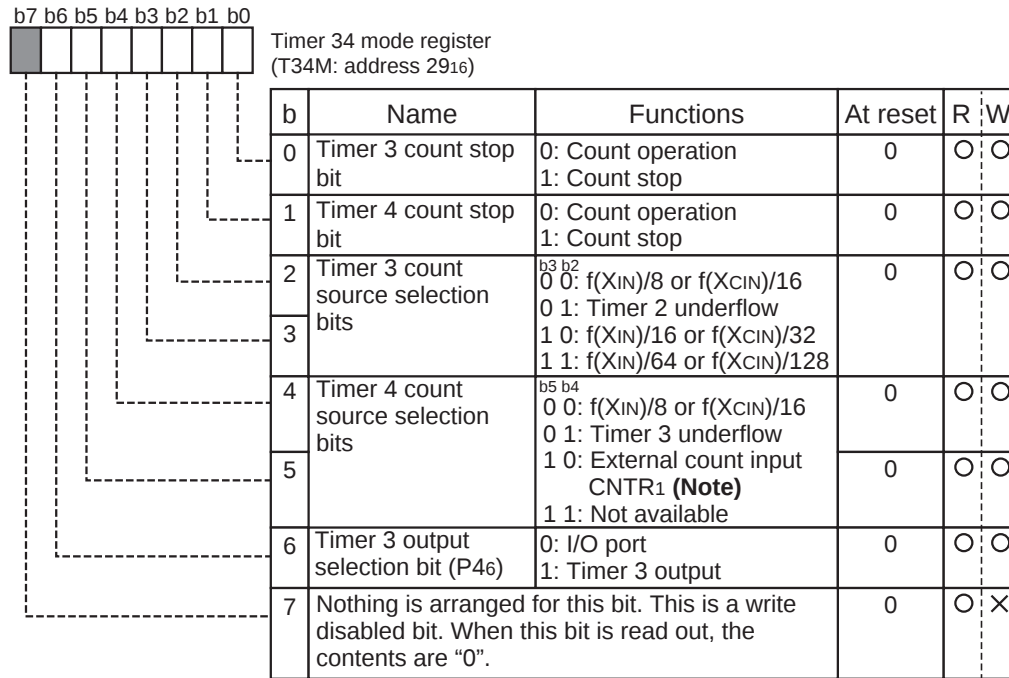


Fig. 3.5.23 Structure of timer 12 mode register

APPENDIX

3.5 Control registers

Timer 34 mode register



Note: In the mask option type P, CNTR1 function cannot be used.

Fig. 3.5.24 Structure of timer 34 mode register

Timer 56 mode register

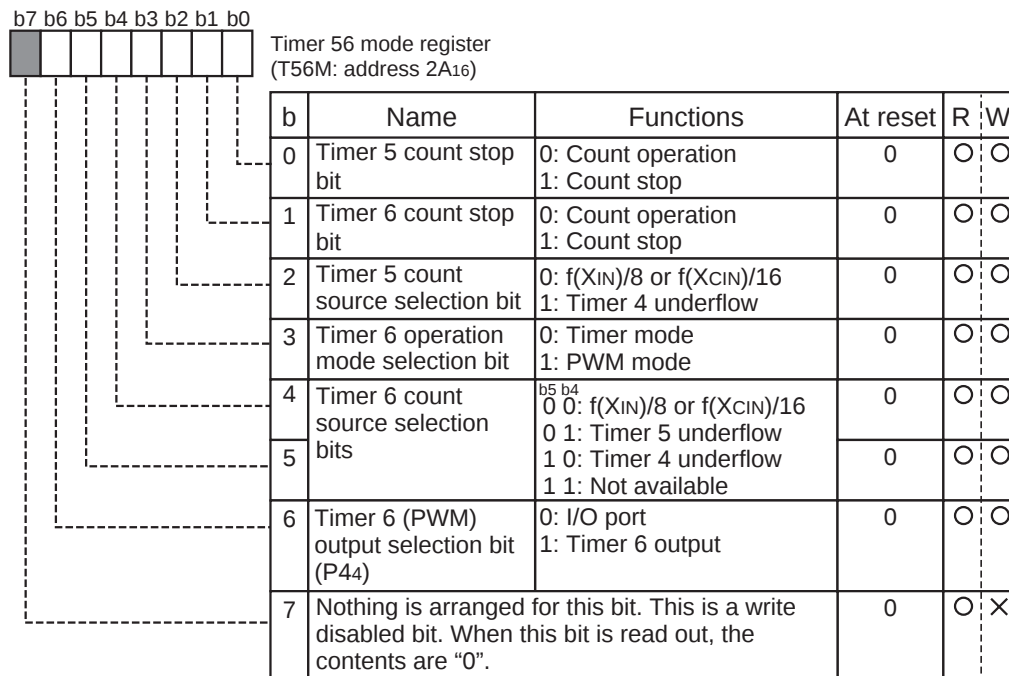


Fig. 3.5.25 Structure of timer 56 mode register

Watchdog timer control register

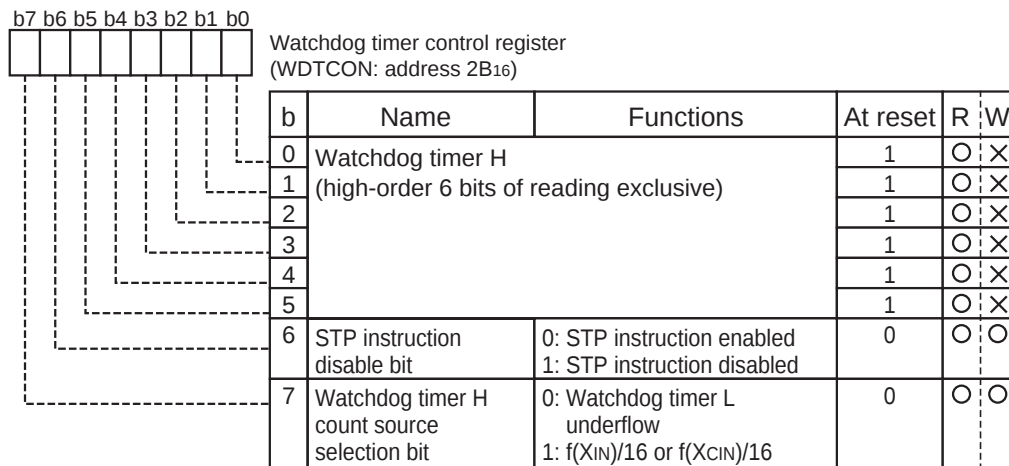
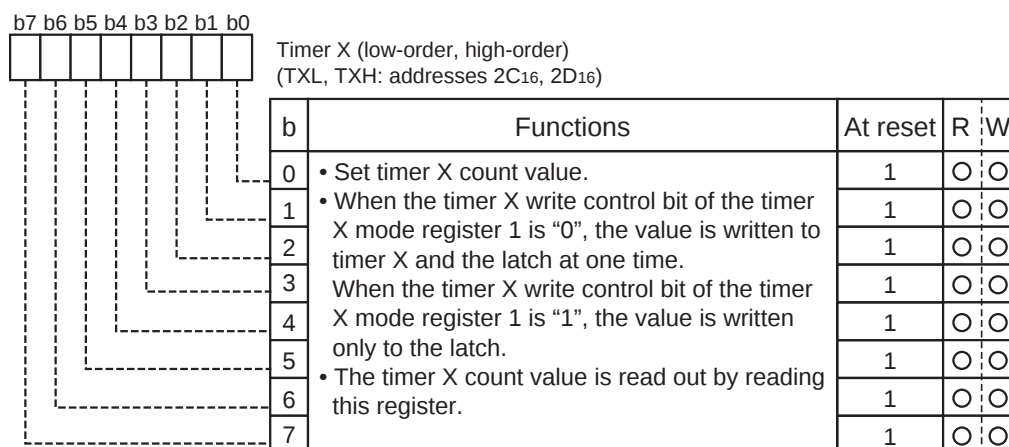


Fig. 3.5.26 Structure of watchdog timer control register

Timer X (low-order, high-order)



- Notes**
- 1: When reading and writing, perform them to both the high-order and low-order bytes.
 - 2: Read both registers in order of TXH and TXL following.
 - 3: Write both registers in order of TXL and TXH following.
 - 4: Do not read both registers during a write, and do not write to both registers during a read.

Fig. 3.5.27 Structure of timer X (low-order, high-order)

APPENDIX

3.5 Control registers

Timer X mode register 1

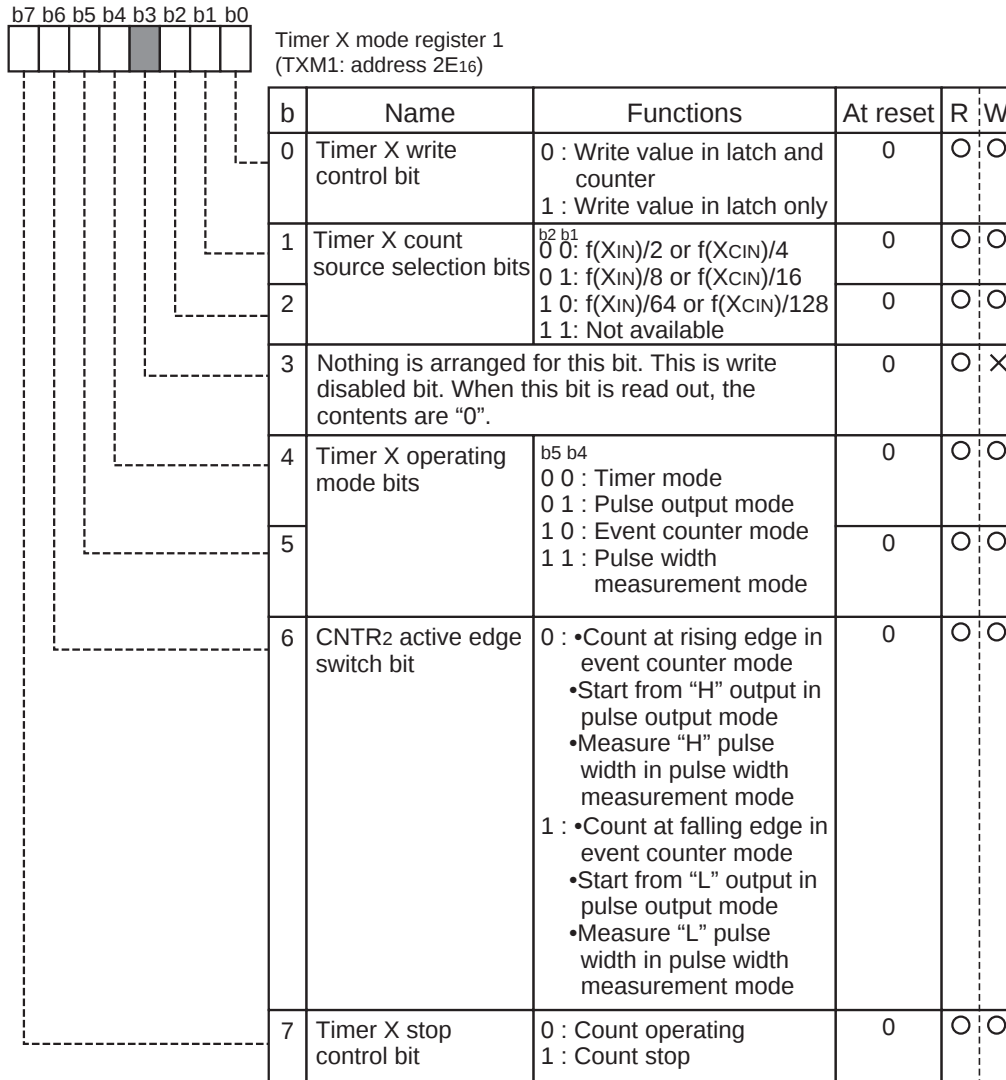


Fig. 3.5.28 Structure of timer X mode register 1

Timer X mode register 2

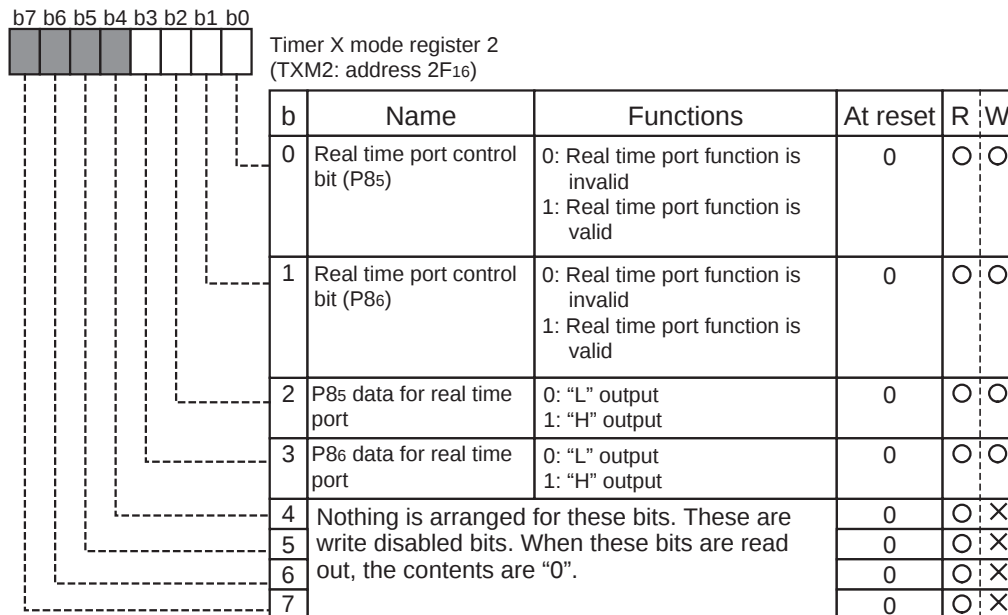
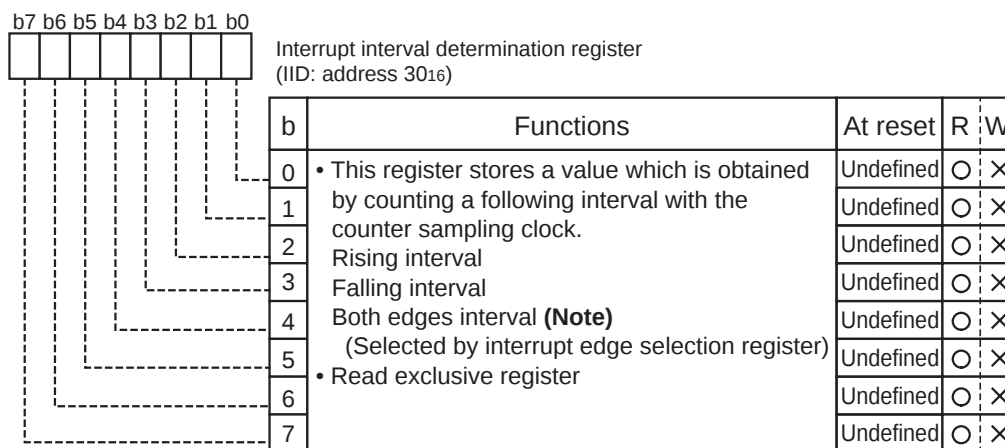


Fig. 3.5.29 Structure of timer X mode register 2

Interrupt interval determination register



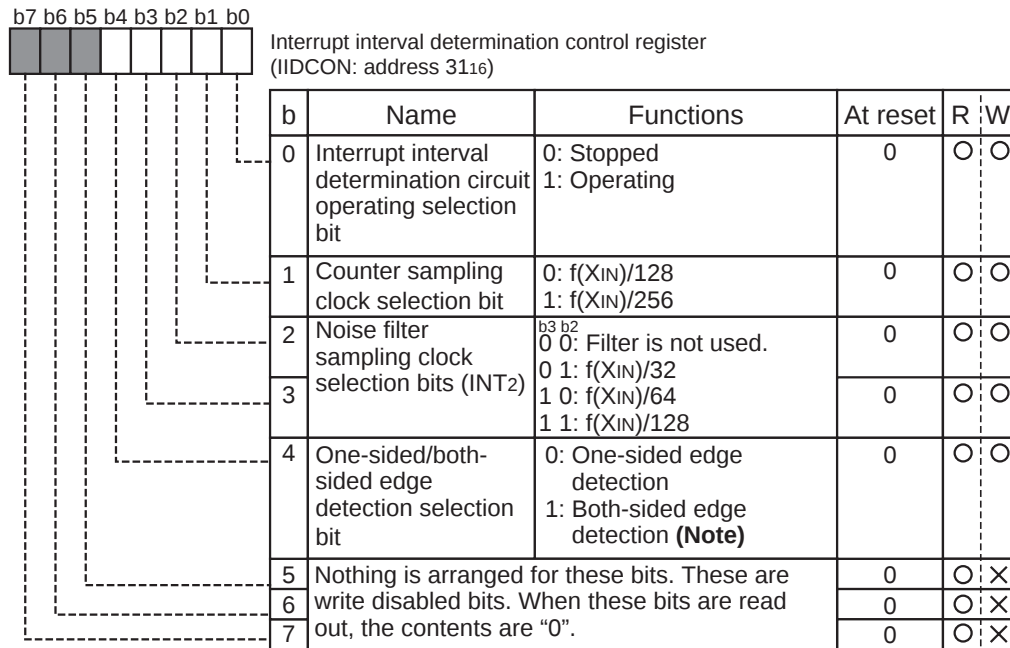
Note: When the noise filter sampling clock selection bits (bits 2, 3) of the interrupt interval determination control register is "00", the both-sided edge detection function cannot be used.

Fig. 3.5.30 Structure of interrupt interval determination register

APPENDIX

3.5 Control registers

Interrupt interval determination control register



Note: When the noise filter sampling clock selection bits (bits 2, 3) is "00", the both-sided edge detection function cannot be used.

Fig. 3.5.31 Structure of interrupt interval determination control register

A-D control register

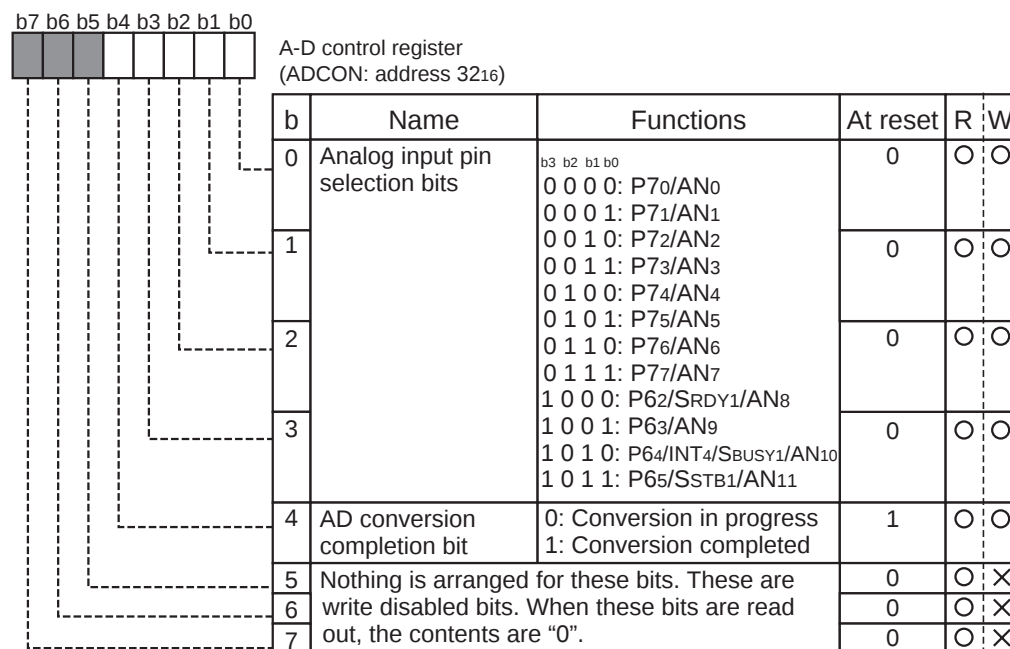


Fig. 3.5.32 Structure of A-D control register

A-D conversion register (low-order)

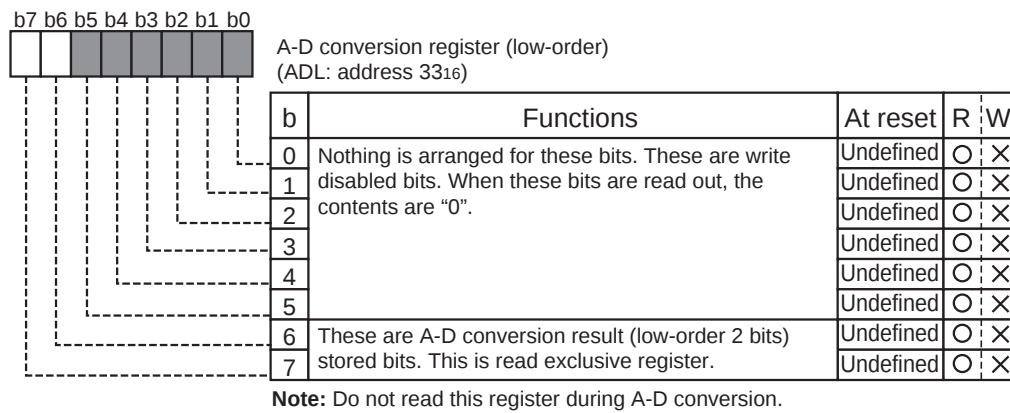


Fig. 3.5.33 Structure of A-D conversion register (low-order)

A-D conversion register (high-order)

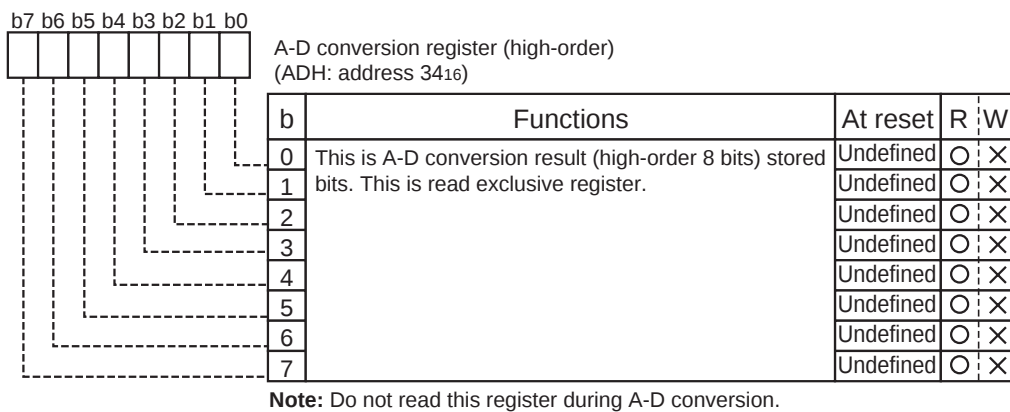


Fig. 3.5.34 Structure of A-D conversion register (high-order)

APPENDIX

3.5 Control registers

Interrupt source switch register

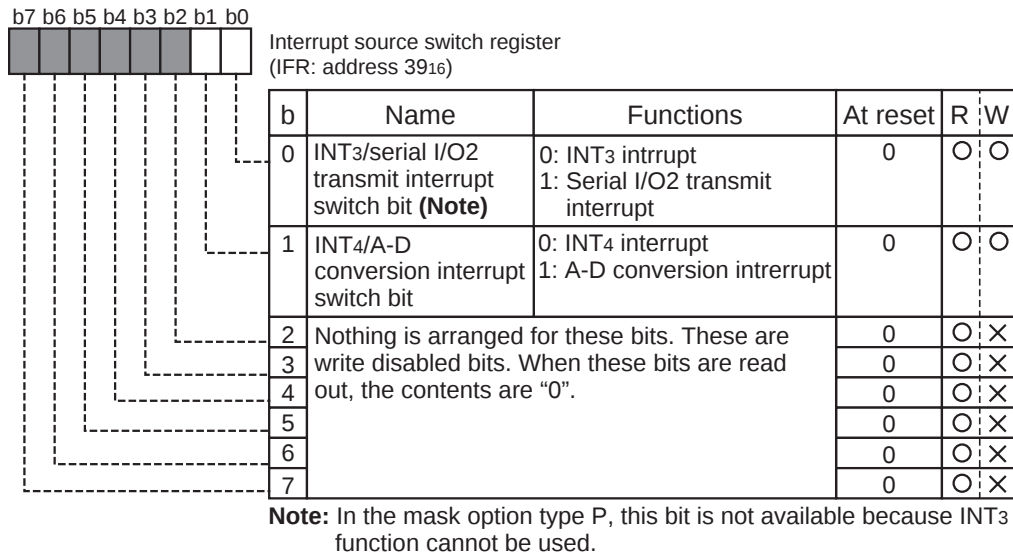


Fig. 3.5.35 Structure of interrupt source switch register

Interrupt edge selection register

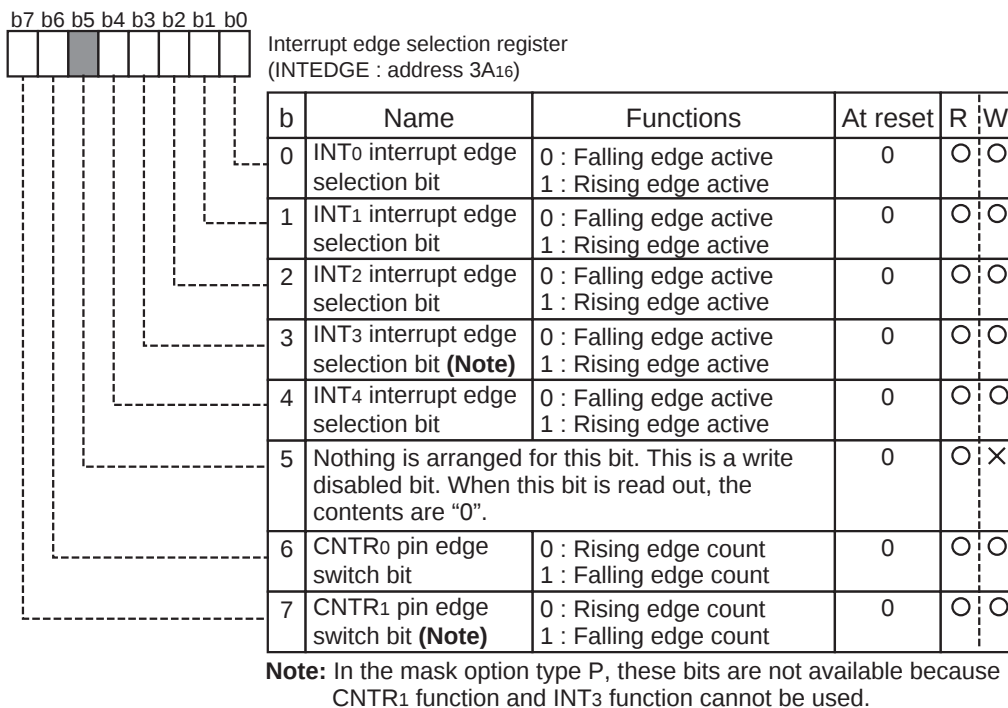


Fig. 3.5.36 Structure of interrupt edge selection register

CPU mode register

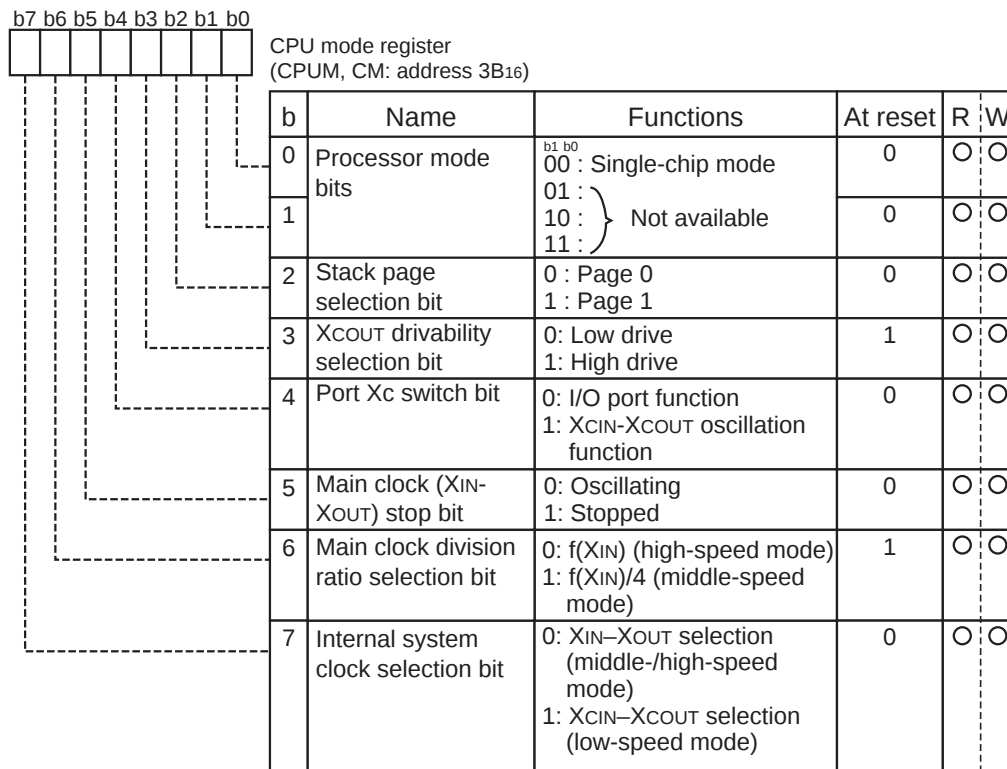


Fig. 3.5.37 Structure of CPU mode register

APPENDIX

3.5 Control registers

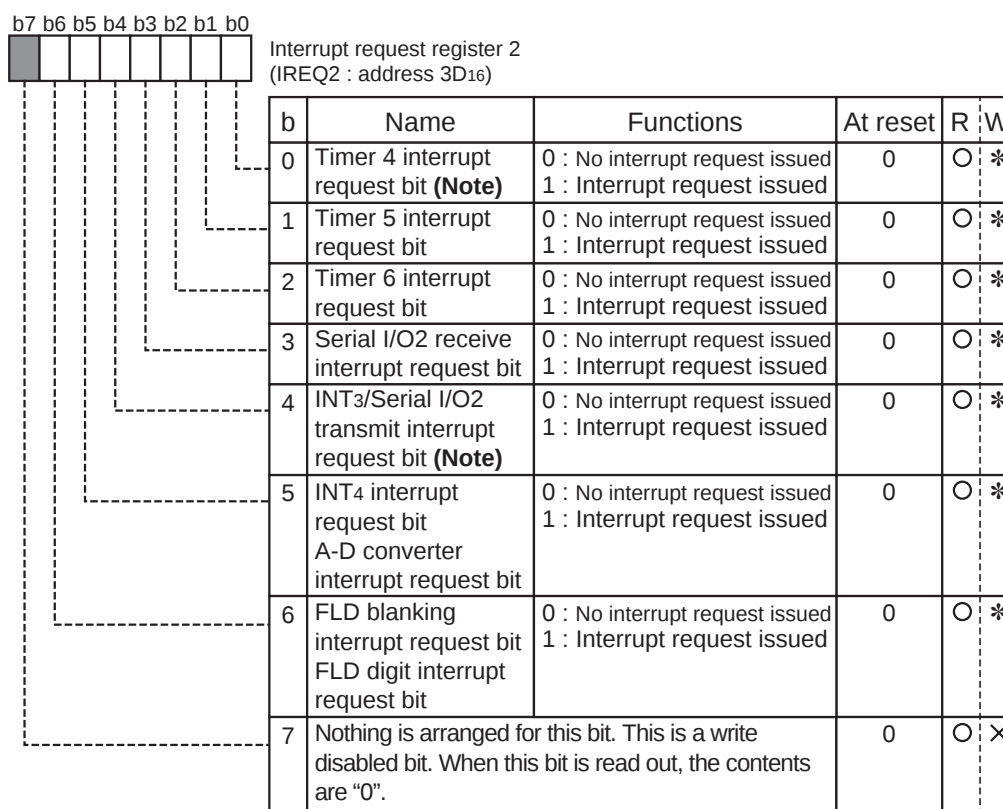
Interrupt request register 1

b7	b6	b5	b4	b3	b2	b1	b0	Interrupt request register 1 (IREQ1 : address 3C16)

※: "0" can be set by software, but "1" cannot be set.

Fig. 3.5.38 Structure of interrupt request register 1

Interrupt request register 2



*: "0" can be set by software, but "1" cannot be set.

Note: In the mask option type P, if timer 4 interrupt whose count source is CNTR1 input and INT3 interrupt are selected, these bits do not become "1".

Fig. 3.5.39 Structure of interrupt request register 2

APPENDIX

3.5 Control registers

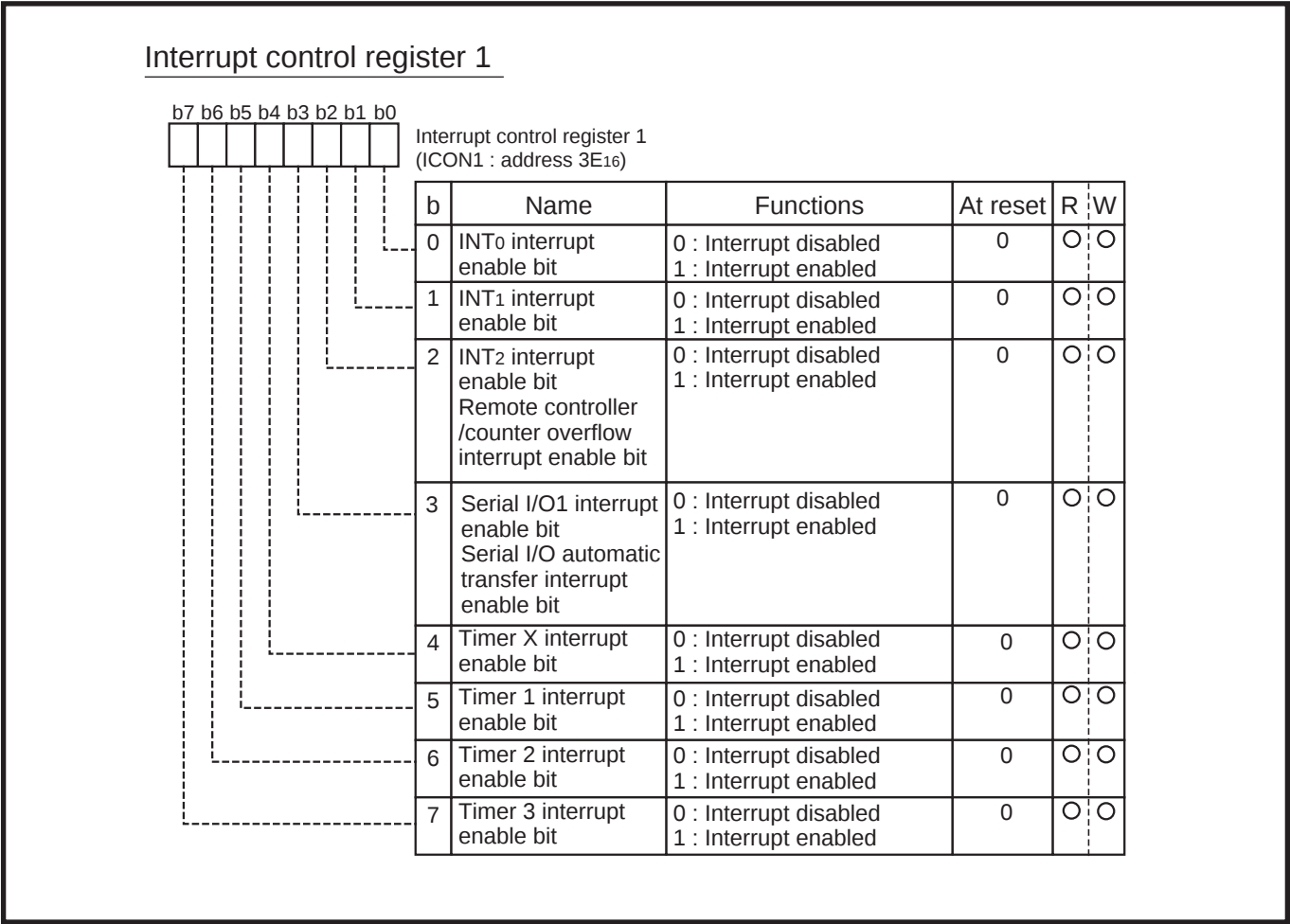
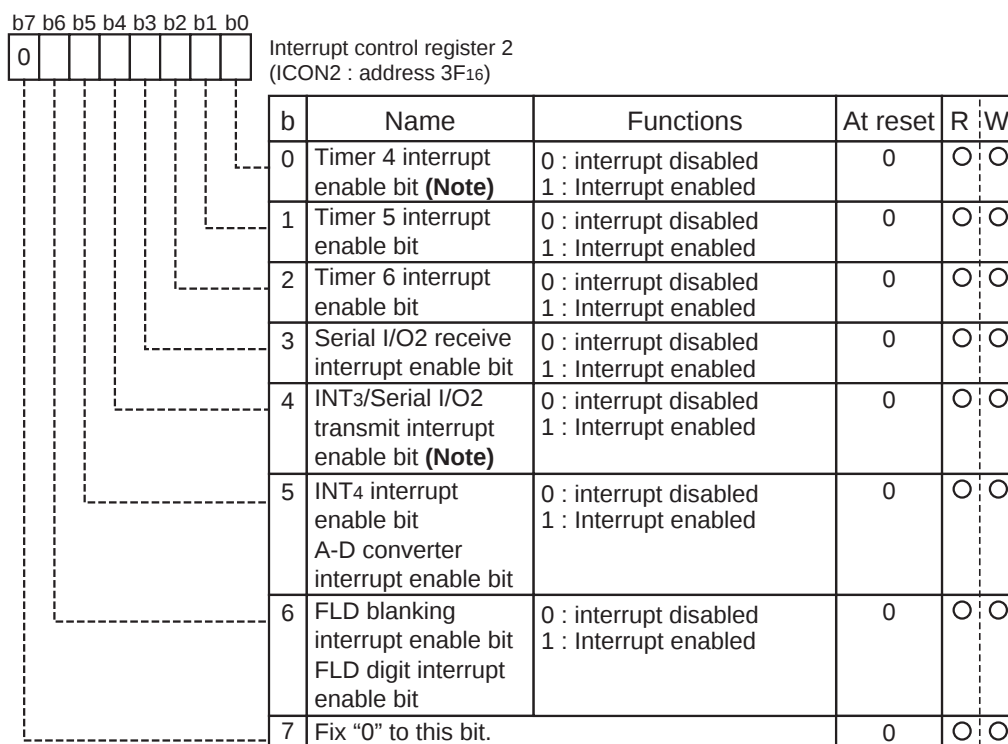


Fig. 3.5.40 Structure of interrupt control register 1

Interrupt control register 2



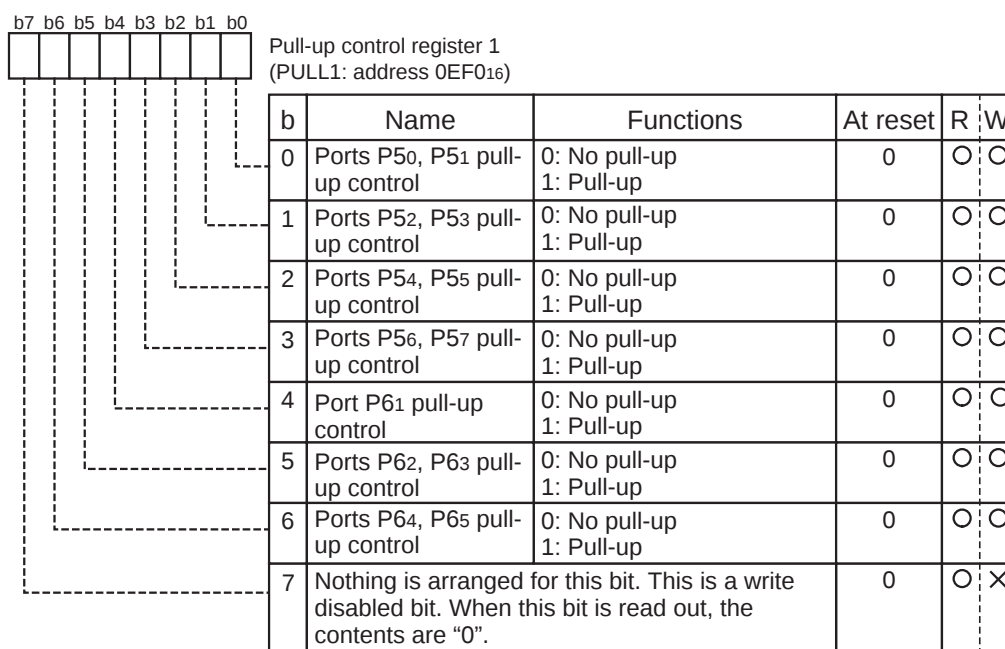
Note: In the mask option type P, timer 4 interrupt whose count source is CNTR1 input and INT3 interrupt are not available.

Fig. 3.5.41 Structure of interrupt control register 2

APPENDIX

3.5 Control registers

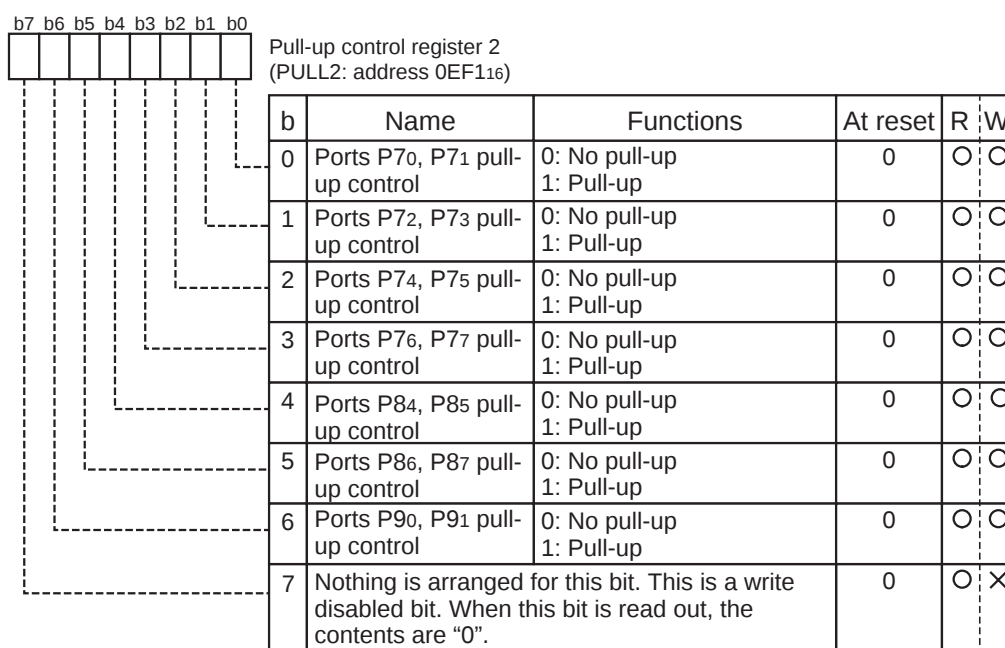
Pull-up control register 1



Note: The pin set to output port is cut off from pull-up control.

Fig. 3.5.42 Structure of pull-up control register 1

Pull-up control register 2



Note: The pin set to output port is cut off from pull-up control.

Fig. 3.5.43 Structure of pull-up control register 2

P1FLDRAM write disable register

b7	b6	b5	b4	b3	b2	b1	b0	P1FLDRAM write disable register (P1FLDRAM: address 0EF216)					
								b	Name	Functions	At reset	R	W
								0	FLDRAM corresponding to port P10 write disable bit	0: Operating normally 1: Write disabled	0	○	○
								1	FLDRAM corresponding to port P11 write disable bit	0: Operating normally 1: Write disabled	0	○	○
								2	FLDRAM corresponding to port P12 write disable bit	0: Operating normally 1: Write disabled	0	○	○
								3	FLDRAM corresponding to port P13 write disable bit	0: Operating normally 1: Write disabled	0	○	○
								4	FLDRAM corresponding to port P14 write disable bit	0: Operating normally 1: Write disabled	0	○	○
								5	FLDRAM corresponding to port P15 write disable bit	0: Operating normally 1: Write disabled	0	○	○
								6	FLDRAM corresponding to port P16 write disable bit	0: Operating normally 1: Write disabled	0	○	○
								7	FLDRAM corresponding to port P17 write disable bit	0: Operating normally 1: Write disabled	0	○	○

Fig. 3.5.44 Structure of P1FLDRAM write disable register

APPENDIX

3.5 Control registers

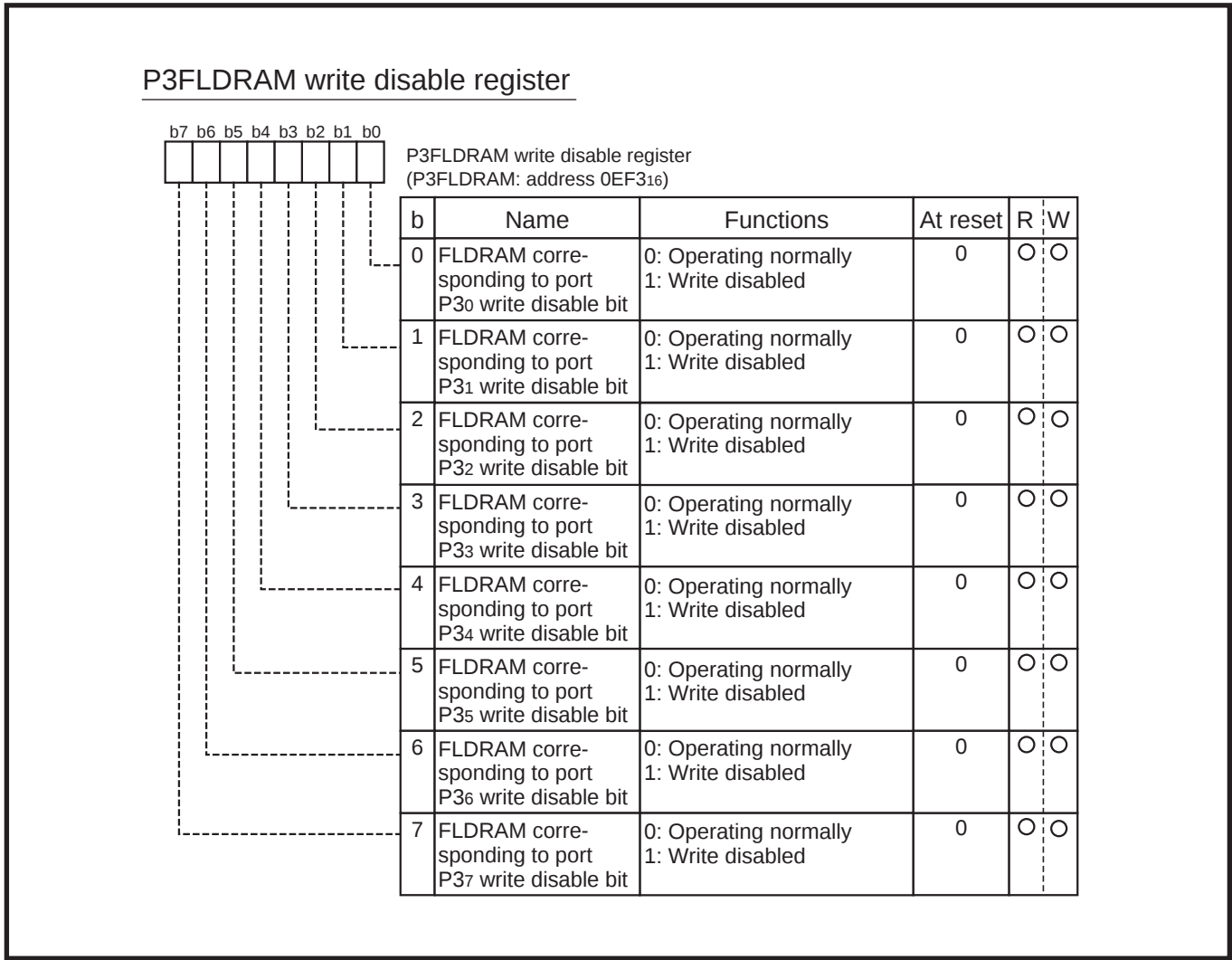


Fig. 3.5.45 Structure of P3FLDRAM write disable register

FLDC mode register

b7 b6 b5 b4 b3 b2 b1 b0								FLDC mode register (FLDM: address 0EF416)					
								b	Name	Functions	At reset	R	W
								0	Automatic display control bit (P0, P1, P2, P3, P8)	0 : General-purpose mode 1 : Automatic display mode	0	○	○
								1	Display start bit	0 : Display stopped 1 : Display in progress (display starts by writing "1")	0	○	○
								2	Tscan control bits	b3 b2 0 0 : 0 FLD digit interrupt (at rising edge of each digit) 0 1 : 1 × Tdisp } 1 0 : 2 × Tdisp } 1 1 : 3 × Tdisp } FLD blanking interrupt (at falling edge of last digit)	0	○	○
								3			0	○	○
								4	Timing number control bit	0 : 16 timing mode 1 : 32 timing mode (Note 2)	0	○	○
								5	Gradation display mode selection control bit	0 : Not selected 1 : Selected (Notes 1, 2)	0	○	○
								6	Tdisp counter count source selection bit	0 : f(XIN)/16 or f(XCIN)/32 1 : f(XIN)/64 or f(XCIN)/128	0	○	○
								7	High-breakdown voltage port drivability selection bit	0 : Drivability strong 1 : Drivability weak	0	○	○

Notes 1: When the gradation display mode is selected, the number of timing is max. 16 timing. (Set "0" to the timing number control bit (b4).)

2: When switching the timing number control bit (b4) or the gradation display mode selection control bit (b5), set "0" to the display start bit (b1) (display stop state) before that.

Fig. 3.5.46 Structure of FLDC mode register

APPENDIX

3.5 Control registers

Tdisp time set register

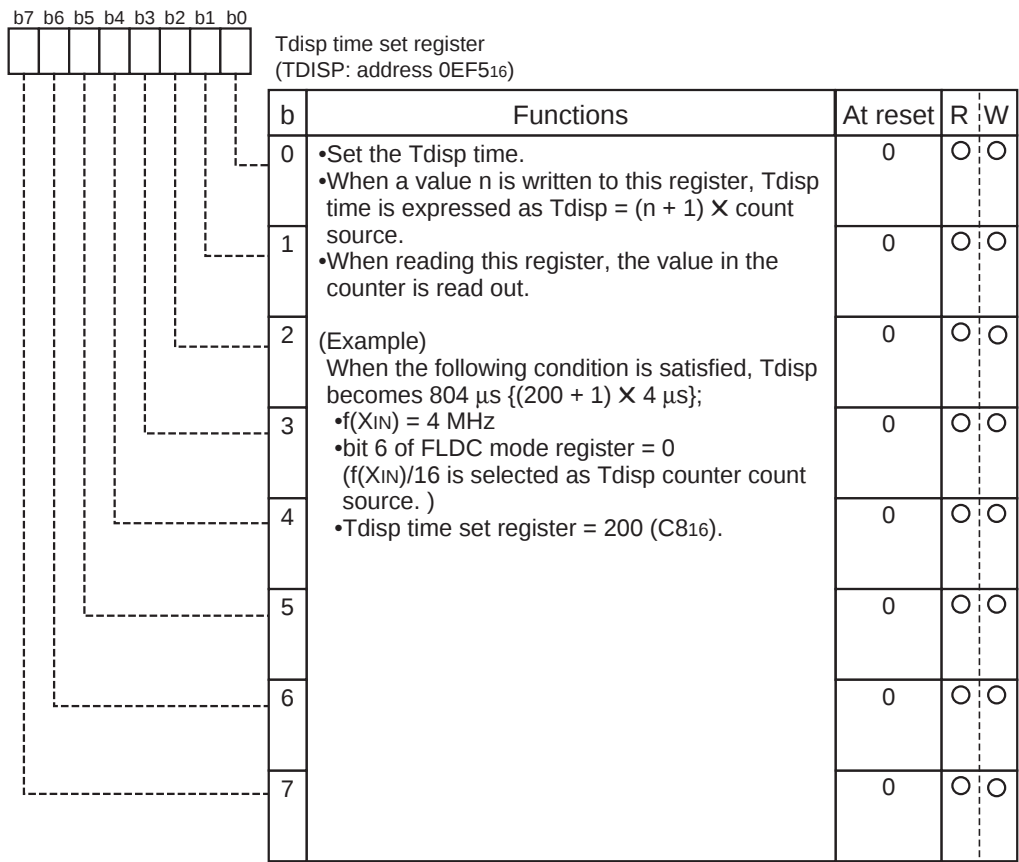


Fig. 3.5.47 Structure of Tdisp time set register

Toff1 time set register

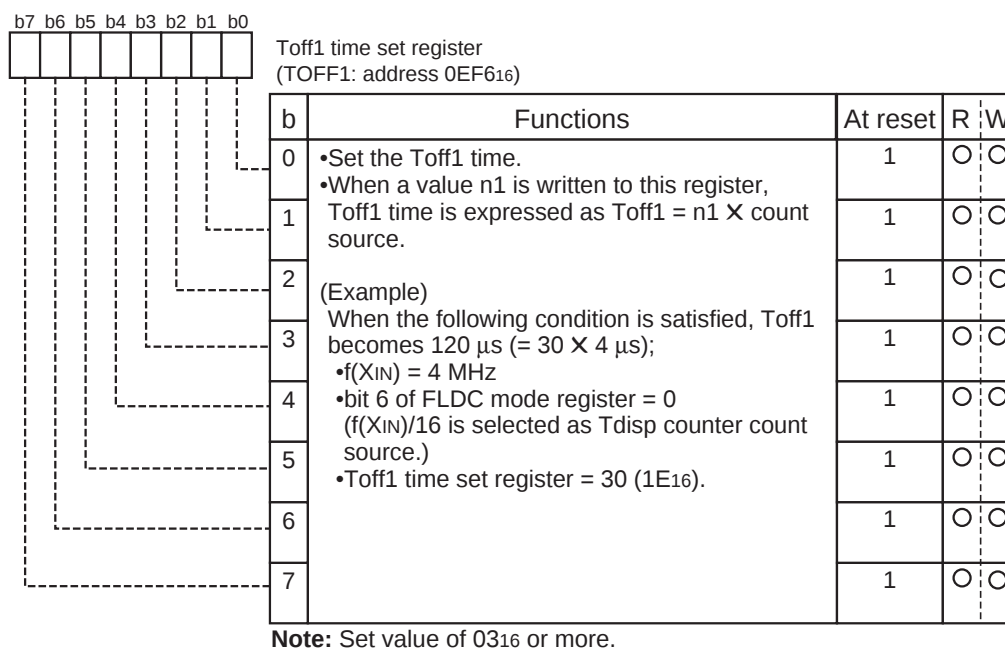


Fig. 3.5.48 Structure of Toff1 time set register

Toff2 time set register

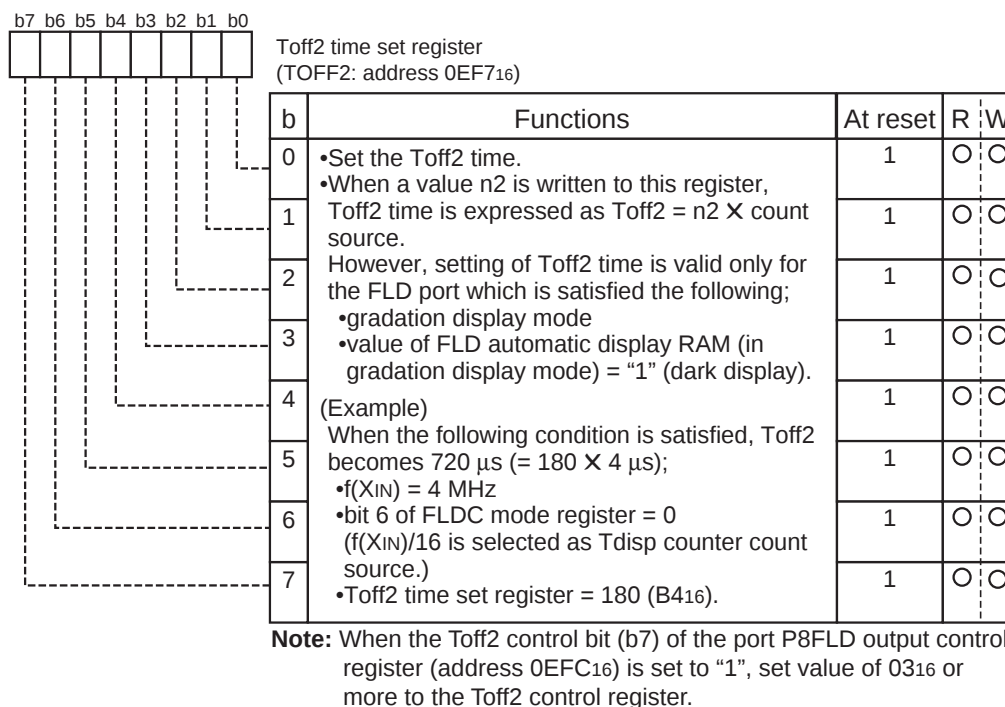


Fig. 3.5.49 Structure of Toff2 time set register

APPENDIX

3.5 Control registers

FLD data pointer/FLD data pointer reload register

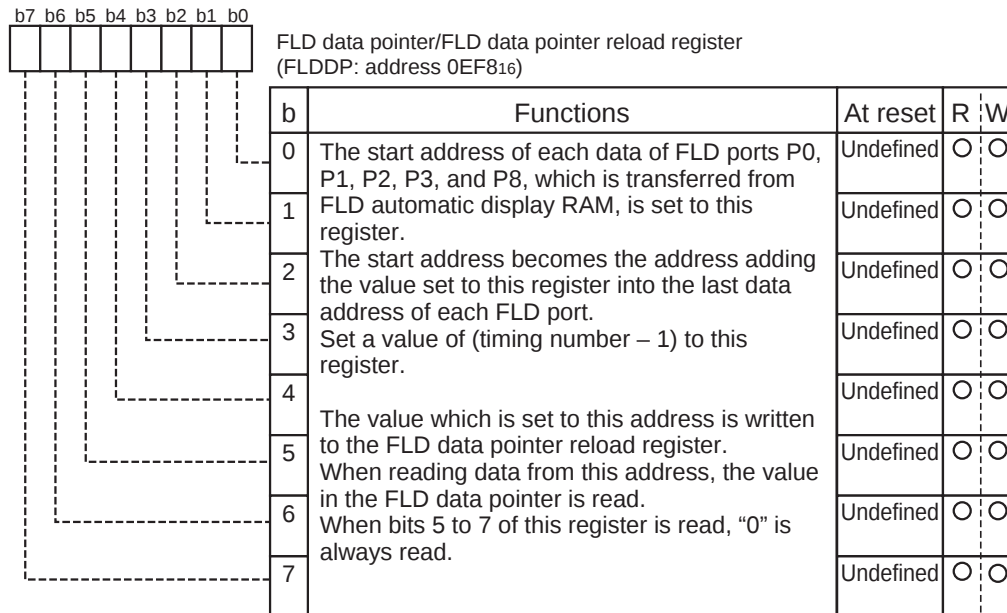


Fig. 3.5.50 Structure of FLD data pointer/FLD data pointer reload register

Port P0FLD/port switch register

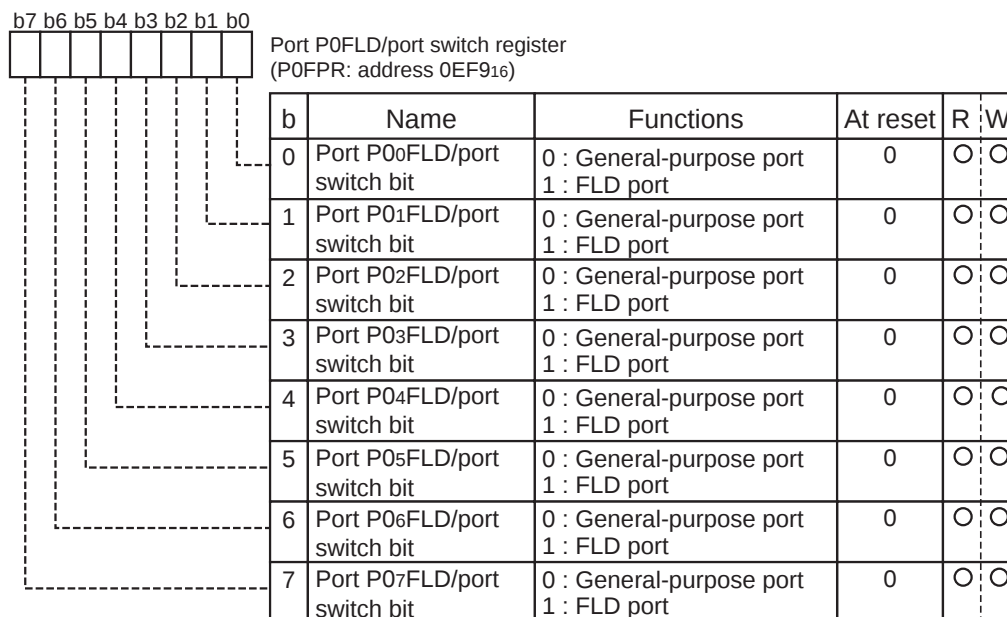


Fig. 3.5.51 Structure of port P0FLD/Port switch register

Port P2FLD/port switch register

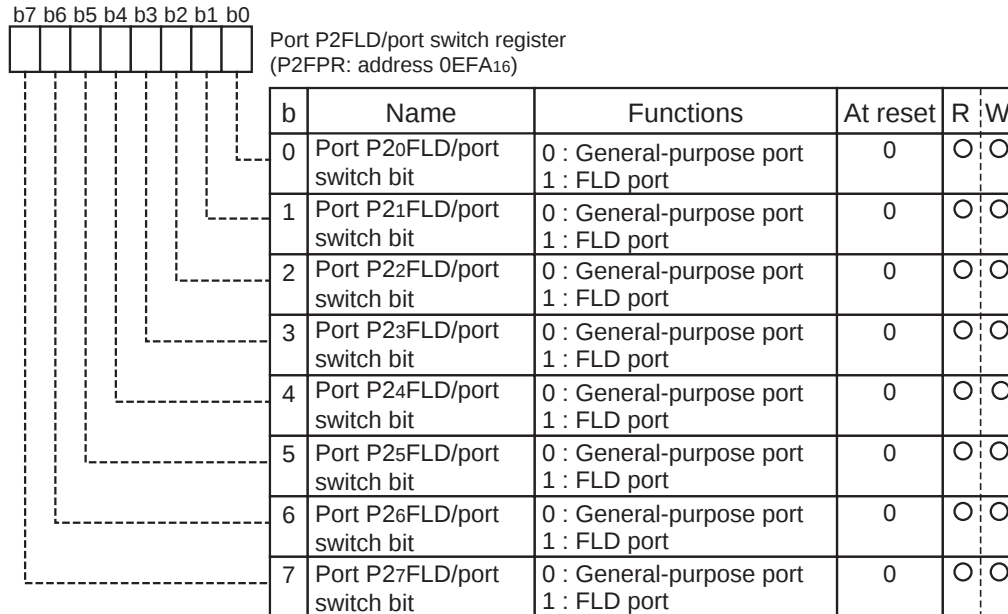


Fig. 3.5.52 Structure of port P2FLD/port switch register

Port P8FLD/port switch register

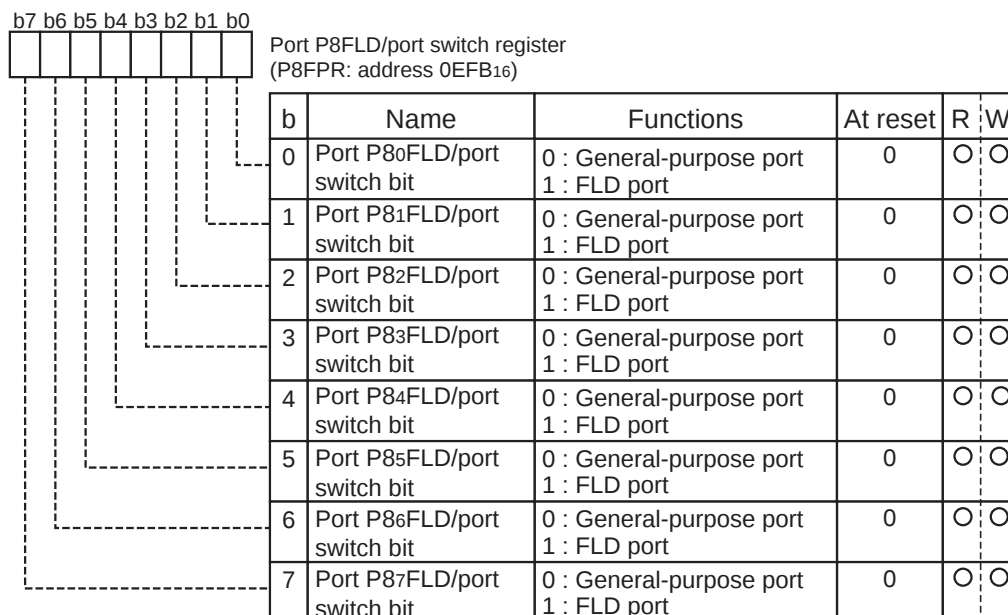


Fig. 3.5.53 Structure of port P8FLD/port switch register

APPENDIX

3.5 Control registers

Port P8FLD output control register

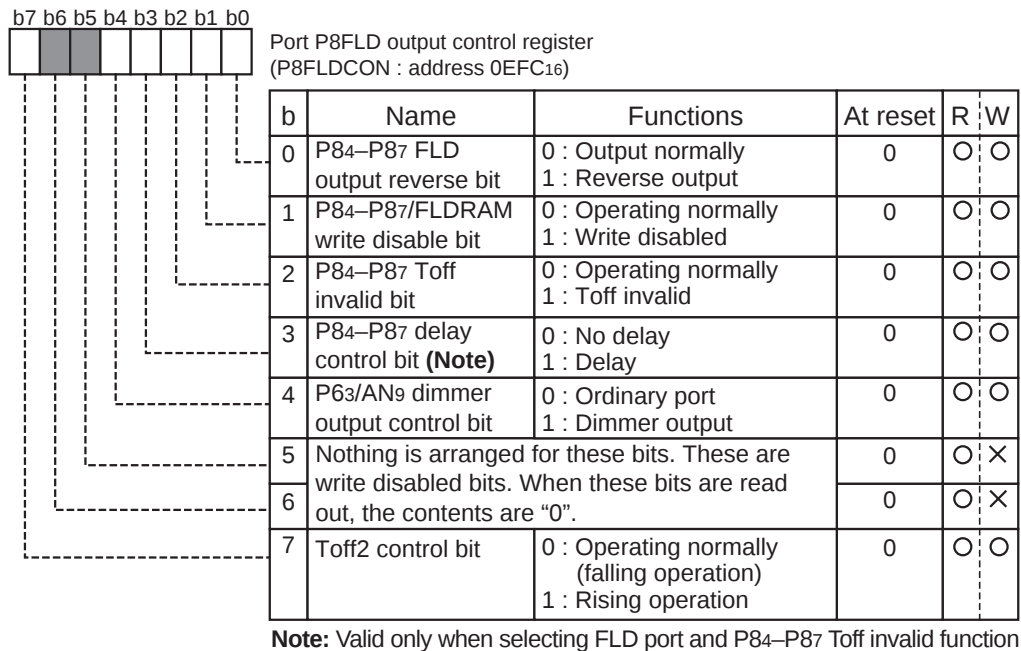


Fig. 3.5.54 Structure of port P8FLD output control register

Buzzer output control register

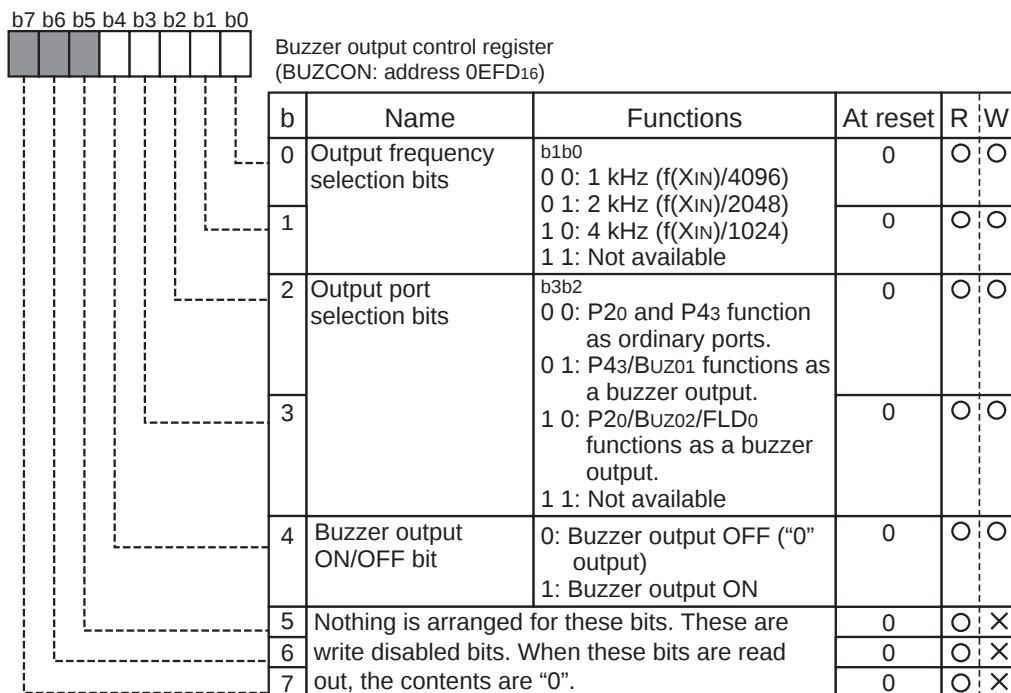


Fig. 3.5.55 Structure of buzzer output control register

3.6 Mask ROM confirmation form

GZZ-SH54-19B<88A1>

Mask ROM number

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38B57M6-XXXFP
mitsubishi electric

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked *.

* Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date:		 	

* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

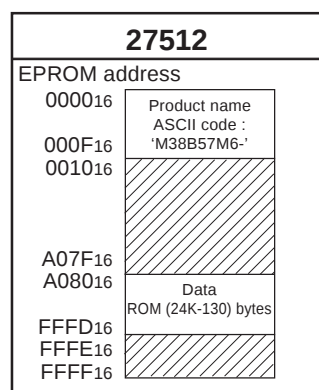
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

--	--	--	--

(hexadecimal notation)

EPROM type



In the address space of the microcomputer, the internal ROM area is from address A080₁₆ to FFFD₁₆. The reset vector is stored in addresses FFFC₁₆ and FFFD₁₆.

- (1) Set the data in the unused area (the shaded area of the diagram) to "FF₁₆".
- (2) The ASCII codes of the product name "M38B57M6-" must be entered in addresses 0000₁₆ to 0008₁₆. And set the data "FF₁₆" in addresses 0009₁₆ to 000F₁₆. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address

0000 ₁₆	'M' = 4D ₁₆
0001 ₁₆	'3' = 33 ₁₆
0002 ₁₆	'8' = 38 ₁₆
0003 ₁₆	'B' = 42 ₁₆
0004 ₁₆	'5' = 35 ₁₆
0005 ₁₆	'7' = 37 ₁₆
0006 ₁₆	'M' = 4D ₁₆
0007 ₁₆	'6' = 36 ₁₆

Address

0008 ₁₆	'-' = 2D ₁₆
0009 ₁₆	FF ₁₆
000A ₁₆	FF ₁₆
000B ₁₆	FF ₁₆
000C ₁₆	FF ₁₆
000D ₁₆	FF ₁₆
000E ₁₆	FF ₁₆
000F ₁₆	FF ₁₆

APPENDIX

3.6 Mask ROM confirmation form

GZZ-SH54-19B<88A1>

Mask ROM number	
-----------------	--

740 FAMILY MASK ROM CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M38B57M6-XXXFP MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program because ASCII codes of the product name are written to addresses 0000₁₆ to 0008₁₆ of EPROM.

EPROM type	27512
The pseudo-command	*=△\$0000 .BYTE △'M38B57M6-'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N) and attach it to the mask ROM confirmation form.

※ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator?

- | | |
|---|---|
| ☐ Ceramic resonator | ☐ Quartz crystal |
| ☐ External clock input | ☐ Other () |

At what frequency?

f(X_{IN}) = MHz

(2) How will you use the X_{CIN}-X_{COU}T oscillator?

- | | |
|---|---|
| ☐ Ceramic resonator | ☐ Quartz crystal |
| ☐ External clock input | ☐ Other () |

At what frequency?

f(X_{CIN}) = kHz

※ 4. Comments

3.6 Mask ROM confirmation form

GZZ-SH54-20B<88A1>

Mask ROM number

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38B57MCH- **XXXFP**
mitsubishi electric

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked *.

*	Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

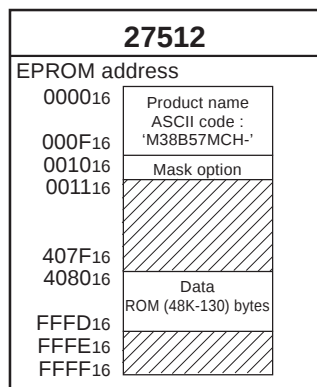
Three EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

(hexadecimal notation)

EPROM type



In the address space of the microcomputer, the internal ROM area is from address 4080₁₆ to FFFD₁₆. The reset vector is stored in addresses FFFC₁₆ and FFFD₁₆.

- (1) Set the data in the unused area (the shaded area of the diagram) to "FF₁₆".
- (2) The ASCII codes of the product name "M38B57MCH-" must be entered in addresses 0000₁₆ to 0009₁₆. And set the data "FF₁₆" in addresses 000A₁₆ to 000F₁₆. The ASCII codes and addresses are listed to the right in hexadecimal notation.
The option data must be entered in address 0010₁₆.

Address

0000 ₁₆	'M' = 4D ₁₆
0001 ₁₆	'3' = 33 ₁₆
0002 ₁₆	'8' = 38 ₁₆
0003 ₁₆	'B' = 42 ₁₆
0004 ₁₆	'5' = 35 ₁₆
0005 ₁₆	'7' = 37 ₁₆
0006 ₁₆	'M' = 4D ₁₆
0007 ₁₆	'C' = 43 ₁₆

Address

0008 ₁₆	'H' = 48 ₁₆
0009 ₁₆	'-' = 2D ₁₆
000A ₁₆	FF ₁₆
000B ₁₆	FF ₁₆
000C ₁₆	FF ₁₆
000D ₁₆	FF ₁₆
000E ₁₆	FF ₁₆
000F ₁₆	FF ₁₆

APPENDIX

3.6 Mask ROM confirmation form

GZZ-SH54-20B<88A1>

Mask ROM number

740 FAMILY MASK ROM CONFIRMATION FORM

SINGLE-CHIP MICROCOMPUTER M38B57MCH- XXXFP

MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program because ASCII codes of the product name are written to addresses 0000₁₆ to 0009₁₆ of EPROM.

EPROM type	27512
The pseudo-command	*= Δ \$0000 .BYTE Δ 'M38B57MCH-'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※ 2. Mask option specification

High-breakdown voltage ports P20 to P27 and P80 to P83 can be selected whether pull-down resistors are built-in or not from among the following 8 types by the mask option.

Select built-in type of pull-down resistors from among the following A to G, P, and fill out the following certainly.

(Fill out the upper part of page 1/3 also.)

Set the data of the same option type name in EPROM specified address. (Set the ASCII code of A to G, P; 41₁₆ to 47₁₆, 50₁₆.)

Set the following pseudo-command to the assembler source program.

EPROM type	27512
The pseudo-command	*= Δ \$0010 .BYTE Δ \$XX

Option type	Connective port of pull-down resistor (connected at "1" writing)											
	P20	P21	P22	P23	P24	P25	P26	P27	P80	P81	P82	P83
A (\$41)												
B (\$42)							1	1				
C (\$43)					1	1	1	1				
D (\$44)			1	1	1	1	1	1				
E (\$45)	1	1	1	1	1	1	1	1				
F (\$46)	1	1	1	1	1	1	1	1	1	1		
G (\$47)	1	1	1	1	1	1	1	1	1	1	1	1
P (\$50)	1	1	1	1	1	1	1	1				

↓

M38B57MCH- XXXFP

Option type
 Fill out with any one of A to G, P.
 (2/3)

GZZ-SH54-20B<88A1>

Mask ROM number

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38B57MCH- [*]XXXFP
MITSUBISHI ELECTRIC

✳ 3. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N) and attach it to the mask ROM confirmation form.

✳ 4. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator?

- | | |
|---|---|
| ☐ Ceramic resonator | ☐ Quartz crystal |
| ☐ External clock input | ☐ Other () |

At what frequency?

f(X_{IN}) = MHz(2) How will you use the X_{CIN}-X_{COU}T oscillator?

- | | |
|---|---|
| ☐ Ceramic resonator | ☐ Quartz crystal |
| ☐ External clock input | ☐ Other () |

At what frequency?

f(X_{CIN}) = kHz

✳ 5. Comments

APPENDIX

3.6 Mask ROM confirmation form

GZZ-SH54-21B<88A1>

Mask ROM number

740 FAMILY MASK ROM CONFIRMATION FORM

SINGLE-CHIP MICROCOMPUTER M38B59MFH-XXXFP

MITSUBISHI ELECTRIC

Receipt

Date:

Section head signature

Supervisor signature

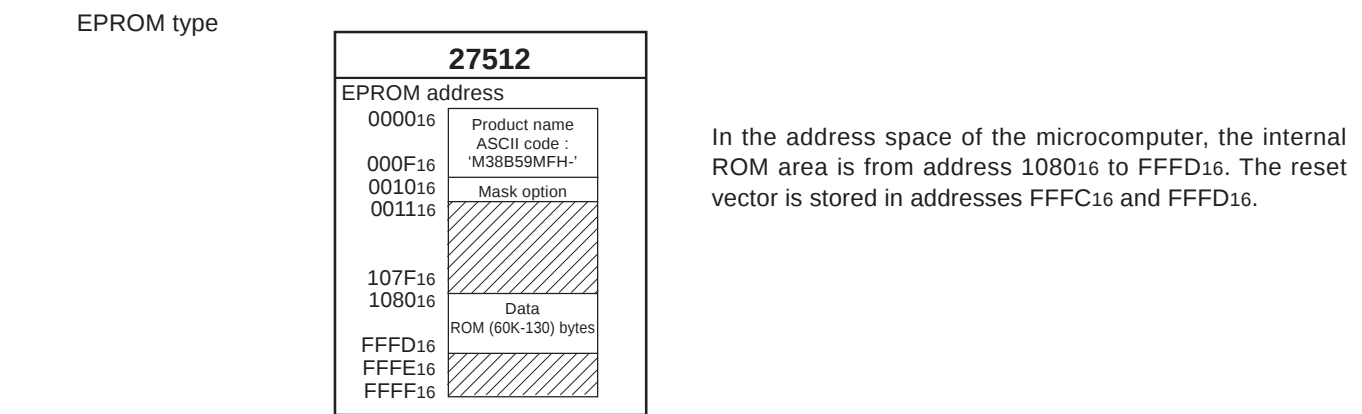
Note : Please fill in all items marked ※.

※ Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
	Date issued	Date:			

- ※ 1. Confirmation
- Specify the name of the product being ordered and the type of EPROMs submitted.
- Three EPROMs are required for each pattern.
- If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

(hexadecimal notation)



- (1) Set the data in the unused area (the shaded area of the diagram) to "FF16".

(2) The ASCII codes of the product name "M38B59MFH-" must be entered in addresses 000016 to 000916. And set the data "FF16" in addresses 000A16 to 000F16. The ASCII codes and addresses are listed to the right in hexadecimal notation.

The option data must be entered in address 001016.
- Address

000016

'M' = 4D16

000116

'3' = 3316

000216

'8' = 3816

000316

'B' = 4216

000416

'5' = 3516

000516

'9' = 3916

000616

'M' = 4D16

000716

'F' = 4616
- Address

000816

'H' = 4816

000916

'_' = 2D16

000A16

FF16

000B16

FF16

000C16

FF16

000D16

FF16

000E16

FF16

000F16

FF16

3.6 Mask ROM confirmation form

GZZ-SH54-21B<88A1>

Mask ROM number

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38B59MFH- * XXXFP
MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program because ASCII codes of the product name are written to addresses 0000₁₆ to 0009₁₆ of EPROM.

EPROM type	27512
The pseudo-command	*= △\$0000 .BYTE △'M38B59MFH-'

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation form, the ROM will not be processed.

※ 2. Mask option specification

High-breakdown voltage ports P20 to P27 and P80 to P83 can be selected whether pull-down resistors are built-in or not from among the following 8 types by the mask option.

Select built-in type of pull-down resistors from among the following A to G, P, and fill out the following certainly.

(Fill out the upper part of page 1/3 also.)

Set the data of the same option type name in EPROM specified address. (Set the ASCII code of A to G, P; 41₁₆ to 47₁₆, 50₁₆.)

Set the following pseudo-command to the assembler source program.

EPROM type	27512
The pseudo-command	*= △\$0010 .BYTE △\$XX

Option type	Connective port of pull-down resistor (connected at "1" writing)											
	P20	P21	P22	P23	P24	P25	P26	P27	P80	P81	P82	P83
A (\$41)												
B (\$42)							1	1				
C (\$43)					1	1	1	1				
D (\$44)			1	1	1	1	1	1				
E (\$45)	1	1	1	1	1	1	1	1				
F (\$46)	1	1	1	1	1	1	1	1	1	1		
G (\$47)	1	1	1	1	1	1	1	1	1	1	1	1
P (\$50)	1	1	1	1	1	1	1	1				



Option type
Fill out with any one of A to G, P.

(2/3)

APPENDIX

3.6 Mask ROM confirmation form

GZZ-SH54-21B<88A1>

Mask ROM number	
-----------------	--

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38B59MFH- [*]XXXFP
MITSUBISHI ELECTRIC

※ 3. Mark specification
Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N) and attach it to the mask ROM confirmation form.

※ 4. Usage conditions
Please answer the following questions about usage for use in our product inspection :

(1) How will you use the XIN-XOUT oscillator?

☐ Ceramic resonator	☐ Quartz crystal
☐ External clock input	☐ Other ()

At what frequency? f(XIN) = MHz

(2) How will you use the XCIN-XCOUT oscillator?

☐ Ceramic resonator	☐ Quartz crystal
☐ External clock input	☐ Other ()

At what frequency? f(XCIN) = kHz

※ 5. Comments

3.7 ROM programming confirmation form

3.7 ROM programming confirmation form

GZZ-SH54-22B<88A0>

ROM number

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M38B59EF-XXXFP
mitsubishi electric

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked *.

*	Customer	Company name	TEL ()	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern.

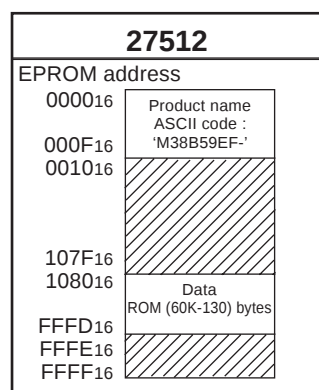
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM programming based on this data. We shall assume the responsibility for errors only if the ROM programming data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

--	--	--	--

(hexadecimal notation)

EPROM type



In the address space of the microcomputer, the internal ROM area is from address 1080₁₆ to FFFD₁₆. The reset vector is stored in addresses FFFC₁₆ and FFFD₁₆.

- (1) Set the data in the unused area (the shaded area of the diagram) to "FF₁₆".
- (2) The ASCII codes of the product name "M38B59EF-" must be entered in addresses 0000₁₆ to 0008₁₆. And set the data "FF₁₆" in addresses 0009₁₆ to 000F₁₆. The ASCII codes and addresses are listed to the right in hexadecimal notation.

Address

0000 ₁₆	'M' = 4D ₁₆
0001 ₁₆	'3' = 33 ₁₆
0002 ₁₆	'8' = 38 ₁₆
0003 ₁₆	'B' = 42 ₁₆
0004 ₁₆	'5' = 35 ₁₆
0005 ₁₆	'9' = 39 ₁₆
0006 ₁₆	'E' = 45 ₁₆
0007 ₁₆	'F' = 46 ₁₆

Address

0008 ₁₆	'-' = 2D ₁₆
0009 ₁₆	FF ₁₆
000A ₁₆	FF ₁₆
000B ₁₆	FF ₁₆
000C ₁₆	FF ₁₆
000D ₁₆	FF ₁₆
000E ₁₆	FF ₁₆
000F ₁₆	FF ₁₆

APPENDIX

3.7 ROM programming confirmation form

GZZ-SH54-22B<88A0>

ROM number	
------------	--

740 FAMILY ROM PROGRAMMING CONFIRMATION FORM SINGLE-CHIP MICROCOMPUTER M38B59EF-XXXFP MITSUBISHI ELECTRIC

We recommend the use of the following pseudo-command to set the start address of the assembler source program because ASCII codes of the product name are written to addresses 0000₁₆ to 0008₁₆ of EPROM.

EPROM type	27512
The pseudo-command	*= Δ\$0000 .BYTE Δ'M38B59EF-'

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM will not be processed.

✳ 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered. Fill out the appropriate mark specification form (80P6N) and attach it to the ROM programming confirmation form.

✳ 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X_{IN}-X_{OUT} oscillator?

- | | |
|---|---|
| ☐ Ceramic resonator | ☐ Quartz crystal |
| ☐ External clock input | ☐ Other () |

At what frequency?

f(X_{IN}) = MHz

(2) How will you use the X_{CIN}-X_{COU}T oscillator?

- | | |
|---|---|
| ☐ Ceramic resonator | ☐ Quartz crystal |
| ☐ External clock input | ☐ Other () |

At what frequency?

f(X_{CIN}) = kHz

✳ 4. Comments

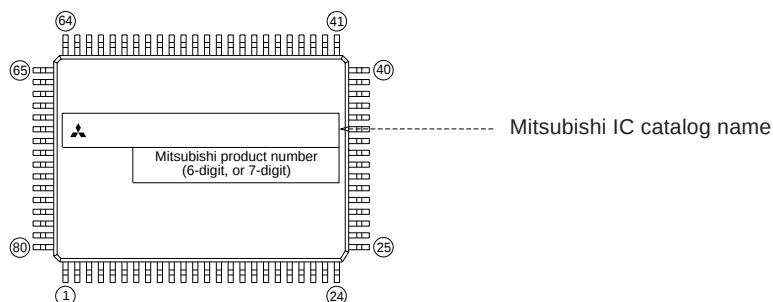
3.8 Mark specification form

80P6N (80-PIN QFP) MARK SPECIFICATION FORM

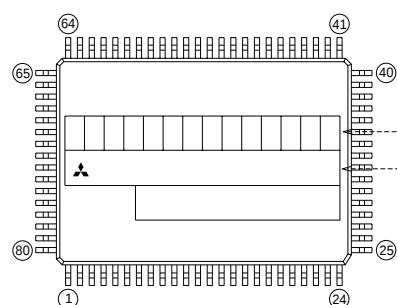
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi IC Catalog Name



Customer's Parts Number

Note : The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Notes 1 : The mark field should be written right aligned.

2 : The fonts and size of characters are standard Mitsubishi type.

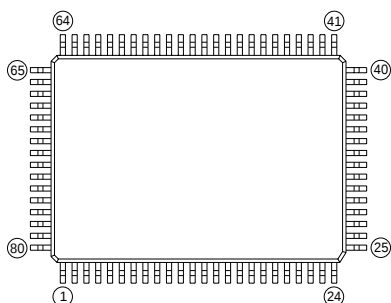
3 : Customer's parts number can be up to 14 alphanumeric characters for capital letters, hyphens, commas, periods and so on.

4 : If the Mitsubishi logo  is not required, check the box below.

 Mitsubishi logo is not required

☐

C. Special Mark Required



Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible.

Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.

2 : If special character fonts (e.g., customer's trade mark logo) must be used in Special Mark, check the box below.

For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

Special character fonts required

☐

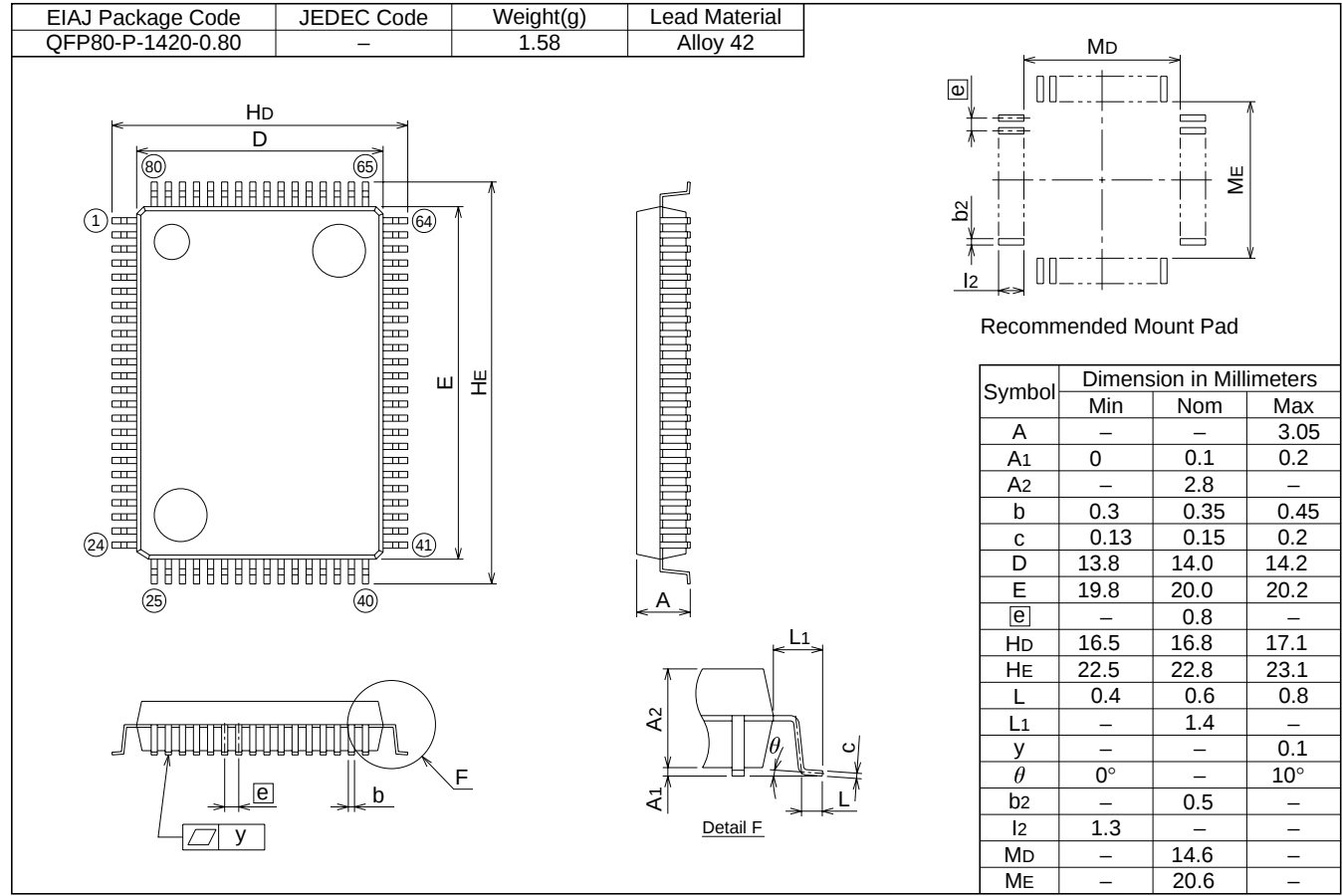
APPENDIX

3.9 Package outline

3.9 Package outline

80P6N-A

Plastic 80pin 14X20mm body QFP



3.10 List of instruction code

D7 – D4 D3 – D0	Hexadecimal notation	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	BRK	ORA IND, X	JSR ZP, IND	BBS 0, A	—	ORA ZP	ASL ZP	BBS 0, ZP	PHP	ORA IMM	ASL A	SEB 0, A	—	ORA ABS	ASL ABS	SEB 0, ZP
0001	1	BPL	ORA IND, Y	CLT	BBC 0, A	—	ORA ZP, X	ASL ZP, X	BBC 0, ZP	CLC	ORA ABS, Y	DEC A	CLB 0, A	—	ORA ABS, X	ASL ABS, X	CLB 0, ZP
0010	2	JSR ABS	AND IND, X	JSR SP	BBS 1, A	BIT ZP	AND ZP	ROL ZP	BBS 1, ZP	PLP	AND IMM	ROL A	SEB 1, A	BIT ABS	AND ABS	ROL ABS	SEB 1, ZP
0011	3	BMI	AND IND, Y	SET	BBC 1, A	—	AND ZP, X	ROL ZP, X	BBC 1, ZP	SEC	AND ABS, Y	INC A	CLB 1, A	LDM ZP	AND ABS, X	ROL ABS, X	CLB 1, ZP
0100	4	RTI	EOR IND, X	STP	BBS 2, A	COM ZP	EOR ZP	LSR ZP	BBS 2, ZP	PHA	EOR IMM	LSR A	SEB 2, A	JMP ABS	EOR ABS	LSR ABS	SEB 2, ZP
0101	5	BVC	EOR IND, Y	—	BBC 2, A	—	EOR ZP, X	LSR ZP, X	BBC 2, ZP	CLI	EOR ABS, Y	—	CLB 2, A	—	EOR ABS, X	LSR ABS, X	CLB 2, ZP
0110	6	RTS	ADC IND, X	MUL ZP, X	BBS 3, A	TST ZP	ADC ZP	ROR ZP	BBS 3, ZP	PLA	ADC IMM	ROR A	SEB 3, A	JMP IND	ADC ABS	ROR ABS	SEB 3, ZP
0111	7	BVS	ADC IND, Y	—	BBC 3, A	—	ADC ZP, X	ROR ZP, X	BBC 3, ZP	SEI	ADC ABS, Y	—	CLB 3, A	—	ADC ABS, X	ROR ABS, X	CLB 3, ZP
1000	8	BRA	STA IND, X	RRF ZP	BBS 4, A	STY ZP	STA ZP	STX ZP	BBS 4, ZP	DEY	—	TXA	SEB 4, A	STY ABS	STA ABS	STX ABS	SEB 4, ZP
1001	9	BCC	STA IND, Y	—	BBC 4, A	STY ZP, X	STA ZP, X	STX ZP, Y	BBC 4, ZP	TYA	STA ABS, Y	TXS	CLB 4, A	—	STA ABS, X	—	CLB 4, ZP
1010	A	LDY IMM	LDA IND, X	LDX IMM	BBS 5, A	LDY ZP	LDA ZP	LDX ZP	BBS 5, ZP	TAY	LDA IMM	TAX	SEB 5, A	LDY ABS	LDA ABS	LDX ABS	SEB 5, ZP
1011	B	BCS	LDA IND, Y	JMP ZP, IND	BBC 5, A	LDY ZP, X	LDA ZP, X	LDX ZP, Y	BBC 5, ZP	CLV	LDA ABS, Y	TSX	CLB 5, A	LDY ABS, X	LDA ABS, X	LDX ABS, Y	CLB 5, ZP
1100	C	CPY IMM	CMP IND, X	WIT	BBS 6, A	CPY ZP	CMP ZP	DEC ZP	BBS 6, ZP	INY	CMP IMM	DEX	SEB 6, A	CPY ABS	CMP ABS	DEC ABS	SEB 6, ZP
1101	D	BNE	CMP IND, Y	—	BBC 6, A	—	CMP ZP, X	DEC ZP, X	BBC 6, ZP	CLD	CMP ABS, Y	—	CLB 6, A	—	CMP ABS, X	DEC ABS, X	CLB 6, ZP
1110	E	CPX IMM	SBC IND, X	DIV ZP, X	BBS 7, A	CPX ZP	SBC ZP	INC ZP	BBS 7, ZP	INX	SBC IMM	NOP	SEB 7, A	CPX ABS	SBC ABS	INC ABS	SEB 7, ZP
1111	F	BEQ	SBC IND, Y	—	BBC 7, A	—	SBC ZP, X	INC ZP, X	BBC 7, ZP	SED	SBC ABS, Y	—	CLB 7, A	—	SBC ABS, X	INC ABS, X	CLB 7, ZP

 : 3-byte instruction

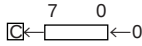
 : 2-byte instruction

 : 1-byte instruction

APPENDIX

3.11 Machine instructions

3.11 Machine instructions

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT, A, R			ZP			BIT, ZP, R		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC (Note 1) (Note 5)	When T = 0 $A \leftarrow A + M + C$ When T = 1 $M(X) \leftarrow M(X) + M + C$	When T = 0, this instruction adds the contents M, C, and A; and stores the results in A and C. When T = 1, this instruction adds the contents of M(X), M and C; and stores the results in M(X) and C. When T=1, the contents of A remain unchanged, but the contents of status flags are changed. M(X) represents the contents of memory where is indicated by X.				69	2	2							65	3	2			
AND (Note 1)	When T = 0 $A \leftarrow A \wedge M$ When T = 1 $M(X) \leftarrow M(X) \wedge M$	When T = 0, this instruction transfers the contents of A and M to the ALU which performs a bit-wise AND operation and stores the result back in A. When T = 1, this instruction transfers the contents M(X) and M to the ALU which performs a bit-wise AND operation and stores the results back in M(X). When T = 1, the contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				29	2	2							25	3	2			
ASL		This instruction shifts the content of A or M by one bit to the left, with bit 0 always being set to 0 and bit 7 of A or M always being contained in C.							0A	2	1				06	5	2			
BBC (Note 4)	Ai or Mi = 0?	This instruction tests the designated bit i of M or A and takes a branch if the bit is 0. The branch address is specified by a relative address. If the bit is 1, next instruction is executed.										13 20i	4	2				17 20i	5	3
BBS (Note 4)	Ai or Mi = 1?	This instruction tests the designated bit i of the M or A and takes a branch if the bit is 1. The branch address is specified by a relative address. If the bit is 0, next instruction is executed.										03 20i	4	2				07 20i	5	3
BCC (Note 4)	C = 0?	This instruction takes a branch to the appointed address if C is 0. The branch address is specified by a relative address. If C is 1, the next instruction is executed.																		
BCS (Note 4)	C = 1?	This instruction takes a branch to the appointed address if C is 1. The branch address is specified by a relative address. If C is 0, the next instruction is executed.																		
BEQ (Note 4)	Z = 1?	This instruction takes a branch to the appointed address when Z is 1. The branch address is specified by a relative address. If Z is 0, the next instruction is executed.																		
BIT	$A \wedge M$	This instruction takes a bit-wise logical AND of A and M contents; however, the contents of A and M are not modified. The contents of N, V, Z are changed, but the contents of A, M remain unchanged.													24	3	2			
BMI (Note 4)	N = 1?	This instruction takes a branch to the appointed address when N is 1. The branch address is specified by a relative address. If N is 0, the next instruction is executed.																		
BNE (Note 4)	Z = 0?	This instruction takes a branch to the appointed address if Z is 0. The branch address is specified by a relative address. If Z is 1, the next instruction is executed.																		

3.11 Machine instructions

Addressing mode																				Processor status register																							
ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0			
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C						
75	4	2				6D	4	3	7D	5	3	79	5	3									61	6	2	71	6	2							N	V	•	•	•	•	Z	C	
35	4	2				2D	4	3	3D	5	3	39	5	3									21	6	2	31	6	2							N	•	•	•	•	•	•	Z	•
16	6	2				0E	6	3	1E	7	3																						N	•	•	•	•	•	•	Z	C		
																												</															

APPENDIX

3.11 Machine instructions

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT, A			ZP			BIT, ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
BPL (Note 4)	N = 0?	This instruction takes a branch to the ap- pointed address if N is 0. The branch address is specified by a relative address. If N is 1, the next instruction is executed.																		
BRA	PC ← PC ± offset	This instruction branches to the appointed ad- dress. The branch address is specified by a relative address.																		
BRK	B ← 1 (PC) ← (PC) + 2 M(S) ← PCH S ← S − 1 M(S) ← PCL S ← S − 1 M(S) ← PS S ← S − 1 I ← 1 PCL ← ADL PCH ← ADH	When the BRK instruction is executed, the CPU pushes the current PC contents onto the stack. The BADRS designated in the interrupt vector table is stored into the PC.	00	7	1															
BVC (Note 4)	V = 0?	This instruction takes a branch to the ap- pointed address if V is 0. The branch address is specified by a relative address. If V is 1, the next instruction is executed.																		
BVS (Note 4)	V = 1?	This instruction takes a branch to the ap- pointed address when V is 1. The branch address is specified by a relative address. When V is 0, the next instruction is executed.																		
CLB	Ai or Mi ← 0	This instruction clears the designated bit i of A or M.										1B 20i	2	1				1F 20i	5	2
CLC	C ← 0	This instruction clears C.	18	2	1															
CLD	D ← 0	This instruction clears D.	D8	2	1															
CLI	I ← 0	This instruction clears I.	58	2	1															
CLT	T ← 0	This instruction clears T.	12	2	1															
CLV	V ← 0	This instruction clears V.	B8	2	1															
CMP (Note 3)	When T = 0 A − M When T = 1 M(X) − M	When T = 0, this instruction subtracts the con- tents of M from the contents of A. The result is not stored and the contents of A or M are not modified. When T = 1, the CMP subtracts the contents of M from the contents of M(X). The result is not stored and the contents of X, M, and A are not modified. M(X) represents the contents of memory where is indicated by X.				C9	2	2							C5	3	2			
COM	M ← M	This instruction takes the one's complement of the contents of M and stores the result in M.													44	5	2			
CPX	X − M	This instruction subtracts the contents of M from the contents of X. The result is not stored and the contents of X and M are not modified.				E0	2	2							E4	3	2			
CPY	Y − M	This instruction subtracts the contents of M from the contents of Y. The result is not stored and the contents of Y and M are not modified.				C0	2	2							C4	3	2			
DEC	A ← A − 1 or M ← M − 1	This instruction subtracts 1 from the contents of A or M.							1A	2	1				C6	5	2			

APPENDIX

3.11 Machine instructions

Addressing mode																												Processor status register												
ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C			
																														.	.	.	.	.	.	.	.			
																														.	.	.	.	.	.	.	.			
																														.	.	.	1	.	1	.	.			
																														.	.	.	.	.	.	.	.			
																														.	.	.	.	.	.	.	.			
																														.	.	.	.	.	.	.	.			
																														.	.	.	.	.	.	.	.			
																														.	.	.	.	.	.	.	0			
																														.	.	.	.	0	.	.	.			
																														.	.	.	.	.	0	.	.			
																														.	.	0	.	.	.	.	.			
																														.	0	.	.	.	.	.	.			
D5	4	2				CD	4	3	DD	5	3	D9	5	3				C1	6	2	D1	6	2					N	.	.	.	.	.	.	Z	C				
																													N	.	.	.	.	.	.	Z	.			
						EC	4	3																				N	.	.	.	.	.	.	Z	C				
						CC	4	3																				N	.	.	.	.	.	.	Z	C				
D6	6	2				CE	6	3	DE	7	3																	N	.	.	.	.	.	.	Z	.				

APPENDIX

3.11 Machine instructions

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT, A			ZP			BIT, ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
DEX	$X \leftarrow X - 1$	This instruction subtracts one from the current contents of X.	CA	2	1															
DEY	$Y \leftarrow Y - 1$	This instruction subtracts one from the current contents of Y.	88	2	1															
DIV	$A \leftarrow (M(zz + X + 1), M(zz + X)) / A$ $M(S) \leftarrow \text{one's complement of Remainder}$ $S \leftarrow S - 1$	This instruction divides the 16-bit data in M(zz+(X)) (low-order byte) and M(zz+(X)+1) (high-order byte) by the contents of A. The quotient is stored in A and the one's complement of the remainder is pushed onto the stack.																		
EOR (Note 1)	When T = 0 $A \leftarrow A \vee M$ When T = 1 $M(X) \leftarrow M(X) \vee M$	When T = 0, this instruction transfers the contents of the M and A to the ALU which performs a bit-wise Exclusive OR, and stores the result in A. When T = 1, the contents of M(X) and M are transferred to the ALU, which performs a bit-wise Exclusive OR and stores the results in M(X). The contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				49	2	2							45	3	2			
INC	$A \leftarrow A + 1$ or $M \leftarrow M + 1$	This instruction adds one to the contents of A or M.							3A	2	1				E6	5	2			
INX	$X \leftarrow X + 1$	This instruction adds one to the contents of X.	E8	2	1															
INY	$Y \leftarrow Y + 1$	This instruction adds one to the contents of Y.	C8	2	1															
JMP	If addressing mode is ABS $PCL \leftarrow ADL$ $PCH \leftarrow ADH$ If addressing mode is IND $PCL \leftarrow M(ADH, ADL)$ $PCH \leftarrow M(ADH, ADL + 1)$ If addressing mode is ZP, IND $PCL \leftarrow M(00, ADL)$ $PCH \leftarrow M(00, ADL + 1)$	This instruction jumps to the address designated by the following three addressing modes: Absolute Indirect Absolute Zero Page Indirect Absolute																		
JSR	$M(S) \leftarrow PCH$ $S \leftarrow S - 1$ $M(S) \leftarrow PCL$ $S \leftarrow S - 1$ After executing the above, if addressing mode is ABS, $PCL \leftarrow ADL$ $PCH \leftarrow ADH$ if addressing mode is SP, $PCL \leftarrow ADL$ $PCH \leftarrow FF$ If addressing mode is ZP, IND, $PCL \leftarrow M(00, ADL)$ $PCH \leftarrow M(00, ADL + 1)$	This instruction stores the contents of the PC in the stack, then jumps to the address designated by the following addressing modes: Absolute Special Page Zero Page Indirect Absolute																		
LDA (Note 2)	When T = 0 $A \leftarrow M$ When T = 1 $M(X) \leftarrow M$	When T = 0, this instruction transfers the contents of M to A. When T = 1, this instruction transfers the contents of M to (M(X)). The contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				A9	2	2							A5	3	2			
LDM	$M \leftarrow nn$	This instruction loads the immediate value in M.													3C	4	3			
LDX	$X \leftarrow M$	This instruction loads the contents of M in X.				A2	2	2							A6	3	2			
LDY	$Y \leftarrow M$	This instruction loads the contents of M in Y.				A0	2	2							A4	3	2			

3.11 Machine instructions

Addressing mode																		Processor status register																						
ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C			
																														N	•	•	•	•	•	•	Z	•		
																														N	•	•	•	•	•	•	Z	•		
E2	16	2																												•	•	•	•	•	•	•	•	•		
55	4	2				4D	4	3	5D	5	3	59	5	3							41	6	2	51	6	2				N	•	•	•	•	•	•	Z	•		
F6	6	2				EE	6	3	FE	7	3																		N	•	•	•	•	•	•	Z	•			
																														N	•	•	•	•	•	•	Z	•		
																														N	•	•	•	•	•	•	Z	•		
						4C	3	3						6C	5	3	B2	4	2											•	•	•	•	•	•	•	•	•		
						20	6	3									02	7	2									22	5	2	•	•	•	•	•	•	•	•	•	
B5	4	2				AD	4	3	BD	5	3	B9	5	3							A1	6	2	B1	6	2				N	•	•	•	•	•	•	Z	•		
																														•	•	•	•	•	•	•	•	•		
																														N	•	•	•	•	•	•	Z	•		
B4	4	2				AC	4	3	BC	5	3																		N	•	•	•	•	•	•	Z	•			

APPENDIX

3.11 Machine instructions

Symbol	Function	Details	Addressing mode																		
			IMP			IMM			A			BIT, A			ZP			BIT, ZP			
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	
LSR		This instruction shifts either A or M one bit to the right such that bit 7 of the result always is set to 0, and the bit 0 is stored in C.								4A	2	1				46	5	2			
MUL	$M(S) \cdot A \leftarrow A * M(zz + X)$ $S \leftarrow S - 1$	This instruction multiply Accumulator with the memory specified by the Zero Page X address mode and stores the high-order byte of the result on the Stack and the low-order byte in A.																			
NOP	$PC \leftarrow PC + 1$	This instruction adds one to the PC but does no otheroperation.	EA	2	1																
ORA (Note 1)	When T = 0 $A \leftarrow A \vee M$ When T = 1 $M(X) \leftarrow M(X) \vee M$	When T = 0, this instruction transfers the contents of A and M to the ALU which performs a bit-wise “OR”, and stores the result in A. When T = 1, this instruction transfers the contents of M(X) and the M to the ALU which performs a bit-wise OR, and stores the result in M(X). The contents of A remain unchanged, but status flags are changed. M(X) represents the contents of memory where is indicated by X.				09	2	2								05	3	2			
PHA	$M(S) \leftarrow A$ $S \leftarrow S - 1$	This instruction pushes the contents of A to the memory location designated by S, and decrements the contents of S by one.	48	3	1																
PHP	$M(S) \leftarrow PS$ $S \leftarrow S - 1$	This instruction pushes the contents of PS to the memory location designated by S and decrements the contents of S by one.	08	3	1																
PLA	$S \leftarrow S + 1$ $A \leftarrow M(S)$	This instruction increments S by one and stores the contents of the memory designated by S in A.	68	4	1																
PLP	$S \leftarrow S + 1$ $PS \leftarrow M(S)$	This instruction increments S by one and stores the contents of the memory location designated by S in PS.	28	4	1																
ROL		This instruction shifts either A or M one bit left through C. C is stored in bit 0 and bit 7 is stored in C.								2A	2	1				26	5	2			
ROR		This instruction shifts either A or M one bit right through C. C is stored in bit 7 and bit 0 is stored in C.								6A	2	1				66	5	2			
RRF		This instruction rotates 4 bits of the M content to the right.														82	8	2			
RTI	$S \leftarrow S + 1$ $PS \leftarrow M(S)$ $S \leftarrow S + 1$ $PCL \leftarrow M(S)$ $S \leftarrow S + 1$ $PCH \leftarrow M(S)$	This instruction increments S by one, and stores the contents of the memory location designated by S in PS. S is again incremented by one and stores the contents of the memory location designated by S in PCL. S is again incremented by one and stores the contents of the memory location designated by S in PCH.	40	6	1																
RTS	$S \leftarrow S + 1$ $PCL \leftarrow M(S)$ $S \leftarrow S + 1$ $PCH \leftarrow M(S)$ $(PC) \leftarrow (PC) + 1$	This instruction increments S by one and stores the contents of the memory location designated by S in PCL. S is again incremented by one and the contents of the memory location is stored in PCH. PC is incremented by 1.	60	6	1																

3.11 Machine instructions

Addressing mode																								Processor status register																			
ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0			
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C						
56	6	2				4E	6	3	5E	7	3																		0	.	.	.	.	.	.	Z	C						
62	15	2																												.	.	.	.	.	.	.	.	.					
																														.	.	.	.	.	.	.	.	.					
15	4	2				0D	4	3	1D	5	3	19	5	3							01	6	2	11	6	2				N	.	.	.	.	.	.	Z	.					
																														.	.	.	.	.	.	.	.	.					
																														.	.	.	.	.	.	.	.	.					
																														N	.	.	.	.	.	.	Z	.					
																														(Value saved in stack)													
36	6	2				2E	6	3	3E	7	3																		N	.	.	.	.	.	.	Z	C						
76	6	2				6E	6	3	7E	7	3																		N	.	.	.	.	.	.	Z	C						
																														.	.	.	.	.	.	.	.	.					
																														(Value saved in stack)													
																														.	.	.	.	.	.	.	.	.					

APPENDIX

3.11 Machine instructions

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT, A			ZP			BIT, ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
SBC (Note 1) (Note 5)	When T = 0 $A \leftarrow A - M - \overline{C}$ When T = 1 $M(X) \leftarrow M(X) - M - \overline{C}$	When T = 0, this instruction subtracts the value of M and the complement of C from A, and stores the results in A and C. When T = 1, the instruction subtracts the contents of M and the complement of C from the contents of M(X), and stores the results in M(X) and C. A remain unchanged, but status flag are changed. M(X) represents the contents of memory where is indicated by X.				E9	2	2							E5	3	2			
SEB	A_i or $M_i \leftarrow 1$	This instruction sets the designated bit i of A or M.										0F 20i	2	1				0F 20i	5	2
SEC	$C \leftarrow 1$	This instruction sets C.	38	2	1															
SED	$D \leftarrow 1$	This instruction set D.	F8	2	1															
SEI	$I \leftarrow 1$	This instruction set I.	78	2	1															
SET	$T \leftarrow 1$	This instruction set T.	32	2	1															
STA	$M \leftarrow A$	This instruction stores the contents of A in M. The contents of A does not change.													85	4	2			
STP		This instruction resets the oscillation control F/ F and the oscillation stops. Reset or interrupt input is needed to wake up from this mode.	42	2	1															
STX	$M \leftarrow X$	This instruction stores the contents of X in M. The contents of X does not change.													86	4	2			
STY	$M \leftarrow Y$	This instruction stores the contents of Y in M. The contents of Y does not change.													84	4	2			
TAX	$X \leftarrow A$	This instruction stores the contents of A in X. The contents of A does not change.	AA	2	1															
TAY	$Y \leftarrow A$	This instruction stores the contents of A in Y. The contents of A does not change.	A8	2	1															
TST	$M = 0?$	This instruction tests whether the contents of M are "0" or not and modifies the N and Z.													64	3	2			
TSX	$X \leftarrow S$	This instruction transfers the contents of S in X.	BA	2	1															
TXA	$A \leftarrow X$	This instruction stores the contents of X in A.	8A	2	1															
TXS	$S \leftarrow X$	This instruction stores the contents of X in S.	9A	2	1															
TYA	$A \leftarrow Y$	This instruction stores the contents of Y in A.	98	2	1															
WIT		The WIT instruction stops the internal clock but not the oscillation of the oscillation circuit is not stopped. CPU starts its function after the Timer X over flows (comes to the terminal count). All registers or internal memory contents except Timer X will not change during this mode. (Of course needs VDD).	C2	2	1															

Notes 1 : The number of cycles "n" is increased by 3 when T is 1.
2 : The number of cycles "n" is increased by 2 when T is 1.
3 : The number of cycles "n" is increased by 1 when T is 1.
4 : The number of cycles "n" is increased by 2 when branching has occurred.
5 : N, V, and Z flags are invalid in decimal operation mode.

3.11 Machine instructions

Addressing mode																		Processor status register																						
ZP, X			ZP, Y			ABS			ABS, X			ABS, Y			IND			ZP, IND			IND, X			IND, Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C			
F5	4	2				ED	4	3	FD	5	3	F9	5	3							E1	6	2	F1	6	2				N	V	•	•	•	•	Z	C			
																														•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	1			
																														•	•	•	•	1	•	•	•			
																														•	•	•	•	•	1	•	•			
																														•	•	1	•	•	•	•	•			
95	5	2				8D	5	3	9D	6	3	99	6	3							81	7	2	91	7	2				•	•	•	•	•	•	•	•			
																														•	•	•	•	•	•	•	•			
			96	5	2	8E	5	3																					•	•	•	•	•	•	•	•	•			
94	5	2				8C	5	3																					•	•	•	•	•	•	•	•	•			
																														N	•	•	•	•	•	•	Z	•		
																														N	•	•	•	•	•	•	Z	•		
																														N	•	•	•	•	•	•	Z	•		
																														N	•	•	•	•	•	•	Z	•		
																														•	•	•	•	•	•	•	•	•		
																														N	•	•	•	•	•	•	Z	•		
																														•	•	•	•	•	•	•	•	•		

APPENDIX

3.11 Machine instructions

Symbol	Contents	Symbol	Contents
IMP	Implied addressing mode	+	Addition
IMM	Immediate addressing mode	−	Subtraction
A	Accumulator or Accumulator addressing mode	*	Multiplication
BIT, A	Accumulator bit addressing mode	/	Division
BIT, A, R	Accumulator bit relative addressing mode	Λ	Logical OR
ZP	Zero page addressing mode	V	Logical AND
BIT, ZP	Zero page bit addressing mode	∨	Logical exclusive OR
BIT, ZP, R	Zero page bit relative addressing mode	—	Negation
ZP, X	Zero page X addressing mode	←	Shows direction of data flow
ZP, Y	Zero page Y addressing mode	X	Index register X
ABS	Absolute addressing mode	Y	Index register Y
ABS, X	Absolute X addressing mode	S	Stack pointer
ABS, Y	Absolute Y addressing mode	PC	Program counter
IND	Indirect absolute addressing mode	PS	Processor status register
		PCH	8 high-order bits of program counter
ZP, IND	Zero page indirect absolute addressing mode	PCL	8 low-order bits of program counter
		ADH	8 high-order bits of address
IND, X	Indirect X addressing mode	ADL	8 low-order bits of address
IND, Y	Indirect Y addressing mode	FF	FF in Hexadecimal notation
REL	Relative addressing mode	nn	Immediate value
SP	Special page addressing mode	zz	Zero page address
C	Carry flag	M	Memory specified by address designation of any addressing mode
Z	Zero flag	M(X)	Memory of address indicated by contents of index register X
I	Interrupt disable flag	M(S)	Memory of address indicated by contents of stack pointer
D	Decimal mode flag	M(ADH, ADL)	Contents of memory at address indicated by ADH and ADL, in ADH is 8 high-order bits and ADL is 8 low-order bits.
B	Break flag	M(00, ADL)	Contents of address indicated by zero page ADL
T	X-modified arithmetic mode flag	Ai	Bit i (i = 0 to 7) of accumulator
V	Overflow flag	Mi	Bit i (i = 0 to 7) of memory
N	Negative flag	OP	Opcode
		n	Number of cycles
		#	Number of bytes

3.12 M35501FP

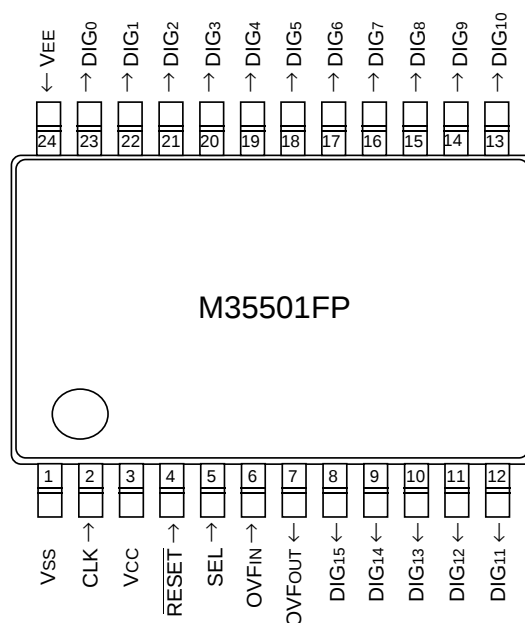
DESCRIPTION

The M35501FP generates digit signals for fluorescent display when connected to the output port of a microcomputer. There are up to 16 digit pins available, and more can be added by connecting additional M35501FPs. The number of fluorescent displays can be increased easily by connecting the M35501FP to the CMOS FLD output pins of an 8-bit microcomputer in MITSUBISHI's 38B5 Group. The M35501FP is suitable for fluorescent display control on household electric appliances, audio products, etc.

FEATURES

- Digit output 16 (maximum)
 - Up to 16 pins can be selected
 - More digits available by connecting additional M35501FPs
 - Output structure: high-breakdown voltage, P-channel open-drain; built-in pull-down resistor between digit output pins and VEE pin
- Power-on reset circuit Built-in
- Power source voltage 4.0 to 5.5 V
- Pull-down power source voltage $V_{CC} - 43\text{ V}$
- Operating temperature range -20 to $85\text{ }^{\circ}\text{C}$
- Package 24P2E
- Power dissipation $250\text{ }\mu\text{W}$ (at 100 kHz operation clock)

PIN CONFIGURATION (TOP VIEW)



Outline: 24P2E-A
24-pin plastic-molded SSOP

Fig. 3.12.1 Pin configuration of M35501FP

APPENDIX

3.12 M35501FP

FUNCTIONAL BLOCK

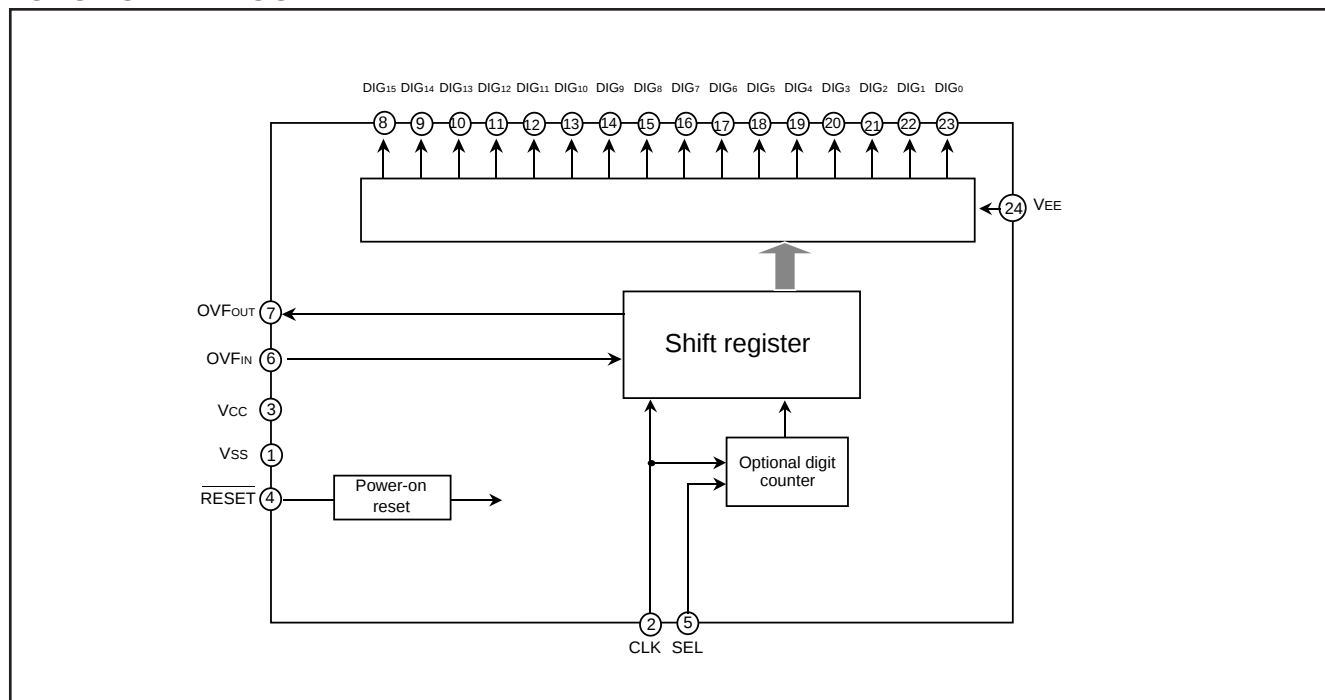


Fig. 3.12.2 Functional block diagram

PIN DESCRIPTION

Table 3.12.1 Pin description

Pin	Name	Function	Output Structure	Fig. No.
Vcc, Vss	Power source input	Apply 4.0–5.5 V to Vcc, and 0V to Vss.	–	–
RESET	Reset input	Reset internal shift register (built-in power-on reset circuit).	CMOS input level Built-in pull-up resistor	3
CLK	Clock input	Digit output varies according to rising edge of clock input.	CMOS input level Built-in pull-down resistor	2
SEL	Select input	Use when specifying the number of digits.	CMOS input level Built-in pull-down resistor	2
OVFin	Overflow signal input	Input "H" when using one M35501FP. Connect to OVFOut pin of additional M35501FPs when using multiple M35501FPs (to use 17 digits or more).	CMOS input level	4
OVFOut	Overflow signal output	Leave open when using one M35501FP. Connect to OVFin pin of additional M35501FPs when using multiple M35501FPs (to use 17 digits or more).	CMOS output	5
DIG15–DIG0	Digit output	Output the digit output waveform of fluorescent display. Leave open when not in use (Vee level output).	High-breakdown-voltage P-channel open-drain output Built-in pull-down resistor	1
Vee	Pull-down power source input	Apply voltage to DIG0–DIG15 pull-down resistors.	–	–

PORT BLOCK

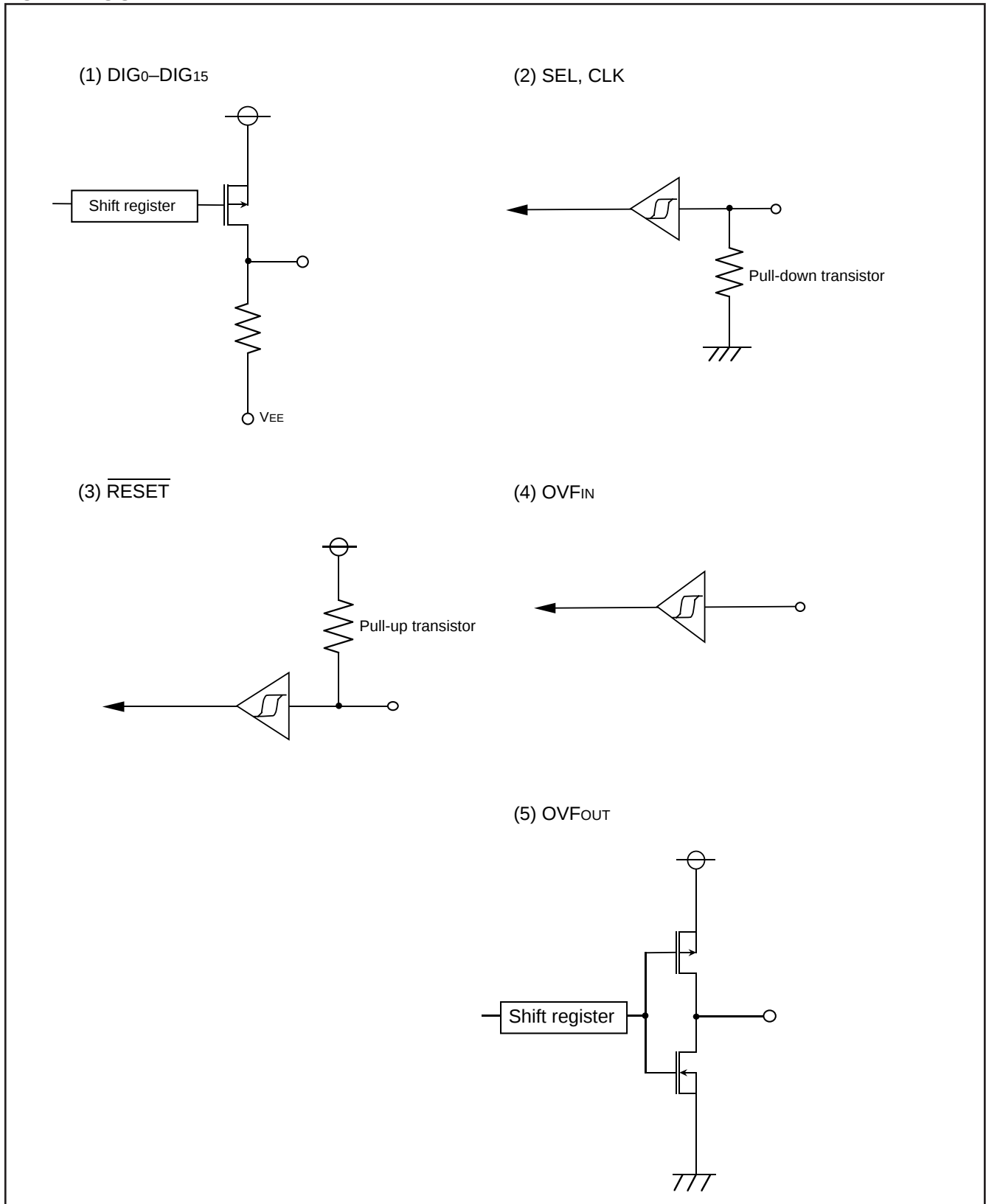


Fig. 3.12.3 Port block diagram

APPENDIX

3.12 M35501FP

USAGE

Three usages of the M35501FP are described below.

(1) 16-Digit Mode: 16 digits selected

The number of digits is set to 16 by fixing the OVFIN pin to "H" and the SEL pin to "L." Figure 3.12.5 shows the output waveform.

(2) Optional Digit Mode: 1-16 digits selectable

When the number of CLK pin rising edges during an "H" period of the SEL pin is n and the OVFIN pin is fixed to "H," the number of digits set is n . If n is 16 or more, all 16 digits are set. Figure 3.12.6 shows the output waveform.

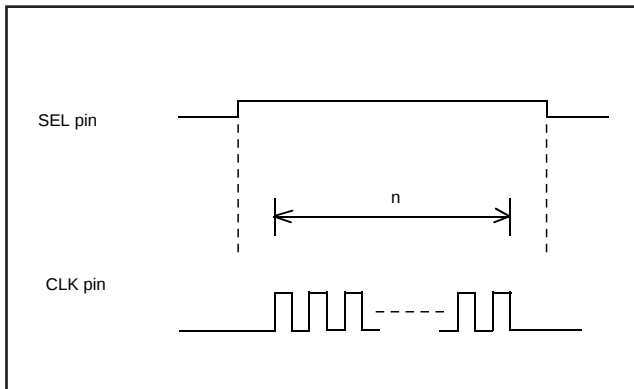


Fig. 3.12.4 Digit setting

(3) Cascade Mode: 17 digits or more selectable

17 digits or more can be used by connecting two M35501FPs or more. Figure 3.12.7 shows an example using three M35501FPs, offering 33 to 48 digit outputs.

Cascade mode will not operate if all M35501FPs are in 16-digit mode (SEL = "L"). Use the most significant M35501FP in the optional digit mode for DIG output. Figure 3.12.8 shows the output waveform.

DIGIT OUTPUT WAVEFORM

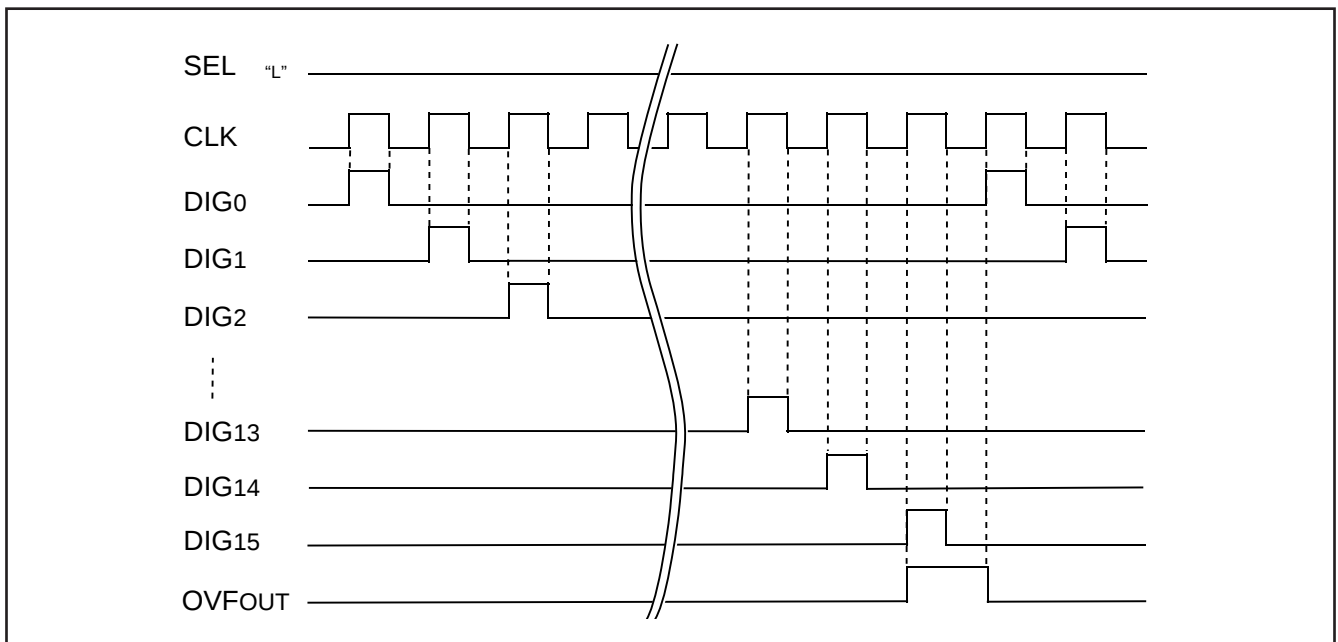


Fig. 3.12.5 16-digit mode output waveform

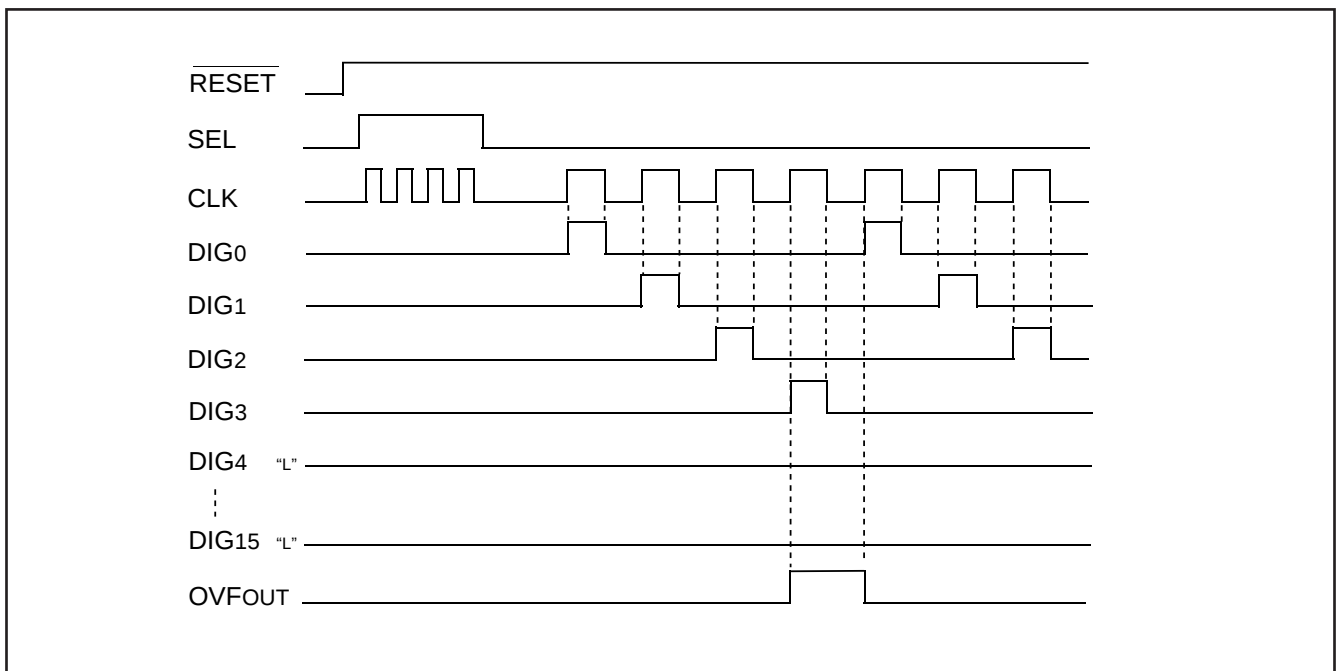


Fig. 3.12.6 Optional digit mode output waveform

APPENDIX

3.12 M35501FP

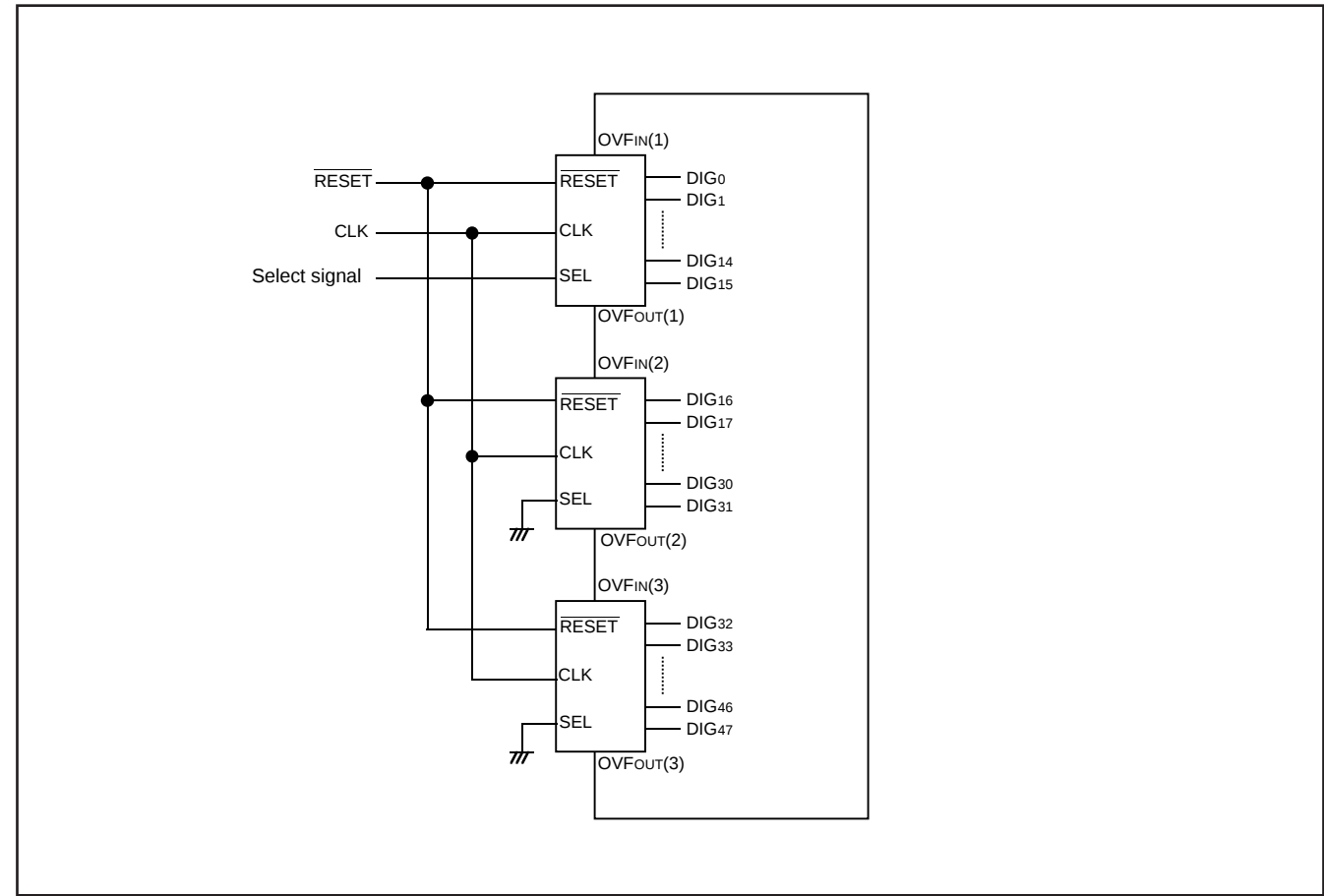


Fig. 3.12.7 Cascade mode connection example: 17 digits or more selected

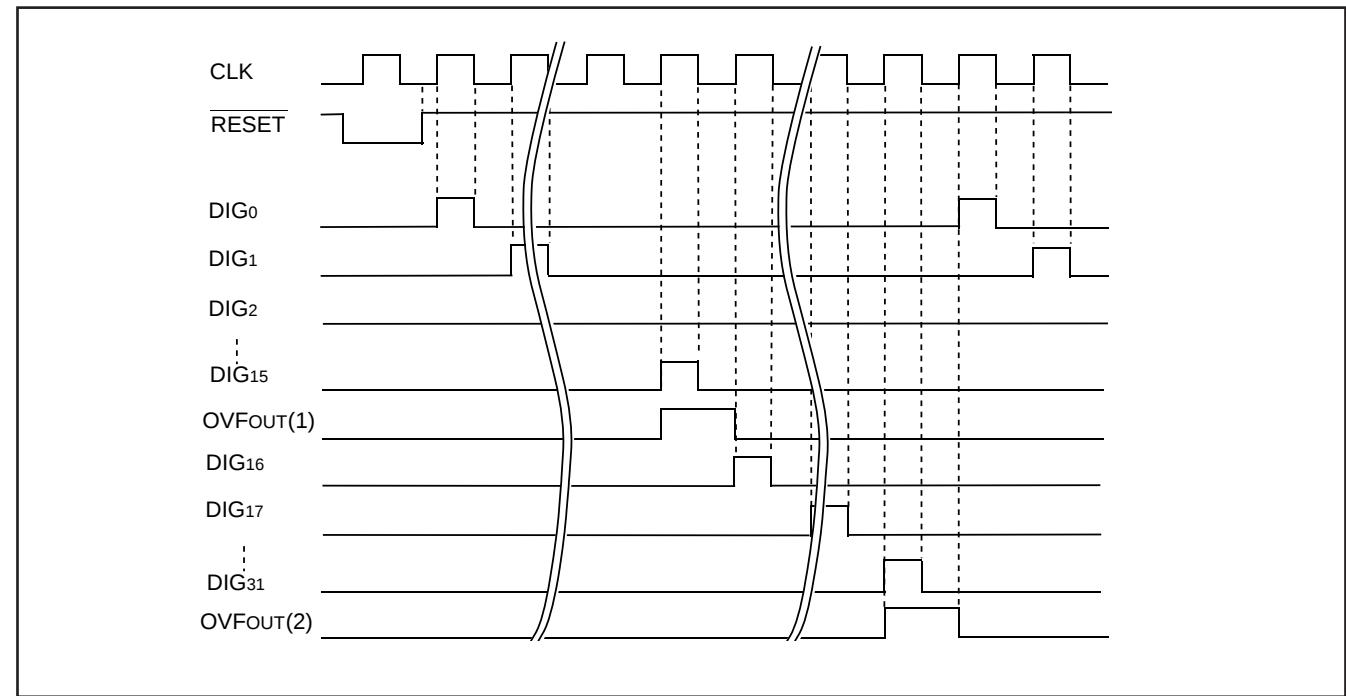


Fig. 3.12.8 Cascade mode output waveform

The number of fluorescent displays can be increased by connecting the M35501FP to the CMOS FLD output pins on a 38B5 Group microcomputer.

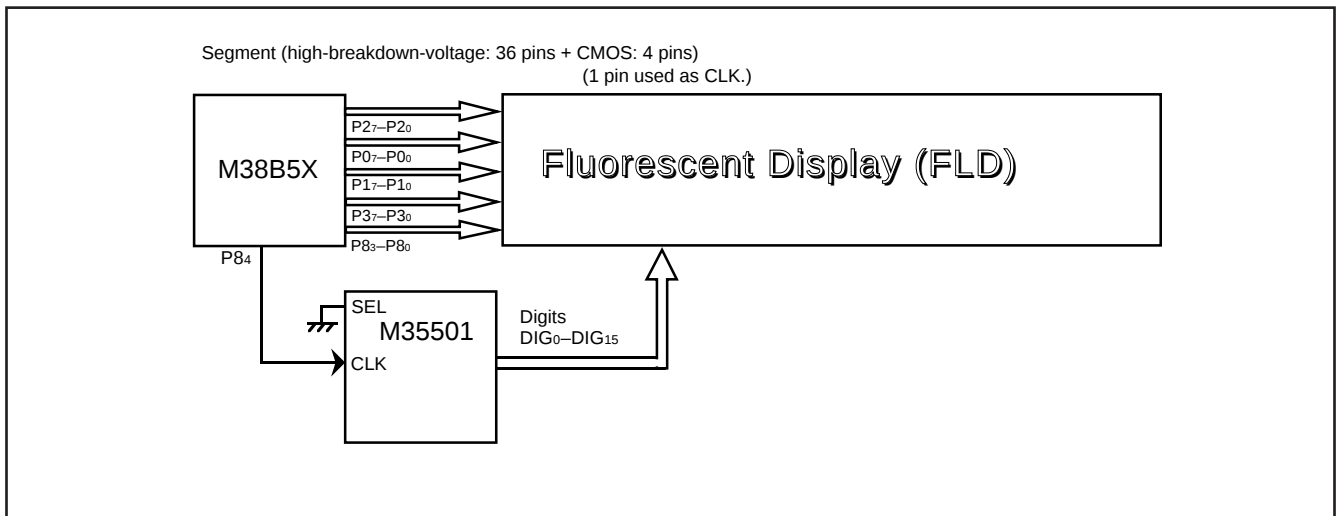


Fig. 3.12.9 Connection example with 38B5 Group microcomputer (1 to 16 digits)

This FLD controller can control up to 32 digits using the 32 timing mode of the 38B5 Group microcomputer.

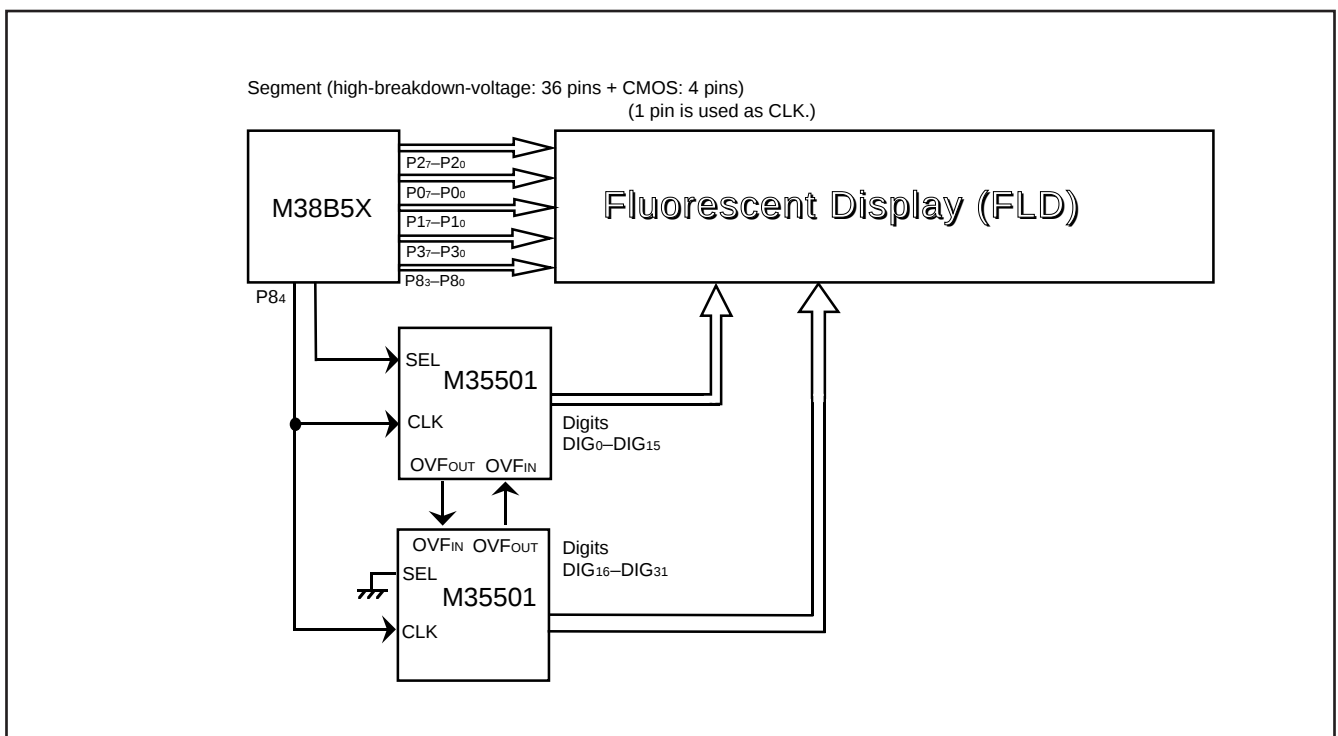


Fig. 3.12.10 Connection example with 38B5 Group microcomputer (17 to 32 digits)

APPENDIX

3.12 M35501FP

RESET CIRCUIT

To reset the controller, the $\overline{\text{RESET}}$ pin should be held at “L” for 2 μs or more. Reset is released when the $\overline{\text{RESET}}$ pin is returned to “H” and the power source voltage is between 4.0 V and 5.5 V.

- Notes**1: Perform the reset release when CLK input signal is “L.”
2: When setting the number of digits by SEL signal, optional digit counter is set to “0” by reset.

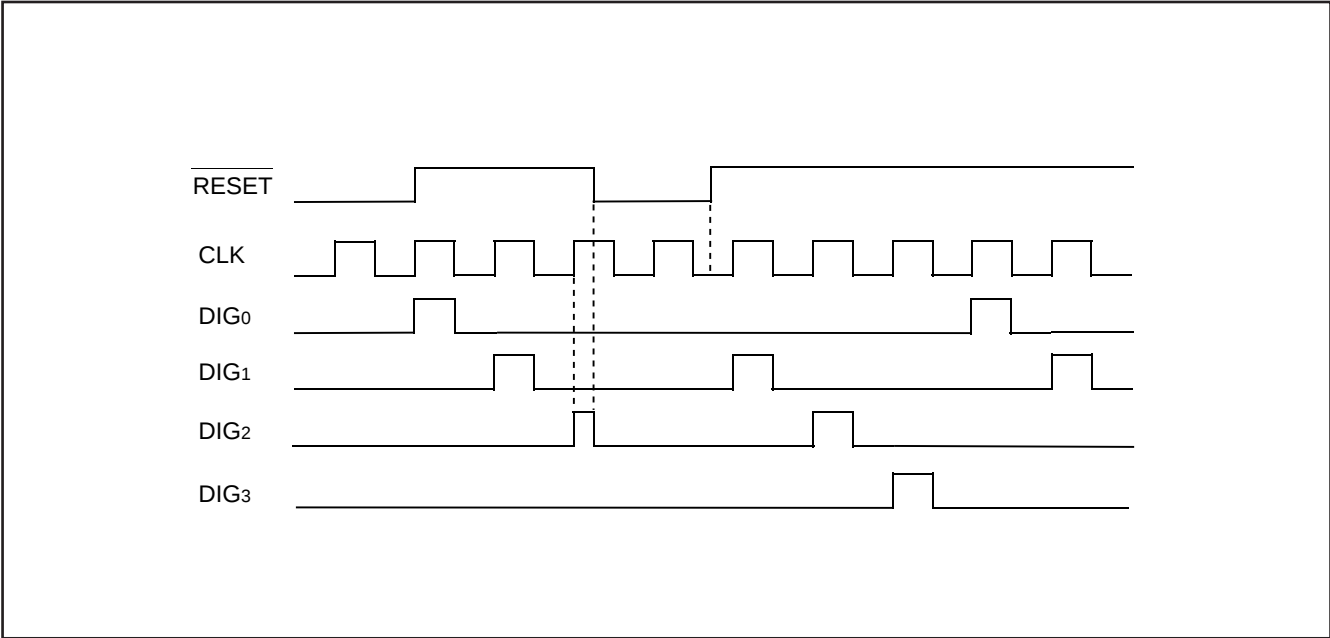


Fig. 3.12.11 Digit output waveform when reset signal is input

POWER-ON RESET

Reset can be performed automatically during power on (power-on reset) by the built-in power-on reset circuit. When using this circuit, set 100 μ s or less for the period in which it takes to reach minimum operation guaranteed voltage from reset.

If the rising time exceeds 100 μ s, connect the capacitor between the RESET pin and Vss at the shortest distance. Consequently, the RESET pin should be held at "L" until the minimum operation guaranteed voltage is reached.

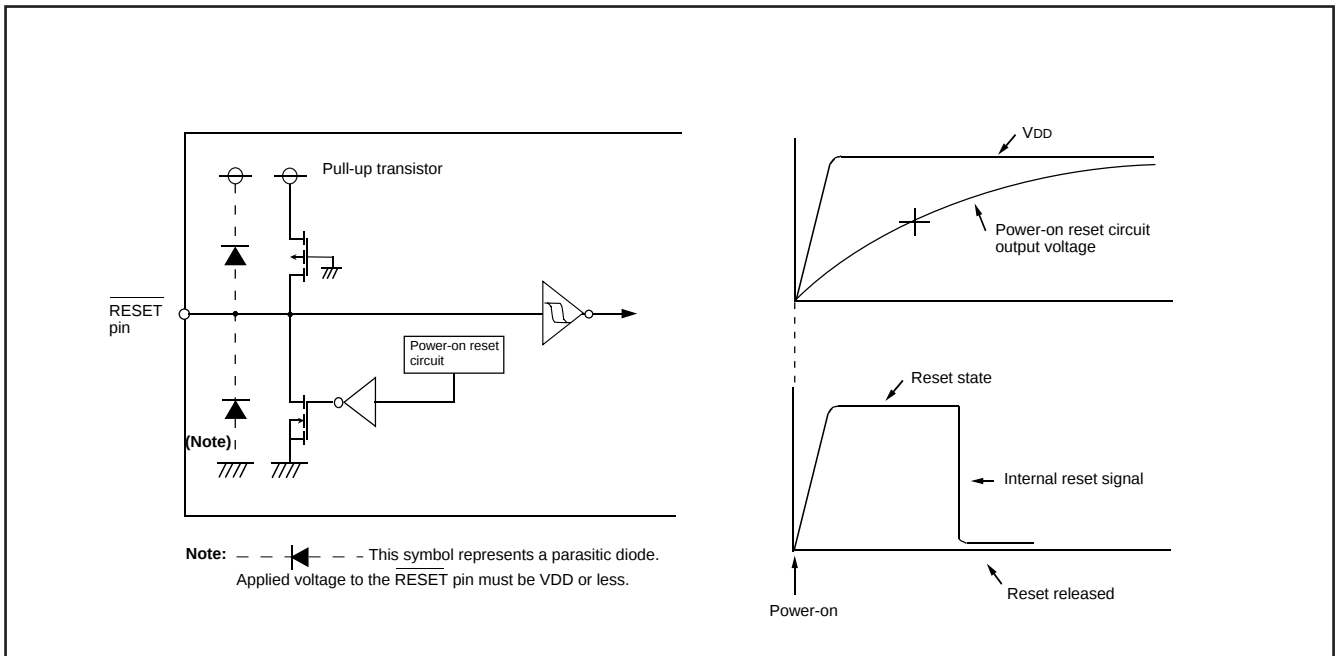


Fig. 3.12.12 Power-on reset circuit

APPENDIX

3.12 M35501FP

Table 3.12.2 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Power source voltage	•All voltages are based on V_{SS}. •Output transistors are off.	–0.3 to 7.0	V
V _{EE}	Pull-down power source voltage		V _{CC} –45 to V _{CC} +0.3	V
V _I	Input voltage CLK, SEL, OVFIN		–0.3 to V _{CC} +0.3	V
V _I	Input voltage RESET		–0.3 to V _{CC} +0.3	V
V _O	Output voltage DIG0–DIG15		V _{CC} –45 to V _{CC} +0.3	V
V _O	Output voltage OVFOUT		–0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _a = 25 °C	250	mW
T _{opr}	Operating temperature		–20 to 85	°C
T _{stg}	Storage temperature		–40 to 125	°C

Table 3.12.3 Recommended operating conditions (V_{CC} = 4.0 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Power source voltage	4.0	5.0	5.5	V
V _{SS}	Power source voltage		0		V
V _{EE}	Pull-down power source voltage	V _{CC} –43		V _{SS}	V
V _{IH}	“H” input voltage CLK, SEL, OVFIN	0.8V _{CC}		V _{CC}	V
V _{IH}	“H” input voltage RESET	0.8V _{CC}		V _{CC}	V
V _{IL}	“L” input voltage CLK, SEL, OVFIN	0		0.2V _{CC}	V
V _{IL}	“L” input voltage RESET	0		0.2V _{CC}	V

Table 3.12.4 Recommended operating conditions (V_{CC} = 4.0 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
I _{OH} (peak)	“H” peak output current DIG0 – DIG15 (Note 1)			–36	mA
I _{OH} (peak)	“H” peak output current OVFOUT (Note 1)			–10	mA
I _{OL} (peak)	“L” peak output current OVFOUT (Note 1)			10	mA
I _{OH} (avg)	“H” average current DIG0 – DIG15 (Note 2)			–18	mA
I _{OH} (avg)	“H” average current OVFOUT (Note 2)			–5.0	mA
I _{OL} (avg)	“L” average current OVFOUT (Note 2)			5.0	mA
CLK	Clock input frequency			2	MHz

Notes 1: The peak output current is the peak current flowing in each port.

2: The average output current is an average value measured over 100 ms.

Table 3.12.5 Electrical characteristics ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	DIG output DIG0–DIG15	$I_{OH} = -18$ mA	$V_{CC} - 2.0$			V
V_{OH}	"H" output voltage	$\overline{OVFOUT}$	$I_{OH} = -10$ mA	$V_{CC} - 2.0$			V
V_{OL}	"L" output voltage	$\overline{OVFOUT}$	$I_{OL} = 10$ mA			2.0	V
$V_{T+} - V_{T-}$	Hysteresis	CLK, $\overline{OVFIN}$ RESET	$V_{CC} = 5.0$ V		0.4		V
I_{IH}	"H" input current	$\overline{OVFIN}$ RESET	$V_I = V_{CC}$			5.0	μA
I_{IH}	"H" input current	CLK, SEL	$V_I = V_{CC}$ $V_{CC} = 5.0$ V	30	70	140	μA
I_{IL}	"L" input current	$\overline{OVFIN}$ CLK, SEL	$V_I = V_{SS}$			-5.0	μA
I_{IL}	"L" input current	RESET	$V_I = V_{SS}$ $V_{CC} = 5.0$ V	-60	-130	-185	μA
I_{LOAD}	Output load current	DIG0 – DIG15	$V_{EE} = V_{CC} - 43$ V $V_{OL} = V_{CC}$ Output transistors are off.	500	650	800	μA
I_{LEAK}	Output leakage current	DIG0–DIG15	$V_{EE} = V_{CC} - 43$ V $V_{OL} = V_{CC} - 43$ V Output transistors are off.			-10	μA
I_{CC}	Power source	$V_{CC} = 5.0$ V, CLK = 100 kHz Output transistors are off.			50		μA

APPENDIX

3.12 M35501FP

Table 3.12.6 Timing requirements (Vcc = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input “L” pulse width	2			μs
tc(CLK)	Clock input cycle time	500			ns
twH(CLK)	Clock input “H” pulse width	200			ns
twL(CLK)	Clock input “L” pulse width	200			ns
tsu(SEL)	Select input setup time	500			ns
th(SEL)	Select input hold time	500			ns
th(CLK)	Clock input setup time	500			ns

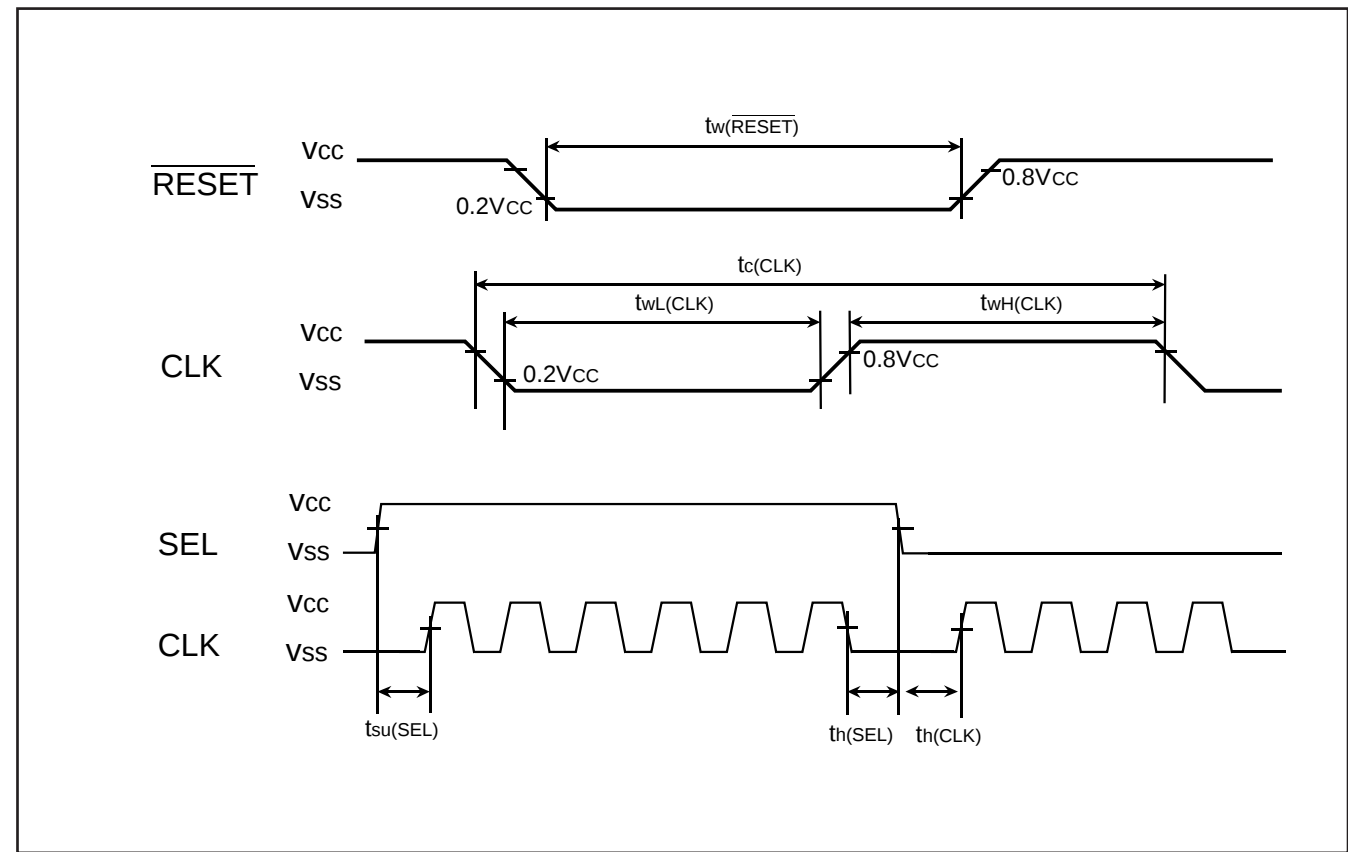


Fig. 3.12.13 Timing diagram

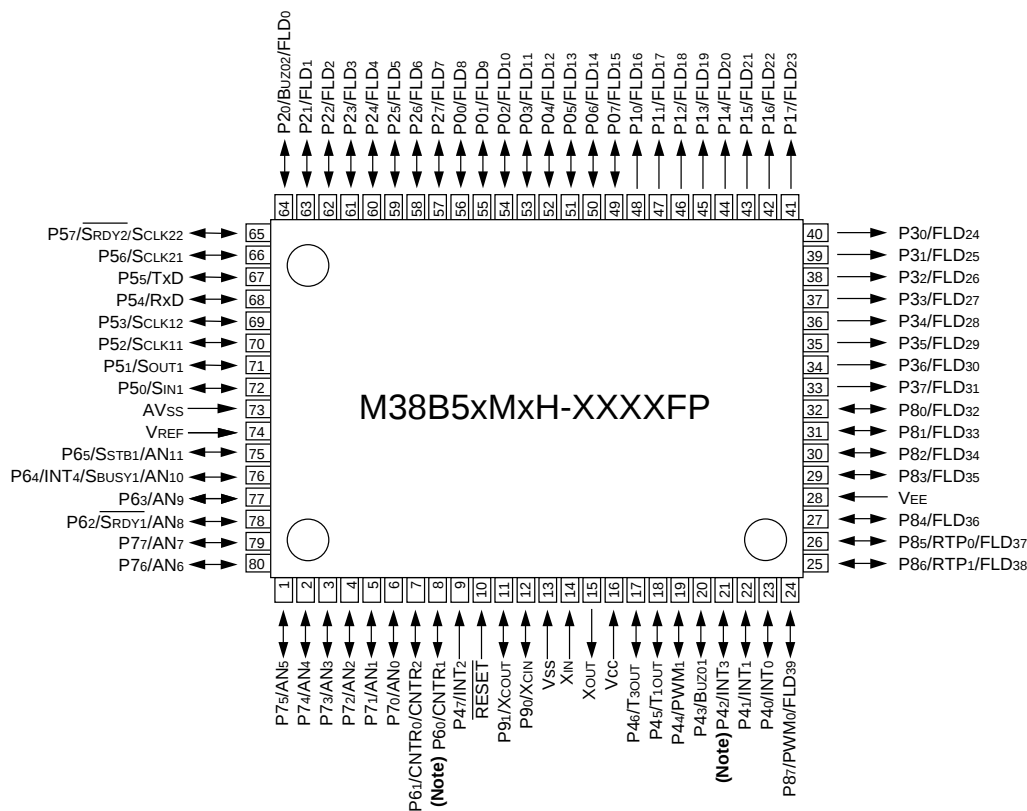
3.13 SFR memory map

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Timer 1 (T1)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	Timer 2 (T2)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 3 (T3)
0003 ₁₆		0023 ₁₆	Timer 4 (T4)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer 5 (T5)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer 6 (T6)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	PWM control register (PWMCON)
0007 ₁₆		0027 ₁₆	Timer 6 PWM register (T6PWM)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer 12 mode register (T12M)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Timer 34 mode register (T34M)
000A ₁₆	Port P5 (P5)	002A ₁₆	Timer 56 mode register (T56M)
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	Watchdog timer control register (WDTCON)
000C ₁₆	Port P6 (P6)	002C ₁₆	Timer X (low-order) (TXL)
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	Timer X (high-order) (TXH)
000E ₁₆	Port P7 (P7)	002E ₁₆	Timer X mode register 1 (TXM1)
000F ₁₆	Port P7 direction register (P7D)	002F ₁₆	Timer X mode register 2 (TXM2)
0010 ₁₆	Port P8 (P8)	0030 ₁₆	Interrupt interval determination register (IID)
0011 ₁₆	Port P8 direction register (P8D)	0031 ₁₆	Interrupt interval determination control register (IIDCON)
0012 ₁₆	Port P9 (P9)	0032 ₁₆	A-D control register (ADCON)
0013 ₁₆	Port P9 direction register (P9D)	0033 ₁₆	A-D conversion register (low-order) (ADL)
0014 ₁₆	PWM register (high-order) (PWMH)	0034 ₁₆	A-D conversion register (high-order) (ADH)
0015 ₁₆	PWM register (low-order) (PWM L)	0035 ₁₆	
0016 ₁₆	Baud rate generator (BRG)	0036 ₁₆	
0017 ₁₆	UART control register (UARTCON)	0037 ₁₆	
0018 ₁₆	Serial I/O1 automatic transfer data pointer (SIO1DP)	0038 ₁₆	
0019 ₁₆	Serial I/O1 control register 1 (SIO1CON1)	0039 ₁₆	Interrupt source switch register (IFR)
001A ₁₆	Serial I/O1 control register 2 (SIO1CON2)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	Serial I/O1 register/Transfer counter (SIO1)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Serial I/O1 control register 3 (SIO1CON3)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	Serial I/O2 control register (SIO2CON)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆	Serial I/O2 status register (SIO2STS)	003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	Serial I/O2 transmit/receive buffer register (TB/RB)	003F ₁₆	Interrupt control register 2 (ICON2)
0EF0 ₁₆	Pull-up control register 1 (PULL1)	0EF8 ₁₆	FLD data pointer (FLDDP)
0EF1 ₁₆	Pull-up control register 2 (PULL2)	0EF9 ₁₆	Port P0FLD/port switch register (P0FPR)
0EF2 ₁₆	P1FLDRAM write disable register (P1FLDRAM)	0EFA ₁₆	Port P2FLD/port switch register (P2FPR)
0EF3 ₁₆	P3FLDRAM write disable register (P3FLDRAM)	0EFB ₁₆	Port P8FLD/port switch register (P8FPR)
0EF4 ₁₆	FLDC mode register (FLDM)	0EFC ₁₆	Port P8FLD output control register (P8FLDCON)
0EF5 ₁₆	Tdisp time set register (TDISP)	0EFD ₁₆	Buzzer output control register (BUZCON)
0EF6 ₁₆	Toff1 time set register (TOFF1)	0EFE ₁₆	
0EF7 ₁₆	Toff2 time set register (TOFF2)	0EFF ₁₆	

APPENDIX

3.14 Pin configuration

3.14 Pin configuration



Note: In the mask option type P, INT3 and CNTR1 cannot be used.

(Top view)

Package type: 80P6N-A
80-pin plastic molded QFP

**MITSUBISHI SEMICONDUCTORS
USER'S MANUAL
38B5 Group**

Nov. First Edition 1998

Edited by
Committee of editing of Mitsubishi Semiconductor USER'S MANUAL

Published by
Mitsubishi Electric Corp., Semiconductor Marketing Division

This book, or parts thereof, may not be reproduced in any form without permission of Mitsubishi Electric Corporation.

©1998 MITSUBISHI ELECTRIC CORPORATION

User's Manual

38B5 Group

Renesas Technology Corp.
Nippon Bldg., 6-2, Otemachi 2-chome, Chiyoda-ku, Tokyo, 100-0004 Japan

