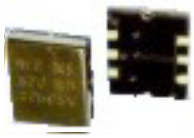
GF64 CMOS VCXO

11.4 x 9.6 x 4.7mm 6 pad SMD

- **Frequency range 50.01MHz to 200MHz (15pF load)**
- **Frequency range 50.01MHz to 320MHz (10pF load)**
- **LVCMOS Output**
- **Supply Voltage 3.3 VDC**
- **Ultra low jitter less than 1ps**

RoHS COMPLIANT 2002 / 95 /EC



DESCRIPTION

GF64 VCXOs, are packaged in an industry-standard, 6 pad, 11.4mm x 9.6mm x 4.7mm SMD package. GF64 VCXOs provide excellent phase jitter performance, less than 1ps.

SPECIFICATION

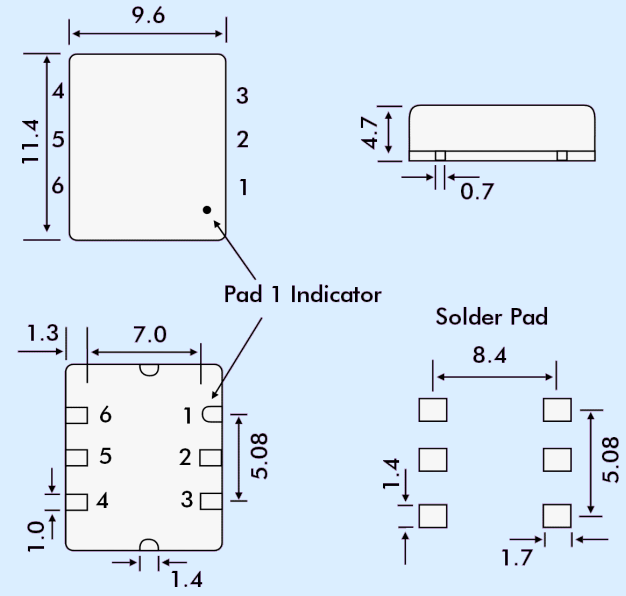
Frequency Range	
Load 15pF:	50.01MHz to 200.0MHz
Load 10pF:	50.01MHz to 320.0MHz
Supply Voltage:	3.3 VDC ±5%
Output Logic:	LVCMOS
Integrated Phase Jitter:	0.4ps typical, 0.5ps maximum (for 155.250MHz)
Period Jitter RMS:	3.0ps typical (for 155.250MHz)
Period Jitter Peak to peak:	20ps typical (for 155.250MHz)
Phase Noise:	*See table below*
Initial Frequency Accuracy:	Tune to the nominal frequency with Vc= 1.65 ±0.2VDC
Output Voltage HIGH (1):	90% Vdd minimum
Output Voltage LOW (0):	10% Vdd maximum
Pulling Range:	From ±30ppm to ±150ppm
Temperature Stability:	*See table*
Output Load:	15pF
Start-up Time:	10ms maximum, 5ms typical
Duty Cycle:	50% ±5% measured at 50% Vdd
Rise/Fall Times:	0.7ns typical (15pF load)
Current Consumption	
<100MHz:	30mA maximum (15pF load)
>100MHz:	40mA maximum (15pF load)
Linearity:	10% maximum, 6% typical
Modulation Bandwidth:	25kHz minimum
Input Impedance:	60kΩ minimum
Slope Polarity: (Transfer function)	Monotonic and Positive. *(An increase of control voltage always increases output frequency.)*
Storage Temperature:	-50° to +100°C
Ageing:	±5ppm per year maximum
Enable/Disable (Tristate):	Pad 2, Enable high or 70% Vdd min. applied to Tri-state pad to enable output. 30% Vdd max. to disable output (high impedance)
RoHS Status:	Fully compliant

FREQUENCY STABILITY

Stability Code	Stability ±ppm	Temp. Range
A	25	0°~+70°C
B	50	0°~+70°C
C	100	0°~+70°C
D	25	-40°~+85°C
E	50	-40°~+85°C
F	100	-40°~+85°C

If non-standard frequency stability is required
Use 'I' followed by stability, i.e. I20 for ±20ppm

OUTLINE & DIMENSIONS



Pad Connections

1 Voltage Control (rounded pad)
2 Tri-state*
3 Ground
4 Output
5 Tristate*
6 Supply Voltage

*Pads 2 and 5 are connected internally

PHASE NOISE

Offset	Frequency 155.25MHz
10Hz	-62dBc/Hz
100Hz	-92dBc/Hz
1kHz	-120dBc/Hz
10kHz	-132dBc/Hz
100kHz	-128dBc/Hz
1MHz	-140dBc/Hz
10MHz	-150dBc/Hz

PART NUMBER SCHEDULE

Example: 3GF64B-80N-156.25

Supply Voltage
3 = +3.3V
Series Designator
GF64
Stability over temperature range
(See table)
Pullability in ±ppm
Pullability determinator
N = minimum
M = maximum
T = Typical
Frequency in MHz

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