

2SK1764

Silicon N Channel MOS FET

REJ03G0970-0200
(Previous: ADE-208-1317)
Rev.2.00
Sep 07, 2005

Application

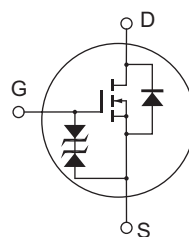
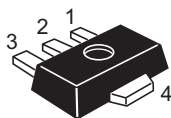
- Low frequency amplifier
- High speed switching

Features

- Low on-resistance
- High speed switching
- 4 V Gate drive device can be driven from 5 V source
- Suitable for switching regulator, DC-DC converter

Outline

RENESAS Package code: PLZZ0004CA-A
(Package name: UPAK[®])



1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is "KY".

*UPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	60	V
Gate to source voltage	V_{GS}	± 20	V
Drain current	I_D	2	A
Drain peak current	$I_{D(pulse)}^{*1}$	4	A
Body to drain diode reverse drain current	I_{DR}	2	A
Channel power dissipation	P_{ch}^{*2}	1	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 100 \mu s$, duty cycle $\leq 10 \%$

2. Value on the alumina ceramic board (12.5 x 20 x 0.7 mm)

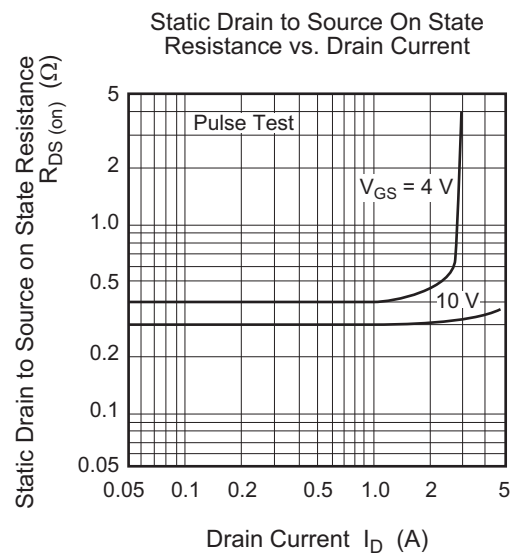
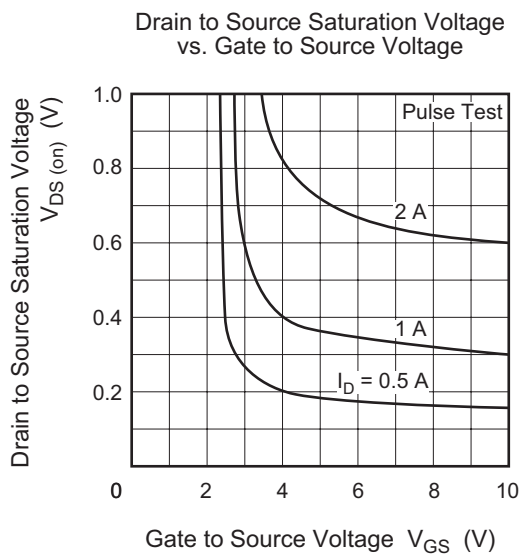
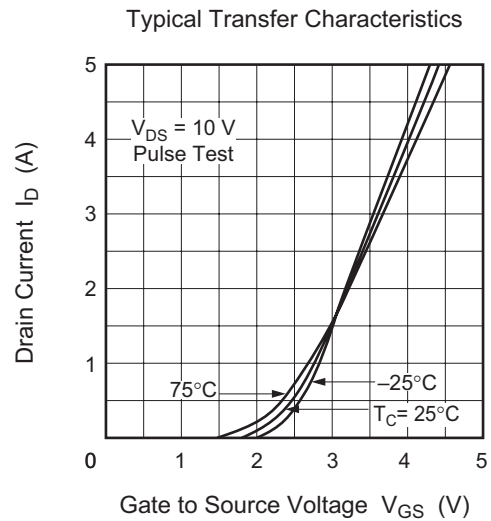
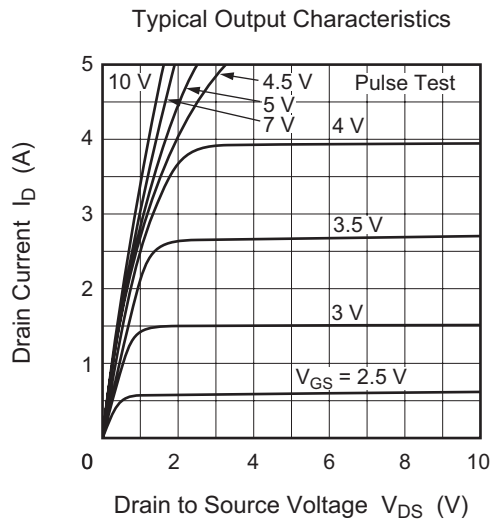
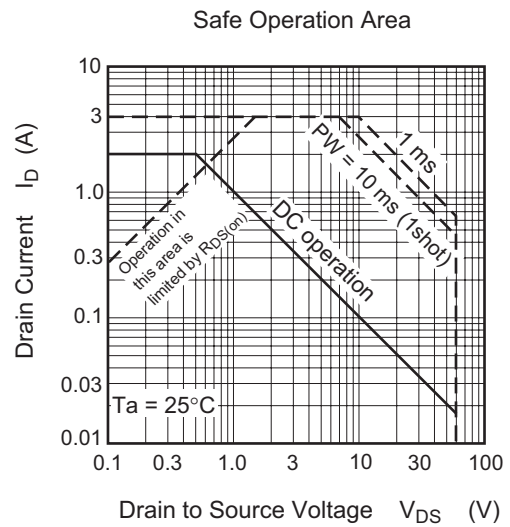
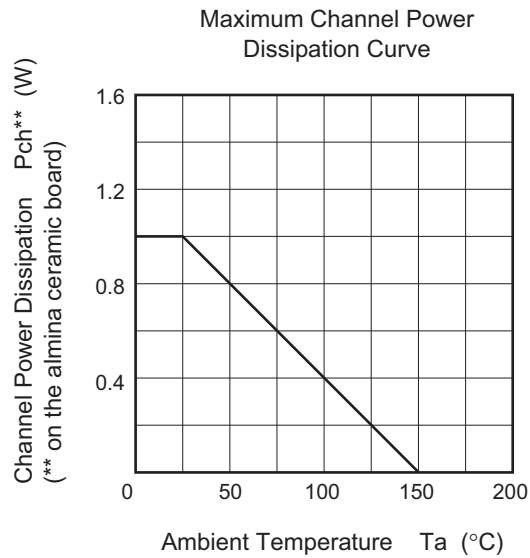
Electrical Characteristics

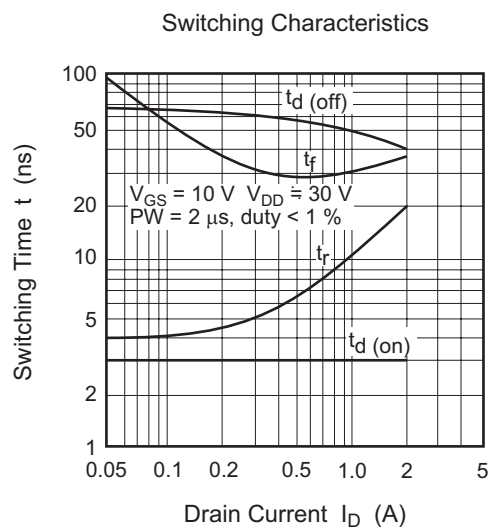
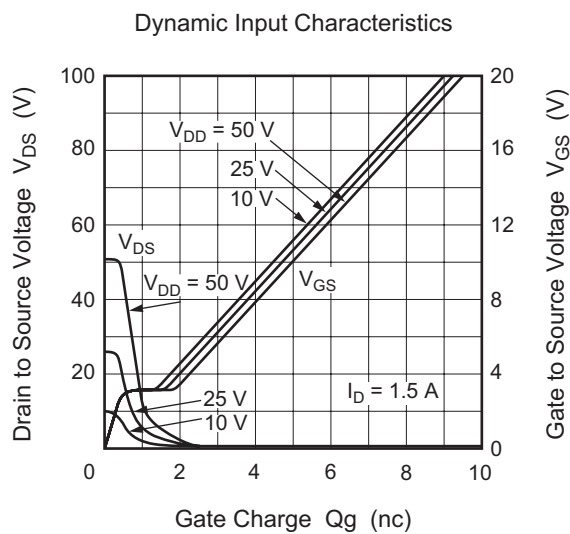
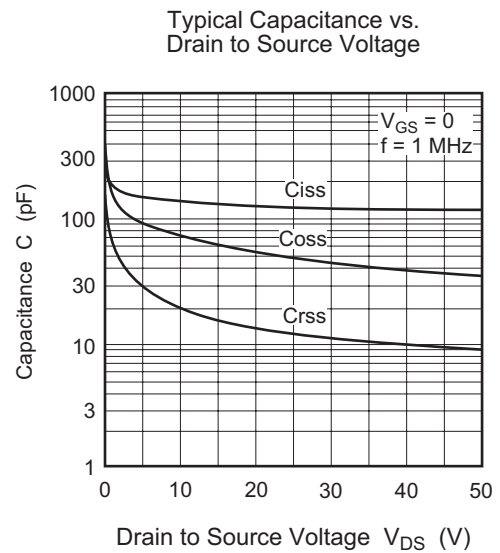
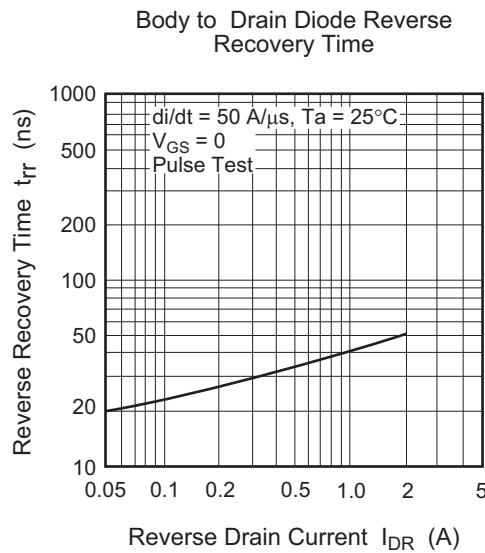
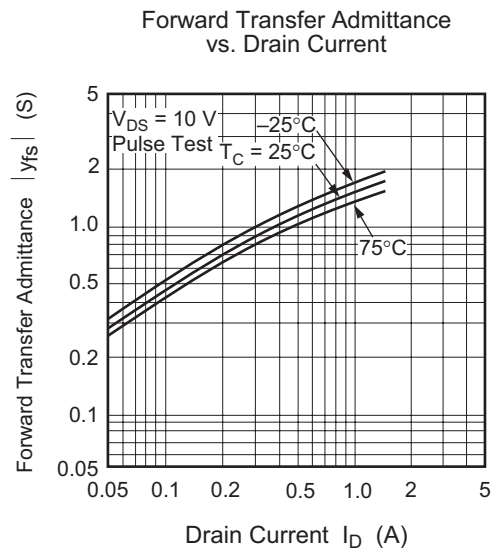
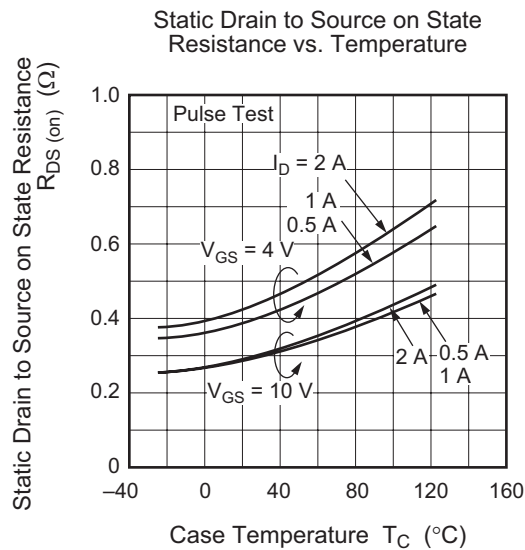
(Ta = 25°C)

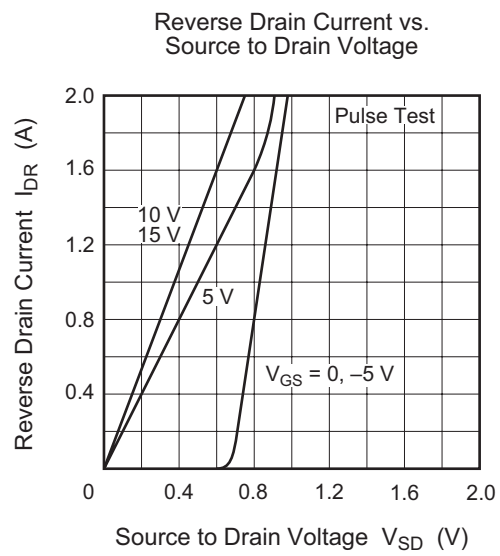
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1	—	2	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Drain to source cutoff current	I_{DSS}	—	—	10	μA	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff current	I_{GSS}	—	—	± 5	μA	$V_{GS} = \pm 15 \text{ V}$, $V_{DS} = 0$
Static drain to source on state resistance	$R_{DS(on)1}$	—	0.3	0.45	Ω	$V_{GS} = 10 \text{ V}$, $I_D = 1 \text{ A}^{*3}$
Static drain to source on state resistance	$R_{DS(on)2}$	—	0.4	0.60	Ω	$V_{GS} = 4 \text{ V}$, $I_D = 1 \text{ A}^{*3}$
Forward transfer admittance	$ y_{fs} $	0.9	1.7	—	S	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ A}^{*3}$
Input capacitance	C_{iss}	—	140	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	75	—	pF	
Reverse transfer capacitance	C_{rss}	—	20	—	pF	
Turn on time	t_{on}	—	18	—	ns	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ A}^{*3}$, $R_L = 30 \Omega$
Turn off time	t_{off}	—	80	—	ns	

Note: 3. Pulse Test

Main Characteristics







Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]	Unit: mm
SC-62	PLZZ0004CA-A	UPAK / UPAKV	0.050g	

The drawing shows three views of the package: top, side, and end. The top view shows a rectangular package with a central circular feature of diameter $\phi 1$. Dimensions include a total width of 4.5 ± 0.1 mm, a maximum width of 1.8 mm, a height of 0.4 mm, and a central feature diameter of $\phi 1$. The side view shows a maximum height of 1.5 ± 0.1 mm and a maximum width of 0.44 mm. The end view shows a maximum width of 1.5 mm and a maximum height of 0.44 mm. Other dimensions include 0.53 Max, 0.48 Max, 1.5 , 3.0 , 0.8 Min, 2.5 ± 0.1 , and 4.25 Max.

Ordering Information

Part Name	Quantity	Shipping Container
2SK1764KYTL-E	3000 pcs	Taping, $\phi 178$ mm Reel
2SK1764KYTR-E	3000 pcs	Taping, $\phi 178$ mm Reel

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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