

8 pin DIL VCXO

- Frequency range 60MHz to 240MHz
- LVPECL Output
- Supply Voltage 3.3 VDC
- Phase jitter 0.2ps typical
- Pull range from $\pm 30\text{ppm}$ to $\pm 150\text{ppm}$

DESCRIPTION

GPA576 VCXOs are packaged in a 6 pad 7mm x 5mm SMD package. Typical phase jitter for GPA series VCXOs is 0.2 ps. Output is LVPECL. Applications include phase lock loop, SONET/ATM, set-top boxes, MPEG, audio/video modulation, video game consoles and HDTV.

SPECIFICATION

Frequency Range:	60.0MHz to 240.0MHz
Supply Voltage:	3.3 VDC $\pm 5\%$
Output Logic:	LVPECL
RMS Period Jitter	
60.0MHz ~ 120MHz:	2.5ps typical
120MHz ~ 240MHz:	4.7ps typical
Peak to Peak Jitter	
60.0MHz ~ 120MHz:	17.5ps typical
120MHz ~ 240MHz:	24.5ps typical
Phase Jitter:	0.2ps typical
Initial Frequency Accuracy:	Tune to the nominal frequency with $V_c = 1.65 \pm 0.2\text{VDC}$
Output Voltage HIGH (1):	Vdd-1.025V minimum Vdd-0.880V maximum
Output Voltage LOW (0):	Vdd-1.810V minimum Vdd-1.620V maximum ($R_L = 50\Omega$ to Vdd-2V)
Pulling Range:	From $\pm 30\text{ppm}$ to $\pm 150\text{ppm}$
Control Voltage Range:	1.65 ± 0.35 Volts
Temperature Stability:	See table
Output Load:	50 Ω into Vdd or Thevenin equiv.
Rise/Fall Times:	0.5ns typ., 0.7ns max. 20% Vdd to 80% Vdd
Duty Cycle:	50% $\pm 5\%$ (Measured at Vdd-1.3V)
Start-up Time:	10ms maximum, 5ms typical
Current Consumption:	75mA maximum at 212.5MHz 80mA maximum at 622.08MHz
Static Discharge Protection:	2kV maximum
Storage Temperature:	-55° to +150°C
Ageing:	$\pm 2\text{ppm}$ per year maximum
Enable/Disable:	Not implemented - 4 pin package
RoHS Status:	Fully compliant or non-compliant

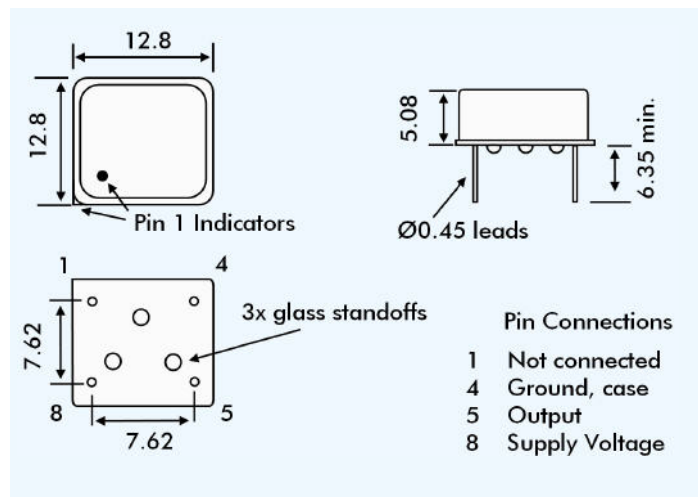
FREQUENCY STABILITY

Stability Code	Stability $\pm\text{ppm}$	Temp. Range
A	25	0°~+70°C
B	50	0°~+70°C
C	100	0°~+70°C
D	25	-40°~+85°C
E	50	-40°~+85°C
F	100	-40°~+85°C

If non-standard frequency stability is required
Use 'I' followed by stability, i.e. I20 for $\pm 20\text{ppm}$



OUTLINE & DIMENSIONS



PART NUMBERING

